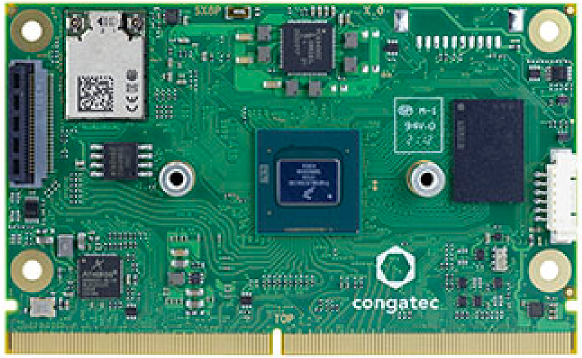

conga-SMX8-Plus

SMARC® 2.1.1 Module with NXP® i.MX 8M Plus Processors

User's Guide

Revision 1.00

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2021-12-17	BEU	• Preliminary release
0.2	2022-07-26	BEU	• Added commercial variant 051301 to table 1 and 5 • Updated camera accessories in table 3 • Updated power mode descriptions in table 4 • Added RTC power consumption values to table 6 • Added CAN/CAN-FD information to section 2.1 "Feature List", 5.8 "CAN Bus", table 1, and table 2 • Added UART bus number for optional WiFi/BT module in section 3 "Block Diagram" • Added QSPI information to section 5.4 "SPI" and 6.3 "SPI NOR Flash" • Updated section 5.1 "PCI Express®" • Removed temperature cliassification from the PHY part number in section 5.11 "Ethernet"
1.00	2023-08-02	BEU	• Updated title page • Updated RoHS Directive • Updated power consumption values in table 5 and 6 • Official release

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Preface

This user's guide provides information about the components, features and connectors available on the conga-SMX8-Plus. It is one of five documents that should be referred to when designing a SMARC® application.

The other reference documents that should be used include the following:

conga-SMX8-Plus Pinout Description (https://git.congatec.com/arm-nxp/imx8-family/doc/cgtimx8_pinlist/tree/cgtsx8p_pinlist)
SMARC® Design Guide 2.1.1 (https://sget.org)
SMARC® Hardware Specification 2.1.1 (https://sget.org)
NXP® i.MX 8M Plus Applications Processor Datasheet for Industrial Products (www.nxp.com)

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Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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Contents

List of Tables

Terminology

Term	Description
°C	Degrees Celsius
µA	Microamp
µs	Microsecond
A	Ampere
AN	Application Note
ARM	Advanced RISC Machine
AVB	Audio Video Bridging
BT	Bluetooth
CAAM	Cryptographic Acceleration and Assurance Module
CMOS	Complementary Metal Oxide Semiconductor
COM	Computer-on-Module
CPU	Central Processing Unit
CSI	Camera Serial Interface
CSP	Cooling Solution Passive
DDR	Double Data Rate
DDRC	Double Data Rate Controller
DP	DisplayPort
DP++	DisplayPort Dual-Mode
DRAM	Dynamic Random Access Memory
DSI	Digital Serial Interface
D-SUB	D-Subminiature
eMMC	embedded Multi-Media Controller
FlexCAN	Flexible Controller Area Network
GB	Gigabyte
GbE	Gigabit Ethernet
GHz	Gigahertz
GND	Ground
GPIO	General-Purpose Input/Output
GPU	Graphics Processing Unit
GTps	Gigatransfers per second
HW	Hardware
HAB	High Assurance Boot
HSP	Heat Spreader
Hz	Hertz
I/O	Input/Output
I²C (I2C)	Inter-Integrated Circuit
I²S (I2S)	Inter-Integrated Circuit Sound
IEEE	Institute of Electrical and Electronics Engineers
JEIDA	Japan Electronic Industries Development Association
JTAG	Joint Test Action Group
KS	Key State
LPDDR	Low-Power Double Data Rate
LVDS	Low-Voltage Differential Signaling
Mbps	Megabits per second
MBps	Megabytes per second
MHz	Megahertz
mm	Millimeter
MMU	Memory Management Unit
mVpp	Millivolts Peak to Peak
MXM	Mobile PCI Express Module
NC	Not Connected
Nm	Newton metre
NXP	NeXt exPerience
OS	Operating System
OTG	On-The-Go
PCB	Printed Circuit Board
PCI Express	Peripheral Component Interconnect Express
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
PN	Part Number
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit-Media Independent Interface
RS-232	Recommended Standard 232
RTC	Real-Time Clock
SAI	Synchronous Audio Interface
SD	Secure Digital
SDIO	Secure Digital Input Output
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SDXC	Secure Digital eXtended Capacity
SGET	Standardization Group for Embedded Technologies e.V
SMARC	Smart Mobility ARChitecture
SoC	System on Chip
SPI	Serial Peripheral Interface
TBD	To Be Defined
UART	Universal Asynchronous Receiver-Transmitter
U-Boot	Universal Boot Loader
UHS	Ultra High Speed
USB	Universal Serial Bus
uSDHC	ultra Secured Digital Host Controller
V	Volt
Vdc	Volts direct current
VESA	Video Electronics Standards Association
W	Watt
Wi-Fi	Wireless Fidelity

1 Introduction

1.1 SMARC® Concept

The Standardization Group for Embedded Technologies e.V (SGET) defined the SMARC® standard for small form factor computer modules that target applications with low power, low cost and high performance. The SMARC® connector and interfaces are optimized for high-speed communication, and are suitable for ARM SoCs and low power x86 SoCs.

The SMARC® standard bridges the gap between the COM Express® standard and the Qseven® standard by offering most of the interfaces defined in the COM Express® specification at a lower power. With a footprint of 82 mm x 50 mm or 82 mm x 80 mm, the SMARC® standard promotes the design of highly integrated, energy efficient systems.

Due to its small size and lower power demands, PC appliance designers can design low cost devices as well as explore a huge variety of product development options—from compact space-saving designs to fully functional systems. This solution allows scalability, product diversification and faster time to market.

1.2 conga-SMX8-Plus

The conga-SMX8-Plus is a Computer On Module (COM) based on the SMARC® Hardware Specification 2.1.1. The conga-SMX8-Plus features an NXP® i.MX 8M Plus applications processor with four Arm® Cortex®-A53 cores and an integrated 2.3 TOPS Neural Processing Unit (NPU) for machine learning applications. The System on Chip (SoC) is manufactured using the 14nm LPC FinFET technology for high computing performance at low power. The conga-SMX8-Plus only requires 2 - 6 W @ 5V for typical applications.

By offering most of the functional requirement for any SMARC® application, the conga-SMX8-Plus provides manufacturers and developers with a platform to jump-start the development of systems and applications based on SMARC® Hardware Specification. Its features and capabilities make it an ideal platform for designing compact, energy-efficient, performance-oriented embedded systems.

1.2.1 Options Information

The conga-SMX8-Plus is available in the following variants:

Table 1 Commercial Variant

PN	051300	051301
NXP® Processor	i.MX 8M Plus Quad	i.MX 8M Plus Quad
Cortex®-A53	4x 1.8 GHz	4x 1.8 GHz
SDRAM	4 GB LPDDR4 @ 2000 MHz (32 bit) with In-line ECC	2 GB LPDDR4 @ 2000 MHz (32 bit) with In-line ECC
eMMC	16 GB	16 GB
CAN	2x CAN	2x CAN

Table 2 Industrial Variants

PN	051320	051321
NXP® Processor	i.MX 8M Plus Quad	i.MX 8M Plus Quad
Cortex®-A53	4x 1.6 GHz	4x 1.6 GHz
SDRAM	4 GB LPDDR4 @ 2000 MHz (32 bit) with In-line ECC	2 GB LPDDR4 @ 2000 MHz (32 bit) with In-line ECC
eMMC	16 GB	16 GB
CAN	2x CAN-FD	2x CAN-FD

1.2.2 Accessories

Table 3 Accessories

PN	Product Name	Comments
48000023	RS-232 adapter cable for conga-ARM module	Adapter cable for ARM console. MOLEX PicoBlade 6 circuit to two D-SUB 9 connector.
020750	conga-SMC1/SMARC-ARM	Compact sized 3.5" Carrier Board for ARM based SMARC 2.1 modules.
007010	conga-SEVAL	Evaluation Carrier Board for SMARC 2.1 modules.
44500041	daA3840-30mc	Basler Dart MIPI Camera daA3840-30mc, 8MP, 30 fps, color, rolling shutter
10000399	FFC BCON, 200mm (Basler MIPI cameras)	FFC cable to connect conga-SMC1 with MIPI camera
10000429	Evetar Lens M118B0418IR F1.8 f4mm 1/1.8" - Lens	Evetar S-mount lens with a fixed focal length of 4 mm and a fixed F-stop of F1.8. With IR-cut filter. (dedicated for Basler dart camera PN 44500041)

2 Specifications

2.1 Feature List

Form Factor	SMARC® Hardware Specification 2.1.1
SoC	NXP® i.MX 8M Plus Quad: 4x Arm® Cortex®-A53 cores @ 1.8 GHz (commercial) or 1.6 GHz (industrial) | 1x Arm® Cortex®-M7 @ 800MHz | NPU 2.3 TOPS | GPU GC7000UL
DRAM	Up to 6 GByte onboard LPDDR4 memory | 4000 MT/s | inline ECC
Ethernet	2x Gbit Ethernet with IEEE 1588 Support (1x with TSN support)
I/O Interfaces	1x dual-role USB 2.0 2x USB 2.0 2x USB 3.0 1x SDIO 3.0 1x PCIe 3.0 2x I²C 1x SPI 3x UART (2x with Handshake) 2x CAN (commercial variants) or CAN-FD (industrial variants) 14x GPIO 1x optional soldered M.2 1216 Wi-Fi/BT
Mass Storage	eMMC5.1 up to 128 GByte | SPI Flash 64Mbit (Uboot)
Sound	2x I²S | HiFi 4 DSP
Graphics	Integrated in SoC | GC7000UL3D graphics with 2 high performance vec4 shaders | GC520L 2D graphic | supports up to 2x1080p60 or 1x4kp30 display resolution | Up to 3 independent displays | VPU up to 1080p60 H.265/H.264 decoding and encoding | OpenGL ES 3.1 | Vulcan® extensions | OpenCL 1.2 FP | OpenVG 1.1
Video Interfaces	1x HDMI® 2.0a 1x dual channel 24-bit LVDS 1x optional MIPI DSI 4-lane instead of second LVDS channel 2x MIPI-CSI 2x integrated Image Signal Processor (ISP) for cameras with up to 12 MP resolution
Features	Watchdog Timer | Cortex-A53 Console | optional JTAG debug interface | High Precision Real Time Clock
AI & Machine Learning	Neural Processing Unit (NPU) with up to 2.3 TOP/s | NXP eIQML SW tools and libraries
Security	Cryptographic Acceleration and Assurance Module | Resource Domain Controller | ARM® TrustZone® | High Assurance Boot support | SHE, Encryption Engine AES-128/192/256, DES/3DES, RC4, RSA4096, TRNG | SHA-1/224/256 | RSA-1024, 2048, 3072, 4096 and secure key storage | side channel attack resistance
Boot Loader	U-Boot
Operating Systems	Linux, Yocto Project | Android
Power Consumption	Low power Cortex-A53 / Cortex-M7 | typ. application 2-6W @ 5V
Temperature Range	Operating Temperature Range: 0 to +60°C commercial grade | -40 to +85°C industrial grade Storage Temperature Range: -40 to +85°C
Humidity	Operating: 10 -90% r. H. non cond. | Storage: 5 -95% r. H. non cond.
Size	82 x 50 mm (3,23" x 1,97")

2.2 Supported Operating Systems

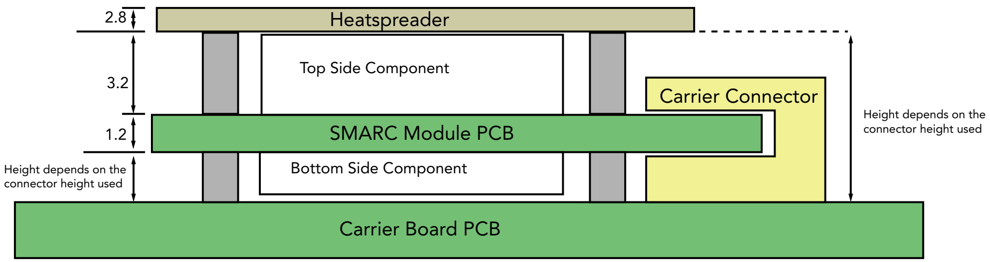
The conga-SMX8-Plus supports the following operating systems:

- Linux® (Yocto Project®)
- Android™

2.3 Mechanical Dimensions

- 82.0 mm x 50.0 mm

The height of the module, heatspreader and stack is shown below:

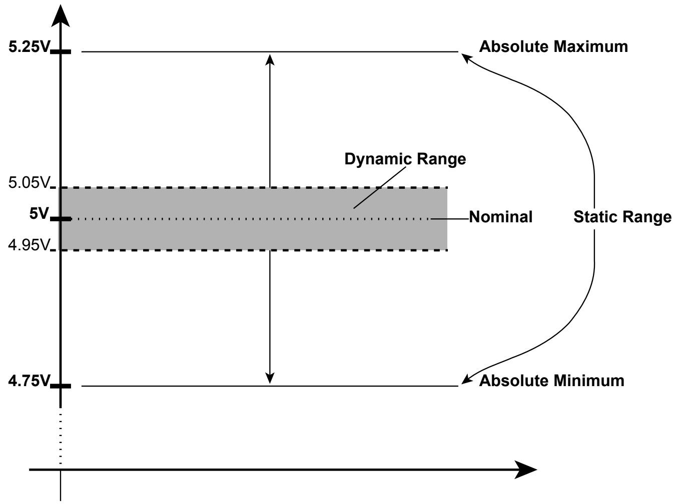


All dimensions are in millimeters

2.4 Standard Power

2.4.1 Supply Voltage

- 4.75 V – 5.25 V



2.4.2 Electrical Characteristics

Power Rail		Min.	Typ.	Max.	Units	Comment
VDD_IN	Voltage	4.75	5.00	5.25	Vdc	
	Ripple	-	-	± 50	mV_{PP}	0-20 MHz
VDD_RTC (optional)	Voltage	2.0	-	3.25	Vdc	

2.4.3 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- Input voltage +5 V
- conga-SMX8-Plus
- conga-SEVAL carrier board
- conga-SMX8-Plus cooling solution

The power consumption values were recorded during the modes described in the table below.

Table 4 Measurement Description

Mode	Description	Comment
Suspend	Lowest power state with external supplies on	For more information about the modes, refer to the AN13054 "i.MX 8M Plus Power Consumption Measurement" available at the NXP® website www.nxp.com.
Idle	IDLE_DEFAULT without display	
100%	100% CPU and GPU workload	The CPU and GPU were stressed to their maximum frequency with stress-ng and Glmark2.
Peak	100% CPU and GPU workload at ~100°C peak power consumption	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.

The table below provides the power consumption values of each conga-SMX8-Plus variant during different operating modes:

Table 5 Power Consumption Values

PN	Memory Size	HW Revision	U-Boot	OS	SoC	Current (A) @ 5 V			
						Suspend	Idle	100%	Peak
051300	4 GB	A.1	2022.04	Yocto Zeus 5.4	i.MX 8M Plus Quad (1.8 GHz)	0.09	0.61	1.17	1.22
051301	2 GB	A.1	2020.04	Yocto Zeus 5.4	i.MX 8M Plus Quad (1.8 GHz)	0.09	0.58	1.11	1.17
051320	4 GB	A.0	2020.04	Yocto Zeus 5.4	i.MX 8M Plus Quad (1.6 GHz)	0.10	0.62	1.08	1.23
051321	2 GB	A.0	2020.04	Yocto Zeus 5.4	i.MX 8M Plus Quad (1.6 GHz)	0.10	0.61	1.05	1.16

2.6 Supply Voltage Battery Power

Table 6 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	1.21 µA
20°C	3V DC	1.27 µA
70°C	3V DC	1.55 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec website at www.congatec.com/support/application-notes*

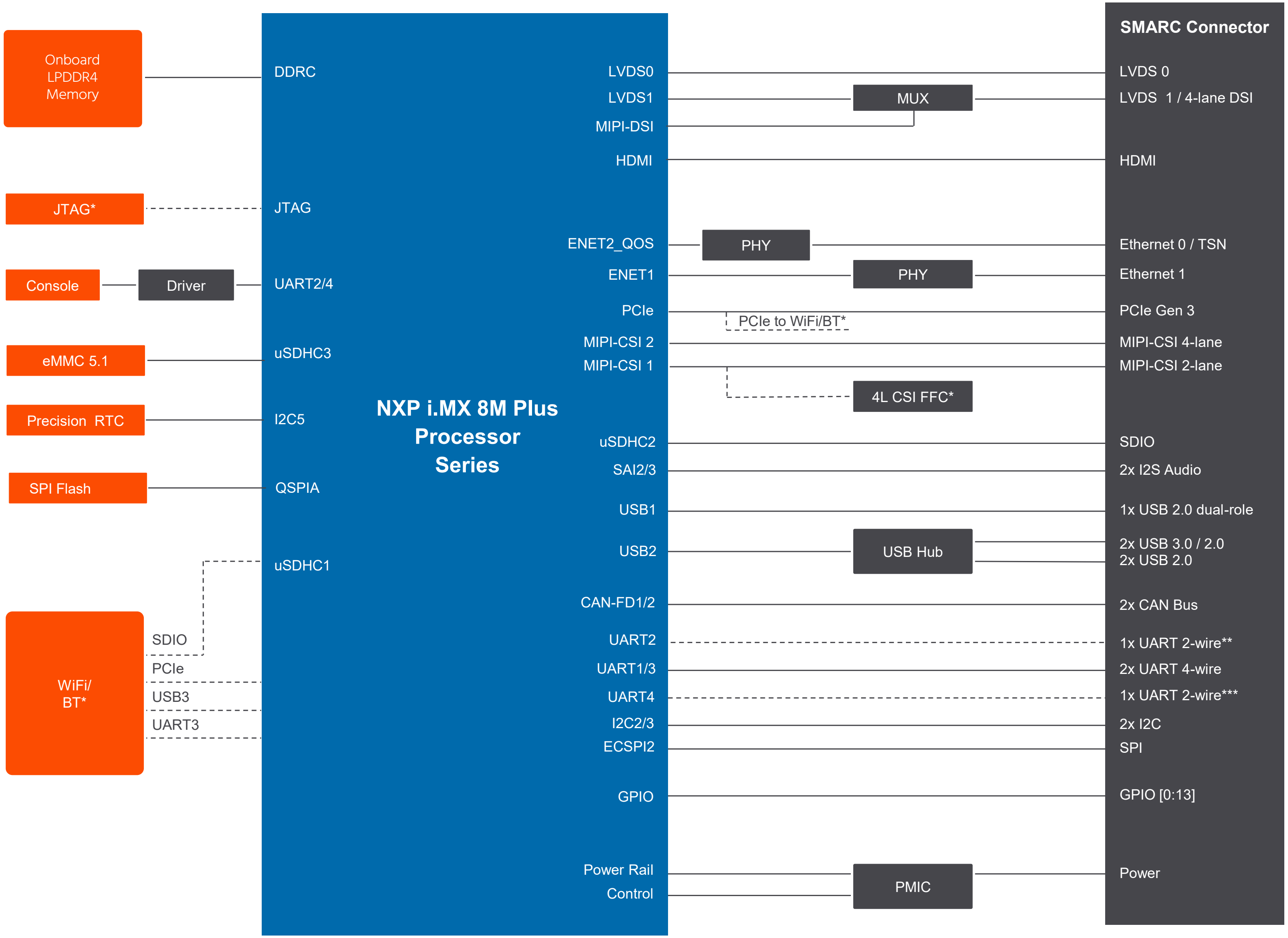
2.7 Environmental Specifications

Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -40° to +85°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to +85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

1. *The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.*
2. *Humidity specifications are for non-condensing conditions.*

3 Block Diagram



* Assembly Option
** Shared with Console
*** Shared with M7

4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-SMX8-Plus variants. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 7 Cooling Solution Variants

Cooling Solution	PN	Description
CSP	051350	Passive cooling solution for SMARC module conga-SMX8-Plus. All standoffs are with 2.7mm bore hole.
HSP	051351	Heat spreader solution for SMARC module conga-SMX8-Plus. All standoffs are with 2.7mm bore hole.
CSA-Adapter	050060	Active cooling solution adapter for SMARC modules used in combination with module heat spreader.

Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board and module mounting screws.*
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

Caution

1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

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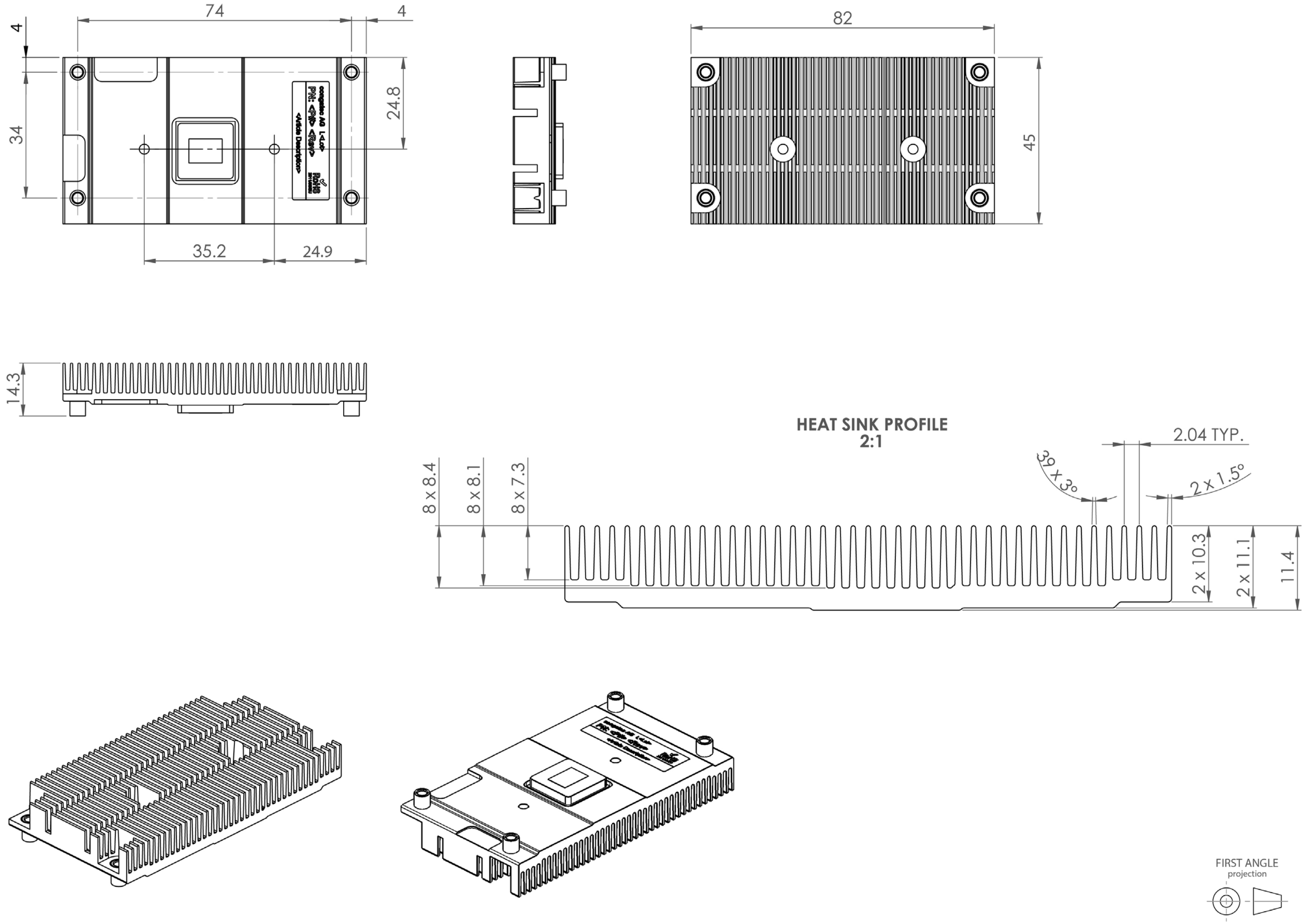
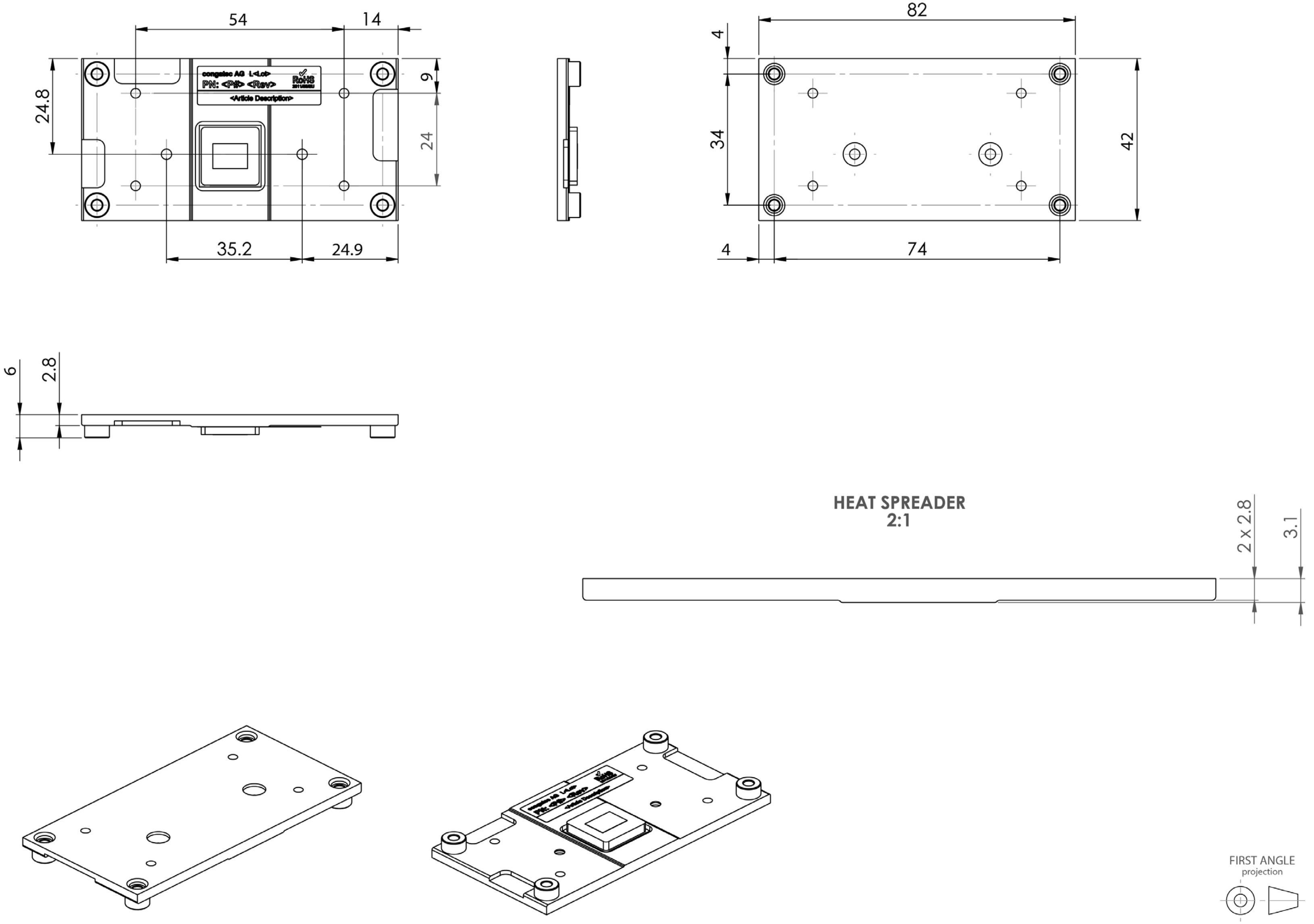
4.1 CSP Dimensions



4.2 HSP Dimensions



5 Connector Rows

The conga-SMX8-Plus has 314 edge fingers that mate with the MXM3 connector located on the carrier board. This connector is able to interface the signals of the conga-SMX8-Plus with the carrier board peripherals.

5.1 Display Interfaces

The conga-SMX8-Plus supports up to three independent displays as shown in the table below:

Table 8 Display Combinations

	Display 1		Display 2		Display 3	
	Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution
Default	Dual channel LVDS	1920x1080p60	-	-	HDMI®	3840x2160p30
Assembly Option	Single channel LVDS	1280x720p60	MIPI DSI®	2560x1080p60	HDMI®	3840x2160p30

Note

The MIPI® DSI interface only supports max. resolution 2560x1080p60 if it is the only display interface in use. Otherwise, the MIPI® DSI interface supports max. resolution 1920x1200p60 (MIPI® DSI + LVDS/HDMI®) or 1920x1080p60 (MIPI® DSI + LVDS + HDMI®).

5.1.1 LVDS / MIPI® DSI

The conga-SMX8-Plus offers LVDS[0:1] pins for one 18 / 24 bit dual channel LVDS interface by default.

Optionally, the LVDS1 pins can be used as DSI1 pins for one 4-lane MIPI DSI® interface instead as defined in the SMARC® Hardware Specification (assembly option).

Note

The conga-SMX8-Plus does not support eDP™.

5.1.2 HDMI®

The conga-SMX8-Plus offers HDMI pins for one HDMI® 2.0a display interface with support for multi-channel audio output.

Note

The conga-SMX8-Plus does not support DisplayPort++™ (DP++™).

5.2 Camera Inteface (MIPI CSI-2®)

The conga-SMX8-Plus offers CSI[0:1] pins for up to two MIPI CSI-2® camera interfaces by default:

- CSI0 offers two lanes (up to 1.5 Gbps/lane)
- CSI1 offers four lanes (up to 1.5 Gbps/lane)

Optionally, the conga-SMX8-Plus can offer an onboard connector for Basler's proprietary BCON for MIPI interface with four lanes instead of CSI0 with two lanes (assembly option).

Note

For camera accessories, refer to section 1.2.2 "Accessories".

5.3 SDIO Card (4 bit) Interface

The conga-SMX8-Plus offers pins for one SD card / SDIO interface. This interface supports:

- OS boot (Optionally, also bootcontainer)
- SD/SDIO specification 3.0
- 200 MHz 1.8V signaling for up to 100 MBps
- Secure Digital eXtended Capacity (SDXC™) cards
- UHS-I (SDR104/50 and DDR50) [1]
- Default Mode and High Speed Mode

Note

1. *The conga-SEVAL evaluation carrier board only supports UHS-I with full-size SD cards. Adadpters (microSD to SD) are not supported.*

5.4 SPI

The conga-SMX8-Plus offers SPI0 pins for one Serial Peripheral Interface (SPI) with two device chip selects via the SPI0_CS[0:1]# pins. The max. supported clock frequency for read operations is 25 MHz and 50 MHz for write operations. SPI0 is connected to ECSPI2 of the SoC.

Optionally, the conga-SMX8-Plus can offer SPI1 pins for an additional SPI interface instead of SER2 pins (assembly option). For more information, see section 5.7 "Serial Ports". With this assembly option, SPI1 is connected to ECSPI1 of the SoC.

Optionally, the conga-SMX8-Plus can offer QSP/SPI1 pins for an additional SPI instead of the onboard NOR SPI flash memory chip (assembly option). For more information, see section 6.3 "SPI NOR Flash". With this assembly option, QSPI/SPI1 is connected to QSPIA of the SoC.

Note

The conga-SMX8-Plus does not support eSPI.

5.5 Audio (I2S)

The conga-SMX8-Plus offers I2S0 and I2S2 pins for two Inter-IC Sound (I^2S) buses by default:

- I2S0 is connected to SoC SAI2
- I2S2 is connected to SoC SAI3

Optionally, the I2S0 signals can be connected to the optional onboard Wi-Fi/BT module instead of the SMARC® connector (assembly option).

Note

The conga-SMX8-Plus does not support HDA.

5.6 I2C Interfaces

The conga-SMX8-Plus offers the Inter-Integrated Circuit (I^2C) buses as defined in the SMARC® Hardware Specification. The buses support the recommended multi-master capability and data rates of 100 kHz and 384 kHz.

- The I2C_PM bus (SoC I2C2) is shared with SMARC® LVDS/DSI DDC and CSI0/2 interfaces.
- The I2C_GP bus (SoC I2C3) is shared with the SMARC® CSI1 interface.

Note

All devices must have a unique I^2C address.

5.7 Serial Ports

The conga-SMX8-Plus offers SER[0:2] pins for three asynchronous serial ports by default. Each port supports programmable baud rates of up to 4 Mbps. SER0 and SER2 support handshaking. Optionally, the conga-SMX8-Plus can offer:

- Arm® Cortex®-M7 debug interface via onboard connector X2 instead of SER1 (assembly option)
- SPI1 pins for an additional SPI interface instead of SER2 pins (assembly option)
- Wi-Fi/BT module instead of the SMARC® SER2 pins (assembly option)

5.8 CAN Bus

The conga-SMX8-Plus offers CAN[0:1] pins for two Controller Area Network (CAN) buses via two FlexCAN controllers integrated in the SoC. Commercial variants support the CAN 2.0B protocol. Industrial variants support CAN-FD and the CAN 2.0B protocols.

5.9 USB Interfaces

The conga-SMX8-Plus offers USB[0:4] pins for five USB ports by default. The USB[1:4] pins are provided via a TI TUSB8041 USB hub. USB0 is directly routed to the SoC. [1]

Optionally, the conga-SMX8-Plus can be offered without the USB hub (assembly option). The USB signals from the SoC can be directly routed to the SMARC® USB3 pins.

Table 9 USB Interfaces - Default and Options Description

SMARC	Default	Assembly Option (Without USB Hub)
USB0[1]	USB 2.0 Dual-Role	USB 2.0 Dual-Role
USB1	USB 2.0	N/A
USB2	USB 3.0 (5 Gbps)	N/A
USB3	USB 3.0 (5 Gbps)	USB 3.0 (5 Gbps)
USB4	USB 2.0	N/A

Note

1. *USB0 can be used for the Serial Downloader mode. Fore more information, see FORCE_RECOV# description in section 5.13 "Boot Select".*

5.10 PCI Express®

The conga-SMX8-Plus offers PCIE_A pins for one PCIe® x1 Gen 3 bus with a bitrate of up to 8 GTps. The reference clock for PCIE_A (PCIE_A_REFCK±) is generated by an onboard precision oscillator (DSC557-03).

Optionally, the SoC PCIe interface can be connected to the optional onboard WiFi/BT module instead of SMARC® PCIE_A (assembly option).

Note

1. *PCIE L1 substates are not supported.*

2. *PCIE_A_CKREQ# is driven to low by the module.*

5.11 Ethernet

The conga-SMX8-Plus offers GBE[0:1] pins for two ethernet interfaces via two onboard TI DP83867 Physical Layers (PHYs). Both interfaces support:

- 10/100/1000 Mbps
- Energy Efficient Ethernet (EEE)
- Ethernet AVB
- IEEE 1588v2 Precision Timing Protocol (PTP)

In addition, GBE0 also supports Time Sensitive Networking (TSN).

5.12 GPIO

The conga-SMX8-Plus offers GPIO[0:13] pins for 14 GPIOs. All pins are capable of bi-directional operation and are pulled up to 1.8V via SoC internal 22k pull-up resistors. Several GPIOs can be used for alternative functions as defined in the SMARC® Hardware Specification.

Table 10 GPIO[0:13] Pinout Description

Signal Name	Pin	Description	PU / PD	Alternative Use
GPIO0	P108	GPIO Pin 0 Preferred Output	socPU-22k	CAM0_PWR#
GPIO1	P109	GPIO Pin 1 Preferred Output	socPU-22k	CAM1_PWR#
GPIO2	P110	GPIO Pin 2 Preferred Output	socPU-22k	CAM0_RST#
GPIO3	P111	GPIO Pin 3 Preferred Output	socPU-22k	CAM1_RST#
GPIO4	P112	GPIO Pin 4 Preferred Output	socPU-22k	HDA_RST# is not supported
GPIO5	P113	GPIO Pin 5 Preferred Output	socPU-22k	PWM_OUT
GPIO6	P114	GPIO Pin 6 Preferred Input	socPU-22k	TACHIN is not supported
GPIO7	P115	GPIO Pin 7 Preferred Input	socPU-22k	
GPIO8	P116	GPIO Pin 8 Preferred Input	socPU-22k	
GPIO9	P117	GPIO Pin 9 Preferred Input	socPU-22k	
GPIO10	P118	GPIO Pin 10 Preferred Input	socPU-22k	
GPIO11	P119	GPIO Pin 11 Preferred Input	socPU-22k	
GPIO12	S142	GPIO Pin 12 Preferred Input	socPU-22k	
GPIO13	S123	GPIO Pin 13 Preferred Input	socPU-22k	

Note

The conga-SMX8-Plus does not support HDA_RST# and TACHIN.

5.13 Boot Select

The bootcontainer source can be selected via BOOT_SEL[2:0]# as described in the table below: [1]

BOOT_SEL			Selected Boot Source
0#	1#	2#	
Float	Float	Float	SPI Flash eFuse (default) [2]
Float	Ground	Ground	SPI Flash
Ground	Ground	Float	SD card
Float	Ground	Float	eMMC
Ground	Float	Float	Serial Download Mode [3]

On the conga-SEVAL evaluation carrier board, the boot source can be selected via DIP switches M17 and M18 as described in the table below:

M17		M18	Selected Boot Source
#1	#2	#1	
OFF	OFF	OFF	SPI Flash eFuse (default) [2]
OFF	ON	ON	SPI Flash
ON	ON	OFF	SD card
OFF	ON	OFF	eMMC
ON	OFF	OFF	Serial Download Mode [3]

The OS boot device is defined via the U-Boot environment variables. For more information, refer to the conga-SMX8-Plus online software documentation at https://wiki.congatec.com

Note

1. *The available boot sources and their selection via BOOT_SEL[2:0]# pins correspond with the boot mode options and configuration pins defined by NXP®. Therefore, select the desired boot source according to this table instead of the SMARC® Hardware Specification.*
2. *Bootcontainer in onboard SPI Flash. eFuses select FlexSPI.*
3. *The Serial Download Mode can also be selected via the FORCE_RECOV# pin. For normal operation, ensure this pin is not low.*

FORCE_RECOV#

Low on the FORCE_RECOV# pin enables the Serial Download Mode regardless of the selected boot source via the BOOT_SEL[2:0]# pins. For normal operation, ensure this pin is not low. The program image can be downloaded over the USB0 port (see section 5.9 "USB Interfaces"). On the conga-SEVAL evaluation carrier board, set the jumper X45 to position 2-3 to enable the Serial Download Mode. For normal operation, ensure the jumper X45 is set to the default position 1-2.

5.14 Power Control

The power-up sequence of the conga-SMX8-Plus is described below:

1. The carrier board provides the input voltage (VDD_IN) to the module.
2. If VIN_PWR_BAD# is not driven low, the module enables its power circuits.
3. After the first VIN power on, the module starts the power-up sequence.
4. The module enables the carrier board power by asserting CARRIER_PWR_ON (SUS_S5#) and CARRIER_STBY# (SUS_S3#).
5. The module releases RESET_OUT# and starts the boot process.
6. RESET_IN# can be used for postpone boot process.

VIN_PWR_BAD#

VIN_PWR_BAD# (pin S150) is an active-low input signal. It indicates that the input voltage to the module is either not ready or out of specified range. Carrier board hardware should drive this signal low until the input power is up and stable. Releasing VIN_PWR_BAD# too early can cause numerous boot up problems. The module has a 10k pull up resistor to VDD_IN.

CARRIER_PWR_ON

CARRIER_PWR_ON (pin S154) is an active-high output signal. The module asserts this signal to enable power supplies for devices connected to the carrier board.

CARRIER_STBY#

The CARRIER_STBY# signal (pin S153) is an active-low output that can be used to indicate that the module is going into suspend state, where the A53 core power is turned off.

RESET_IN#

The RESET_IN# signal (pin P127) is an active-low input signal from the carrier board. The signal may be used to force the module to reset.

RESET_OUT#

The RESET_OUT# signal (pin P126) is an active-low output signal from the module. The module asserts this signal during the power-up sequencing to allow the carrier board power circuits to come up. The module deasserts this signal to begin the boot-up process.

POWER_BTN#

The POWER_BTN# (pin P128) is an active-low power button input from the carrier board. This power button signal is used to wake the system. Driving this signal low for at least 5 seconds powers off the system immediately.

Power Supply Implementation Guidelines

The operational power source for the conga-SMX8-Plus is 5 V. The remaining necessary voltages are internally generated on the module with onboard voltage regulators.

A carrier board designer should be aware of the important information below when designing a power supply for a conga-SMX8-Plus application:

- We have noticed that on some occasions, problems occur when using a 5 V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction. This problem though rare, has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through an oscilloscope. This will help to determine if the rise is indeed monotonic and does not have any dips. You should do this during the power supply qualification phase to ensure that the problem does not occur in the application. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

Inrush and Maximum Current Peaks on VDD_IN

The maximum peak-current on the conga-SMX8-Plus VDD_IN (5 V) power rail can be as high as TBD A for a maximum of TBD μs. You should therefore ensure the power supply and decoupling capacitors provide enough power to drive the module.

Note

For more information about power control event signals, refer to the SMARC® Hardware Specification.

6 Onboard Interfaces and Devices

6.1 DRAM

The conga-SMX8-Plus offers up to 6 GB 32 bit LPDDR4 onboard SDRAM @ 2000 MHz with support for In-band ECC. The memory size of each conga-SMX8-Plus variant is listed in section 1.2.1 "Options Information".

6.2 eMMC

The conga-SMX8-Plus offers an onboard eMMC 5.1 HS400 storage device with up to 128 GB (16 GB assembled by default). Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology. The performance of the newer eMMC may vary depending on the eMMC technology.

Note

For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions.

6.3 SPI NOR Flash

The conga-SMX8-Plus offers an onboard SPI NOR flash memory chip with up to 256 Mbit (64 Mbit assembled by default). The SPI NOR flash memory chip is connected via QSPI by default. Optionally, the conga-SMX8-Plus can offer QSPI/SPI1 pins for an additional SPI instead of the onboard NOR SPI flash memory chip (assembly option).

6.4 Wi-Fi and Bluetooth

Optionally, the conga-SMX8-Plus can offer Wi-Fi and Bluetooth connectivity via an onboard Azure Wave AW-CM276NF 802.11 a/b/g/n/ac 2x2+BT5.0 or Azure Wave AW-NM191NF 802.11 b/g/n 1x1 M.2 1216 module (assembly option).

We recommended to connect this module via an SDIO interface of the SoC. However, it is possible to connect the module via interfaces that are routed to the SMARC® connector by default:

- PCI Express (instead of PCIE_A)
- USB (instead of USB4)
- Serial Port (instead of SER2; can only be used for Bluetooth)

Optionally, SoC SAI2 signals can be connected to this module (assembly option). For more information, see section 5.5 "Audio (I2S)".

6.5 RTC

The conga-SMX8-Plus offers a discrete Real-Time Clock (RTC) via an onboard MicroCrystal RV-4162-C7 module (I²C Address: 0xD0). This RTC module is powered via the SMARC® VDD_RTC rail or a 3.3V rail.

Note

The conga-SMX8-Plus has onboard Schottky diodes that prevent reverse current.

6.6 Console and Debug Interfaces

6.6.1 A53 Console and M7 Debug

The conga-SMX8-Plus offers an Arm® Cortex®-A53 console interface via the onboard connector X2.

Optionally, the conga-SMX8-Plus can also offer an Arm® Cortex®-M7 debug interface on this connector shared with SMARC® SER1 pins.

The connector pinout is described in the table below:

Table 11 A53 and Optional M7 Connector (X2) Pinout Description

Pin	SoC Ball	Description
1	UART4_TXD	M7 Debug: Transmit signal via ISL3243E RS-232 Transmitter/Receiver connected to UART4_TXD of the SoC
2	+VIN	SMARC VDD_IN (+5 V)
3	GND	Ground
4	UART2_TXD	A53 Console: Transmit signal via ISL3243E RS-232 Transmitter/Receiver connected to UART2_TXD of the SoC
5	UART2_RXD	A53 Console: Receive signal via ISL3243E RS-232 Transmitter/Receiver connected to UART2_RXD of the SoC
6	UART4_RXD	M7 Debug: Receive signal via ISL3243E RS-232 Transmitter/Receiver connected to UART4_RXD of the SoC

Connector Type

X2: Molex PicoBlade 0532610671 (6 Circuits, 1.25mm Pitch, Right-Angle, Friction Lock)
Mates with Molex PicoBlade Cable Assembly Series 15134 with 6 Circuits
For a matching cable with two D-SUB 9 connectors, see PN 48000023 in Table 3.

6.6.2 JTAG Debug

Optionally, the conga-SMX8-Plus can offer an onboard JTAG debug interface (X3) (assembly option).

The connector pinout is described in the table below:

Table 12 Optional JTAG Debug Connector (X3) Pinout Description

Pin	SoC Ball	Description
1	JTAG_VREF	+1.8V sourced by Module
2	JTAG_TMS	JTAG mode select
3	GND	Ground
4	JTAG_TCK	JTAG clock
5	GND	Ground
6	JTAG_TDO	JTAG data out
7	JTAG_MOD	Not connected
8	JTAG_TDI	JTAG data in
9	GND	Ground
10	JTAG_SRST#	System Reset, active low

Connector Type

X3: Molex PicoBlade 0532611071 (10 Circuits, 1.25mm Pitch, Right-Angle)

7 Signal Descriptions and Pinout Tables

Click on the screenshot or link below to directly download the conga-SMX8-Plus pinout as an Excel file:

X1A + X1B - SX8P SMARC edge connection							
SX8P / conga-SMX8-Plus Interfac	i.MX8MP Ball Nam	i.MX8MP Ball	SMARC Pin Name	SMARC Pin	I/O	PU/PD	Remark
I2S	SAI2_MCLK	AJ15	AUDIO_MCK	S38	O		
Management Pins	NAND_READY_B	T28	BATLOW#	S156	I	PU-10k	
Boot Select	BOOT_MODE0	G10	BOOT_SEL0#	P123	I	PU-10k	via inverter, on engeneering samples only
Boot Select	BOOT_MODE1	F8	BOOT_SEL1#	P124	I	PU-10k	via inverter, on engeneering samples only
Boot Select	BOOT_MODE2	G8	BOOT_SEL2#	P125	I	PU-10k	via inverter, on engeneering samples only
CSI Master clock output	GPIO1_IO15	B5	CAM_MCK	S6	O		
CAN0	SAI5_RXD2	AF16	CAN0_RX	P144	I	socPU-22k	
CAN0	SAI5_RXD1	AD16	CAN0_TX	P143	O	socPU-22k	
CAN1	SAI5_MCLK	AF14	CAN1_RX	P146	I	socPU-22k	
CAN1	SAI5_RXD3	AE14	CAN1_TX	P145	O	socPU-22k	
Management Pins	PMIC_ON_REQ	F22	CARRIER_PWR_ON	S154	O	PD-2k2	via buffer
Management Pins	PMIC_STBY_REQ	J24	CARRIER_STBY#	S153	O	PD-2k2	via inverter from SOC PMIC_STBY_REQ; enabled by I2C5_PCAL6524_P2_2
Management Pins	SAI1_MCLK	AE12	CHARGER_PRSNT#	S152	I	PU-10k	
Management Pins	SAI5_RXC	AD14	CHARGING#	S151	I	PU-10k	

https://git.congatec.com/arm-nxp/imx8-family/doc/cgtimx8_pinlist/-/raw/cgtsx8p_pinlist/cgtsx8p_pin_connection.xlsx

Alternatively, you can find the conga-SMX8-Plus pinout by selecting it from the drop-down list at:

https://git.congatec.com/arm-nxp/imx8-family/doc/cgtimx8_pinlist/tree/master

The SMARC® signals are described in the SMARC® Hardware Specification publicly available at:

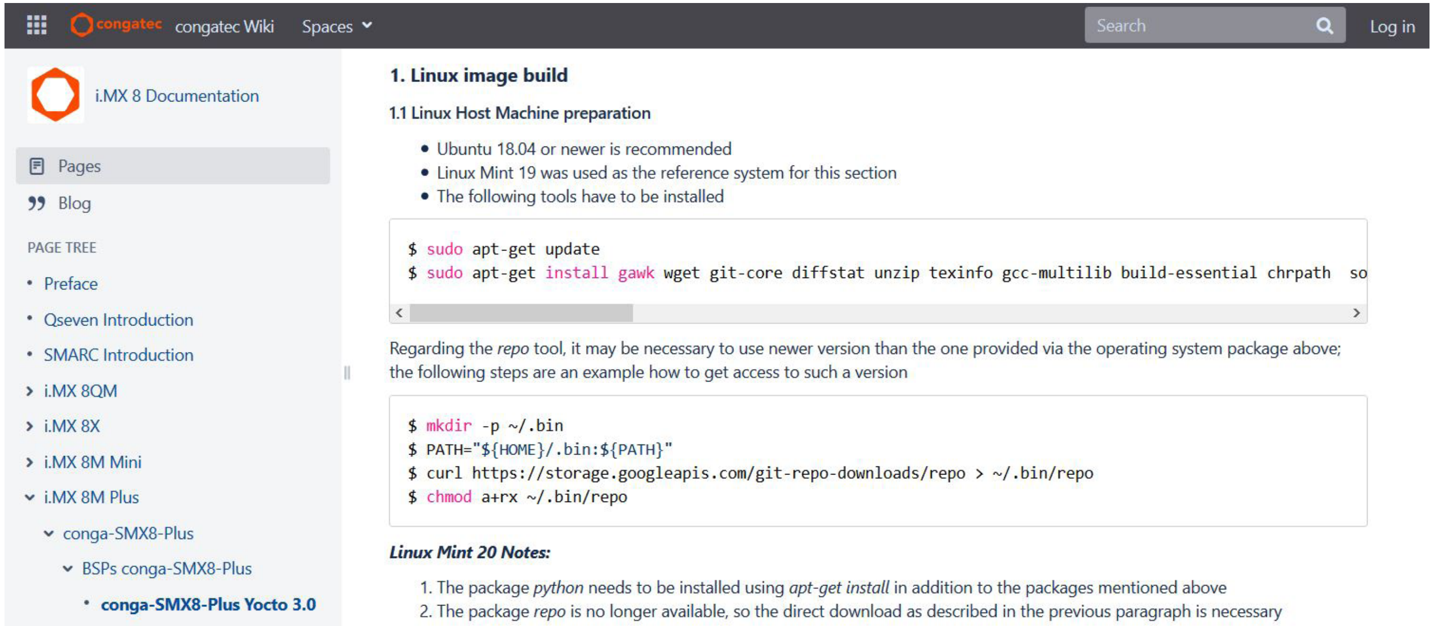
https://sget.org

The NXP® i.MX 8M Plus Applications Processor Datasheet for Commercial and Industrial Products is available at:

https://www.nxp.com

8 Software Documentation

Click on the screenshot or link below to open the conga-SMX8-Plus software documentation in your browser:



https://wiki.congatec.com/pages/viewpage.action?pageId=9339238

Alternatively, you can find the conga-SMX8-Plus software documentation by selecting it from the navigation menu at:

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