Qseven 2.0 Evaluation Baseboard

Rev. B.4

Content
Page 1 MAIN
Page 2 Block Diagram
Page 3 Qseven 2.0 Connector
Page 4 PCIe Clock Buffer
Page 5 PCIe x1 Slot 1-3 / USB OTG
Page 6 PCIe x1 Slot 0 / miniPCIe
Page 7 Ethernet / 2x USB 2.0
Page 8 USB ReDriver / 2x USB 3.0
Page 9 4x USB 2.0 / USB Setup
Page 10 PCIe x16 for GCA / COM 2
Page 11 LVDS (eDP)
Page 12 SATA / SDIO
Page 13 Audio Codec Card Slot
Page 14 HDA Codec
Page 15 Super IO / COM 0-1
Page 16 LPC (GPIO) / I2C EEPROM / SPI / CAN
Page 17 POST display
Page 18 BATT / SPKR / Feature / FAN
Page 19 SVR +VSS, +V3.3S
Page 20 +V5A / SVR +V3.3A / Power LEDs
Page 21 ATX / DC Power Input
Page 22 Revision History

Variants
Base Components used on all options

for Qseven module assembly
#57000002 MQ7ALUBAR4H, Qseven aluminum bar, 4x M2.5, 70mmx5mmx5mm
#53000001 4x Machine Screw M2.5x5mm, pan head, philips, DIN965/ISO7045
#52500001 4x Flat Washer dia. 2.7mm, thickness 0.3mm

firmware
#63000005 QEVAP001 (to be programmed to U32)

H1-28 NA

Place close to Qseven IO cooling plane
USB OTG

0.5A continuous load max.
1A current limit typ.
2V DVLD

Dual-role device by default
SATA Aux Power

cable Item# 14000032
2.5" HDD only

0.5A continuous load max.
1A current limit typ.
2V UVLO
LPC / GPIO

SPI socket (SOIC8) / SPI header

CAN transceiver

I2C EEPROM

Default state:
A: All ON
Device address: 0xA0
Normal R/W operations

Jumper X9 settings:
1-2: CAN termination enabled
2-3: CAN termination disabled (default)
If removed, SMPS1 enables after SMPS2 is in regulation.
+3.3V Standby

+5V Standby

Power LEDs
**Revision History**

- **Rev. X.0  MAY/16/2013  LIKR**  all  design created
- **Rev. A.0  OCT/25/2013  LIKR**  all  Test points were changed to the same type.
  1. H8 connected to GND. Probe M33 was added.
  3. SDVO signals were connected to module. TP1-TP4 were removed.
  4. Test points were added - TP16, TP17.
  6. R275 was replaced by X36.
  10. SDVO signals were added for supporting Qseven 1.2 modules.
  14. Connection of S/PDIF IN and S/PDIF OUT was corrected.
  16. Option for supplying SPI socket from standby power rail was added.
  18. Value of R264 was updated. U4 was changed for a new type.
  19. DC/DC converter connected to +V12_IN. Values of R200,R201,C200,R195,R196,C198 were updated.
  20. +V3.3A DC/DC converter was updated (R246,U33,L4).
  21. C189 connection was changed from +V12 to +V12_IN. C275 and D30 were added.

- **Rev. B.0  JUN/04/2014  LIKR**  5  USB OTG implementation (USB B connector was changed for micro USB AB)
  10. R92 was added (NA by default)
  13. HDA topology improvement

- **Rev. B.1  JUL/29/2014  LIKR**  5  USB OTG updated to achieve compatibility with Qseven 1.2 (R158, R159), U23 set to NA

- **Rev. B.2  SEP/22/2014  LIKR**  5  USB OTG updated. Jumper X37 was added to drive USB ID pin manually.

- **Rev. B.3  NOV/03/2014  LIKR**  5  USB OTG updated. R158 is set to NA, R159 is changed to 0R (QEV2 is no longer backward compatible with Qseven 1.2 modules).

- **Rev. B.4  JUN/13/2016  LIKR**  8  R172, R291, R293, R305 are added to BOM (reason for change is behaviour of USB port on QA40).