CET6
COM.0 Type 6 Evaluation Baseboard
Rev. C.0

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Variants
Base    Standard w/ SuperIO W83627-DHG-P
KLI B.O.: C387, C388 were changed to 0603, C043 was added
Layout note: Short traces between R398 and X75 / 399 and X76
USB 3.0

USB 3.0 spec. requires low ESR cap (>= 120 uF) directly connected to I/O connector.

Layout note: Route USB 3.0 signals through D46, D47, D55 in the following style.

Layout note: Place D46, D47 close to X3 and X4.

Layout note: Place D67, D68 close to X3 and X4.
**USB 4 + 7**

**Gigabit LAN**

- **FB15**: 3 USB4_N
- **FB17**: 3 USB4_P
- **FB19**: 2 USB7_P
- **FB20**: 2 USB7_P
- **FB100R1A7S03**: 1 USB7_N
- **FB100R1A7S03**: 1 USB7_N

### Layout notes:
- GND void under magnets

**set jumper 1-2 if LAN Controller is powered from standby voltage (default)**

**set jumper 2-3 if LAN Controller is powered from 5V voltage**

**KLI C.0:**
- C24, C27 and U16 were changed

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**USB 2.0, Gigabit Ethernet**

**Date:** Thursday, July 03, 2014

**Size:** B

**Document Number:** C0

**Rev:** C.0

**CET6SC0 C.0:**
- Changed to SBY voltage to support wake on USB
PCI Express Clock Buffer

KLI C.0: X79 was added

R79 was changed from NP to installed. R113 was changed to NP.
KLI B.0:
SATA connectors were changed from TH to SMT type.

VCC was changed from main to standby
KLI B.0:
AC coupling capacitors were changed from 0603 to 0402

KLI B.0:
12C bus for S0 only

KLI B.0:
I2C bus is connected to X23

KLI B.0:
I2C bus for S0 only

DDI AUX SEL:
Set Jumper to 1-2 for DP
Set Jumper to 2-3 for HDMI / DVI / SDVO (default)

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Digital Display Interface 1

Created
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Sheet 12 of 25
Digital Display Interface 2 to HDMI / DISPLAY PORT

DisplayPort re-driver switch with TMDs translator was changed for a new type SH7DGF126.

NOTE: CAD DisplayPort is selected: CAD_SRC = CAD_SNK (active high as default)
HDMI/DVI is selected: CAD_SRC is driven high

When the HDMI/DVI sink is selected:
A jumper 1-2: output is DVI 1.0 compliant
A jumper 2-3: output is HDMI 1.4b compliant (default)

TMDs slew rate control = transition rise and fall time at 20% and 80% (default is 85ps...160ps)

HDP_SNK are 5V tolerant with 130k pull-down
**I²C EEPROM**

**SPI BIOS Flash**

**TPM header**

**Digital IO over I²C**

<table>
<thead>
<tr>
<th>BIOS_DisI#</th>
<th>BIOS_DisO#</th>
<th>BIOS ENTRY / SPI_CS#</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>on-module firmware (default)</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>carrier firmware from SPI</td>
</tr>
</tbody>
</table>

**Battery Support**

![Congatec AG logo]

**Title**

**Size**

**Document Number**

**Rev**

**Date:** Sheet 20 25 Thursday, July 03, 2014

**Sheet 1 of 25**
**Type detection**

- **Type0**: N.C.
- **Type1**: N.C.
- **Type2**: N.C.

**Power Button**

- **M19**: P0WRTN# -> P0WBTN# 3.3V, 21

**Disco Drive Power**

- **T04, T0A0425**
- **R06, R1%100kS03**
- **R06, R1%100kS03**
- **R05, R1%2k2S03**

**Disk Drive Power**

- **C395, C10uS05V16X**
- **C090, C100nS03V50X**
- **R358, R5%1k0S03**

**ATX Power, 5V Standby Always**

- **R34, R1%18kS03**
- **R34, R1%18kS03**
- **R302, R5%330RS03**

**KLI B.0:**
- C295, C296 were changed for C329, C330, C351

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**Type 2 Rev 1.0:**
- 12V N.C. N.C. N.C. N.C.

**Type 2 Rev 2.0:**
- N.C. N.C. N.C. N.C.

**Type 2: Type 0:**
- N.C. N.C. N.C. N.C.

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**KLI B.0:**
- B305 were changed
  (simplification of B0M)

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**Load resistors causing additional 200 mA load current at 5V_ATX helping ATX PSU to turn on**

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**Notes:**
- N.C. A.0: overvoltage protection: disables +12V at X72 at about 13.6V
- X72 usage note: Power output for peripherals (e.g., HDD) when supplying the system with 12 V only
- set jumper 1-2 for pull-up on PWR_OK; only for debug
- set jumper 3-4 for PWR_OK from ATX supply (default)
- set jumper 5-6 for PWR_OK from DC/DC (only in single 12 V mode)

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**KLI B.0:**
- C295, C296 were changed for C329, C330, C351
Postcode Display

Layout note:
- Serial links were disconnected from U50
- Place R351 close to COM Express Connector

**1.5 V**

**3.3 V Standby**

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Power In connectors - BANANA JACK

KLI B.C.: C405 was added

KLI C.O.: SVR controller was changed

VCC3V3

KLI B.C.: C405 was added

KLI C.O.: SVR controller was changed
**HISTORY**

10.01.2011  SRO  design created

19.08.2011  SRO  page 3: set SUS_S3# buffer to be populated
                page 4: swapped connection of DDI2_AUX, DDI3_AUX
                page 6: changed SHLDGND - GND connection
                page 7: exchanged UP16C21200 by UIC89DB1233 (PCIe Gen. 3 compatible Clock Buffer)
                page 9: connected X12.R17, B31, B81 to B48, to enable PCIeRefClk also with x1, x4 and x16 cards
                page 11: exchanged SATA connectors
                page 13, 14: swapped connection of TMDS_B_CLK and TMDS_C_CLK at U29, U30,
                        added circuitry to connect DDC-PFU only in TMDS mode

12.03.2011  SRO  page 18: changed oscillator at Super I/O from 48 MHz to 24 MHz
page 19: mirrored X42, X44 to be compatible to conga-adapPS2
page 19: swapped DTR and TXD signals at X47, X62 to maintain compatibility to conga-CEVAL
page 20: added PU at SPI_CS# to ensure stable level at SPI flash
page 21: changed connection of X53.1 and X53.3 from 3.3V to 5V
page 22: changed VCCSV5_SBY_ALW_Oring circuit
                added overvoltage protection circuit to Disk Drive Power Connector

General: changed connection of I/O connector's shield from SHLDGND to GND
General: changed CLE150UC6E25 to CLE150UD6E15

7.8.2013  KLI  page 3: C389, C402, C403 were added. C385, C386 were changed from 0805 to 0603 (0805 too high to place under module).
page 4: R398, R399, X76, X76 were added (power consumption measurement). C404 was added. C407, C408 were changed from 0805 to 0603.
page 5: TP82062 were changed for TP82062C (previous chip has a bug).
page 6: C24, C27 were changed from 100u (tantalum) to 150u (polymer). U16 was changed to a new type for better signal quality.
page 6, 9: C59, C59, C74, C76, C88, C100 were changed for 47u MLCC (8V and they are sensitive for high ripple current, not recommended for 12V).
page 11: VCC for U27 and U28 was changed from VCC3V3 to VCC3V3_SBY. SATA connectors were changed from TR to SM type (X68-X71) for better signal integrity.
page 12: AC coupling capacitors C370-C377 were changed from 0603 to 0402. C146, C151 were changed (new DC blocking capacitors for 12V). C153 was deleted.
page 13, 14: SN75DP122 was changed for SN75DP126 (new type, higher bandwidth).
page 15: New connection for X55.6, pin is connected to LVDS_BKLT_EN_JP
page 18: AUX FAN circuit was changed (new option for driving Spin FAN by COMe module)
page 19: FB75, FB80 were changed for 10OR/1.7A
page 20: SPI socket (U43) was changed for a different type. LPC header was added for different types of LPC devices.
page 21: PAN2_SENSE signal was connected to D2. C401 and D28 were added. X77 was added for connection to a probe.
page 22: C295, C296 (100u tantalum, 10u MLCC) were changed for C329, C330 and C351 (3x 22u MLCC)
page 23: R88, R89 were changed for R368-R375 (from 150R to 75R)
page 24: C400 was added (high voltage MLCC)

27.6.2014  KLI  page 6: C405 was added.
page 7: R73 was changed to installed. R113 was changed to NP (PLL bandwidth of PCIe clock buffer is set to Low, better signal integrity).
X79, R436-R437 were added for measuring PCIe CLK signal from COMe module.
page 17: Connection of R210 was changed. R210 is connected to U36 pin 2 (signal HDA_RST#_CDC).
page 18: Clock oscillator for Super I/O was changed. New oscillator can provide 24MHz or 48MHz (selectable by jumper).
page 20: LPC header was changed for TPM header, requested to have the connector for TPM module from Fujitsu.
page 21: Jumper X80 was added to have an option to disconnect RTC battery.
page 23: SER0_TX/RX and SER1_TX/RX were disconnected from USO (not used by USO)
page 24: SVR was changed, previous controller has output discharge (unwanted when using ATX PSU). ISL62392 was replaced by LTC3850.