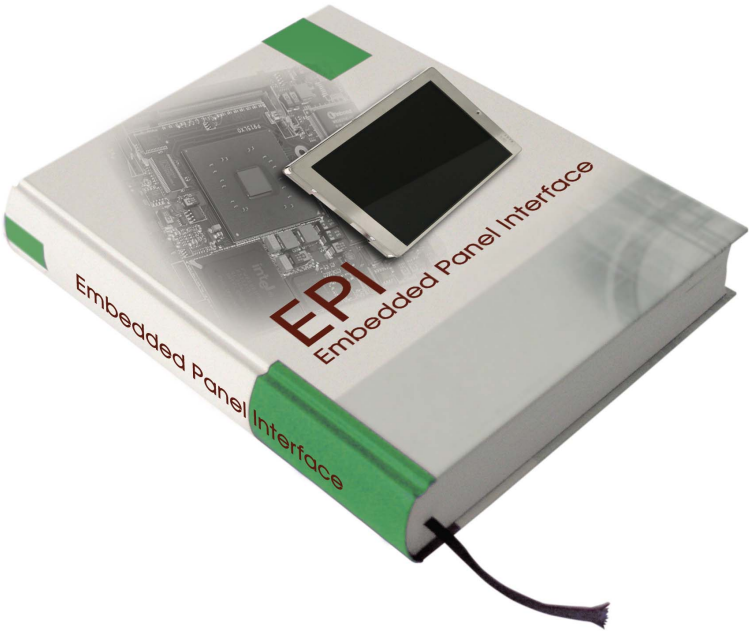
EPI
Embedded Panel Interface



EPI Embedded Panel Interface

Signal/mapping and display parameter table standardization descriptions

EPI Specification

Revision 1.0

Revision History

Revision	Date (dd.mm.yy)	Author	Changes
1.0	23.02.07	EPI Consortium	Official release

Preface

This specification defines the EPI (embedded panel interface) signals and mappings as well as a display parameter table standardization.

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Symbols

The following symbol may be used in this documentation:

Note

Notes call attention to important information that should be observed.

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EPI Website

A current version of this document can be found at http://www.epi-standard.org, as well as more information about EPI.

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1 Introduction

EPI (Embedded Panel Interface) is an open standard that allows for easy and direct control of all digital flat panel displays with maximum interchangeability.

One of the biggest advantages of COM's (Computer On Modules) is the interchangeability of modules between different suppliers. The only weak point was the direct control of digital flat panel displays. Due to the lack of a uniform standard all manufacturers had to define their own interface strategy.

This problem is now solved with the use of EPI (Embedded Panel Interface). EPI is based on the VESA standard EDID™ (Extended Display Identification Data) 1.3 and defines the software format for display properties and the scalable hardware interface.

The EDID™1.3 data set is implemented in all commercial monitors, which have a local intelligence. The problem is that this local intelligence is not available for embedded applications on the display side. In order for an Embedded Computer Module to have direct control of a digital flat panel display some more information is required within the EDID™ data set. Therefore, EPI adds the missing parameters to the complete set of EDID™ 1.3 data by using a 13byte data area within block 4 of the EDID™ 1.3 DTD (Detailed Timing Descriptor). The VESA EDID™ 2.0 specification, which is no longer supported, failed to solve this problem. This was mainly due to its high complexity.

An EPI data set, used to describe the control of a digital flat panel display, can be easily created using the information found in the display's datasheet. The EPI data set description is independent from the video controller and is interpreted by the BIOS of the COM in order to set the correct display parameters. The result is a manufacturer independent “plug-and-display” solution that enables free interchangeability of displays and COM's.

1.1 Related Documents

This EPI specification references other documents. This referencing was done to help enable low cost implementations and plug and play interoperability. The following is a list of the documents that were used and should be referred to for more information.

- *E-EDID™ Implementation Guide Version 1.0* from VESA under the file name ***EEDIDguideV1.pdf*** at www.vesa.org/public
- *VESA Notebook Standard Panel 17-inch Wide Version 1* under the file name ***Pnl17wV1.pdf*** at www.vesa.org/public/Panel%20Standards
- *Open LVDS Display Interface Specification v0.95* from National Semiconductor at http://www.national.com/appinfo/fpd/0,2132,228,00.html
- *Digital Visual Interface DVI Revision 1.0* from the Digital Display Working Group found at www.ddwg.org/downloads.asp
- *SPWG v3.5 Spec.* from the Standard Panel Working Group found at www.spwg.org

2 EPI Signal Description

The following table contains the signal names and definitions for the Embedded Panel Interface (EPI). This document does not specify a particular connector. The pure signal description allows a flexible OEM connector design. The table lists the EPI naming convention for the individual signals. The corresponding ETX spec. 2.7 and COM Express spec. 1.0 signal names are listed as interface examples.

Table 1 EPI Signals with ETX and COM Express Interface

EPI signal name	ETX spec. 2.7 signal name	COM Express spec. 1.0 signal name	Signal Description
LCD_DDC_DAT	JILI_DAT	LVDS_I2C_DAT	Serial I²C interface for reading the display parameter table from EEPROM
LCD_DDC_CLK	JILI_CLK	LVDS_I2C_CLK	Serial I²C interface for reading the display parameter table from EEPROM
LCDD0....25	LCDD0....25	LVDS_A0..A3+ LVDS_A0..A3- LVDS_B0..B3+ LVDS_B0..B3- LVDS_A_CK+ LVDS_A_CK- LVDS_B_CK+ LVDS_B_CK-	Display data, different mappings and levels are possible *Note: See Table 2 in section 3 of this document for more information about data mapping.*
LCD_VSYNC	VSYNC	N/A	VSYNC signal
LCD_HSYNC	HSYNC	N/A	HSYNC signal
LCD_VDD_EN	DIGON	LVDS_VDD_EN	Display power enable, typically used to switch the display power (active high)
LCD_BKLT_EN	BLON#	LVDS_BKLT_EN	Backlight enable, typically used to switch the backlight inverter (active low)
DETECT#	DETECT#	N/A	Display plug detection (active low, static)
VDMS	N/A	N/A	Vertical display mode select (optional)
HDMS	N/A	N/A	Horizontal display mode select (optional)

Note

N/A in the column indicates that there is no corresponding signal defined.

3 EPI Data Mappings

Table 2 lists the functions of signals LCDD0..25, LCD_VSYNC and LCD_HSYNC. EPI compliant systems may implement one, multiple or all of the below mappings.

Terminology for EPI Interface Data Mapping Table:

xxxN/P = Signal level Negative/Positive
FL0..4x = First LVDS channel data
SL0..4x = Second LVDS channel data
FLCx, SLCx = LVDS clock signals
FT0.2x = First TMDS channel data
ST0.2x = Second TMDS channel data
TCLx = TMDS clock signal
A = 24 Bit mode
B = Dual pixel mode
C = 30 Bit mode

Table 2 EPI Interface Data Mappings

SIGNAL	TTL 18 Bit	TTL 24 Bit	LVDS	TMDS
LCDD0	RED0	RED2	FL0N	ST0N[B]
LCDD1	RED1	RED3	FL0P	ST0P[B]
LCDD2	RED2	RED4	FL1N	ST1N[B]
LCDD3	RED3	RED5	FL1P	ST1P[B]
LCDD4	RED4	RED6	FL2N	ST2N[B]
LCDD5	RED5	RED7	FL2P	ST2P[B]
LCDD6	GREEN0	GREEN2	FLCN	
LCDD7	GREEN1	GREEN3	FLCP	
LCDD8	GREEN2	GREEN4	FL3N[A]	
LCDD9	GREEN3	GREEN5	FL3P[A]	
LCDD10	GREEN4	GREEN6	SL0N[B]	FT0N
LCDD11	GREEN5	GREEN7	SL0P[B]	FT0P
LCDD12	BLUE0	BLUE2	SL1N[B]	FT1N
LCDD13	BLUE1	BLUE3	SL1P[B]	FT1P
LCDD14	BLUE2	BLUE4	SL2N[B]	FT2N
LCDD15	BLUE3	BLUE5	SL2P[B]	FT2P
LCDD16	BLUE4	BLUE6	SLCN[B]	TCLN
LCDD17	BLUE5	BLUE7	SLCP[B]	TCLP
LCDD18	DCLK	DCLK	SL3N[AB]	
LCDD19	DE	DE	SL3P[AB]	
LCDD20		RED0	FL4N[C]	
LCDD21		RED1	FL4P[C]	
LCDD22		GREEN0	SL4N[BC]	
LCDD23		GREEN1	SL4P[BC]	
LCDD24		BLUE0		
LCDD25		BLUE1		
LCD_VSYNC	VSYNC	VSYNC		
LCD_HSYNC	HSYNC	HSYNC		

4 EPI Display Parameter Table Standard

The display configuration is based on VESA EDID™ 1.3, which describes a universal 128byte display identification record. To connect directly to display modules some additional parameters must be stored.

EPI uses a multipurpose data set inside the EDID™ 1.3 structure in the DTD (Detailed Timing Descriptor) block #4 to store some additional parameters and from here on it will be referred to as the EPI Descriptor within this specification. To identify it as the EPI Descriptor its data type tag must be 0Eh. Table 4 describes all 18 bytes of the EPI Descriptor beginning from offset 6Ch inside the EDID™ 1.3 structure.

Table 3 EPI Descriptor Revision 1.0

Offset	Position	Content	Description
6Ch	5 Bytes	00h, 00, 00h, 0Eh, 00h	EPI Descriptor Header
71h	Bit [2:0]	Bits per pixel	000b = 18bit 001b = 24bit 010b = 30bit 011b...111b = reserved
	Bit [4:3]	Pixels per clock	00b = 1 pixel/clock 01b = 2 pixel/clock 10b = 4 pixel/clock 11b = reserved
	Bit [6:5]	Data color mapping	00b = conventional (FPDI/VESA) 01b = non-conventional (openLDI) 10b, 11b = reserved
	Bit [7]	Reserved for later use	
72h	Bit [3:0]	Interface type	0000b = LVDS TFT 0001b = monoSTN 4/8 Bit 0010b = colorSTN 8/16 Bit 0011b = 18 Bit TFT 0100b = 24 Bit TFT 0101b = TMDS 0110b...1111b = reserved
	Bit [4]	DE polarity (high active/low active)	0b = DE high active 1b = DE low active
	Bit [5]	FPSCLK polarity	0b = FPSCLK not inverted 1b = FPSCLK inverted
	Bit [7:6]	Reserved for later use	
73h	Bit [0]	Vertical display mode	0b = normal 1b = Up/Down reverse mode
	Bit [1]	Horizontal display mode	0b = normal 1b = Left/Right reverse mode
	Bit [7:2]	Reserved for later use	
74h	Bit [3:0]	Total power on sequencing delay	0000b = VGA controller default 0001b...1111b = 10ms...150ms
	Bit [7:4]	Total power off sequencing delay	0000b = VGA controller default 0001b...1111b = 10ms...150ms

Offset	Position	Content	Description
75h	Bit [3:0]	Contrast power on sequencing delay	0000b = VGA controller default 0001b...1111b = 10ms...150ms
	Bit [7:4]	Contrast power off sequencing delay	0000b = VGA controller default 0001b...1111b = 10ms...150ms
76h	Bit [5:0]	Backlight brightness control	0...63 steps, 0 = min, 63 = max
	Bit [6]	Backlight enable	Defines if the backlight should be switched on at boot up time or not. 0b = on 1b = off
	Bit [7]	Backlight control enable	0b = disabled, bits [6:0] are don't cares 1b = enabled, bits [6:0] are valid
77h	Bit [5:0]	Contrast voltage control	0...63 steps, 0 = min, 63 = max
	Bit [6]	Reserved	
	Bit [7]	Contrast control enable	0b = disabled, bits [6:0] are don't cares 1b = enabled, bits [6:0] are valid
78h	5 Bytes	Reserved	
7Dh	Bit [3:0]	0h	Minor revision of EPI descriptor
	Bit [7:4]	1h	Major revision of EPI descriptor

Note

Refer to E-EDID™ Implementation Guide Version 1.0 for additional information.