SEVA
SMARC 2.0 Evaluation Carrierboard
Rev. C.0

Content
Page 1  Main
Page 2  Block Diagram
Page 3  Power Map
Page 4  SMARC Connector
Page 5  USB 2.0, 3.0, OTG, PCIe Routing Option
Page 6  USB Type C
Page 7  PCIe, miniPCIe
Page 8  M.2, SDIO
Page 9  GBE, CSI2, RS232
Page 10  HDA, I2S
Page 11  Audio Card Slot
Page 12  LVDS, DSI
Page 13  eDP
Page 14  HDMI0, DP0
Page 15  Feature, eSPI, SPI, Buttons, Fan
Page 16  CAN, BOOT SEL, SATA, I2C
Page 17  ATX Input, Load Switches, 5V ORing, +V3.3_ATX
Page 18  +V3.3, +V5, Postcode Display
Page 19  AT Input, +V12S, +V1.8, +V1.5S, RTC
Page 20  Module Power Path, LEDs, HDD Power Output
Page 21  Revision Power Path, LEDs, HDD Power Output
Page 22  Revision History 2/2
SEVA - Power Map

USB C

AT Carrier

ATX

AT SMARC

LTC3850

MP2908A

TLV62084

AOZ2002PI

Voltage Monitor

Standard

Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

Title

SEVA - Power Map

Document

SEVASC0 C.0

Created

Tuesday, October 30, 2018

Sheet

3

of

24
PCIe A

+V3.3A 3A
+V12S 2.1A

PCiE Clock Buffer

+V1.8S 50mA
+V1.8S 0.375A

PCiE D

+V3.3A 2.75A
+V1.5S 0.5A

mini PCIe

+V3.3A 2.1A
+V12S 0.375A

according to SWAC spec PCIe A should be used to generate PCIe_D_REFCLK.

Nevertheless, PCIe C is more suitable for SEVA design.

SEVA - PCIe, miniPCIe

I2C Address: Low = 0xD6 Mid = 0xD8 High = 0xDA

Congatec AG Auwiesenstrasse 5 D-94469 Deggendorf Germany
SMARC module must be able to sink 24mA according to SMARC spec.

Pinout according to SGET QSeven 2.0 Addendum A2.00

CSI2/3 is not hotplug capable -> no ESD protection

SEVA - GBE, CSI2, RS232

Same pinout as on QEVAL, TEVAL etc.
Place U73 close to SMARC connector

CN10 is no PCIe x1 slot!
Place similar to CN10 on QEV2!
y: 1657.95
rotation: 270°
SMARC Carriers may include an I2C serial EEPROM on the I2C_PM bus.

*The device used should be an Atmel 24C32 or equivalent.*

The device shall operate at 1.8V. The Carrier serial EEPROM should

---

**CAN0**

- +V1.8S
- +V5S

**GP I2C EEPROM**

- +V1.8S
- +V5S

**PM I2C EEPROM**

- +V1.8S
- +V5S

**BOOT_SEL**

- +V1.8S
- +V5S

**PM I2C (SMB)**

- +V1.8S
- +V5S

**SATA**

- +V3.3S

---

**Notes:**

1. The device shall be operated at 1.8V.
2. The Carrier serial EEPROM should be chosen to match the I2C slave address. If it is not, it should be set to binary 111.
HDD Power in non-ATX Mode

**Auto Mode:**

- When +V3.3 gets enabled, the status of +AT_SMARC will be used to select Power Path (AT vs. 3.3V/5V)
- Once activated, the AT_SMARC path will be kept active until a full power cycle is performed

---

**SEL_3.3V/SEL_5V#**

- 1=3.3V Module Supply Voltage
- 2=5V Module Supply Voltage

---

**AT_SMARC Path**

- AT_SMARC Path
- +AT_SMARC
- +AT_SMARC
- +AT_SMARC

---

**3.3V_SMARC_LED**

- D75: DLED0603GRN
- D76: DLED0603GRN
- D77: DLED0603GRN

---

**5V_SMARC_LED**

- D78: DLED0603GRN
- D79: DLED0603GRN
- D80: DLED0603GRN

---

**AT_SMARC_V+**

- +AT_SMARC_V+
- +AT_SMARC_V+

---

**AT_SMARC_V-**

- +AT_SMARC_V-
- +AT_SMARC_V-

---

**LEDs**

- D68: DLED0603YEL
- D69: DLED0603YEL
- D70: DLED0603YEL

---

**VIN_PWRBAD#**

- +VIN_PWRBAD# 4.15V

---

**Non-ATX Mode (3.3V/5V)**

- +V3.3
- +V5
- +AT_SMARC

---

**Overvoltage and Undervoltage Protection:**

- 2.2V < Vin < 6.5V

---

**R1%10k0S02**

- R1%10k0S02
- R1%10k0S02
- R1%10k0S02

---

**Size Document Number Rev**

- A3
- A3
- A3

---

**Date: Sheet**

- 2022 Tuesday, October 30, 2018
Revision History 1/2

SRO X.0 23.05.16 Design created
LRO A.0 02.01.17

page 1: added additional GND probe pin
page 4: added missing stand-offs, swapped ESP1_I00 and ESP1_I01 (see SMARC 2.0 errata)
page 6: removed connection of +USB_C to D9, replaced D5 with zener diode, replace Type C 1.6mm PCB compatible type. set R45 to be populated instead of R43 - allows dead battery mode. Replaced HD3S5460 by USB1046DC1. Added socket for SPI flash.
page 8: connected 1.8V I2C to M.2 socket instead of 3.3V (according to M.2 ECN) changed SMB_ALERT# levelshifting to 2 FET solution in order to avoid leakage. Added Bypass resistor option for SDIO Mux.
page 9: added Pull-Ups to LINK100# and LINK1000# signals. Swapped LEDs: Yellow = 1Gbit / Green = 100MBit.
page 10: updated HP_JD resistor to 5k. Set D31 to np. Updated R138/R140 to reduce BOM lines
page 11: updated eDP HPD levelshifting circuitry to active OD-buffer
page 12: updated HPD levelshifting circuitry to active OD-buffer, introduced weak PD @ HPD signal
page 13: added JTAG header for CGBCB programming & debugging. Added option to power SPI0 from +1.8V. Added ESD protection device for BOOT_SEL dip switches.
page 14: increased SMB 3V Pull-Ups to 3k6
page 15: added hysteresis and prioritization to 5V ORing circuit
page 16: Set C255 to be populated. Updated compensation. Added R326 to enable DCM mode.
page 18: added C323
page 19: added T58 to avoid leakage current that enables the overvoltage protection. added voltage monitor to create +V3.3_PG which is indepenent of supply path

BMI B.0 06.02.18
page 1: place M39 at least 10mm away from SMARC module silhouette (take in account module break aways)
page 4: added module detection: R385, X64
page 5: added ESD diodes D80, D81, D82, D83, D84, D85
page 6: changed source for '20V_PRESNT' detection from +AT_CARRIER to +AT_CARRIER_IN
page 8: changed SD card socket CNI and M11 switch to I-Temp parts
page 9: place X16 at least 10mm away from SMARC module silhouette (take in account module break aways), changed R107, R315, R316, R317 to 270 Ohm
page 10: added circuitry to avoid feedback from +AT_CARRIER to +AT_CARRIER_IN (T62, T63, R384), changed battery B1 to BR2032 (I-Temp), changed CN3 to I-Temp part, added seperate voltage monitor U76 for +V12S

BMI B.1 19.07.18
page 8: changed U12 to #43001421
page 11: unstuffed R408, tied (former) signal 'ACC_PRESNT#' to GND, stuffed R402
Revision History 1/2

BMI C.0 02.10.18

page 4: 2x 150µF bulk caps C357, C358 added on +VIN_SMARC
page 5: USB ferrite beads FB2, FB3, FB6 changed to 90 Ohm parts #43500203
page 7: USB ferrite bead FB9 changed to 90 Ohm part #43500203
page 8: added SDIO_PWREN as input to X11.23 via 0 Ohm resistor R428 as default,
        RESET_OUT# is option, SDIO power switch U12 changed to #43001421
        USB ferrite bead FB11 changed to 90 Ohm part #43500203
page 10: added ferrite beads FB27, FB28, FB29, FB30 on audio lines
page 11: changed polarity on signal at U75.1, added T65 and R427, layout position of CN10 changed
page 14: HDMI ferrite beads FB23, FB24, FB25, FB26 changed to 90 Ohm parts #43500203,
        added opt. PU R429 (via jumper on X65) for use as recording device,
        added D87, D86 to avoid leakage on HDMI0_DDC if SEVA is unpowered,
        U30-U32: deleted NXP CBTL06DP213EE as sourcing, left only TIHD3SS215IZQE
        replaced R173 with 10k (was 100k) to increase robustness
page 15: set D39 and D41 to np, since they are not suitable for voltages above 5V