QEVA

Qseven Evaluation Backplane

Rev. B.0

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Variants
Base  Components used on all options
Optional Qseven PCIE0 port / PCIE SLOT 4 connection:

- **OPTION A**: Qseven PCIE0 port connected to PCIE SWITCH
  - PCIE SLOT 4 connected to PCIE SWITCH

- **OPTION B**: Qseven PCIE0 port connected to PCIE SLOT 4

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**PEX8505-AA25BIG**

**PBGA 196**

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Date: **Friday, February 18, 2011**
NOTE: Supports only ADD2-N cards in this slot. ADD2-R cards are not supported.
set jumper 1-2 for 12V backlight voltage (default)
set jumper 2-3 for 5V backlight voltage

set jumper 1-2 for 3.3V backlight voltage
set jumper 2-3 for 5V backlight voltage (default)

set jumper 1-2 for backlight enable HIGH active (default)
set jumper 2-3 for backlight enable LOW active

set jumper 1-2 for backlight control by I2C DAC (default)
set jumper 2-3 for backlight control by J2T (default)
set jumper 1-2 for USB1 as Host USB Port (default)
set jumper 2-3 for USB1 as Client USB Port
set jumper 1-2 if LAN controller is powered from standby voltage (default)
set jumper 2-3 if LAN controller is powered from main voltage

These capacitors across the CHASSIS to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.

**LED State** | **Description**
---|---
Off | No Link
Steady On | Link established, no activity detected
Blinking | Link established, activity detected

**LED State** | **Description**
---|---
Off | 10 Mbps link speed
Green | 100 Mbps link speed
Orange | 1000 Mbps Link speed

**HDA/AC97 CARD EDGE CONNECTOR**

**PLACE NEXT TO PCIE4 CONNECTOR**

**BACK PANEL SIDE**

**Ethernet connector / HDA/AC97 CARD EDGE CONNECTOR**
NOTE 1. In order to avoid incorrect JD recognition, all of JD resistors should be placed as close as possible to the sense pin of codec.
Firmware Hub

SMBus Eeprom

off module BOOT FLASH LED

NOTE: isolating buffer for modules with BOOT_ALT# active in S5

Note: pull-up resistor should be integrated on module

I2C Eeprom

SPI SOIC8W

SPI DIP8 SOCKET

SPI HEADER

set jumper 1-2 for boot from off module BIOS FLASH
set jumper 2-3 for boot from on module BIOS FLASH (default)
CAN TRANSCEIVER

set jumper 1-2 for CM termination enabled
set jumper 1-3 for 83/84h (default)
Revision History

Rev. A.1 JUL\01\2009 DAKO PG A11 design created

Rev. A.2 OCT\01\2009 DAKO PG A11 design converted to Arena
PG9 U7 changed to ATMEL AT25S10AN-10SU-2.7

Rev. B.0 NOV\01\2009 DAKO PG3 added current sense resistors R293, R294, CN56, CN57
PG3 updated Qseven connector pinout according to specification 1.12; pins 91, 92, CAN0, SPI
PG4 U4 74CBT3306 changed to 2x BSS138; SMBus for PCI Express connected to suspend powered SMBus
PG6 miniCard socket connecting updated according to specification 1.2, added assembly option for back compatibility
PG7 changed connection EXCD0_SHDN# to SUS_S5# and EXCD0_STBY# to SUS_S3#
PG9 added assembly option for direct connection of Qseven PCIE0 port to PCIE slot 4
PG9 removed SMBus connection to PEX8505 I2C interface; added pull-ups and test points to PEX8505 I2C interface
PG12 updated SD/MMC Card Socket to MMC4.0 type (8bit)
PG13 updated USB1 Host/Client selection circuit
PG14 added support for configuration LED LINK10# instead of LINK#
PG15 added all ALC888 input/output connection
PG16 added PS/2 Keyboard and Mouse header connector; added KBD enable/disable to SW2
PG17 added SPI Flash
PG20 added current load at ATX 5V and 3.3V

DEC\23\2010 PG3 updated Qseven connector according to specification v1.20; added SPI, CAN connection; moved MFG pins to one header
PG4 added PD resistors on all PCIE reset signals
PG10 added DP/HDMI_HPD# connection to SDVO connector
PG11 added J11130 connector; LVDS BKLT PWM to Analog converter
PG13 changed USB ESD devices; updated USB1_CC circuit
PG17 added BOOT_ALT# isolation buffer; added I2C EEPROM address DIP switch; added SMB EEPROM socket; added SPI header and DIP socket
PG18 inserted sheet with CAN transceiver and POST
PG19 added RTC battery diode; LID header; changed FAN CN37 connector to 4pin type
PG21 changed PWGIN PU to 5V; changed QND probe