

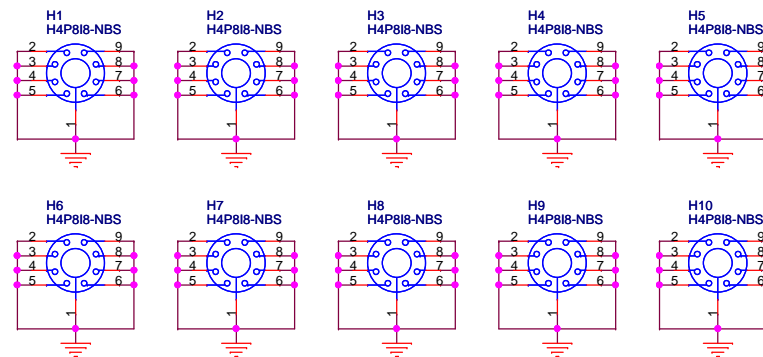
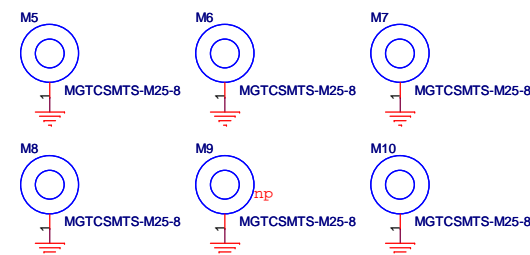
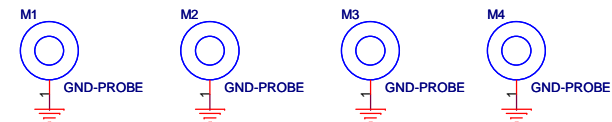
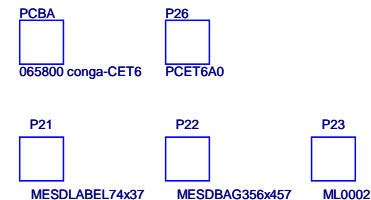
CET6

COM.0 Type 6 Evaluation Baseboard

Rev. A.0

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Page 2	Block Diagram
Page 3	COM Express connector AB
Page 4	COM Express connector CD
Page 5	USB 3.0
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Page 10	Express Card / Mini PCIe
Page 11	SATA / SDIO
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Page 17	HD Audio
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Page 19	RS232 / Parallel Port
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Page 21	Battery / SPK / Feature / FAN
Page 22	ATX Power
Page 23	Postcode / 1.5 V / 3.3 V Standby
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Variants

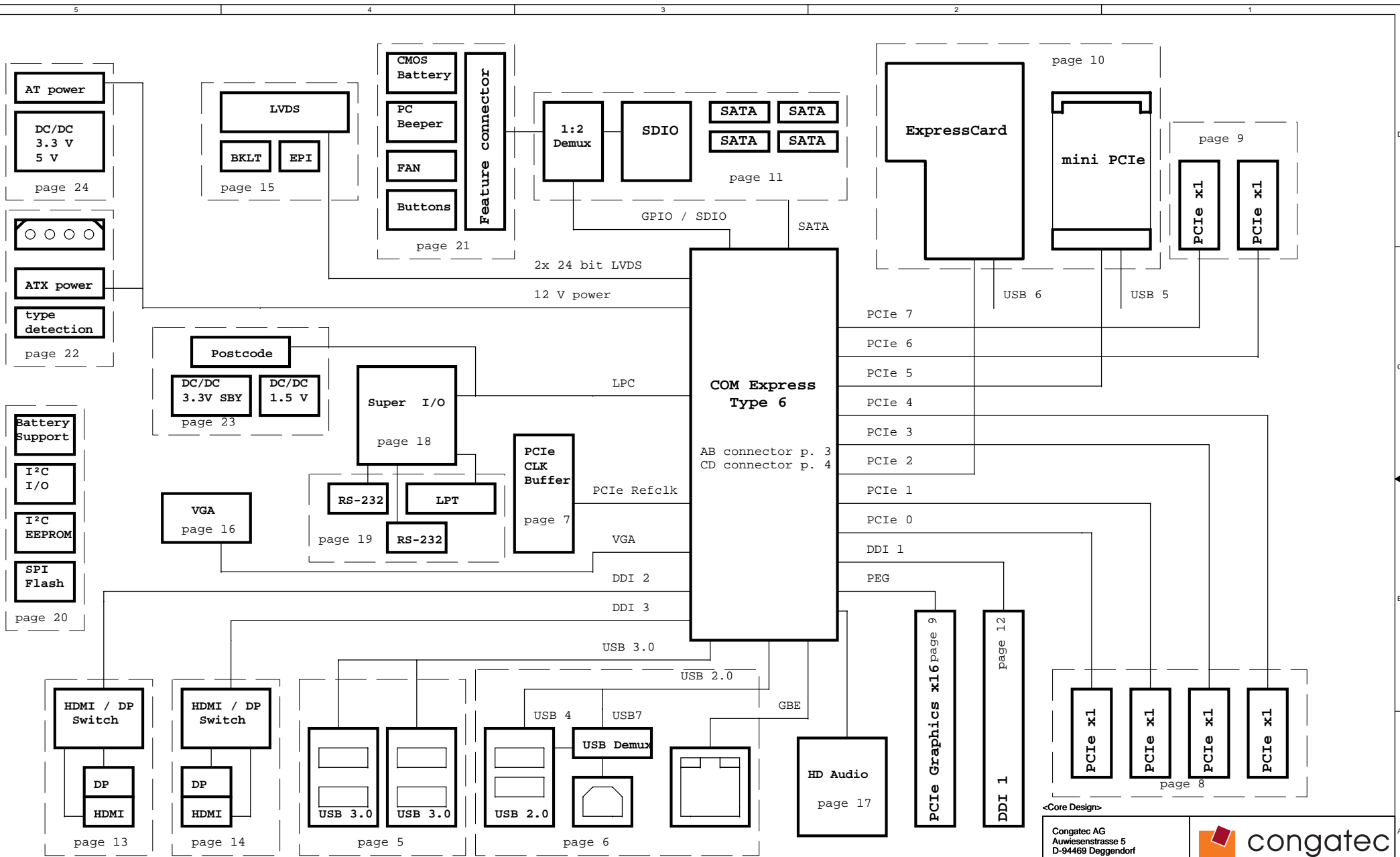
Base Standard w/ SuperIO W83627-DHG-P

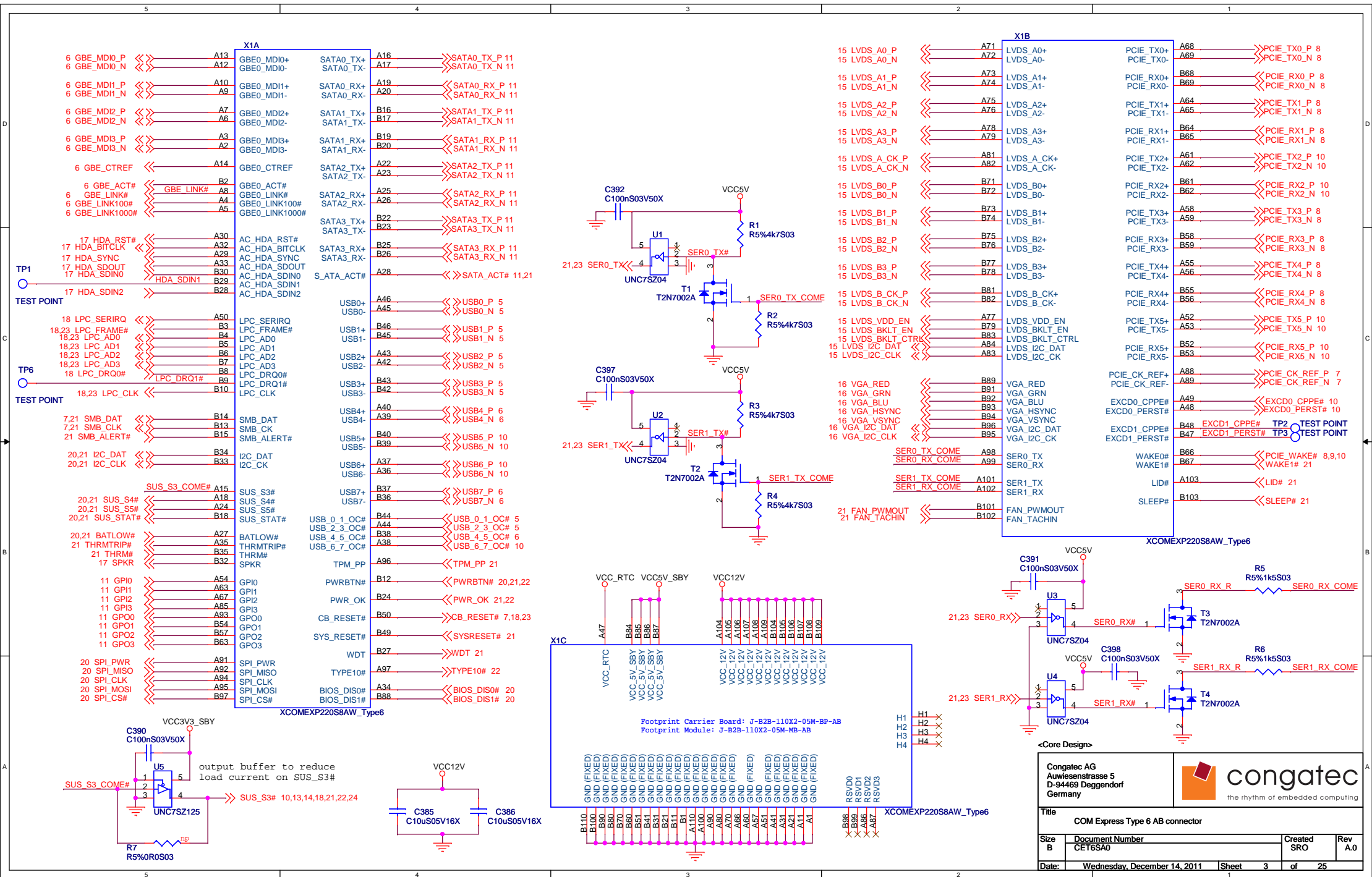
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Title			
CET6 - COM Express Type 6 Evaluation Backplane			
Size B	Document Number	Created SRO	Rev A.0
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Date:	Thursday, December 01, 2011	Sheet 1	of 25





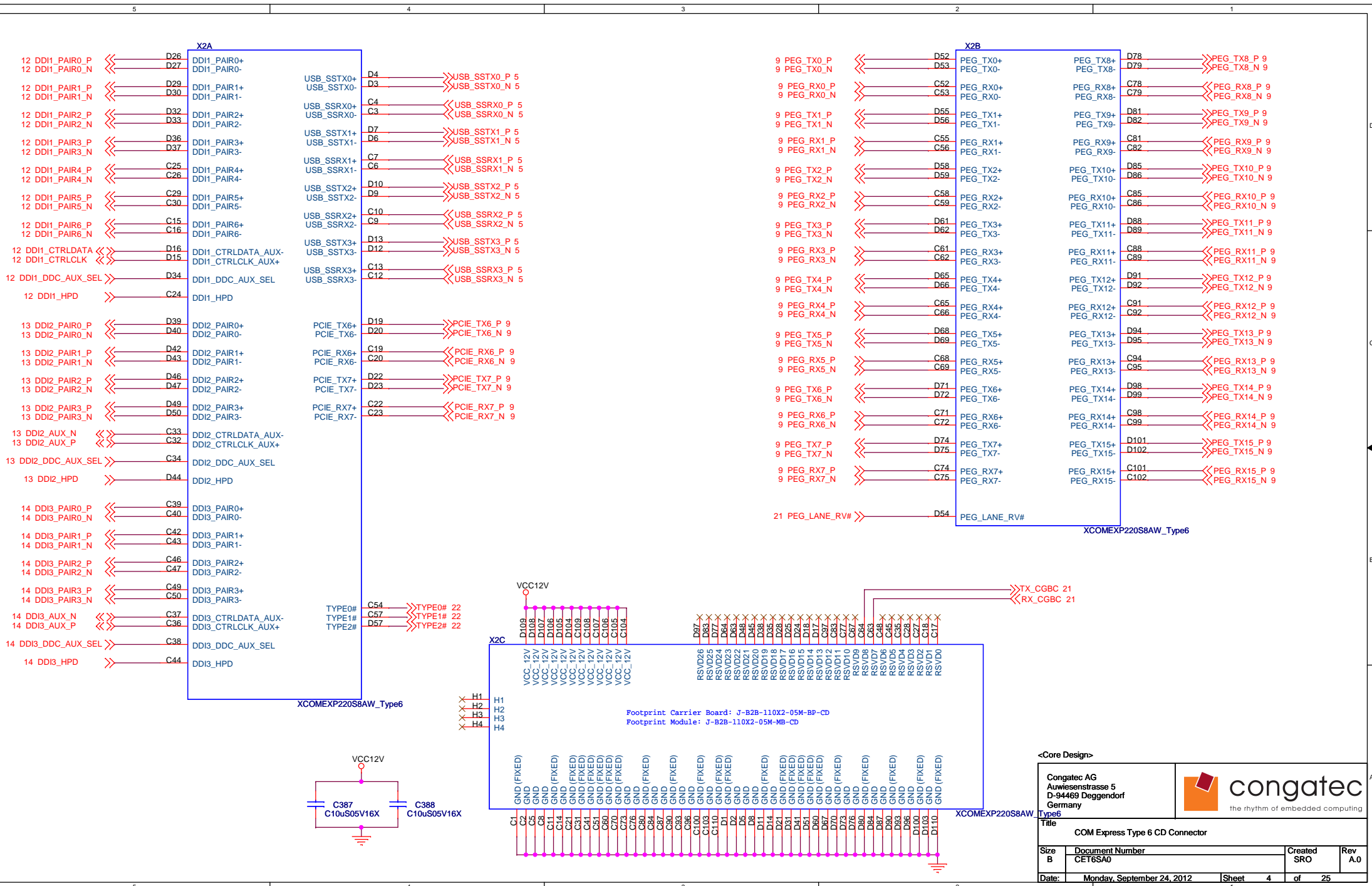
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Title: COM Express Type 6 AB connector

Size B	Document Number CET6SA0	Created SRO	Rev A.0
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<Core Design>

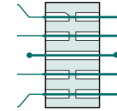
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Title
COM Express Type 6 CD Connector

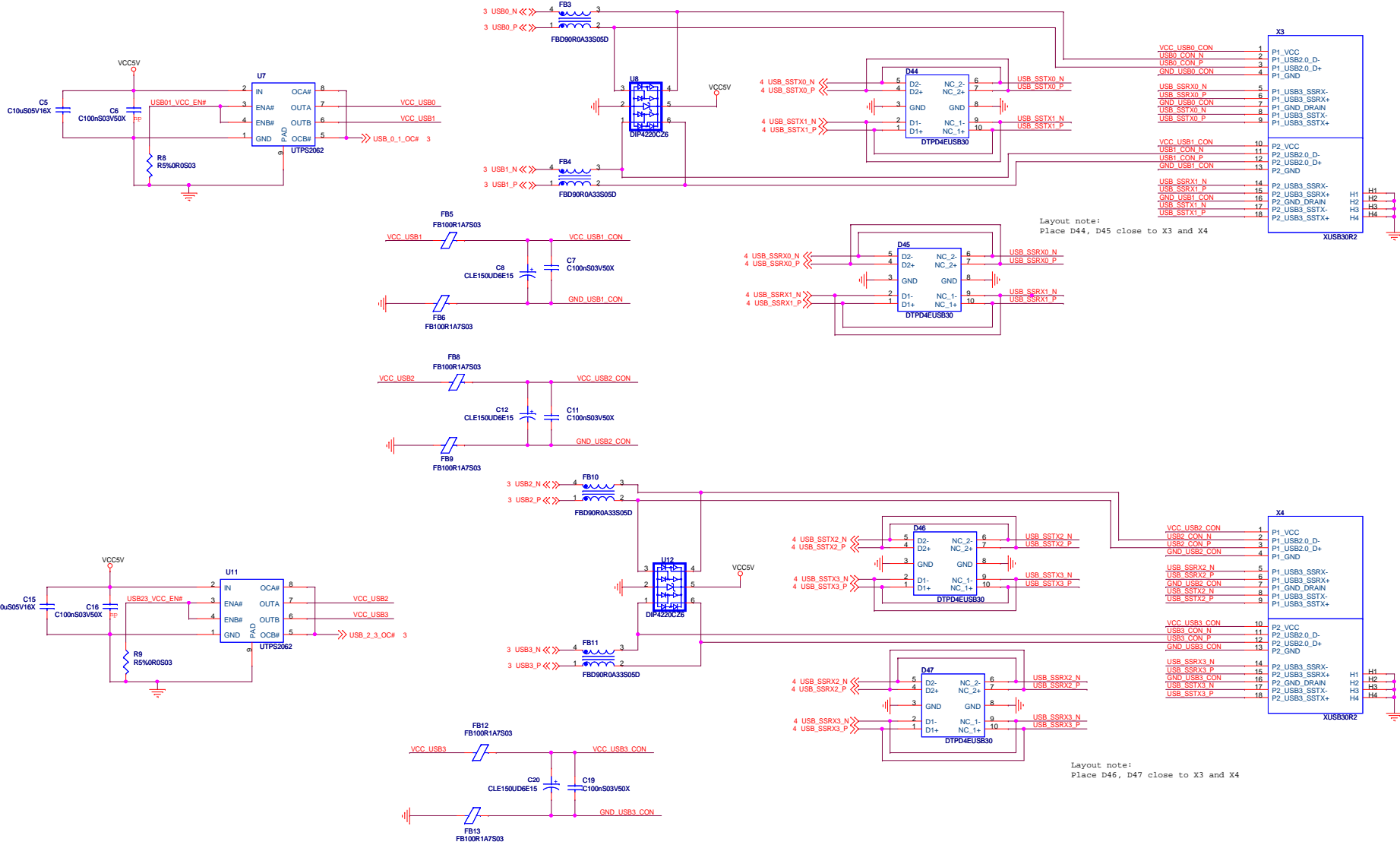
Size B	Document Number CET6SA0	Created SRO	Rev A.0
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USB 3.0

Layout Note: Route USB 3.0 signals through D44, D45, D46, D47 in the following style



USB 3.0 spec. requires low ESR cap ($\geq 120 \mu\text{F}$) directly connected to I/O connector



Layout note: Place D44, D45 close to X3 and X4

Layout note: Place D46, D47 close to X3 and X4

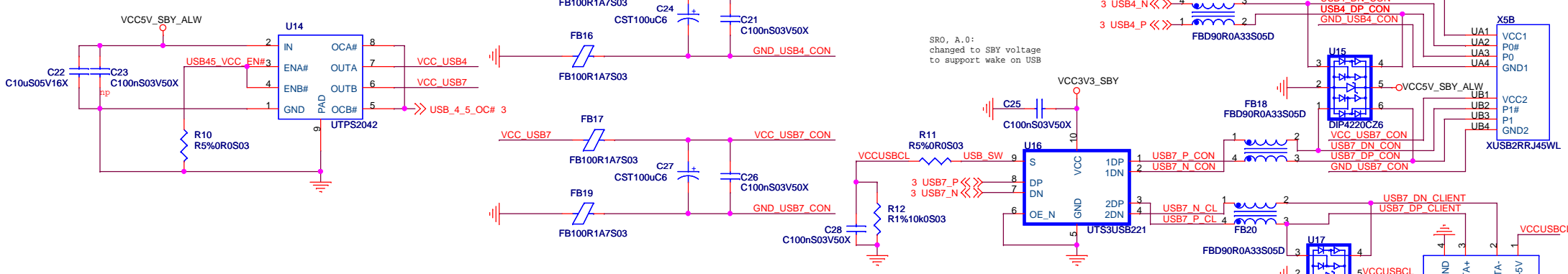
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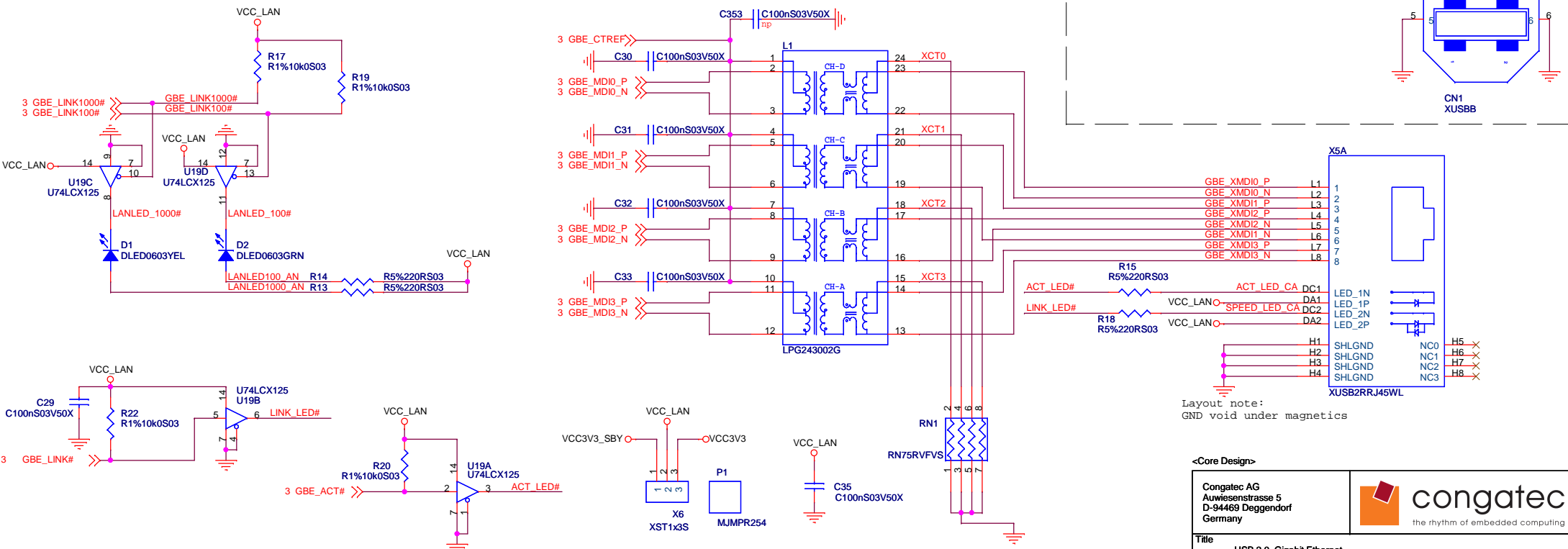
Title		USB 3.0	
Size	Document Number	Created	Rev
C	CET6350	SRO	A.0
Date:	Monday, September 24, 2012	Sheet	5 of 25

USB 4 + 7




SRO, A.0:
changed to SBY voltage
to support wake on USB

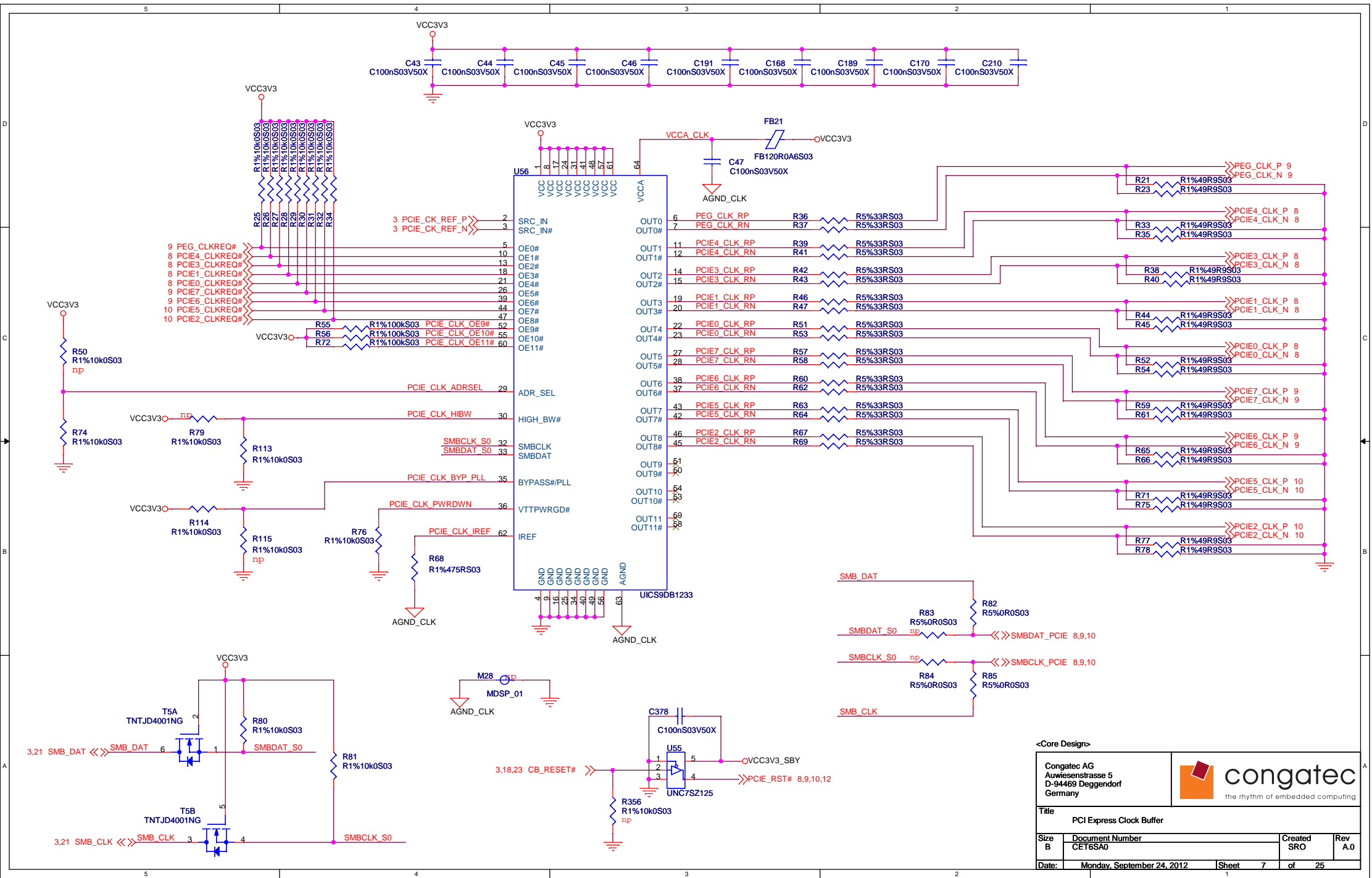
Gigabit LAN




Layout note:
GND void under magnetics

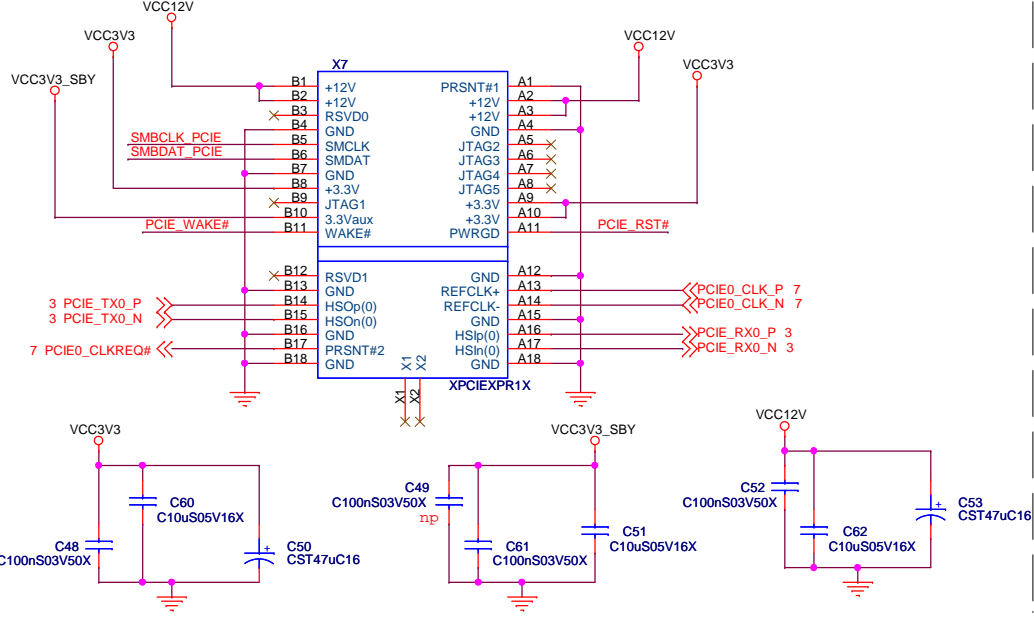
set jumper 1-2 if LAN Controller is powered from standby voltage (default)
set jumper 2-3 if LAN Controller is powered from S0 voltage

<Core Design> Congatec AG Auwiesenstrasse 5 D-94469 Deggendorf Germany		 the rhythm of embedded computing	
Title: USB 2.0, Gigabit Ethernet			
Size B	Document Number CET6SA0	Created SRO	Rev A.0
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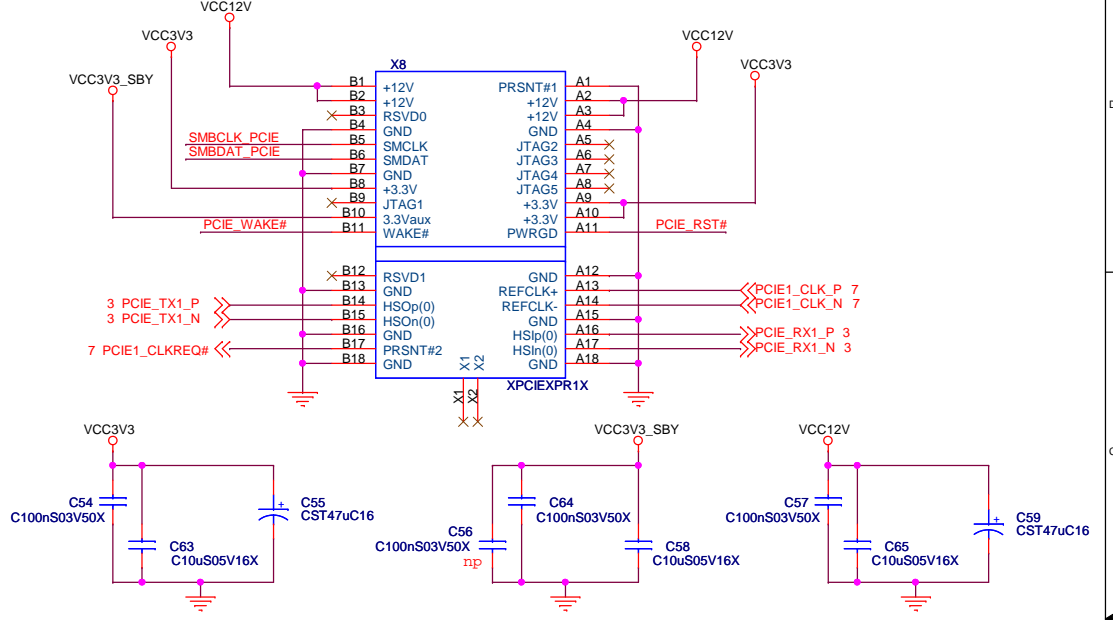


<Core Design>			
Congatec AG Auwiesenstrasse 5 D-94469 Deggendorf Germany		 the rhythm of embedded computing	
Title: PCI Express Clock Buffer			
Size B	Document Number: CET6SA0	Created SRO	Rev A.0
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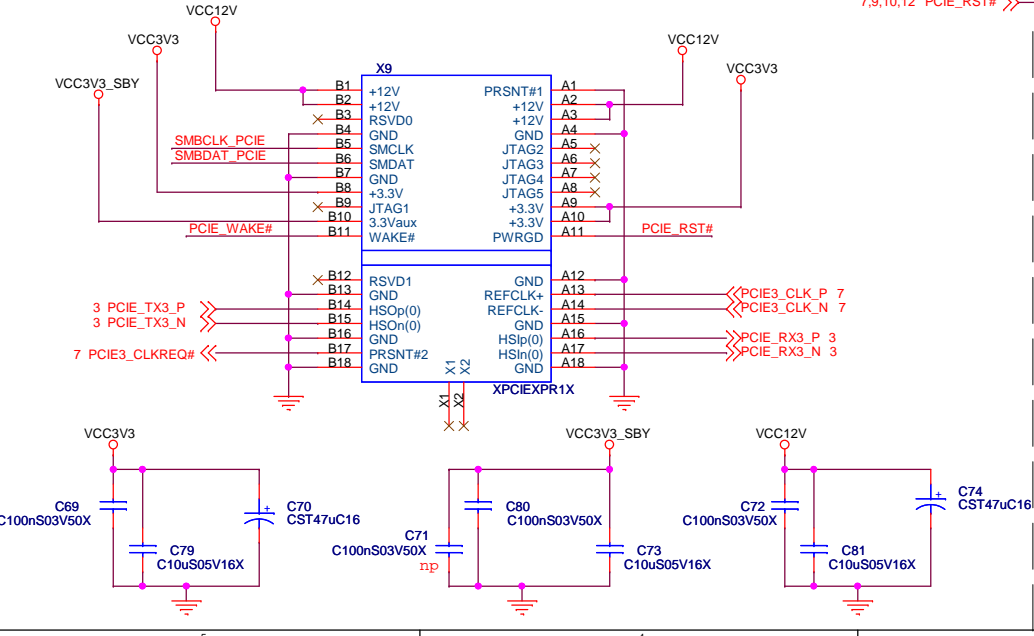
PCI Express SLOT 0 / Lane 0



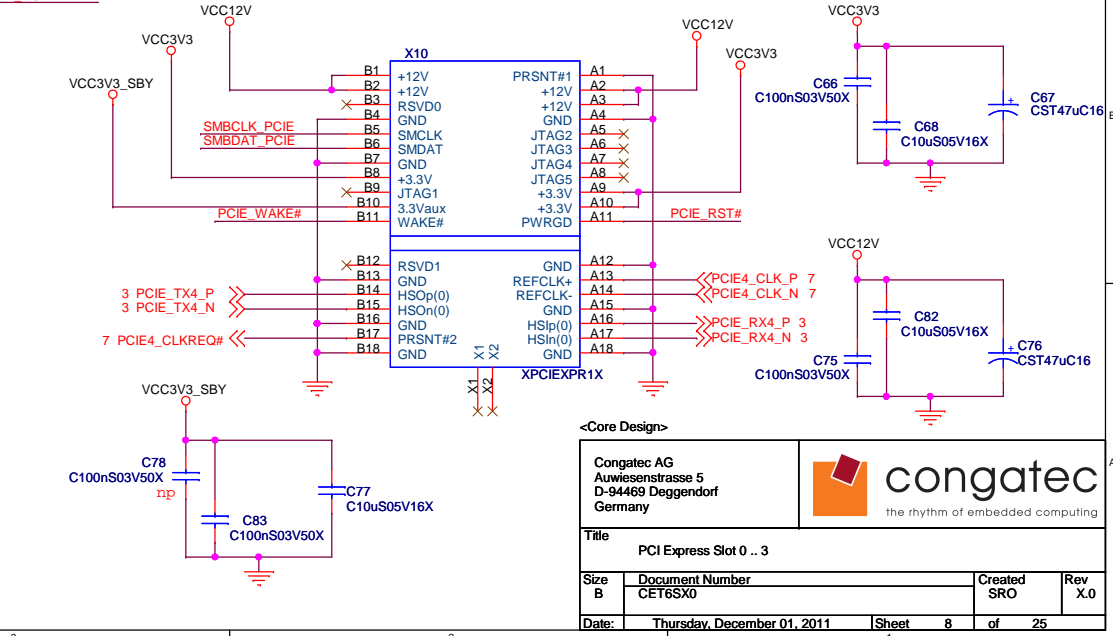
PCI Express SLOT 1 / Lane 1



PCI Express SLOT 2 / Lane 3



PCI Express SLOT 3 / Lane 4



7,9,10 SMBCLK_PCIE <<> SMBCLK_PCIE
 7,9,10 SMBDAT_PCIE <<> SMBDAT_PCIE
 3,9,10 PCIE_WAKE# <<> PCIE_WAKE#
 7,9,10,12 PCIE_RST# <<> PCIE_RST#

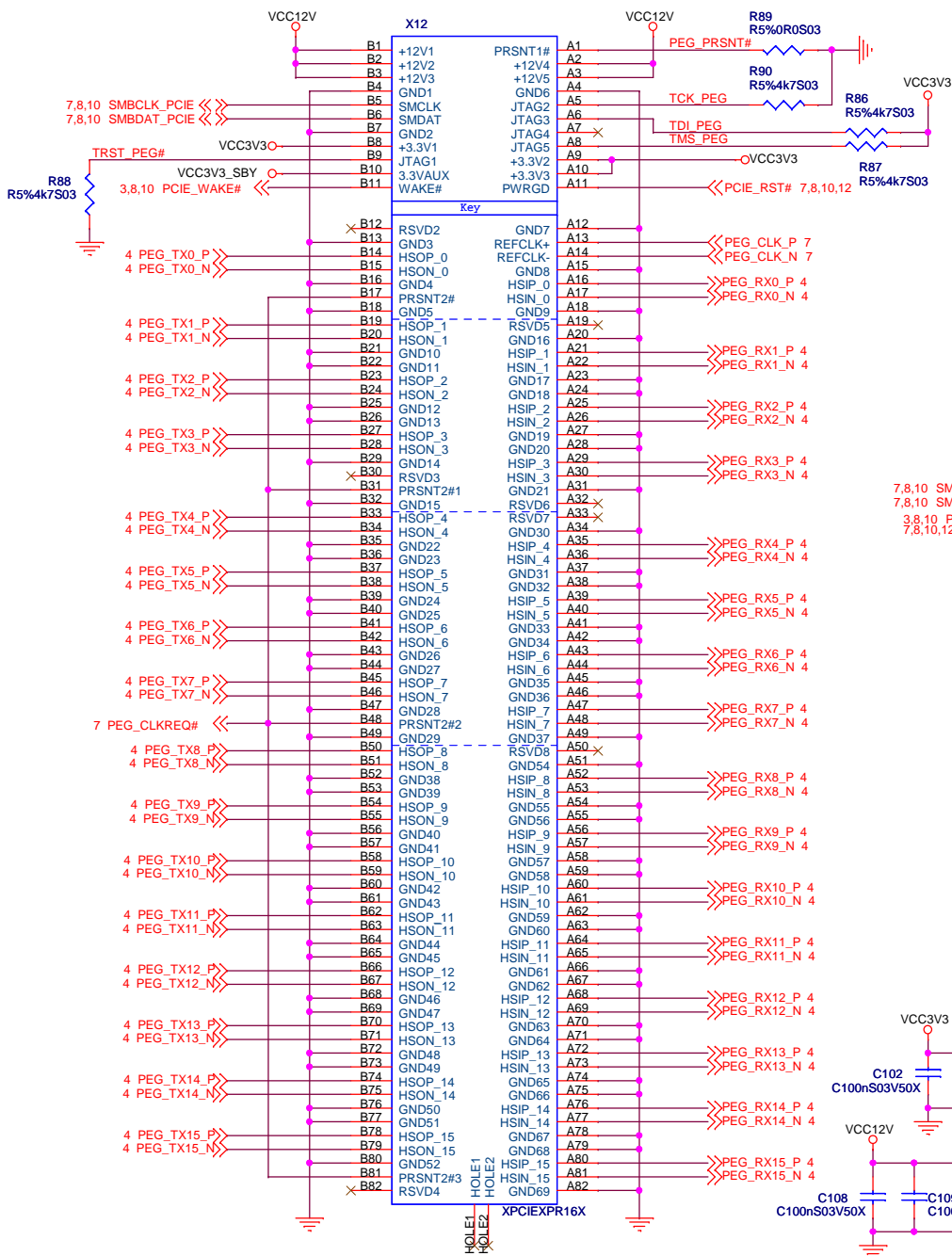
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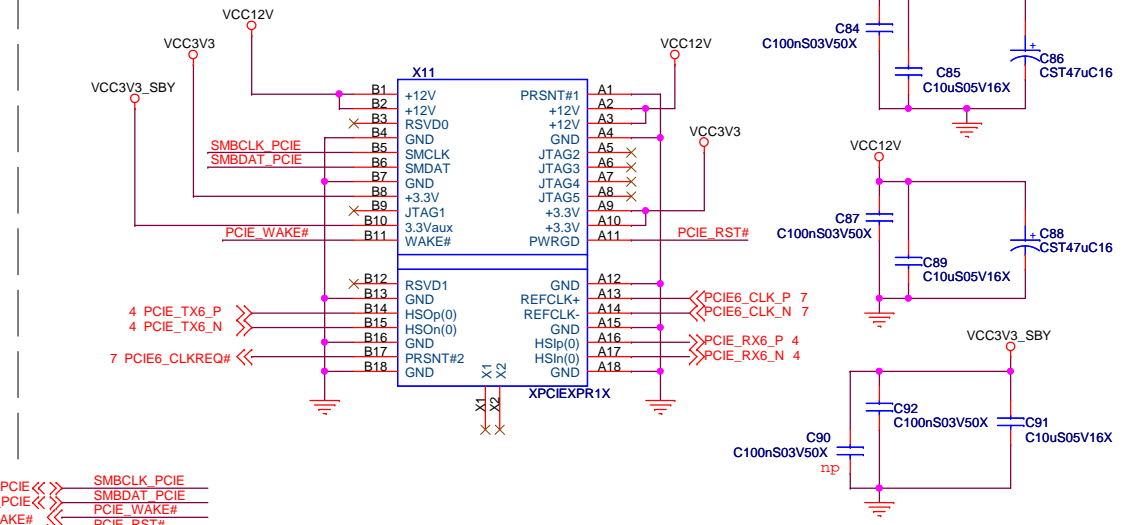
Title: PCI Express Slot 0 .. 3

Size B	Document Number CET6SX0	Created SRO	Rev X.0
Date: Thursday, December 01, 2011	Sheet 8	of 25	

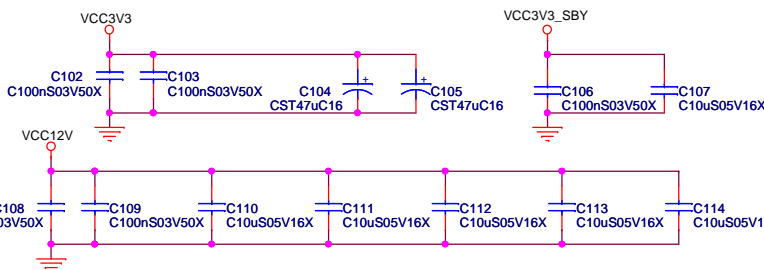
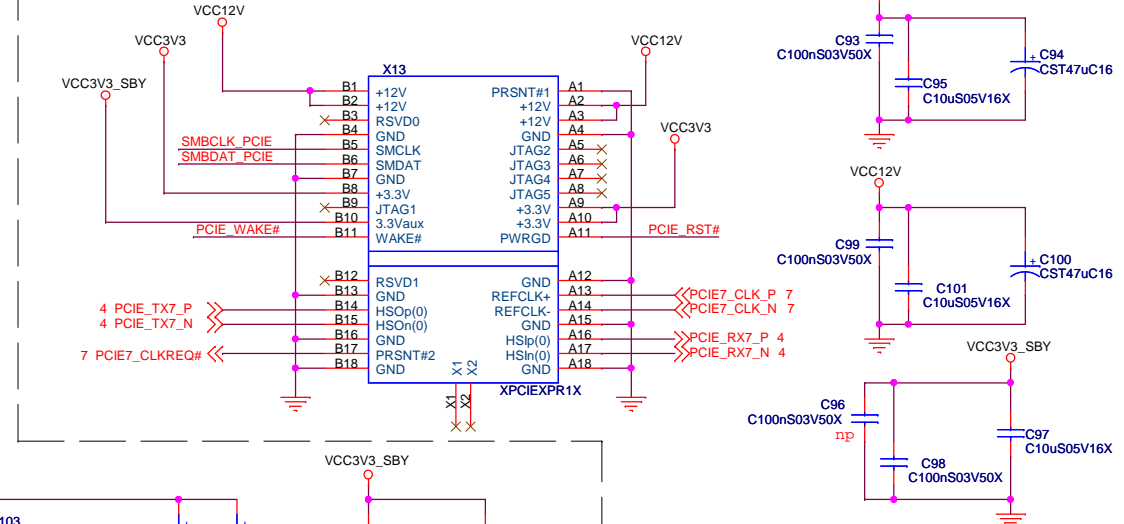
PCI Express for Graphics (PEG)



PCI Express SLOT 4 / Lane 6



PCI Express SLOT 5 / Lane 7

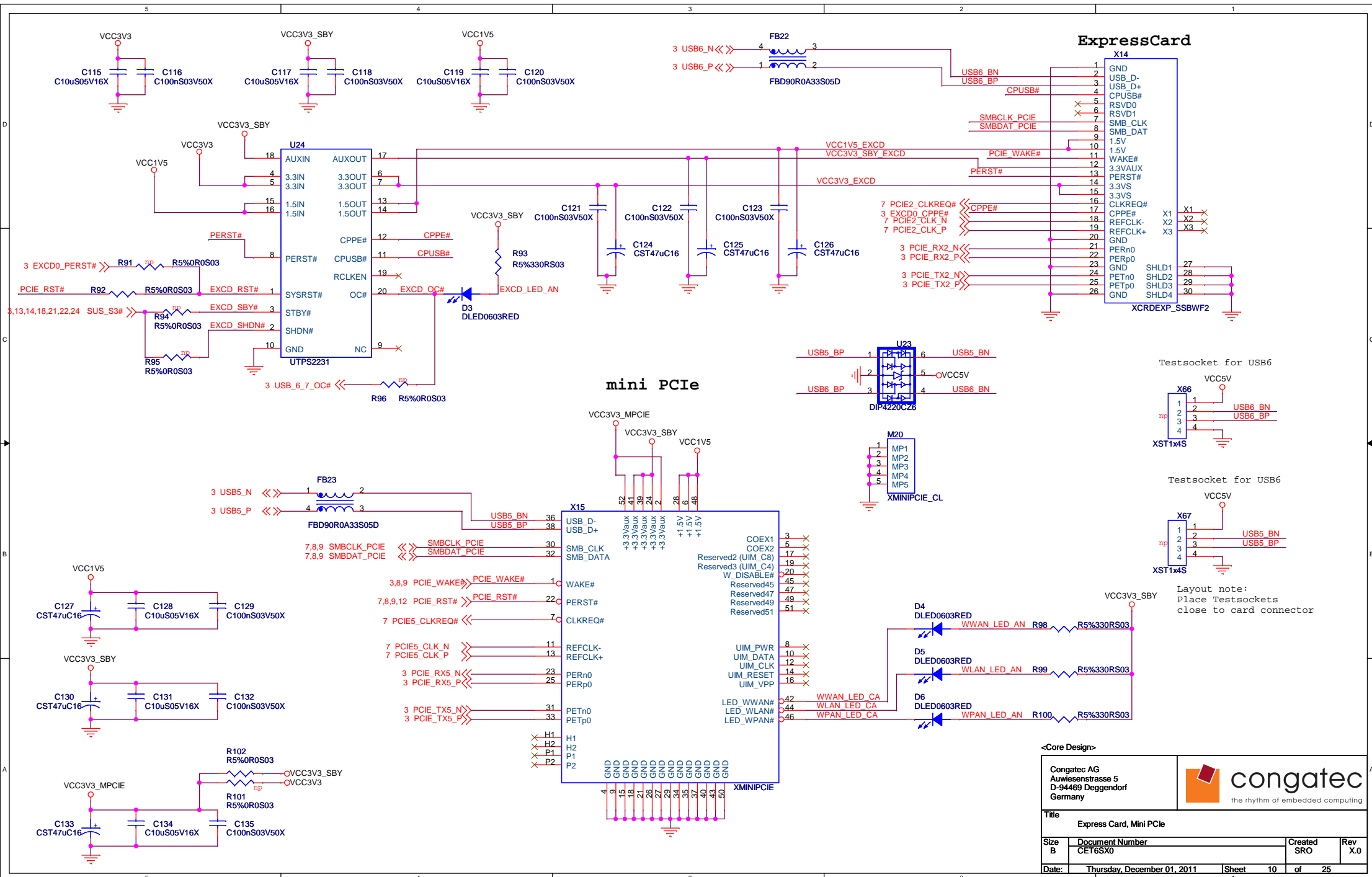


<Core Design>


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Title: PEG, PCIe 4.. 5

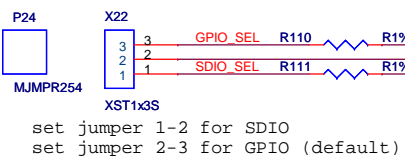
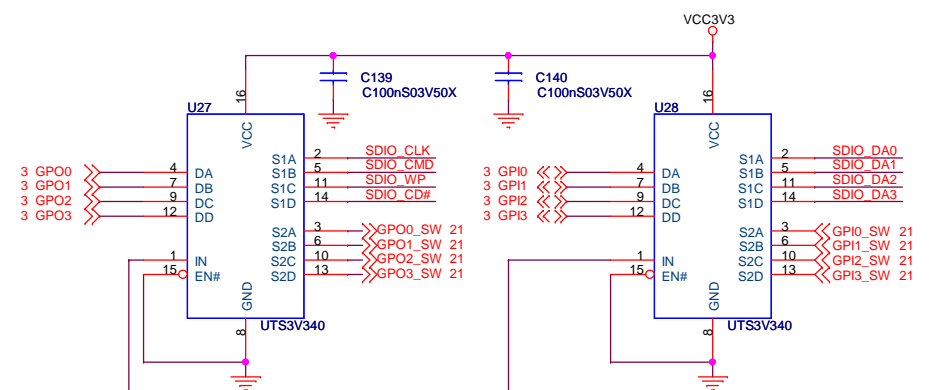
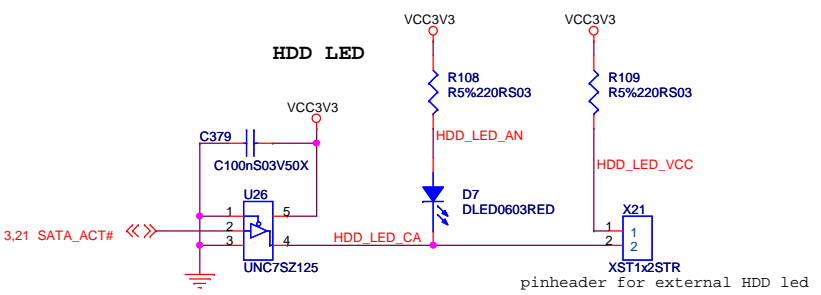
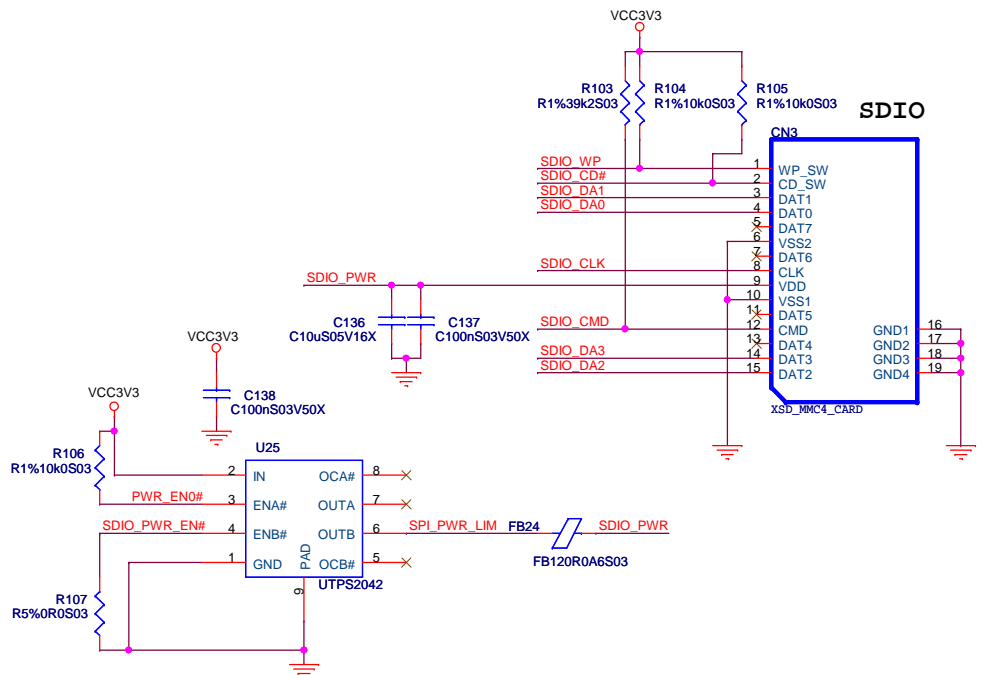
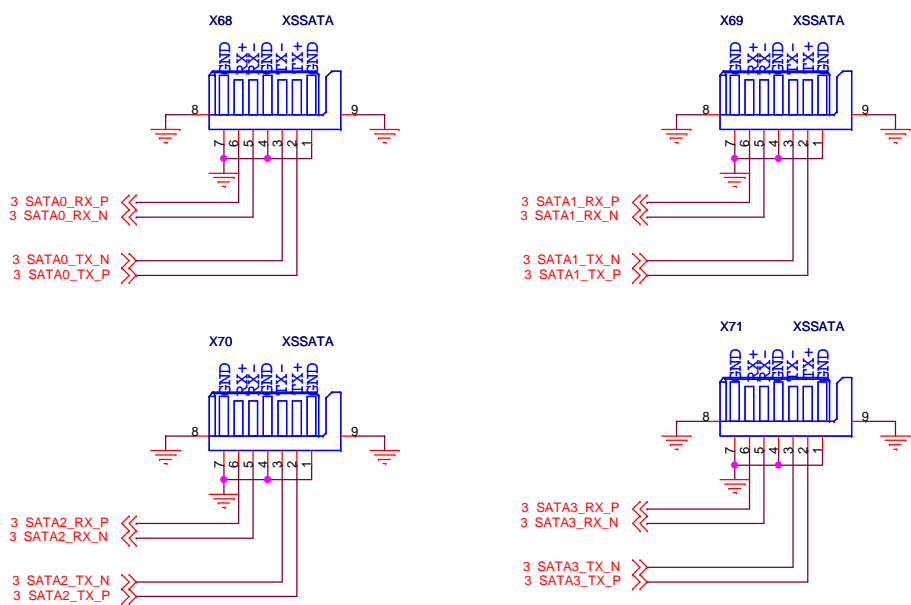
Size B	Document Number CET6SA0	Created SRO	Rev A.0
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<Core Design>

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Title: Express Card, Mini PCIe			
Size B	Document Number CET6SX0	Created SRO	Rev X.0
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SATA



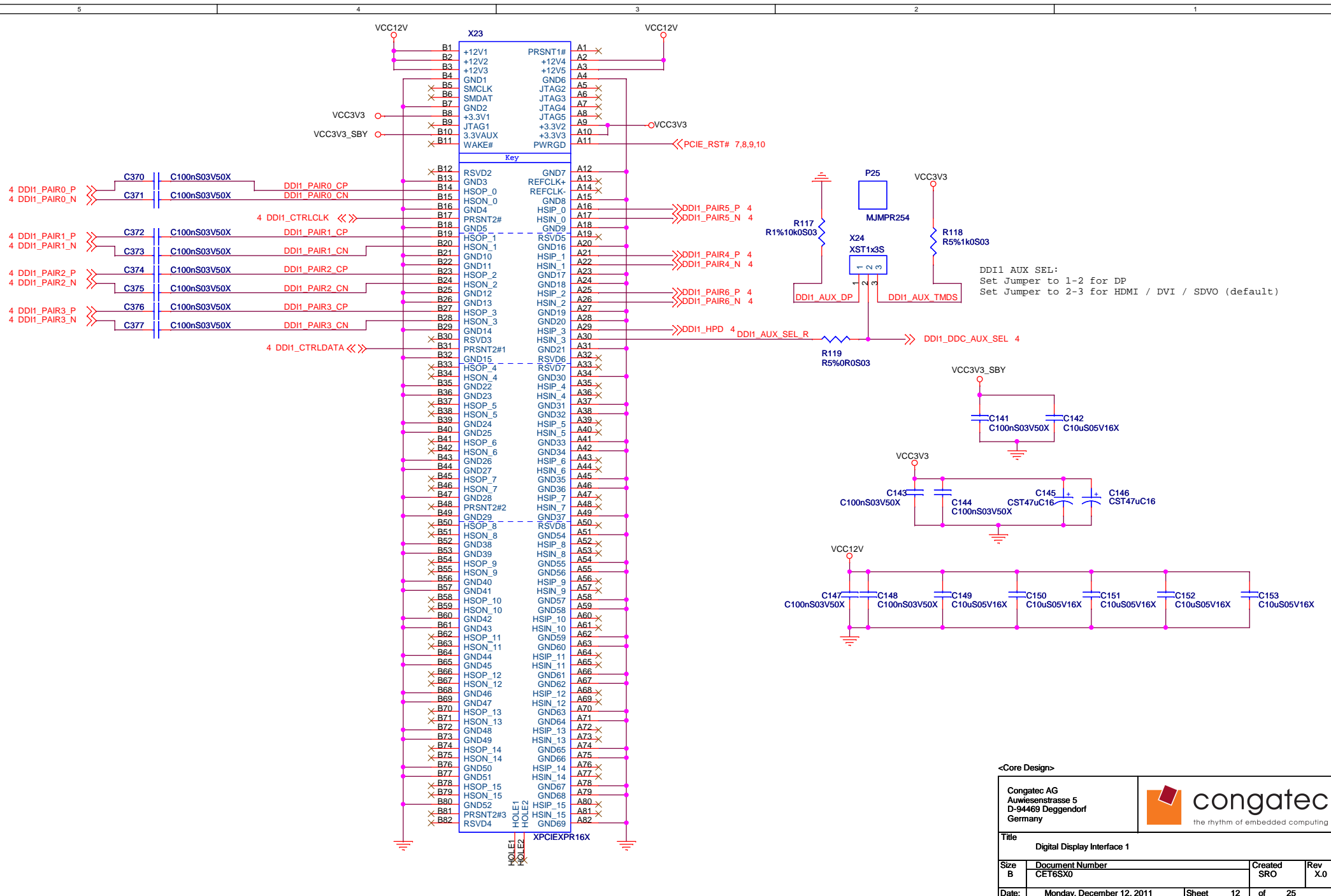
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Title
SATA, SDIO

Size B	Document Number CET6SX0	Created SRO	Rev X.0
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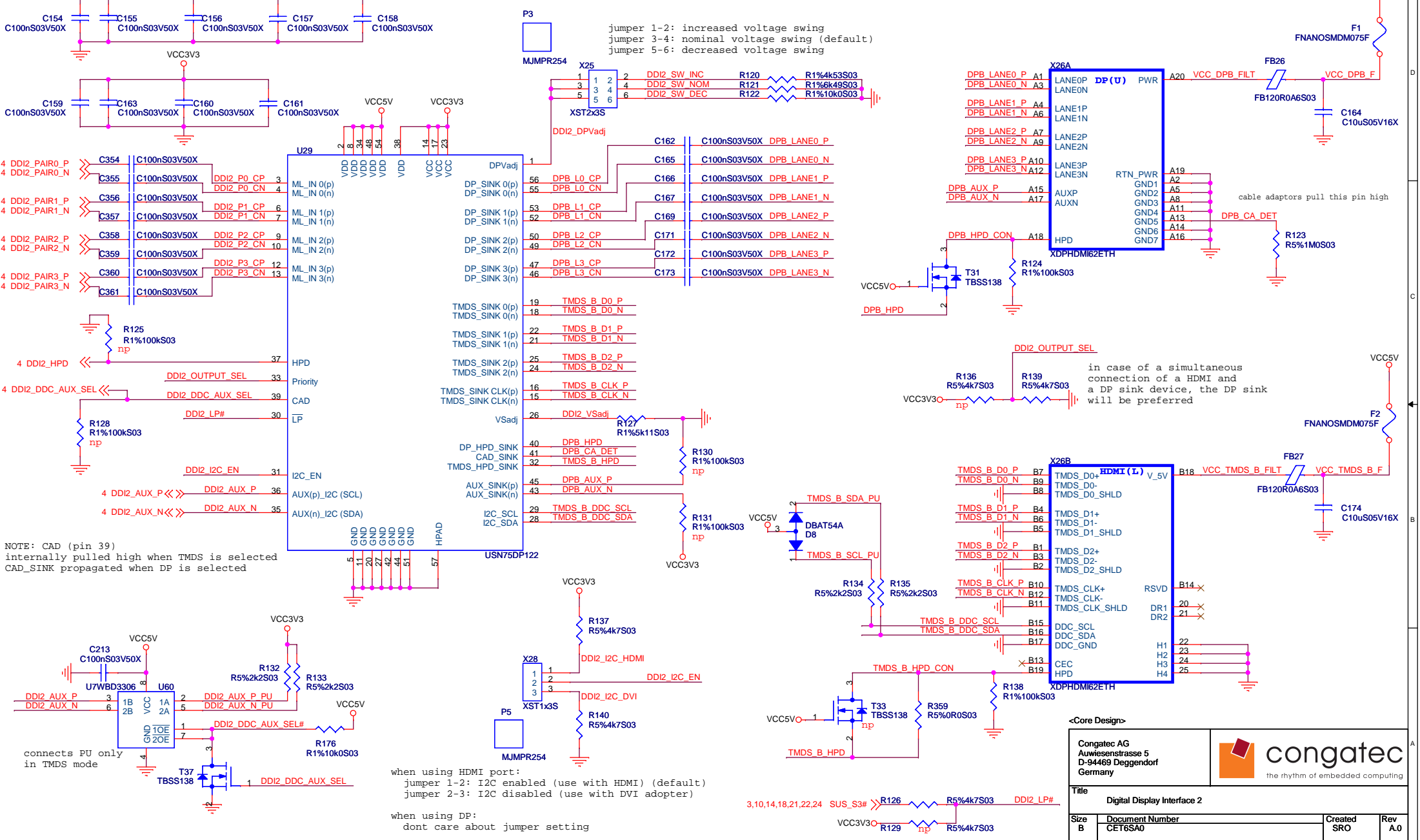
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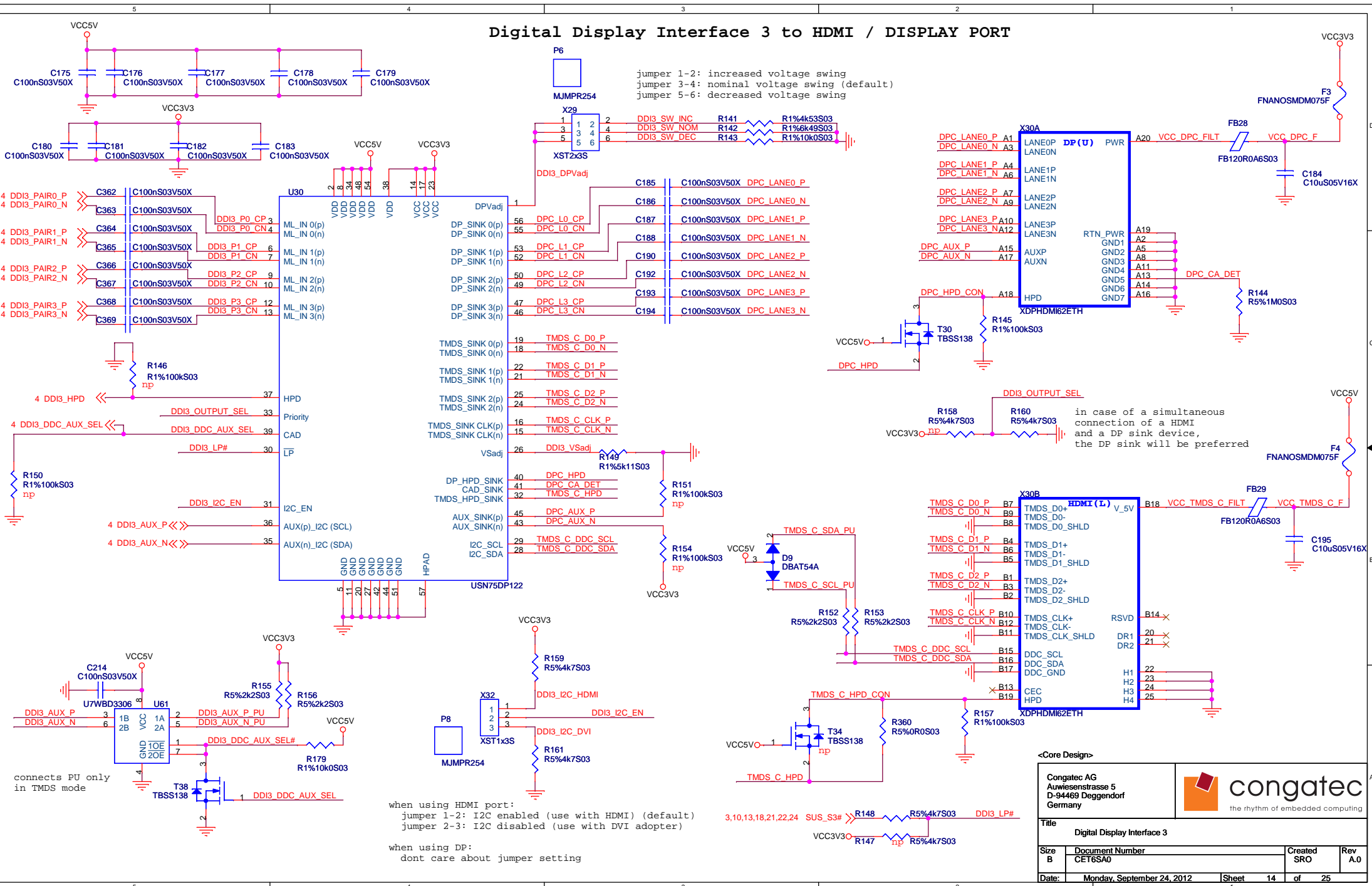
Title			
Digital Display Interface 1			
Size B	Document Number	Created SRO	Rev X.0
	CET6SX0		
Date:	Monday, December 12, 2011	Sheet 12	of 25

Digital Display Interface 2 to HDMI / DISPLAY PORT



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Title Digital Display Interface 2			
Size B	Document Number CET6SA0	Created SRO	Rev A.0
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Digital Display Interface 3 to HDMI / DISPLAY PORT



jumper 1-2: increased voltage swing
jumper 3-4: nominal voltage swing (default)
jumper 5-6: decreased voltage swing

in case of a simultaneous connection of a HDMI and a DP sink device, the DP sink will be preferred

connects PU only in TMDS mode

when using HDMI port:
jumper 1-2: I2C enabled (use with HDMI) (default)
jumper 2-3: I2C disabled (use with DVI adopter)

when using DP:
dont care about jumper setting

<Core Design>

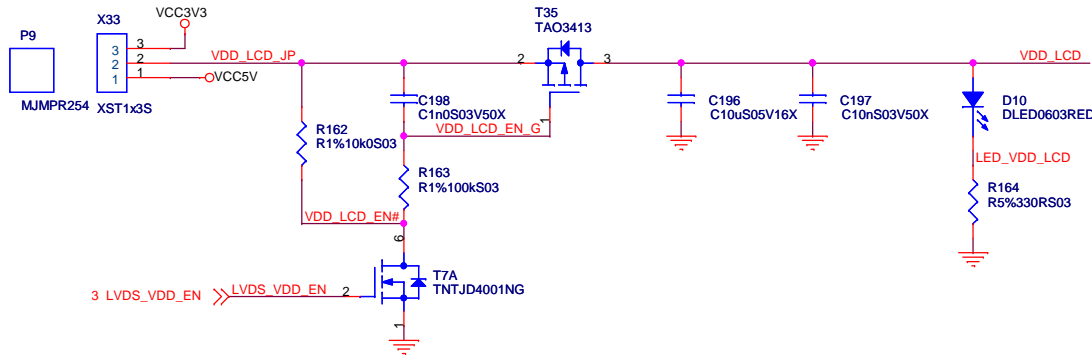
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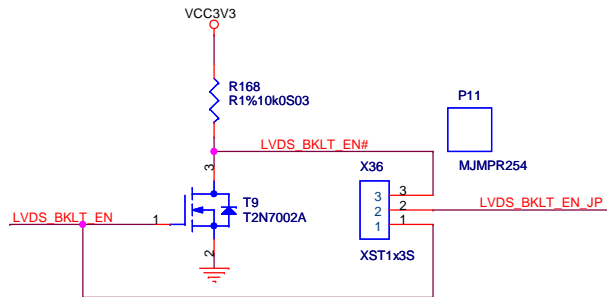
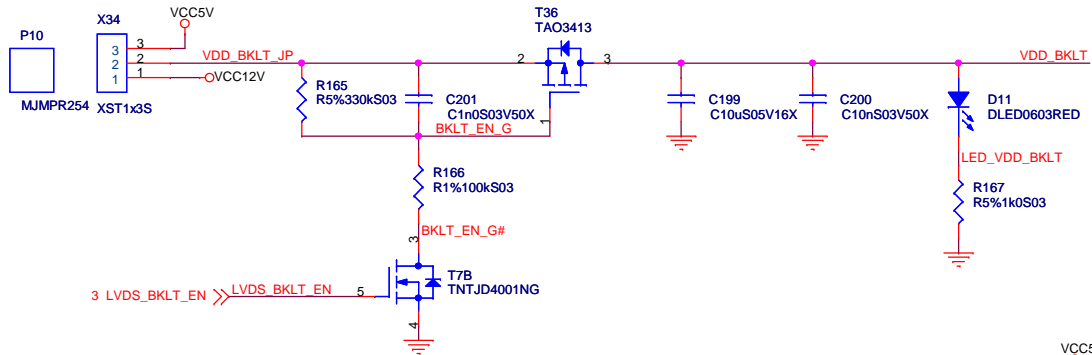
Title: Digital Display Interface 3

Size B	Document Number CET6SA0	Created SRO	Rev A.0
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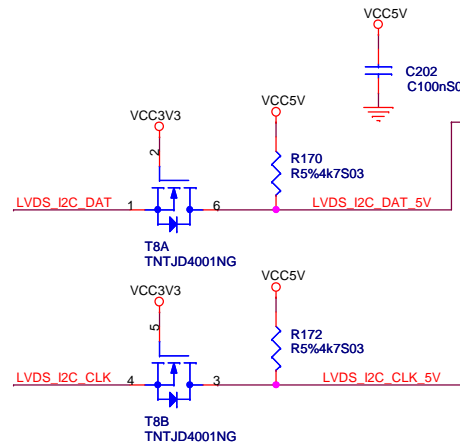
set jumper 1-2 for 5 V LCD supply voltage (default)
 set jumper 2-3 for 3.3 V LCD supply voltage



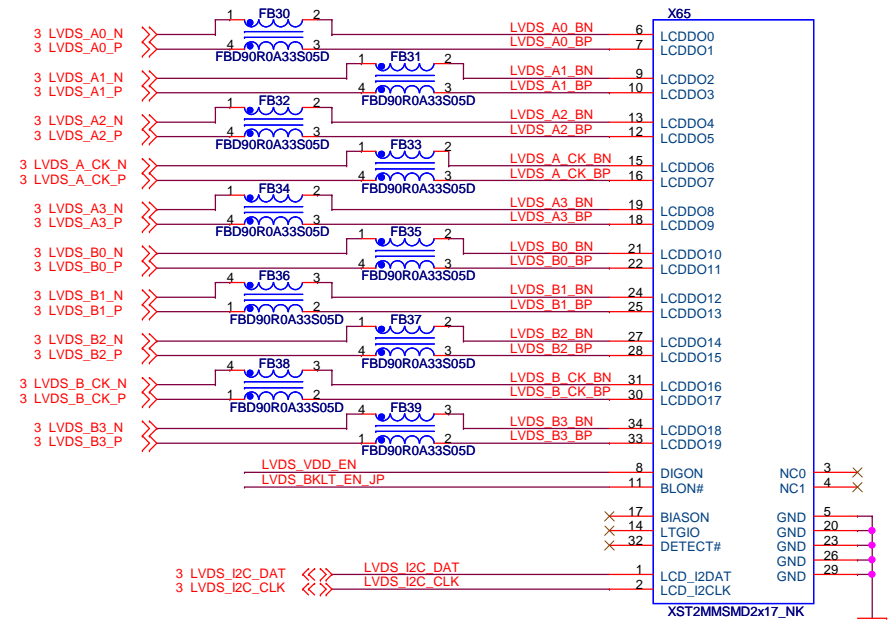
set jumper 1-2 for 12 V backlight voltage (default)
 set jumper 2-3 for 5 V backlight voltage



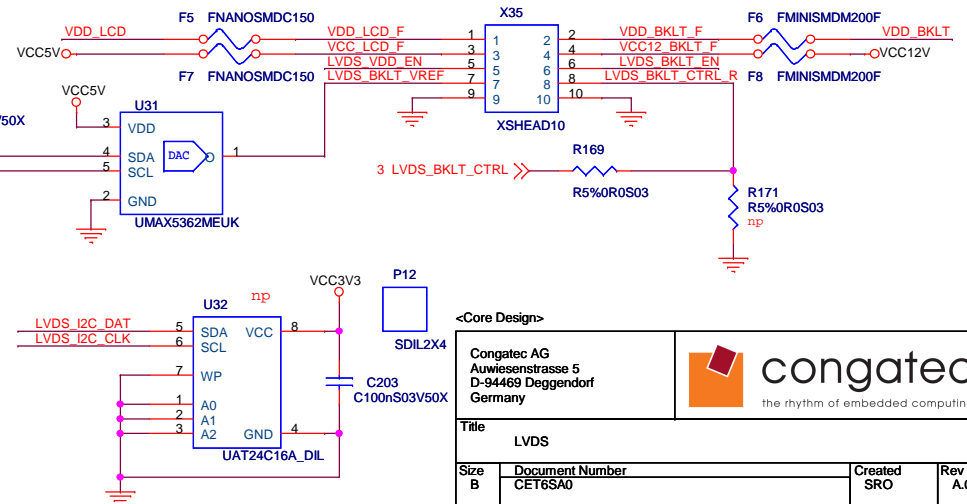
set jumper 1-2 for non-inverted BKLKT_EN signal (default)
 set jumper 2-3 for inverted BKLKT_EN signal



LCD



LCD / BKLT POWER



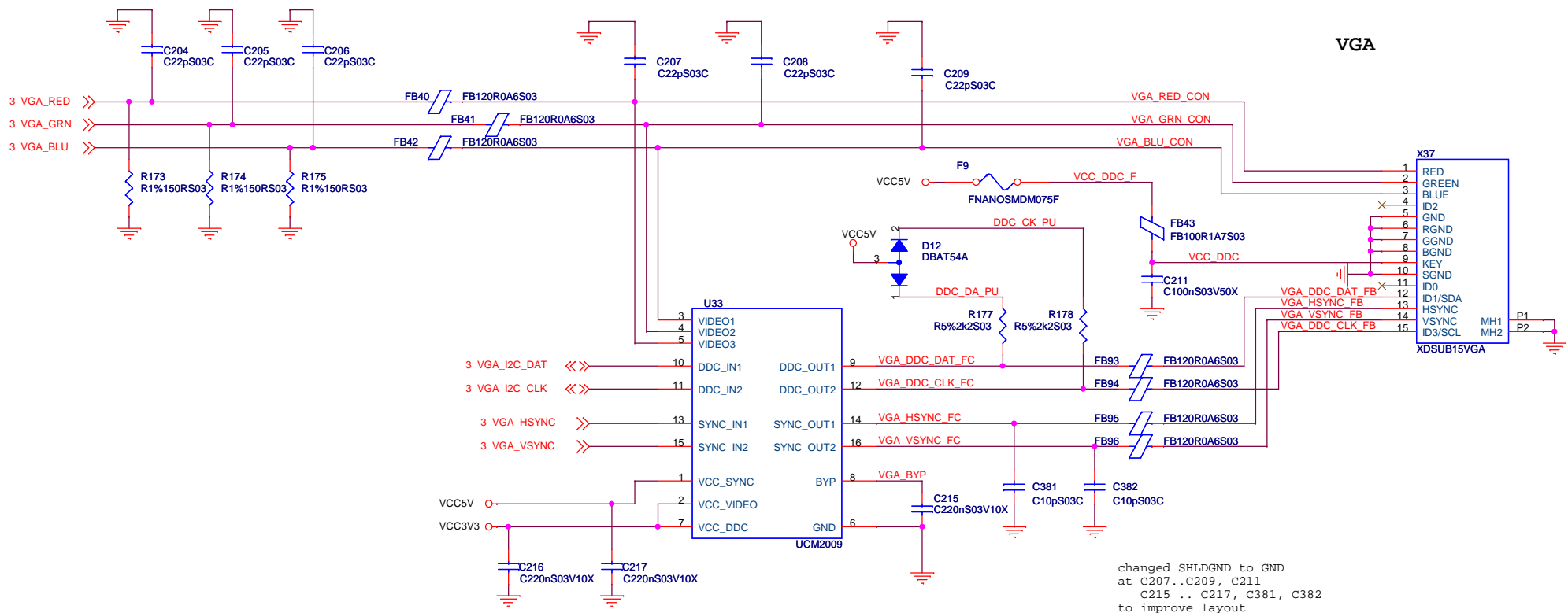
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Title: LVDS

Size B	Document Number CET6SA0	Created SRO	Rev A.0
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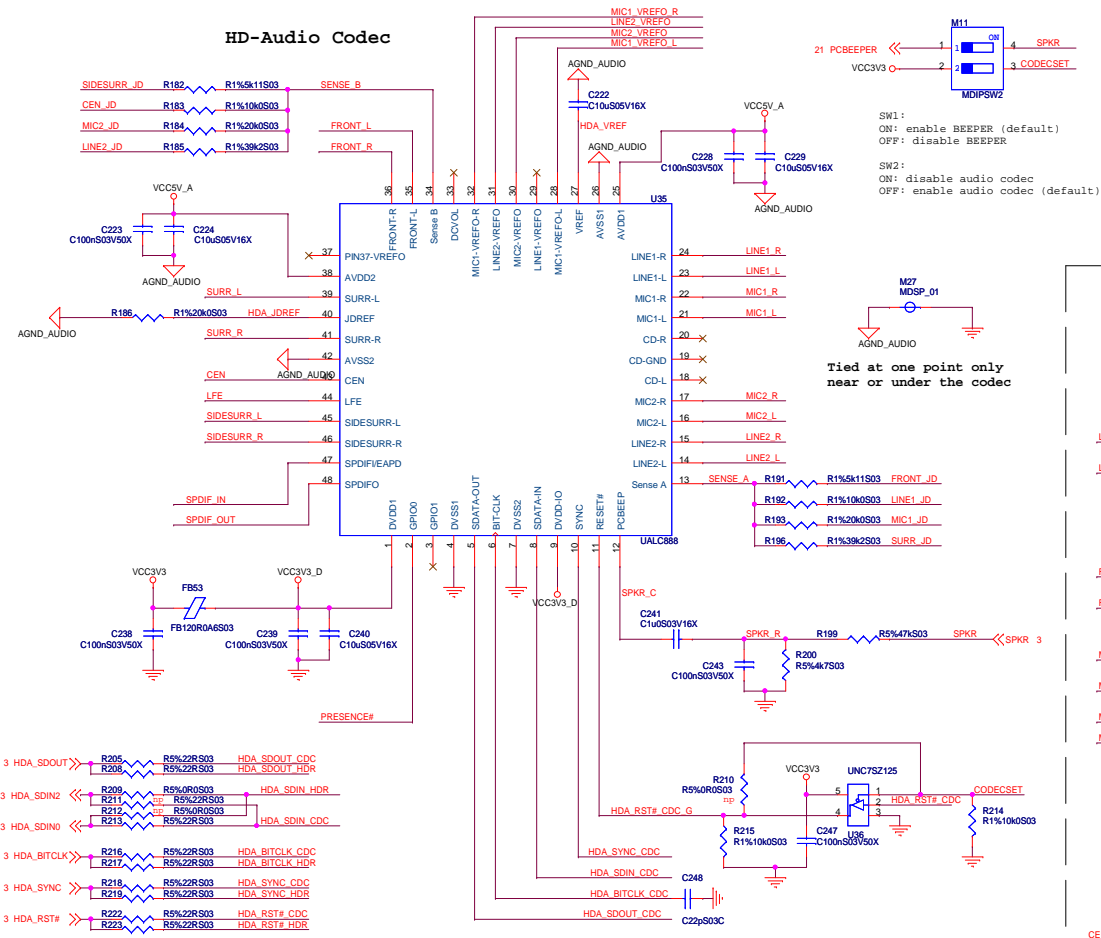


changed SHLDGND to GND
 at C207..C209, C211
 C215 .. C217, C381, C382
 to improve layout

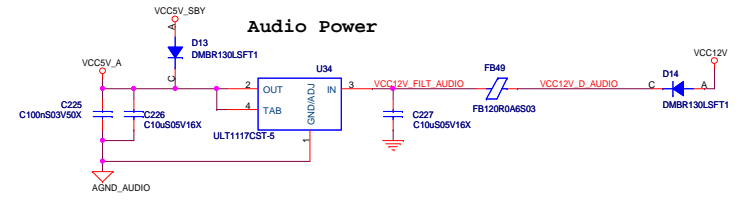
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Title VGA			
Size B	Document Number CET6SX0	Created SRO	Rev X.0
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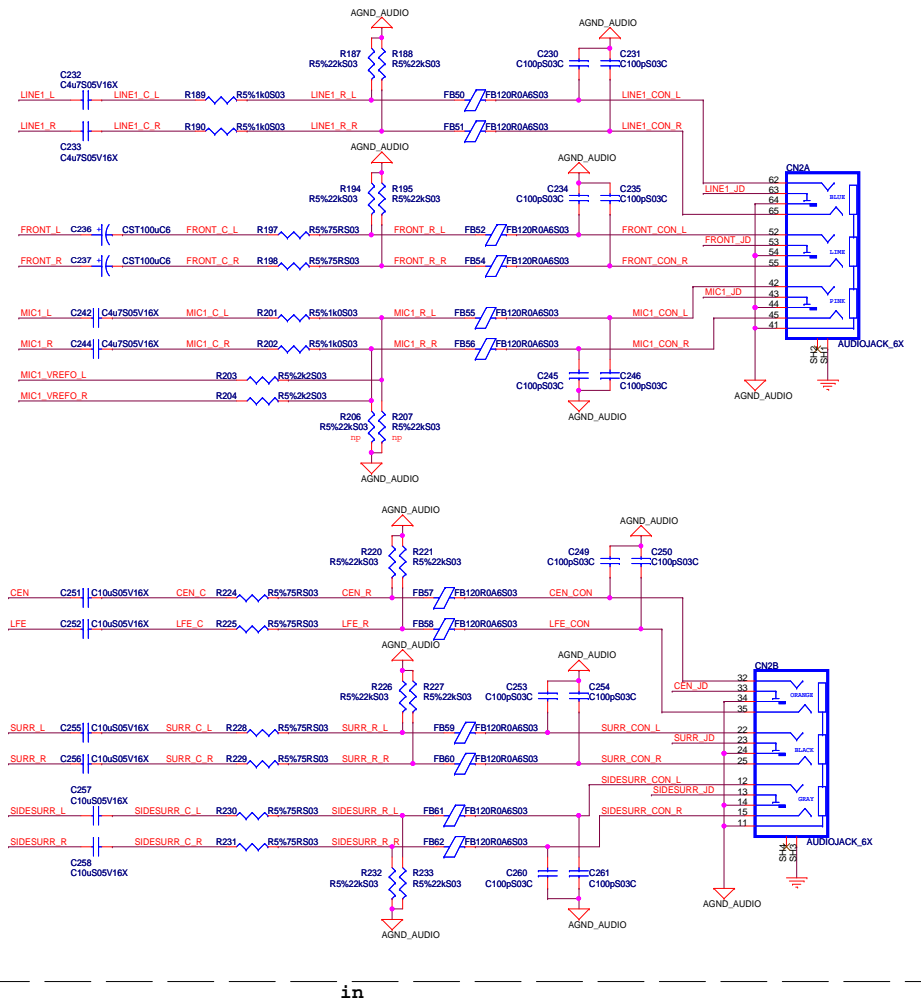
HD-Audio Codec



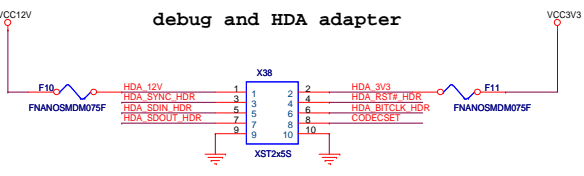
Audio Power



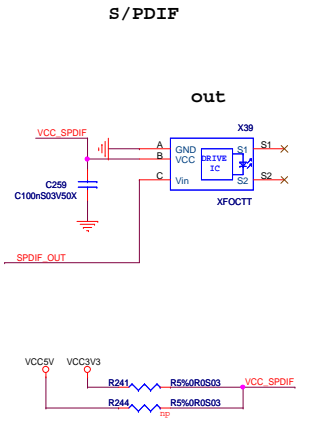
Rear Panel 7.1



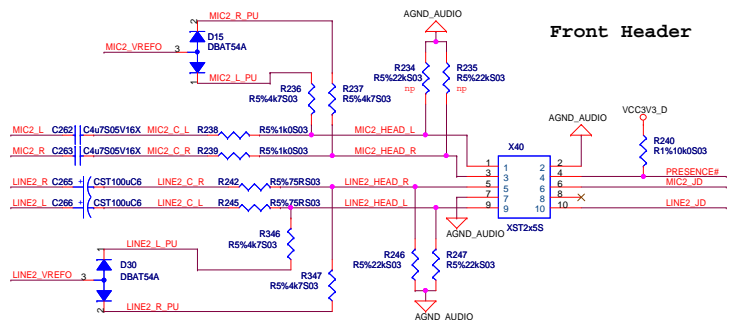
debug and HDA adapter



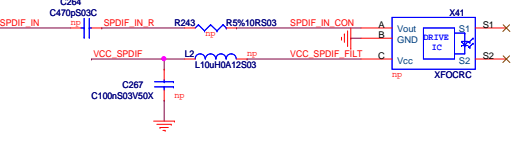
S/PDIF



Front Header



in

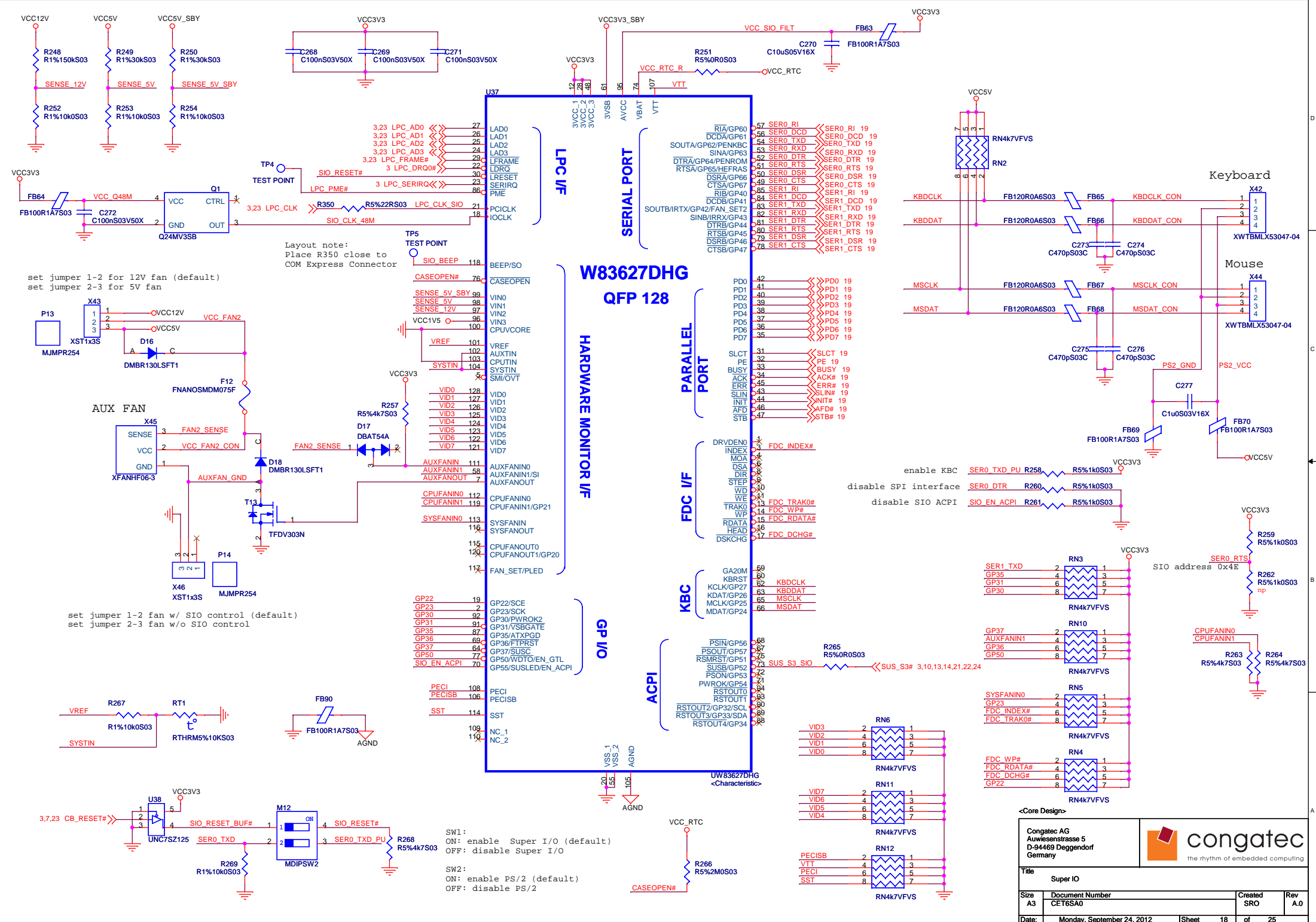


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Title		HD Audio	
Size	Document Number	Created	Rev
C	CET6850	SRO	X.0
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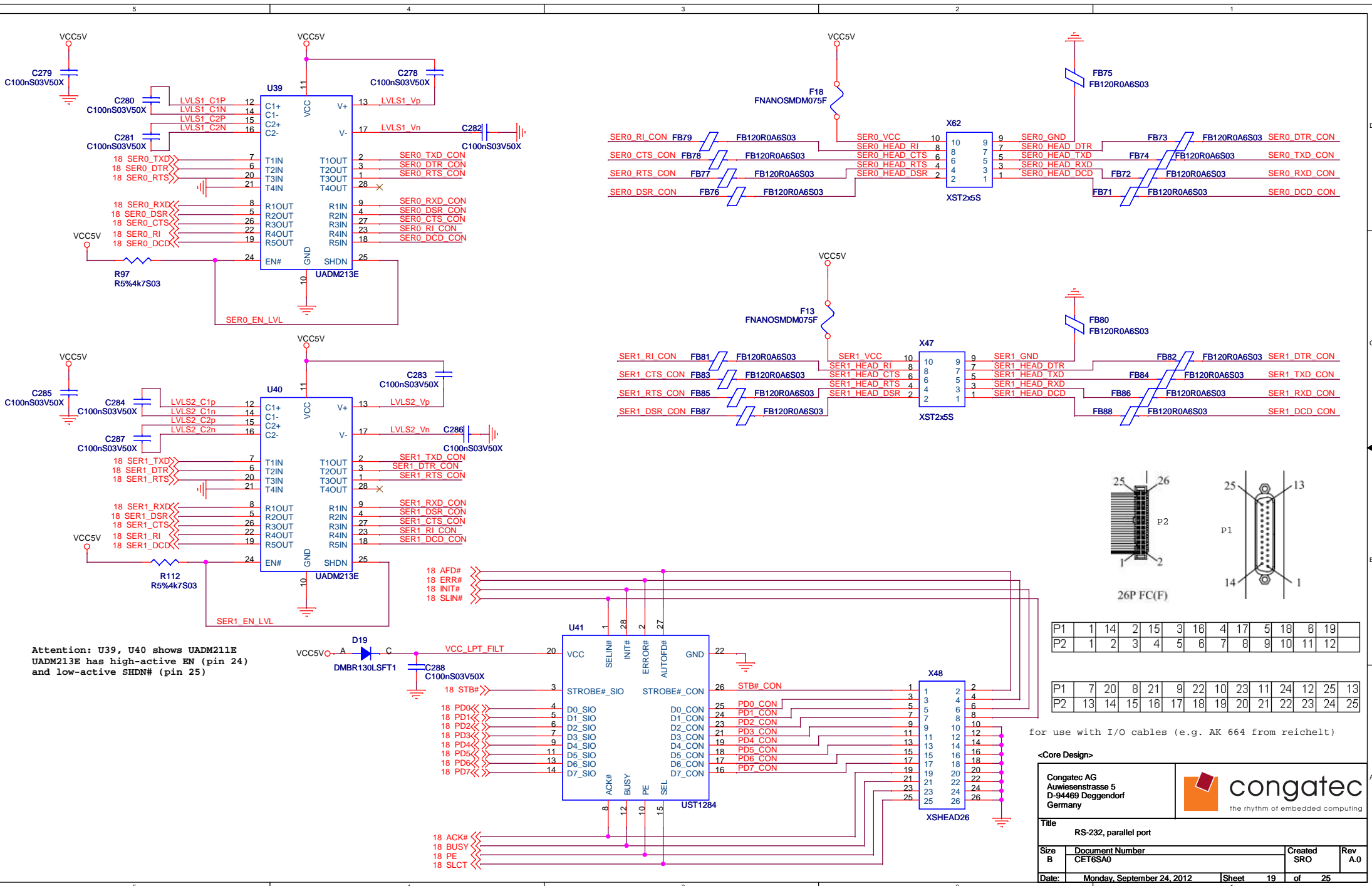
Core Design

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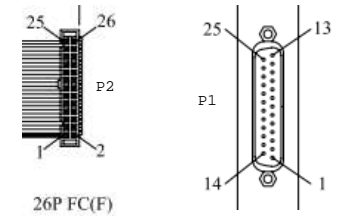
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Title: Super IO

Size A3	Document Number CET6SA0	Created SRO	Rev A.0
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Attention: U39, U40 shows UADM211E
 UADM213E has high-active EN# (pin 24)
 and low-active SHDN# (pin 25)



P1	1	14	2	15	3	16	4	17	5	18	6	19
P2	1	2	3	4	5	6	7	8	9	10	11	12

P1	7	20	8	21	9	22	10	23	11	24	12	25	13
P2	13	14	15	16	17	18	19	20	21	22	23	24	25

for use with I/O cables (e.g. AK 664 from reichelt)

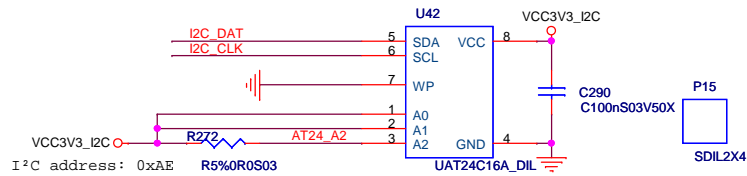
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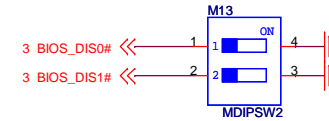
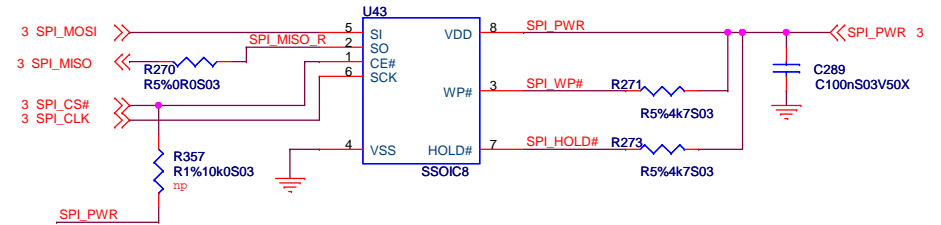
Title: RS-232, parallel port

Size B	Document Number CET6SA0	Created SRO	Rev A.0
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I²C EEPROM

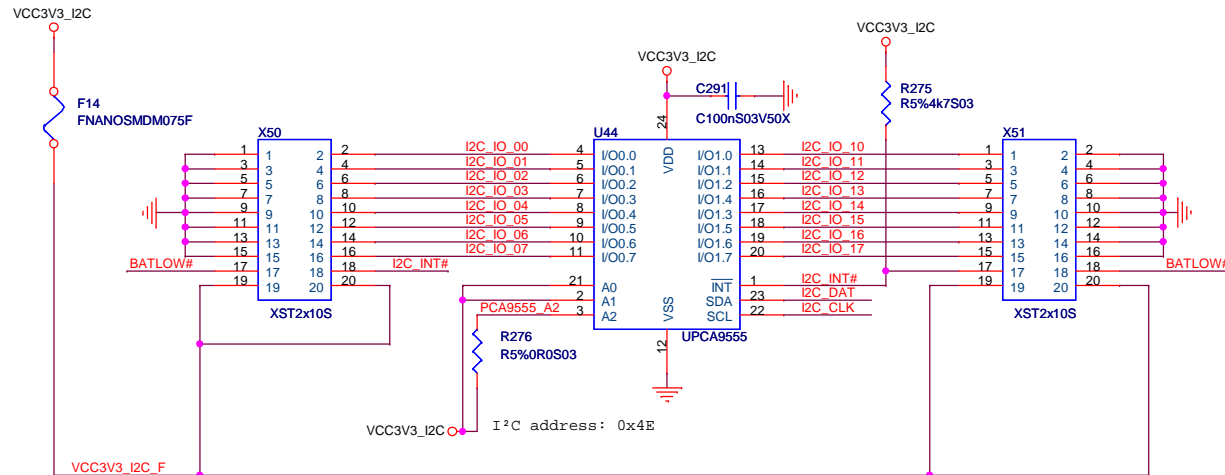


SPI BIOS Flash

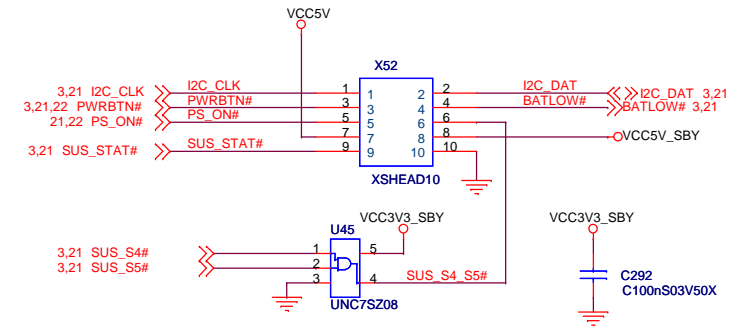


BIOS_DIS1#	BIOS_DIS0#	BIOS ENTRY / SPI_CS#
OFF	OFF	on-module firmware (default)
OFF	ON	carrier FWH (not supported)
ON	OFF	carrier firmware from SPI
ON	ON	on-module firmware, carrier SPI contains management data

Digital IO over I2C



Battery Support



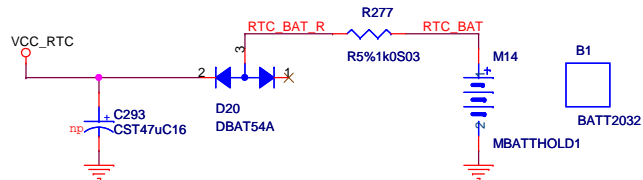
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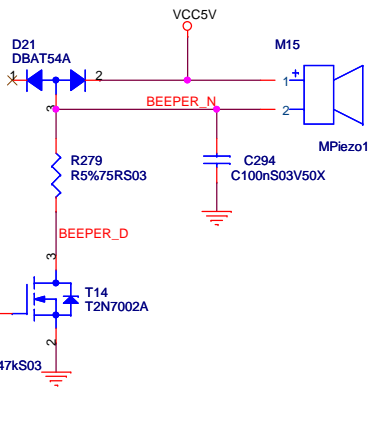


Title		SPI, I2C, Battery Support	
Size B	Document Number	Created SRO	Rev A.0
	CET6SA0		
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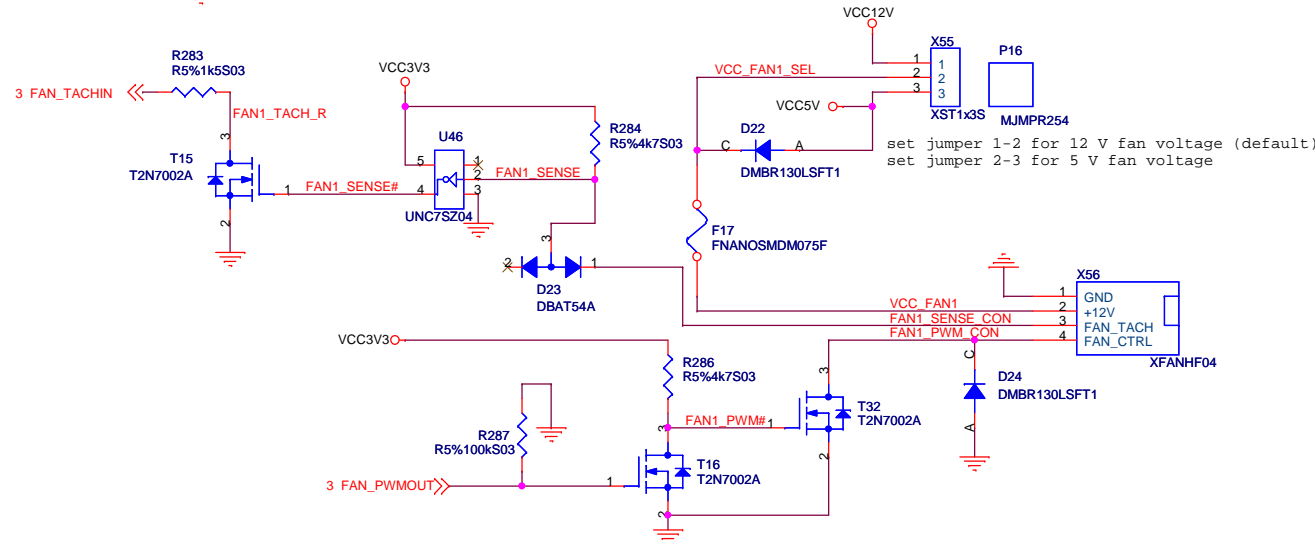
RTC / CMOS Battery



PC BEEPER

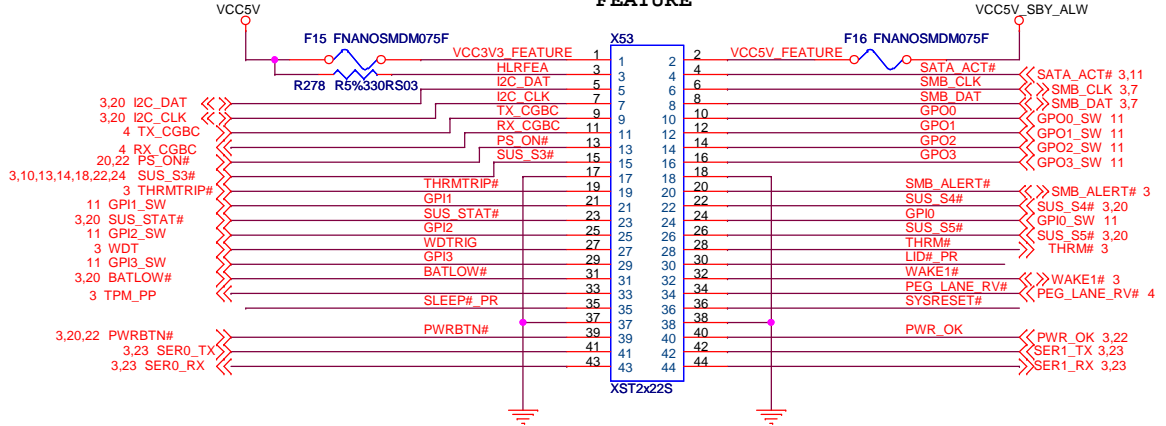


FAN Control

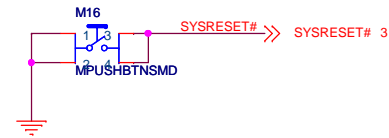


SRO, A.0:
changed to 5V to be compatible to previous platforms

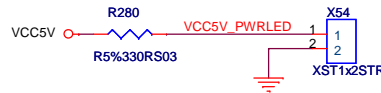
FEATURE



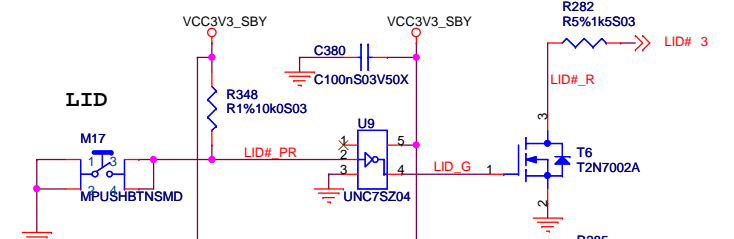
RESET



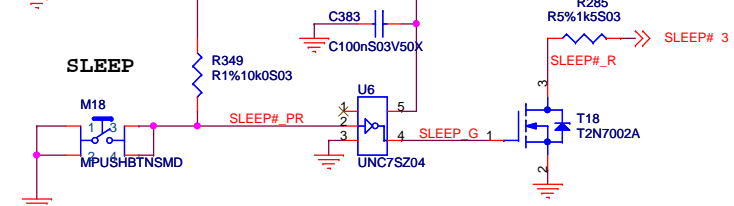
PWR LED



LID



SLEEP



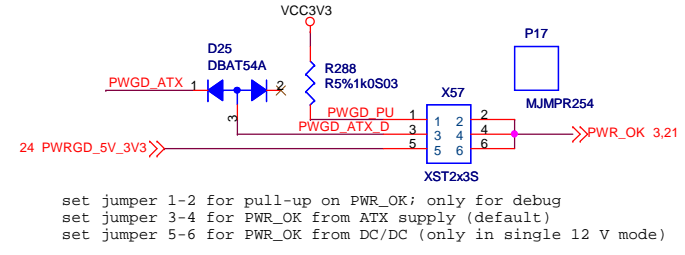
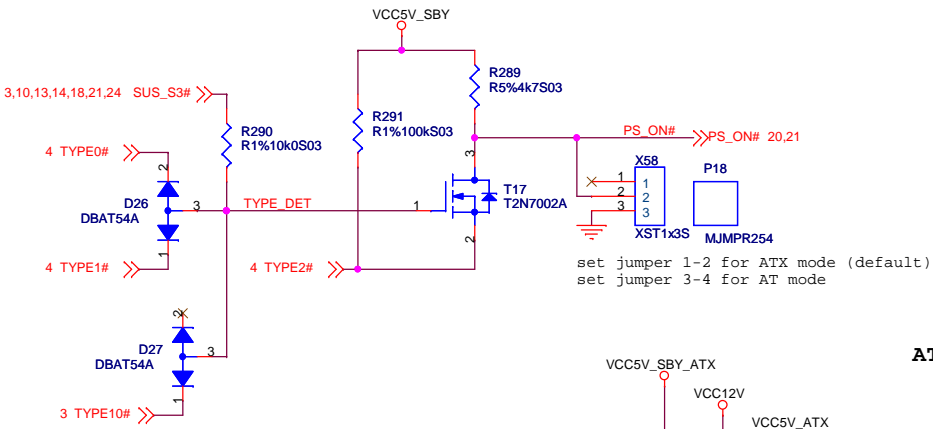
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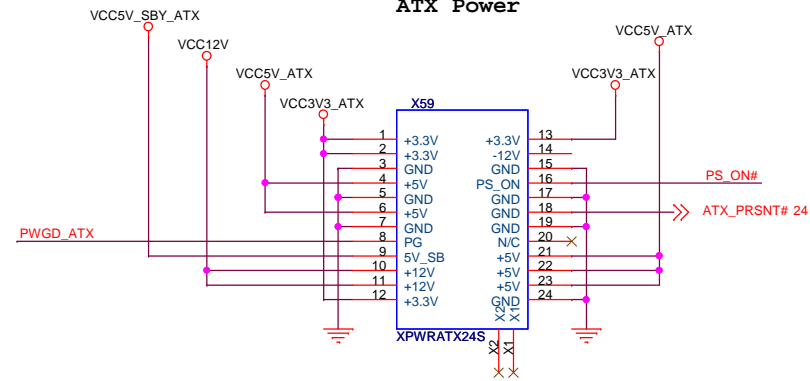


Title		CMOS Battery, Speaker, FAN, Feature Connector	
Size B	Document Number	Created	Rev
	CET6SA0	SRO	A.0
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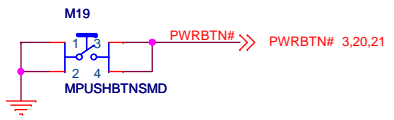
Type detection



ATX Power

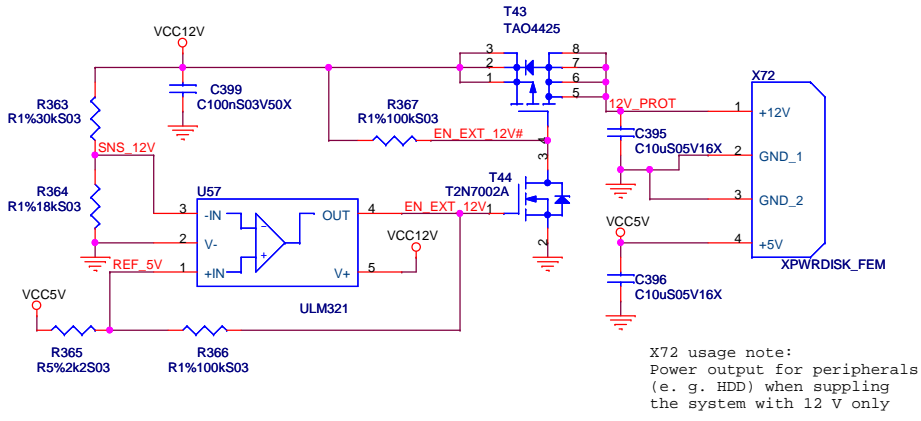


Power Button

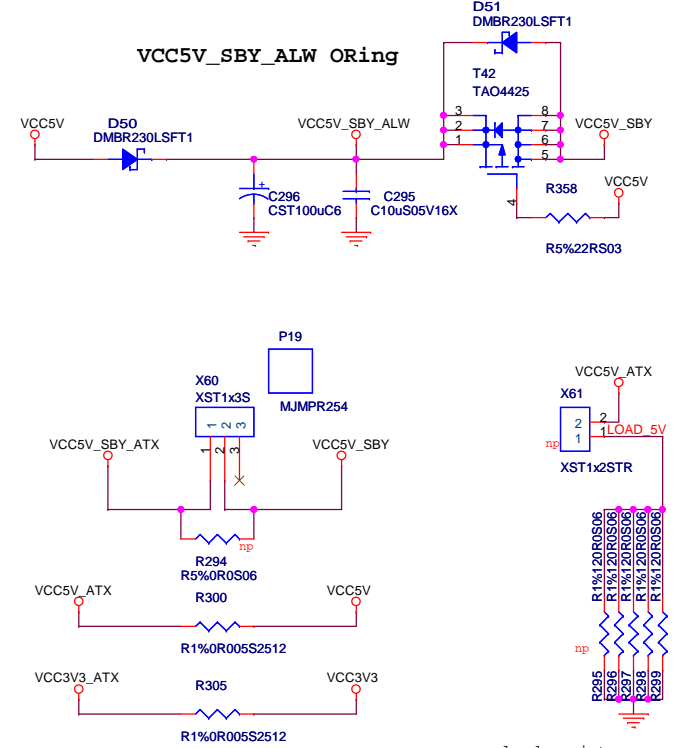


SRO, A.0: overvoltage protection:
 disables +12V at X72 at about 13.6V

Disk Drive Power



VCC5V_SBY_ALW Oring



load resistors
 causing additional 200 mA
 load current at 5V_ATX
 helping ATX PSU to turn on

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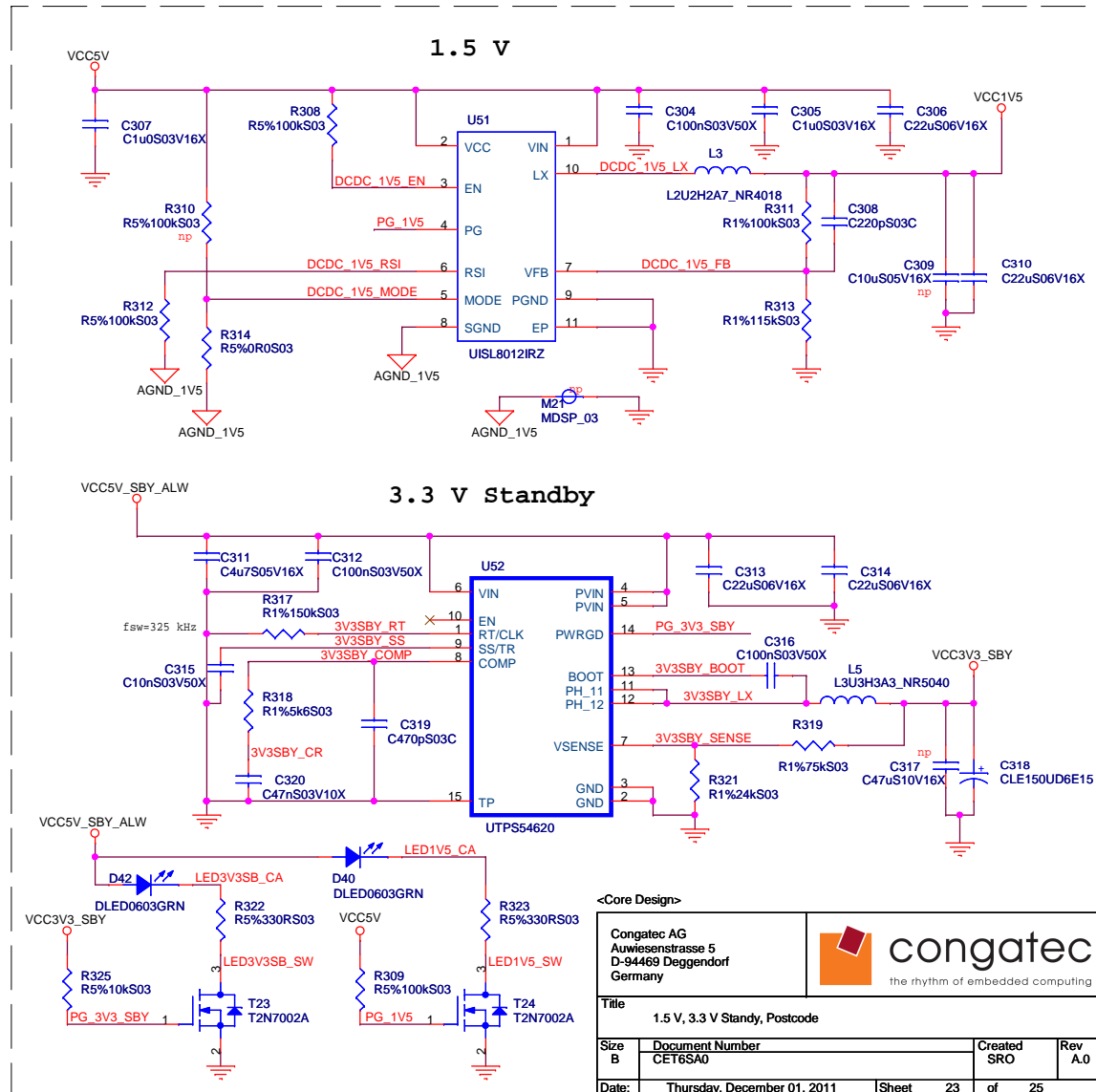
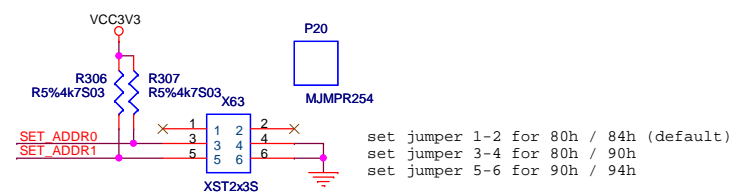
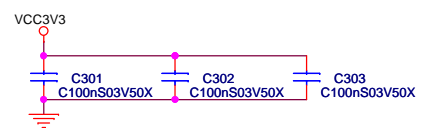
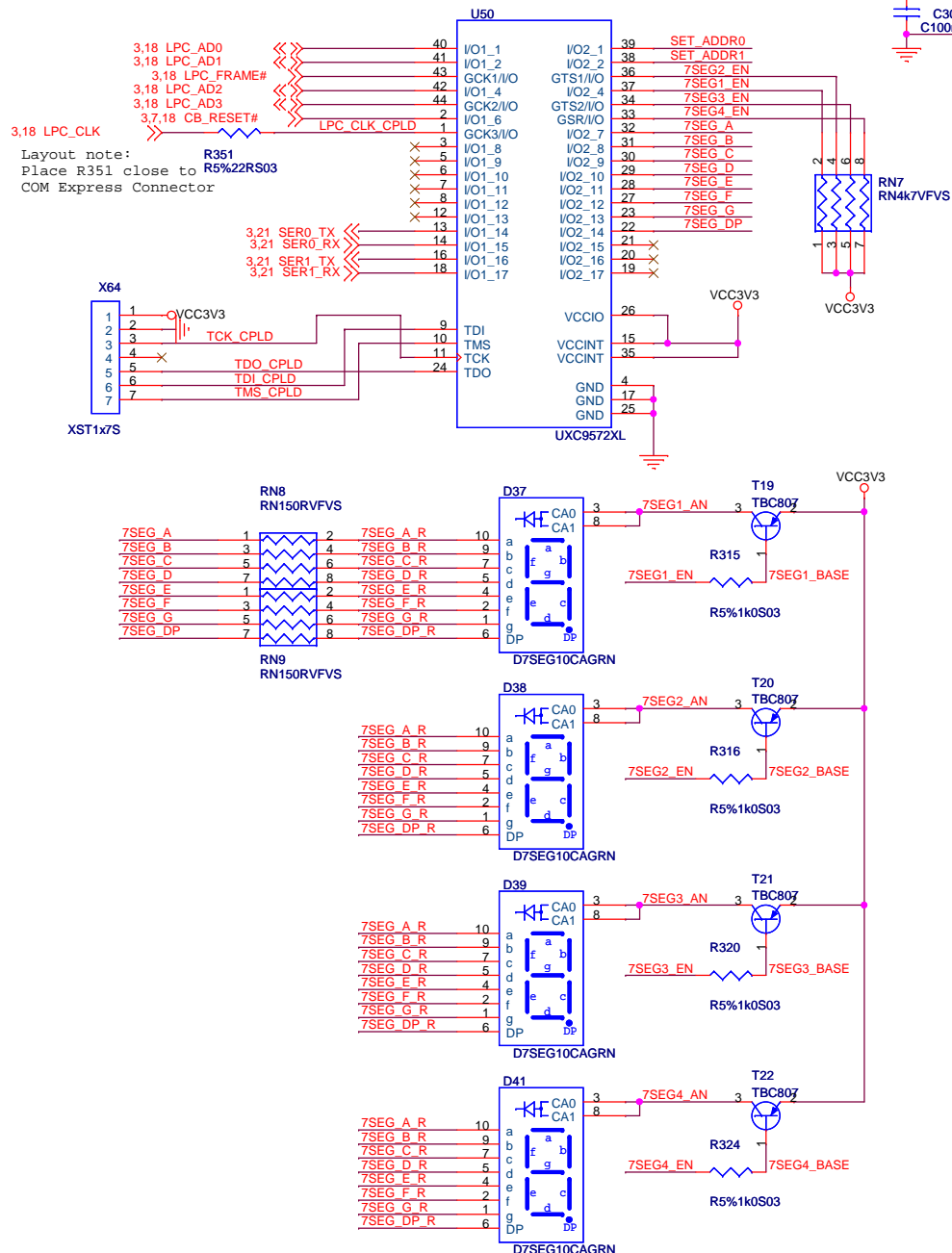
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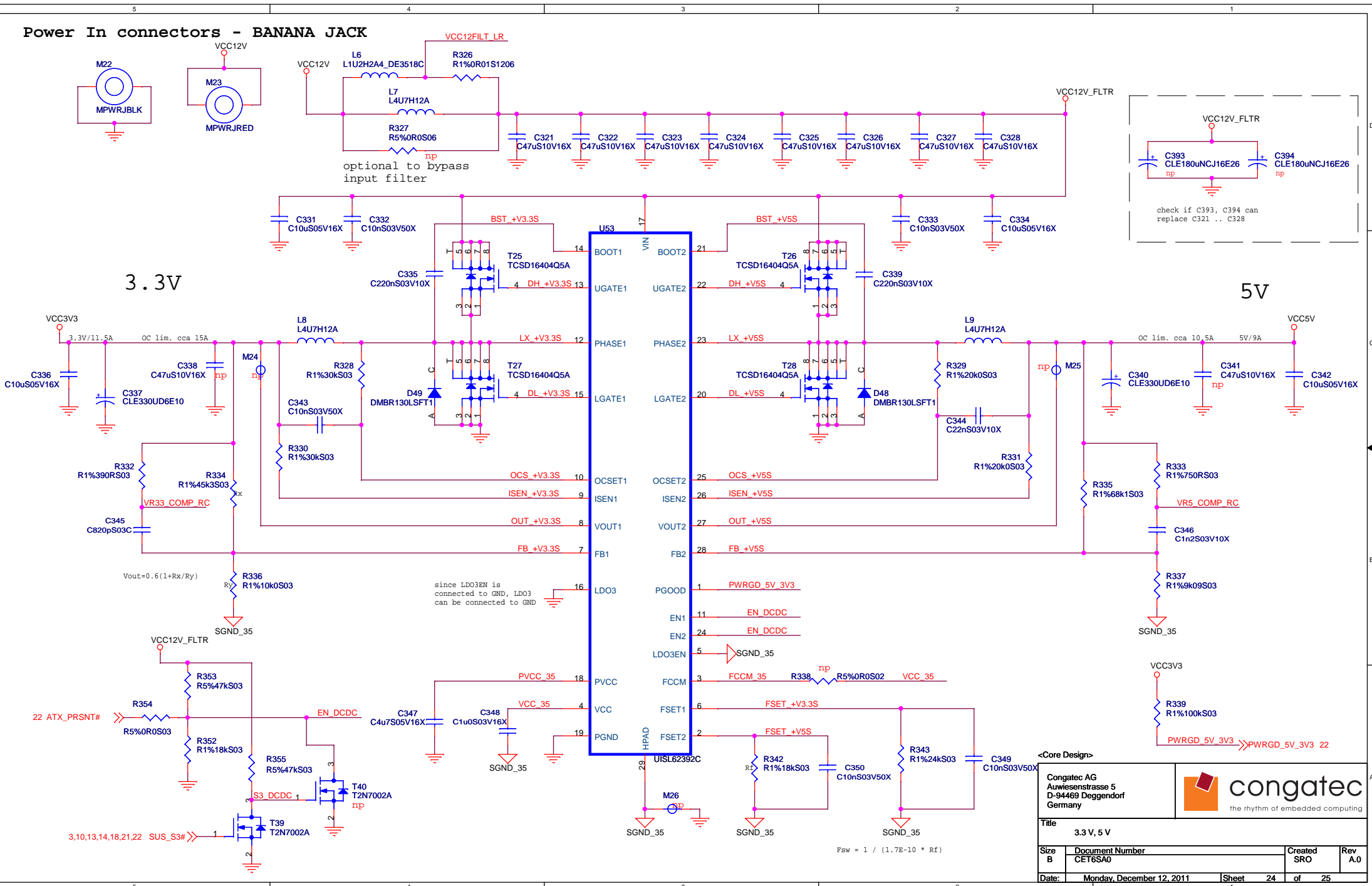
Title: ATX Power, 5V Standby Always

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Postcode Display



Power In connectors - BANANA JACK



VCC12V_FLTR

C393 CLE180uNCJ16E26 np
C394 CLE180uNCJ16E26 np

check if C393, C394 can replace C321 ... C328

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Title: 3.3 V, 5 V

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$P_{sw} = 1 / (1.7E-10 * R_f)$

HISTORY


10.01.2011 SRO design created

19.08.2011 SRO

- page 3: set SUS_S3# buffer to be populated
- page 4: swapped connection of DDI2_AUX, DDI3_AUX
- page 6: changed SHLDGND - GND connection
- page 7: exchanged UPI6C21200 by UICS9DB1233 (PCIe Gen. 3 compatible Clock Buffer)
- page 9: connected X12.B17, B31, B81 to B48, to enable PCIe RefClk also with x1, x4 and x16 cards
- page 11: exchanged SATA connectors
- page 13, 14: swapped connection of TMDS_B_CLK and TMDS_C_CLK at U29, U30,
added circuitry to connect DDC-PU only in TMDS mode
- page 18: changed oscillator at Super I/O from 48 MHz to 24 MHz
mirrored X42, X44 to be compatible to conga-adapPS2
- page 19: connected U39.24, U39.25, U40.24, U40.25 to VCC5V to enable RS232 Levelshifter
swapped DTR and TXD signals at X47, X62 to maintain compatibility to conga-CEVAL
- page 20: added PU at SPI_CS# to ensure stable level at SPI flash
- page 21: changed connection of X53.1 and X53.3 from 3.3V to 5V
- page 22: changed VCC5V_SBY_ALW Oring circuit
added overvoltage protection circuit to Disk Drive Power Connector

General: changed connection of I/O connector's shield from SHLDGND to GND
General: changed CLE150UC6E25 to CLE150UD6E15

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Title History			
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