CET6
COM.0 Type 6 Evaluation Baseboard
Rev. A.0

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Variants
Base   Standard w/ SuperIO W83627-DHG-P
USB 3.0 spec. requires low ESR cap (>= 120 µF) directly connected to I/O connector.

Layout note:
- Place D46, D47 close to X3 and X4
- Place D44, D45 close to X3 and X4
set jumper 1-2 if LAN Controller is powered from standby voltage (default)
set jumper 2-3 if LAN Controller is powered from 5V voltage
set jumper 1-2 for SDIO
set jumper 2-3 for GPIO (default)
Digital Display Interface 2 to HDMI / DISPLAY PORT

Jumper 1-2: increased voltage swing
Jumper 3-4: nominal voltage swing (default)
Jumper 5-6: decreased voltage swing

In case of a simultaneous connection of a HDMI and a DP sink device, the DP sink will be preferred

NOTE: CAD (pin 39) internally pulled high when TMDS is selected
SUS_S3# 3, 10, 14, 18, 21, 22, 24

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set jumper 1-2 for 5 V LCD supply voltage (default)
set jumper 2-3 for 3.3 V LCD supply voltage

set jumper 1-2 for 12 V backlight voltage (default)
set jumper 2-3 for 5 V backlight voltage

set jumper 1-2 for non-inverted BLKT_EN signal (default)
set jumper 2-3 for inverted BLKT_EN signal

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**LCD**

- **LVDS DC CLK**
- **LVDS DC DAT**
- **LVDS I2C CLOCK**
- **LVDS I2C DATA**
- **LVDS VDD EN**
- **LVDS B KLT EN**
- **LVDS B KLT VREF**
- **LVDS B KLT CTRL**

**LCD / BKLT POWER**

- **VDD LCD**
- **VDD BKLT**
- **VDD DC CLK**
- **VDD I2C CLOCK**
- **VDD I2C DATA**
- **VDD VDD EN**
- **VDD BKLT**
- **VDD DIO**
- **VDD BLKLT J**
- **VDD DETECT**

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**Title**

LVDS

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**Title**

LVDS

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**Sheet**

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**Date**

Monday, September 24, 2012
changed SHLDGND to GND at C207..C209, C211
C215 .. C217, C381, C382
to improve layout
Attention: U39, U40 shows UADM211E UADM213E has high-active EN (pin 24) and low-active SHDN# (pin 25) and low-active SHDN# (pin 25)
Digital IO over I2C

Battery Support

I2C EEPROM

SPI BIOS Flash

<table>
<thead>
<tr>
<th>BIOS_DIS1#</th>
<th>BIOS_DIS0#</th>
<th>BIOS ENTRY / SPI_CS#</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>on-module firmware (default)</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
<td>carrier FWH (not supported)</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>carrier firmware from SPI</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>on-module firmware, carrier SPI contains management data</td>
</tr>
</tbody>
</table>

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- Changed VCC to 5V to be compatible with previous platforms.

**FEATURE**

- **VCC5V**: 5V power supply.
- **VCC5V_SBY_ALW**: standby power supply.
- **R277**: resistor.
- **F15 FNANOSMDM075F**: a component.

**RTC / CMOS Battery**

- **R277**: resistor.
- **R5%100kS03**: 100k ohm resistor.
- **F16 FNANOSMDM075F**: a component.
- **C293**: capacitor.

**PC BEEP**

- **D21 DBAT54A**: a component.
- **M16 MPUSHBTNSMD**: a component.
- **R280**: resistor.

**FAN Control**

- **FAN1_PWMOUT**: a pin.
- **FAN1_SENSE**: a pin.

**REPLACE**

- **X53**: a pin.

**FEATURE**

- **X53**: a pin.
- **F16 FNANOSMDM075F**: a component.

**RESET**

- **M16 MPUSHBTNSMD**: a component.
- **SYRESET**: a pin.

**LID**

- **R348**: resistor.
- **R349**: resistor.
- **U6 UNC7SZ04**: an IC.
- **T32 T2N7002A**: a transistor.

**SLEEP**

- **M18 MPUSHBTNSMD**: a component.
- **SLEEP_G**: a pin.

**PWR LED**

- **VCC5V_PWRLED**: power supply for the LED.
- **X54**: a pin.
- **R282**: resistor.
### Type Detection

<table>
<thead>
<tr>
<th>Type</th>
<th>Type 2</th>
<th>Type 2 Rev 1.0</th>
<th>Type 2 Rev 2.0</th>
<th>Type 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type0#</td>
<td>N.C.</td>
<td>N.C.</td>
<td>N.C.</td>
<td>N.C.</td>
</tr>
<tr>
<td>Type1#</td>
<td>N.C.</td>
<td>N.C.</td>
<td>N.C.</td>
<td>N.C.</td>
</tr>
<tr>
<td>Type10#</td>
<td>Type2#</td>
<td>Type1#</td>
<td>Type0#</td>
<td>Type 2 Rev 1.0: 12 V N.C. N.C. N.C. Type 2 Rev 2.0: N.C. N.C. N.C. N.C. Type 6: N.C. GND N.C. N.C.</td>
</tr>
</tbody>
</table>

### ATX Power

- **VCC5V_SBY**
- **VCC5V**
- **VCC12V**
- **VCC3V3**

**Set jumper 1-2 for ATX mode (default)**

**Set jumper 3-4 for AT mode**

**Load resistors causing additional 200 mA load current at 5V_ATX helping ATX PSU to turn on**

### Disk Drive Power

- **C298**
- **C299**
- **C300**

**Set jumper 1-2 for pull-up on PWR_OK only for debug**

**Set jumper 3-4 for PWR_OK from ATX supply (default)**

**Set jumper 5-6 for PWR_OK from DC/DC (only in single 12 V mode)**

### Power Button

- **M19**

**Set jumper 1-2 for PWR_OK from ATX supply (default)**

**Set jumper 3-4 for PWR_OK from DC/DC (only in single 12 V mode)**

**Overvoltage protection: disables +12V at X72 at about 13.6V**

### Disk Drive Power Usage Note

- **X72 usage note:** Power output for peripherals (e.g. HDD) when supplying the system with 12 V only
HISTORY

10.01.2011    SRO    design created

19.08.2011    SRO
page 3: set SUS_S3# buffer to be populated
page 4: swapped connection of DDI2_AUX, DDI3_AUX
page 6: changed SHLDGND - GND connection
page 7: exchanged UP16C21200 by UICS9DB1233 (PCIe Gen. 3 compatible Clock Buffer)
page 9: connected X12.B17, B31, B81 to B48, to enable PCIe RefClk also with x1, x4 and x16 cards
page 11: exchanged SATA connectors
page 13, 14: swapped connection of TMDS_B_CLK and TMDS_C_CLK at U29, U30,
added circuitry to connect DDC-PU only in TMDS mode
page 18: changed oscillator at Super I/O from 48 MHz to 24 MHz
mirrored X42, X44 to be compatible to conga-adapPS2
page 19: connected U39.24, U39.25, U40.24, U40.25 to VCC5V to enable RS232 Levelshifter
swapped DTR and TXD signals at X47, X62 to maintain compatibility to conga-CEVAL
page 20: added PU at SPI_CS# to ensure stable level at SPI flash
page 21: changed connection of X53.1 and X53.3 from 3.3V to 5V
page 22: changed VCC5V_SBY_ALW Oring circuit
added overvoltage protection circuit to Disk Drive Power Connector

General: changed connection of I/O connector's shield from SHLDGND to GND
General: changed CLE150UC6E25 to CLE150UD6E15

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Title
History

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A4 CET6SX0 SRO X.0

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