USER GUIDE

COMh-sdID (E2)

Rev 1.2

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1. General Information

1.1 Disclaimer

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Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Follow the “General Safety Instructions” supplied with the product.

You find the most recent version of the “General Safety Instructions“ online in the download area of this product on our JUMPtec website.

This product is not suited for storage or operation in corrosive environments, in particular under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact JUMPtec Support.

1.3 Terms and Conditions

JUMPtec warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit https://www.jumptec.com/en/terms-and-conditions.

JUMPtec sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit https://www.jumptec.com/en/terms-and-conditions.

For contact information, please visit our website CONTACT US.

1.4 Customer Support

Find JUMPtec contacts by visiting: https://www.jumptec.com/en/service-support.

1.5 Customer Service

As a trusted technology innovator and global solutions provider, JUMPtec extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables JUMPtec to provide exceptional peace of mind to build and maintain successful products. For more details on JUMPtec's service offerings such as: enhanced repair services, extended warranty, training academy, and more visit https://www.jumptec.com/en/service-support.

1.6 Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact JUMPtec Support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

1.7 Symbols

The following symbols may be used in this user guide of COMh-sdID

Simple Box

Info-Box

Important-Box

Alert-Box

Tip-Box

Help-Box

Todo-Box

Download-Box

1.8 For Your Safety

Your new JUMPtec product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new JUMPtec product, you are requested to conform with the following guidelines.

1.9 High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

Electric Shock!

Before installing a non hot-swappable JUMPtec product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product. Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

1.10 Special Handling and Unpacking Instruction

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes

unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

1.11 Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

1.12 General Instructions on Usage

In order to maintain JUMPtec's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by JUMPtec and described in this user guide or received from JUMPtec Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account. In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product, then re-pack it in the same manner as it was delivered. Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

1.13 Quality and Environmental Management

JUMPtec aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding JUMPtec's quality and environmental responsibilities, visit https://www.jumptec.com/en/about-jumptec/quality.

1.13.1 Disposal and Recycling

JUMPtec's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

1.13.2 WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with JUMPtec.

JUMPtec follows the WEEE directive.

You are encouraged to return our products for proper disposal.

2. Introduction

This user guide describes the COM-HPC® Server Size D Computer-On-Module COMh-sdID made by JUMPtec and focuses on describing the module's special features. JUMPtec recommends users to study this user guide before powering on the module.

2.1 Product Naming Clarification

COM-HPC® defines a Computer-On-Module (COM), with all the components necessary for a bootable host computer, packaged as a super component. The product name for JUMPtec COM-HPC® Computer-On-Modules consists of:

Standard short form	Type	Module size	Processor family identifier	Available temperature variants
COMh-	m = mini c = client s = server	7 = Size (95mm x 70mm) a = Size A (95mm x 120mm) b = Size B (120mm x 120mm) c = Size C (160mm x 120mm) d = Size D (160mm x 160mm) e = Size E (200mm x 160mm)	ID = IceLake D AP = AlderLake P AS = AlderLake S etc.	none= Commercial Extended (E1) Industrial (E2) Screened industrial (E2S)

Table 1: COM-HPC® Product Naming Clarification

2.2 Product description

The COMh-sdID with scalability from 4 to 20 cores and SKUs for an extended temperature range and 24×7 / 10 years reliability allows very robust implementations for harsh environments and extreme conditions in a small mechanical footprint.

The module accommodates 4x DIMM sockets for a max. of 512GB DDR4 memory at 3200 MT/s. As storage medium, a soldered NVMe SSD onboard with up to 1 TByte (TLC) storage capacity is optionally available.

With 48x PCIe lanes (32x PCIe Gen4 plus 16x PCIe Gen3 lanes) and 2x Quad LAN interfaces supporting 100Gb Ethernet, the COMh-sdID is an ideal platform for high data throughput requirements in demanding I/O and network structures.

Key features are:

- Size D form factor – 160 x 160 mm
- Intel Xeon D-2700/D-2800 (formerly Ice Lake D) Server platform

- Up to 20 cores, processor TDP up to 125W
- 32x PCIe Gen 4.0 lanes + 16x PCIe Gen 3.0 lanes
- 8x LAN Ports for various configurations - up to 100GbE
- Memory: Max 512GB DDR4-DIMM with 4x DIMM sockets
- Optional onboard storage NVMe
- Industrial temperature versions
- Embedded management controller

2.3 COM-HPC® Documentation

The COM-HPC® specification defines the COM-HPC® module form factor, pinout and signals. For more COM-HPC® specification information, visit the PCI Industrial Computer Manufacturers Group (PICMG®) website.

2.4 COM-HPC® Server Functionality

All JUMPtec COM-HPC® Server modules are populated two 400-pin connectors, each has 4 rows called A to D on connector J1 and row E to H on connector J2. The COM-HPC® Server Computer-on-Module features the following maximum amount of interfaces according to the PICMG module pinout type.

Interface	**Server min/max**	**COMh-sdID (E2)**
PCIe 0:47	8/48	48
PCIe 48:63	0/16	0
PCIe BMC	1/1	1
NBASE-T	1	1 (1/2.5GBASE-T)
ETH_KR	2/8	8 (various configurations)
USB 2.0	4/8	4
USB 3.2 Gen1 or Gen2	0/2	2 (USB 3.2 Gen1)
USB 3.2 Gen2x2	0/2	2 (USB 3.2 Gen1)
USB 4.0 Support	0/2	0
SATA	0/2	2
UART	1/2	2
eSPI	0/1	1
BOOT_SPI	1/1	1
GP_SPI	1/1	1
SMB	1/1	1
I^2C	2/2	2
IPMB	0/1	1
GPIO	12/12	12/12

Table 2: COM-HPC® Server and COMh-sdID functionality

2.5 COM-HPC® Benefits

COM-HPC® defines a Computer-On-Module (COM), with all the components necessary for a bootable host computer, packaged as a highly integrated computer. All JUMPtec COM-HPC® modules are very compact and feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each COM module is based on the COM-HPC® specification. This standardization allows designers to create a single-system carrier board that can accept present and future COM-HPC® modules. The carrier board designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application, on a carrier board optimally designed to fit a system’s packaging. A single carrier board design can use a range of COM-HPC® modules with different sizes and pinouts. This flexibility differentiates products at various price and performance points and provides a built-in upgrade path when designing future-proof systems. The modularity of a COM-HPC® solution also ensures against obsolescence when computer technology evolves. A properly designed COM-HPC® carrier board can work with several successive generations of COM-HPC® modules. A COM-HPC® carrier board design has many advantages of a customized computer-board design and, additionally, delivers better obsolescence protection, heavily reduced engineering effort, and faster time to market.

3. Product specification

3.1 Module Variants

3.1.1 Commercial Grade Modules (0°C to +60°C)

Part Number	Product Name	CPU	Use Condition
HSD01-0000-98-2	COMh-sdID D-2798NT	D-2798NT	Industrial, commercial temperature
HSD01-0000-76-2	COMh-sdID D-2776NT	D-2776NT	Industrial, commercial temperature
HSD01-0000-53-2	COMh-sdID D-2753NT	D-2753NT	Industrial, commercial temperature

Table 3: Product Number for Commercial Grade Modules (0°C to +60°C)

3.1.2 Industrial Temperature Grade Modules (E2, -40°C to +85°C)

Part Number	Product Name	CPU	Use Condition
HSD02-0000-96-1	COMh-sdID E2 D-2796TE	D-2796TE	Industrial, extended temperature
HSD02-0000-75-1	COMh-sdID E2 D-2775TE	D-2775TE	Industrial, extended temperature
HSD02-0000-52-1	COMh-sdID E2 D-2752TER	D-2752TER	Industrial, extended temperature

Table 4: Product Number for Industrial Grade Modules (-40°C to +85°C)

3.2 Accessories

Accessories are product specific, COM-HPC® specific or general COM accessories. For more information, contact your local JUMPtec Sales Representative or JUMPtec Inside Sales.

3.2.1 Cooling

Any LGA115x cooler can be used for the COMh-sdID. In this case please use our HSD01-0000-99-A COMh-sdID (E2) Adapter and HSD01-0000-99-B COMh-sdID (E2) Backplate for cooler mounting. Alternatively our standard heat spreader solutions can be used, which are available in a threaded and non-threaded (through hole) version.

JUMPtec PN	Product Name	Description
HSD01-0000-99-0	COMh-sdID (E2) Heat Spreader threaded	Standard COM-HPC Heat Spreader for COMh-sdID with threads
HSD01-0000-99-1	COMh-sdID (E2) Heat Spreader through hole	Standard COM-HPC Heat Spreader for COMh-sdID through hole
HSD99-0000-99-0	COMh Size D Active Uni Cooler (w/o HSP)	Universal Active Cooler for Heatspreader Mounting (160 x 100 x 46 mm)
HSD99-0000-99-1	COMh Size D Passive Uni Cooler (w/o HSP)	Universal Passive Cooler for Heatspreader Mounting (160 x 100 x 46 mm)

JUMPtec PN	Product Name	Description
HSD01-0000-99-A	COMh-sdID (E2) Adapter	Adapter for a standard LGA115x cooling solution
HSD01-0000-99-B	COMh-sdID (E2) Backplate	Backplate for a standard LGA115x cooling solution
HSD01-0000-99-C	COMh-sdID (E2) Cooler	Standard LGA115x cooler, needs in addition HSD01-0000-99-A and HSD01-0000-99-B

Table 5: Cooling Equipment for COMh-sdID available from JUMPtec

3.2.2 DIMM Memory

JUMPtec provides following RDIMM memory module:

JUMPtec PN	Product Name	Size	ECC	Op. Temperature
97100-1632-SDID	DDR4-3200 RDIMM 16GB ECC_SDID	16GB	ECC	0°C to +60°C
97100-3232-SDID	DDR4-3200 RDIMM 32GB ECC_SDID	32GB	ECC	0°C to +60°C
97100-6432-SDID	DDR4-3200 RDIMM 64GB ECC_SDID	64GB	ECC	0°C to +60°C
97101-1632-SDID	DDR4-3200 RDIMM 16GB ECC E2_SDID	16GB	ECC	-40°C to +85°C
97101-3232-SDID	DDR4-3200 RDIMM 32GB ECC E2_SDID	32GB	ECC	-40°C to +85°C
97101-6432-SDID	DDR4-3200 RDIMM 64GB ECC E2_SDID	64GB	ECC	-40°C to +85°C

Table 6: RDIMM memory modules for COMh-sdID available from JUMPtec

3.2.3 Evaluation Carrier

JUMPtec PN	Product Name	Description
HST01-0000-10-0	COM-HPC Server Carrier 10mm	COM-HPC Server Carrier with 10mm Connector Height

Table 7: Evaluation Carrier from JUMPtec

3.3 Functional Specification

3.3.1 Technical Data

Function	Definition
Compliance	COM-HPC®/Server, Size D
Dimension (H X W)	160 mm x 160 mm
Processors	Intel Xeon® D-2700/D-2800 Processor Series
Chipset	Integrated in SOC
Main Memory	4x DDR4 DIMM sockets for up to 512 GByte LR/RDIMM
Ethernet Controller	Intel® I226-LM/IT Intel® 2x Quad 25GbE LAN integrated in SoC
Ethernet	1x 1/2.5 Gb Ethernet 8x Ethernet ports supporting versatile configurations depending on CPU SKU: 100GbE / 2x 50GbE / 4x 25GbE / 2x 25GbE + 4x 10GbE / 8x 10GbE

Function	Definition
Storage	2x SATA 6 Gb/s
Flash On-board	NVMe SSD (on request) - up to 1 TByte TLC or 333 GByte pSLC
PCI Express	32x PCIe Gen4 (2 x16, 4 x8, 8 x4) 16x PCIe Gen3 (2 x8, 4 x4, 8 x2)
USB	4x USB 3.0 / USB 2.0
Serial	2x serial interface (RX/TX/CTS/RTS)
Other Features	SPI, SMB, Fast I²C, Staged Watchdog, RTC
Special Features	Trusted Platform Module (TPM) 2.0
Features on Request	NVMe SSD
Power Management	ACPI 6.0
Power Supply	12 V ATX and/or Single Supply Power
BIOS	AMI UEFI
Operating Systems	Linux, Windows 10 IoT Enterprise, Windows Server 2022
Temperature	Commercial temperature: 0 °C to +60 °C operating, -30 °C to +85 °C non-operating Industrial temperature: -40 °C to +80 °C operating, -30 °C to +85 °C non-operating
Humidity	93 % relative Humidity at 40 °C, non-condensing (according to IEC 60068-2-78)

Table 8: Technical Data

3.3.2 Block Diagram

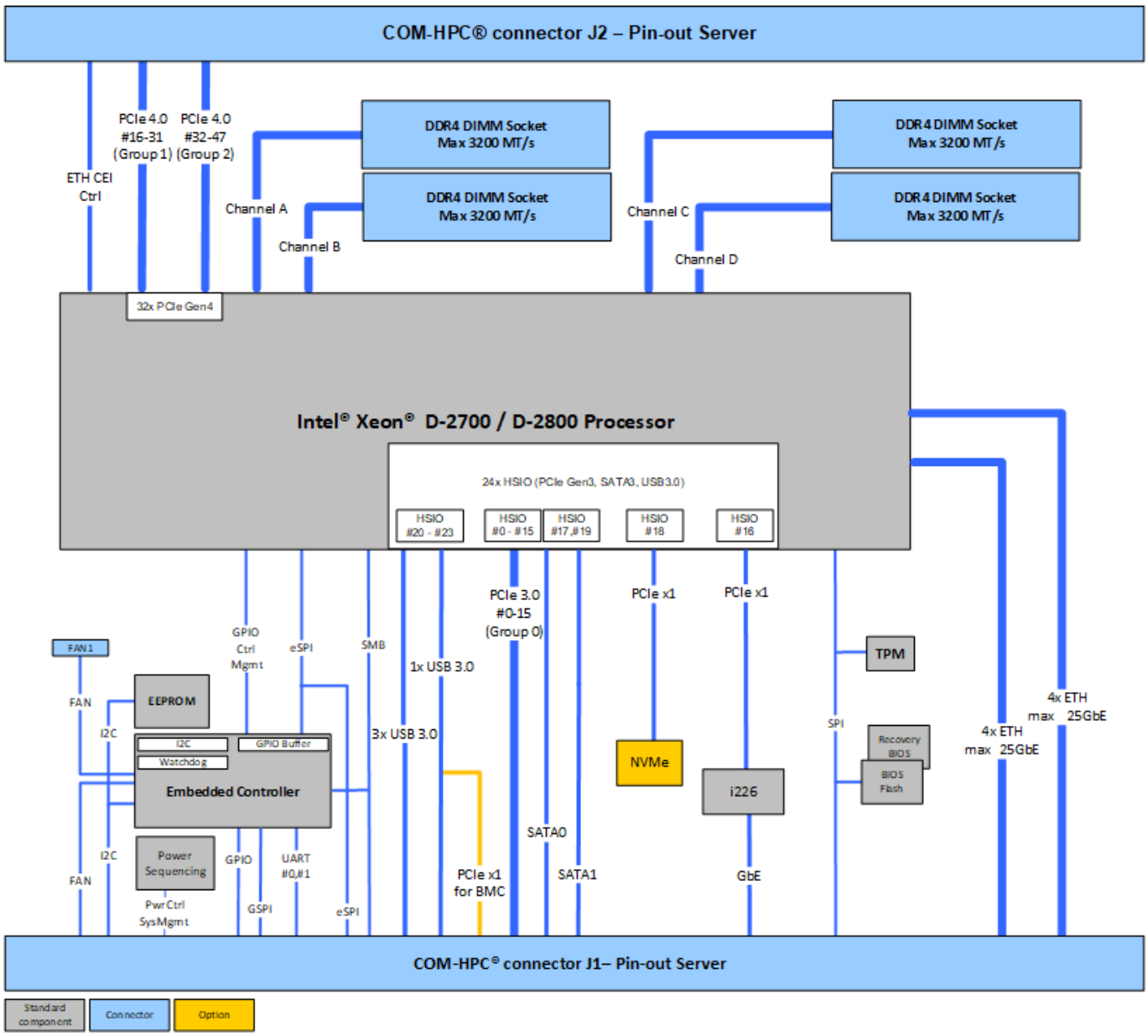

Figure 1: COMh-sdID Block Diagram

3.3.3 Top Side

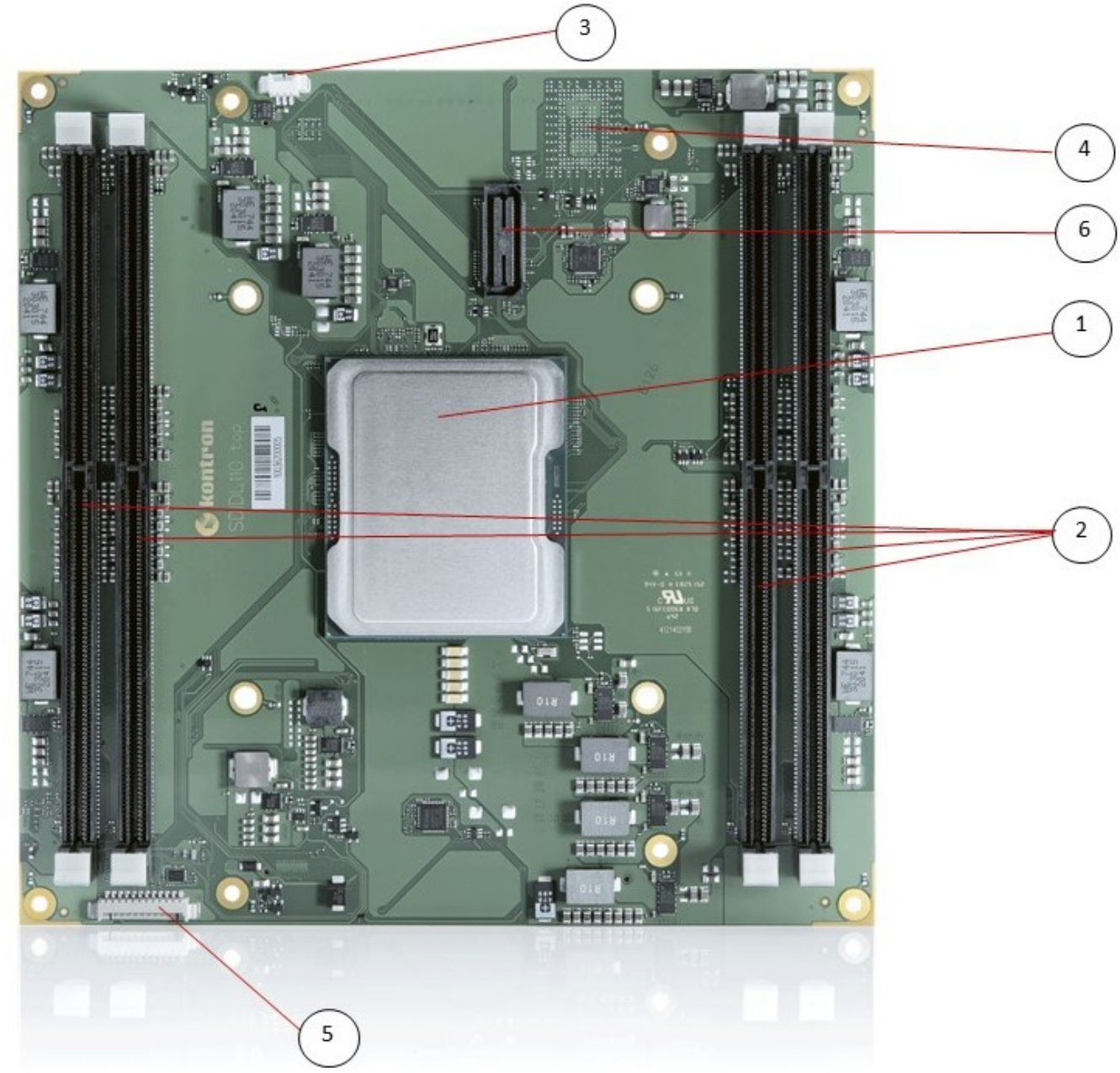

Figure 2: COMh-sdID Front Side

1. Processor
2. 4x DDR4 DIMM sockets
3. Fan Connector
4. Optional NVMe
5. Programming connector for embedded controller
6. XDP debug port (not populated on production units)

3.3.4 Bottom Side

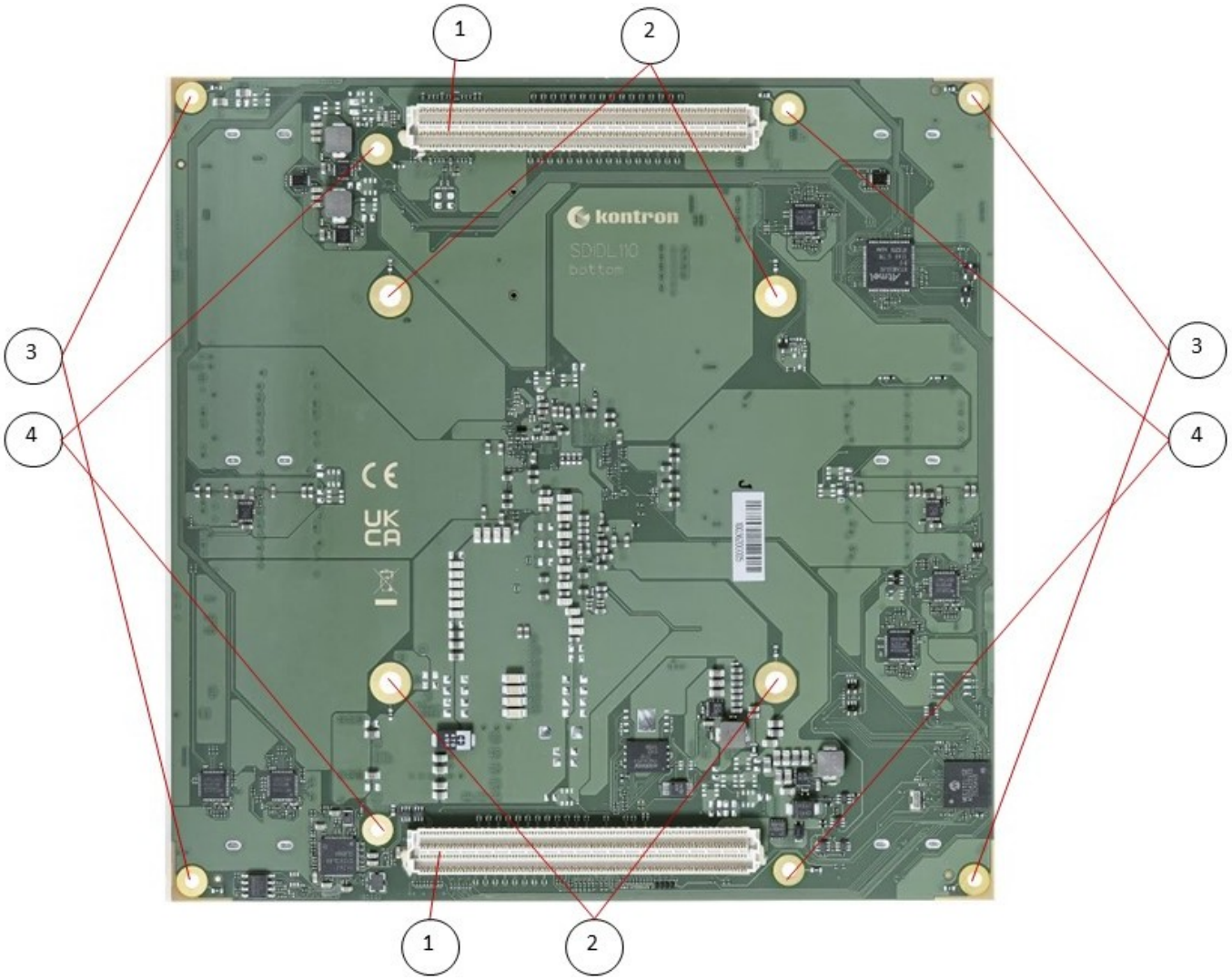

Figure 3: COMh-sdID Bottom Side

1. COM-HPC connectors
2. 4 mounting holes - for heatspreader mounting to module backplate (JUMPtec specific)
3. 4 mounting holes - for module mounting to carrier
4. 4 mounting holes - for heatspreader to module, module to carrier mounting

3.3.5 Processor (CPU)

The COMh-sdID is based on the Intel® Xeon® D-2700/D-2800 processor family, the next generation System-on-Chip (SoC) with processor cores built using Intel 10-nanometer process technology. The three major complexes in this highly-integrated SoC are referred to as CPU, PCH and NAC.
The Central Processing Unit (CPU) complex contains up to 20 next-generation 64-bit processor cores (code name Ice Lake Server).
The Platform Controller Hub (PCH) of the SoC is architected with a rich set of interconnect technologies.
The Network Accelerator Complex (NAC) includes technologies for security and packet processing.
The SoC architecture is highly scalable and efficient, providing a unified solution across an array of products. Product SKUs are targeted for long life supply availability with extended reliability in industrial environments.

Topline Specifications are:

- Up to 20 processor cores based on architecture code name Ice Lake server:
- Each core has L1 (first-level) data and instruction caches:
  - 48 KB data, 64-byte cache line size parity protected
  - 32 KB instruction, 64-byte cache line size parity protected
- Mid-Level Cache (MLC) unified instruction/data cache, ECC protected:
  - 1.25 MB of MLC per core (non-inclusive with the LLC)
- Last-Level Cache (LLC) unified instruction/data cache, DECTED ECC protected:
  - 2.5 MB of LLC per CHA tile shared by all cores

- Four memory channels up to 3200 MT/s:
  - 72-bit wide (64-bit data + 8-bit ECC) operating up to 3200 MT/s memory
  - Single-rank or dual-rank per DIMM module
  - ECC and non-ECC support

- 32 PCI Express lanes, 16 GT/s data rate:
  - Maximum Root Port width is 16-lanes with support for x8, x4

- 24 HSIO lanes, 8.0 GT/s data rate:
  - High-Speed IO lanes with multi-purpose configuration capabilities as PCIe, SATA, USB
  - Maximum Root Port width is 8-lanes with support for x4, x2

- Network Accelerator Complex (NAC) with high performance, programmable, packetprocessing acceleration technology, including:
  - Network Interface and Scheduler
  - Intel® QuickAssist Technology (Intel® QAT v1.8) that performs security and compression acceleration

CPU	STD /on request	Cores	TDP (W)	IOTG	Temp min (°C)	DTS max (°C)	DDR4 1DPC (M/T)	Ethernet mode	QAT	BaseFreq (MHz)	All Core Turbo (MHz)
D-2796TE	STD	20	118	Yes	-40	102	2933	100G	No	2.0	2.5
D-2896TER	on request	20	110	Yes	-40	102	2933	100G	No	2.0	2.4
D-2775TE	STD	16	100	Yes	-40	100	2933	100G	No	2.0	2.4
D-2752TER	STD	12	77	Yes	-40	100	2667	50G	No	1.8	2.1
D-2733NT	on request	8	80	Yes	0	100	2667	50G	Yes	2.1	2.6
D-2712T	on request	4	65	Yes	0	100	2667	50G	No	1.9	2.4
D-2786NTE	on request	18	118	No	-40	100	2933	100G	Yes	2.1	2.5
D-2899NT	on request	22	135	No	0	100	2933	100G	Yes	2.1	2.6
D-2798NX	on request	20	126	No	0	100	2667	100G	Yes	2.2	2.7
D-2796NT	STD	20	120	No	0	102	2667	50G	Yes	2.5	3.0
D-2798NT	on request	20	125	No	0	100	2667	50G	Yes	2.4	2.9
D-2896NT	on request	20	120	No	0	99	3200	100G	Yes	2.2	2.8
D-2777NX	on request	16	116	No	0	100	2933	100G	Yes	2.0	2.6
D-2776NT	on request	16	117	No	0	100	2933	100G	Yes	2.0	2.5
D-2876NT	on request	16	100	No	0	100	3200	100G	Yes	2.1	2.6
D-2766NT	on request	14	97	No	0	100	2933	100G	Yes	2.0	2.5
D-2753NT	on request	12	87	No	0	99	2933	100G	Yes	2.1	2.6
D-2752NTE	on request	12	84	No	-40	100	2667	100G	Yes	2.0	2.5

CPU	STD /on request	Cores	TDP (W)	IOTG	Temp min (°C)	DTS max (°C)	DDR4 1DPC (M/T)	Ethernet mode	QAT	BaseFreq (MHz)	All Core Turbo (MHz)
D-2757NX	on request	12	107	No	0	100	2667	100G	Yes	2.0	2.5
D-2745NX	on request	10	96	No	0	100	2667	50G	Yes	1.9	2.3
D-2843NT	on request	10	80	No	0	99	2667	50G	Yes	2.0	2.6
D-2832NT	on request	8	70	No	0	100	2667	50G	Yes	2.1	2.6
D-2799	on request	20	129	No	0	100	3200	No	No	2.4	2.6
D-2779	on request	16	126	No	0	100	3200	No	No	2.5	2.8
D-2738	on request	8	88	No	0	100	2933	No	No	2.5	3.0

Table 9: CPU Feature Overview

Intel® DTR (Dynamic Temperature Range)

For this processor family the Dynamic Temperature Range (DTR) behavior applies. DTR is the temperature range the processor can operate in. The temperature range starts with the temperature of the processor (Tj = junction temperature) at boot time and can transition to a lower and/or higher temperature within the Tj min and Tj max limits.

E.g.: Tj min = -40°, the Tj max = 100°C and the DTR = +-90°C
TBoot = -40°C: the processor can operate from -40°C up to + 50°C
TBoot = -20°C: the processor can operate from -40°C up to + 70°C
TBoot = +20°C: the processor can operate from -40°C up to + 100°C

A Tj outside of the DTR range requires a cold reset but is not enforced by the hardware.

The behavior is described in Intel whitepaper 814861 as DTR = Dynamic Temperature Range. Please contact JUMPtec Support for further information.

CPU Use Condition	Commercial Temp: Embedded Broad Market/Industrial	Extended Temp: Embedded Broad Market/Industrial
CPU Tj Min.	0°C	-40°C
CPU Tj Max.	100°C	100°C
DTR (Cold to Hot Transition)	TBoot + 90°C	TBoot + 90°C
DTR (Hot to Cold Transition)	TBoot - 90°C	TBoot - 90°C

Table 10: DTR values and limits

By default the DTR-range is +-90°C. Within Tjunction limits the max. temperature range during operation can be increased to +-110°C by reducing interface speeds, such as e.g. PCIe Gen4 to PCIe Gen3.

For more details please see Intel document #631107 and/or contact JUMPtec Support

3.3.6 System Memory

The COMh-sdID offers 4x DIMM sockets supporting up to 64 GByte of RDIMM ECC memory per socket.

Socket	288-pin
Memory Type	Registered ECC DIMM 1.2V
Memory Speed	3200 MTs (max)
Channels	Four channels
Max Memory	Up to 256GByte (4x 64GByte)

Table 11: System Memory

3.3.7 High-Speed Interface Overview

The integrated SoC PCH supports 24x HSIO lanes #0-23 (HSIO) which can be configured as PCIe Gen 3.0 lanes with up to 3 RPC (Root Port Controller), 4 RP (Root Port) per RPC (12 RPs max). The HSIO PCIe lanes are partly multiplexed with USB3.0 and SATA.

The HSIO lanes #0 - #15 are used as PCIe Gen 3.0 lanes to support COM-HPC J1 Group 0 PCIe #0 -15.
The HSIO lane #16 is used as PCIe Gen 3.0 lane for the onboard 1 /2.5 GbE Controller Intel i226.
The HSIO lane #17 and #19 are defined as SATA.
The HSIO lane #18 is used as PCIe Gen 3.0 lane for an optional onboard NVMe SSD.
The HSIO lanes #20, #21 and #23 are defined as USB3.0.
The HSIO lane #22 is defined as USB 3.0 for USB #3 - as a BOM option the HSIO lane #22 can be defined as 1x PCIe Gen 3.0 lane for a BMC controller on the carrier board.

HSIO Lane#	PCIe Gen 3.0	USB 3.0	SATA	Description
0	PCIe 0	-	-	COM-HPC Connector - Group 0 low - PCIe Gen 3
1	PCIe 1	-	-	
2	PCIe 2	-	-	
3	PCIe 3	-	-	
4	PCIe 4	-	-	
5	PCIe 5	-	-	
6	PCIe 6	-	-	
7	PCIe 7	-	-	COM-HPC Connector - Group 0 high - PCIe Gen 3
8	PCIe 8	-	-	
9	PCIe 9	-	-	
10	PCIe 10	-	-	
11	PCIe 11	-	-	
12	PCIe 12	-	-	
13	PCIe 13	-	-	
14	PCIe 14	-	-	
15	PCIe 15	-	-	

HSIO Lane#	PCIe Gen 3.0	USB 3.0	SATA	Description
16	PCIe	-	-	For onboard GbE controller routed to COM-HPC Connector - NBASE-T
17	-	-	SATA 0	COM-HPC Connector - SATA #0
18	PCIe	-	-	Option: For onboard NVMe
19	-	-	SATA 1	COM-HPC Connector - SATA #1
20	-	USB 0	-	COM-HPC Connector - USB #0
21	-	USB 1	-	COM-HPC Connector - USB #1
22	PCIe (option)	USB 3 (default)	-	COM-HPC Connector - USB #3 Option: COM-HPC Connector PCIe x1 lane for BMC
23	-	USB 2	-	COM-HPC Connector - USB #2

Table 12: HSIO Mapping

3.4 Interfaces

3.4.1 PCIe

COM-HPC allows for up 65 PCIe lanes on the Server Module. The PCIe lanes are divided into 5 Groups:

- Group 0 Low: PCIe lanes 0:7 and also an additional lane for BMC use
- Group 0 High: PCIe lanes 8:15
- Group 1: PCIe lanes 16:31
- Group 2: PCIe lanes 32:47
- Group 3: PCIe lanes 48:63

The integrated SoC PCH supports 24x HSIO lanes #0-23 (HSIO) which can be configured as PCIe Gen 3.0 lanes with up to 3 RPC (Root Port Controller), 4 RP (Root Port) per RPC (12 RPs max). The HSIO PCIe lanes are partly multiplexed with USB3.0 and SATA.
Further information see chapter 3.3.7 High-Speed Interface Overview

COMh Group	COMh Lane	PCH/HSIO PCIe Lane	Lane Config			PCIe Gen
0 LOW	0	HSIO PCIE 0	x2	x4	x8	3
	1	HSIO PCIE 1				
	2	HSIO PCIE 2	x2			
	3	HSIO PCIE 3				
	4	HSIO PCIE 4	x2	x4		
	5	HSIO PCIE 5				
	6	HSIO PCIE 6	x2			
	7	HSIO PCIE 7				
0 HIGH	8	HSIO PCIE 8	x2	x4	x8	
	9	HSIO PCIE 9				
	10	HSIO PCIE 10	x2			
	11	HSIO PCIE 11				
	12	HSIO PCIE 12	x2	x4		
	13	HSIO PCIE 13				
	14	HSIO PCIE 14	x2			
	15	HSIO PCIE 15				

Table 13: PCH HSIO usage

In addition the SoC CPU provides 32x PCIe Gen 4.0 lanes.

COMh Group	COMh Lane	CPU PCIe Lane	Lane Config			PCIe Gen
1	16	CPU PCIE 0	x4	x8	x16	4
	17	CPU PCIE 1				
	18	CPU PCIE 2				
	19	CPU PCIE 3				
	20	CPU PCIE 4	x4			
	21	CPU PCIE 5				
	22	CPU PCIE 6				
	23	CPU PCIE 7				
	24	CPU PCIE 8	x4	x8		
	25	CPU PCIE 9				
	26	CPU PCIE 10				
	27	CPU PCIE 11				
	28	CPU PCIE 12	x4			
	29	CPU PCIE 13				
	30	CPU PCIE 14				
	31	CPU PCIE 15				
2	32	CPU PCIE 16	x4	x8	x16	4
	33	CPU PCIE 17				
	34	CPU PCIE 18				
	35	CPU PCIE 19				
	36	CPU PCIE 20	x4			
	37	CPU PCIE 21				
	38	CPU PCIE 22				
	39	CPU PCIE 23				
	40	CPU PCIE 24	x4	x8		
	41	CPU PCIE 25				
	42	CPU PCIE 26				
	43	CPU PCIE 27				
	44	CPU PCIE 28	x4			
	45	CPU PCIE 29				
	46	CPU PCIE 30				
	47	CPU PCIE 31				

Table 14: CPU PCI Express lanes

The COMh-sdID supports 4x USB 3.0 ports.

COM-HPC connector	HSIO Lane#	USB Speed	Comment
USB0	20	USB 3.0	USB 3.2 Gen 1×1
USB1	21	USB 3.0	USB 3.2 Gen 1×1
USB2	23	USB 3.0	USB 3.2 Gen 1×1
USB3	22	USB 3.0	USB 3.2 Gen 1×1 option: configured as PCIe x1 for an BMC controller on the carrier board

Table 15: USB 3.0 support and HSIO

See also chapter 3.3.7 High-Speed Interface Overview.

3.4.3 SATA

Two SATA links for support of SATA-150 (revision 1.0, 1.5Gb/s), SATA-300 (revision 2.0, 3Gb/s), and SATA-600 (revision 3.0, 6Gb/s) devices are defined, for the Client Module and the Server Module.

The COMh-sdID supports following SATA interfaces:

COM-HPC Connector	HSIO Lane #	Description
SATA0	17	SATA Gen 3, 6 Gb/s
SATA1	19	SATA Gen 3, 6 Gb/s

Table 16: SATA Port Connections

See also chapter 3.3.7 High-Speed Interface Overview.

The COMh-sdID supports one 1/2.5GBASE-T port and and up to eight KR interfaces.
HSIO lane #16 of the integrated SOC PCH is used as PCIe Gen 3.0 lane for the onboard 1/2.5 GbE Controller Intel i226 (see chapter 3.3.7 High-Speed Interface Overview).

The Intel® Xeon® D-2700/D-2800 processor family supports up to two integrated PHY Quads with 1G/2.5G/10G/25G/40G/50G/100G rates (depending on the processor SKU).

D-2700 SKU	Ethernet MAC	Quad 0				Quad 1			
		Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
100G	2x 100G	100G				100G (limited total BW 100G)			
	2x 50G	50G				50G			
	2x 40G	40G				40G			
	2x 25G + 4x 10G	25G	25G			10G	10G	10G	10G
	4x 25G	25G	25G	25G	25G				
	8x 10G	10G	10G	10G	10G	10G	10G	10G	10G
50G	1x 50G	50G							
	1x 40G	40G							
	2x 25G	25G		25G					
	4x 10G	10G	10G	10G	10G				
	1x 25G + 2x 10G	25G	10G	10G					
	5x 10G	10G	10G	10G	10G	10G			
	4x 10G + 4x 2.5G	10G	10G	10G	10G	2.5G	2.5G	2.5G	2.5G

Figure 4: D-2700/D-2800 Ethernet MAC configurations

COM-HPC supports both MDIO and I2C control interfaces for the PHYs to be located on the carrier. The MDIO and I2C control interfaces are grouped into quads, for KR ports 0:3 and ports 4:7. With COM-HPC the so-called CEI (Common Electrical Interface) from Intel is introduced for the Ethernet interface. One CEI interface comprises the Ethernet KR signals as well as the sideband and control signals for one quad. Two CEI interfaces are supported for two quads.
With CEI the Ethernet sideband and control signals are serialized in order to reduce the overall required signals between the module and the carrier.
The carrier is to de-serialize these signals using small, low cost I2C based I/O expanders. Details are presented in the *COM-HPC Carrier Board Design Guide*.

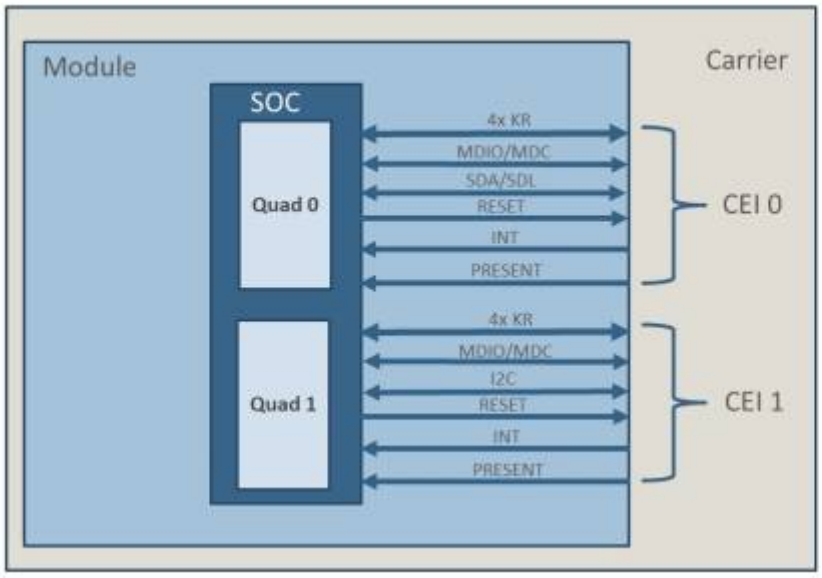

Figure 5: CEI interface

COM-HPC Signal Name	Pin Type	Intel CEI Mapping	Description
ETH[0:3]_TX+/TX-	O	CEI0_PMD_L[0:3]	Ethernet KR ports, transmit output differential pairs.
ETH[0:3]_RX+/RX-	I	CEI0_PMD_L[0:3]	Ethernet KR ports, receive input differential pairs.
ETH[4:7]_TX+/TX-	O	CEI1_PMD_L[0:3]	Ethernet KR ports, transmit output differential pairs.
ETH[4:7]_RX+/RX-	I	CEI1_PMD_L[0:3]	Ethernet KR ports, receive input differential pairs.
ETH0-3_MDIO_DAT	I/O	CEI0_MDIO	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 3 .
ETH0-3_MDIO_CLK	O	CEI0_MDC	Clock signal for Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 3.
ETH4-7_MDIO_DAT	I/O	CEI1_MDIO	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 4 to 7.
ETH4-7_MDIO_CLK	O	CEI1_MDC	Clock signal for Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 4 to 7.
ETH0-3_INT#	I	CEI0_INT#	Active low interrupt signal from IO Port expanders for ETH ports 0 to 3.
ETH4-7_INT#	I	CEI1_INT#	Active low interrupt signal from IO Port expanders for ETH ports 4 to 7.
ETH0-3_PHY_RST#	O	CEI0_RESET#	Active low output PHY reset signal for ETH ports 0 to 3.
ETH4-7_PHY_RST#	O	CEI1_RESET#	Active low output PHY reset signal for ETH ports 4 to 7.
ETH0-3_I2C_DAT	I/O	CEI0_SDA	I2C data signal of the 2-wire management interface used by the Ethernet KR controller to access the management registers of an external SFP Module or to configure the Carrier PHY for ETHx ports 0 to 3 and for serialized status information (e.g. LED states).
ETH0-3_I2C_CLK	I/O	CEI0_SCL	The I2C clock signals associated with ETH0-3 I2C data lines in the row above.
ETH4-7_I2C_DAT	I/O	CEI1_SDA	I2C data signal of the 2-wire management interface used by the Ethernet KR controller to access the management registers of an external SFP Module or to configure the Carrier PHY for ETHx ports 4 to 7 and for serialized status information (e.g. LED states).
ETH4-7_I2C_CLK	I/O	CEI1_SCL	The I2C clock signals associated with ETH4-7 I2C data lines in the row above.

COM-HPC Signal Name	Pin Type	Intel CEI Mapping	Description
ETH0-3_PRSNT#	I	CEI0_PRESENT#	Carrier pulls this line to GND if there is Carrier hardware present to support Ethernet KR signaling on ETH0 through ETH3. If the entire KR quad is not supported it should fill from ETH0 on up.
ETH4-7_PRSNT#	I	CEI1_PRESENT#	Carrier pulls this line to GND if there is Carrier hardware present to support Ethernet KR signaling on ETH4 through ETH7. If the entire KR quad is not supported it should fill from ETH4 on up.

Table 17: Mapping of COM-HPC Server specification to CEI interface

In general the COMh-sdID can support the LAN configurations - enabled by different LEK (LAN Enabling Kit) files - which are aligned with the CEI interface. These are overall described in the following table.

Hardware Configuration					Quad 0				Quad 1			
Cfg ID	# Ports	Quad 0 HW	Quad 1 HW	D-2700	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
7,0	2	CEI	Disabled	50G	25G		25G					
	2	CEI	CEI	100G	100G				100G			
	4	CEI	Disabled	50G	10G	10G	10G	10G				
	4	CEI	Disabled	100G	25G	25G	25G	25G				
	8	CEI	CEI	50G	10G	10G	10G	10G	1G	1G	1G	1G
	8	CEI	CEI	100G	10G	10G	10G	10G	10G	10G	10G	10G
7,1	8	CEI	Backplane	50G	10G	10G	10G	10G	2.5G	2.5G	2.5G	2.5G
	8	CEI	Backplane	100G	10G	10G	10G	10G	10G	10G	10G	10G
7,2	8	CEI	4xSFP (w/Exp)	50G	10G	10G	10G	10G	1G	1G	1G	1G
	8	CEI	4xSFP (w/Exp)	100G	10G	10G	10G	10G	10G	10G	10G	10G
7,5	4	4xSFP (w/Exp)	Disabled	100G	10G	10G	10G	10G				
	8	4xSFP (w/Exp)	CEI	100G	10G	10G	10G	10G	10G	10G	10G	10G
7,6	1	Backplane	Disabled	50G	50G							
	1	Backplane	Disabled	100G	100G							
	2	Backplane	Disabled	50G	25G		25G					
	2	Backplane	Backplane	100G	100G				100G			
	4	Backplane	Disabled	50G	10G	10G	10G	10G				
	4	Backplane	Disabled	100G	25G	25G	25G	25G				
	5	Backplane	Backplane	50G	10G	10G	10G	10G	10G			
	6	Backplane	Backplane	100G	25G	25G			10G	10G	10G	10G
	8	Backplane	Backplane	50G	10G	10G	10G	10G	2.5G	2.5G	2.5G	2.5G
	8	Backplane	Backplane	100G	10G	10G	10G	10G	10G	10G	10G	10G
7,7	2	2xSFP (w/Exp)	Disabled	50G	25G		25G					
	4	4xSFP (w/Exp)	Disabled	50G	10G	10G	10G	10G				
	4	4xSFP (w/Exp)	Disabled	100G	25G	25G	25G	25G				
	5	4xSFP (w/Exp)	4xSFP (w/Exp)	50G	10G	10G	10G	10G	10G			
	6	4xSFP (w/Exp)	4xSFP (w/Exp)	100G	25G	25G			10G	10G	10G	10G
	8	4xSFP (w/Exp)	4xSFP (w/Exp)	50G	10G	10G	10G	10G	1G	1G	1G	1G
	8	4xSFP (w/Exp)	4xSFP (w/Exp)	100G	10G	10G	10G	10G	10G	10G	10G	10G
7,9	2	Backplane	4xSFP (w/Exp)	100G	50G				10G			
	6	Backplane	4xSFP (w/Exp)	100G	25G	25G			10G	10G	10G	10G
	8	Backplane	4xSFP (w/Exp)	50G	10G	10G	10G	10G	1G	1G	1G	1G
	8	Backplane	4xSFP (w/Exp)	100G	10G	10G	10G	10G	10G	10G	10G	10G

Figure 6: Supported LAN configs

The COMh-sdID is preconfigured with CFG 7.0 supporting 4 ports.

Please get familiar with Intel documents #631178 and #645149

3.4.5 Graphics Interfaces

A COM-HPC Server module doesn't support graphic interfaces.

3.4.6 Audio Interfaces

A COM-HPC Server module doesn't support audio interfaces.

3.4.7 UART

Two 3.3V logic level asynchronous serial ports, designated UART0 and UART1 are defined by COM-HPC. Each port has TX and RX signals for data use and RTS# and CTS# signals for optional handshake / flow control use. For logic level use, the TX and RX signals are active high and the RTS# and CTS# signals are active low. Some data sheets omit the trailing '#' signal but the logic level handshake signals are active low nonetheless. The idle state, or 'mark' state, of the logic level TX line is high, or 3.3V in the COM-HPC case.
These ports may be used directly as logic level asynchronous serial connections between COM-HPC Module and Carrier based devices, or between COM-HPC Module and Carrier based mezzanine devices such as certain Mini-PCIe or M.2 cards. Care has to be taken that the logic I/O levels match up.

The UART interfaces on the COMh-sdID is supported by default via the EC (embedded controller). It can be reconnected to the SOC's PCH's UARTs on request.

COM-HPC	EC (Default)	SOC PCH(Optional)
UART0_TX	UART0_TX	option on request
UART0_RX	UART0_RX	
UART0_RTS#	UART0_RTS#	
UART0_CTS#	UART0_CTS#	
UART1_TX	UART1_TX	option on request
UART1_RX	UART1_RX	
UART1_RTS#	UART1_RTS#	
UART1_CTS#	UART1_CTS#	

Table 18: UART interfaces on COMh-sdID

3.4.8 General Purpose SPI interface

COM-HPC Client and Server modules can support a General Purpose SPI interface (GP_SPI) to connect multiple peripherals.

The COM-HPC GP_SPI interface on the COMh-sdID is handled by the EC (embedded controller).

EC	COM-HPC
EC_GP_SPI_CLK	GP_SPI_CLK
EC_GP_SPI_MOSI	GP_SPI_MOSI
EC_GP_SPI_MISO	GP_SPI_MISO
EC_GP_SPI_CS0#	GP_SPI_CS0#
EC_GP_SPI_CS1#	GP_SPI_CS1#
EC_GP_SPI_CS2#	GP_SPI_CS2#
EC_GP_SPI_CS3#	GP_SPI_CS3#
EC_GP_SPI_ALERT#	GP_SPI_ALERT#

Table 19: GP-SPI on COMh-sdID

3.4.9 Boot SPI

The Boot SPI interface is used to support loading all or parts of the system BIOS from a Module or Carrier based SPI (Serial Peripheral Interface) or SQI (Serial Quad Interface) flash device. The SPI or SQI flash device can be up to 64 MB (512 Mb). Two flash devices may be used on the Module, allowing up to 128 MB of boot code storage on the Module. Alternatively there may be a flash device on the Carrier and / or on the Module, for a combined total of up to 128 MB. In most situations, only one flash device, either on the Module or on the Carrier, is used.

An external BIOS ROM can be placed on the carrier and connected via QSPI. Boot source is selected by pulling BSEL [2:0] pins low on the COM-HPC carrier (pull-up on module). BSEL is decoded by the EC (embedded controller) which controls a multiplexer IC via SPI_CS_SEL[1:0] to assign the chip selects from the PCH to their designation.

Usage	BSEL Coding			EC Control Outputs		PCH CS Assignment	
	BSEL 2	BSEL 1	BSEL 0	SPI_CS_SEL1	SPI_CS_SEL0	SPI_CS1#	SPI_CS0#
Internal Boot	1	1	1	1	0	Carrier	Module
External Boot	1	1	0	0	1	Module	Carrier
Do not use	1	0	1	1	0	Carrier	Module
Do not use	1	0	0	1	0	Carrier	Module
Do not use	0	1	1	1	0	Carrier	Module
Do not use	0	1	0	1	0	Carrier	Module
Do not use	0	0	1	1	0	Carrier	Module
Do not use	0	0	0	1	0	Carrier	Module

Table 20: BIOS Boot options on the COMh-sdID

3.4.10 eSPI

COM-HPC supports an eSPI port for general purpose I/O. The eSPI interface (like LPC before it) can be useful for general purpose devices such as Carrier Super I/O devices, Carrier CPLDs or FPGAs, hardware monitoring devices, and others. It is also possible to boot the BIOS over eSPI. The eSPI bus

runs from a 1.8V supply.
COM-HPC does not support LPC.

The COMh-sdID supports following eSPI interface:

SOC (Master)	EC (Slave 0)	COM-HPC Connector (Slave 1)
ESPI_CLK	ESPI_CLK	ESPI_CLK
ESPI_RESET#	ESPI_RESET#	ESPI_RST#
ESPI_IO_[0:3]	ESPI_IO[0:3]	ESPI_IO[0:3]
ESPI_CS0#	ESPI_CS#	-
ESPI_CS1#	-	ESPI_CS0#
ESPI_ALERT0#	ESPI_ALERT#	-
ESPI_ALERT1#	-	ESPI_ALERT0#

ESPI_CS1# and ESPI_ALERT1# on the COM-HPC connector are just terminated but not connected to other platform devices.

3.4.11 I2C

Two general purpose I2C ports are defined for COM-HPC.

On the COMh-sdID several I2C interfaces are managed by the EC (embedded controller).

COM-HPC	EC	Description
I2C0_CLK	I2C02_SCL	General I2C with 3.3V Power Rail
I2C0_DAT	I2C02_SDA	
I2C1_CLK	I2C03_SCL	General I2C with 1.8V Power Rail
I2C1_DAT	I2C03_SDA	
IPMB_CLK	I2C06_SCL	IPMB (Intelligent Platform Management Bus)
IPMB_DAT	I2C06_SDA	

Table 22: I2C interfaces on COMh-sdID

3.4.12 GPIO

The COMh-sdID offers 12 GPIO pins on the dedicated pins of COM-HPC®. The type of termination resistor used sets the direction of the GPIO; where GPI terminations are pull-up resistors, and GPO terminations are pull-down resistors.
Due to the fact that both the pull-up and pull-down termination resistors are weak (e.g. 100k), it is possible to override the termination resistors using external pull-ups, pull-downs or IOs. Overriding the termination resistors means that the 12 GPIO pins can be considered as bi-directional since there are no restrictions whether you use the available GPIO pins in the in-direction or out-direction.

3.4.13 SMB

The System Management Bus (SMB) is a simple 2-wire bus for low-speed system management communication. The PCH or the SOC controls the SMB. The module’s SMB connects typically to the memory and the hardware controller.

The SMBus address uses the LSB (Bit 0) for the direction of the device.
Bit0 = 0 defines the write address
Bit0 = 1 defines the read address
The following table specifies the SMBus write address for onboard devices.

8-bit Address	7-bit Address	Device
0xE6	0x73	Onboard embedded controller

Table 23: Reserved onboard SMBus addresses

Don't use this addresses for external devices under any circumstances.

3.5 Features

3.5.1 ACPI Power States

ACPI enables the system to power down, save power when not required (suspend) and wake up when required (resume).
ACPI controls the power states S0-S5, where S0 has the highest priority and S5 the lowest priority.

S0	Working state
S1	Sleep (typically not supported anymore)
S2	Deep Sleep (typically not supported anymore)
S3	Suspend-to-RAM
S4	Suspend-to-disk / Hibernate
S5	Soft-off state

Table 24: ACPI Power States Function

Not all ACPI defined power states are available.
The COMh-sdID supports ACPI 6.0 and the power states S0, S5 only.

To power on from state S5 use

- Power Button

3.5.2 Embedded Controller - Hardware Monitor

The embedded controller (EC) provides a broad set of functionality:
- monitoring the module’s processor temperature, power supply voltages (VCC /5 VSB), battery voltage V_BAT
- monitoring and configuring the on-board and external fans
- acting as hub or super-IO for low speed interfaces such as UART, I2C/SMB, GSPI, GPIO
- supporting watchdog functions

The EC is accessible through the API in the Board Support Package.

3.5.3 Trusted Platform Module (TPM)

The COMh-sdID supports a TPM chip which is directly connected to a dedicated SPI interface from the SOC-PCH.

3.5.4 Watchdog

The watchdog timer interupt (WD_OUT) is a hardware or software timer implemented by the module to the carrier board if there is a fault condition in the main program; the watchdog triggers a system reset or other corrective actions after a specific time, with the aim to bring the system back from a non-responsive to normal state.

The COMh-sdID supports an independently programmable watchdog that works with two stages that can be used stage by stage.

No action	Stage is off and will be skipped
Reset	Restarts the module and starts a new POST and operating system
Delay → No action	Might be necessary when an operating system must be started and the time for the first trigger pulse must be extended. Only available in the first stage!
WD_OUT only	Triggers WD_OUT pin on the carrier board connector only
Reset + WD_OUT	
Delay + WD_OUT → No action	

Table 25: Dual Staged Watchdog Timer - Time-Out Events

Watchdog Time-out

The COMh-sdID has 2 signals interfering with the watchdog.
WD_STROBE# is an input to trigger the watchdog timer. Periodic strobing prevents the watchdog, if enabled, from timing out.
WD_OUT is an output indicating that a watchdog time-out event has occurred, when the setting activates this signal.

COM-HPC	EC	Description
WD_OUT	GPIO036	Passed through Embedded Controller. Output indicating that a watchdog time-out event has occurred.
WD_STROBE#	GPIO035	Passed through Embedded Controller. Strobe input to watchdog timer.

Table 26: Watchdog signal on COM-HPC connector

3.5.5 Real-Time Clock (RTC)

The RTC keeps track of the current time accurately. The RTC's low power consumption enables the RTC to continue operation and keep time using a lower secondary source of power while the primary source of power is switched off or unavailable.
The COMh-sdID supports typical RTC values of 3 V and less than 10 µA. When powered by the main power supply on-module regulators generate the RTC voltage, to reduce RTC current draw. The RTC's battery voltage range is 2.8 V to 3.47 V.

It is not recommended to run a system without a RTC battery on the carrier board. Even if the RTC battery is not required to keep the actual time and date when main power is

off, a missing RTC battery will cause other side effects such as longer boot times. Intel processor environments are generally designed to rely on RTC battery voltage.

3.5.6 NVME

On some COM-HPC modules a PCIe NVMe NAND Flash SSD (with a capacity up to 1TB) can be populated optionally.

As BOM option an NVMe SDD (BGA) can be populated on the COMh-sdID.
The optional NVMe SSD uses HSIO #18 of the SoC - see also chapter 3.3.7 High-Speed Interface Overview.

The NVMe is based on TLC technology and can be configured as pSLC as well. Configuring the TLC-NVMe as pSLC results in dividing the capacity by three.

3.5.7 Boot EEPROM

The SPI interface, which is routed to the COM-HPC connector, supports onboard the serial flash (for BIOS firmware) and the TPM chip.

Following Flash Devices are supported by the BIOS:

- MT25QL512ABB1EW9-0SIT
- W25Q512JVEIQ

3.5.8 Embedded EEPROM

The module's 32 kbit serial EEPROM (formerly known as JIDA EEPROM) device is attached to the I2C bus (I2C_EXT) from the Embedded Controller and accessible via I2C bus 8-bit address 0x0A (see chapter 3.4.11).

3.5.9 Features on Request

On the COMh-sdID following optional features are available on request:

Optional Features (on request)	
NVMe SSD	Up to 1 TByte NVMe PCIe SSD NAND Flash - TLC technology - configuration as pSLC can be offered
PCIe for BMC	Support of PCIe x1 to carrier for an BMC
2nd SPI Flash	On-module fail-safe 2nd SPI flash implemented for additional safety
UART	2 UART serial RX/TX ports from SOC (PCIe based, non-legacy, no RTS/CTS) instead of Embedded Controller

3.6 Electrical Specification

The module powers on by connecting to a carrier board via the COM-HPC interface connectors. The COM-HPC interface connector pins on the module limit the amount of power received.

Before connecting the module's interface connector to the carrier board's corresponding connector, ensure that the carrier board is switched off and disconnected from the main power supply. Failure to disconnect the main power supply could result in personal injury and damage to the module and/or carrier board.

Observe that only trained personnel aware of the associated dangers connect the module, within an access controlled ESD-safe workplace

3.6.1 Power Supply Specification

The power specification of the module supports a supply voltage of 12 V. Other supported voltages are 5 V standby and 3.3 V RTC battery input

Supply Voltage (VCC)	12 V ± 5%
Standby Voltage (VCC_5V_SBY)	5 V ± 5% - Note: Standby voltage is not mandatory for operation
RTC Voltage (VCC_RTC)	2.8 V to 3.47 V

Table 27: Electrical Specification

Only connect to an external power supply delivering the specified input rating and complying with the requirements of Safety Extra Low Voltage (SELV) and Limited Power Source (LPS) of UL/IEC 60950-1 or (PS2) of UL/IEC 62368-1.

To protect external power lines of peripheral devices, make sure that the wires have the right diameter to withstand the maximum available current and the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN 62368-1.

If any of the supply voltages drops below the allowed operating level longer than the specified hold-up time, all the supply voltages should be shut down and left OFF for a time long enough to allow the internal board voltages to discharge sufficiently.

If the OFF time is not observed, parts of the board or attached peripherals may work incorrectly or even suffer a reduction of MTBF. The minimum OFF time depends on the implemented PSU model and other electrical factors and must be measured individually for each case.

Power Supply Voltage Rise Time

The input voltage rise time is 0.1 ms to 20 ms from input voltage ≤10% to nominal input voltage. To comply with the ATX specification there must be a smooth and continuous ramp of each DC input voltage from 10 % to 90 % of the DC input voltage final set point.

Power Supply Voltage Ripple

The maximum power supply voltage ripple and noise is 200 mV peak-to-peak measured over a frequency bandwidth of 0 MHz to 20 MHz. The voltage ripple, must not cause the input voltage range to be exceeded.

Power Supply Inrush Current

The maximum inrush current at 5 V standby is 2 A. From states G3 (module is mechanically completely off, with no power consumption) or S5 (module appears to be completely off) to state S0 (module is fully usable) the maximum inrush current meets the SFX Design Guide.

3.6.2 Power Management

The Advanced Configuration and Power Interface (ACPI) 6.0 hardware specification supports features such as power button and suspend states. The power management options are available within the BIOS set up menu: **Advanced>ACPI Settings>**

Suspend States

If power is removed, 5V can be applied to the V_5V_SBY pins to support the ACPI suspend-states:

- Suspend to RAM (S3)
- Suspend to Disk (S4)
- Soft-off (S5)

If power is removed, the wake-up event (S0) requires 12V VCC to power on the module for normal operation.

Power Supply Control Signals

Power supply control settings are set in the BIOS and enable the module to shut down, reset and wake from standby.

COM-HPC Signal	Pin	Description
Power Button (PWRBTN#)	B02	A PWRBTN# falling edge signal creates power button event (50 ms ≤ t < 4 s, typical 400 ms) at low level). Power button events can be used to bring a system out of S5 soft-off and other suspend states, as well as powering the system down. Pressing the power button for at least four seconds turns off power to the module Power Button Override.
Power Good (VIN_PWR_OK)	C06	Indicates that all power supplies to the module are stable within specified ranges. PWR_OK signal goes active and module internal power supplies are enabled. PWR_OK can be driven low to prevent module from powering up until the carrier is ready and releases the signal. PWR_OK should not be deactivated after the module enters S0 unless there is a power fail condition.
Reset Button (RSTBTN#)	C02	Reset button input. The RSTBTN# may be level sensitive (active low) or may be triggered by the falling edge of the signal. There are some situations in which it is desirable for a sustained low state of the RSTBTN# to keep the CPU Module unit in a reset condition. This situation comes up with large Carrier or module based FPGAs that need more time to be loaded and configured than the CPU boot time allows. Therefore, COM-HPC Module designs should either keep the CPU Module in a reset state while RSTBTN# is low, or they should pause the boot process in an early state while RSTBTN# is low. This can be done by the Module BIOS monitoring the RSTBTN# line through an I/O port. The BIOS should be paused in an early point, before PCIe and USB enumerations take place. Additionally, the Module PLTRST# signal (below) should not be released (driven or pulled high) while the RSTBTN# is low. For situations when RSTBTN# is not able to reestablish control of the system, VIN_PWR_OK or a power cycle may be used.
Platform Reset (PLTRST#)	A12	Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.
Suspend to RAM (SUS_S3#)	B08	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board should be used to enable the non-standby power on a typical ATX supply. Even in single input supply system implementations (AT mode, no standby input), the SUS_S3# Module output should be used disable any Carrier voltage regulators when SUS_S3# is low, to prevent bleed leakage from Carrier circuits into the Module.
Suspend to Disk (SUS_S4_S5#)	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.
Suspend Clock (SUS_CLK)	A87	32.768 kHz +/- 100 ppm clock used by Carrier peripherals such as M.2 cards in their low power modes.
PCIe Wake UP (WAKE0#)	D10	PCI Express wake up signal.

COM-HPC Signal	Pin	Description
GP Wake UP (WAKE1#)	D11	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.
Battery Low (BATLOW#)	A11	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.
Lid detection (LID#)	B45	LID switch. COM-HPC/Client only: Low active signal used by the ACPI operating system for a LID switch.
Sleep button (SLEEP#)	B46	Sleep button. COM-HPC/Client only: Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.
Tamper Signal (TAMPER#)	B06	Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a Tamper event.
No power (AC_PRESENT)	D34	Driven hard low on Carrier if system AC power is not present.
Resume Reset (RSMRST_OUT#)	B86	This is a buffered copy of the internal Module RSMRST# (Resume Reset, active low) signal. The internal Module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable. USB devices on the Carrier that are to be active in S5 / S3 / S0 should not have their 5V supply applied before RSMRST_OUT# goes high. RSMRST_OUT# shall be a 3.3V CMOS Module output, active in all power states.

Table 28: Power Supply Control Signals

3.7.5 Temperature Sensors

The modules's processor is capable of reading its internal temperature. The on-module Hardware Monitor (HWM), located in the embedded controller (EC), uses an on-chip temperature sensor to measure the modules's temperature on the board.

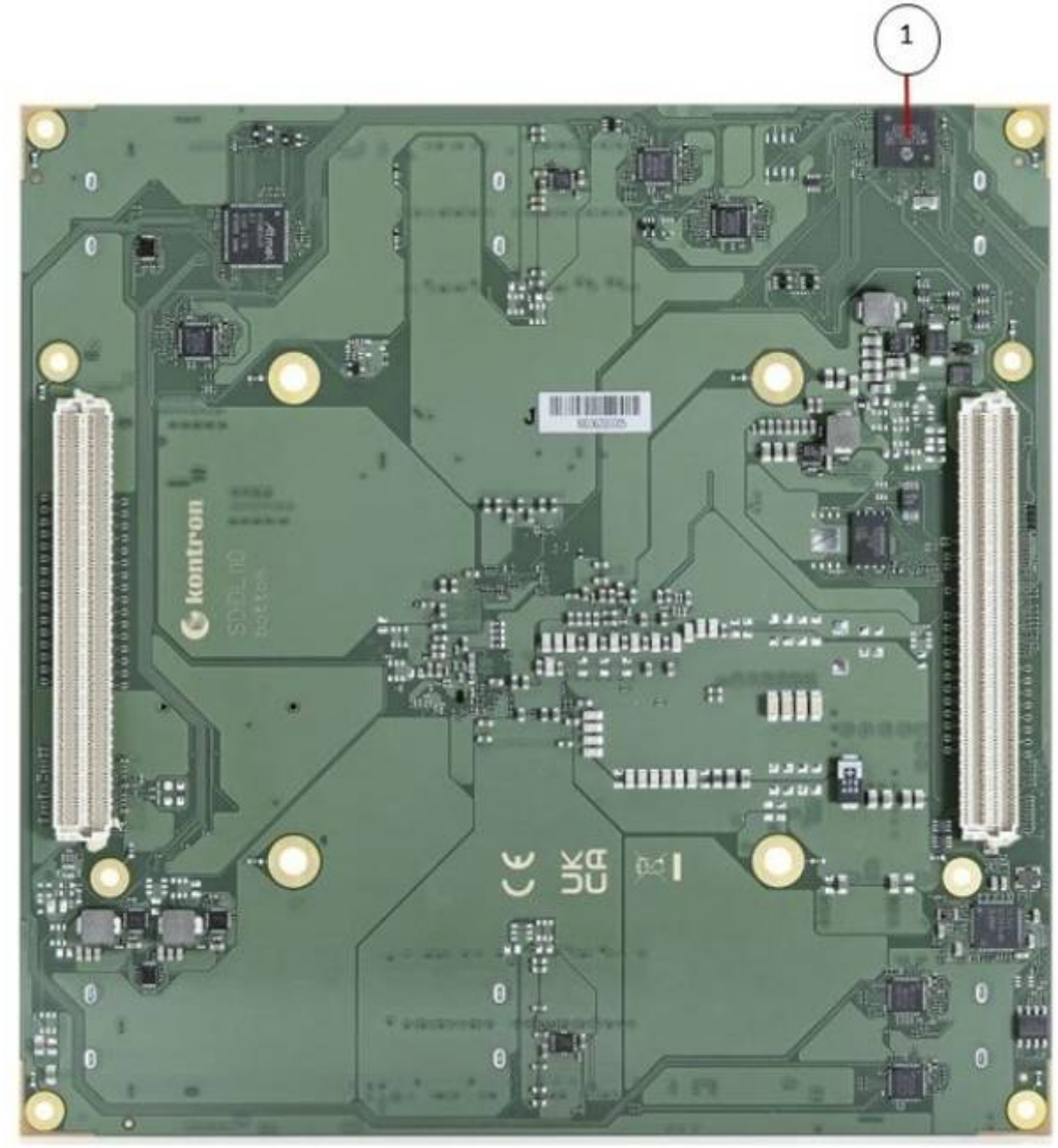

Figure 7: Module Temperature Sensor

3.7.6 On-Module Fan Connector

The module's fan connector powers, controls and monitors an external fan. To connect a standard 3-pin connector fan to the module, use fan cables:
KAB-HSP 200 mm (96079-0000-00-0)
KAB-HSP 400 mm (96079-0000-00-2)

Position of the fan connector see chapter 3.3.3

Pin	Signal	Description	Type
1	Fan_Tach_IN#	Fan input voltage from COMh connector	Input
2	V_FAN	12 V ±10% (max.) across module input range	PWR
3	GND	Power GND	PWR

Table 29: Fan Connector (3-Pin) Pin Assignment

Always check the fan specification according to the limitations of the supply current and supply voltage.

3.8 Mechanical Specification

The COMh-sdID is compatible with the COM-HPC® Server Size D mechanical specification.

3.8.1 Module Dimensions

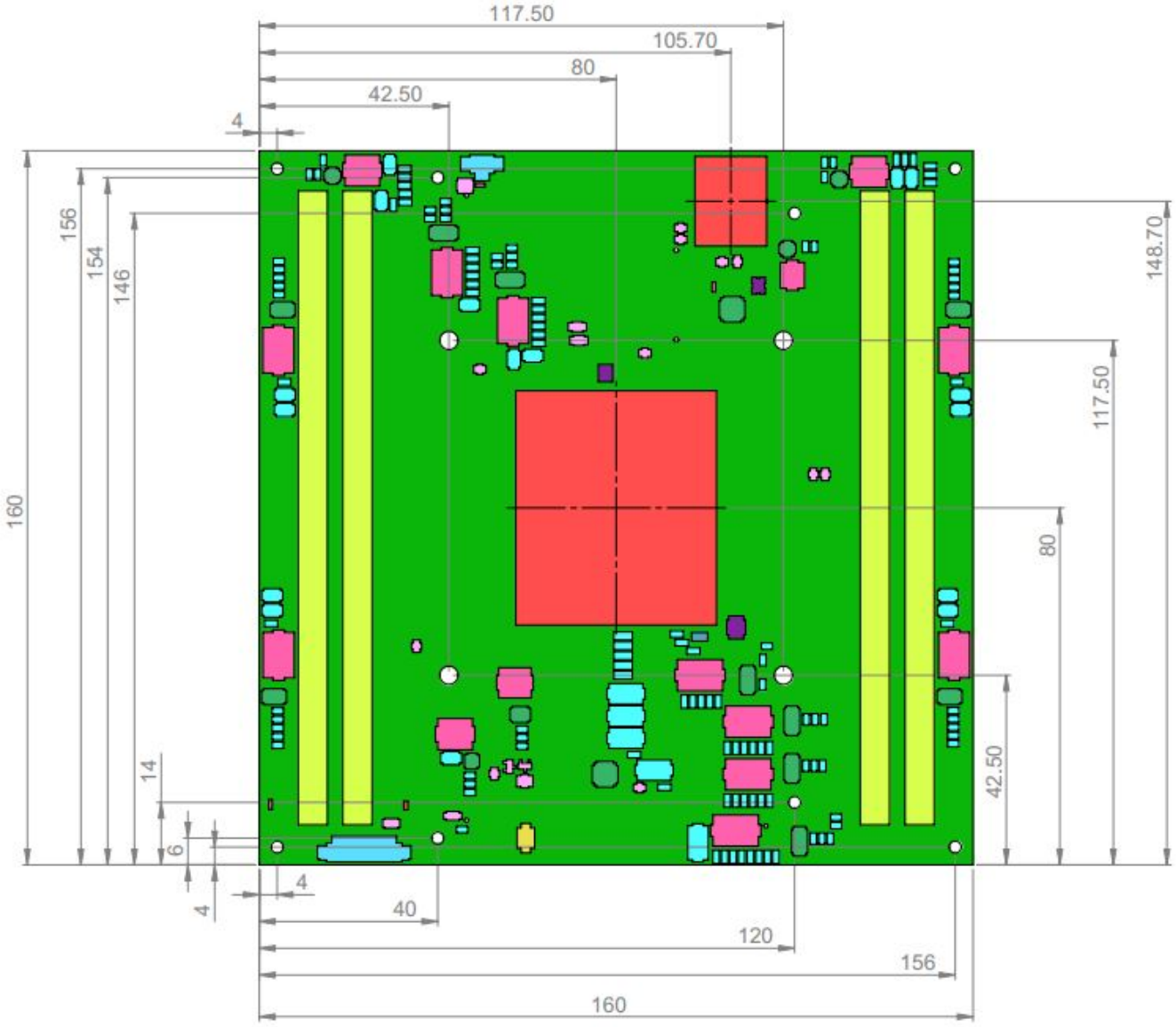

Figure 8: Module Dimensions

3.8.2 Module Height

The COM-HPC specification defines a module height of approximatly 18mm, when measured from the bottom of the module's PCB board to the top of the heatspreader. The overall height of the module and carrier board depends on

- which carrier board connectors are used (5mm and 10mm height are available)
- which cooling solution is used. The height of the cooling solution is not specified in the COM-HPC specification

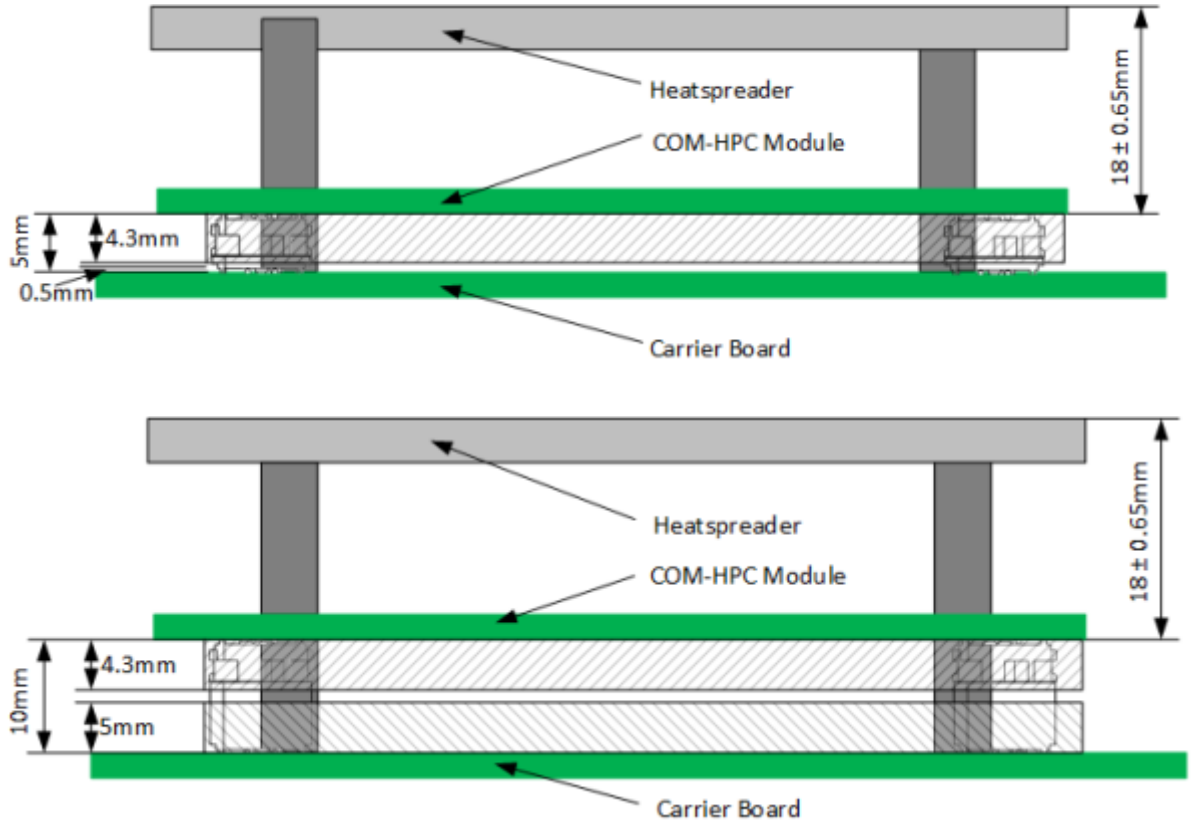

Figure 9: Module and Carrier Height with 10mm and 5mm connector height

3.8.3 Heatspreader Plate Assembly Dimension

Please check our Customer Section for Heatspreader 3D models and drawings.

3.9 Environmental Specification

The COMh-sdID supports commercial and industrial temperature grades.

Environmental		**Description**
Commercial Grade	Operating	0°C to +60°C (32°F to 140°F)
	Non-operating	-30°C to +85°C (-22°F to 185°F)
Industrial Grade (E2)	Operating	-40°C to +85°C (-40°F to 185°F)
	Non-operating	-40°C to +85°C (-22°F to 185°F)
Relative Humidity		93 % @40°C, non-condensing
Shock (according to IEC / EN 60068-2-27)		Non-operating shock test (half-sinusoidal, 11ms, 15g)
Vibration (according to IEC / EN 60068-2-6)		Non-operating vibration (sinusoidal, 10 Hz to 2000 Hz, +/- 0.15 mm, 2 g)

Table 30: Environmental Specification

3.10 Compliance

The COMh-sdID complies with the following or the latest status thereof. If modified, the prerequisites for specific approvals may no longer apply. For more information, contact JUMPtec Support.

Europe - CE Mark	
Directives	**2014/30/EU**: Electromagnetic Compatibility **2014/35/EU**: Low Voltage **2011/65/EU**: RoHS II **2001/95/EC**: General Product Safety
EMC	**EN 55032 Class B**: Electromagnetic compatibility of multimedia equipment - Emission Requirements Class A **EN 61000-6-2**: Electromagnetic compatibility (EMC) Part 6-2: Generic standards - Immunity standard for industrial environments
Safety	**EN 62368-1**: Audio/video, information and communication technology equipment - Part 1: Safety requirements

Table 31: Compliance CE Mark

USA/Canada	
Safety	**UL 62368-1 & CSA C22.2 No. 62368-1 (Component Recognition)**: Audio/video, information and communication technology equipment - Part 1: Safety requirements Recognized by Underwriters Laboratories Inc. Representative samples of this component have been evaluated by UL and meet applicable UL requirements. **UL listings**: AZOT2.E547070 AZOT8.E547070
UK CA Mark	
EMC	**BS EN 55032 Class B**: Electromagnetic compatibility of multimedia equipment - Emission Requirements Class A **BS EN 61000-6-2**: Electromagnetic compatibility (EMC) Part 6-2: Generic standards - Immunity standard for industrial environments
Safety	**BS EN 62368-1**: Audio/video, information and communication technology equipment - Part 1: Safety requirements
CB scheme (For International Certifications)	
Safety	**IEC 62368-1**: Audio/video, information and communication technology equipment - Part 1: Safety requirements

Table 32: Country Compliance

If the product is modified, the prerequisites for specific approvals may no longer apply.

JUMPtec is not responsible for any radio television interference caused by unauthorized modifications of the delivered product or the substitution or attachment of connecting cables and equipment other than those specified by JUMPtec. The correction of interference caused by unauthorized modification, substitution or attachment is the user’s responsibility.

3.11 MTBF

The MTBF (Mean Time Before Failure) values were calculated using a combination of the manufacturer's test data (if available) and the Telcordia (Bellcore) issue 2 calculation for the remaining parts.
The Telcordia calculation used is "Method 1 Case 3" in a ground benign, controlled environment. This particular method takes into account varying temperature and stress data and the system is assumed to have not been burned-in. Other environmental stresses (such as extreme altitude, vibration, salt-water exposure) lower MTBF values.

	MTBF Value @40°C	**Part Number**
MTBF (hours)	488445	HSD02-0010-96-1EVL

Table 33: MTBF

The MTBF estimated value above assumes no fan, but a passive heat sinking arrangement. Estimated RTC battery life (as opposed to battery failures) is not accounted for and needs to be considered separately. Battery life depends on both temperature and operating conditions. When the module is connected to external power, the only battery drain is from leakage paths.

4. COM-HPC Interface Connector

The COMh-sdID is a COM-HPC® Server module populated with two 400-pin connectors J1 and J2; each with 4 rows called rows and all rows are named
A to D on the primary connector J1
E to H on the secondary connector J2

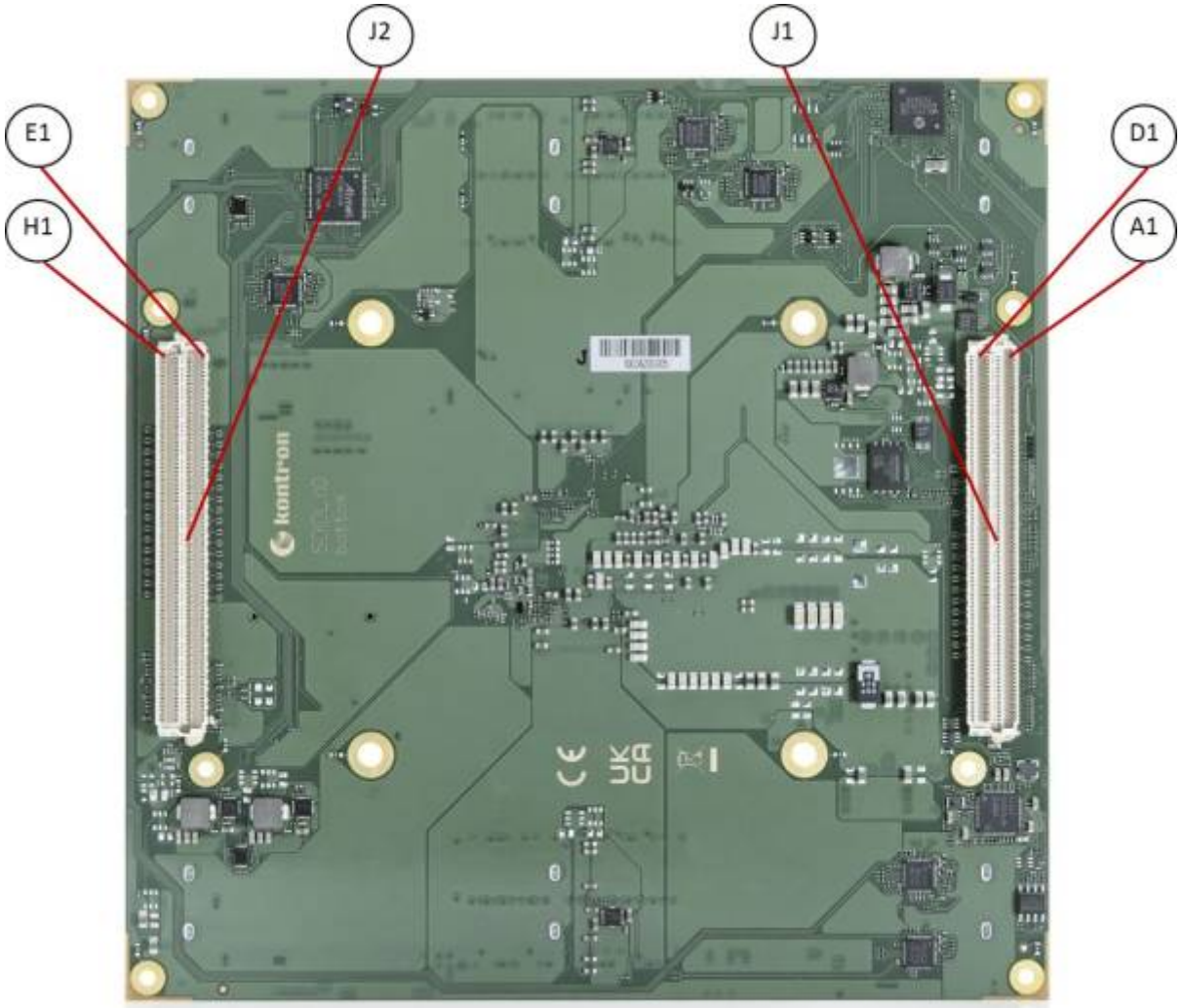

Figure 10: COM-HPC Interface Connectors

4.1 Connecting COM-HPC Interface Connector to Carrier Board

The COM-HPC interface connectors (J1, J2) are inserted into the corresponding connectors on the carrier board and secured using the mounting points and standoffs. The height of the standoffs depends on the height of the carrier board's connector.

The module is powered on by connecting to the carrier board using the interface connector. Before connecting the module's interface connector to the carrier board's corresponding connector, ensure that the carrier board is switch off and disconnected from the main power supply. Failure to disconnect the main power supply could result in

personal injury and damage to the module and/or carrier board. Observe that only trained personnel aware of the associated dangers connect the module, within an access controlled ESD-safe workplace.

To protect external power lines of peripheral devices, make sure that the wires have the right diameter to withstand the maximum available current. The enclosure of the peripheral device fulfills the fire-protection requirements of IEC/EN 62368.

4.2 J1 and J2 signals

The type of an interface pin consists of the pin type and the buffer type.

Pin Types	Description
I	Input to the Module
O	Output from the Module
I/O	Bi-directional input / output signal
OD	Open drain output
REF	Analog reference voltage output – low voltage (GND min, 3.3V max)

Table 34: Pin Types

Buffer Types	Description
CMOS	Logic input or output. Input thresholds and output levels shall be at or over 80% of supply rail for the high side and at or under 20% of the relevant supply rail for the low side.
LV_DIFF	Low voltage differential signals – may include DP, TMDS, DP_AUX, MIPI D-PHY and HCSL (High Speed Current Steering Logic) used for PCIe clock pairs. Exact details for these variants differ, but the all of these signals are well under 3.3V and the LV_DIFF type label serves well to describe them as a group.
KR	Ethernet 25GBASE-KR or 10GBASE-KR compatible signal.
KX	Ethernet 1000BASE-KX compatible signal.
DP	Display Port compatible signal. Used for DDI interfaces.
MDI	Media Dependent Interface, used for NBASE-T signaling.
NFET	N channel FET output, drain pin, Module can pull low to GND or float.
PCIE	PCI Express compatible differential signals. Includes signaling up to PCIe Gen 5.
PDS	Pull-down strap. Module either pulls these lines to GND or leaves them open.
SATA	SATA compatible differential signals.
USB	USB 2.0 compliant differential signals.
USB_SS	USB Super Speed compliant signals; includes USB 3.0, USB 3.1, USB 3.2 and USB4.

Table 35: Buffer Types

Other Notation	Description
PD	Pull-Down
PU	Pull-Up
2K2	2.2 Kohm resistor (and so on for other values)

Table 36: Other Notation

4.3 Connector J1

4.3.1 Pins A1 - A100 / B1 - B100

	Row A		Row B	
Pin #	Name	Type / Module Termination	Name	Type / Module Termination
1	VCC	Main Supply Input	VCC	Main Supply Input
2	VCC	Main Supply Input	PWRBTN#	In - 10K PU (3.3V S5)
3	VCC	Main Supply Input	VCC	Main Supply Input
4	VCC	Main Supply Input	THERMTRIP#	Out – Push-pull
5	VCC	Main Supply Input	VCC	Main Supply Input
6	VCC	Main Supply Input	TAMPER#	In – 1M PU (2.5V RTC G3)
7	VCC	Main Supply Input	VCC	Main Supply Input
8	VCC	Main Supply Input	SUS_S3#	Out – Push-pull
9	VCC	Main Supply Input	VCC	Main Supply Input
10	GND	Ground	WD_STROBE#	In - 10K PU (3.3V S0)
11	BATLOW#	In - 10K PU (3.3V S5)	WD_OUT	Out – Push-pull
12	PLTRST#	Out – Push-Pull	GND	Ground
13	GND	Ground	USB5-	Not Connected
14	USB7-	Not Connected	USB5+	Not Connected
15	USB7+	Not Connected	GND	Ground
16	GND	Ground	USB4-	Not Connected
17	USB6-	Not Connected	USB4+	Not Connected
18	USB6+	Not Connected	GND	Ground
19	GND	Ground	RSVD	Not Connected
20	ETH4_RX-	SERDES Receive	RSVD	Not Connected
21	ETH4_RX+	SERDES Receive	RSVD	Not Connected
22	GND	Ground	RSVD	Not Connected
23	ETH5_RX-	SERDES Receive	RSVD	Not Connected
24	ETH5_RX+	SERDES Receive	VCC_5V_SBY	Standby Supply Input
25	GND	Ground	USB67_OC#	In – 10K PU (3.3V S5)
26	ETH6_RX-	SERDES Receive	USB45_OC#	In – 10K PU (3.3V S5)
27	ETH6_RX+	SERDES Receive	USB23_OC#	In – 10K PU (3.3V S5)
28	GND	Ground	USB01_OC#	In – 10K PU (3.3V S5)
29	ETH7_RX-	SERDES Receive	SML1_CLK	In – 10K PU (3.3V S5)
30	ETH7_RX+	SERDES Receive	SML1_DAT	In – 10K PU (3.3V S5)
31	GND	Ground	PMCALERT#	In - 10K PU (3.3V S0)

	Row A		Row B	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
32	RSVD	Not Connected	SML0_CLK	In – 10K PU (3.3V S5)
33	RSVD	Not Connected	SML0_DAT	In – 10K PU (3.3V S5)
34	GND	Ground	USB_PD_ALERT#	In – 10K PU (3.3V S5)
35	ETH4_TX-	SERDES Transmit	USB_PD_I2C_CLK	Out – 10K PU (3.3V S5)
36	ETH4_TX+	SERDES Transmit	USB_PD_I2C_DAT	Bi – 10K PU (3.3V S5)
37	GND	Ground	USB_RT_ENA	In – 10K PU (3.3V S0)
38	ETH5_TX-	SERDES Transmit	USB1_LSRX	In – 10K PD
39	ETH5_TX+	SERDES Transmit	USB1_LSTX	In – 10K PD
40	GND	Ground	USB0_LSRX	In – 10K PD
41	ETH6_TX-	SERDES Transmit	USB0_LSTX	In – 10K PD
42	ETH6_TX+	SERDES Transmit	GND	Ground
43	Ground	Ground	USB0_AUX-	Not Connected
44	ETH7_TX-	SERDES Transmit	USB0_AUX+	Not Connected
45	ETH7_TX+	SERDES Transmit	RSVD	Not Connected
46	GND	Ground	RSVD	Not Connected
47	USB1_AUX-	Not Connected	VCC_BOOT_SPI	SPI Supply Output
48	USB1_AUX+	Not Connected	BOOT_SPI_CS#	Out – Push-pull
49	GND	Ground	BSEL0	10K PU (3.3V S5)
50	eSPI_IO0	Bi – 20K PU (1.8V S5)	BSEL1	10K PU (3.3V S5)
51	eSPI_IO1	Bi – 20K PU (1.8V S5)	BSEL2	10K PU (3.3V S5)
52	eSPI_IO2	Bi – 20K PU (1.8V S5)	eSPI_ALERT0#	In – 20K PU (1.8V S5)
53	eSPI_IO3	Bi – 20K PU (1.8V S5)	eSPI_ALERT1#	In – 20K PU (1.8V S5)
54	eSPI_CLK	Out – 20K PD	eSPI_CS0#	Out – 20K PU (1.8V S5)
55	GND	Ground	eSPI_CS1#	Out – 20K PU (1.8V S5)
56	PCIe_CLKREQ0_LO#	In - 10K PU (3.3V S0)	eSPI_RST#	Out – 20K PU (1.8V S5)
57	PCIe_CLKREQ0_HI#	In - 10K PU (3.3V S0)	GND	Ground
58	GND	Ground	PCIe_BMC_RX-	HSIO Receive
59	PCIe_BMC_TX-	HSIO Transmit	PCIe_BMC_RX+	HSIO Receive
60	PCIe_BMC_TX+	HSIO Transmit	GND	Ground
61	Ground	Ground	PCIe08_RX-	HSIO Receive
62	PCIe08_TX-	HSIO Transmit	PCIe08_RX+	HSIO Receive
63	PCIe08_TX+	HSIO Transmit	GND	Ground
64	GND	Ground	PCIe09_RX-	HSIO Receive
65	PCIe09_TX-	HSIO Transmit	PCIe09_RX+	HSIO Receive
66	PCIe09_TX+	HSIO Transmit	GND	Ground
67	GND	Ground	PCIe10_RX-	HSIO Receive
68	PCIe10_TX-	HSIO Transmit	PCIe10_RX+	HSIO Receive
69	PCIe10_TX+	HSIO Transmit	GND	Ground
70	GND	Ground	PCIe11_RX-	HSIO Receive
71	PCIe11_TX-	HSIO Transmit	PCIe11_RX+	HSIO Receive
72	PCIe11_TX+	HSIO Transmit	GND	Ground
73	GND	Ground	PCIe12_RX-	HSIO Receive
74	PCIe12_TX-	HSIO Transmit	PCIe12_RX+	HSIO Receive

	Row A		Row B	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
75	PCIe12_TX+	HSIO Transmit	GND	Ground
76	GND	Ground	PCIe13_RX-	HSIO Receive
77	PCIe13_TX-	HSIO Transmit	PCIe13_RX+	HSIO Receive
78	PCIe13_TX+	HSIO Transmit	GND	Ground
79	GND	Ground	PCIe14_RX-	HSIO Receive
80	PCIe14_TX-	HSIO Transmit	PCIe14_RX+	HSIO Receive
81	PCIe14_TX+	HSIO Transmit	GND	Ground
82	GND	Ground	PCIe15_RX-	HSIO Receive
83	PCIe15_TX-	HSIO Transmit	PCIe15_RX+	HSIO Receive
84	PCIe15_TX+	HSIO Transmit	GND	Ground
85	GND	Ground	RSVD	HPC_TEST
86	VCC_RTC	RTC Supply Input	RSMRST_OUT#	Out – Push-pull
87	SUS_CLK	Output – Push-Pull + 20K PD	UART1_TX	Output – Push-Pull
88	GPIO_00	100K PU (3.3V S5)	UART1_RX	10K PU (3.3V S0)
89	GPIO_01	100K PU (3.3V S5)	UART1_RTS#	Output – Push-Pull
90	GPIO_02	100K PU (3.3V S5)	UART1_CTS#	10K PU (3.3V S0)
91	GPIO_03	100K PU (3.3V S5)	IPMB_CLK	47K PU (3.3V S5)
92	GPIO_04	100K PU (3.3V S5)	IPMB_DAT	47K PU (3.3V S5)
93	GPIO_05	100K PU (3.3V S5)	GP_SPI_MOSI	Output – Push-pull
94	GPIO_06	100K PU (3.3V S5)	GP_SPI_MISO	In – 10K PU (3.3V S0)
95	GPIO_07	100K PU (3.3V S5)	GP_SPI_CS0#	Output – Push-pull
96	GPIO_08	100K PU (3.3V S5)	GP_SPI_CS1#	Output – Push-pull
97	GPIO_09	100K PU (3.3V S5)	GP_SPI_CS2#	Output – Push-pull
98	GPIO_10	100K PU (3.3V S5)	GP_SPI_CS3#	Output – Push-pull
99	GPIO_11	100K PU (3.3V S5)	GP_SPI_CLK	Output – Push-pull
100	TYPE0	Ground	GP_SPI_ALERT#	10K PU (3.3V S0)

Table 37: Connector J1 Pins A1 - A100 / B1 - B100

4.3.2 Pins C1 - C100 / D1 - D100

	Row C		Row D	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
1	VCC	Main Supply Input	VCC	Main Supply Input
2	RSTBTN#	In - 10K PU (3.3V S5)	VCC	Main Supply Input
3	VCC	Main Supply Input	VCC	Main Supply Input
4	CARRIER_HOT#	In - 10K PU (3.3V S0)	VCC	Main Supply Input
5	VCC	Main Supply Input	VCC	Main Supply Input
6	VIN_PWROK	In - 22K PU (3.3V S0/S5)	VCC	Main Supply Input
7	VCC	Main Supply Input	VCC	Main Supply Input
8	SUS_S4_S5#	Out - Push-pull	VCC	Main Supply Input
9	VCC	Main Supply Input	VCC	Main Supply Input

	Row C		Row D	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
10	GND	Ground	WAKE0#	In - 10K PU (3.3V S5)
11	FAN_PWMOUT	Out - Push-pull	WAKE1#	In - 10K PU (3.3V S5)
12	FAN_TACHIN	In - 10K PU (3.3V S0)	GND	Ground
13	GND	Ground	USB1-	USB2 PHY
14	USB3-	USB2 PHY	USB1+	USB2 PHY
15	USB3+	USB2 PHY	GND	Ground
16	GND	Ground	USB0-	USB2 PHY
17	USB2-	USB2 PHY	USB0+	USB2 PHY
18	USB2+	USB2 PHY	GND	Ground
19	GND	Ground	ETH0_RX-	SERDES Receive
20	ETH0_TX-	SERDES Transmit	ETH0_RX+	SERDES Receive
21	ETH0_TX+	SERDES Transmit	GND	Ground
22	GND	Ground	ETH1_RX-	SERDES Receive
23	ETH1_TX-	SERDES Transmit	ETH1_RX+	SERDES Receive
24	ETH1_TX+	SERDES Transmit	GND	Ground
25	GND	Ground	ETH2_RX-	SERDES Receive
26	ETH2_TX-	SERDES Transmit	ETH2_RX+	SERDES Receive
27	ETH2_TX+	SERDES Transmit	GND	Ground
28	GND	Ground	ETH3_RX-	SERDES Receive
29	ETH3_TX-	SERDES Transmit	ETH3_RX+	SERDES Receive
30	ETH3_TX+	SERDES Transmit	GND	Ground
31	GND	Ground	USB3_SSTX-	HSIO Transmit / 100nF series
32	USB3_SSRX-	HSIO Receive	USB3_SSTX+	HSIO Transmit / 100nF series
33	USB3_SSRX+	HSIO Receive	GND	Ground
34	GND	Ground	USB2_SSTX-	HSIO Transmit / 100nF series
35	USB2_SSRX-	HSIO Receive	USB2_SSTX+	HSIO Transmit / 100nF series
36	USB2_SSRX+	HSIO Receive	GND	Ground
37	GND	Ground	USB1_SSTX0-	HSIO Transmit / 100nF series
38	USB1_SSRX0-	HSIO Receive	USB1_SSTX0+	HSIO Transmit / 100nF series
39	USB1_SSRX0+	HSIO Receive	GND	Ground
40	GND	Ground	USB1_SSTX1-	Not connected
41	USB1_SSRX1-	Not connected	USB1_SSTX1+	Not connected
42	USB1_SSRX1+	Not connected	GND	Ground
43	GND	Ground	USB0_SSTX0-	HSIO Transmit / 100nF series
44	USB0_SSRX0-	HSIO Receive	USB0_SSTX0+	HSIO Transmit / 100nF series
45	USB0_SSRX0+	HSIO Receive	GND	Ground
46	GND	Ground	USB0_SSTX1-	Not connected

	Row C		Row D	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
47	USB0_SSRX1-	Not connected	USB0_SSTX1+	Not connected
48	USB0_SSRX1+	Not connected	GND	Ground
49	GND	Ground	SATA0_RX-	HSIO Receive
50	BOOT_SPI_IO0	Bi - 20k PU (V_SPI / 3.3V S5 on SDID)	SATA0_RX+	HSIO Receive
51	BOOT_SPI_IO1	Bi - 20k PU (V_SPI / 3.3V S5 on SDID)	GND	Ground
52	BOOT_SPI_IO2	Bi - 20k PU (V_SPI / 3.3V S5 on SDID)	SATA0_TX-	HSIO Transmit / 10nF series
53	BOOT_SPI_IO3	Bi - 20k PU (V_SPI / 3.3V S5 on SDID)	SATA0_TX+	HSIO Transmit / 10nF series
54	BOOT_SPI_CLK	Out - 20k PU (V_SPI / 3.3V S5 on SDID)	GND	Ground
55	GND	Ground	SATA1_RX-	HSIO Receive
56	PCIe_REFCLK0_HI-	PCIE Clock Transmit	SATA1_RX+	HSIO Receive
57	PCIe_REFCLK0_HI+	PCIE Clock Transmit	GND	Ground
58	GND	Ground	SATA1_TX-	HSIO Transmit / 10nF series
59	PCIe_REFCLK0_LO-	PCIE Clock Transmit	SATA1_TX+	HSIO Transmit / 10nF series
60	PCIe_REFCLK0_LO+	PCIE Clock Transmit	GND	Ground
61	GND	Ground	PCIe00_TX-	HSIO Transmit / 100nF series
62	PCIe00_RX-	HSIO Receive	PCIe00_TX+	HSIO Transmit / 100nF series
63	PCIe00_RX+	HSIO Receive	GND	Ground
64	GND	Ground	PCIe01_TX-	HSIO Transmit / 100nF series
65	PCIe01_RX-	HSIO Receive	PCIe01_TX+	HSIO Transmit / 100nF series
66	PCIe01_RX+	HSIO Receive	GND	Ground
67	GND	Ground	PCIe02_TX-	HSIO Transmit / 100nF series
68	PCIe02_RX-	HSIO Receive	PCIe02_TX+	HSIO Transmit / 100nF series
69	PCIe02_RX+	HSIO Receive	GND	Ground
70	GND	Ground	PCIe03_TX-	HSIO Transmit / 100nF series
71	PCIe03_RX-	HSIO Receive	PCIe03_TX+	HSIO Transmit / 100nF series
72	PCIe03_RX+	HSIO Receive	GND	Ground
73	GND	Ground	PCIe04_TX-	HSIO Transmit / 100nF series
74	PCIe04_RX-	HSIO Receive	PCIe04_TX+	HSIO Transmit / 100nF series
75	PCIe04_RX+	HSIO Receive	GND	Ground

	Row C		Row D	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
76	GND	Ground	PCIe05_TX-	HSIO Transmit / 100nF series
77	PCIe05_RX-	HSIO Receive	PCIe05_TX+	HSIO Transmit / 100nF series
78	PCIe05_RX+	HSIO Receive	GND	Ground
79	GND	Ground	PCIe06_TX-	HSIO Transmit / 100nF series
80	PCIe06_RX-	HSIO Receive	PCIe06_TX+	HSIO Transmit / 100nF series
81	PCIe06_RX+	HSIO Receive	GND	Ground
82	GND	Ground	PCIe07_TX-	HSIO Transmit / 100nF series
83	PCIe07_RX-	HSIO Receive	PCIe07_TX+	HSIO Transmit / 100nF series
84	PCIe07_RX+	HSIO Receive	GND	Ground
85	GND	Ground	NBASET0_MDI0-	NBase-T MDI
86	SMB_CLK	Out - 3K3 PU (3.3V S5)	NBASET0_MDI0+	NBase-T MDI
87	SMB_DAT	Bi - 3K3 PU (3.3V S5)	GND	Ground
88	SMB_ALERT#	In - 3K3 PU (3.3V S5)	NBASET0_MDI1-	NBase-T MDI
89	UART0_TX	Output - Push-Pull	NBASET0_MDI1+	NBase-T MDI
90	UART0_RX	10K PU (3.3V S0)	GND	Ground
91	UART0_RTS#	Output - Push-Pull	NBASET0_MDI2-	NBase-T MDI
92	UART0_CTS#	10K PU (3.3V S0)	NBASET0_MDI2+	NBase-T MDI
93	I2C0_CLK	Out - 2K2 PU (3.3V S5)	GND	Ground
94	I2C0_DAT	Bi - 2K2 PU (3.3V S5)	NBASET0_MDI3-	NBase-T MDI
95	I2C0_ALERT#	In - 2K2 PU (3.3V S5)	NBASET0_MDI3+	NBase-T MDI
96	I2C1_CLK	Out - 2K2 PU (1.8V S5)	GND	Ground
97	I2C1_DAT	Bi - 2K2 PU (1.8V S5)	NBASET0_LINK_MAX#	Out - Push-pull
98	NBASET0_SDP	Bi - No Termination (3.3V S5)	NBASET0_LINK_MID#	Out - Push-pull
99	NBASET0_CTREF	1uF to Ground	NBASET0_LINK_ACT#	Out - Push-pull
100	TYPE1	Ground	TYPE2	Not connected

Table 38: Connector J1 Pins C1 - C100 / D1 - D100

4.4 Connector J2

4.4.1 Pins E1 - E100 / F1 - F100

	Row E		Row F	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
1	RAPID_SHUTDOWN	In – 100K PD	ETH2_SDP	Bi – 20K PU (3.3V S5) after RSMRST

	Row E		Row F	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
2	GND	Ground	ETH3_SDP	Bi – 20K PU (3.3V S5) after RSMRST
3	RSVD	Not connected	ETH4_SDP	Not connected
4	RSVD	Not connected	ETH5_SDP	Not connected
5	GND	Ground	ETH6_SDP	Not connected
6	RSVD	Not connected	ETH7_SDP	Not connected
7	RSVD	Not connected	ETH4-7_I2C_CLK	Out – 2K2 PU (3.3V S5)
8	GND	Ground	ETH4-7_I2C_DAT	Bi – 2K2 PU (3.3V S5)
9	RSVD	Not connected	ETH4-7_INT#	In – 2K2 PU (3.3V S5)
10	RSVD	Not connected	ETH4-7_MDIO_CLK	Out – 2K2 PU (3.3V S5) – Shared ETH0-3
11	GND	Ground	ETH4-7_MDIO_DAT	Bi – 2K2 PU (3.3V S5) – Shared ETH0-3
12	RSVD	Not connected	ETH4-7_PHY_INT#	In – 2K2 PU (3.3V S5)
13	RSVD	Not connected	ETH4-7_PHY_RST#	Out – 10k PD
14	GND	Ground	ETH4-7_PRSNT#	In – 2K2 PU (3.3V S5)
15	RSVD	Not connected	RSVD	Not connected
16	RSVD	Not connected	RSVD	Not connected
17	GND	Ground	RSVD	Not connected
18	RSVD	Not connected	RSVD	Not connected
19	RSVD	Not connected	GND	Ground
20	GND	Ground	PCIe32_RX-	HSIO Receive
21	PCIe32_TX-	HSIO Transmit / 100nF series	PCIe32_RX+	HSIO Receive
22	PCIe32_TX+	HSIO Transmit / 100nF series	GND	Ground
23	GND	Ground	PCIe33_RX-	HSIO Receive
24	PCIe33_TX-	HSIO Transmit / 100nF series	PCIe33_RX+	HSIO Receive
25	PCIe33_TX+	HSIO Transmit / 100nF series	GND	Ground
26	GND	Ground	PCIe34_RX-	HSIO Receive
27	PCIe34_TX-	HSIO Transmit / 100nF series	PCIe34_RX+	HSIO Receive
28	PCIe34_TX+	HSIO Transmit / 100nF series	GND	Ground
29	GND	Ground	PCIe35_RX-	HSIO Receive
30	PCIe35_TX-	HSIO Transmit / 100nF series	PCIe35_RX+	HSIO Receive
31	PCIe35_TX+	HSIO Transmit / 100nF series	GND	Ground
32	GND	Ground	PCIe36_RX-	HSIO Receive
33	PCIe36_TX-	HSIO Transmit / 100nF series	PCIe36_RX+	HSIO Receive
34	PCIe36_TX+	HSIO Transmit / 100nF series	GND	Ground

	Row E		Row F	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
35	GND	Ground	PCIe37_RX-	HSIO Receive
36	PCIe37_TX-	HSIO Transmit / 100nF series	PCIe37_RX+	HSIO Receive
37	PCIe37_TX+	HSIO Transmit / 100nF series	GND	Ground
38	GND	Ground	PCIe38_RX-	HSIO Receive
39	PCIe38_TX-	HSIO Transmit / 100nF series	PCIe38_RX+	HSIO Receive
40	PCIe38_TX+	HSIO Transmit / 100nF series	GND	Ground
41	GND	Ground	PCIe39_RX-	HSIO Receive
42	PCIe39_TX-	HSIO Transmit / 100nF series	PCIe39_RX+	HSIO Receive
43	PCIe39_TX+	HSIO Transmit / 100nF series	GND	Ground
44	GND	Ground	PCIe16_RX-	HSIO Receive
45	PCIe16_TX-	HSIO Transmit / 100nF series	PCIe16_RX+	HSIO Receive
46	PCIe16_TX+	HSIO Transmit / 100nF series	GND	Ground
47	GND	Ground	PCIe17_RX-	HSIO Receive
48	PCIe17_TX-	HSIO Transmit / 100nF series	PCIe17_RX+	HSIO Receive
49	PCIe17_TX+	HSIO Transmit / 100nF series	GND	Ground
50	GND	Ground	PCIe18_RX-	HSIO Receive
51	PCIe18_TX-	HSIO Transmit / 100nF series	PCIe18_RX+	HSIO Receive
52	PCIe18_TX+	HSIO Transmit / 100nF series	GND	Ground
53	GND	Ground	PCIe19_RX-	HSIO Receive
54	PCIe19_TX-	HSIO Transmit / 100nF series	PCIe19_RX+	HSIO Receive
55	PCIe19_TX+	HSIO Transmit / 100nF series	GND	Ground
56	GND	Ground	PCIe20_RX-	HSIO Receive
57	PCIe20_TX-	HSIO Transmit / 100nF series	PCIe20_RX+	HSIO Receive
58	PCIe20_TX+	HSIO Transmit / 100nF series	GND	Ground
59	GND	Ground	PCIe21_RX-	HSIO Receive
60	PCIe21_TX-	HSIO Transmit / 100nF series	PCIe21_RX+	HSIO Receive
61	PCIe21_TX+	HSIO Transmit / 100nF series	GND	Ground
62	GND	Ground	PCIe22_RX-	HSIO Receive

	Row E		Row F	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
63	PCIe22_TX-	HSIO Transmit / 100nF series	PCIe22_RX+	HSIO Receive
64	PCIe22_TX+	HSIO Transmit / 100nF series	GND	Ground
65	GND	Ground	PCIe23_RX-	HSIO Receive
66	PCIe23_TX-	HSIO Transmit / 100nF series	PCIe23_RX+	HSIO Receive
67	PCIe23_TX+	HSIO Transmit / 100nF series	GND	Ground
68	GND	Ground	PCIe48_RX-	HSIO Receive
69	PCIe48_TX-	HSIO Transmit / 100nF series	PCIe48_RX+	HSIO Receive
70	PCIe48_TX+	HSIO Transmit / 100nF series	GND	Ground
71	GND	Ground	PCIe49_RX-	HSIO Receive
72	PCIe49_TX-	HSIO Transmit / 100nF series	PCIe49_RX+	HSIO Receive
73	PCIe49_TX+	HSIO Transmit / 100nF series	GND	Ground
74	GND	Ground	PCIe50_RX-	HSIO Receive
75	PCIe50_TX-	HSIO Transmit / 100nF series	PCIe50_RX+	HSIO Receive
76	PCIe50_TX+	HSIO Transmit / 100nF series	GND	Ground
77	GND	Ground	PCIe51_RX-	HSIO Receive
78	PCIe51_TX-	HSIO Transmit / 100nF series	PCIe51_RX+	HSIO Receive
79	PCIe51_TX+	HSIO Transmit / 100nF series	GND	Ground
80	GND	Ground	PCIe52_RX-	HSIO Receive
81	PCIe52_TX-	HSIO Transmit / 100nF series	PCIe52_RX+	HSIO Receive
82	PCIe52_TX+	HSIO Transmit / 100nF series	GND	Ground
83	GND	Ground	PCIe53_RX-	HSIO Receive
84	PCIe53_TX-	HSIO Transmit / 100nF series	PCIe53_RX+	HSIO Receive
85	PCIe53_TX+	HSIO Transmit / 100nF series	GND	Ground
86	GND	Ground	PCIe54_RX-	HSIO Receive
87	PCIe54_TX-	HSIO Transmit / 100nF series	PCIe54_RX+	HSIO Receive
88	PCIe54_TX+	HSIO Transmit / 100nF series	GND	Ground
89	GND	Ground	PCIe55_RX-	HSIO Receive
90	PCIe55_TX-	HSIO Transmit / 100nF series	PCIe55_RX+	HSIO Receive

	Row E		Row F	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
91	PCIe55_TX+	HSIO Transmit / 100nF series	GND	Ground
92	GND	Ground	PCIe_REFCLK2-	PCIE Clock Transmit
93	PCIe_REFCLK1-	PCIE Clock Transmit	PCIe_REFCLK2+	PCIE Clock Transmit
94	PCIe_REFCLK1+	PCIE Clock Transmit	GND	Ground
95	GND	Ground	PCIe_CLKREQ3#	In – 10K PU (3.3V S0)
96	PCIe_CLKREQ1#	In – 10K PU (3.3V S0)	ETH0-3_PRSNT#	In – 2K2 PU (3.3V S5)
97	PCIe_CLKREQ2#	In – 10K PU (3.3V S0)	ETH0-3_PHY_RST#	Out – 10k PD
98	PCIe_CLKREQ_OUT0#	Not connected	ETH0_SDP	Bi – 20K PU (3.3V S5) after RSMRST
99	PCIe_CLKREQ_OUT1#	Not connected	ETH1_SDP	Bi – 20K PU (3.3V S5) after RSMRST
100	PCIe_PERST_IN0#	Not used – 100K PD	PCIe_PERST_IN1#	Not used – 100K PD

Table 39: Connector J1 Pins E1 - E100 / F1 - F100

4.4.2 Pins G1 - G100 / H1 - H100

	Row G		Row H	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
1	RSVD	Not connected	RSVD	Not connected
2	RSVD	Not connected	RSVD	Not connected
3	RSVD	Not connected	RSVD	Not connected
4	RSVD	Not connected	RSVD	Not connected
5	RSVD	Not connected	RSVD	Not connected
6	RSVD	Not connected	RSVD	Not connected
7	RSVD	Not connected	RSVD	Not connected
8	RSVD	Not connected	RSVD	Not connected
9	RSVD	Not connected	RSVD	Not connected
10	RSVD	Not connected	RSVD	Not connected
11	RSVD	Not connected	RSVD	Not connected
12	RSVD	Not connected	RSVD	Not connected
13	RSVD	Not connected	RSVD	Not connected
14	GND	Ground	RSVD	Not connected
15	RSVD	Not connected	RSVD	Not connected
16	RSVD	Not connected	RSVD	Not connected
17	RSVD	Not connected	RSVD	Not connected
18	RSVD	Not connected	RSVD	Not connected
19	RSVD	Not connected	GND	Ground
20	GND	Ground	PCIe40_TX-	HSIO Transmit / 100nF series
21	PCIe40_RX-	HSIO Receive	PCIe40_TX+	HSIO Transmit / 100nF series
22	PCIe40_RX+	HSIO Receive	GND	Ground
23	GND	Ground	PCIe41_TX-	HSIO Transmit / 100nF series

	Row G		Row H	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
24	PCIe41_RX-	HSIO Receive	PCIe41_TX+	HSIO Transmit / 100nF series
25	PCIe41_RX+	HSIO Receive	GND	Ground
26	GND	Ground	PCIe42_TX-	HSIO Transmit / 100nF series
27	PCIe42_RX-	HSIO Receive	PCIe42_TX+	HSIO Transmit / 100nF series
28	PCIe42_RX+	HSIO Receive	GND	Ground
29	GND	Ground	PCIe43_TX-	HSIO Transmit / 100nF series
30	PCIe43_RX-	HSIO Receive	PCIe43_TX+	HSIO Transmit / 100nF series
31	PCIe43_RX+	HSIO Receive	GND	Ground
32	GND	Ground	PCIe44_TX-	HSIO Transmit / 100nF series
33	PCIe44_RX-	HSIO Receive	PCIe44_TX+	HSIO Transmit / 100nF series
34	PCIe44_RX+	HSIO Receive	GND	Ground
35	GND	Ground	PCIe45_TX-	HSIO Transmit / 100nF series
36	PCIe45_RX-	HSIO Receive	PCIe45_TX+	HSIO Transmit / 100nF series
37	PCIe45_RX+	HSIO Receive	GND	Ground
38	GND	Ground	PCIe46_TX-	HSIO Transmit / 100nF series
39	PCIe46_RX-	HSIO Receive	PCIe46_TX+	HSIO Transmit / 100nF series
40	PCIe46_RX+	HSIO Receive	GND	Ground
41	GND	Ground	PCIe47_TX-	HSIO Transmit / 100nF series
42	PCIe47_RX-	HSIO Receive	PCIe47_TX+	HSIO Transmit / 100nF series
43	PCIe47_RX+	HSIO Receive	GND	Ground
44	GND	Ground	PCIe24_TX-	HSIO Transmit / 100nF series
45	PCIe24_RX-	HSIO Receive	PCIe24_TX+	HSIO Transmit / 100nF series
46	PCIe24_RX+	HSIO Receive	GND	Ground
47	GND	Ground	PCIe25_TX-	HSIO Transmit / 100nF series
48	PCIe25_RX-	HSIO Receive	PCIe25_TX+	HSIO Transmit / 100nF series
49	PCIe25_RX+	HSIO Receive	GND	Ground
50	GND	Ground	PCIe26_TX-	HSIO Transmit / 100nF series
51	PCIe26_RX-	HSIO Receive	PCIe26_TX+	HSIO Transmit / 100nF series
52	PCIe26_RX+	HSIO Receive	GND	Ground
53	GND	Ground	PCIe27_TX-	HSIO Transmit / 100nF series
54	PCIe27_RX-	HSIO Receive	PCIe27_TX+	HSIO Transmit / 100nF series
55	PCIe27_RX+	HSIO Receive	GND	Ground
56	GND	Ground	PCIe28_TX-	HSIO Transmit / 100nF series
57	PCIe28_RX-	HSIO Receive	PCIe28_TX+	HSIO Transmit / 100nF series
58	PCIe28_RX+	HSIO Receive	GND	Ground
59	GND	Ground	PCIe29_TX-	HSIO Transmit / 100nF series
60	PCIe29_RX-	HSIO Receive	PCIe29_TX+	HSIO Transmit / 100nF series
61	PCIe29_RX+	HSIO Receive	GND	Ground
62	GND	Ground	PCIe30_TX-	HSIO Transmit / 100nF series
63	PCIe30_RX-	HSIO Receive	PCIe30_TX+	HSIO Transmit / 100nF series
64	PCIe30_RX+	HSIO Receive	GND	Ground
65	GND	Ground	PCIe31_TX-	HSIO Transmit / 100nF series
66	PCIe31_RX-	HSIO Receive	PCIe31_TX+	HSIO Transmit / 100nF series

	Row G		Row H	
Pin #	**Name**	**Type / Module Termination**	**Name**	**Type / Module Termination**
67	PCIe31_RX+	HSIO Receive	GND	Ground
68	GND	Ground	PCIe56_TX-	HSIO Transmit / 100nF series
69	PCIe56_RX-	HSIO Receive	PCIe56_TX+	HSIO Transmit / 100nF series
70	PCIe56_RX+	HSIO Receive	GND	Ground
71	GND	Ground	PCIe57_TX-	HSIO Transmit / 100nF series
72	PCIe57_RX-	HSIO Receive	PCIe57_TX+	HSIO Transmit / 100nF series
73	PCIe57_RX+	HSIO Receive	GND	Ground
74	GND	Ground	PCIe58_TX-	HSIO Transmit / 100nF series
75	PCIe58_RX-	HSIO Receive	PCIe58_TX+	HSIO Transmit / 100nF series
76	PCIe58_RX+	HSIO Receive	GND	Ground
77	GND	Ground	PCIe59_TX-	HSIO Transmit / 100nF series
78	PCIe59_RX-	HSIO Receive	PCIe59_TX+	HSIO Transmit / 100nF series
79	PCIe59_RX+	HSIO Receive	GND	Ground
80	GND	Ground	PCIe60_TX-	HSIO Transmit / 100nF series
81	PCIe60_RX-	HSIO Receive	PCIe60_TX+	HSIO Transmit / 100nF series
82	PCIe60_RX+	HSIO Receive	GND	Ground
83	GND	Ground	PCIe61_TX-	HSIO Transmit / 100nF series
84	PCIe61_RX-	HSIO Receive	PCIe61_TX+	HSIO Transmit / 100nF series
85	PCIe61_RX+	HSIO Receive	GND	Ground
86	GND	Ground	PCIe62_TX-	HSIO Transmit / 100nF series
87	PCIe62_RX-	HSIO Receive	PCIe62_TX+	HSIO Transmit / 100nF series
88	PCIe62_RX+	HSIO Receive	GND	Ground
89	GND	Ground	PCIe63_TX-	HSIO Transmit / 100nF series
90	PCIe63_RX-	HSIO Receive	PCIe63_TX+	HSIO Transmit / 100nF series
91	PCIe63_RX+	HSIO Receive	GND	Ground
92	GND	Ground	PCIe_REFCLKIN0-	Not connected
93	PCIe_REFCLK3-	PCIE Clock Transmit	PCIe_REFCLKIN0+	Not connected
94	PCIe_REFCLK3+	PCIE Clock Transmit	GND	Ground
95	GND	Ground	PCIe_REFCLKIN1-	Not connected
96	ETH0-3_I2C_CLK	Out – 2K2 PU (3.3V S5)	PCIe_REFCLKIN1+	Not connected
97	ETH0-3_I2C_DAT	Bi – 2K2 PU (3.3V S5)	GND	Ground
98	ETH0-3_PHY_INT#	In – 2K2 PU (3.3V S5)	ETH0-3_MDIO_CLK	Out – 2K2 PU (3.3V S5) – Shared ETH4-7
99	ETH0-3_INT#	In – 2K2 PU (3.3V S5)	ETH0-3_MDIO_DAT	Bi – 2K2 PU (3.3V S5) – Shared ETH4-7
100	PCIe_WAKE_OUT0#	Not connected	PCIe_WAKE_OUT1#	Not connected

Table 40: Connector J1 Pins G1 - G100 / H1 - H100

5. UEFI BIOS

5.1 Starting the UEFI BIOS

The COMh-sdID uses a JUMPtec-customized, pre-installed and configured version of AMI Aptio® V BIOS based on the Unified Extensible Firmware Interface (UEFI) specification and the Intel® Platform Innovation Framework for EFI.
The UEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the COMh-sdID.

This chapter provides an overview of the BIOS and its setup. A more detailed listing and description of all BIOS setup nodes can be found in the BIOS file package available on our Customer Section. Please register there to get access to BIOS downloads and Product Change Notifications.

The UEFI BIOS comes with a Setup program that provides quick and easy access to the individual function settings for control or modification of the default configuration. The Setup program allows access to various menus resp. sub-menus that provide the specific functions.
To start the UEFI BIOS Setup program, follow the steps below:

1. Power on the board
2. Wait until the first characters appear on the screen (POST messages or splash screen)
3. Press the <DEL> key
4. If the UEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password
5. The Setup menu appears

5.2 Navigating the UEFI BIOS

The COMh-sdID UEFI BIOS Setup program uses a hot key navigation system with a corresponding legend bar displayed on the setup screens. The following table provides a list of navigation hot keys available in the legend bar.

Hot Key	Description
<F1>	<F1> key invokes the General Help window
< - >	<Minus> key selects the next lower value within a field
<+>	<Plus> key selects the next higher value within a field
<F2>	<F2> key loads previous values
<F3>	<F3> key loads optimized defaults
<F4>	<F4> key Saves and Exits
<←> or <→>	<Left/Right> arrows select major Setup menus on menu bar, for example, Main or Advanced
<↑> or <↓>	<Up/Down> arrows select fields in the current menu, for example, Setup function or sub-screen
<ESC>	<ESC> key exits a major Setup menu and enters the Exit Setup menu. Pressing the <ESC> key in a sub-menu displays the next higher menu level
<RETURN>	<RETURN> key executes a command or selects a sub-menu

Table 41: Navigation Hot Keys Available in the Legend Bar

5.3 Setup Menus

The Setup utility features a selection bar at the top of the screen that lists the menus

Figure 11: Setup Menu Selection Bar

The Setup menus available for the COMh-sdID are:

- Main
- Advanced
- Chipset
- Security
- Boot
- Save & Exit

The currently active menu is highlighted in grey, the currently active UEFI BIOS Setup item in white. Use the left and right arrow keys to select the Setup menu.
Each Setup menu provides two main frames. The left frame displays all available functions and configurable ones are displayed in blue. Functions displayed in grey provide information about the status or the operational configuration.

5.4 Getting Help

The right frame displays a help window. The help window provides an explanation of the respective function.

5.5 UEFI Shell

The JUMPtec UEFI BIOS features a built-in and enhanced version of the UEFI Shell. For a detailed description of the available standard shell scripting, refer to the EFI Shell User Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage: http://sourceforge.net/projects/efi-shell/files/documents/.

JUMPtec UEFI BIOS does not provide all shell commands described in the EFI Shell Command Manual.

5.5.1 Entering the UEFI Shell

To enter the UEFI Shell, follow the steps below:

1. Power on the board
2. Press the <F7> key (instead of <DEL>) to display a choice of boot devices
3. Select 'UEFI: Built-in EFI shell'

```
UEFI Interactive Shell v2.2
EDK II / JUMPtec add-on v0.3
UEFI v2.80 (American Megatrands, 0x0005001A)
map: No mapping found.
```

1. Press the <ESC> key within 5 seconds to skip startup.nsh or any other key to continue
2. The output produced by the device-mapping table can vary depending on the board's configuration
3. If the <ESC> key is pressed before the 5 second timeout elapses, the shell prompt is shown:

```
Shell>
```

5.5.2 Exiting the UEFI Shell

To exit the UEFI Shell, follow one of the steps below:

- Use the **exit** UEFI Shell command to select the boot device, in the Boot menu, that the OS boots from
- Reset the board using the **reset** UEFI Shell command
- Press the reset button of the board or power down/up the board

5.6 UEFI Shell Scripting

5.6.1 Startup Scripting

If the <ESC> key is not pressed and the timeout has run out, then the UEFI Shell automatically tries to execute some startup scripts. The UEFI shell searches for scripts and executes them in the following order:

1. Initially searches for JUMPtec flash-stored startup script
2. If there is no JUMPtec flash-stored startup script present, then the UEFI-specified **startup.nsh** script is used. This script must be located on the root of any of the attached FAT-formatted disk drives
3. If none of the startup scripts are present or the startup script terminates then the default boot order is continued

5.6.2 Create a Startup Script

Startup scripts can be created using the UEFI Shell built-in editor **edit** or under any OS with a plain text editor of your choice.

5.6.3 Example of Startup Scripts

Execute Shell Script on other Harddrive

This example (**startup.nsh**) executes the shell script named **bootme.nsh** located in the root of the first detected disk drive (**fs0**).

```
fs0:
bootme.nsh
```

5.7 Firmware Update

Firmware updates are typically delivered as a ZIP archive. Please find the latest available BIOS-ZIP archive on JUMPtec's Customer Section. Further information about the firmware update procedure can be found in the included “flash_instruction.txt”-file.

Register to JUMPtec's Customer Section to get access to BIOS downloads, additional documentation and Product Change Notification service.

6. Technical Support

For technical support contact our Support Department:

E-Mail:	techsupport@jumptec.com

Make sure you have the following information available when contacting us:

- Product ID Number (PN)
- Serial Number (SN)
- Module’s revision
- Operating System and Kernel/Build version
- Software modifications
- Additional connected hardware/full description of hardware set up

The Serial Number can be found on the Type Label, located on the product.

Be ready to explain the nature of your problem to the service technician.

6.1 Warranty

Due to their limited service life, parts that by their nature are subject to a particularly high degree of wear (wearing parts) are excluded from the warranty beyond that provided by law.

If there is a protection label on your product, then the warranty is lost if the product is opened.

6.2 Returning Defective Material

All equipment returned to JUMPtec must have a Return of Material Authorization (RMA) number assigned exclusively by JUMPtec. JUMPtec cannot be held responsible for any loss or damage caused to the equipment received without an RMA number. The buyer accepts responsibility for all freight charges for the return of goods to JUMPtec’s designated facility. JUMPtec will pay the return freight charges back to the buyer’s location in the event that the equipment is repaired or replaced within the stipulated warranty period. Follow these steps before returning any product to JUMPtec:

1. Visit the RMA Information website: RMA Information - JUMPtec
2. Download the RMA Request sheet and fill out the form. Take care to include a short detailed description of the observed problem or failure and to include the product identification information (Name of product, Product Number and Serial Number). If a delivery includes more

than one product, fill out the above information in the RMA Request form for each product.

3. Send the completed RMA-Request form to the fax or email address given at JUMPtec GmbH. JUMPtec GmbH will provide an RMA-Number within one business day.
4. The goods for repair must be packed properly for shipping, considering shock and ESD protection.

Goods returned to JUMPtec GmbH in non-proper packaging will be considered as customer caused faults and cannot be accepted as warranty repairs.

5. Include the RMA-Number with the shipping paperwork and send the product to the delivery address provided in the RMA form or received from JUMPtec RMA Support.

7. Document Revision

The following table shows the revision of this document.

Revision	Author	Date	Comment
0.1	HIR	2023-02-15	initial preliminary release
0.2	HIR	2023-05-16	updated several pages
1.0	HIR	2023-07-03	released version
1.1	HIR	2024-02-19	add D-2800 support
1.2	HIR	2025-05-28	JUMPtec

Table 42: Document Revision Table