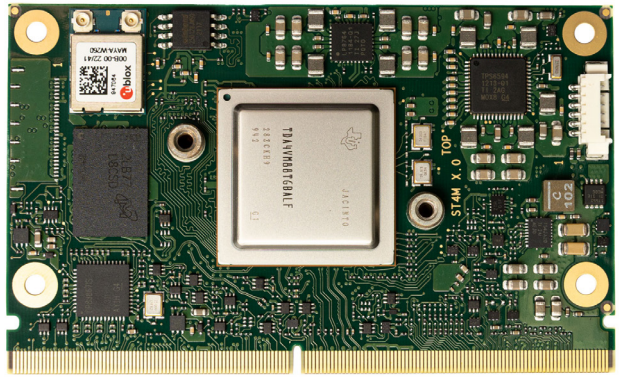

conga-STDA4

SMARC 2.2 Module with Jacinto™ 7 architecture from TI

User's Guide

Revision 0.1 (Preliminary)

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2025-08-04	RVI	• Preliminary release

Preface

This user's guide provides information about the components, features and connectors available on the conga-STDA4. It is one of five documents that should be referred to when designing a SMARC® application.

The other reference documents that should be used include the following:

SMARC® Design Guide 2.2 (https://sget.org)
SMARC® Specification 2.2 (https://sget.org)
TI Jacinto™ 7 Data Sheet (www.ti.com)

Ensure regular consultation of the customer login area at www.congatec.com and the congatec customer knowledge base at wiki.congatec.com for the most recent and legally binding product-related documents—such as errata sheets, list of limitation, and Product Change Notifications (PCNs).

Additionally, refer to the official websites of the respective silicon vendors for further information, including general chip limitations, errata sheets, sighting reports, and other technical or regulatory updates. These documents may contain mandatory and legally relevant information concerning product usage, compliance, and performance.

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Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Disclaimer

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RoHS Directive

All congatec GmbH designs comply with EU RoHS Directive 2011/65/EU and Delegated Directive 2015/863.

WEEE Directive

To comply with Directive 2012/19/EU on Waste Electrical and Electronic Equipment (WEEE), ensure that this product is disposed of correctly at the end of its lifecycle. Customers are required to take electrical and electronic equipment to designated collection facilities separate from unsorted municipal waste, following applicable regional laws.

Proper disposal through designated collection points allows for the recycling, recovery, and reuse of valuable materials, supporting a more efficient use of resources and reducing environmental impact.

Note

Standalone congatec components, such as modules, carrier boards, and cooling solutions are designed to function only within other products. WEEE registration for the complete product must be completed by the entity placing the final product on the market.

Electrostatic Sensitive Device

All congatec GmbH products are electrostatic sensitive devices. They are enclosed in static shielding bags, and shipped enclosed in secondary packaging (protective packaging). The secondary packaging does not provide electrostatic protection.

Do not remove the device from the static shielding bag or handle it, except at an electrostatic-free workstation. Also, do not ship or store electronic devices near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original packaging. Be aware that failure to comply with these guidelines will void the congatec GmbH Limited Warranty.

Wireless Regulatory Compliance

Declaration for Wireless Compliance

We hereby expressly point out that this product is not a radio/wireless equipment (end product) according to regulations such as the Radio Equipment Directive and the Federal Communications Commission (RED, FCC). This product is only a sub-assembly, which has to be integrated into the end product by the customer and is not functional without further integration. The customer is solely and exclusively responsible for complying with all applicable and local regulations relating to the end product (e.g., RED, FCC) and for having the necessary (testing) procedures and certifications carried out at their own expense.

Scope of System-Level Compliance Testing

Due to the modular nature of COMs and their broad applicability, congatec performs preliminary system-level compliance testing using representative commercial off-the-shelf (COTS) accessories, including antennas. The purpose of these tests is to demonstrate the feasibility of achieving compliance in final customer-designed products and to show that the functionality and conformity of the used Wi-Fi module is not limited by the congatec design. However, test results are limited exclusively to the specific configurations tested by congatec. The results cannot be transferred directly to alternative configurations or designs but can be shared with customers for further information.

Cybersecurity Compliance under RED

congatec has thoroughly evaluated cybersecurity requirements outlined in standards such as EN 18031-1. By design, COMs (Computer-on-Modules) do not include the hardware and software required to support standalone cybersecurity assessments. Therefore, congatec modules alone do not meet these cybersecurity requirements. Compliance with cybersecurity requirements is thus the responsibility of the final product manufacturer, who has detailed knowledge of the intended use and operating environment. congatec actively supports its customers by providing necessary technical documentation to aid in achieving cybersecurity compliance.

Cybersecurity Maintenance under IEC 62443-4-1

congatec provides security maintenance updates according to IEC 62443-4-1. This includes monitoring component supplier information about hardware and firmware security vulnerabilities of the Wi-Fi module.

congatec promptly informs customers about hardware and firmware security vulnerabilities via vulnerability disclosures and about product changes via Product Change Notifications (PCNs)—including changes implemented to mitigate security vulnerabilities. Customers are responsible for monitoring the PCNs, independently monitoring security vulnerabilities beyond hardware and firmware, assessing their implications, and implementing relevant security updates.

Certification Documentation for Wi-Fi Module

For certification and compliance documentation, refer to the Intel documentation or contact your local sales representative.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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The products may include software. Use of the software is subject to the terms and conditions set out in the respective owner's license agreements, which are available at www.congatec.com and/or upon request.

Beginning on the date of shipment to its direct customer and continuing for the published warranty period, congatec GmbH represents that the products are new and warrants that each product failing to function properly under normal use, due to a defect in materials or workmanship or due to non conformance to the agreed upon specifications, will be repaired or exchanged, at congatec's option and expense.

Customer will obtain a Return Material Authorization ("RMA") number from congatec GmbH prior to returning the non conforming product freight prepaid. congatec GmbH will pay for transporting the repaired or exchanged product to the customer.

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Except as set forth in writing in the Limited Warranty, congatec makes no performance representations, warranties, or guarantees, either express or implied, oral or written, with respect to the products, including without limitation any implied warranty (a) of merchantability, (b) of fitness for a particular purpose, or (c) arising from course of performance, course of dealing, or usage of trade.

congatec GmbH shall in no event be liable to the end user for collateral or consequential damages of any kind. congatec shall not otherwise be liable for loss, damage or expense directly or indirectly arising from the use of the product or from any other cause. The sole and exclusive remedy against congatec, whether a claim sound in contract, warranty, tort or any other legal theory, shall be repair or replacement of the product only.

Certification

congatec GmbH is certified to DIN EN ISO 9001 standard.

Technical Support

congatec GmbH technicians and engineers are committed to providing the best possible technical support for our customers so that our products can be easily used and implemented. We request that you first visit our website at www.congatec.com for the latest documentation, utilities and drivers, which have been made available to assist you. If you still require assistance after visiting our website then contact our technical support department by email at support@congatec.com.

Terminology

Term	Description
°C	Degrees Celsius
µA	Microamp
µs	Microsecond
A	Ampere
AI	Artificial-Intelligence
AN	Application Note
ARM	Advanced RISC Machine
BOM	Bill of Material
BT	Bluetooth
CAN	Controller Area Network
CMOS	Complementary Metal Oxide Semiconductor
COM	Computer-on-Module
CPU	Central Processing Unit
CSI	Camera Serial Interface
CSP	Cooling Solution Passive
DDR	Double Data Rate
DP	DisplayPort
DP++	DisplayPort Dual-Mode
DRAM	Dynamic Random Access Memory
DSI	Digital Serial Interface
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
eMMC	embedded Multi-Media Card
FET	Field-Effect Transistor
GB	Gigabyte
GbE	Gigabit Ethernet
GHz	Gigahertz
GND	Ground
GPIO	General-Purpose Input/Output
GPU	Graphics Processing Unit
HW	Hardware
HAB	High Assurance Boot
HSP	Heat Spreader
Hz	Hertz
I/O	Input/Output
I²C (I2C)	Inter-Integrated Circuit
I²S (I2S)	Inter-Integrated Circuit Sound
IEEE	Institute of Electrical and Electronics Engineers
JTAG	Joint Test Action Group
LPDDR	Low-Power Double Data Rate
LVDS	Low-Voltage Differential Signaling
MAC	Media Access Control
Mbps	Megabits per second
MBps	Megabytes per second
MCU	Micro-Controller Unit
MDIO	Management Data Input/Output
MHz	Megahertz
MIPI	Mobile Industry Processor Interface
mm	Millimeter
MMU	Memory Management Unit
MST	Multi-Stream Transport
mVpp	Millivolts Peak to Peak
MXM	Mobile PCI Express Module
N/A	Not Applicable
NC	Not Connected
Nm	Newton metre
OS	Operating System
OTG	On-The-Go
PCB	Printed Circuit Board
PCI Express	Peripheral Component Interconnect Express
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
PN	Part Number
pSLC	Pseudo Single Level Cell
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit-Media Independent Interface
RS-232	Recommended Standard 232
RTC	Real-Time Clock
RTOS	Real-Time Operating System
SD	Secure Digital
SDIO	Secure Digital Input Output
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SGET	Standardization Group for Embedded Technologies e.V
SMARC	Smart Mobility ARChitecture
SoC	System on Chip
SPI	Serial Peripheral Interface
STBY	Standby
SW	Software
TBD	To Be Defined
TI	Texas Instruments
UART	Universal Asynchronous Receiver-Transmitter
U-Boot	Universal Boot Loader
UHS	Ultra High Speed
USB	Universal Serial Bus
V	Volt
Vdc	Volts direct current
W	Watt
WD	Watchdog
Wi-Fi	Wireless Fidelity

Contents

List of Tables

1 Introduction

1.1 SMARC® Concept

The Standardization Group for Embedded Technologies e.V (SGET) defined the SMARC standard for small form factor computer modules that target applications with low power, low cost and high performance. The SMARC connector and interfaces are optimized for high-speed communication, and are suitable for ARM SoCs and low power x86 SoCs.

The SMARC standard bridges the gap between the COM Express standard and the Qseven standard by offering most of the interfaces defined in the COM Express specification at a lower power. With a footprint of 82 mm x 50 mm or 82 mm x 80 mm, the SMARC standard promotes the design of highly integrated, energy efficient systems.

Due to its small size and lower power demands, PC appliance designers can design low cost devices and also explore a huge variety of product development options, from compact space-saving designs to fully functional systems. This solution allows scalability, product diversification and faster time to market.

1.2 conga-STDA4

The conga-STDA4 is designed based on the SMARC 2.2 Specification and features TI TDA4VM Arm® Application processor and DRA829J Arm® Networking Processor. With a superior power to performance ratio, the conga-STDA4 is a unique combination of high-performance computing, deep-learning engine, dedicated accelerators for signal and image processing in a functional safety compliant targeted architecture, which makes conga-STDA4 a great choice for many industrial applications, such as industrial AI, real-time control, robotics, machine vision, autonomous mobility solutions and many more.

By offering most of the functional requirement for any SMARC application, the conga-STDA4 provides manufacturers and developers with a platform to jump-start the development of systems and applications based on SMARC specification. Its features and capabilities make it an ideal platform for designing compact, energy-efficient, performance-oriented embedded systems.

1.2.1 Options Information

The conga-STDA4 is available in 5 industrial variants:

Table 1 Industrial Variants

PN	051510	051511	051512	051513	051520
TI® Processor	TI TDA4VM Arm® Application Processor	TI TDA4VM Arm® Application Processor	TI DRA829J Arm® Networking processor	TI DRA829J Arm® Networking processor	TI TDA4VM Arm® Application processor
Cortex®-A72	2x 2.0 GHz	2x 2.0 GHz	2x 2.0 GHz	2x 2.0 GHz	2x 2.0 GHz
SDRAM	4 GB LPDDR4 @ 2133 MHz (32 bit)	2 GB LPDDR4 @ 2133 MHz (32 bit)	4 GB LPDDR4 @ 2133 MHz (32 bit)	2 GB LPDDR4 @ 2133 MHz (32 bit)	2 GB LPDDR4 @ 2133 MHz (32 bit)
Onboard eMMC	32GB	32GB	32GB	32GB	32GB
Ethernet	2x 1 Gigabit	2x 1 Gigabit	2x 1 Gigabit	2x 1 Gigabit	2x 1 Gigabit
Wi-Fi/BT	Optional	Optional	Optional	Optional	u-blox Wifi /BT module MAYA W260
USB	3x USB 2.0 2x USB 3.0	3x USB 2.0 2x USB 3.0	3x USB 2.0 2x USB 3.0	3x USB 2.0 2x USB 3.0	3x USB 2.0 2x USB 3.0
Audio	2x I²S	2x I²S	2x I²S	2x I²S	2x I²S

1.2.2 Accessories

Table 2 conga-STDA4 Accessories

PN	48000023	020750	007010	N/A
Product	RS-232 adapter cable for conga-ARM modules	conga-SMC1/SMARC-ARM	conga-SEVAL	conga-SKIT/TI ARM TDA4 Vision
Description	Adapter cable for ARM console. MOLEX PicoBlade 6 circuit to two D-SUB 9 connectors.	Compact sized 3.5" Carrier Board for ARM based SMARC 2.1 modules.	Evaluation Carrier Board for SMARC 2.1 modules.	Virtual Starterkit for SMARC 2.1 modules based on TI ARM Jacinto ARM processor TDA4VM.

2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	SMARC Module Specification 2.2	
SoC	TI TDA4VM and DRA829J Arm® Application and Networking Processors	
Memory	Up to 8GB based on single 32bit LPDDR4-4266	
Ethernet	2x Gbit Ethernet with IEEE 1588 support	
I/O Interfaces	1x dual-role USB 2.0 ; 2x USB 2.0 ; 2x USB 3.0 ; 1x SDIO 3.0 ; 2x PCIe 3.0 x1 + 1x PCIe 3.0 x2 ; 2x I²C ; 2x SPI ; 4x UART (2x with Handshake) ; 2x CAN FD ; 14x GPIO ; optional full industrial onboard u-blox WiFi/BT module	
Storage	eMMC 5.1 up to 128 GB	
Audio	2x I²S	
Video Interfaces	1x dual channel 24-bit LVDS ; 1x Display Port 1.3 supports up to 4096x2160p60 or up to four 1920x1080p60 via MST; optional 1x MIPI-DSI 4-lane shared with LVDS ; 2x MIPI-CSI	
Features	Watchdog timer ; Console Port ; Real Time Clock module with I2C	
Bootloader	U-Boot (stored in SPI Flash)	
Operating Systems	Linux	
Power Consumption	Typ. application 5-10W	
Temperature Range	Operating Temperature Range: Storage Temperature Range:	-40 to +85°C industrial grade -40 to +85°C
Humidity	Operating: 10 - 90% r. H. non cond.	Storage: 5 - 95% r. H. non cond.
Size	82 x 50 mm (3,23” x 1,97”)	

2.2 Supported Operating Systems

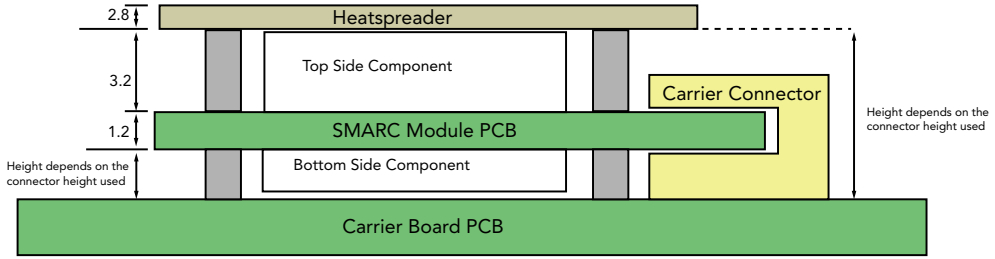
The conga-STDA4 supports the following operating systems:

- Linux® (Yocto Project®)

2.3 Mechanical Dimensions

- 82.0 mm x 50.0 mm

The height of the module, heatspreader and stack is shown below:



All dimensions are in millimeters

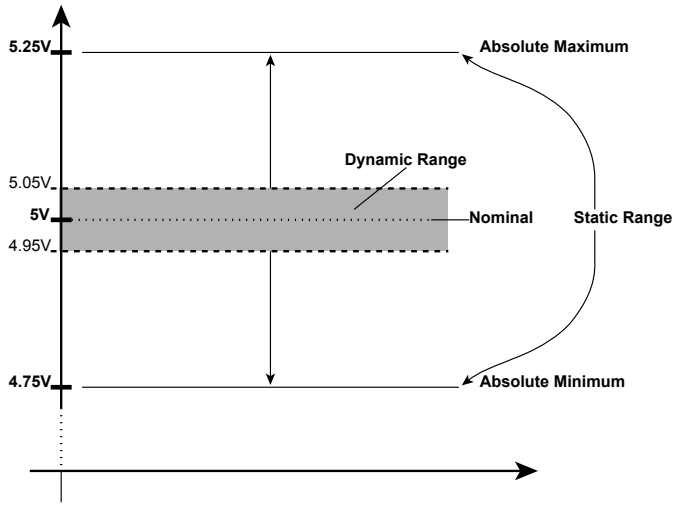
Note

1. *Maximum height of the connector for the console (X1) is 3.4mm*
2. *3D models of congatec products are available at* www.congatec.com/login. *These models indicate the overall length, height and width of each product. If you need login access, contact your local sales representative.*

2.4 Standard Power

2.4.1 Supply Voltage

- 4.75 V – 5.25 V



2.4.2 Electrical Characteristics

Table 4 Module Power

Characteristics			Min.	Typ.	Max.	Units	Comment
5V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV_{PP}	0-20 MHz
	Current						

2.4.3 Rise Time

The recommended rate for the input voltage rise is 1000V/s or less with a non-decreasing (monotonic) slope.

2.4.4 Inrush Current

The table below compares the inrush current and slew rate values of the conga-STDA4 at different voltage ramp durations.

Table 5 Inrush Current

Power Rail	Inrush Current [A]	Slew Rate [kV/s]	Voltage Ramp [ms]	Comment
VCC	TBD	TBD	TBD	Worst-case scenario
VCC_5V_SBY	TBD	TBD	TBD	
VCC	TBD	TBD	TBD	Typical scenario
VCC_5V_SBY	TBD	TBD	TBD	

Note

Ensure the power supply and decoupling capacitors on the carrier board are adequate for proper power sequencing.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- Input voltage +5 V
- conga-STDA4
- conga-SEVAL carrier board
- conga-STDA4 cooling solution
- conga-SMARC CSP adapter (cooling fan)

The power consumption values were recorded during the following operating modes:

Table 6 Measurement Description

Mode	Description	Comment
1	Full Active	The entire system, including Main and MCU domains, DDR, IO interfaces, and all peripherals, is fully powered and active.
2	Power-off	Lowest power state, where the majority of the device including all Cortex-A, Cortex-R, and Cortex-M cores, internal logic, and memory is fully powered down. Only the PMIC input power remains active.

The table below provides the power consumption values of each conga-STDA4 variant during different operating modes:

Table 7 Power Consumption Values

PN	Memory Size	HW Revision	SoC	Current (A) @ 5 V	
				1	2
051510	4GB	A.2	TI TDA4VM Arm® Application Processor	TBD	TBD
051511	2GB	A.2	TI TDA4VM Arm® Application Processor	TBD	TBD
051512	4GB	A.2	TI DRA829J Arm® Networking processor	TBD	TBD
051513	2GB	A.2	TI DRA829J Arm® Networking processor	TBD	TBD
051520	4GB	A.2	TI TDA4VM Arm® Application Processor	TBD	TBD

2.6 Supply Voltage Battery Power

Table 8 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	TBD µA
20°C	3V DC	TBD µA
70°C	3V DC	TBD µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-STDA4.*

2.7 Environmental Specifications

Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to +85°C
Relative Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

1. *The above operating temperatures must be strictly adhered to at all times. When using a congatec heat spreader, the maximum operating temperature refers to any measurable spot on the heat spreader's surface.*

2. *Humidity specifications are for non-condensing conditions.*

2.8 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

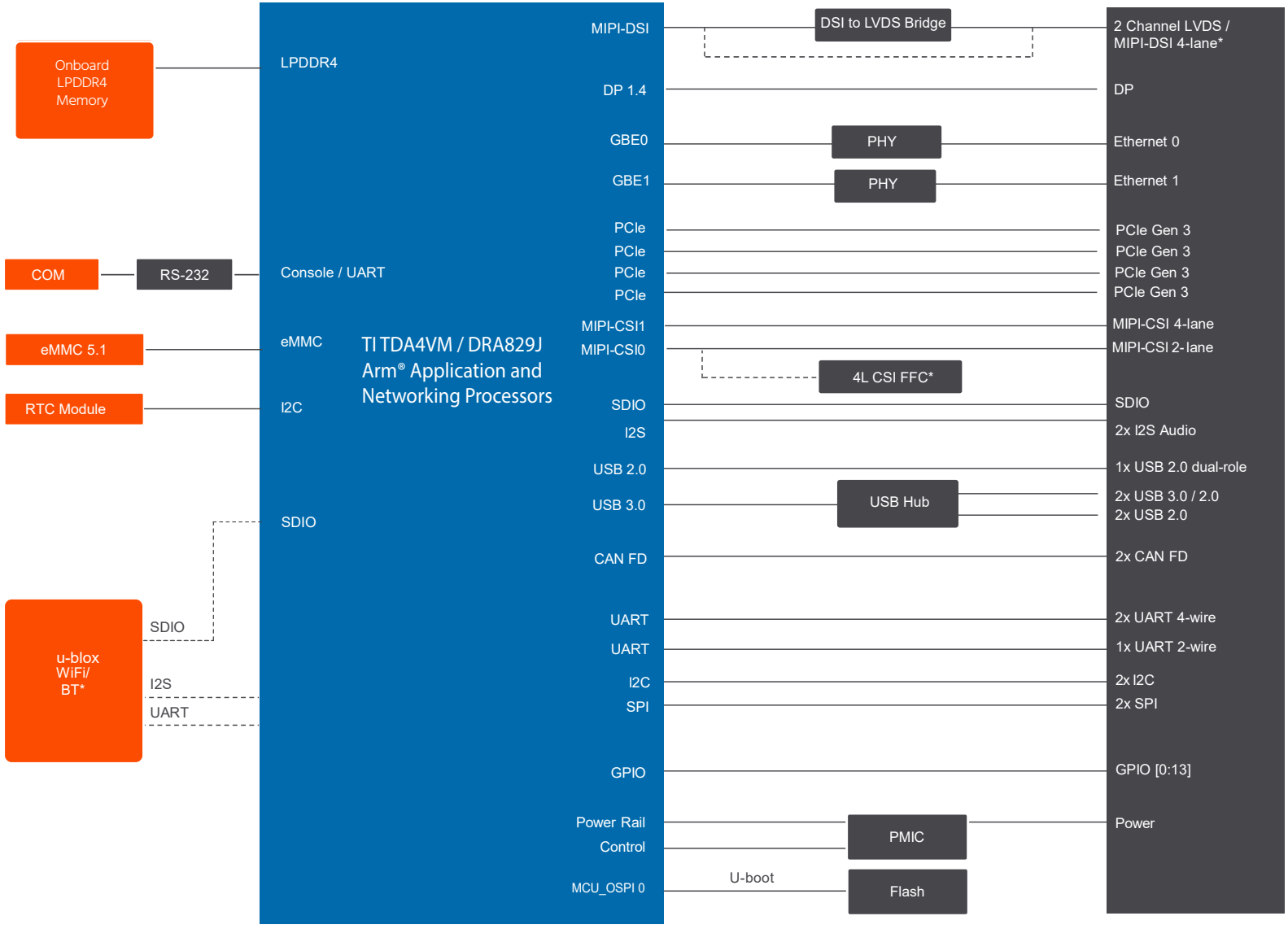
2.8.1 Module

For long-term storage of the conga-STDA4 (more than six months), keep the conga-STDA4 in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

Note

We do not recommend storing the conga-STDA4 for more than five years under these conditions.

3 Block Diagram



* Assembly Option

4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-STDA4 variants. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

Cooling Solution	PN	Description
CSP	051550	Passive cooling solution for SMARC 2.2 module conga-STDA4, 20.1 mm height. For modules with lidded TI Jacinto® 7 ARM processor. All standoffs are with 2.7mm bore hole.
HSP	051551	Heat spreader solution for SMARC 2.2 module conga-STDA4, 6mm height. For modules with lidded TI Jacinto® 7 ARM processor. All standoffs are with 2.7mm bore hole.

Caution

1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

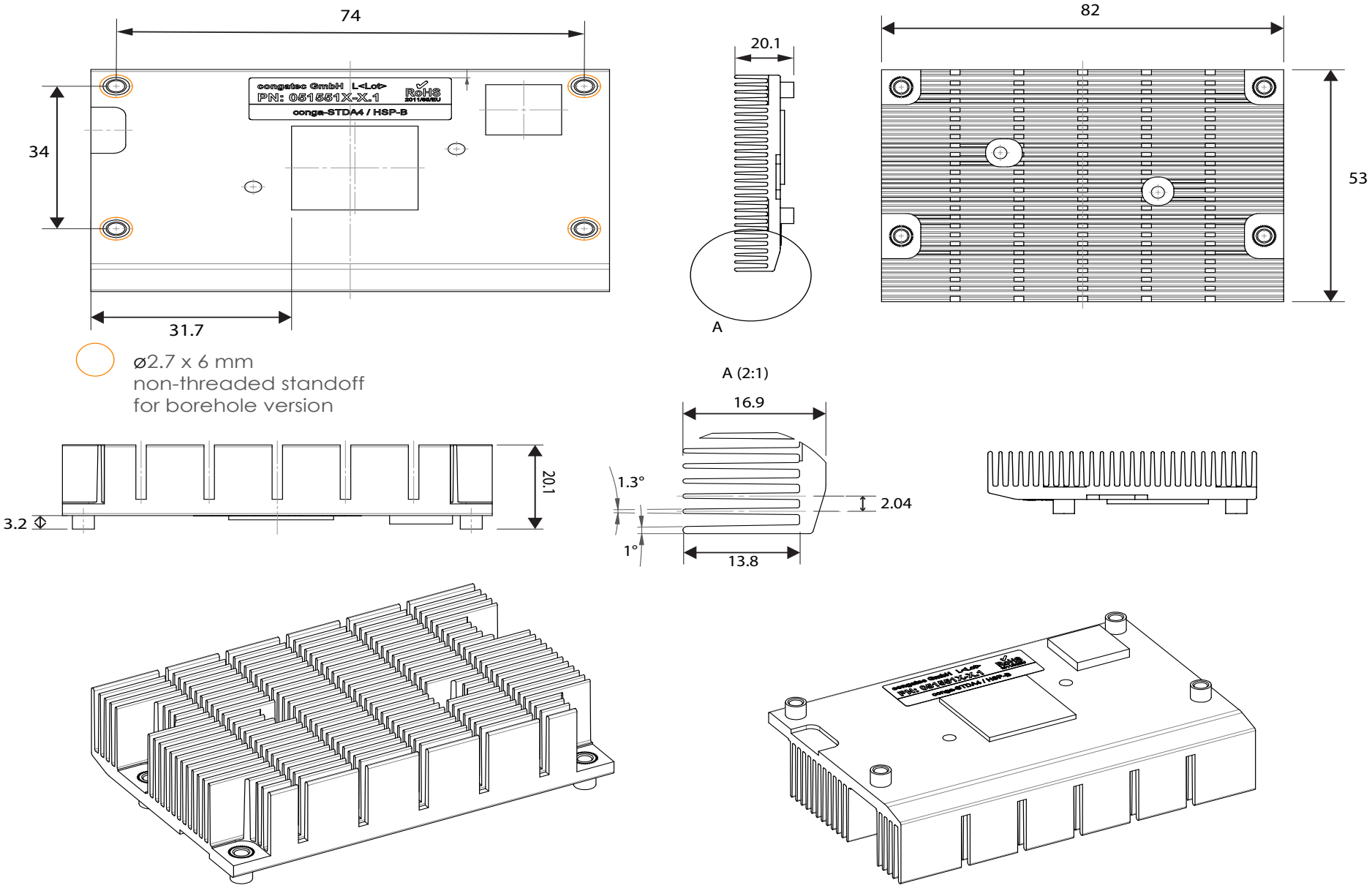
Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board and module mounting screws.*

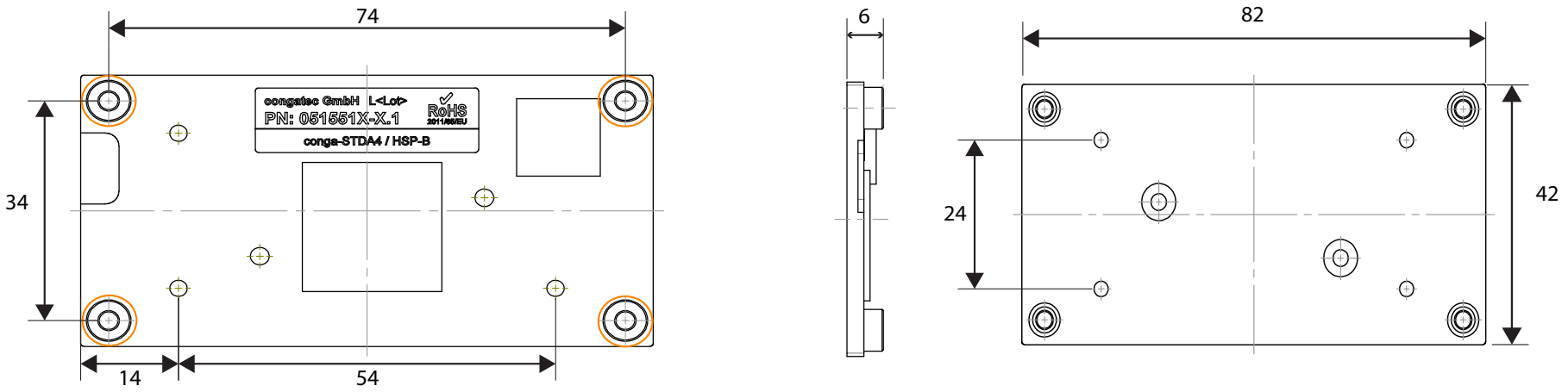
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

3. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

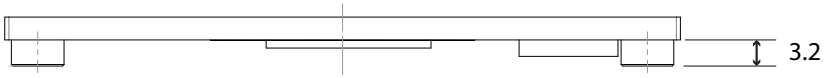
4.1 CSP Dimensions

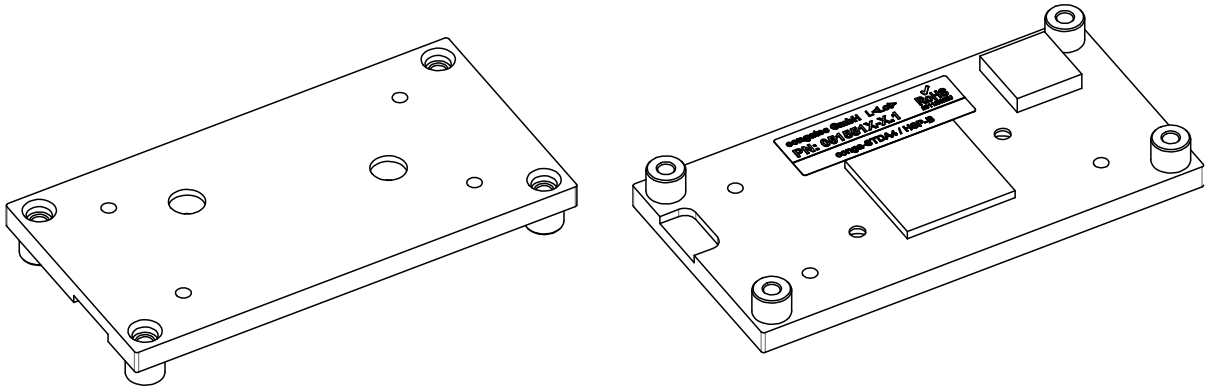


4.2 HSP Dimensions



ø2.7 x 6 mm
non-threaded standoff
for borehole version





5 Connector Rows

The conga-STDA4 has 314 edge fingers that mate with the MXM3 connector located on the carrier board. This connector is able to interface the signals of the conga-STDA4 with the carrier board peripherals.

5.1 Display Interfaces

The conga-STDA4 supports two display interfaces: LVDS/DSI and DP (DisplayPort).

5.1.1 LVDS/DSI

The conga-STDA4 offers one 24-bit dual channel LVDS display over the LVDS[0:1] pins. SN65DSI84 DSI to LVDS bridge enables the LVDS support through DSI interface of the CPU and supports resolutions up to 1920x1200p60.

Alternatively, the DSI interface can directly be connected to the SMARC DSI0 port as an assembly option.

Note

1. *Support for multiple LVDS resolutions from 640x480 to 1920x1080 has been tested by congatec.*
2. *LVDS support is disabled in default software and congatec can provide new *.dts file for specific LCD resolution upon request.*
3. *It is advised to check the pixel clock information provided by congatec to evaluate the suitability for an LVDS panel due to possible accuracy limitations.*

5.1.2 DisplayPort (DP)

The conga-STDA4 offers DP 1.3 support directly through CPU and supports resolutions up to 4096x2160p60. conga-STDA4 also supports up to 4 individual video streams of 1920x1080p60 (1080p/Full HD) and one audio stream through DisplayPort MST (Multi-Stream Transport).

5.2 Camera Inteface (MIPI® CSI)

The conga-STDA4 supports 2 MIPI CSI ports CSI0 and CSI1. CSI0 supports 2 lanes and CSI1 supports 4 lanes. Altogether, the conga-STDA4 allows 2 cameras to be directly connected to CSI ports and supports a bitrate of up to 2.5 Gbps per lane.

Optionally, the on-module Basler BCON interface which shall be used with Basler MIPI or other compatible camera can be used in place of

CSI0, disconnecting it from the SMARC connector. CSI0 supports 4 lanes via a Hirose FH41 series (FFC) connector. However, as of March 2025, Basler does not provide SW support for TI processors and according to the official statement of Basler, they have no plans to create SW support for TI as of now.

Note

1. *Single CSI port can accept multiple video streams (multiple cameras), but requires an aggregator bridge or a de-serializer hub. Detailed instructions are provided at: https://www.ti.com/lit/an/spracx9/spracx9.pdf.*
2. *The connector provides 5V power for a camera (max 500 mA), sourced from the SMARC power input via a power switch.*
3. *USB cameras can be used over the USB port.*

5.3 SDIO Card (4-bit) Interface

The conga-STDA4 offers SDIO pins for one SD/SDIO card interface (4-bit). This interface:

- Is connected through MMC1 interface on CPU.
- Complies with SDIO specification 3.0, SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01
- Support up to UHS-I @SDR 104 or DDR50 [1]
- Is used as the backup boot mode in case the primary boot mode fails [2,3]

Note

1. *congatec has only tested and verified SDIO speeds SDR50 and DDR50 (due to the limitations explained on TI errata i2312). Support for other SDIO speeds has not been tested. HS400 is not supported due to the limitations of TI errata i2024.*
2. *The backup boot mode is fixed as the SD card and cannot be modified via the SMARC Boot Select pins. If booting from another source is required, it can be done through a BOM change (assembly option).*
3. *SD card can also be used as the primary boot mode via the SMARC boot select pins.*

5.4 SPI

The conga-STDA4 uses 3 SPI interfaces: on-module SPI Flash and SMARC SPI[0:1]. All SPI interfaces support the standard SPI mode (SPI 1/1/1). The on-module SPI Flash is reserved for primary boot and contains U-Boot. conga-STDA4 does not support eSPI.

Table 10 SPI Interfaces

Connector Pin	Note
SMARC SPI0	CPU Main domain
SMARC SPI1 / QSPI	MCU domain (MCU_OSPI1_CLK has PD 100k according to TI recommendation)

Note

1. *congatec has observed spurious DMA interrupts when dual or quad mode is used for an SPI interface.*
2. *congatec recommends 25MHz or lower SPI clock frequencies for reliable operation.*
3. *In the default configuration, no pull-up resistors have been added on CS signals for SMARC SPI0 and SMARC SPI1/QSPI.*

5.5 Audio (I2S)

The conga-STDA4 uses 3 McASP (Multichannel Audio Serial Port) ports.

- 2 ports are connected to I2S interfaces on SMARC (I2S0 and I2S2)
- 1 port is connected to optional Wi-Fi module (Bluetooth audio support)

5.6 I2C Interfaces

The conga-STDA4 supports up to 9 I2C buses. 5 ports are connected to CPU Main domain (I2C0 to I2C5), 3 ports are located in the MCU domain (MCU_I2C0, MCU_I2C1, WKUP_I2C0).

Table 11 I2C Interfaces

I2C Port on CPU	Connector Pin	Notes
I2C0	SMARC I2C CSI0	
I2C1	SMARC I2C CSI1	
I2C2	SMARC I2C GP	
I2C3	EEPROM & Temp. sensors	EEPROM is used for board ID and manufacturing data, and is write-protected by default
I2C4	SMARC I2C LCD	
I2C5	DSI to LVDS bridge	
MCU_I2C0	PMIC	Reserved to PMIC driver (SW), not accessible as other I2C ports

I2C Port on CPU	Connector Pin	Notes
MCU_I2C1	SMARC I2C PM	
WKUP_I2C0	PMIC & RTC	Reserved to PMIC and RTC driver (SW), not accessible as other I2C ports

Note

1. *All I2C ports have 2k2 pull-up resistors to 1.8V.*
2. *I2C3 can optionally be connected to SMARC I2C PM if I2C from main domain is required there, it is an assembly option with BOM change.*
3. *I2C EEPROM typically stores board ID information, DRAM size, MAC addresses and other information such as customer information if requested.*

5.7 Serial Ports

The conga-STDA4 offers SER[0:3] pins as 4 serial ports (UART) on SMARC interface by default. Each port supports programmable baud rates of up to 3.6 Mbps. SER0 and SER2 support handshaking / flow control (RTS, CTS).

Additionally two RS232 ports are available on onboard connector, it is primary used for console and debug purposes. For RS232 ports, congatec has tested with 115200 baud rate, although higher baud rates might be possible depending on the transmitter load, it has not been tested and verified. Further information and pinout table can be found in the section 6.9.1 “Console and MCU Debugging”.

SER[0:3] pins are connected to CPU Main domain. SER3 can optionally be connected to WKUP_UART which is in MCU domain (assembly option / BOM change).

If Wi-Fi module is available, an additional UART port is connected to the Wi-Fi module (Bluetooth support).

Note

congatec does not use DMA mode for serial ports. If DMA mode is used, it is strongly advised to implement a retry mechanism for reliable data transfer, because data loss has been observed with DMA mode at high processor loads.

5.8 CAN Bus

The conga-STDA4 offers CAN[0:1] pins for two CAN buses by default. CAN ports support classic CAN or CAN FD (CAN with Flexible Data-Rate) and conform with CAN Protocol version 2.0 part A, B and ISO 11898-1:2015.

Optionally, the CAN[0:1] pins can be connected to the MCU domain (assembly option / BOM change).

5.9 USB Interfaces

The conga-STDA4 offers pins for five USB ports by default. The USB[1:4] pins are provided via a TI TUSB8041 USB 3.0 hub.

USB0 is directly routed to the SoC and it can support dual role mode (Host or Client mode). USB0 is also used as USB DFU boot source (USB0 as primary boot source), if the Force Recovery function is activated.

USB2 and 3 on SMARC support USB 3.0 with up to 5 Gb/s. USB5 on SMARC is not supported.

The table below shows the default and optional USB combinations. All options are assembly options (BOM change).

Table 12 USB Combination

SMARC Port	Default	Assembly Option (Without USB Hub)
USB0	USB 2.0	USB 2.0
USB1	USB 2.0	N/A
USB2	USB 3.0	N/A
USB3	USB 3.0	USB 3.0
USB4	USB 2.0	N/A

5.10 PCI Express

The conga-STDA4 offers support up to 3 PCI Express ports by default and supports speeds up to PCIe Gen 3. The table below shows the default and optional PCIe combination which is an assembly option (BOM change).

Table 13 PCIe Configuration Options

SMARC Port	Default	Alternative Configuration
PCIe A	X1	X2
PCIe B	X1	
PCIe C	X2	X2
PCIe D		

Note

1. *PCIe clock may exceed RMS jitter limit as a result of the limitations explained on Errata i2238 of TI.*

2. *PCIe X2 ports can operate as X1, if only the PCIe A lane or PCIe C lane is connected.*

3. *Only the default setup has been tested and verified.*

4. *CLKREQ signals have on-module pull-up resistors (3.3V), therefore the carrier board only drives the signals to GND (active low inputs on module).*

5.11 Ethernet

The conga-STDA4 offers GbE[0:1] pins for two Gigabit Ethernet interfaces via two onboard TI DP83867 Physical Layers (PHYs) with support for IEEE 1588, 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols, Time Sensitive Network (TSN).

The conga-STDA4 routes MDIO signals via the SMARC interface to support external devices on SERDES (SGMII) ports when PCIe C and D are used in alternate (e.g., Ethernet) modes. However, congatec does not test or validate the functionality of SGMII devices managed through the MDIO interface on conga-STDA4.

Note

1. *GbE0 on SMARC is connected to the MCU domain (MCU_RGMII1) and can optionally be connected to the Main domain (RGMII1) through an assembly option (BOM change), but Ethernet boot is supported only via GbE0 when it is connected to the MCU domain.*

2. *GbE1 on SMARC is connected to the Main domain (RGMII2), and if GbE0 is switched to the Main domain, GbE0 and GbE1 ports are not fully independent as RGMII1 and RGMII2 are connected to an Ethernet switch inside the CPU.*

3. *GbE SDP pins on the SMARC interface are connected to the PHY devices (specifically the GPIO0 pin on the PHY). These PHY devices support only the Start of Frame (SFD) functionality, and not the complete IEEE 1588 stack.*

5.12 GPIO

The conga-STDA4 offers GPIO[0:13] pins for fourteen GPIOs as defined in the SMARC Hardware Specification 2.2.

GPIO[0:3] pins are typically used for Cameras (power enable and reset).

GPIO[5:6] pins are typically used for FAN control (PWM output and TACHO input) but a function is not implemented in software (SW).

GPIO[6:13] can optionally be connected to ADC (Analog-to-Digital Converter, 12-bit) modules inside the CPU. GPIO[6:9] can be connected to module 0 and GPIO[10:13] to module 1. It is important to note that this is an assembly option requiring BOM change and this configuration has not been tested by congatec. It is available upon request only.

Note

GPIO signals do not have a termination by default, a termination (pull-up or pull-down) can be enabled at the CPU pin (during boot up) or a pull-up to 1.8V can be added on request (assembly option / BOM change). Alternatively, a weak pull-down can be included on the carrier board.

5.13 Boot Select

BOOT_SEL[0:2]#

The primary boot source can be selected via the SMARC connector pins BOOT_SEL[0:2]# as described in the table below: [1]

Table 14 Boot Select Options

BOOT_SEL			Force Recovery (USB boot)	Selected Boot Source
0#	1#	2#		
VCC	VCC	Any	VCC	On-module SPI flash (default) [2]
Ground	Ground	Any	VCC	SD card
VCC	Ground	Any	VCC	GbE0
Ground	VCC	Ground	VCC	eMMC on module - File-system mode
Ground	VCC	VCC	VCC	eMMC on module - Boot Partition mode
Any	Any	Any	Ground	DFU mode (from USB0)

Note

1. *The available boot sources and their selection via BOOT_SEL[0:2]# pins corresponds with the boot mode options and configuration pins defined for conga-STDA4 rev. A.0 and later. The table deviates from the SMARC 2.2 specification and shall take precedence over it.*

2. *SD card boot uses File-system mode, the Raw mode option is not supported.*

3. *Under VCC, signal is driven by pull-up resistor on the conga-STDA4. A carrier board shall use OD (open drain) output or a DIP switch only.*

4. *If the set primary boot mode fails, the processor boots from the SD card as it is the fixed backup boot mode for conga-STDA4.*

5. *The Serial Download Mode can also be selected via the FORCE_RECOV# pin. For normal operation, ensure this pin is not low.*

The OS boot device is defined via the U-Boot environment variables. For more information, refer to the conga-STDA4 online software documentation at https://wiki.congatec.com.

FORCE_RECOV#

Low on the FORCE_RECOV# pin enables the Serial Download Mode regardless of the selected boot source via the BOOT_SEL[0:2]# pins. For normal operation, ensure this pin is not low. The program image can be downloaded over the USB0 port (see section 5.9 “USB Interfaces”).

5.14 Power Control

The module operates within an input voltage range of 5 V. The power-up sequence is described below:

1. The carrier board provides the input voltage (VDD_IN) to the module.
2. If VIN_PWR_BAD# is not driven low, the module enables its power circuits.
3. After the first VIN power on, the module starts the power-up sequence (pressing the power button is not required).
4. The module enables the carrier board power by asserting CARRIER_PWR_ON (SUS_S5#) and CARRIER_STBY# (SUS_S3#).
5. The module releases processor reset inputs, starts the boot process and releases RESET_OUT# signal.

The power control signals are described below:

VIN_PWR_BAD#

VIN_PWR_BAD# (pin S150) is an active-low input signal. It indicates that the input voltage to the module is either not ready or out of specified range. Carrier board hardware should drive this signal low until the input power is up and stable. Releasing VIN_PWR_BAD# too early can cause numerous boot up problems. The signal is pulled to approx. 4 V via divider 20k pull-up resistor to VDD_IN and 100k pull-down resistor.

CARRIER_PWR_ON

CARRIER_PWR_ON (pin S154) is an active-high output signal. The module asserts this signal to enable power supplies for devices connected to the carrier board.

CARRIER_STBY#

The CARRIER_STBY# signal (pin S153) is an active-low output that can be used to indicate that the module is going into suspend state, where the A53 core power is turned off.

RESET_IN#

The RESET_IN# signal (pin P127) is an active-low input signal from the carrier board. The signal may be used to force the module to warm reset (POR processor inputs/outputs are not asserted).

RESET_OUT#

The RESET_OUT# signal (pin P126) is an active-low output signal from the module. The output is driven by TI processor via signals RESETSTAT# and MCU_RESETSTAT#.

POWER_BTN#

The POWER_BTN# (pin P128) is an active-low power button input from the carrier board. This power button signal is used to wake the system. Driving this signal low for at least 5 seconds powers off the system immediately (forced shutdown).

Note

Since TI does not support any suspend modes, CARRIER_STBY# and CARRIER_PWR_ON functions similarly.

Power Supply Implementation Guidelines

The operational power source for the conga-STDA4 is 5V. The remaining necessary voltages are internally generated on the module with onboard voltage regulators.

Inrush and Maximum Current Peaks on VDD_IN

The maximum peak-current on the conga-STDA4 VDD_IN (5 V) power rail can be as high as 2.7 A. You should therefore ensure the power supply and decoupling capacitors provide enough power to drive the module.

Note

1. *As the VDD_IN is applied, TI PMIC enables OVP protection using FET which may generate high inrush currents, typically up to 2 A. PSU must be capable of catering such high current demands if a standby voltage rail is used to power-up the module.*

2. *For more information about power control event signals, refer to the SMARC® 2.2 specification.*

6 Onboard Interfaces and Devices

6.1 DRAM

The conga-STDA4 offers up to 8 GB 32 bit LPDDR4 onboard SDRAM @ 2133 MHz. The memory size of each conga-STDA4 variant is listed in section 1.2.1 "Options Information".

Note

1. *Inline Error Correcting Code (ECC) support is optional and can be enabled via software configuration. When enabled, ECC implementation consumes 1/8 of the total memory space.*

2. *When image processing with edge AI is required, a minimum of 4GB of RAM is recommended based on congatec's experience, which indicates that 2GB of RAM may be insufficient for optimal performance in such applications.*

6.2 eMMC

The conga-STDA4 offers an onboard eMMC 5.1 storage device from Micron with up to 128 GB (32 GB assembled by default) capacity and 4MB boot partition which can be used for UBOOT. Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology. The performance of the newer eMMC may vary depending on the eMMC technology.

Note

1. *congatec uses DDR52 for eMMC. The proper functioning with HS200 and SDR104 for MMCSD are not guaranteed due to the limitations explained in errata i2312.*

1. *For adequate operation of the eMMC, ensure that at least 15% of the eMMC storage is reserved for vendor-specific functions.*

2. *conga-STDA4 can be configured to boot up from eMMC (see "5.13 Boot Select" on page 29 above).*

3. *According to Micron, the eMMC chip features a PE cycle limit of 3000 cycles (40000 with pSLC enabled) and data retention up to 10 years (at 55°C and 10% of PE limit).*

6.3 SPI Flash

The conga-STDA4 offers an onboard SPI flash memory connected thorugh MCU_OSPI0 interface and is primarily used for UBOOT (primary boot device).

conga-STDA4 uses Winbond SPI Flash with BGA package, which offers 128Mbit for standard variants but Winbond offers options up to 2Gbit. In case of conga-STDA4, OSPI (8-bit, octal SPI) is not supported, only the support for standard SPI mode (SPI 1/1/1) has been verified [1].

Note

1. *congatec has observed spurious DMA interrupts when dual or quad mode is used for an SPI interface.*

6.4 Wi-Fi and Bluetooth

The conga-STDA4 can offer Wi-Fi and Bluetooth connectivity via an optional onboard u-blox MAYA-W260 module connected through MMC, UART and McASP ports (assembly option).[1]

MAYA-W260 module supports:

- Dual-band Wi-Fi 6 (802.11a/b/g/n/ac/ax), 2.4 and 5GHz
- Wi-Fi security (WPA3, WPA2, WAPI, AES)
- Bluetooth 5.4
- U.FL connectors
- Industrial grade conditions (-40 to +85°C)

Note

1. *PN: 051520 offers Wi-Fi/BT by default.*

6.5 RTC

The conga-STDA4 offers a discrete Real-Time Clock (RTC) via an onboard MicroCrystal RV-4162-C7 module with the I²C device address 0xD0.

If SMARC main power (VDD_IN) is not available, the RTC is powered by the VDD_RTC. conga-STDA4 supports a coin cell battery or a supercap for VDD_RTC.

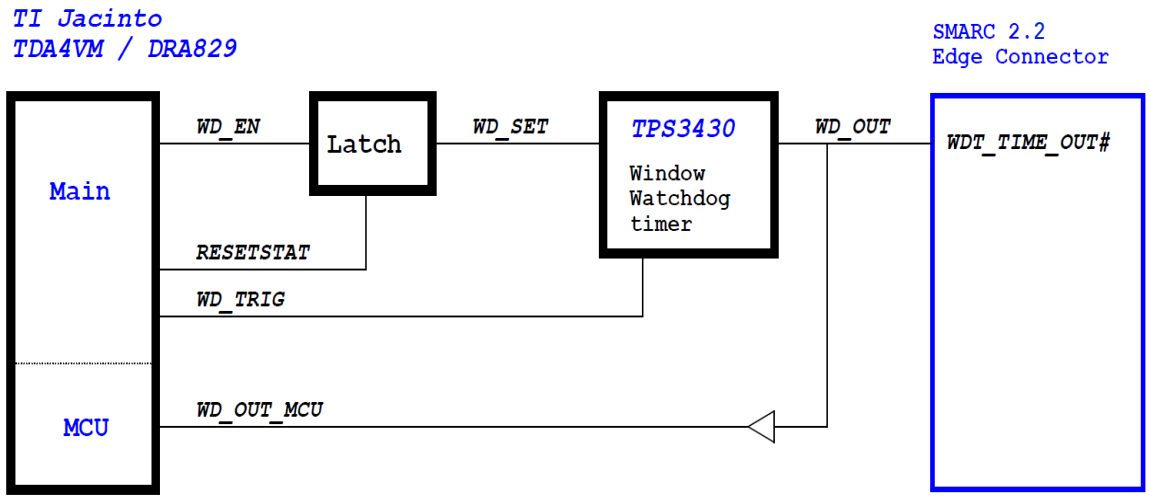
Note

1. *Current flows from module to the supercap via a 240Ω resistor.*
2. *If coin cell battery is used, it must be protected by a diode on the carrier board*

6.6 Watchdog (WD)

The conga-STDA4 offers multiple Watchdog (WD) solutions:

1. CPU Internal Watchdog Timers
   - SW can activate internal WDs supported by the CPU.
2. PMIC (TPS6594) Watchdog
   - The PMIC supports both monitoring and watchdog functionality.
3. Onboard Watchdog Chip (TPS3430)
   - Controlled by CPU through GPIO pins.
   - WD output (WD_OUT) is connected to the SMARC interface and handled by the carrier board.
   - conga-STDA4 does not perform self-recovery on WD trigger; it signals the carrier board for appropriate response.



The TPS3430-based Watchdog has following behavior:

- Activation
  - After system boot, software enables the watchdog by asserting WD_EN.
  - Once enabled, the watchdog cannot be disabled via software due to a hardware latch.

  - WD_EN is an active-high signal with an on-module pull-down resistor.
- *Feeding the Watchdog*
  - The CPU feeds the watchdog via WD_TRIG, which triggers on a falling edge.
  - WD_TRIG has an on-module pull-up resistor.
  - Feeding must occur within a fixed time window (non-configurable without BOM change):

    Upper boundary: 225 ms ± 20% (180 - 270 ms)

    Lower boundary: 28 ms ± 20% (22.5 - 33.7 ms)
  - conga-STDA4 is designed for a ~100 ms trigger rate.
- Failure Handling
  - If feeding occurs outside the allowed time window, WD_OUT is asserted for 10ms and it repeats until trigger is back inside the time window.
  - This output is routed to the carrier board for recovery handling.
  - WD_OUT_MCU is connected to a GPIO in the MCU domain but does not trigger an automatic reset of the module (signal is optional and not mandatory to use).
- System Reset Behavior
  - A system reset deactivates the watchdog (RESETSTAT).
  - Software must re-enable the watchdog after boot-up.

6.7 Temperature Monitoring

conga-STDA4 features temperature sensors inside the CPU and two additional temperature sensors on-board connected with the I2C3 interface. One of these sensors is located on the top side next to the DDR and CPU, and the other sensor is placed on the bottom side at the board edge.

6.8 System Control, Battery, and Charging Interfaces

The conga-STDA4 provides a set of System Control and Battery Management signals through the SMARC module interface. These signals are designed to support standard power control functions as well as battery-powered system management features.

6.8.1 Buttons and Lid Switch

Table 15 Buttons and Control Signals

Signal	Description	Comments
PWR_BTN#	Power button	Supported and connected to PMIC and is activated after the first power up.
RESET_IN#	Reset button	Supported and connected to warm reset inputs, does not trigger POR reset inputs.
SLEEP#	Sleep button	Connected to PMIC and CPU (GPIO), but function is not implemented in SW as a sleep state is currently not supported by TI.
LID#	Lid switch	Connected to CPU (GPIO), but function is not implemented in SW.

Note

These signals have on-module pull-up resistors (1.8V) and should be driven by button/switch or OD output (open drain / collector) on the carrier board.

6.8.2 Battery and Charging Signals

BATLOW#, TEST#, CHARGING# and CHARGING_PRSTN# signals are connected directly to the CPU (GPIO pins), but a function is not implemented in SW.

Note

These signals have on-module pull-up resistors (1.8V) and should be driven by button/switch or OD output (open drain / collector) on the carrier board.

6.9 Console and Debug Interfaces

6.9.1 Console and MCU Debugging

The conga-STDA4 is equipped with a 6-pin Molex PicoBlade connector that provides two serial interfaces with RS-232 voltage levels (TX and RX only). The primary console interface is UART0 from the CPU and the secondary (auxiliary) interface is connected to MCU_UART0 and is intended for MCU debugging purposes. The baud rate for console port is 115200. The connector pinout is described in the table below.

Table 16 Serial Console Connector (X1) Pinout Description

Pin	Signal	Description
1	COM1 TX	Auxiliary MCU/debug serial port output (RS232)
2	+VIN	Auxiliary power output (5V), connected to SMARC power input, max 500mA is recommended

Pin	Signal	Description
3	GND	Reference Ground
4	COM2 TX	Console RS232 output
5	COM2 RX	Console RS232 input
6	COM1 RX	Auxiliary MCU/debug serial port input (RS232)

Connector Type

X1: Molex PicoBlade 0532610671 (6 Circuits, 1.25mm Pitch, Right-Angle, Friction Lock)
Mates with Molex PicoBlade Cable Assembly Series 15134 with 6 Circuits.

6.9.2 JTAG Debug

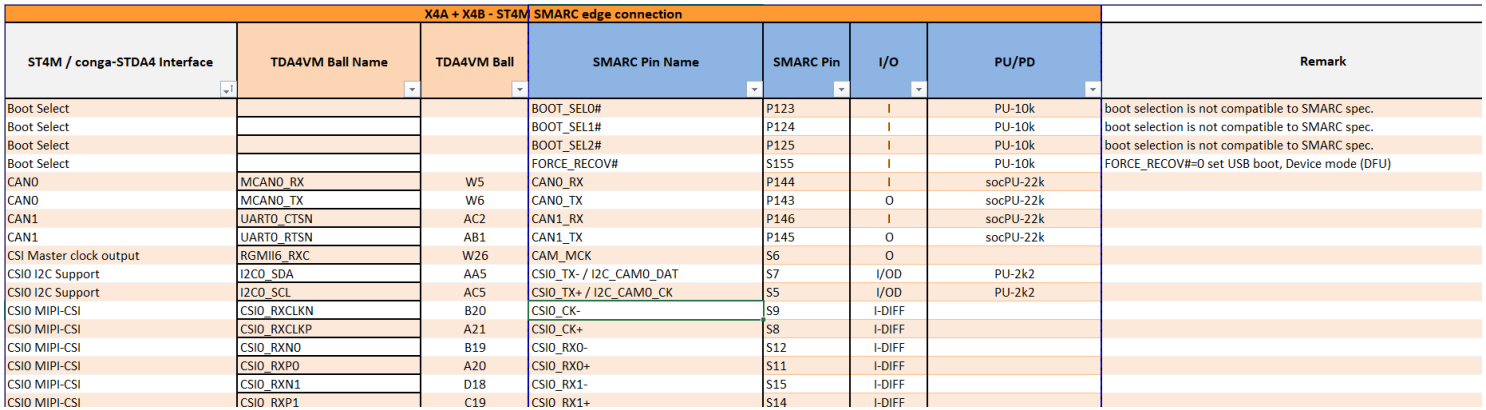
The conga-STDA4 offers access to the onboard JTAG interface via test points which are placed on the bottom side edge of the PCB.

Note

The JTAG signals are 1.8V.

7 Signal Descriptions and Pinout Tables

Click on the screenshot or link below to directly download the conga-STDA4 pinout as an Excel file:



X4A + X4B - ST4M SMARC edge connection							
ST4M / conga-STDA4 Interface	TDA4VM Ball Name	TDA4VM Ball	SMARC Pin Name	SMARC Pin	I/O	PU/PD	Remark
Boot Select			BOOT_SEL0#	P123	I	PU-10k	boot selection is not compatible to SMARC spec.
Boot Select			BOOT_SEL1#	P124	I	PU-10k	boot selection is not compatible to SMARC spec.
Boot Select			BOOT_SEL2#	P125	I	PU-10k	boot selection is not compatible to SMARC spec.
Boot Select			FORCE_RECOV#	S155	I	PU-10k	FORCE_RECOV#=0 set USB boot, Device mode (DFU)
CAN0	MCAN0_RX	W5	CAN0_RX	P144	I	socPU-22k	
CAN0	MCAN0_TX	W6	CAN0_TX	P143	O	socPU-22k	
CAN1	UART0_CTSN	AC2	CAN1_RX	P146	I	socPU-22k	
CAN1	UART0_RTSN	AB1	CAN1_TX	P145	O	socPU-22k	
CSI Master clock output	RGMII6_RXC	W26	CAM_MCK	S6	O		
CSI0 I2C Support	I2C0_SDA	AA5	CSI0_TX- / I2C_CAM0_DAT	S7	I/OD	PU-2k2	
CSI0 I2C Support	I2C0_SCL	AC5	CSI0_TX+ / I2C_CAM0_CK	S5	I/OD	PU-2k2	
CSI0 MIPI-CSI	CSI0_RXCLKN	B20	CSI0_CK-	S9	I-DIFF		
CSI0 MIPI-CSI	CSI0_RXCLKP	A21	CSI0_CK+	S8	I-DIFF		
CSI0 MIPI-CSI	CSI0_RXN0	B19	CSI0_RX0-	S12	I-DIFF		
CSI0 MIPI-CSI	CSI0_RXP0	A20	CSI0_RX0+	S11	I-DIFF		
CSI0 MIPI-CSI	CSI0_RXN1	D18	CSI0_RX1-	S15	I-DIFF		
CSI0 MIPI-CSI	CSI0_RXP1	C19	CSI0_RX1+	S14	I-DIFF		

https://git.congatec.com/arm-ti/jacinto-family-ea/doc/cgtj721e_pinlist/-/blob/cgtst4m_pinlist/cgtst4m_pin_connection.xlsx?ref_type=heads

Alternatively, you can find the conga-STDA4 pinout by selecting it from the drop-down list at:

https://git.congatec.com/arm-ti/jacinto-family-ea/doc/cgtj721e_pinlist/tree/main

The SMARC signals are described in the SMARC 2.2 Hardware Specification publicly available at:

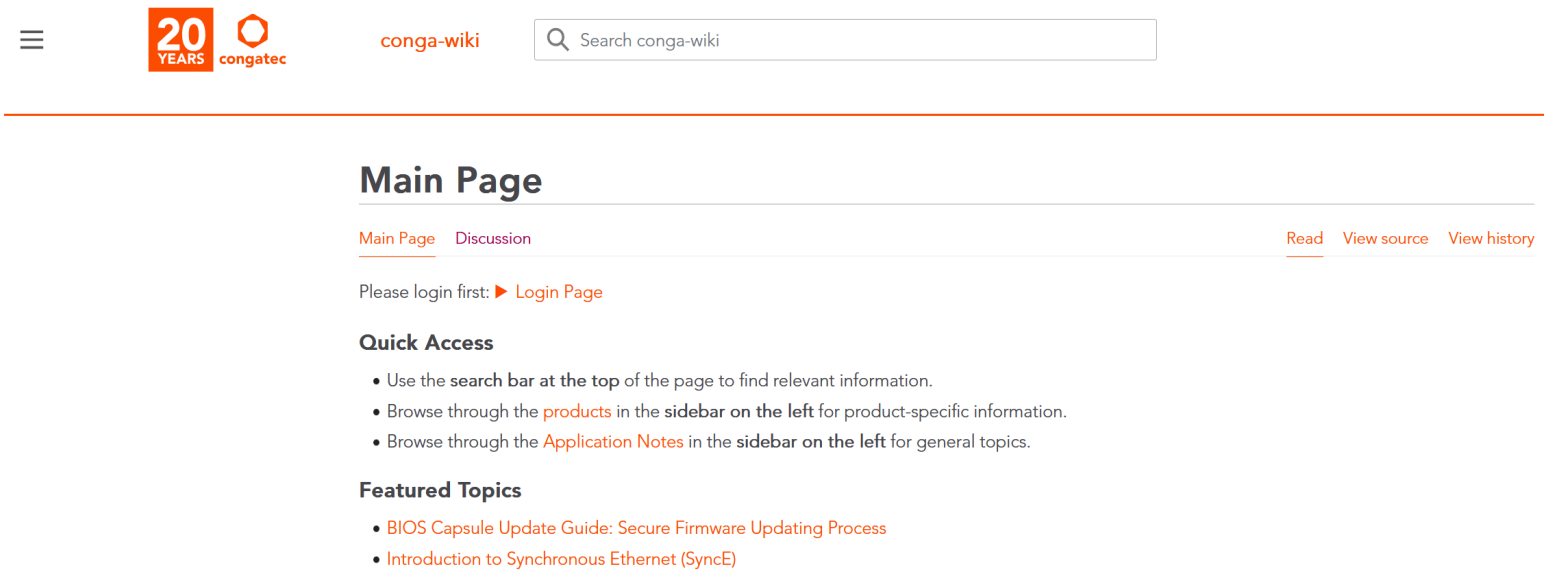
https://sget.org

The SoC documentation is available at:

https://www.ti.com

8 Software Documentation

Click on the screenshot or link below to open the conga-STDA4 software documentation in your browser:



https://wiki.congatec.com/wiki/Category:Conga-STDA4

Alternatively, you can find the conga-STDA4 software documentation by selecting it from the navigation menu at:

https://wiki.congatec.com