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# XTX™ conga-XAF

***AMD® Embedded G-Series processors and AMD A55E controller hub***

***User's Guide***

***Revision 1.5***

# Revision History

| Revision | Date (yyyy.mm.dd) | Author | Changes |
|---|---|---|---|
| 1.0 | 2011.07.29 | GDA | Official release |
| 1.1 | 2011.08.09 | GDA | Corrected TDP values for AMD G-T40E 1.0 GHz Dual Core and AMD G-T40R 1.0 GHz Single Core conga-XAF in the Options Information table on page 8. |
| 1.2 | 2011.10.19 | GDA | Removed information from section 6.3 about limiting the maximum processor frequency via BIOS setup node, this feature is not available. Added note throughout about Native and Compatible IDE support. Added information about Native and Compatible option in section 6. Updated BIOS section. |
| 1.3 | 2011.10.24 | GDA | Corrected product name in “conga-XAF Options Information” section and in section 6. |
| 1.4 | 2012.07.13 | GDA | Added maximum memory speed to Options Information table and Feature List table 1. Added section 6.8 “HDMI/DisplayPort (DP) Audio Support.“ Updated section 9 'BIOS Setup Description.” |
| 1.5 | 2013.06.11 | AEM | Removed conga-XAF variants with part numbers 041032, 041033 and 041035 from “Options Information”, section 1.1 “Feature List” and section 1.5 “Power Consumption. Changed maximum torque rating for heatspreader screws in section 3.1 “Heatspreader Dimensions” and added a caution statement. Added section 7.9 “Boot Strap Signal”. Updated section 9 “ BIOS setup description”.<br>Added a warning note regarding the flat foil cable in section 7.8 “DDI Connector X6”.<br>Updated section 9 “BIOS Setup Description”. Updated the whole document. |

# Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-XAF. It is one of four documents that should be referred to when designing an XTX™ application. The other reference documents that should be used include the following:

XTX™ Design Guide
XTX™ Specification
ETX® Design Guide

The links to these documents can be found on the congatec AG website at www.congatec.com

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## Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

## Symbols

The following symbols are used in this user's guide:

**Warning**

*Warnings indicate conditions that, if not observed, can cause personal injury.*

**Caution**

*Cautions warn the user about how to prevent damage to hardware or loss of data.*

**Note**

*Notes call attention to important information that should be observed.*

## Terminology

| Term | Description |
|---|---|
| GB | Gigabyte (1,073,741,824 bytes) |
| GHz | Gigahertz (one billion hertz) |
| kB | Kilobyte (1024 bytes) |
| MB | Megabyte (1,048,576 bytes) |
| Mbit | Megabit (1,048,576 bits) |
| kHz | Kilohertz (one thousand hertz) |
| MHz | Megahertz (one million hertz) |
| T.O.M. | Top of memory = max. DRAM installed |
| TDP | Thermal Design Power |
| SATA | Serial ATA |
| PATA | Parallel ATA |
| HDA | High Definition Audio |
| APU | Accelerated Processor Unit |
| CH | Controller Hub |
| I/F | Interface |
| N.C. | Not connected |
| N.A. | Not available |
| TBD | To be determined |

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## ETX® Concept and XTX™ Extension

The ETX® concept is an off the shelf, multi-vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific baseboard. ETX® modules have a standardized form factor of 95mm x 114mm and have specified pinouts on the four system connectors that remain the same regardless of the vendor. The ETX® module provides most of the functional requirements for any application. These functions include, but are not limited to, graphics, sound, keyboard/mouse, IDE, Ethernet, parallel, serial and USB ports. Four ruggedized connectors provide the baseboard interface and carry all the I/O signals to and from the ETX® module.

Baseboard designers can utilize as little or as many of the I/O interfaces as deemed necessary. The baseboard can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly ETX® applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class ETX® modules. Simply unplug one module and replace it with another, no redesign is necessary.

XTX™ is an expansion and continuation of the well-established and highly successful ETX® standard. XTX™ offers the newest I/O technologies on this proven form factor. Now that the ISA bus is being used less and less in modern embedded applications congatec AG offers an array of different features on the X2 connector than those currently found on the ETX® platform. These features include new serial high speed buses such as PCI Express™ and Serial ATA®. All other signals found on connectors X1, X3, and X4 remain the same in accordance to the ETX® standard (Rev. 2.7) and therefore will be completely compatible. If the embedded PC application still requires the ISA bus then an ISA bridge can be implemented on the application specific baseboard or the readily available LPC bus located on the XTX™ module may be used. Contact congatec technical support for details.

## Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

## Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

## conga-XAF Options Information

The conga-XAF is available in four variants. This user's guide describes all of these options. Below you will find an order table showing the different configurations that are currently offered by congatec AG. Check the table for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

| Part-No. | 041031 | 041034 | 041037 | 041036 |
|---|---|---|---|---|
| **CPU** | AMD G-T56N 1.6 GHz Dual Core | AMD G-T52R 1.5 GHz Single Core | AMD G-T40E 1.0 GHz Dual Core | AMD G-T40R 1.0 GHz Single Core |
| **DDR3 Speed** | DDR3-1333 | DDR3-1333 | DDR3-1066 | DDR3-1066 |
| **Cache** | 512kB x 2 | 512kB | 512kB x 2 | 512kB |
| **LVDS** | Yes | Yes | Yes | Yes |
| **Graphic** | Radeon™ HD 6320 | Radeon™ HD 6310 | Radeon™ HD 6250 | Radeon™ HD 6250 |
| **DisplayPort (DP)** | Yes (shared with HDMI) | Yes (shared with HDMI) | Yes (shared with HDMI) | Yes (shared with HDMI) |
| **HDMI** | Yes (shared with DP) | Yes (shared with DP) | Yes (shared with DP) | Yes (shared with DP) |
| **SATA** | x 2 | x 2 | x 2 | x 2 |
| **TDP** | 18W | 18W | 6.4W | 5.5W |
| **Suspend to RAM (S3)** | Yes | Yes | Yes | Yes |

# Contents

# 1 Specifications

## 1.1 Feature List

**Table 1 Feature Summary**

| | |
|---|---|
| **Form Factor** | ETX® standard (Rev. 2.7) with XTX™ extension |
| **Processor** | AMD G-T56N 1.6 GHz Dual Core with L2 cache 512kB x2<br>AMD G-T40E 1.0 GHz Dual Core with L2 cache 512kB x2<br>AMD G-T52R 1.5 GHz Single Core with L2 cache 512kB<br>AMD G-T40R 1.0 GHz Single Core with L2 cache 512kB |
| **Memory** | DDR3 SO-DIMM memory 1333 MT/s (666MHz) and 1066 MT/s (533 MHz) up to 4-GByte |
| **Chipset** | AMD A55E Controller Hub |
| **Audio** | Realtek ALC 262 HDA (High Definition Audio) codec |
| **Ethernet** | Realtek RTL8105E |
| **Graphics Options** | Integrated High Performance Video AMD Radeon™ HD 6310 or AMD Radeon™ HD 6250, DirectX®11 graphics with UVD 3.0, Integrated VGA DAC, Dual Simultaneous Display Support<br>• CRT Interface 400 MHz RAMDAC, Resolutions up to 1920x1200 @ 60Hz (WUXGA)<br>• 2x DisplayPort 1.1a, Resolutions up to 1920x1200, shared with HDMI port provided on flat-foil connector<br>• 2x HDMI 1.3a Port, Resolutions up to 1920x1080, shared with DisplayPort provided on flat-foil connector<br>• 1x DisplayPort/HDMI port is used for LVDS if module supports LVDS<br>• Flat panel Interface (provided by Analogix ANX3110 DisplayPort to LVDS converter)<br>• Single-channel LVDS interface support: 1 x 18 bpp or 1 x 24 bpp<br>• Dual-channel LVDS interface support: 2 x 18 bpp or 2 x 24 bpp panel support VESA standard or JEDIA data mapping<br>• Automatic Panel Detection via EDID/EPI (Embedded Panel Interface based on VESA EDID™ 1.3) Resolutions up to 1900x1200 (WUXGA) @ 60 Hz |
| **Super I/O** | Winbond 83627DHG |
| **Peripheral Interfaces** | • PS/2 Keyboard, Mouse<br>• PCI Bus Rev. 2.3<br>• LPC Bus (no ISA Bus)<br>• 2x EIDE (UDMA-66/100/133)<br>• 4x Serial ATA® Raid support 0,1<br>• 4x x1 PCI Express Links<br>• 6x USB 2.0 (EHCI)<br>• I²C Bus, Fast Mode (400 kHz)<br>• LPT (EEP/ECP)<br>• 2 x COM Ports, TTL Level<br>• 1 x IrDA Port |
| **BIOS** | AMI Aptio® UEFI 2.x firmware, 4MByte serial SPI with congatec Embedded BIOS features |
| **Power Management** | ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3). |

**Note**

*Some of the features mentioned in the Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 8 of this user's guide to determine what options are available on your particular module.*

## 1.2 Supported Operating Systems

The conga-XAF supports the following operating systems.

- Microsoft® Windows® 7 (32 and 64 bit)
- Microsoft® Windows® 7 Embedded
- Microsoft® Windows® XP
- Microsoft® Windows ®XP Embedded
- Linux

**Note**

*The IDE interface on the conga-XAF can only be used in Native IDE mode (no compatible/legacy mode support). This means that any OS that is booted from the IDE interface must support Native IDE mode.*

## 1.3 Mechanical Dimensions

- 95.0 mm x 114.0 mm (3.75” x 4.5”)
- Height approx. 12mm (0.4”)

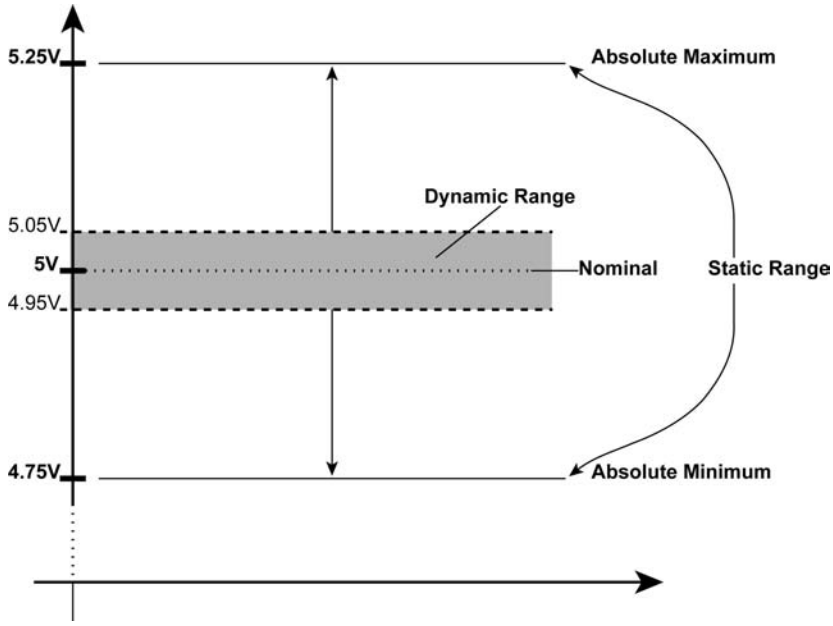
## 1.4 Electrical Characteristics

| Characteristics | | | Min | Typ | Max | Units | Comment |
|---|---|---|---|---|---|---|---|
| 5V | Voltage | +/-5% | 4.75 | 5.00 | 5.25 | Vdc | |
| | Ripple | | - | - | 100 | $mV_{pp}$ | 0-20MHz |
| | Current | See section 1.5 'Power Consumption' for supply current information. | | | | | |
| 5V_SB | Voltage | +/-5% | 4.75 | 5.00 | 5.25 | Vdc | |
| | Current | | | TBD | TBD | mA | S3 status |

### 1.4.1 Supply Voltage Ripple

Maximum 100mV peak to peak over a frequency band of 10Hz to 20MHz.

The dynamic range shall not exceed the static range.




### 1.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

## 1.5 Power Consumption

The power consumption values listed in this document were measured under controlled environment. The XTX module was mounted onto a special baseboard. This special baseboard does not have any power consuming components mounted on it. It provides one connector for a CRT monitor connection, a PS/2 keyboard and mouse connection, and an IDE device connection. The baseboard is powered by a Direct Current (DC) power supply that is set to output 5 Volts and is connected directly to the special baseboard. Additionally, positive and negative sense lines are connected to the baseboard in order to measure the current consumption of the module. This current consumption value is displayed by the DC power supply's readout and this is the value that is recorded as the power consumption measurement. All recorded values are approximate.

All external peripheral devices, such as the hard drive, are externally powered so that they do not influence the power consumption value that is measured for the module. This ensures the value measured reflects the true power consumption of the module and only the module. A keyboard is used to configure the module and then it is

disconnected before the measurement is recorded. If the keyboard remained connected, an additional current consumption of approximately 10 mA is noticed.

Each module was measured while running Windows XP Professional with SP3 (service pack 3) and the “Power Scheme” was set to “Portable/Laptop”. This setting ensures that processor core is running in LFM (lowest frequency mode) with minimal core voltage during desktop idle. Each conga-XAF variant was tested while using a 2GB memory module. Using different sizes of RAM will cause slight variances in the measured results.

**Windows XP Professional SP2**

- Desktop Idle
- 100% CPU workload (see note below)
- Windows XP Professional Standby Mode (requires setup node “Suspend Mode” in the BIOS to be configured to S1 POS (Power On Suspend))
- Suspend to RAM (requires setup node “Suspend Mode” in BIOS to be configured to S3 STR (Suspend to RAM))

**Note**

*A software tool was used to stress the CPU to 100% workload.*

### 1.5.1 conga-XAF AMD G-T56N 1.6 GHz Dual Core

**With 2GB memory installed**

| conga-XAF Article No. 041031 | AMD T56N 1.6 GHz Dual Core L2 cache 512kB x2 40nm Layout Rev. XBRALA0 /BIOS Rev. XBRAR006 | | |
|---|---|---|---|
| Memory Size | 2GB | | |
| Operating System | Windows XP Professional SP3 | | |
| Power State | Desktop Idle | 100% workload | Standby |
| Power consumption (measured in Amperes/Watts) | 1.3 A/6.5 W | 2.8 A/14.0 W | 0.06 A/0.3 W |

### 1.5.2 conga-XAF AMD G-T40E 1.0 GHz Dual Core

**With 2GB memory installed**

| conga-XAF Article No. 041037 | AMD T40E 1.0 GHz Dual Core L2 cache 512kB x2<br>40nm<br>Layout Rev. XBRALA0 /BIOS Rev. XBRAR006 | | |
|---|---|---|---|
| Memory Size | 2GB | | |
| Operating System | Windows XP Professional SP3 | | |
| Power State | Desktop Idle | 100% workload | Standby |
| Power consumption (measured in Amperes/Watts) | TBD A/TBD W | TBD A/TBD W | TBD A/TBD W |

### 1.5.3 conga-XAF AMD G-T52R 1.5 GHz Single Core

**With 2GB memory installed**

| conga-XAF Article No. 041034 | AMD T52R 1.5 GHz Single Core L2 cache 512kB<br>40nm<br>Layout Rev. XBRALA0 /BIOS Rev. XBRAR006 | | |
|---|---|---|---|
| Memory Size | 2GB | | |
| Operating System | Windows XP Professional SP3 | | |
| Power State | Desktop Idle | 100% workload | Standby |
| Power consumption (measured in Amperes/Watts) | 1.3 A/6.5 W | 2.1 A/10.5 W | 0.06 A/0.3 W |

### 1.5.4 conga-XAF AMD G-T40R 1.0 GHz Single Core

**With 2GB memory installed**

| conga-XAF Article No. 041036 | AMD T40R 1.0 GHz Single Core L2 cache 512kB<br>40nm<br>Layout Rev. XBRALA0 /BIOS Rev. XBRAR006 | | |
|---|---|---|---|
| Memory Size | 2GB | | |
| Operating System | Windows XP Professional SP3 | | |
| Power State | Desktop Idle | 100% workload | Standby |
| Power consumption (measured in Amperes/Watts) | TBD A/TBD W | TBD A/TBD W | TBD A/TBD W |

**Note**

*All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.*

## 1.6 Supply Voltage Battery Power

- 2.0V-3.6V DC
- Typical 3V DC

### 1.6.1 CMOS Battery Power Consumption

| RTC @ 20ºC | Voltage | Current |
|---|---|---|
| Integrated in the AMD A55E FCH | 3.0V | 2.04 µA |

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

## 1.7 Environmental Specifications

| | | |
|---|---|---|
| Temperature | Operation: 0° to 60°C | Storage: -20° to +80°C |
| Humidity | Operation: 10% to 90% | Storage: 5% to 95% |

**Caution**

*The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.*

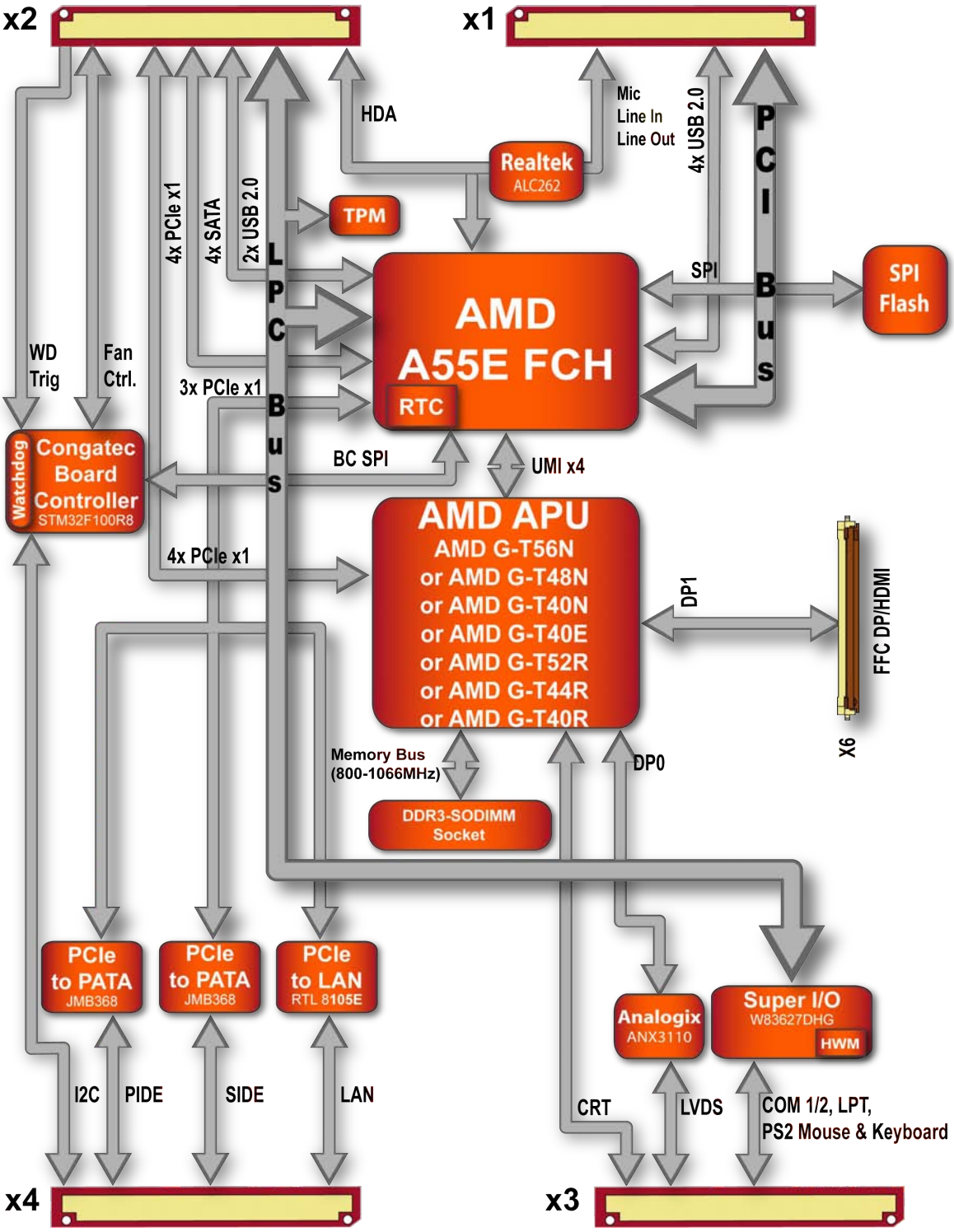
*congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.*

*If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.*

*For more information about operating a congatec module without heatspreader contact congatec technical support.*

*Humidity specifications are for non-condensing conditions.*

# 2 Block Diagram



# 3 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module and its aluminum plate is 2mm thick.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis thereby using the whole chassis as a heat dissipator.

**Caution**

*There are mounting holes on the heatspreader designed to attach the heatspreader to the module. These mounting holes must be used to ensure that all components that are required to make contact with heatspreader do so. Failure to utilize the these mounting holes will result in improper contact between these components and heatspreader thereby reducing heat dissipation efficiency.*

*Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.*

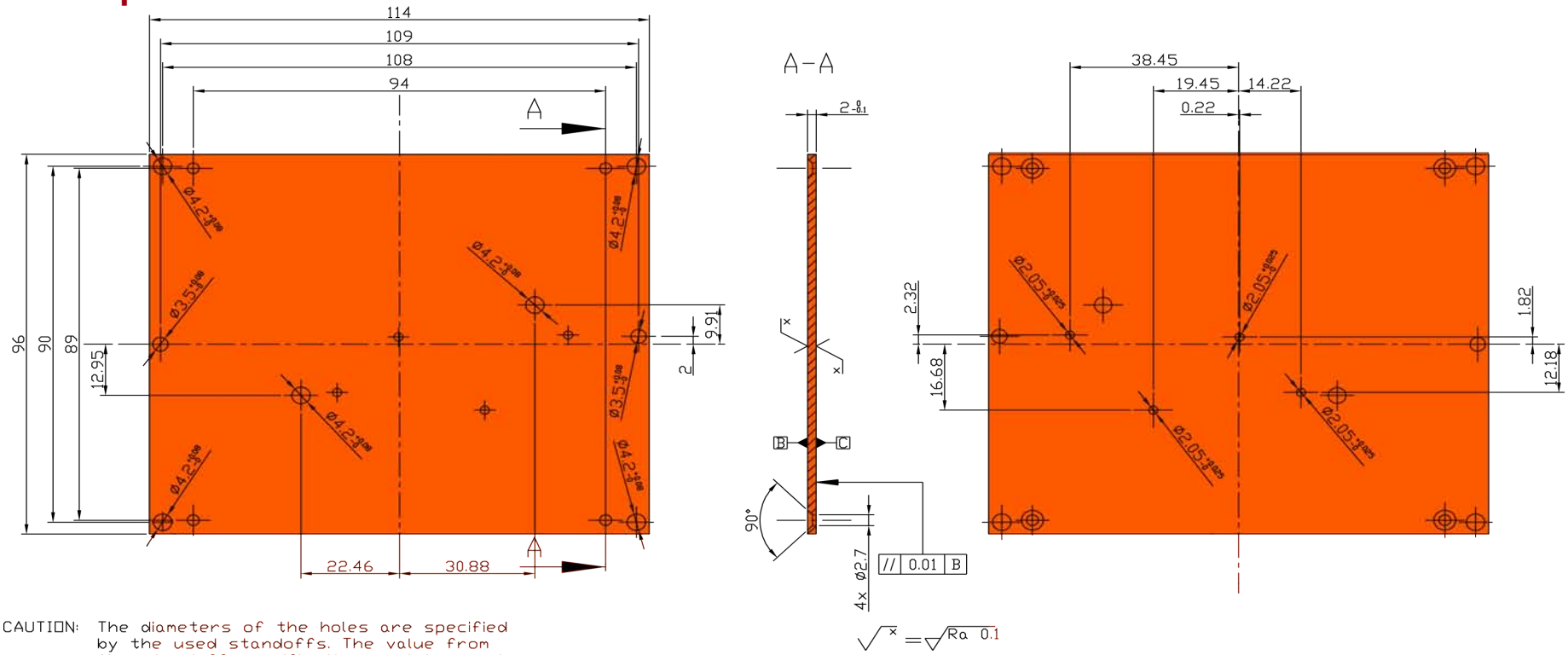
*For more information about this subject refer to Application Note AN14_ETX_XTX_Mounting_Solutions.pdf that can be found on the congatec website.*

*Only heatspreaders that feature micro pins that secure the thermal stacks should be used for applications that require the heatspreader to be mounted vertically. It cannot be guaranteed that the thermal stacks will not move if a heatspreader that does not have the pilot pin feature is used in vertically mounted applications.*

*Additionally, the gap pad material used on all heatspreaders contains silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

*For more information about heatspreader mounting refer to Application Note AN14_ETX_XTX_Mounting_Solutions.pdf that can be found on the congatec website.*

## 3.1 Heatspreader Dimensions




CAUTION: The diameters of the holes are specified by the used standoffs. The value from the standoff specification must be used.

**Note**

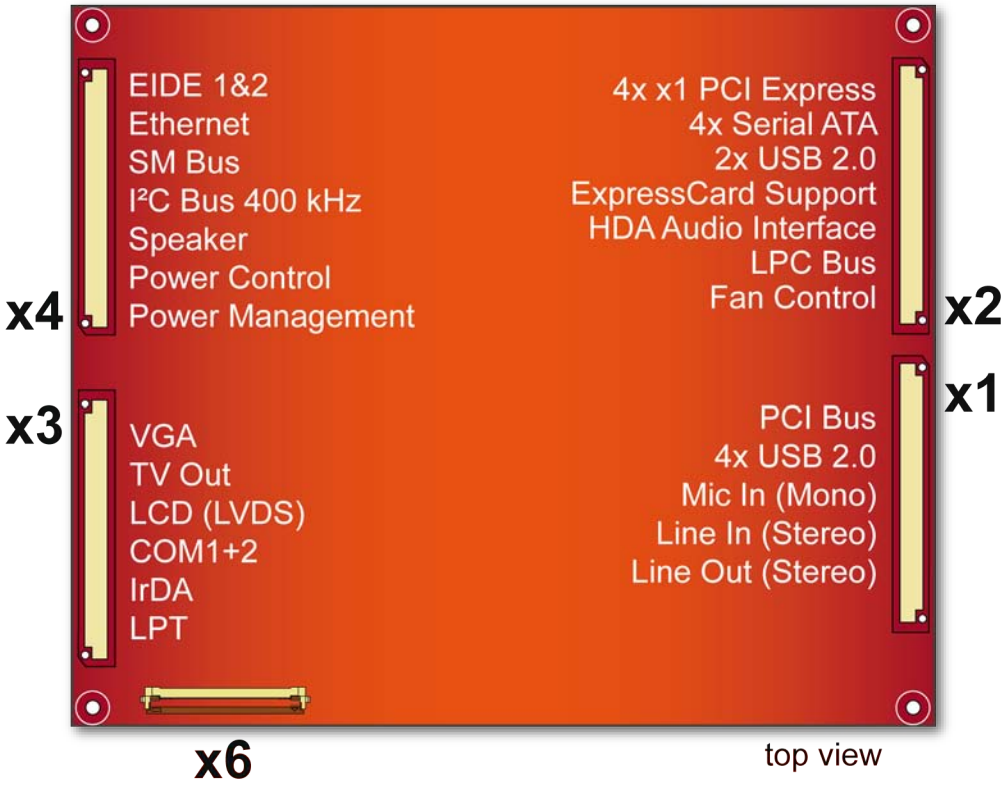
*All measurements are in millimeters. Torque specification for heatspreader screws is 0.3 Nm.*

**Caution**

*When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.*

# 4 Connector Subsystems

## X connector Subsystems (top view)




In this view the connectors are seen “through” the module.

## 4.1 Connector X1

The following subsystems can be found on connector X1.

### 4.1.1 PCI Bus

The PCI bus complies with PCI specification Rev. 2.3 and ETX® specification Rev. 3.02. It provides a 32bit parallel bus that is capable of operating at 33MHz.

**Note**

*The PCI interface is specified to be +5V tolerant, with +3.3V signaling.*

### 4.1.2 USB

The conga-XAF offers 4 USB host ports on the X1 connector via the AMD A55E FCH. These ports comply with USB standard 1.1 and 2.0 and they are located on the X1 connector. Each port is capable of supporting USB 1.1 and 2.0 compliant devices.

**Note**

*The USB controller is a PCI bus device. The BIOS allocates the necessary system resources when configuring the PCI devices.*

### 4.1.3 Audio

The conga-XAF module is equipped with a Realtek ALC262 HDA (High Definition Audio) codec onboard. The codec offers analog audio signals on the X1 connector.

### 4.1.4 Onboard Generated Supply Voltage

Pins 12, 16 and 24 on the X1 connector provide the ability to connect external devices to the supply voltage (3.3V±5%) generated onboard the module. 3.3V external devices can be connected to these pins but must not exceed a maximum external load of 500mA. For more information about this feature contact congatec AG technical support.

**Caution**

*Do not connect pins 12, 16 and 24 to a 3.3V external power supply. This will cause a current cross-flow and may result in either a system malfunction and/or damage to the external power supply and the module.*

## 4.2 Connector X2 (XTX™ Extension)

congatec AG replaced the outdated ISA bus found on X2 connector of the ETX module with the lastest technologies available. This implementation is called XTX™. The XTX™ extension is an enhancement of the ETX® standard and provides consumers the ability to equip their embedded applications with the latest technology while still utilizing the ETX® standard form factor.

The following subsystems can be found on connector X2.

### 4.2.1 LPC

The conga-XAF offers the LPC (Low Pin Count) bus through the AMD A55E FCH. There are many devices available for this bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific baseboard using this bus.

### 4.2.2 USB 2.0

The conga-XAF offers two additional USB ports on the X2 connector via the AMD A55E FCH. These ports are both USB 1.1 and 2.0 compliant. For more information about how the USB host controllers are routed see section 6.7 .

### 4.2.3 Serial ATA™

Two Serial ATA150 connections are provided via the AMD A55E FCH. Serial ATA, an enhancement of the parallel ATA offers higher performance. As a result of this enhancement, the traditional restrictions of parallel ATA are overcome with respect to speed and EMI. Serial ATA starts with a transfer rate of 150 Mbytes/s and can be expanded up to 600 Mbytes/s in order to accommodate future developments. Serial ATA is completely protocol and software compatible to parallel ATA.

### 4.2.4 PCI Express™

The conga-XAF offers 4 x1 PCI Express links via the AMD APU, which can be configured to support PCI Express edge cards or ExpressCards. Additionally, these links can be statically configured as 4 x1 or 1 x4. The Chipset Configuration Submenu in the BIOS setup program can be used to switch PCI Express channels 0-3 between x1 and x4 mode. The PCI Express interface is based on the *PCI Express Specification 2.0.*

### 4.2.5 ExpressCard™

The conga-XAF supports the implementation of ExpressCards, which requires the dedication of one USB port and one PCI Express lane for each ExpressCard used.

### 4.2.6 HDA (High Definition Audio) Digital Audio

The conga-XAF provides an interface that supports the connection of HDA audio codecs. For more information about this interface consult the XTX Design Guide.

### 4.2.7 Extended System Management

conga-XAF has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) Output. Additionally there is an input signal called FAN_TACHOIN that provides the ability to monitor the system fan's RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended. These features are implemented by the Winbond W83627DHG Super I/O.

## 4.3 Connector X3

The following subsystems can be found on connector X3. The implementation of all the subsystems comply with ETX® specification 2.7. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

### 4.3.1 Graphics

The conga-XAF features integrated high performance video within the AMD APU. Either AMD Radeon™ HD 6310 (18W APU) or AMD Radeon™ HD 6250 (9W APU) is integrated in the AMD processor. It supports DirectX®11 graphics with UVD 3.0, integrated VGA DAC, and dual simultaneous display.

### 4.3.2 LCD

The conga-XAF offers a dual channel LVDS interface. This interface is provided through the use of Analogix ANX3110 attached to one of the two APU DisplayPort interfaces. ANX3110 is a high quality DisplayPort™ to LVDS converter, offering up to 24 bits per pixel and single/dual channel LVDS output support. If the LVDS option (default) is present then the second DisplayPort/HDMI port is not available.

### 4.3.3 Serial Ports (1 and 2)

The conga-XAF offers two serial interfaces (TTL) via the Winbond W83627DHG Super I/O controller located on the conga-XAF.

### 4.3.4 Serial Infrared Interface

Serial port 2 can be configured as a serial infrared interface. The Infrared (IrDA) function provides point-to-point (or multi-point to multi-point) wireless communication, which can operate under various transmission protocols including IrDA SIR. This feature is also implemented by the onboard Winbond W83627DHG Super I/O.

### 4.3.5 Parallel Port

The multi-mode parallel port can be configured as either a conventional LPT parallel port, an Enhanced Parallel Port (EPP) or an Extended Capabilities Parallel Port (ECP). This is software implemented and can be configured in the BIOS setup program. See section 9.4.12 of this document for information about configuring the parallel port.

### 4.3.6 Keyboard/Mouse

The implementation of these subsystems comply with ETX® specification 2.7.

## 4.4 Connector X4

The following subsystems can be found on connector X4. The implementation of all the subsystems comply with ETX® specification 2.7. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

### 4.4.1 IDE

The conga-XAF supports an IDE interface that is capable of UDMA-66/100/133 operation. This interface is implemented by converting PCI Express to parallel ATA channels using JMicron's JMB368 chip on-module translation. IDE provides the connection of two channels (master/slave) and the primary and secondary devices are available at any given moment.

**Note**

*The IDE interface on the conga-XAF can only be used in Native IDE mode (no compatible/legacy IDE mode support).*

### 4.4.2 Ethernet

Ethernet interface is provided by a Realtek RTL8105E Fast Ethernet NIC controller. The controller is IEEE 802.3u, 10/100Base-Tx fast Ethernet compatible. The interface provides single-ended differential signals that have to be routed through an Ethernet transformer to the 10/100 BaseT RJ45 connector placed on the carrier board.

### 4.4.3 I²C Bus 400kHz

The I²C bus is implemented through the use of STMicroelectronics STM32F100R8 microcontroller. It provides a Fast Mode (400kHz max.) multi-master I²C Bus that has maximum I²C bandwidth.

### 4.4.4 Power Control

**PWGIN**

PWGIN (pin 4 on the X4 connector) can be connected to an external power good circuit or it may also be utilized as a manual reset input. In order to use PWGIN as a manual reset, the pin must be grounded through the use of a momentary-contact pushbutton switch. When external circuitry asserts this signal, it is necessary that an open-drain driver drives this signal causing it to be held low for a minimum of 15ms to initiate a reset. Using this input is optional. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies, the conga-XAF module is capable of generating its own power-on reset.

The conga-XAF provides support for controlling ATX-style power supplies. In order to do this the power supply must provide a constant source of 5V power. When not using an ATX power supply then the conga-XAF's pins PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

### PS_ON#

The PS_ON (pin 5 on the X4 connector) signal is an active-low output that turns on the main outputs of an ATX-style power supply. This open-collector signal can be pulled up to the 5V_SB supply voltage through the use of a 1K resistor. Usually there is a pull-up resistor internally implemented in the power supply itself yet it is also good practice to implement a footprint for the pull-up resistor in the baseboard circuitry.

### PWRBTN#

When using ATX-style power supplies, PWRBTN# (pin 7 on the X4 connector) is used to connect to a momentary-contact, active-low pushbutton input while the other terminal on the pushbutton must be connected to ground. This signal is XTX™ internally pulled up to 5V_SB using a 4k7 resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

## Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-XAF. The other necessary voltages are internally generated on the module using onboard power supplies. A baseboard designer should be aware of the following important information when designing a power supply for a conga-XAF application:

- As mentioned earlier in section 4.1.4 the conga-XAF is capable of generating an onboard 3.3V supply with an output current that is limited to 500mA. If an external device requires more than the 500mA limit then it is necessary to design a 3.3V supply into the baseboard.

**Caution**

*It is not possible to connect an external 3.3V supply to the onboard generated 3.3V supply pins on the conga-XAF module. This will cause a current cross-flow and may result in either a system malfunction and/or damage to the external power supply and the module.*

- Sometimes when designing baseboards, baseboard designers choose to fuse power to some external devices such as keyboards or USB devices by using solid-state or polyswitch overcurrent protection devices. This results in the protective devices typically only opening after they pass their rated current several times for long periods of time. When the application power supply is incapable of generating the necessary current needed to open these protective devices, it is possible that the application crashes as a result of an external fault and therefore will reduce the reliability of the application as well as make a fault diagnosis difficult.

- It has also been noticed that on some occasions problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed

monotonic and does not have any dips. This should be done during the power supply qualification phase, therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document “ATX12V Power Supply Design Guide V2.2”.

### 4.4.5 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

## 4.5 Connector X6

Flat foil connector X6 provides a Digital Display Interface (DDI), that can be configured as DisplayPort or HDMI/DVI Interface.

# 5 Additional Features

## 5.1 Watchdog

The conga-XAF is equipped with a multi-stage watchdog. This solution can be triggered by software and external OEM hardware (input pin is pin 48 on the X2 connector called WDTRG#). For more information about the Watchdog feature see the BIOS setup description section 9.4.2 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

## 5.2 Onboard Microcontroller

The conga-XAF is equipped with a STMicroelectronics STM32F100R8 microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

## 5.3 Embedded BIOS

The conga-XAF is equipped with congatec Embedded BIOS and has the following features:

- ACPI Power Management
- ACPI Battery Support
- Supports Customer Specific CMOS Defaults
- Multi-stage Watchdog
- User Data Storage
- Manufacturing Data and Board Information
- OEM Splash Screen
- Flat Panel Auto Detection and Backlight Control
- BIOS Setup Data Backup
- Fast Mode I²C Bus
- Real Headless Operation
- Console Redirection via Serial Port

## 5.4 DDI

The conga-XAF provides one Digital Display Interface (DDI), which is implemented by the AMD APU. This interface is available via a connector (X6) located on the bottomside of conga-XAF. DDI can be configured to support DisplayPort or TMDS signals used by by HDMI or DVI. The DisplayPort is compliant with DisplayPort Standard Version 1.1a; HDMI is compliant with High-Definition Multimedia Interface Specification Version 1.3a; DVI is compliant with Digital Visual Interface Revision 1.0. For information about the pinout of the X6 connector see section 7.8 .

## 5.5 Security Features

The conga-XAF can be equipped optionally with a “Trusted Platform Module“ (TPM 1.2). This TPM 1.2 includes co-processors to calculate efficient hash and RSA algorithms with key lengths up to 2,048 bits as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity and confidence levels.

## 5.6 Suspend to RAM (S3)

The Suspend to RAM feature is available on the conga-XAF.

## 5.7 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-XAF BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM² User’s Guide

# 6 conga Tech Notes

The conga-XAF has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

## 6.1 Native vs. Compatible IDE mode

### 6.1.1 Compatible Mode

When operating in compatible mode, the SATA controller needs two legacy IRQs (14 and 15) and is unable to share these IRQs with other devices. This is because the SATA controller emulates the primary and secondary legacy IDE controllers. The two PATA controllers on conga-XAF do not support compatible IDE mode.

The SATA controller defaults to native IDE mode but can be set to Compatible/Legacy IDE mode in the “SATA/PATA Configuration Submenu” in the BIOS setup program. See section 9.4.10 of this user's guide for more information about this.

### 6.1.2 Native Mode

Native mode allows the SATA controller and PATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources, which means they can be configured anywhere within the system. When either controller runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system. Running the SATA controller in native mode frees up IRQs 14 and 15 to be used for the ISA bus and decreases the chance that there may be a shortage of interrupts when installing devices.

**Note**

*If your operating system supports native mode then congatec AG recommends you enable it. Only operating systems supporting native IDE mode can be booted from the PATA interface.*

## 6.2 Thermal Monitor and Catastrophic Thermal Protection

G-Series processors provide a side-band thermal sensor interface (SB-TSI) to read the die temperature. The thermal diode is not supported on G-Series processors. SB-TSI is an on-die temperature sensing interface that accesses the internal digital temperature sensor. SB-TSI uses SMBus protocol, which allows use of an embedded controller. Additionally on G-Series processors, SB-TSI can set a P-state limit to limit the CPU power consumption.

**Note**

*The maximum operating temperature for G-Series processors is 100°C.*

## 6.3 Processor Thermal Management

G-Series processors provide hardware thermal control (HTC), local hardware thermal control (LHTC), PROCHOT_L pin, and THERMTRIP to ensure that the processor is within its functional temperature limits.

• HTC is a hardware mechanism activated internally by the processor to reduce its power consumption.

• LHTC provides an additional layer of thermal protection. When the LHTC temperature threshold is exceeded, the processor limits the maximum P-state of all cores to reduce power consumption. Typically, the LHTC temperature threshold is few degrees below the HTC temperature threshold. Also, the LHTC limits the processor to a higher P-state than HTC, i.e., the reduction in power with LHTC is less than that with HTC.

• The PROCHOT_L pin, as a bidirectional pin, provides a mechanism for hardware (e.g. an embedded controller or external temperature sensor) to activate HTC. It is useful for current limiting under battery control and system thermal management.

• THERMTRIP is a hardware-enforced thermal protection mechanism activated by the processor. The processor clocks are gated off and a low voltage VID is sent to the voltage regulator. THERMTRIP activates only when the processor temperature is much greater than the specified maximum temperature (approximately at 125°C).

## 6.4 Processor Performance Control

G-Series processors run at different voltage/frequency states (performance states), which is referred to P-State technology. Operating systems that support performance control take advantage of microprocessors that use several performance states in order to efficiently operate the processor when it is not being fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows operating systems links its processor performance control policy to the power scheme setting found in the control panel option applet.

**Note**

*If the "Home/Office" or "Always On" power scheme is selected when using Windows operating systems then the processor will always run at the highest performance state. For more information about this subject see chapter 8 of the ACPI Specification Revision 2.0c, which can be found at www.acpi.info. Also visit Microsoft's website and search for the document called "Windows Native Processor Performance Control".*

## 6.5 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-XAF ACPI thermal solution offers three different cooling policies.

- Passive Cooling

  When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the “passive cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- Active Cooling

  During this cooling policy the operating system turns the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without reducing the overall system performance. Use the “active cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

- Critical Trip Point

  If the temperature in the thermal zone reaches a critical point then the operating system performs a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the “critical trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

**Note**

*The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points. If passive cooling is activated and the processor temperature is above the trip point, the processor clock is throttled.*

## 6.6 ACPI Suspend Modes and Resume Events

conga-XAF supports the S3 (STR= Suspend to RAM) state. For more information about S3 wake events see section 9.4.4 “ACPI Configuration Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Winodws 7/Vista/XP/2K
- Linux

This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

| Wake Event | Conditions/Remarks |
|---|---|
| Power Button | Wakes unconditionally from S3-S5. |
| Onboard LAN Event | Device driver must be configured for Wake On LAN support. |
| PME# | Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu. |
| USB Mouse/Keyboard Event | |
| RTC Alarm | Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5. |
| Watchdog Power Button Event | Wakes unconditionally from S3-S5. |

**Note**

*The above list has been verified using a Windows XP SP3 ACPI enabled installation.*

## 6.7 USB 2.0 EHCI Host Controller Support

The 6 USB ports are shared between the 3 EHCI host controller and the 3 OHCI host controllers. Within the EHC functionality there is a port-routing logic that executes the muxing between the two different types of host controllers (EHCI and OHCI). This means that when a USB device is connected, the routing logic determines who owns the port. If the device is not USB 2.0 compliant or if the software drivers for EHCI support are not installed, then the OHCI controller owns the ports.

## 6.8 HDMI/DisplayPort (DP) Audio Support

In order to support HDMI/DP audio on the X6 connector, the system must be configured as follows:

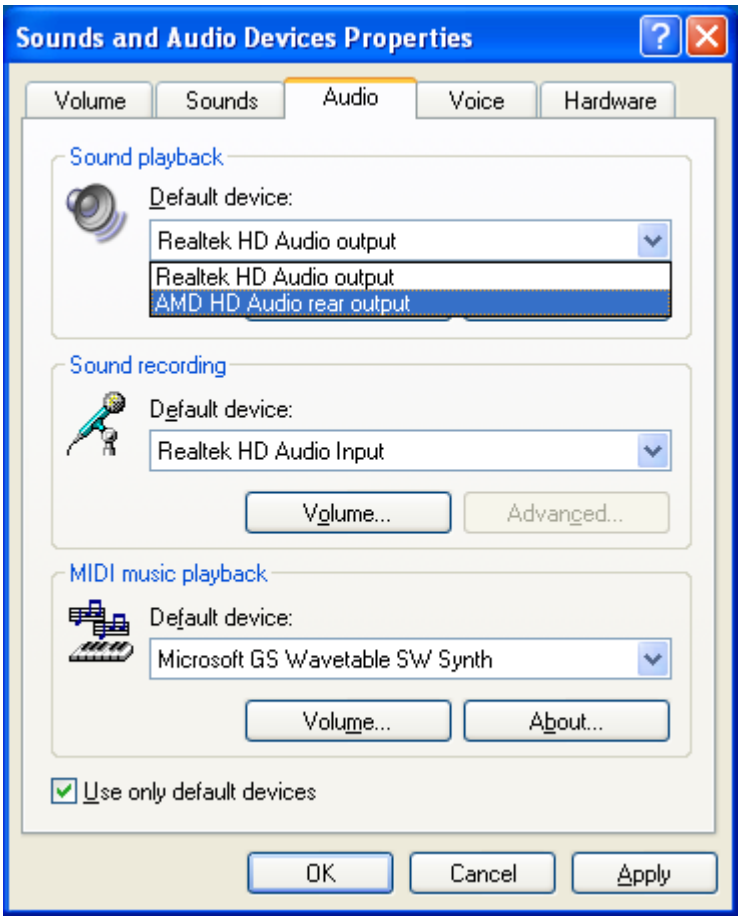
- BIOS default settings (HDA Controller ENABLED, HDMI/DP Audio Support ENABLED)
- Installation of AMD chipset drivers include HDMI/DP audio support
- Installation of Realtek HDA codec driver

HDMI/DP audio and native HDA audio can only work one at a time, not both at the same time. The desired audio output must be selected in the audio device driver and/or OS setting.

congatec has validated the HDMI/DP audio functionality within Windows XP SP3 by using the following test procedures and settings.

Play wma/mp3 (video/audio) file with Microsoft Windows media player:

- Audio functions on one output only (either HDMI/DP or HDA):
- Connect headphones to HDMI/DP monitor -> validate that this is functioning.
- Next step (while audio is still present) connect another speaker to the native audio output of the conga-EAF -> validate that no audio is present.
- Change the default “Sound Playback device” in the “Sound and Audio Device Properties” menu (see below) to “Realtek HD Audio output”.




After this change the audio is no longer present in the headphones connected to the HDMI/DP monitor but the audio is now present on the native audio output of the conga-XAF.

# 7 Signal Descriptions and Pinout Tables

The following section describes the signals found on the four X connectors located on the bottom of the module. X1, X3, and X4 connectors are ETX® standard compliant while the X2 connector complies with the XTX™ extension specification. Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a XTX® module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

**Note**

*The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.*

**Table 2 Signal Tables Terminology Descriptions**

| Term | Description |
|---|---|
| PU | congatec implemented pull-up resistor |
| PD | congatec implemented pull-down resistor |
| I/O 3.3V | Bi-directional signal 3.3V tolerant |
| I/O 5V | Bi-directional signal 5V tolerant |
| I 3.3V | Input 3.3V tolerant |
| I 5V | Input 5V tolerant |
| I/O 3.3VSB | Input 3.3V tolerant active in standby state |
| O 3.3V | Output 3.3V signal level |
| O 5V | Output 5V signal level |
| P | Power Input/Output |
| DDC | Display Data Channel |
| PCIE | In compliance with PCI Express Base Specification, Revision 2.0 |
| SATA | In compliance with Serial ATA specification, Revision 2.6 |
| LVDS | Low Voltage Differential Signal-350mV nominal; 450mV maximum differential signal |
| TPM | Trusted Platform Module |

## 7.1 X1 Connector Signal Descriptions

**Table 3 Signal Descriptions**

| Signal | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|
| VCC | Power Supply +5VDC ±5% | P | | External supply |
| GND | Power Ground | P | | External supply |
| 3V | Power Supply +3.3VDC | P | | See section 4.1.4 |
| N.C. | Not Connected | N.A. | | Do not connect |
| SERIRQ | Serial Interrupt request | I 3.3V | | Used in conjunction with LPC bus |

**Table 4 PCI Signal Descriptions**

| Signal | Description of PCI Bus Signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| PCICLK1..4. | Clock output | O 3.3V | | |
| REQ0..3# | Bus request | I 3.3V | | 5V Tolerant |
| GNT0..3# | Bus grant | O 3.3V | | |
| AD0..31 | Address/Data bus lines | I/O 3.3V | | 5V Tolerant |
| CBE0..3# | Bus command/byte enables | I/O 3.3V | | 5V Tolerant |
| PAR | Bus parity | I/O 3.3V | | 5V Tolerant |
| SERR# | Bus system error | I/O 3.3V | | 5V Tolerant |
| GPERR# | Bus grant parity error | I/O 3.3V | | 5V Tolerant |
| PME# | Bus power management event | I/O 3.3VSB | | 5V Tolerant |
| LOCK# | Bus lock | I/O 3.3V | | 5V Tolerant |
| DEVSEL# | Bus device select | I/O 3.3V | | 5V Tolerant |
| TRDY# | Bus target ready | I/O 3.3V | | 5V Tolerant |
| IRDY# | Bus initiator ready | I/O 3.3V | | 5V Tolerant |
| STOP# | Bus stop | I/O 3.3V | | 5V Tolerant |
| FRAME# | Bus frame | I/O 3.3V | | 5V Tolerant |
| PCIRST# | Bus reset | O 3.3V | | Asserted during system reset |
| INTA# | Bus interrupt A | I 3.3V | | 5V Tolerant |
| INTB# | Bus interrupt B | I 3.3V | | 5V Tolerant |
| INTC# | Bus interrupt C | I 3.3V | | 5V Tolerant |
| INTD# | Bus interrupt D | I 3.3V | | 5V Tolerant |

### Table 5 USB Signal Descriptions

| Signal | Description of USB Signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| USB0 | USB Port 0, data + or D+ | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |
| USB0# | USB Port 0, data - or D- | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |
| USB1 | USB Port 1, data + or D+ | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |
| USB1# | USB Port 1, data - or D- | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |
| USB2 | USB Port 2, data + or D+ | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |
| USB2# | USB Port 2, data - or D- | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |
| USB3 | USB Port 3, data + or D+ | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |
| USB3# | USB Port 3, data - or D- | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |

### Table 6 Audio Signal Descriptions

| Signal | Description of Audio Signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| SNDL | Line-Level stereo output left | O | | Analog output (1 Vrms) |
| SNDR | Line-Level stereo output right | O | | Analog output (1 Vrms) |
| AUXAL | Auxiliary input A left | I | | Analog input (1 Vrms) |
| AUXAR | Auxiliary input A right | I | | Analog input (1 Vrms) |
| MIC | Microphone input | I | | Analog input (1 Vrms) |
| ASGND | Analog ground of sound controller | P | | |
| ASVCC | Analog supply of sound controller | P | | Internally connected to+3.3 audio voltage for reference, max. 10mA |

## 7.2 Connector X1 Pinout

**Table 7 X1 Connector Pinout**

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | GND | 2 | GND | 51 | VCC | 52 | VCC |
| 3 | PCICLK3 | 4 | PCICLK4 | 53 | PAR | 54 | SERR# |
| 5 | GND | 6 | GND | 55 | GPERR# | 56 | Reserved |
| 7 | PCICLK1 | 8 | PCICLK2 | 57 | PME# | 58 | USB2# |
| 9 | REQ3# | 10 | GNT3# | 59 | LOCK# | 60 | DEVSEL# |
| 11 | GNT2# | 12 | 3V | 61 | TRDY# | 62 | USB3# |
| 13 | REQ2# | 14 | GNT1# | 63 | IRDY# | 64 | STOP# |
| 15 | REQ1# | 16 | 3V | 65 | FRAME# | 66 | USB2 |
| 17 | GNT0# | 18 | RESERVED | 67 | GND | 68 | GND |
| 19 | VCC | 20 | VCC | 69 | AD16 | 70 | CBE2# |
| 21 | SERIRQ | 22 | REQ0# | 71 | AD17 | 72 | USB3 |
| 23 | AD0 | 24 | 3V | 73 | AD19 | 74 | AD18 |
| 25 | AD1 | 26 | AD2 | 75 | AD20 | 76 | USB0# |
| 27 | AD4 | 28 | AD3 | 77 | AD22 | 78 | AD21 |
| 29 | AD6 | 30 | AD5 | 79 | AD23 | 80 | USB1# |
| 31 | CBE0# | 32 | AD7 | 81 | AD24 | 82 | CBE3# |
| 33 | AD8 | 34 | AD9 | 83 | VCC | 84 | VCC |
| 35 | GND | 36 | GND | 85 | AD25 | 86 | AD26 |
| 37 | AD10 | 38 | AUXAL | 87 | AD28 | 88 | USB0 |
| 39 | AD11 | 40 | MIC | 89 | AD27 | 90 | AD29 |
| 41 | AD12 | 42 | AUXAR | 91 | AD30 | 92 | USB1 |
| 43 | AD13 | 44 | ASVCC | 93 | PCIRST# | 94 | AD31 |
| 45 | AD14 | 46 | SNDL | 95 | INTC# | 96 | INTD# |
| 47 | AD15 | 48 | ASGND | 97 | INTA# | 98 | INTB# |
| 49 | CBE1# | 50 | SNDR | 99 | GND | 100 | GND |

## 7.3 X2 Connector Signal Descriptions (XTX™ extension)

### Table 8 LPC Interface Signal Descriptions

| Signal | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|
| LPC_AD[0..3] | Multiplexed Command, Address and Data. | I/O 3.3V | | |
| LPC_FRAME# | Frame: Indicates start of a new cycle or termination of a broken cycle. | O 3.3V | | |
| LPC_DRQ[0..1]# | Encoded DMA/Bus Master Request. | I 3.3V | | |

### Table 9 Serial ATA Signal Descriptions

| Signal | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|
| SATA0_RX+<br>SATA0_RX- | Serial ATA channel 0, Receive Input differential pair. | I SATA | | Supports Serial ATA specification, Revision 2.6 |
| SATA0_TX+<br>SATA0_TX- | Serial ATA channel 0, Transmit Output differential pair. | O SATA | | Supports Serial ATA specification, Revision 2.6 |
| SATA1_RX+<br>SATA1_RX- | Serial ATA channel 1, Receive Input differential pair. | I SATA | | Supports Serial ATA specification, Revision 2.6 |
| SATA1_TX+<br>SATA1_TX- | Serial ATA channel 1, Transmit Output differential pair. | O SATA | | Supports Serial ATA specification, Revision 2.6 |
| SATA2_RX+<br>SATA2_RX- | Serial ATA channel 2, Receive Input differential pair. | I SATA | | Supports Serial ATA specification, Revision 2.6 |
| SATA2_TX+<br>SATA2_TX- | Serial ATA channel 2, Transmit Output differential pair. | O SATA | | Supports Serial ATA specification, Revision 2.6 |
| SATA3_RX+<br>SATA3_RX- | Serial ATA channel 3, Receive Input differential pair. | I SATA | | Supports Serial ATA specification, Revision 2.6 |
| SATA3_TX+<br>SATA3_TX- | Serial ATA channel 3, Transmit Output differential pair. | O SATA | | Supports Serial ATA specification, Revision 2.6 |
| IL_SATA# | Serial ATA Interlock Switch Input. | I 3.3V | | Not supported |
| SATALED# | Serial ATA Led. Open collector output pin driven during SATA command activity. | OC 3.3V | | |

### Table 10 PCI Express Signal Descriptions

| Signal | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|
| PCIE0_RX+<br>PCIE0_RX- | PCI Express channel 0, Receive Input differential pair. | I PCIE | | Supports PCI Express Base Specification, Revision 2.0 |
| PCIE0_TX+<br>PCIE0_TX- | PCI Express channel 0, Transmit Output differential pair. | O PCIE | | Supports PCI Express Base Specification, Revision 2.0 |
| PCIE1_RX+<br>PCIE1_RX- | PCI Express channel 1, Receive Input differential pair. | I PCIE | | Supports PCI Express Base Specification, Revision 2.0 |
| PCIE1_TX+<br>PCIE1_TX- | PCI Express channel 1, Transmit Output differential pair. | O PCIE | | Supports PCI Express Base Specification, Revision 2.0 |
| PCIE2_RX+<br>PCIE2_RX- | PCI Express channel 2, Receive Input differential pair. | I PCIE | | Supports PCI Express Base Specification, Revision 2.0 |
| PCIE2_TX+<br>PCIE2_TX- | PCI Express channel 2, Transmit Output differential pair. | O PCIE | | Supports PCI Express Base Specification, Revision 2.0 |
| PCIE3_RX+<br>PCIE3_RX- | PCI Express channel 3, Receive Input differential pair. | I PCIE | | Supports PCI Express Base Specification, Revision 2.0 |
| PCIE3_TX+<br>PCIE3_TX- | PCI Express channel 3, Transmit Output differential pair. | O PCIE | | Supports PCI Express Base Specification, Revision 2.0 |
| PCIE_CLK_REF+<br>PCIE_CLK_REF- | PCI Express Reference Clock for Lanes 0 to 3. | O PCIE | | Refer to XTX design guide for additional information |
| PCE_WAKE# | PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup. | I 3.3VSB | | |

### Table 11 ExpressCard Support Pins Descriptions

| Signal | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|
| EXEC_CPPE[0..1]# | ExpressCard capable card request. | I 3.3VSB | | |
| EXEC_RST[0..1]# | ExpressCard Reset | O 3.3V | | |

### Table 12 Audio Codec Signal Descriptions

| Signal | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|
| AC_RST# | CODEC Reset | O 3.3V | | |
| AC_SYNC | Serial Bus Synchronization. | O 3.3V | | |
| AC_BIT_CLK | 12.228 MHz Serial Bit Clock from CODEC. | O 3.3V | | |
| AC_SDOUT | Audio Serial Data Output to CODEC. | O 3.3V | | |
| AC_SDIN[0..2] | Audio Serial Data Input from CODEC0..CODEC2. | I 3.3V | | |
| CODECSET | Disable onboard Audio Codec. | I 3.3V | | Not supported |

### Table 13 USB Signal Descriptions

| Signal | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|
| USBP4 | USB Port 4, data + or D+ | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |
| USBP4# | USB Port 4, data - or D- | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |
| USBP5 | USB Port 5, data + or D+ | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |
| USBP5# | USB Port 5, data - or D- | I/O 3.3V | | USB 2.0 compliant and backwards compatible to USB 1.1 |

### Table 14 Miscellaneous Signal Descriptions

| Signal | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|
| GND | Ground. All GND pins should be connected to the baseboard ground plane. | P | | |
| 5V_SB | Additional Power input for the internal suspend and power-control circuitry. This signal is connected to XTX-Connector X4/Pin3. Refer to XTX Specification for further details. | P | | |
| VCC | 5V Power Input. All VCC pins should be connected to the baseboard 5 Volt power plane. | P | | |
| SUS_STAT# | Suspend Status: indicates that the system will be entering a low power state soon. | O 3.3VSB | | |
| SLP_S3# | S3 Sleep Control: This signal shuts off power to all non-critical systems when in S3 (Suspend to Ram), S4 or S5 states. | O 3.3VSB | | |
| SLP_S5# | SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (soft off) states. | O 3.3VSB | | |
| PCI_CLKRUN# | This clock supports the PCI CLKRUN protocol. It connects to peripherals that need to request clock restart or prevention of clock stopping. | I/O 3.3V | | |
| PCI_GNT#A | reserved | O 3.3V | | Not supported |
| PCI_REQ#A | reserved | I 3.3V | | Not supported |
| FAN_PWMOUT | Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. | O 5V | | |
| FAN_TACHOIN | Fan tachometer input. | I 5V | | |
| WDTRIG | Watch Dog Trigger signal. | I 5V | | |
| PP_TPM | Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM. | I 3.3V | | |

## 7.4 X2 Connector Pinout

The following table includes a reference column describing the corresponding ETX standard X2 connector pinout.

**Table 15 X2 Connector Pinout**

| Pin | XTX™ Signal | *ETX® Reference* | Pin | XTX™ Signal | *ETX® Reference* |
|---|---|---|---|---|---|
| 1 | GND | GND | 2 | GND | GND |
| 3 | PCIE_CLK_REF+ | SD14 | 4 | SATA0_RX+ | SD15 |
| 5 | PCIE_CLK_REF- | SD13 | 6 | SATA0_RX- | MASTER# |
| 7 | GND | SD12 | 8 | GND | DREQ7 |
| 9 | PCIE3_TX+ | SD11 | 10 | SATA0_TX- | DACK7# |
| 11 | PCIE3_TX- | SD10 | 12 | SATA0_TX+ | DREQ6 |
| 13 | GND | SD9 | 14 | 5V_SB | DACK6# |
| 15 | PCIE3_RX+ | SD8 | 16 | SATA1_RX+ | DREQ5 |
| 17 | PCIE3_RX- | MEMW# | 18 | SATA1_RX- | DACK5# |
| 19 | VCC | MEMR# | 20 | 5V_SB | DREQ0 |
| 21 | EXC1_CPPE# | LA17 | 22 | SATA1_TX- | DACK0# |
| 23 | EXC1_RST# | LA18 | 24 | SATA1_TX+ | IRQ14 |
| 25 | USBP5 | LA19 | 26 | GND | IRQ15 |
| 27 | USBP5# | LA20 | 28 | SATA2_RX+ | IRQ12 |
| 29 | GND | LA21 | 30 | SATA2_RX- | IRQ11 |
| 31 | PCIE2_TX+ | LA22 | 32 | SUS_STAT# | IRQ10 |
| 33 | PCIE2_TX- | LA23 | 34 | PCI_CLKRUN# | IO16# |
| 35 | GND | GND | 36 | GND | GND |
| 37 | PCIE2_RX+ | SBHE# | 38 | SATA2_TX- | M16# |
| 39 | PCIE2_RX- | SA0 | 40 | SATA2_TX+ | OSC |
| 41 | EXC0_CPPE# | SA1 | 42 | GND | BALE |
| 43 | EXC0_RST# | SA2 | 44 | SATA3_RX+ | TC |
| 45 | USBP4 | SA3 | 46 | SATA3_RX- | DACK2# |
| 47 | USBP4# | SA4 | 48 | WDTRIG | IRQ3 |
| 49 | SLP_S3# | SA5 | 50 | SATALED# | IRQ4 |
| 51 | VCC | VCC | 52 | VCC | VCC |
| 53 | PCIE1_RX- | SA6 | 54 | SATA3_TX- | IRQ5 |
| 55 | PCIE1_RX+ | SA7 | 56 | SATA3_TX+ | IRQ6 |
| 57 | GND | SA8 | 58 | IL_SATA# (*) | IRQ7 |
| 59 | PCIE1_TX- | SA9 | 60 | RESERVED | SYSCLK |
| 61 | PCIE1_TX+ | SA10 | 62 | RESERVED | REFSH# |
| 63 | PCE_WAKE# | SA11 | 64 | PCI_GNT#A (*) | DREQ1 |
| 65 | SLP_S5# | SA12 | 66 | PCI_REQ#A (*) | DACK1# |
| 67 | GND | GND | 68 | GND | GND |
| 69 | PCIE0_RX- | SA13 | 70 | RESERVED | DREQ3 |

| Pin | XTX™ Signal | *ETX® Reference* | Pin | XTX™ Signal | *ETX® Reference* |
|---|---|---|---|---|---|
| 71 | PCIE0_RX+ | SA14 | 72 | RESERVED | DACK3# |
| 73 | GND | SA15 | 74 | VCC | IOR# |
| 75 | PCIE0_TX- | SA16 | 76 | RESERVED | IOW# |
| 77 | PCIE0_TX+ | SA18 | 78 | RESERVED | SA17 |
| 79 | CODECSET (*) | SA19 | 80 | VCC | SMEMR# |
| 81 | AC_RST# | IOCHRDY | 82 | AC_SDOUT | AEN |
| 83 | VCC | VCC | 84 | VCC | VCC |
| 85 | AC_SYNC | SD0 | 86 | AC_SDIN0 | SMEMW# |
| 87 | AC_SDIN1 | SD2 | 88 | AC_SDIN2 | SD1 |
| 89 | AC_BIT_CLK | SD3 | 90 | FAN_TACHOIN | NOWS# |
| 91 | LPC_AD0 | DREQ2 | 92 | FAN_PWMOUT | SD4 |
| 93 | LPC_AD1 | SD5 | 94 | LPC_FRAME# | IRQ9 |
| 95 | LPC_AD2 | SD6 | 96 | LPC_DRQ0# | SD7 |
| 97 | LPC_AD3 | IOCHK# | 98 | LPC_DRQ1# | RSTDRV |
| 99 | GND | GND | 100 | GND | GND |

**Note**

*The signals marked with an asterisk symbol (*) are not supported on the conga-XAF.*

## 7.5 X3 Connector Signal Descriptions

### Table 16 Signal Descriptions

| Signal | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|
| VCC | Power Supply +5VDC, ±5% | P | | External supply |
| GND | Power Ground | P | | External supply |
| N.C. | Not connected | N.A. | | Do not connect |
| LTGIO0 | Not connected | N.C. | | Not supported |

### Table 17 CRT Signal Descriptions

| Signal | Description of CRT signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| HSY | Horizontal Synchronization Pulse | O 5V | | |
| VSY | Vertical Synchronization Pulse | O 5V | | |
| R | Red channel RGB Analog Video Output | O | | Analog output |
| G | Green channel RGB Analog Video Output | O | | Analog output |
| B | Blue channel RGB Analog Video Output | O | | Analog output |
| DDCK | Display Data Channel Clock | I/O 5V | | |
| DDDA | Display Data Channel Data | I/O 5V | | |

### Table 18 TV Signal Descriptions

| Signal | Description of CRT signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| SYNC | Composite sync | N.C. | | Not supported |
| Y | Luminance for S-Video or Red for SCART | O | | Not supported |
| C | Chrominance for S-Video or Green for SCART | O | | Not supported |
| COMP | Composite Video or Blue for SCART | O | | Not supported |

### Table 19 COM Signal Descriptions

| Signal | Description of COM signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| DTR1# | Data terminal ready for COM1 | O 3.3V | | |
| DTR2# | Data terminal ready for COM2 | O 3.3V | | |
| RI1#, RI2# | Ring indicator for COM1/COM2 | I 3.3.V | PU 100K | 5V tolerant input |
| TXD1, TXD2 | Data transmit for COM1/COM2 | O 3.3V | | |
| RXD1, RXD2 | Data receive for COM1/COM2 | I 3.3V | PU 100K | 5V tolerant input |
| CTS1#, CTS2# | Clear to send for COM1/COM2 | I 3.3V | PU 100K | 5V tolerant input |
| RTS1# | Request to send for COM1 | O 3.3V | | |
| RTS2# | Request to send for COM2 | O 3.3V | | |
| DCD1#, DCD2# | Data carrier detect for COM1/COM2 | I 3.3V | PU 100K | 5V tolerant input |
| DSR1#, DSR2# | Data set ready for COM1/COM2 | I 3.3V | PU 100K | 5V tolerant input |

**Note**

*Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.9 of this user's guide.*

### Table 20 Keyboard and Infrared Signal Descriptions

| Signal | Description of keyboard and infrared signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| KBDAT | Keyboard Data | I/O 5V | PU 4K7 | |
| KBCLK | Keyboard Clock | O 5V | PU 4K7 | |
| MSDAT | Mouse Data | I/O 5V | PU 4K7 | |
| MSCLK | Mouse Clock | O 5V | PU 4K7 | |
| IRTX | Infrared Transmit | O 5V | PU 100K | |
| IRRX | Infrared Receive | I 5V | PU 100K | |

### Table 21 LVDS Flat Panel Signals

| Signal | Description of LVDS Flat Panel signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| BIASON | Controls display contrast voltage ON | O 3.3V | | |
| DIGON | Controls display Power ON | O 3.3V | | |
| BLON# | Controls display Backlight ON | O 3.3V | | |
| LCDDO0..19 | LVDS channel data 0..19 | O LVDS | | |
| DETECT# | Panel hot-plug detection | N.C. | | Not supported |
| FPDDC_CLK | DDC lines used for flat panel detection and control. | O 3.3V | | |
| FPDDC_DAT | DDC lines used for flat panel detection and control. | I/O 3.3V | | |

### Table 22 LVDS Interface Pinout

| Pin | Signal Name | Signal Mapping | Pin | Signal Name | Signal Mapping |
|---|---|---|---|---|---|
| 1 | GND | | 2 | GND | |
| 3 | R | | 4 | B | |
| 5 | HSY | | 6 | G | |
| 7 | VSY | | 8 | DDCK | |
| 9 | DETECT# (*) | | 10 | DDDA | |
| 11 | LCDDO[16] | TX2OUTCLK- | 12 | LCDDO[18] | TX2OUT3- |
| 13 | LCDDO[17] | TX2OUTCLK+ | 14 | LCDDO[19] | TX2OUT3+ |
| 15 | GND | | 16 | GND | |
| 17 | LCDDO[13] | TX2OUT1+ | 18 | LCDDO[15] | TX2OUT2+ |
| 19 | LCDDO[12] | TX2OUT1- | 20 | LCDDO[14] | TX2OUT2- |
| 21 | GND | | 22 | GND | |
| 23 | LCDDO[8] | TX1OUT3- | 24 | LCDDO[11] | TX2OUT0+ |
| 25 | LCDDO[9] | TX1OUT3+ | 26 | LCDDO[10] | TX2OUT0- |
| 27 | GND | | 28 | GND | |
| 29 | LCDDO[4] | TX1OUT2- | 30 | LCDDO[7] | TX1OUTCLK+ |
| 31 | LCDDO[5] | TX1OUT2+ | 32 | LCDDO[6] | TX1OUTCLK- |
| 33 | GND | | 34 | GND | |
| 35 | LCDDO[1] | TX1OUT0+ | 36 | LCDDO[3] | TX1OUT1+ |
| 37 | LCDDO[0] | TX1OUT0- | 38 | LCDDO[2] | TX1OUT1- |
| 39 | VCC | | 40 | VCC | |
| 41 | FPDDC_DAT | | 42 | LTGIO0 | |
| 43 | FPDDC_CLK | | 44 | BLON# | |
| 45 | BIASON | | 46 | DIGON | |
| 47 | COMP (*) | | 48 | Y (*) | |
| 49 | SYNC (*) | | 50 | C (*) | |

TX1= Channel 1 transmit
TX2= Channel 2 transmit

**Note**

*The signals marked with an asterisk symbol (*) are not supported on the conga-XAF.*

**Table 23 FDC Signal Descriptions (not supported)**

| Signal | Description of FDC signals (shared with LPT) | I/O | PU/PD | Comment |
|---|---|---|---|---|
| FLPY# | Floppy Interface configuration input | I 3.3V | PU 10K | Not supported |
| RES | N.C. | N.A. | | Not available |
| DENSEL | Density select: low = 250/300Kb/s high = 500/1000Kb/s | O 5V | | |
| INDEX# | Index signal | I 5V | | |
| TRK0# | Track signal | I 5V | | |
| WP# | Write protect signal | I 5V | | |
| RDATA# | Raw data read | I 5V | | |
| DSKCHG# | Disk change | I 5V | | |
| HDSEL# | Head select | O 5V | | |
| DIR# | Direction | O 5V | | |
| STEP# | Motor step | O 5V | | |
| DRV | Drive select | O 5V | | |
| MOT# | Motor select | O 5V | | |
| WDATA# | Raw write data | O 5V | | |
| WGATE# | Write enable | O 5V | | |

**Table 24 Floppy Support Mode Pinout (not supported)**

| Floppy Support Mode Pinout | | | |
|---|---|---|---|
| Pin | Signal | Pin | Signal |
| 51 | FLPY# (*) | 52 | RESERVED |
| 53 | VCC | 54 | GND |
| 55 | RESERVED | 56 | DENSEL |
| 57 | RESERVED | 58 | RESERVED |
| 59 | IRRX | 60 | HDSEL# |
| 61 | IRTX | 62 | RESERVED |
| 63 | RXD2 | 64 | DIR# |
| 65 | GND | 66 | GND |
| 67 | RTS2# | 68 | RESERVED |
| 69 | DTR2# | 70 | STEP# |
| 71 | DCD2# | 72 | DSKCHG# |
| 73 | DSR2# | 74 | RDATA# |
| 75 | CTS2# | 76 | WP# |
| 77 | TXD2 | 78 | TRK0# |
| 79 | RI2# | 80 | INDEX# |
| 81 | VCC | 82 | VCC |
| 83 | RXD1 | 84 | DRV |
| 85 | RTS1# | 86 | MOT |
| 87 | DTR1# | 88 | WDATA# |
| 89 | DCD1# | 90 | WGATE# |
| 91 | DSR1# | 92 | MSCLK |
| 93 | CTS1# | 94 | MSDAT |
| 95 | TXD1 | 96 | KBCLK |
| 97 | RI1# | 98 | KBDAT |
| 99 | GND | 100 | GND |

**Note**

*The signals marked with an asterisk symbol (*) are not supported on the conga-XAF.*

### Table 25 LPT Signal Descriptions

| Signal | Description of LPT signals (shared with FDC) | I/O | PU/PD | Comment |
|---|---|---|---|---|
| LPT | LPT Interface configuration input | I 3.3V | PU 10K | Not supported, always set to LPT mode |
| STB# | Strobe signal | O 3.3V | PU 100K | |
| AFD# | Automatic feed | O 3.3V | PU 100K | |
| PD0 | Data bus D0 | I/O 3.3V | PU 100K | 5V tolerant input |
| PD1 | Data bus D1 | I/O 3.3V | PU 100K | 5V tolerant input |
| PD2 | Data bus D2 | I/O 3.3V | PU 100K | 5V tolerant input |
| PD3 | Data bus D3 | I/O 3.3V | PU 100K | 5V tolerant input |
| PD4 | Data bus D4 | I/O 3.3V | PU 100K | 5V tolerant input |
| PD5 | Data bus D5 | I/O 3.3V | PU 100K | 5V tolerant input |
| PD6 | Data bus D6 | I/O 3.3V | PU 100K | 5V tolerant input |
| PD7 | Data bus D7 | I/O 3.3V | PU 100K | 5V tolerant input |
| ERR# | LPT error | I 3.3V | PU 100K | 5V tolerant input |
| INIT# | Initiate | O 3.3V | PU 100K | |
| SLIN# | Select | O 3.3V | PU 100K | |
| ACK# | Acknowledge | I 3.3V | PU 100K | 5V tolerant input |
| BUSY | Busy | I 3.3V | PU 100K | 5V tolerant input |
| PE | Paper empty | I 3.3V | PU 100K | 5V tolerant input |
| SLCT | Power On | I 3.3V | PU 100K | 5V tolerant input |

### Table 26 LPT Support Mode Pinout

| Parallel Port Mode Pinout | | | |
|---|---|---|---|
| Pin | Signal | Pin | Signal |
| 51 | LPT (*) | 52 | RESERVED |
| 53 | VCC | 54 | GND |
| 55 | STB# | 56 | AFD# |
| 57 | RESERVED | 58 | PD7 |
| 59 | IRRX | 60 | ERR# |
| 61 | IRTX | 62 | PD6 |
| 63 | RXD2 | 64 | INIT# |
| 65 | GND | 66 | GND |
| 67 | RTS2# | 68 | PD5 |
| 69 | DTR2# | 70 | SLIN# |
| 71 | DCD2# | 72 | PD4 |
| 73 | DSR2# | 74 | PD3 |
| 75 | CTS2# | 76 | PD2 |
| 77 | TXD2 | 78 | PD1 |
| 79 | RI2# | 80 | PD0 |
| 81 | VCC | 82 | VCC |
| 83 | RXD1 | 84 | ACK# |
| 85 | RTS1# | 86 | BUSY |
| 87 | DTR1# | 88 | PE |
| 89 | DCD1# | 90 | SLCT |
| 91 | DSR1# | 92 | MSCLK |
| 93 | CTS1# | 94 | MSDAT |
| 95 | TXD1 | 96 | KBCLK |
| 97 | RI1# | 98 | KBDAT |
| 99 | GND | 100 | GND |

**Note**

*The signals marked with an asterisk symbol (*) are not supported on the conga-XAF.*

## 7.6 X4 Connector Signal Descriptions

### Table 27 Signal Descriptions

| Signal | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|
| VCC | Power Supply +5VDC, ±5% | P | | External supply |
| GND | Power Ground | P | | External supply |
| N.C. | Not connected | N.A. | | Do not connect |
| PIDE | Refers to Primary IDE channel | I/O | | |
| SIDE | Refers to Secondary IDE channel | N.C. | | |

### Table 28 IDE Signal Descriptions

| Signal | Description of IDE signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| PIDE_D0..15 | Primary IDE Data bus | I/O 3.3V | | 5V tolerant |
| PIDE_A0..2 | Primary IDE Address bus | O 3.3V | | |
| PIDE_CS1# | Primary IDE chip select channel 0 | O 3.3V | | |
| PIDE_CS3# | Primary IDE chip select channel 1 | O 3.3V | | |
| PIDE_DRQ | Primary IDE DMA request | I 3.3V | | 5V tolerant |
| PIDED_AK# | Primary IDE DMA acknowledge | O 3.3V | | |
| PIDE_RDY | Primary IDE ready | I 3.3V | | 5V tolerant |
| PIDE_IOR# | Primary IDE IO read | O 3.3V | | |
| PIDE_IOW# | Primary IDE IO write | O 3.3V | | |
| PIDE_INTRQ | Primary IDE interrupt request | I 3.3V | | 5V tolerant |
| SIDE_D0..15 | Secondary IDE Data bus | I/O 3.3V | | 5V tolerant |
| SIDE_A0..2 | Secondary IDE Address bus | O 3.3V | | |
| SIDE_CS1# | Secondary IDE chip select channel0 | O 3.3V | | |
| SIDE_CS3# | Secondary IDE chip select channel1 | O 3.3V | | |
| SIDE_DRQ | Secondary IDE DMA request | I 3.3V | | 5V tolerant |
| SIDED_AK# | Secondary IDE DMA acknowledge | O 3.3V | | |
| SIDE_RDY | Secondary IDE ready | I 3.3V | | 5V tolerant |
| SIDE_IOR# | Secondary IDE IO read | O 3.3V | | |
| SIDE_IOW# | Secondary IDE IO write | O 3.3V | | |
| SIDE_INTRQ | Secondary IDE interrupt request | I 3.3V | | 5V tolerant |
| DASP_S | Secondary IDE Drive active | N.C. | | Not supported |
| PDIAG_S | Secondary IDE Master/Slave negotiation | I 3.3V | | 5V tolerant |
| HDRST# | Hard Drive reset | O 3.3V | | |
| CBLID_P# | Primary IDE 80 pin cable detect | I 3.3V | | 5V tolerant |

### Table 29 Ethernet Signal Descriptions

| Signal | Description of Ethernet signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| TXD#, TXD | Ethernet transmit signal pair | O | | Signals for external transformer |
| RXD#, RXD | Ethernet receive signal pair | I | | Signals for external transformer |
| ACTLED# | Ethernet activity LED | O 3.3V | | |
| LILED# | Ethernet link LED | O 3.3V | | |
| SPEEDLED# | Ethernet speed LED, ON at 100Mb/s | O 3.3V | | |

### Table 30 Power Control Signals

| Signal | Description of Power Control signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| PWGIN | Power good input | I | | Also usable as reset input, make low with O.C. to cause reset. |
| 5V_SB | Supply of internal suspend circuit | P | | |
| PS_ON# | Power Save ON | O 5VSB | | |
| PWRBTN# | Power Button | I 5VSB | | Pull low to switch ATX on |

### Table 31 Power Management Signals

| Signal | Description of Power Management signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| RSMRST# | Resume / reset input | I 3.3VSB | | |
| SMBALRT# | System management bus alert input | I 3.3VSB | | |
| BATLOW# | Battery low input | I 3.3VSB | | |
| GPE1# | General purpose power management event input 1 | I 3.3VSB | | |
| GPE2# | General purpose power management event input 2 | I 3.3VSB | | |
| EXTSMI# | System management interrupt input | I 3.3VSB | | |

### Table 32 Miscellaneous Signal Descriptions

| Signal | Description of Miscellaneous signals | I/O | PU/PD | Comment |
|---|---|---|---|---|
| SPEAKER | Speaker output | O 3.3V | | |
| BATT | Battery supply | I (2.0 ... 3.6 V) | | Power for RTC |
| I²CLK | I²C Bus clock | I/O 5V | | |
| I²DAT | I²C Bus Data | I/O 5V | | |
| SMBCLK | SM Bus clock | I/O 3.3V | | |
| SMBDATA | SM Bus Data | I/O 3.3V | | |
| KBINH# | Keyboard inhibit | N.A. | | Not supported |
| OVCR# | Over current detect for USB | I 3.3VSB | PU 10K | Pull low to generate USB overcurrent event for OS |
| ROMKBCS# | Do not connect | N.A. | | Not available |
| EXT_PRG | Do not connect | N.A. | | Not available |
| GPCS# | General purpose chip select | N.C. | | Not supported |

## 7.7 X4 Connector Pinout

**Table 33 Connector X4 Pinout**

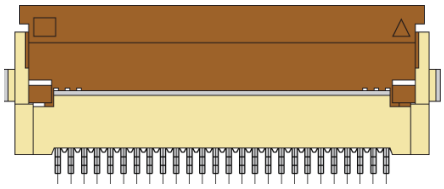
| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | GND | 2 | GND | 51 | SIDE_IOW# | 52 | PIDE_IOR# |
| 3 | 5V_SB | 4 | PWGIN | 53 | SIDE_DRQ | 54 | PIDE_IOW# |
| 5 | PS_ON# | 6 | SPEAKER | 55 | SIDE_D15 | 56 | PIDE_DRQ |
| 7 | PWRBTN# | 8 | BATT | 57 | SIDE_D0 | 58 | PIDE_D15 |
| 9 | KBINH# (*) | 10 | LILED# | 59 | SIDE_D14 | 60 | PIDE_D0 |
| 11 | RSMRST# | 12 | ACTLED# | 61 | SIDE_D1 | 62 | PIDE_D14 |
| 13 | ROMKBCS# (*) | 14 | SPEEDLED# | 63 | SIDE_D13 | 64 | PIDE_D1 |
| 15 | EXT_PRG (*) | 16 | I2CLK | 65 | GND | 66 | GND |
| 17 | VCC | 18 | VCC | 67 | SIDE_D2 | 68 | PIDE_D13 |
| 19 | OVCR# | 20 | GPCS# (*) | 69 | SIDE_D12 | 70 | PIDE_D2 |
| 21 | EXTSMI# | 22 | I2DAT | 71 | SIDE_D3 | 72 | PIDE_D12 |
| 23 | SMBCLK | 24 | SMBDATA | 73 | SIDE_D11 | 74 | PIDE_D3 |
| 25 | SIDE_CS3# | 26 | SMBALRT# | 75 | SIDE_D4 | 76 | PIDE_D11 |
| 27 | SIDE_CS1# | 28 | DASP_S (*) | 77 | SIDE_D10 | 78 | PIDE_D4 |
| 29 | SIDE_A2 | 30 | PIDE_CS3# | 79 | SIDE_D5 | 80 | PIDE_D10 |
| 31 | SIDE_A0 | 32 | PIDE_CS1# | 81 | VCC | 82 | VCC |
| 33 | GND | 34 | GND | 83 | SIDE_D9 | 84 | PIDE_D5 |
| 35 | PDIAG_S | 36 | PIDE_A2 | 85 | SIDE_D6 | 86 | PIDE_D9 |
| 37 | SIDE_A1 | 38 | PIDE_A0 | 87 | SIDE_D8 | 88 | PIDE_D6 |
| 39 | SIDE_INTRQ | 40 | PIDE_A1 | 89 | GPE2# | 90 | CBLID_P# |
| 41 | BATLOW# | 42 | GPE1# | 91 | RXD# | 92 | PIDE_D8 |
| 43 | SIDE_AK# | 44 | PIDE_INTRQ | 93 | RXD | 94 | SIDE_D7 |
| 45 | SIDE_RDY | 46 | PIDE_AK# | 95 | TXD# | 96 | PIDE_D7 |
| 47 | SIDE_IOR# | 48 | PIDE_RDY | 97 | TXD | 98 | HDRST# |
| 49 | VCC | 50 | VCC | 99 | GND | 100 | GND |

**Note**

*The signals marked with an asterisk symbol (*) are not supported on the conga-XAF.*

## 7.8 DDI Connector X6

Connector and flat foil cable information for the DDI connector (X6) located on the bottom side of the conga-XAF.



- Connector type Hirose 0.5mm Pitch Bottom Contact Type
  Order no. FH12-26S-0.5SH
- FFC type 26 positions, 30cm length, 0.5mm pitch both ends opposite sides
  Manufacturer YOUNGSHIN
  Order No. MCAB26x300B05

*The floppy connector X36 on the conga-XEVAL Evaluation Board revision A.x obstructs and compresses the conga-XBRA revision B.1 flat foil cable when the module is mounted on the Evaluation Board. This compression may bend, expose or possibly damage the flat foil cable.*

*congatec therefore recommends the removal of the floppy connector X36 on the conga-XEVAL board revision A.x.*

**Table 34 DDI Pinout Description**

| Pin | Signal | Description | DP Mode | HDMI Mode |
|---|---|---|---|---|
| 1 | GND | Ground | Ground | Ground |
| 2 | DDI_TX0P | DDI Transmitter 0 Positive | ML_Lane 0(p) | TMDS Data 2+ |
| 3 | DDI_TX0N | DDI Transmitter 0 Negative | ML_Lane 0(p) | TMDS Data 2- |
| 4 | GND | Ground | Ground | Ground |
| 5 | DDI_TX1P | DDI Transmitter 1 Positive | ML_Lane 1(p) | TMDS Data 1+ |
| 6 | DDI_TX1N | DDI Transmitter 1 Negative | ML_Lane 1(p) | TMDS Data 1- |
| 7 | GND | Ground | Ground | Ground |
| 8 | DDI_TX2P | DDI Transmitter 2 Positive | ML_Lane 2(p) | TMDS Data 0+ |
| 9 | DDI_TX2N | DDI Transmitter 2 Negative | ML_Lane 2(p) | TMDS Data 0- |
| 10 | GND | Ground | Ground | Ground |
| 11 | DDI_TX3P | DDI Transmitter 3 Positive | ML_Lane 3(p) | TMDS Clock+ |
| 12 | DDI_TX3N | DDI Transmitter 3 Negative | ML_Lane 3(p) | TMDS Clock- |
| 13 | GND | Ground | Ground | Ground |
| 14 | NC | Not connect | Not connect | Not connect |

| Pin | Signal | Description | DP Mode | HDMI Mode |
|---|---|---|---|---|
| 15 | DDI_AUXP | DDI Auxiliary Transmitter Positive | AUX ch(p) | DDC Clock (SCL) |
| 16 | DDI_AUXN | DDI Auxiliary Transmitter Negative | AUX ch(n) | DDC Data (SDA) |
| 17 | GND | Ground | Ground | Ground |
| 18 | DDI_HPD | DDI Hot Plug Detect | Hot Plug Detect | Hot Plug Detect |
| 19 | SMB_DAT | SM Bus Data | SM Bus Data | SM Bus Data |
| 20 | SMB_CLK | SM Bus Clock | SM Bus Clock | SM Bus Clock |
| 21 | GND | Ground | Ground | Ground |
| 22 | GND | Ground | Ground | Ground |
| 23 | GND | Ground | Ground | Ground |
| 24 | VCC_3V3 | Supply Voltage 3.3V | Supply Voltage 3.3V | Supply Voltage 3.3V |
| 25 | VCC_3V3 | Supply Voltage 3.3V | Supply Voltage 3.3V | Supply Voltage 3.3V |
| 26 | VCC_5V0 | Supply Voltage 5.0V | Supply Voltage 5.0V | Supply Voltage 5.0V |

**Note**

*See section 9.4.1 how to configure appropriate mode of DDI (Digital Display Channel 1) supported on the conga-XAF.*

## 7.9 Boot Strap Signals

**Table 35 Signal Descriptions**

| Signal | Pin | Description of Boot Strap Signals | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| PCICLK2 | X1_8 | PCI Clock output | O 3.3V | PU 10K 3.3V | |
| PCICLK3 | X1_3 | PCI Clock output | O 3.3V | PD 10K | |
| PCICLK4 | X1_4 | PCI Clock output | O 3.3V | PD 10K | |
| AC_SDOUT | X2_82 | Audio Serial Data Output to CODEC | O 3.3V | PD 10K | |
| TXD1 | X3_95 | Data transmit for COM1 | O 3.3V | PU 1K 3.3V | |
| RTS1# | X3_85 | Request to send for COM1 | O 3.3V | PD 1K | |
| TXD2 | X3_77 | Data transmit for COM2 | O 3.3V | PU 1K 3.3V | |

**Note**

*The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the module to malfunction and/or cause irreparable damage to the module.*

# 8 System Resources

## 8.1 I/O Address Assignment

The I/O address assignment of the conga-XAF module is functionally identical with a standard PC/AT.

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

### 8.1.1 LPC Bus

On the conga-XAF the PCI Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Bus and not to the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus. In the congatec Embedded BIOS the following I/O address ranges are sent to the LPC Bus:

2Eh – 2Fh

4Eh – 4Fh

60h, 64h

2E8h – 2EFh

2F8h – 2FFh

378h – 37Fh

3E8h – 3EFh

3F8h – 3FFh

778h – 77Fh

A00h – BFFh

Parts of these ranges are not available if the devices of the onboard Super I/O are activated or if an additional Super I/O is used on the carrier board. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

## 8.2 Interrupt Request (IRQ) Lines

**Table 36 IRQ Lines in PIC mode**

| IRQ# | Available | Typical Interrupt Source | Connected to Pin |
|---|---|---|---|
| 0 | No | Counter 0 | Not applicable |
| 1 | No | Keyboard | Not applicable |
| 2 | No | Cascade Interrupt from Slave PIC | Not applicable |
| 3 | Note 2 | Serial Port 1 (COM2) | IRQ3 via SERIRQ or PCI BUS INTx |
| 4 | Note 2 | Serial Port 0 (COM1) | IRQ4 via SERIRQ or PCI BUS INTx |
| 5 | Yes | | IRQ5 via SERIRQ |
| 6 | Yes | | IRQ6 via SERIRQ or PCI BUS INTx |
| 7 | Note 2 | Parallel Port 1 (LPT1) | IRQ7 via SERIRQ or PCI BUS INTx |
| 8 | No | Real-time Clock | Not applicable |
| 9 | No | SCI | Not applicable |
| 10 | Yes | | IRQ10 via SERIRQ or PCI BUS INTx |
| 11 | Yes | | IRQ11 via SERIRQ or PCI BUS INTx |
| 12 | No | PS/2 Mouse | Not applicable |
| 13 | No | Math processor | Not applicable |
| 14 | Note 1 | IDE Controller 0 (IDE0) / Generic | IRQ14 via SERIRQ or PCI BUS INTx |
| 15 | Note 1 | IDE Controller 1 (IDE1) / Generic | IRQ15 via SERIRQ or PCI BUS INTx |

**Notes**

*1. If the SATA interface mode configuration in BIOS setup is NOT set to legacy IDE mode IRQ14 and 15 are free for PCI/LPC bus.*

*2. If the respective onboard Super I/O device is disabled in BIOS, the interrupt can be used for PCI/LPC bus.*

**Table 37 IRQ Lines in APIC mode**

| IRQ# | Available | Typical Interrupt Source | Connected to Pin / Function |
|---|---|---|---|
| 0 | No | Counter 0 | Not applicable |
| 1 | No | Keyboard | Not applicable |
| 2 | No | Cascade Interrupt from Slave PIC | Not applicable |
| 3 | Note 3 | Serial Port 1 (COM2) | IRQ3 via SERIRQ |
| 4 | Note 3 | Serial Port 0 (COM1) | IRQ4 via SERIRQ |
| 5 | Yes | | IRQ5 via SERIRQ |
| 6 | Yes | | IRQ6 via SERIRQ |
| 7 | Note 3 | Parallel Port 1 (LPT1) | IRQ7 via SERIRQ |
| 8 | No | Real-time Clock | Not applicable |
| 9 | No | SCI | Not applicable |
| 10 | Yes | | IRQ10 via SERIRQ |
| 11 | Yes | | IRQ11 via SERIRQ |
| 12 | No | PS/2 Mouse | Not applicable |
| 13 | No | Math processor | Not applicable |
| 14 | Note 1 | IDE Controller 0 (IDE0) / Generic | IRQ14 via SERIRQ |
| 15 | Note 1 | IDE Controller 1 (IDE1) / Generic | IRQ15 via SERIRQ |
| 16 | No | | PIRQA, PCI Express Root Port 0/4/5/6, onboard LAN Controller, PCI Express Port 0 (see Note 2), Main High Definition Audio Controller |
| 17 | No | | PIRQB, PCI Express Root Port 1, PCI Express Port 1 (see Note 2), Addon PATA Controller 0, EHCI Host Controller 0, EHCI Host Controller 1, Chipset IDE Controller 1 (unused) |
| 18 | No | | PIRQC, PCI Express Root Port 2, PCI Express Port 2 (see Note 2), Addon PATA Controller 1, OHCI Host Controller 0, OHCI Host Controller 1, Integrated Graphics Controller |
| 19 | No | | PIRQD, PCI Express Root Port 3, PCI Express Port 3 (see Note 2), Chipset IDE Controller 0 (SATA), HDMI / DisplayPort HDA Controller (for HDMI/DisplayPort integrated audio only) |
| 20 | Yes | | PIRQE, PCI BUS INTA |
| 21 | Yes | | PIRQF, PCI BUS INTB |
| 22 | Yes | | PIRQG, PCI BUS INTC |
| 23 | Yes | | PIRQH, PCI BUS INTD |

In APIC mode, the PCI bus interrupt lines are connected with IRQ 20, 21, 22 and 23.

**Note**

*1. If the SATA interface mode configuration in BIOS setup is NOT set to legacy IDE mode IRQ14 and 15 are free for LPC bus.*

*2. Interrupt used if a single function PCI Express device is connected to the respective PCI Express port.*

*3. If the respective onboard Super I/O device is disabled in BIOS, the interrupt can be used for PCI/LPC bus.*

## 8.3 PCI Configuration Space Map

**Table 38 PCI Configuration Space Map**

| Bus Number (hex) | Device Number (hex) | Function Number (hex) | PCI Interrupt Routing | Description |
|---|---|---|---|---|
| 00h | 00h | 00h | N.A. | Host Bridge |
| 00h | 01h | 00h | Internal | Integrated Graphics Controller (VGA) |
| 00h | 01h | 01h | Internal | HDMI / DisplayPort HDA Controller (for HDMI/DisplayPort integrated audio only) |
| 00h (see Note 1) | 04h | 00h | Internal | PCI Express Root Port 0 |
| 00h (see Note 1) | 05h | 00h | Internal | PCI Express Root Port 1 |
| 00h (see Note 1) | 06h | 00h | Internal | PCI Express Root Port 2 |
| 00h (see Note 1) | 07h | 00h | Internal | PCI Express Root Port 3 |
| 00h | 11h | 00h | Internal | Chipset IDE Controller 0 (SATA) |
| 00h | 12h | 00h | Internal | OHCI Host Controller 0 |
| 00h | 12h | 02h | Internal | EHCI Host Controller 0 |
| 00h | 13h | 00h | Internal | OHCI Host Controller 1 |
| 00h | 13h | 02h | Internal | EHCI Host Controller 1 |
| 00h | 14h | 00h | N.A. | SMBus Host Controller |
| 00h | 14h | 01h | Internal | Chipset IDE Controller 1 (unused) |
| 00h | 14h | 02h | Internal | High Definition Audio Controller |
| 00h | 14h | 03h | N.A. | PCI to LPC Bridge |
| 00h | 14h | 04h | N.A. | PCI to PCI Bridge |
| 00h | 15h | 00h | Internal | PCI Express Root Port 4 |
| 00h | 15h | 01h | Internal | PCI Express Root Port 5 |
| 00h | 15h | 02h | Internal | PCI Express Root Port 6 |
| 00h | 18h | 00h | N.A. | Chipset Configuration Registers |
| 00h | 18h | 01h | N.A. | Chipset Configuration Registers |
| 00h | 18h | 02h | N.A. | Chipset Configuration Registers |
| 00h | 18h | 03h | N.A. | Chipset Configuration Registers |
| 00h | 18h | 04h | N.A. | Chipset Configuration Registers |
| 00h | 18h | 05h | N.A. | Chipset Configuration Registers |
| 00h | 18h | 06h | N.A. | Chipset Configuration Registers |
| 00h | 18h | 07h | N.A. | Chipset Configuration Registers |
| 01h (see Note 2) | 00h | 00h | Internal | PCI Express Port 0 |
| 02h (see Note 2) | 00h | 00h | Internal | PCI Express Port 1 |
| 03h (see Note 2) | 00h | 00h | Internal | PCI Express Port 2 |
| 04h (see Note 2) | 00h | 00h | Internal | PCI Express Port 3 |
| 05h (see Note 2) | 03h | 00h | INTA-INTD | PCI Bus Slot 1 |
| 05h (see Note 2) | 04h | 00h | INTA-INTD | PCI Bus Slot 2 |
| 05h (see Note 2) | 05h | 00h | INTA-INTD | PCI Bus Slot 3 |
| 05h (see Note 2) | 06h | 00h | INTA-INTD | PCI Bus Slot 4 |

| | | | | |
|---|---|---|---|---|
| 06h (see Note 2) | 00h | 00h | Internal | Onboard LAN Controller |
| 07h (see Note 2) | 00h | 00h | Internal | Addon PATA Controller 0 |
| 08h (see Note 2) | 00h | 00h | Internal | Addon PATA Controller 1 |

**Note**

*1. The PCI Express Ports are only visible if the PCI Express Port is set to "Enabled" in the BIOS setup program and a device is attached to the corresponding PCI Express port on the carrier board.*

*2. The above table represents a case when a single function PCI/PCIe device is connected to all possible slots on carrier board. The given bus numbers will change based on the actual configuration of the hardware .*

## 8.4 PCI Interrupt Routing Map

**Table 39 PCI Interrupt Routing Map**

| PIRQ | PCI BUS INT Line [1] | APIC Mode IRQ | VGA | HDA (HDMI / DP) | OHCI 0 | OHCI 1 | EHCI0 | EHCI1 | IDE0 (SATA) | IDE1 (not used) | HDA (Main) | PATA0 | PATA1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | 16 | | | | | | | | | x | | |
| B | | 17 | | | | | x | x | | x | | x | |
| C | | 18 | x | | x | x | | | | | | | x |
| D | | 19 | | x | | | | | x | | | | |
| E | INTA | 20 | | | | | | | | | | | |
| F | INTB | 21 | | | | | | | | | | | |
| G | INTC | 22 | | | | | | | | | | | |
| H | INTD | 23 | | | | | | | | | | | |

**Table 39 PCI Interrupt Routing Map (continued)**

| PIRQ | PCI-EX Root Port 0 | PCI-EX Root Port 1 | PCI-EX Root Port 2 | PCI-EX Root Port 3 | PCI-EX Root Port 4 | PCI-EX Root Port 5 | PCI-EX Root Port 6 | PCI-EX Port 0 | PCI-EX Port 1 | PCI-EX Port 2 | PCI-EX Port 3 | LAN |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | x | | | | x | x | x | x [2] | x [5] | x [4] | x [3] | x |
| B | | x | | | | | | x [3] | x [2] | x [5] | x [4] | |
| C | | | x | | | | | x [4] | x [3] | x [2] | x [5] | |
| D | | | | x | | | | x [5] | x [4] | x [3] | x [2] | |
| E | | | | | | | | | | | | |
| F | | | | | | | | | | | | |
| G | | | | | | | | | | | | |
| H | | | | | | | | | | | | |

**Note**

*[1] These interrupts are available for external devices/slots via the X1 connector.*
*[2] Interrupt used by single function PCI Express devices (INTA).*
*[3] Interrupt used by multifunction PCI Express devices (INTB).*
*[4] Interrupt used by multifunction PCI Express devices (INTC).*
*[5] Interrupt used by multifunction PCI Express devices (INTD).*

## 8.5 PCI Bus Masters

The conga-XAF supports 4 external PCI Bus Masters. There are no limitations in connecting bus master PCI devices.

**Note**

*If there are two devices connected to the same PCI REQ/GNT pair and they are transferring data at the same time then the latency time of these shared PCI devices can not be guaranteed.*

## 8.6 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

## 8.7 SM Bus

System Management (SM) bus signals are connected to the AMD Chipset and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

# 9 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

## 9.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> key during POST.

### 9.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used, a selection will be displayed immediately after POST allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

## 9.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

| Main | Advanced | Boot | Security | Save & Exit |
|---|---|---|---|---|

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

**Note**

*Entries in the option column that are displayed in bold print indicate BIOS default values.*

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

| Key | Description |
|---|---|
| ← → Left/Right | Select a setup menu (e.g. Main, Boot, Exit). |
| ↑ ↓ Up/Down | Select a setup item or sub menu. |
| + - Plus/Minus | Change the field value of a particular setup item. |
| Tab | Select setup fields (e.g. in date and time). |
| F1 | Display General Help screen. |
| F2 | Load previous settings. |
| F9 | Load optimal default settings. |
| F10 | Save changes and exit setup. |
| ESC | Discard changes and exit setup. |
| ENTER | Display options of a particular setup item or enter submenu. |

## 9.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab.

The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

| Feature | Options | Description |
|---|---|---|
| **BIOS Information** | | |
| Main BIOS Version | no option | Displays the main BIOS version. |
| OEM BIOS Version | no option | Displays the additional OEM BIOS version. |
| Build Date | no option | Displays the date the BIOS was built. |
| **Board Information** | | |
| Product Revision | no option | Displays the hardware revision of the board. |
| Serial Number | no option | Displays the serial number of the board. |
| BC Firmware Rev. | no option | Displays the revision of the congatec board controller. |
| MAC Address | no option | Displays the MAC address of the onboard ethernet controller. |
| Boot Counter | no option | Displays the number of boot-ups. (max. 16777215). |
| Running Time | no option | Displays the time the board is running [in hours max. 65535]. |
| **Memory Information** | | |
| Total Memory | no option | Displays amount of installed memory. |
| Memory Clock | no option | Displays current memory clock. |
| **CPU Information** | no option | Displays CPU type and feature information. |
| System Date | Day of week, month/day/year | Specifies the current system date.<br>*Note: The date is in month-day-year format.* |
| System Time | Hour:Minute:Second | Specifies the current system time.<br>*Note: The time is in 24-hour format.* |

## 9.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

| Main | Advanced | Boot | Security | Save & Exit |
|---|---|---|---|---|
| | Graphics Configuration | | | |
| | Watchdog Configuration | | | |
| | PCI & PCI Express Configuration | | | |
| | ACPI Configuration | | | |
| | RTC Wake Settings | | | |
| | Trusted Computing Configuration | | | |
| | CPU Configuration | | | |
| | Chipset Configuration | | | |
| | Hardware Health Monitoring | | | |
| | SATA/PATA Configuration | | | |
| | USB Configuration | | | |
| | Super I/O Configuration | | | |
| | Serial Port Console Redirection | | | |

### 9.4.1 Graphics Configuration Submenu

| Feature | Options | Description |
|---|---|---|
| Primary Graphics Device | IGD<br>**PCI/PCIe** | Select primary graphics adapter to be used during boot up.<br>IGD: Internal Graphics Device<br>PCI/PCIe: Try to use external standard PCI Express or PCI Graphics Device. If not present, IGD is used. |
| Integrated Graphics Device | **Auto Configuration**<br>Disabled<br>Manual Configuration | Deactivate IGD or select frame buffer configuration mode.<br>In auto mode, the frame buffer size will be defined based on the amount of physical memory present. |
| IGD Frame buffer Size | 32M<br>64M<br>128M<br>**256M**<br>512M | Only visible if IGD is set to manual configuration.<br>Set fixed graphics frame buffer size for IGD. The graphics driver might allocate additional memory. |
| Display Channel 0 Output | **LVDS**<br>Disabled | Define output mode and connection of the integrated digital display channel 0. |
| Display Channel 1 Output | **Display Port**<br>HDMI<br>Disabled | Define output mode and connection of the integrated digital display channel 1.<br>*Note: The different output options require different, additional hardware support. Thus not all options can actually work on the same board variant.* |
| IGD Boot Display Device | **Auto**<br>CRT Only<br>Display Channel 0<br>Display Channel 1<br>CRT + Display Channel 0<br>CRT + Display Channel 1<br>Display Channel 0 + 1 | Select the IGD display device(s) used for boot up. |
| Always Try Auto Panel Detect | **No**<br>Yes | If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the LVDS flat panel output. Only if no external EDID data set can be found, the data set selected under 'Local Flat Panel Type' will be used as fallback data set. |
| Local Flat Panel Type | **Auto**<br>VGA 640x480 1x18 (002h)<br>VGA 640x480 1x18 (013h)<br>WVGA 800x480 1x24 (01Bh)<br>SVGA 800x600 1x18 (01Ah)<br>XGA 1024x768 1x18 (006h)<br>XGA 1024x768 2x18 (007h)<br>XGA 1024x768 1x24 (008h)<br>XGA 1024x768 2x24 (012h)<br>WXGA 1280x768 1x24 (01Ch)<br>SXGA 1280x1024 2x24 (00Ah)<br>SXGA 1280x1024 2x24 (018h)<br>UXGA 1600x1200 2x24 (00Ch)<br>HD 1920x1080 2x24 (01Dh)<br>WUXGA 1920x1200 2x18 (015h)<br>WUXGA 1920x1200 2x24 (00Dh)<br>Customized EDID™ 1<br>Customized EDID™ 2<br>Customized EDID™ 3 | Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel.<br>Auto detection is performed by reading an EDID data set via the video I²C bus.<br>The number in brackets specifies the congatec internal number of the respective panel data set.<br>*Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.* |
| Backlight Inverter Type | **None**<br>PWM<br>I2C<br>PWM (no ACPI) | Select the type of backlight inverter used.<br>PWM = Use IGD PWM signal.<br>I2C = Use I2C backlight inverter device connected to the video I²C bus. |

| Feature | Options | Description |
|---|---|---|
| | | PWM (no ACPI) = Use IGD PWM signal; no ACPI interface provided. |
| PWM Inverter Frequency (Hz) | **200**-40000 | Only visible if Backlight Inverter Type is set to PWM. Set the PWM inverter frequency in hertz. |
| Backlight Setting | 0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%** | Actual backlight value in percent of the maximum setting. |
| Inhibit Backlight | **No**<br>Permanent<br>Until End Of POST | Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently. |
| Invert Backlight Setting | **No**<br>Yes | Allow to invert backlight setting values if required for the actual backlight hardware controller. |
| LVDS SSC | **Disabled**<br>Enabled | Enable or disable LVDS spread spectrum clock modulation. |
| SSC Modulation Frequency | **30kHz**<br>35kHz<br>40kHz | Select the LVDS SSC modulation frequency. |
| SSC Modulation Percentage | **0.25%**, 0.50%, 0.75%, 1.00%, 1.25%, 1.50%, 1.75% | Select the LVDS SSC modulation percentage. |

### 9.4.2 Watchdog Configuration Submenu

| Feature | Options | Description |
|---|---|---|
| POST Watchdog | **Disabled**<br>30sec<br>1min<br>2min<br>5min<br>10min<br>30min | Select the timeout value for the POST watchdog.<br><br>The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset. |
| Stop Watchdog For User Interaction | No<br>**Yes** | Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion. |
| Runtime Watchdog | **Disabled**<br>One-time Trigger<br>Single Event<br>Repeated Event | Selects the operating mode of the runtime watchdog.<br>This watchdog will be initialized just before the operating system starts booting.<br>If set to '*One-time Trigger'* the watchdog will be disabled after the first trigger.<br>If set to *'Single Event'*, every stage will be executed only once, then the watchdog will be disabled.<br>If set to *'Repeated Event'* the last stage will be executed repeatedly until a reset occurs. |
| Delay | **Disabled**<br>10sec<br>30sec<br>1min<br>2min<br>5min<br>10min<br>30min | Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load. |
| Event 1 | NMI<br>ACPI Event<br>**Reset**<br>Power Button | Selects the type of event that will be generated when timeout 1 is reached. For more information about *ACPI Event* see note below. |

| Feature | Options | Description |
|---|---|---|
| Event 2 | **Disabled**<br>NMI<br>ACPI Event<br>Reset<br>Power Button | Selects the type of event that will be generated when timeout 2 is reached. |
| Event 3 | **Disabled**<br>NMI<br>ACPI Event<br>Reset<br>Power Button | Selects the type of event that will be generated when timeout 3 is reached. |
| Timeout 1 | 1sec<br>2sec<br>5sec<br>10sec<br>**30sec**<br>1min<br>2min<br>5min<br>10min<br>30min | Selects the timeout value for the first stage watchdog event. |
| Timeout 2 | see above | Selects the timeout value for the second stage watchdog event. |
| Timeout 3 | see above | Selects the timeout value for the third stage watchdog event. |
| Watchdog ACPI Event | **Shutdown**<br>Restart | Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart. |

**Note**

*In ACPI mode it is not possible for a “Watchdog ACPI Event” handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:*

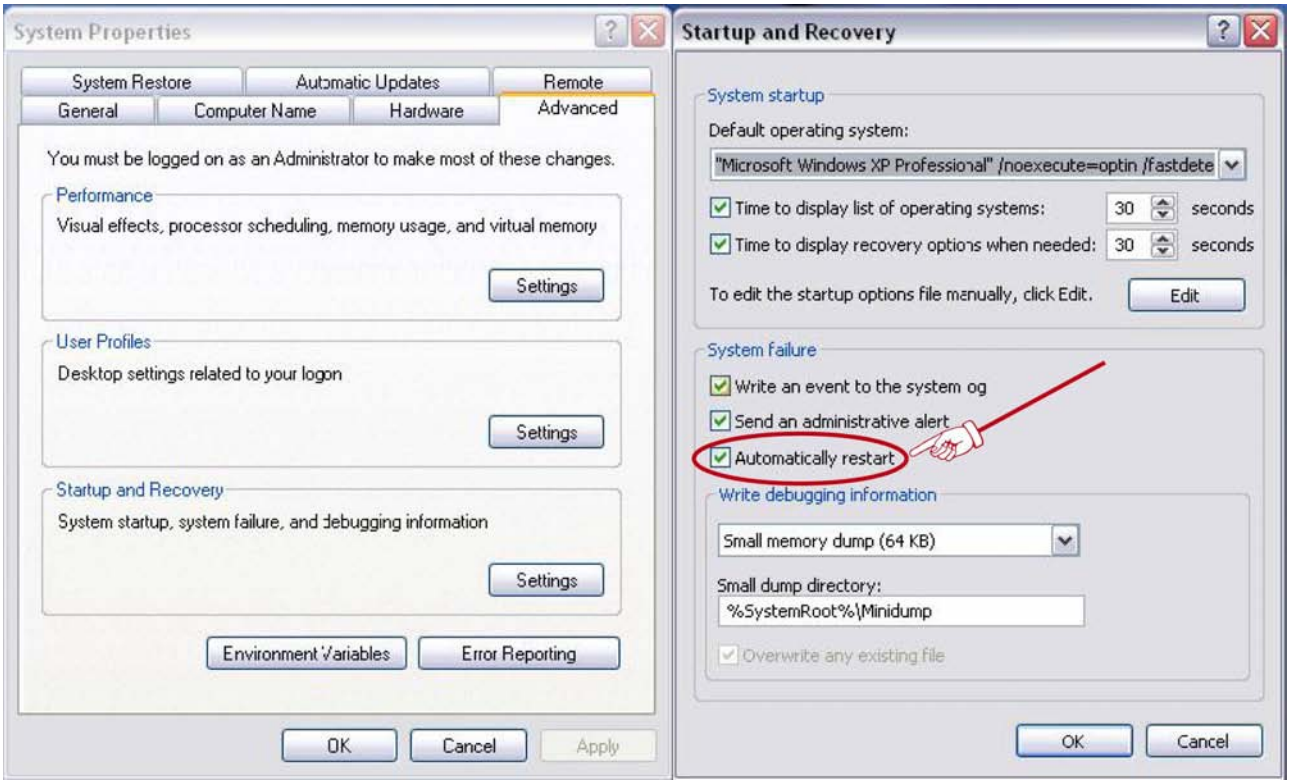
*For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.*

*For Restart: An ACPI fatal error is reported to the OS.*

*It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP/2000 there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very brief blue-screen the system will restart.*

*You can enable this setting by going to the “System Properties” dialog box and choosing the “Advanced” tab. Once there choose the “Settings” button for the “Startup and Recovery” section. This will open the “Startup and Recovery” dialog box. In this dialog box under “System failure” there are three check boxes that define what Windows will do when a fatal error has been detected. In order to ensure that the system restarts after a 'Watchdog ACPI Event” that is set to 'Restart', you must make sure that the check box for the selection “Automatically restart” has been checked. If this option is not selected then Windows will remain at a blue-screen after a 'Watchdog ACPI Event” that has been configured for 'Restart' has been generated. Below is a Windows screen-shot showing the proper configuration.*

# Win XP Watchdog ACPI Event restart configuration



### 9.4.3 PCI & PCI Express Configuration Submenu

| Feature | Options | Description |
|---|---|---|
| PCI ROM Priority | Legacy ROM<br>**EFI Compatible ROM** | Specify which PCI option ROM to launch in case that multiple option ROMs (legacy and EFI compatible) are present. |
| Launch PXE Option ROM | **Disabled**<br>Enabled | Enable or disable start of PXE option ROMs for external legacy network devices. |
| Launch Storage Option ROM | Disabled<br>**Enabled** | Enable or disable start of option ROMs for legacy mass storage devices. |
| PCI Settings | | |
| PCI Latency Timer | **32,** 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks | Select value to be programmed into PCI latency timer register. |
| VGA Palette Snoop | **Disabled**<br>Enabled | Enable or disable VGA palette registers snooping. |
| PERR# Generation | **Disabled**<br>Enabled | Enable or disable PCI device SERR# generation. |
| SERR# Generation | **Disabled**<br>Enabled | Enable or disable PCI device SERR# generation. |
| ►PIRQ Routing | submenu | Opens the PIRQ routing submenu. |
| PCI Express Device & Link Settings | | |
| Relaxed Ordering | **Disabled**<br>Enabled | Enable or disable PCI Express device relaxed ordering. |
| Extended Tag | **Disabled**<br>Enabled | If enabled a device may use an 8-bit tag filed as a requester. |
| No Snoop | Disabled<br>**Enabled** | Enable or disable PCI Express device 'No Snoop' option. |
| Maximum Payload | **Auto**<br>128 Bytes<br>256 Bytes<br>512 Bytes<br>1024 Bytes<br>2048 Bytes<br>4096 Bytes | Set maximum payload of PCI Express devices or allow system BIOS to select the value. |
| Maximum Read Request | **Auto**<br>128 Bytes<br>256 Bytes<br>512 Bytes<br>1024 Bytes<br>2048 Bytes<br>4096 Bytes | Set maximum read request size of PCI Express devices or allow system BIOS to select the value. |
| Extended Synch | **Disabled**<br>Enabled | If enabled, the generation of extended PCI Express synchronization patterns is allowed. |

#### 9.4.3.1 PIRQ Routing Submenu

| Feature | Options | Description |
|---|---|---|
| PIRQA | **Auto**<br>IRQ3<br>IRQ4<br>IRQ6<br>IRQ7<br>IRQ10<br>IRQ11<br>IRQ14<br>IRQ15 | Set interrupt for selected PIRQ. Refer to board's resource list of devices connected to the respective PIRQ.<br>*Note: These settings will only be effective while operating in PIC (non IOAPIC) interrupt mode.* |
| PIRQB | See above | See above |
| PIRQC | See above | See above |
| PIRQD | See above | See above |
| PIRQE (PCI INTA) | See above | See above |
| PIRQF (PCI INTA) | See above | See above |
| PIRQG (PCI INTA) | See above | See above |
| PIRQH (PCI INTA) | See above | See above |

### 9.4.4 ACPI Configuration Submenu

| Feature | Options | Description |
|---|---|---|
| Hibernation Support | Disabled<br>**Enabled** | Enable or disable system ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems. |
| ACPI Sleep State | Suspend Disabled<br>**S3 (Suspend to RAM)** | Select the state used for ACPI system sleep/suspend. |
| S3 Video Repost | **Disabled**<br>Enabled | Enable or disable video BIOS re-post on S3 resume. Required by some operating systems. |
| USB Device Wakeup From S3 or S4 | Disabled<br>**Enabled** | Enable or disable USB device wakeup support from S3 or S4. Additional operating systems may be required as well. |
| Active Trip Point | **Disabled**, 20, 30, 40, 50, 60, 70, 80, 90, 95°C | Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off. |
| Passive Trip Point | **Disabled**, 60, 70, 80, 90, 95°C | Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling. |
| LID Button Support | **Disabled**<br>Enabled | Configure XTX GPE1 to act as ACPI LID button. |

### 9.4.5 RTC Wake Settings Submenu

| Feature | Options | Description |
|---|---|---|
| Wake System At Fixed Time | **Disabled**<br>Enabled | Enable system to wake from S5 using RTC alarm. |
| Wake up hour | | Specify wake up hour. |
| Wake up minute | | Specify wake up minute. |
| Wake up second | | Specify wake up second. |

### 9.4.6 Trusted Computing Configuration Submenu

| Feature | Options | Description |
|---|---|---|
| TPM Support | **Disabled**<br>Enabled | Enable or disable TPM support. System reset is required after change. |
| TPM State | **Disabled**<br>Enabled | Enable or disable TPM chip.<br>*Note: System might restart several times during POST to acquire target state.* |
| Pending TPM Operation | **None,**<br>Enable Take Ownership,<br>Disable Take Ownership,<br>TPM Clear | Perform selected TPM chip operation.<br>*Note: System might restart several times during POST to perform selected operation.* |

**Note**

*This submenu is visible only if the optional TPM chip is implemented. By default, the TPM chip is not implemented.*

### 9.4.7 CPU Configuration Submenu

| Feature | Options | Description |
|---|---|---|
| Limit CPUID Maximum | **Disabled**<br>Enabled | When **enabled**, the processor will limit the maximum CPUID input value to **03h** when queried, even if the processor supports a higher CPUID input value. When **disabled**, the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value. |
| AMD PowerNow! Support | Disabled<br>**Enabled** | Enable or disable support for AMD PowerNow! Technology. Allows operating systems to control CPU performance states. |
| Maximum OS P-State | **P-State 0**<br>P-State 1<br>P-State 2<br>P-State 3<br>P-State 4 | Select the maximum CPU performance state the operating system should support. Higher numbers mean lower performance. P-state 0 is the highest performance state. |
| Maximum Power Up P-State | **P-State 0**<br>P-State 1<br>P-State 2<br>P-State 3<br>P-State 4 | Select the maximum CPU performance state to be set at power up. Higher numbers mean lower performance. P-state 0 is the highest performance state. |
| NX Mode | Disabled<br>**Enabled** | Enable or disable the 'no-execute' page protection function. |
| Virtualization Technology | Disabled<br>**Enabled** | When enabled, a Virtual Machine Manager (VMM) can utilize the integrated hardware virtualization support. |
| C6 Support | **Disabled**<br>Enabled | Enable or disable CPU C6 low power state support. |
| Core Performance Boost | **Auto**<br>Disabled | Controls usage of boosted CPU P-states, i.e. P-states above the standard CPU P-state limit. Availability of boosted P-states depends on CPU type and revision, actual usage on total CPU/GPU power consumption. |

### 9.4.8 Chipset Configuration Submenu

| Feature | Options | Description |
|---|---|---|
| Memory Bank Interleaving | **Disabled**<br>Enabled | Enable or disable memory bank interleaving. |
| Memory Bus Clock | **Auto**<br>400MHz (DDR3-800)<br>533MHz (DDR3-1066) | Select or limit memory frequency. |
| HDA Controller | Auto<br>Disabled<br>**Enabled** | Control activation of the High Definition Audio controller. |
| HDMI/DP Audio Support | Disabled<br>**Enabled** | Enable or disable HDMI/DisplayPort integrated audio support. |
| Onboard LAN | Disabled<br>**Enabled** | Enable or disable the onboard Ethernet controller. |
| Launch Onboard LAN PXE ROM | **Disabled**<br>Enabled | Enable or disable PXE option ROM execution of the onboard Ethernet controller. |
| UMI (NB to SB) PCIE Gen2 Support | Disabled<br>**Enabled** | Enable or disable PCI Express generation 2 link speed for the UMI chipset interface. |
| PCI Express Port 0-3 Configuration | 1 x4 Port<br>2 x2 Ports<br>1 x2 Port + 2 x1 Ports<br>**4 x1 Ports** | Select configuration of PCI Express ports 0-3. |
| PCI Express Port 0 | Disabled<br>**Enabled** | Enable or disable PCI Express port.<br>*Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express devcie is connected.* |
| Link Speed | **Auto**<br>PCIE Gen1<br>PCIE Gen2 | Control link speed for this PCIExpress port. |
| Hotplug Support | **Disabled**<br>Enabled | Enable or disable hotplug support for the respective port. |
| PCI Express Port 1 | Disabled<br>**Enabled** | Enable or disable PCI Express port.<br>*Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express devcie is connected.* |
| Link Speed | **Auto**<br>PCIE Gen1<br>PCIE Gen2 | Control link speed for this PCIExpress port. |
| Hotplug Support | **Disabled**<br>Enabled | Enable or disable hotplug support for the respective port. |
| PCI Express Port 2 | Disabled<br>**Enabled** | Enable or disable PCI Express port.<br>*Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express devcie is connected.* |
| Link Speed | **Auto**<br>PCIE Gen1<br>PCIE Gen2 | Control link speed for this PCIExpress port. |
| Hotplug Support | **Disabled**<br>Enabled | Enable or disable hotplug support for the respective port. |

| Feature | Options | Description |
|---|---|---|
| PCI Express Port 3 | Disabled<br>**Enabled** | Enable or disable PCI Express port.<br>*Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express devcie is connected.* |
| Link Speed | **Auto**<br>PCIE Gen1<br>PCIE Gen2 | Control link speed for this PCIExpress port. |
| Hotplug Support | **Disabled**<br>Enabled | Enable or disable hotplug support for the respective port. |

### 9.4.9 Hardware Health Monitoring Submenu

| Feature | Options | Description |
|---|---|---|
| CPU Temperature | no option | Current CPU temperature. |
| Southbridge Temperature | no option | Current Southbridge temperature. |
| Board Temperature | no option | Current board temperature. |
| DIMM Env. Temperature | no option | Current DIMM environment temperature. |
| 5V Standard | no option | Current 5V input reading. |
| 5V Standby | no option | Current 5V standby input reading. |
| Memory Voltage | no option | Current memory voltage reading. |
| CPU Fan Speed | no option | Current CPU fan speed reading. |

## 9.4.10 SATA/PATA Configuration Submenu

| Feature | Options | Description |
|---|---|---|
| SATA Controller | Disabled<br>**Enabled** | Enable or disable the onboard SATA controller. |
| SATA Interface Mode | **Native IDE**<br>RAID<br>AHCI<br>Legacy IDE | Select onboard SATA controller interface mode. |
| SATA Port 0 | **Enabled**<br>Disabled | Enable or disable selected port. |
| Port Speed | **Auto**<br>Gen1<br>Gen2 | Select SATA speed generation for the selected port. |
| SATA Port 1 | **Enabled**<br>Disabled | Enable or disable selected port. |
| Port Speed | **Auto**<br>Gen1<br>Gen2 | Select SATA speed generation for the selected port. |
| SATA Port 2 | **Enabled**<br>Disabled | Enable or disable selected port. |
| Port Speed | **Auto**<br>Gen1<br>Gen2 | Select SATA speed generation for the selected port. |
| SATA Port 3 | **Enabled**<br>Disabled | Enable or disable selected port. |
| Port Speed | **Auto**<br>Gen1<br>Gen2 | Select SATA speed generation for the selected port. |
| Primary PATA Controller | Disabled<br>**Enabled** | Enable or disable the primary onboard PATA controller. |
| Maximum UDMA Mode | UDMA0<br>UDMA1<br>UDMA2<br>UDMA3<br>UDMA4<br>UDMA5<br>UDMA6 | Allows to limit the UDMA mode that should be supported for drives connected to this controller. |
| Secondary PATA Controller | Disabled<br>**Enabled** | Enable or disable the secondary onboard PATA controller. |
| Maximum UDMA Mode | UDMA0<br>UDMA1<br>UDMA2<br>UDMA3<br>UDMA4<br>UDMA5<br>UDMA6 | Allows to limit the UDMA mode that should be supported for drives connected to this controller. |

## 9.4.11 USB Configuration Submenu

| Feature | Options | Description |
|---|---|---|
| USB Port 0 | Disabled<br>**Enabled** | Enable or disable selected port. |
| USB Port 1 | Disabled<br>**Enabled** | Enable or disable selected port. |
| USB Port 2 | Disabled<br>**Enabled** | Enable or disable selected port. |
| USB Port 3 | Disabled<br>**Enabled** | Enable or disable selected port. |
| USB Port 4 | Disabled<br>**Enabled** | Enable or disable selected port. |
| USB Port 5 | Disabled<br>**Enabled** | Enable or disable selected port. |
| USB Overcurrent Reporting | Disabled<br>**Enabled** | Select whether activation of the USB overcurrent signals results in USB overcurrent register reporting and software event handling as well. |
| Legacy USB Support | **Enabled**<br>Disabled<br>Auto | Enables legacy USB support.<br>Auto option disables legacy support if no USB devices are connected.<br>Disable option will keep USB devices available only for EFI applications and setup. |
| EHCI Hand-off | **Disabled**<br>Enabled | This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver. |
| ►Per-Port Legacy USB Support Control | submenu | Opens the Per-Port Legacy USB Support Control submenu |
| USB Transfer Timeout | 1 sec<br>5sec<br>10 sec<br>**20 sec** | Timeout value for legacy USB control, bulk and interrupt transfers. |
| Device Reset Timeout | 10 sec<br>**20 sec**<br>30 sec<br>40 sec | USB legacy mass storage device start unit command timeout. |
| Device Power-Up Delay Selection | **Auto**<br>Manual | Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port. |
| Device Power-Up Delay Value | **5**<br>1-40 | Actual power-up delay value in seconds. |
| *USB Mass Storage Device Name*<br><br>*(Auto detected USB mass storage devices are listed here dynamically)* | **Auto**<br>Floppy<br>Forced FDD<br>Hard Disk<br>CD-ROM | Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device.<br>*Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.*<br>Select *AUTO* to let the BIOS auto detect the current formatted media.<br>If Floppy is selected then the device will be emulated as a floppy drive.<br>*Forced FDD* allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32.<br>*Hard Disk* allows the device to be emulated as hard disk.<br>*CDROM* assumes the CD.ROM is formatted as bootable media, specified by the 'El Torito' Format Specification. |

#### 9.4.11.1 Per-Port Legacy USB Support Control Submenu

| Feature | Options | Description |
|---|---|---|
| USB0 Port Legacy Support | Disabled<br>**Enabled** | Enable or disable legacy USB support for this port. Enabled is only effective if the port is not disabled by another setting in the USB configuration menu. |
| USB1 Port Legacy Support | See above | See above |
| USB2 Port Legacy Support | See above | See above |
| USB3 Port Legacy Support | See above | See above |
| USB4 Port Legacy Support | See above | See above |
| USB5 Port Legacy Support | See above | See above |

### 9.4.12 Super I/O Configuration Submenu

| Feature | Options | Description |
|---|---|---|
| **Onboard Super IO Configuration** | | |
| Serial Port 0 | Disabled<br>**Enabled** | Enable or disable serial port 0. |
| *Device Settings* | *IO=3F8h; IRQ=4;* | *Fixed configuration of serial port 0 if enabled.* |
| Serial Port 1 | Disabled<br>**Enabled** | Enable or disable serial port 1. |
| *Device Settings* | *IO=2F8h; IRQ=3;* | *Fixed configuration of serial port 1 if enabled.* |
| Parallel Port | Disabled<br>**Enabled** | Enable or disable parallel port. |
| *Device Settings* | *IO=378h; IRQ=7;* | *Fixed configuration of the parallel port if enabled.* |
| Device Mode | **Standard Parallel Mode**<br>EPP Mode<br>ECP Mode<br>EPP Mode & ECP Mode | Set the parallel port mode. |

### 9.4.13 Serial Port Console Redirection

| Feature | Options | Description |
|---|---|---|
| COM0<br>Console Redirection | **Disabled**<br>Enabled | Enable or disable serial port 0 console redirection. |
| ►Console Redirection Settings | submenu | Opens console redirection configuration sub menu. |
| COM1<br>Console Redirection | **Disabled**<br>Enabled | Enable or disable serial port 0 console redirection. |
| ►Console Redirection Settings | submenu | Opens console redirection configuration sub menu. |

### 9.4.13.1 Console Redirection Settings Submenu

| Feature | Options | Description |
|---|---|---|
| Terminal Type | VT100<br>VT100+<br>VT-UTF8<br>**ANSI** | Select terminal type. |
| Baud rate | 9600, 19200, 38400, 57600, **115200** | Select baud rate. |
| Data Bits | 7,<br>**8** | Set number of data bits. |
| Parity | **None**<br>Even<br>Odd<br>Mark<br>Space | Select parity. |
| Stop Bits | **1**<br>2 | Set number of stop bits. |
| Flow Control | **None**<br>Hardware RTS/CTS | Select flow control. |
| Recorder Mode | **Disabled**<br>Enabled | With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data. |
| Resolution 100x31 | **Disabled**<br>Enabled | Enables or disables extended terminal resolution in UEFI environment. |
| Legacy OS Redirection Resolution | **80x24**<br>80x25 | Number of rows and columns supported for legacy OS redirection. |

# 9.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

## 9.5.1 Boot Settings Configuration

| Feature | Options | Description |
|---|---|---|
| Quiet Boot | **Disabled**<br>Enabled | *Disabled* displays normal POST diagnostic messages.<br>*Enabled* displays OEM logo instead of POST messages.<br>*Note: The default OEM logo is a dark screen.* |
| Setup Prompt Timeout | **1**<br>0 - 65535 | Number of seconds to wait for setup activation key.<br>0 means no wait for fastest boot, 65535 means infinite wait. |
| POST/Setup VGA Support | **Disabled**<br>Enabled | Select VGA mode for setup and POST screen. Enables setup and POST screen output support for VGA and WVGA display resolutions. |
| Bootup NumLock State | **On**<br>Off | Select the keyboard numlock state. |
| Enter Setup If No Boot Device | No<br>**Yes** | Select whether the setup menu should be started if no boot device is connected. |
| Enable Popup Boot Menu | No<br>**Yes** | Select whether the popup boot menu can be started. |
| Boot Priority Selection | Device Based<br>**Type Based** | Select between device and type based boot priority lists. The “Device Based” boot priority list allows you to select from a list of currently detected devices only. The “Type Based” boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the “Device Based” boot priority list might change dynamically in cases when devices are physically removed or added to the system. The “Type Based” boot menu is static and can only be changed by the user. |
| 1st, 2nd, 3rd, ...<br>Boot Device<br><br>(Up to 12 boot devices can be prioritized if device based priority list control is selected. If “Type Based” priority list control is enabled only 8 boot devices can be prioritized.) | Disabled<br>SATA 0 Drive<br>SATA 1 Drive<br>SATA 2 Drive<br>SATA 3 Drive<br>Primary PATA Master<br>Primary PATA Slave<br>Secondary PATA Master<br>Secondary PATA Slave<br>USB Floppy<br>USB Harddisk<br>USB CDROM<br>Onboard LAN<br>External LAN<br>Other BEV Device<br>OEM BEV Device | This view is only available when in the default “Type Based” mode.<br><br>When in “Device Based” mode you will only see the devices that are currently connected to the system. |
| Power Loss Control | **Remain Off**<br>Turn On<br>Last State | Specifies the mode of operation if an AC power loss occurs.<br>*Remain Off* keeps the power off until the power button is pressed.<br>*Turn On* restores power to the computer.<br>*Last State* restores the previous power state before power loss occurred.<br>*Note: Only works with an ATX type power supply.* |
| AT Shutdown Mode | **System Reboot**<br>Hot S5 | Determines the behavior of an AT-powered system after a shutdown. |
| System Off Mode | **G3/Mech Off**<br>S5/Soft Off | Define system state after shutdown when a battery system is present. |
| GateA20 Active | **Upon Request** | Gate A20 control. |

| Feature | Options | Description |
|---|---|---|
| | Always | Upon Request = Gate A20 can be disabled using BIOS services.<br>Always = Do not allow disabling Gate A20 |
| Option ROM Messages | **Force BIOS**<br>Keep Current | Set display mode for option ROMs. |
| Interrupt 19 Capture | **Disabled**<br>Enabled | Defines whether option ROMs may trap the INT19h legacy boot vector. |

### Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

## 9.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

### 9.6.1 Security Settings

| Feature | Options | Description |
|---|---|---|
| Administrator Password | enter password | Specifies the setup administrator password. |
| **HDD Security Configuration** | | |
| *List of all detected harddisks supporting the security feature set* | Select device to open device security configuration submenu | |

### 9.6.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

### 9.6.3 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen.

You can display an Save & Exit screen option by highlighting it using the <Arrow> keys.

| Feature | Description |
|---|---|
| Save Changes and Exit | Exit setup menu after saving the changes. The system is only reset if settings have been changed. |
| Discard Changes and Exit | Exit setup menu without saving any changes. |
| Save Changes and Reset | Save changes and reset the system. |
| Discard Changes and Reset | Reset the system without saving any changes. |
| **Save Options** | |
| Save Changes | Save changes made so far to any of the setup options. Stay in setup menu. |
| Discard Changes | Discard changes made so far to any of the setup options. Stay in setup menu. |
| Restore Defaults | Restore default values for all the setup options. |
| **Boot Override** | |
| *List of all boot devices currently detected* | Select device to leave setup menu and boot from the selected device.<br>Only visible and active if Boot Priority Selection setup node is set to “Device Based”. |

# 10 Additional BIOS Features

The conga-XAF uses a congatec/AMI Aptio UEFI firmware that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as XBRAR1xx where XBRA is the congatec internal project name, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

## 10.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” please refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

## 10.2 BIOS Security Features

The BIOS provides a setup administrator password that limits access to the BIOS setup menu.

## 10.3 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to 'lock' and 'unlock' drives using the security password. A 'locked' drive will be detected by the system, but no data can be accessed. Accessing data on a 'locked' drive requires the proper password to 'unlock' the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within five attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

# 11 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

| Specification | Link |
|---|---|
| Low Pin Count Interface Specification, Revision 1.0 (LPC) | http://developer.intel.com/design/chipsets/industry/lpc.htm |
| Universal Serial Bus (USB) Specification, Revision 2.0 | http://www.usb.org/home |
| PCI Specification, Revision 2.2 | http://www.pcisig.com/specifications |
| PCI Express Base Specification, Revision 1.0a | http://www.pcisig.com/specifications |
| Serial ATA Specification, Revision 1.0a | http://www.serialata.org |
| Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003 | http://www.acpi.info |
| Information Technology AT Attachment with Packet Interface -5 (ATA/ATAPI-5) Revision 3, February 29, 2000 | http://www.t13.org |