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the rhythm of embedded computing

XTX™
conga-XLX

AMD Geode™ LX processors with an AMD Geode™ CS5536 companion device

User's Guide

Revision 1.4

Revision History

Revision	Date (dd.mm.yy)	Author	Changes
1.0	20.02.06	GDA	Initial release
1.1	20.09.06	GDA	Updated Power Consumption Tables in section 1.5. Added CMOS backup battery information. Updated heatspreader drawing. Added section 5.3.1 Simplified Overview of BIOS Setup Data Backup. Added Note and Caution statement found below PCI Signal Description Table 4 in section 6.1. Updated BIOS Setup Description section section 8.
1.2	06.08.07	GDA	Added Electrostatic Sensitive Device information. Changed all audio codec references to ALC203. ALC658 is no longer used on conga-XLX. Added section 1.4 Electrical Characteristics and 1.4.1 Supply Voltage Ripple. Added description for PP_TPM pin 60 on X2 connector. Added information about center mounting hole to 'Caution' statement in section 3 Heatspreader. Added information to 'Caution' statement in section 4.1.4 Onboard Generated Supply Voltage. Added note about floppy cable to section 4.3.6 Parallel Port/Floppy Interface. Added section 5.5 'congatec Battery Management Interface'. Added LVDS signal mapping to table 17 LVDS Interface Pinout. Updated section 7 System Resources and section 8 BIOS Setup Description.
1.3	12.11.09	GDA	Improved section 1.4.1 and added section 1.4.2. Updated power consumption numbers in section 1.5. Removed TMP support. Added 'Note' to section 6 'Signal Descriptions and Pinout Tables'.
1.4	09.04.18	BEU	Changed maximum torque rating for heatspreader screws in section 3.1 “Heatspreader Dimensions” and added a caution statement. Removed both SATA ports and second IDE port from all sections. Updated section “Electrostatic Sensitive Device”.

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-XLX. It is one of four documents that should be referred to when designing an XTX™ application. The other reference documents that should be used include the following:

XTX™ Design Guide
ETX® Design Guide
XTX™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHZ	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
T.O.M.	Top of memory = max. DRAM installed
SATA	Serial ATA
PATA	Parallel ATA
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

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ETX® Concept and XTX™ Extension

The ETX® concept is an off the shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. ETX® modules have a standardized form factor of 95mm x 114mm and have specified pinouts on the four system connectors that remain the same regardless of the vendor. The ETX® module provides most of the functional requirements for any application. These functions include, but are not limited to, graphics, sound, keyboard/mouse, IDE, Ethernet, parallel, serial and USB ports. Four ruggedized connectors provide the carrier board interface and carry all the I/O signals to and from the ETX® module.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly ETX® applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class ETX® modules. Simply unplug one module and replace it with another, no redesign is necessary.

XTX™ is an expansion and continuation of the well-established and highly successful ETX® standard. XTX™ offers the newest I/O technologies on this proven form factor. Now that the ISA bus is being used less and less in modern embedded applications congatec AG offers an array of different features on the X2 connector than those currently found on the ETX® platform. These features include new serial high speed buses such as PCI Express™ and Serial ATA®. All other signals found on connectors X1, X3, and X4 remain the same in accordance to the ETX® standard (Rev. 2.7) and therefore will be completely compatible. If the embedded PC application still requires the ISA bus then an ISA bridge can be implemented on the application specific carrier board or the readily available LPC bus located on the XTX™ module may be used. Contact congatec technical support for details.

Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices. They are enclosed in static shielding bags, and shipped enclosed in secondary packaging (protective packaging). The secondary packaging does not provide electrostatic protection.

Do not remove the device from the static shielding bag or handle it, except at an electrostatic-free workstation. Also, do not ship or store electronic devices near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

Certification

congatec AG is certified to DIN EN ISO 9001:2008 standard.

conga-XLX Options Information

The conga-XLX is currently available in two different optional variants. This user's guide describes both of these options. Below you will find an order table showing the different configurations that are currently offered by congatec AG. Check the table for the Part no./Order no. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Part-No.	057824	084267
CPU	AMD Geode™ LX800 500MHz	AMD Geode™ LX800 500MHz
Cache	128 kByte	128 kByte
SATA	N/A	N/A
USB 2.0	4x	4x
LVDS	Yes	No
TTL	No	Yes
TV-Out	No	Optional (see note below)
Suspend to RAM (S3)	Yes	Yes
AC'97 Digital Audio Interface	Yes	Yes

Note

TV-Out is optional only on the conga-XLX TTL variant. Ask your local congatec representative about ordering information for the conga-XLX with the TV-Out feature.

Contents

1 Specifications 11
1.1 Feature List 11
1.2 Supported Operating Systems 12
1.3 Mechanical Dimensions 12
1.4 Supply Voltage Standard Power 12
1.4.1 Supply Voltage Ripple 13
1.4.2 Rise Time 13
1.5 Power Consumption 13
1.5.1 conga-XLX 500MHz with 128 kByte cache 14
1.5.2 conga-XLX 500MHz with 128 kByte cache 15
1.6 Supply Voltage Battery Power 15
1.6.1 CMOS Battery Power Consumption 15
1.7 Environmental Specifications 16
2 Block Diagram 17
3 Heatspreader 18
3.1 Heatspreader Dimensions 19
4 Connector Subsystems 20
4.1 Connector X1 20
4.1.1 PCI Bus 20
4.1.2 USB 2.0 20
4.1.3 Audio 21
4.1.4 Onboard Generated Supply Voltage 21
4.2 Connector X2 (XTX™ Extension) 21
4.2.1 LPC 21
4.2.2 USB 2.0 21
4.2.3 PCI Express™ 22
4.2.4 ExpressCard™ 22
4.2.5 AC'97 Digital Audio 22
4.2.6 Extended System Management 22
4.3 Connector X3 22
4.3.1 Graphics 22
4.3.2 LCD 22
4.3.3 TV-Out 22
4.3.4 Serial Ports (1 and 2) 23
4.3.5 Serial Infrared Interface 23
4.3.6 Parallel Port/Floppy Interface 23
4.3.7 Keyboard/Mouse 23
4.4 Connector X4 23
4.4.1 IDE 23
4.4.2 Ethernet 23
4.4.3 I²C Bus 400kHz 24
4.4.4 Power Control 24
4.4.5 Power Management 25

5 Additional Features....26
5.1 Watchdog....26
5.2 Onboard Microcontroller....26
5.3 Embedded BIOS....26
5.3.1 Simplified Overview of BIOS Setup Data Backup....27
5.4 congatec Battery Management Interface....28
6 Signal Descriptions and Pinout Tables....29
6.1 X1 Connector Signal Descriptions....30
6.2 Connector X1 Pinout....32
6.3 X2 Connector Signal Descriptions (XTX™ extension)....33
6.4 X2 Connector Pinout....37
6.5 X3 Connector Signal Descriptions....39
6.6 X4 Connector Signal Descriptions....45
6.7 X4 Connector Pinout....47
6.8 Boot Strap Signals....48
7 System Resources....49
7.1 System Memory Map....49
7.2 I/O Address Assignment....50
7.3 Interrupt Request (IRQ) Lines....51
7.4 Direct Memory Access (DMA) Channels....52
7.5 PCI Configuration Space Map....52
7.6 PCI Interrupt Routing Map....53
7.7 PCI Bus Masters....53
7.8 I²C Bus....53
7.9 SM Bus....53
7.10 LPC Bus....53
8 BIOS Setup Description....54
8.1 Starting the BIOS setup program....54
8.1.1 Manufacturer Default Settings....54
8.2 Setup Menu and Navigation....54
8.3 Main Menu....55
8.4 Board Information....55
8.5 Device Configuration....56
8.5.1 Drive Configuration Submenu....57
8.5.2 Graphics Configuration Submenu....58
8.5.3 Cache Configuration Submenu....58
8.5.4 PCI Configuration Submenu....59
8.5.5 I/O Interface Configuration Submenu....60
8.5.6 External Super I/O Configuration Submenu....61
8.5.7 USB Configuration Submenu....62
8.5.8 Watchdog Configuration Submenu....63
8.5.9 Hardware Monitoring Submenu....64
8.5.10 Boot Screen Configuration Submenu....64
8.6 Performance Control....65
8.7 Power Management....66
8.8 Boot Device Priority....68
9 Additional BIOS Features....69

9.1 Updating the BIOS....69
10 Industry Specifications....70

1 Specifications

1.1 Feature List

Table 1 Feature Summary

Form Factor	ETX® standard (Rev. 2.7) with XTX™ extension
Processor	AMD Geode™ LX800 500MHz with 128 kByte cache
Memory	SO-DIMM DDR (up to PC2700) maximum 1-GByte
Chipset	AMD Geode™ CS5536 companion device
Audio	Realtek ALC203 AC'97 Rev. 2.3 compatible.
Ethernet	Realtek RTL8100C
Graphics Options	Similar to GX graphics core but with strong improvements. Unified Memory Architecture (UMA) with a maximum of 16MB hardware frame buffer compression. 2-254MB graphics memory space. • CRT Interface 350 MHz RAMDAC Resolutions up to 1920x1440 @ 85Hz • Flat panel Interface External LVDS Transmitter Supports 1x18Bit TFT configurations Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3) Resolutions 640x480 up to 1024x768 (XGA) Optional direct TTL interface, max. resolution 1024x768 1x18Bit • Motion Video Support Hardware Up- and Downscaling High definition digital video support Alpha blending and color keying • TV Out (optional) External TV encoder Supports component + S-Video Supports HDTV (420p, 720p & 1080i)
Super I/O	Winbond 83627HG
Peripheral Interfaces	• PCI Bus Rev. 2.3 • LPC Bus (no ISA Bus) • 1x EIDE (UDMA-66/100) • 4x USB 2.0 (EHCI) • AC'97 Digital Audio Interface • I²C Bus, Fast Mode (400 kHz) • Floppy (shared with LPT) • LPT (EEP/ECP, shared with floppy) • 2 x COM Ports, TTL Level • 1 x IrDA Port • PS/2 Keyboard, Mouse
BIOS	Based on Insyde XpressROM 1MByte Flash BIOS with congatec Embedded BIOS features
Power Management	ACPI 2.0 compliant with battery support. Also supports Suspend to RAM (S3).

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 7 of this user's guide to determine what options are available on your particular module.

1.2 Supported Operating Systems

The conga-XLX supports the following operating systems.

- Microsoft® Windows® XP/2000
- Microsoft® Windows ®XP Embedded
- Microsoft® Windows® CE 5.0 / 6.0
- Linux
- QNX

1.3 Mechanical Dimensions

- 95.0 mm x 114.0 mm (3.75” x 4.5”)
- Height approx. 12mm (0.4”)

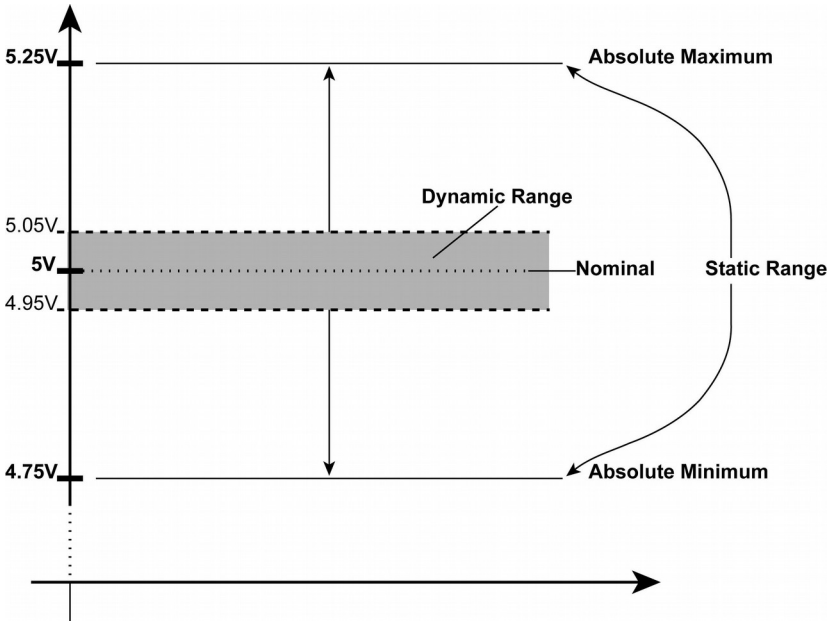
1.4 Supply Voltage Standard Power

Characteristics			Min	Typ	Max	Units	Comment
5V	Voltage	+/-5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	100	mV_{pp}	0-20MHz
	Current	See section 1.5 'Power Consumption' for supply current information.					
5V_SB	Voltage	+/-5%	4.75	5.00	5.25	Vdc	
	Current			250		mA	

1.4.1 Supply Voltage Ripple

- Maximum 100mV peak to peak over a frequency band of 10Hz to 20MHz.

The dynamic range shall not exceed the static range.



1.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum rise time of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

1.5 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The XTX module was mounted into a special carrier board. This carrier board has two Hirose connectors that connect to the corresponding X3 and X4 connectors on the module. The special carrier board does not have any power consuming components mounted on it. It provides one connector for a CRT monitor connection, a PS2 keyboard and mouse connection, and an IDE device connection. The carrier board is powered by a Direct Current (DC) power supply that is set to output 5 Volts and is connected directly to the special carrier board. Additionally, positive and negative sense lines are connected to the carrier board in order to measure the current consumption of the module. This current consumption value is displayed by the DC power supply's readout and this is the value that is recorded as the power consumption measurement. All recorded values are approximate.

All external peripheral devices, such as the hard drive, are externally powered so that they do not influence the power consumption value that is measured for the module. This ensures the value measured reflects the true power consumption of the module

and only the module. A keyboard is used to configure the module and then it is disconnected before the measurement is recorded. If the keyboard remained connected, an additional current consumption of approximately 10 mA is noticed.

Each module was measured while running Windows XP Professional with SP2 (service pack 2) and the "Power Scheme" was set to "Portable/Laptop". The screen resolution was set to 800x600 32bit High Color. The "Performance Control" was set to the BIOS default value "Manual Settings", which is 500MHz CPU clock speed. The conga-XLX was tested while using a swissbit® DDR PC2700 512MB memory module. Using different sizes of RAM will cause slight variances in the measured results. Power consumption values were recorded during the following stages:

Windows XP Professional SP2

- Desktop Idle
- 100% CPU workload *(see note below)*
- Windows Standby *(see note below)*
- Suspend to RAM (requires setup node "Suspend Mode Control" in BIOS to be configured to S3-State (suspend to RAM)).

Note

A software tool was used to stress the CPU to 100% workload.
ACPI OS Standby = S1 = POS = CPU is in sleep mode (internal clocks stopped, no snoops)

1.5.1 conga-XLX 500MHz with 128 kByte cache

With 512MB memory installed

conga-XLX Art. No. 057824 LVDS variant	AMD Geode™ LX800 500MHz with 128 kByte cache Layout Rev. X800LB0 /BIOS Rev. X800R114			
Memory Size	512MB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Standby	Suspend to Ram (S3)
Power consumption (measured in Amperes/Watts)	1.0 A/5 W	1.4 A/7 W	0.8 A/4 W	0.1 A/0.5 W

1.5.2 conga-XLX 500MHz with 128 kByte cache

With 512MB memory installed

conga-XLX Art. No. 084267 TTL variant	AMD Geode™ LX800 500MHz with 128 kByte cache Layout Rev. X800LA0 /BIOS Rev. X800R114			
Memory Size	512MB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Standby	Suspend to Ram (S3)
Power consumption (measured in Amperes/Watts)	**1.0 A/5 W**	**1.4 A/7 W**	**0.9 A/4.5 W**	**0.1 A/0.5 W**

1.6 Supply Voltage Battery Power

- 2.4-3.6V
- Typical 3.0V

1.6.1 CMOS Battery Power Consumption

RTC @ 20ºC	Voltage	Current
Integrated in the AMD Geode™ CS5536 companion device	3V DC	1.53 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

1.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

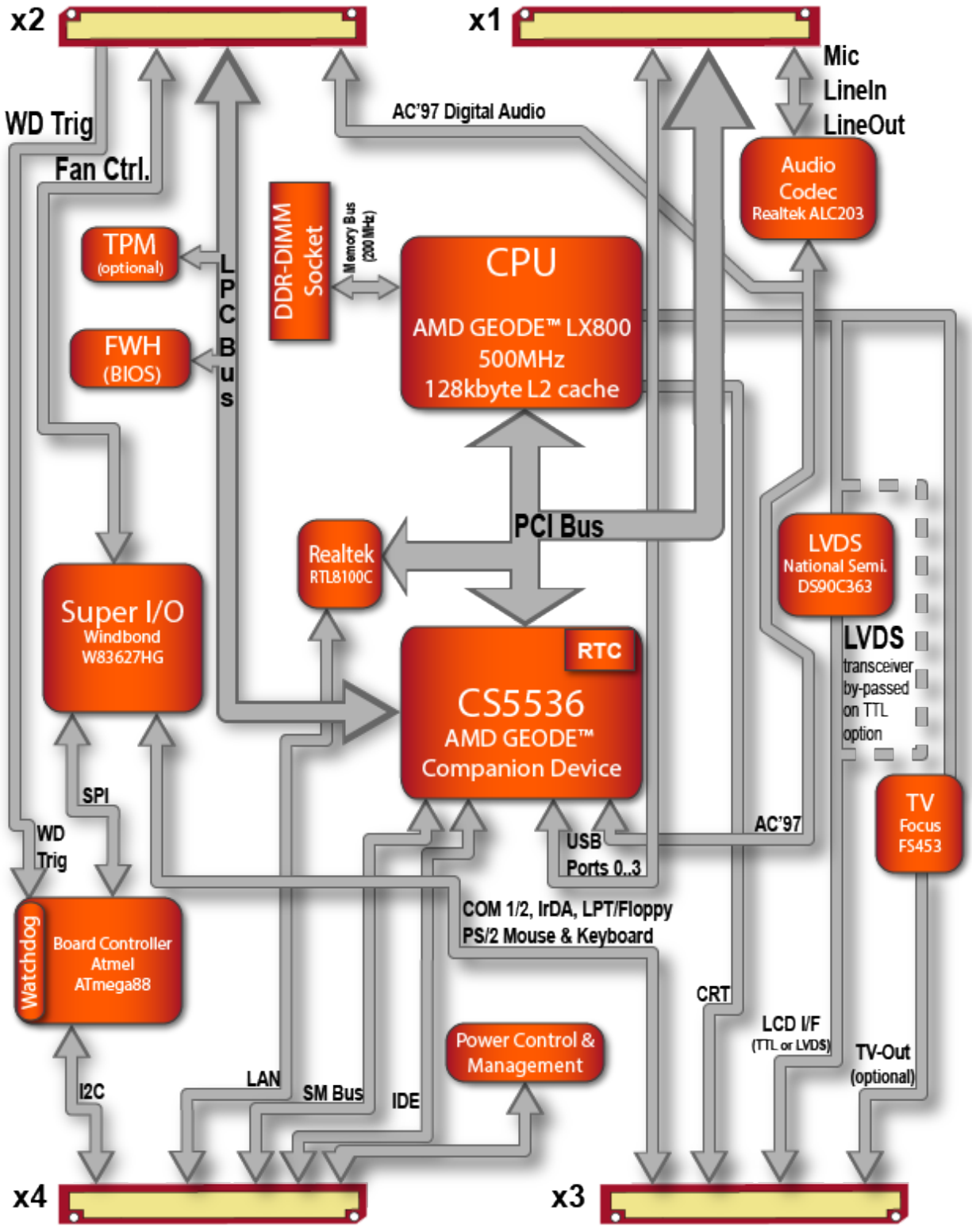
congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.

If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

For more information about operating a congatec module without heatspreader contact congatec technical support.

Humidity specifications are for non-condensing conditions.

2 Block Diagram



3 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module. It is a 2mm thick aluminum plate.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

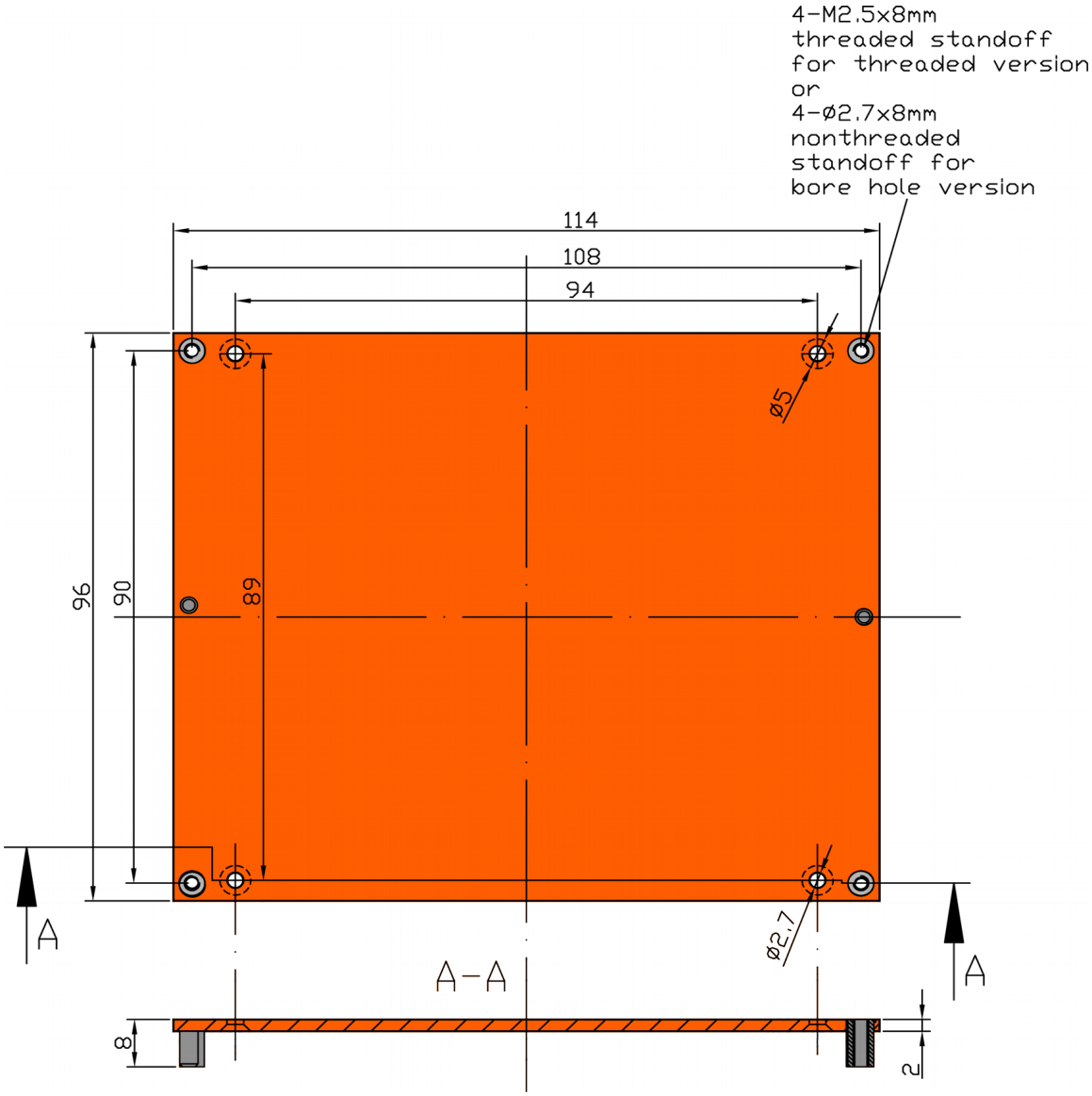
Caution

The center mounting hole on the heatspreader must be used to ensure that all components that are required to make contact with heatspreader do so. Failure to utilize the center mounting hole will result in improper contact between these components and heatspreader thereby reducing heat dissipation efficiency.

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

For more information about this subject refer to Application Note AN14_ETX_XTX_Mounting_Solutions.pdf that can be found on the congatec website.

3.1 Heatspreader Dimensions



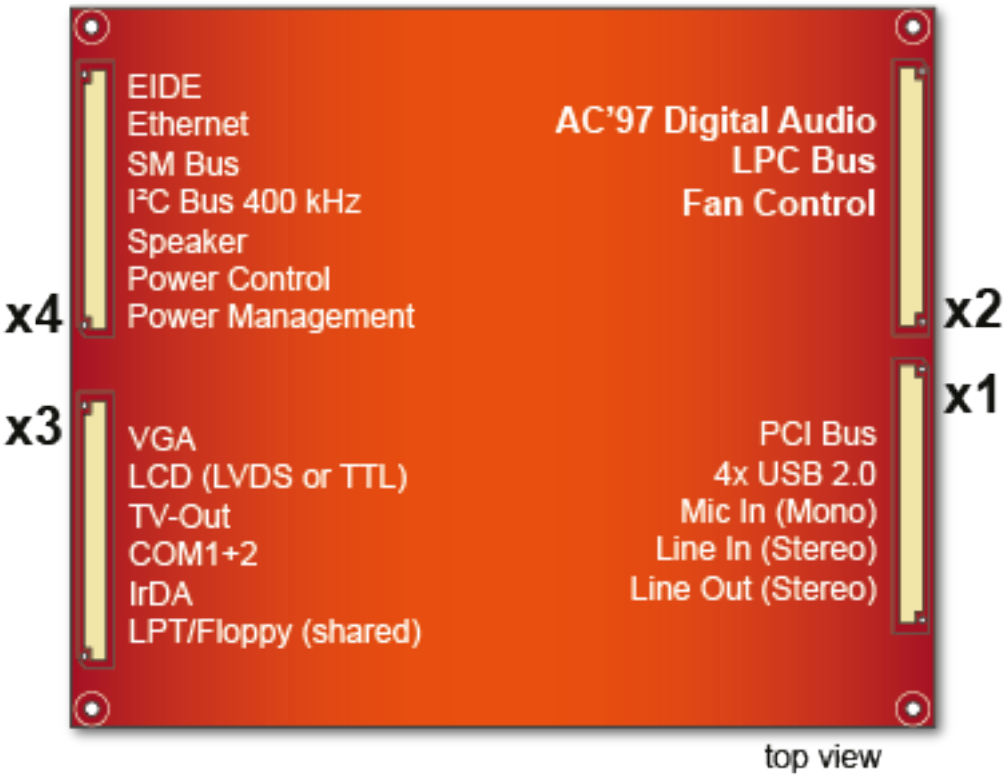
Note

All measurements are in millimeters. Torque specification for heatspreader screws is 0.3 Nm.

Caution

When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.

4 Connector Subsystems



In this view the connectors are seen “through” the module.

4.1 Connector X1

The following subsystems can be found on connector X1.

4.1.1 PCI Bus

The implementation of the PCI bus complies with PCI specification Rev. 2.3 and ETX® specification Rev. 2.7

4.1.2 USB 2.0

The conga-XLX offers one OHCI and one EHCI USB host controller via the AMD Geode™ CS5536 companion device. These controllers comply with USB standard 1.1 and 2.0 and provide a total of four USB ports on the X1 connector that support the connection of USB 2.0 compliant devices.

4.1.3 Audio

The conga-ELXeco is equipped with a Realtek ALC203 audio codec. It is AC'97 2.3 specification compliant. The audio controller is integrated into the AMD Geode™ CS5536 companion device.

Note

The USB and Audio controllers are PCI bus devices. The BIOS allocates the necessary system resources when configuring the PCI devices.

4.1.4 Onboard Generated Supply Voltage

Pins 12, 16 and 24 on the X1 connector provide the ability to connect external devices to the modules onboard generated supply voltage (3.3V±5%). 3.3V external devices can be connected to these pins but must not exceed a maximum external load of 500mA. For more information about this feature contact congatec AG technical support.

Caution

Do not connect pins 12, 16 and 24 to a 3.3V external power supply. This will cause a current cross-flow and may result in either a system malfunction and/or damage to the external power supply and the module.

4.2 Connector X2 (XTX™ Extension)

congatec AG has chosen to replace the outdated ISA bus, currently found on ETX® modules X2 connector, with the latest technologies available in todays market. This implementation is called XTX™. The XTX™ extension is an enhancement of the highly successful ETX® standard and provides consumers the ability to equip their embedded applications with the latest technology while still utilizing the ETX® standard form factor.

The following subsystems can be found on connector X2.

4.2.1 LPC

As a part of the replacement to the no longer supported ISA bus, conga-XLX offers the LPC (Low Pin Count) bus through the use of AMD Geode™ CS5536 companion device. There are already many devices available for this Intel defined bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific carrier board using this bus.

4.2.2 USB 2.0

The AMD Geode™ CS5536 companion device only provides four USB ports and therefore the conga-XLX does not support additional USB ports on the X2 connector.

4.2.3 PCI Express™

PCI Express™ is not supported on the conga-XLX.

4.2.4 ExpressCard™

The optional implementation of ExpressCard™ is not supported on the conga-XLX.

4.2.5 AC'97 Digital Audio

The conga-XLX provides an interface that supports the connection of AC'97 digital audio codecs. For more information about this interface consult the XTX Design Guide.

4.2.6 Extended System Management

conga-XLX has additional signals and functions to further improve power management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) Output. Additionally there is an input signal called FAN_TACHOIN that provides the ability to monitor the system fan's RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason a two pulse per revolution fan, or similar hardware solution, is recommended. These features are implemented by the Winbond W83627HG super I/O.

4.3 Connector X3

The following subsystems can be found on connector X3. The implementation of all the subsystems comply with ETX® specification 2.7. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

4.3.1 Graphics

The conga-XLX graphics are driven by the graphics processor, which is incorporated into the AMD Geode™ LX800 chip found on the conga-XLX. This graphic processor offers strong improvements over the original GX core used on Geode™ chipsets in the past.

4.3.2 LCD

The user interface for flat panels is called EPI (Embedded Panel Interface based on VESA EDID™ 1.3) and is implemented for both LVDS (National Semi. DS90C363 transmitter) and Digital (AMD Geode™ CS5536 companion device) flat panels. Auto detection and backlight control are also supported.

4.3.3 TV-Out

Optional TV-Out support is implemented via the Focus FS453 found on the conga-XLX.

4.3.4 Serial Ports (1 and 2)

The conga-XLX offers two serial interfaces (TTL) that are provided by the I/O controller, which is a Winbond W83627HG super I/O located on the conga-XLX.

4.3.5 Serial Infrared Interface

Serial port 2 can be configured as a serial infrared interface. The Infrared (IrDA) function provides point-to-point (or multi-point to multi-point) wireless communication, which can operate under various transmission protocols including IrDA SIR. This feature is also implemented by the onboard Winbond W83627HG super I/O.

4.3.6 Parallel Port/Floppy Interface

The parallel port/floppy interface can be configured as either a conventional LPT parallel port or a floppy-disk drive port. This is software implemented and can be configured in the BIOS setup program. See section 8.5.5 of this document for information about configuring the parallel port/floppy interface.

Note

When using the onboard floppy interface the floppy drive must be connected via a non-twisted floppy cable versus a twisted cable. The floppy drive will not function when connected via a twisted floppy cable.

4.3.7 Keyboard/Mouse

The implementation of these subsystems comply with ETX® specification 2.7.

4.4 Connector X4

The following subsystems can be found on connector X4. The implementation of all the subsystems comply with ETX® specification 2.7. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

4.4.1 IDE

The conga-XLX provides one IDE channel. The channel originates from the CS5536 AMD Geode™ companion device and is capable of UDMA 66/100 operation.

4.4.2 Ethernet

Ethernet interface is provided by a Realtek RTL8100C Single Chip Fast Ethernet NIC controller. The controller is IEEE 802.3u, 10/100Base-Tx fast Ethernet compatible. The interface provides single-ended differential signals that have to be routed through an Ethernet transformer.

4.4.3 I²C Bus 400kHz

The I²C bus is implemented through the use of ATMEL ATmega88 microcontroller. It provides a Fast Mode (400kHz max.) multi-master I²C Bus that has maximum I²C bandwidth.

4.4.4 Power Control

PWGIN

PWGIN (pin 4 on the X4 connector) can be connected to an external power good circuit or it may also be utilized as a manual reset input. In order to use PWGIN as a manual reset the pin must be grounded through the use of a momentary-contact pushbutton switch. When external circuitry asserts this signal, it's necessary that an open-drain driver drives this signal causing it to be held low for a minimum of 15ms to initiate a reset. Using this input is optional. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies the conga-XLX module is capable of generating its own power-on reset.

The conga-XLX provides support for controlling ATX-style power supplies. In order to do this the power supply must provide a constant source of 5V power. When not using an ATX power supply then the conga-XLX's pins PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

PS_ON#

The PS_ON (pin 5 on the X4 connector) signal is an active-low output that turns on the main outputs of an ATX-style power supply. This open-collector signal can be pulled up to the 5V_SB supply voltage through the use of a 1K resistor. Usually there is a pull-up resistor internally implemented in the power supply itself yet it is also good practice to implement a footprint for the pull-up resistor in the carrier board circuitry.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 7 on the X4 connector) is used to connect to a momentary-contact, active-low pushbutton input while the other terminal on the pushbutton must be connected to ground. This signal is XTX™ internally pulled up to 5V_SB using a 4k7 resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-XLX. The remaining necessary voltages are internally generated on the module using onboard power supplies. A carrier board designer should be aware of the following important information when designing a power supply for a conga-XLX application:

- As mentioned earlier in section 4.1.4 the conga-XLX is capable of generating an onboard 3.3V supply with an output current that is limited to 500mA. If an external device requires more then this 500mA limit then it's necessary to design a 3.3V supply into the carrier board.

Caution

It is not possible to connect an external 3.3V supply to the onboard generate 3.3V supply pins on the conga-XLX module. This will cause a current cross-flow and may result in either a system malfunction and/or damage to the external power supply and the module.

- Sometimes when designing carrier boards, carrier board designers choose to fuse power to some external devices such as keyboards or USB devices by using solid-state or polyswitch overcurrent protection devices. This results in the protective devices typically only opening after they pass several times their rated current for long periods of time. When the application power supply is incapable of generating the necessary current needed to open these protective devices it's possible that the application crashes as a result of an external fault and therefore will reduce the applications reliability as well as make a fault diagnosis of the application difficult.

- It has also been noticed that on some occasions problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document “ATX12V Power Supply Design Guide V2.2”.

4.4.5 Power Management

APM 1.2 compliant. ACPI 2.0 compliant with battery support. Also supports Suspend to RAM (S3).

5 Additional Features

5.1 Watchdog

The conga-XLX is equipped with a multi stage watchdog. This solution can be triggered by software and external OEM hardware (input pin is pin 48 on the X2 connector called WDTRG#). For more information about the Watchdog feature see the BIOS setup description section 8.5.8 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

5.2 Onboard Microcontroller

The conga-XLX is equipped with an ATMEL Atmega88 microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

5.3 Embedded BIOS

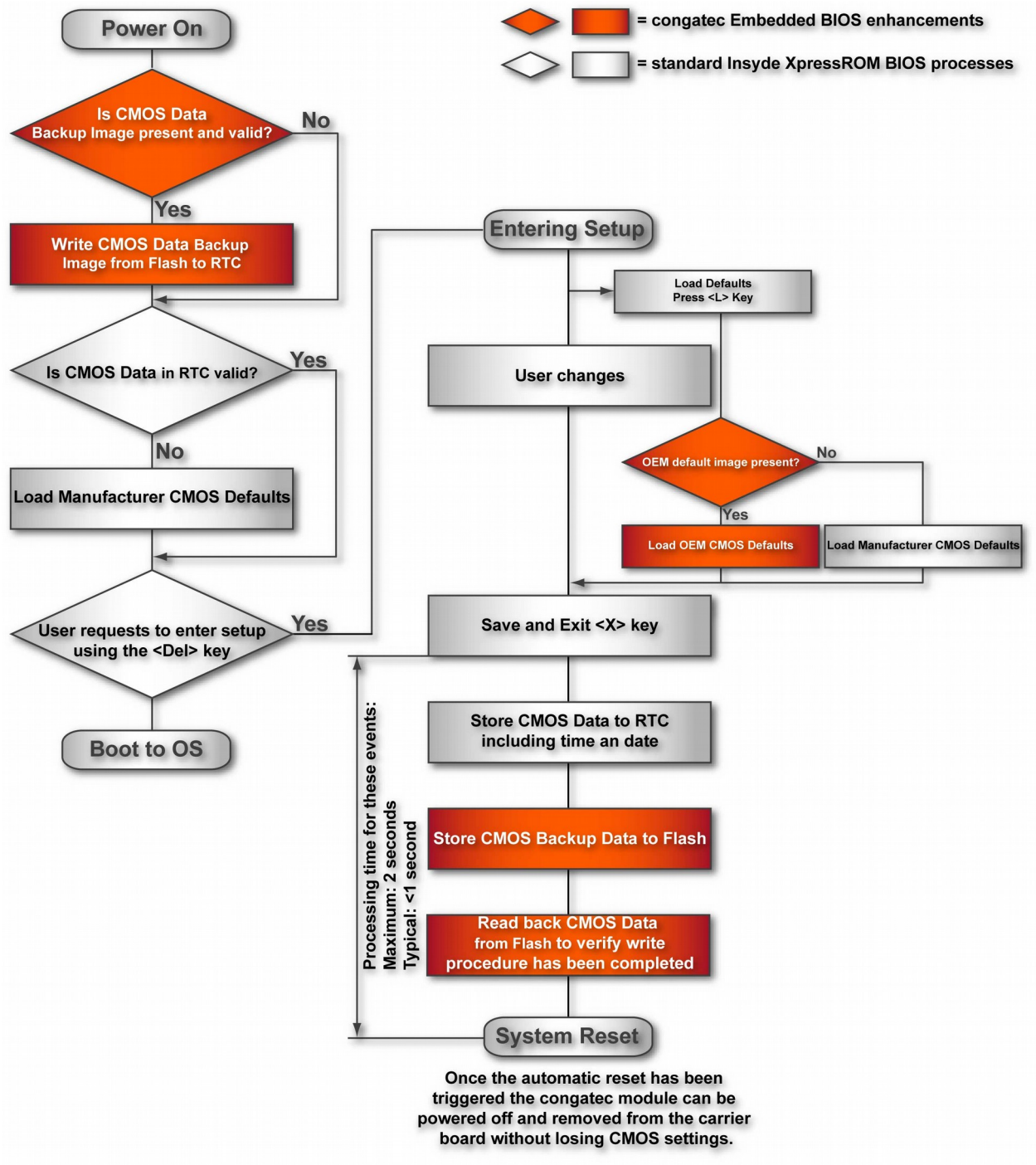
The conga-XLX is equipped with congatec Embedded BIOS and has the following features:

- ACPI Power Management
- ACPI Battery Support
- Supports Customer Specific CMOS Defaults
- Multistage Watchdog
- User Data Storage
- Manufacturing Data and Board Information
- OEM Splash Screen
- Flat Panel Auto Detection
- BIOS Setup Data Backup
- Fast Mode I²C Bus
- Real Headless Operation

Note

The conga-XLX embedded BIOS is based on the Insyde Xpress ROM BIOS and therefore does not support 'System Plug and Play' mechanism.

5.3.1 Simplified Overview of BIOS Setup Data Backup



The above diagram provides an overview of how the BIOS Setup Data is backed up on conga-XLX.

Once the BIOS Setup Program has been entered and the settings have been changed,

the user saves the settings and exits the BIOS Setup Program using the X key feature. After the X function has been invoked, the CMOS Data is stored in a dedicated non-volatile CMOS Data Backup area located in the BIOS Flash ROM chip as well as RTC. The CMOS Data is written to and read back from the CMOS Data Backup area in order to verify that the write procedure was successful. Once verified the X key Save and Exit function continues to perform some minor processing tasks and finally reaches an automatic reset point, which instructs the module to reboot. After the Automatic Reset has been triggered the congatec module can be powered off and, if need be, removed from the carrier board without losing the new CMOS settings.

5.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-XLX BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

congatec Battery Management Interface Specification

Battery System Design Guide

conga-SBM² User's Guide

6 Signal Descriptions and Pinout Tables

The following section describes the signals found on the four X connectors located on the bottom of the module. X1, X3, and X4 connectors are ETX® standard compliant while the X2 connector complies with the XTX™ extension specification. Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a XTX® module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 2 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
SATA	In compliance with Serial ATA specification, Revision 1.0a
LVDS	Low Voltage Differential Signal-350mV nominal; 450mV maximum differential signal
TPM	Trusted Platform Module

6.1 X1 Connector Signal Descriptions

Table 3 Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC ±5%	P		External supply
GND	Power Ground	P		External supply
3V	Power Supply +3.3VDC	P		See section 4.1.4
N.C.	Not Connected	N.A.		Do not connect
SERIRQ	Serial Interrupt request	I		Used in conjunction with LPC bus

Table 4 PCI Signal Descriptions

Signal	Description of PCI Bus Signals	I/O	PU/PD	Comment
PCICLK1..4.	Clock output	O 3.3V		
REQ0..3#	Bus request	I 3.3V		
GNT0..3#	Bus grant	O 3.3V		
AD0..31	Address/Data bus lines	I/O 3.3V		
CBE0..3#	Bus command/byte enables	I/O 3.3V		
PAR	Bus parity	I/O 3.3V		
SERR#	Bus system error	I/O 3.3V	PU 10k 3.3V	Not supported by chipset
GPERR#	Bus grant parity error	I/O 3.3V	PU 10k 3.3V	Not supported by chipset
PME#	Bus power management event	I/O 3.3VSB	PU 5k6 3.3VSB	
LOCK#	Bus lock	I/O 3.3V	-	Not supported by chipset
DEVSEL#	Bus device select	I/O 3.3V	PU 10k 3.3V	
TRDY#	Bus target ready	I/O 3.3V	PU 10k 3.3V	
IRDY#	Bus initiator ready	I/O 3.3V	PU 10k 3.3V	
STOP#	Bus stop	I/O 3.3V	PU 10k 3.3V	
FRAME#	Bus frame	I/O 3.3V	PU 10k 3.3V	
PCIRST#	Bus reset	O 3.3V		Asserted during system reset
INTA#	Bus interrupt A	I 3.3V	PU 10k 3.3V	
INTB#	Bus interrupt B	I 3.3V	PU 10k 3.3V	
INTC#	Bus interrupt C	I 3.3V	PU 10k 3.3V	
INTD#	Bus interrupt D	I 3.3V	PU 10k 3.3V	

Note

The PCI bus on the conga-XLX is not 5V tolerant.

Caution

Connecting 5V PCI devices to the conga-XLX will cause damage to hardware and/or loss of data.

Table 5 USB Signal Descriptions

Signal	Description of USB Signals	I/O	PU/PD	Comment
USB0	USB Port 0, data + or D+	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB0#	USB Port 0, data - or D-	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB1	USB Port 1, data + or D+	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB1#	USB Port 1, data - or D-	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB2	USB Port 2, data + or D+	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB2#	USB Port 2, data - or D-	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB3	USB Port 3, data + or D+	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB3#	USB Port 3, data - or D-	I/O		USB 2.0 compliant and backwards compatible to USB 1.1

Table 6 Audio Signal Descriptions

Signal	Description of Audio Signals	I/O	PU/PD	Comment
SNDL	Line-Level stereo output left	O		Analog output (1 Vrms)
SNDR	Line-Level stereo output right	O		Analog output (1 Vrms)
AUXAL	Auxiliary input A left	I	22k PD	Analog input (1 Vrms)
AUXAR	Auxiliary input A right	I	22k PD	Analog input (1 Vrms)
MIC	Microphone input	I	2k2 PU to Audio Vref (2,5V)	Analog input (1 Vrms)
ASGND	Analog ground of sound controller	P		
ASVCC	Analog supply of sound controller	P		5V power output (Can be used as an analog supply for analog amplifier maximum 30mA)

6.2 Connector X1 Pinout

Table 7 X1 Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	PCICLK3	4	PCICLK4	53	PAR	54	SERR# (*)
5	GND	6	GND	55	GPERR# (*)	56	Reserved
7	PCICLK1	8	PCICLK2	57	PME#	58	USB2#
9	REQ3#	10	GNT3#	59	LOCK# (*)	60	DEVSEL#
11	GNT2#	12	3V	61	TRDY#	62	USB3#
13	REQ2#	14	GNT1#	63	IRDY#	64	STOP#
15	REQ1#	16	3V	65	FRAME#	66	USB2
17	GNT0#	18	RESERVED	67	GND	68	GND
19	VCC	20	VCC	69	AD16	70	CBE2#
21	SERIRQ	22	REQ0#	71	AD17	72	USB3
23	AD0	24	3V	73	AD19	74	AD18
25	AD1	26	AD2	75	AD20	76	USB0#
27	AD4	28	AD3	77	AD22	78	AD21
29	AD6	30	AD5	79	AD23	80	USB1#
31	CBE0#	32	AD7	81	AD24	82	CBE3#
33	AD8	34	AD9	83	VCC	84	VCC
35	GND	36	GND	85	AD25	86	AD26
37	AD10	38	AUXAL	87	AD28	88	USB0
39	AD11	40	MIC	89	AD27	90	AD29
41	AD12	42	AUXAR	91	AD30	92	USB1
43	AD13	44	ASVCC	93	PCIRST#	94	AD31
45	AD14	46	SNDL	95	INTC#	96	INTD#
47	AD15	48	ASGND	97	INTA#	98	INTB#
49	CBE1#	50	SNDR	99	GND	100	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-XLX.

6.3 X2 Connector Signal Descriptions (XTX™ extension)

Table 8 LPC Interface Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
LPC_AD[0..3]	Multiplexed Command, Address and Data.	I/O3.3V	PU 10k 3.3V	
LPC_FRAME#	Frame: Indicates start of a new cycle or termination of a broken cycle.	O 3.3V	PU 10k 3.3V	
LPC_DRQ[0..1]#	Encoded DMA/Bus Master Request.	I 3.3V	PU 10k 3.3V	LPC_DRQ1 not supported

Table 9 Serial ATA Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	Serial ATA channel 0, Receive Input differential pair.	N.C.		Not supported
SATA0_TX+ SATA0_TX-	Serial ATA channel 0, Transmit Output differential pair.	N.C.		Not supported
SATA1_RX+ SATA1_RX-	Serial ATA channel 1, Receive Input differential pair.	N.C.		Not supported
SATA1_TX+ SATA1_TX-	Serial ATA channel 1, Transmit Output differential pair.	N.C.		Not supported
SATA2_RX+ SATA2_RX-	Serial ATA channel 2, Receive Input differential pair.	N.C.		Not supported
SATA2_TX+ SATA2_TX-	Serial ATA channel 2, Transmit Output differential pair.	N.C.		Not supported
SATA3_RX+ SATA3_RX-	Serial ATA channel 3, Receive Input differential pair.	N.C.		Not supported
SATA3_TX+ SATA3_TX-	Serial ATA channel 3, Transmit Output differential pair.	N.C.		Not supported
IL_SATA#	Serial ATA Interlock Switch Input.	I		Not supported
SATALED#	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V		Not supported

Table 10 PCI Express Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	PCI Express channel 0, Receive Input differential pair.	N.C.		Not supported
PCIE0_TX+ PCIE0_TX-	PCI Express channel 0, Transmit Output differential pair.	N.C.		Not supported
PCIE1_RX+ PCIE1_RX-	PCI Express channel 1, Receive Input differential pair.	N.C.		Not supported
PCIE1_TX+ PCIE1_TX-	PCI Express channel 1, Transmit Output differential pair.	N.C.		Not supported
PCIE2_RX+ PCIE2_RX-	PCI Express channel 2, Receive Input differential pair.	N.C.		Not supported
PCIE2_TX+ PCIE2_TX-	PCI Express channel 2, Transmit Output differential pair.	N.C.		Not supported
PCIE3_RX+ PCIE3_RX-	PCI Express channel 3, Receive Input differential pair.	N.C.		Not supported
PCIE3_TX+ PCIE3_TX-	PCI Express channel 3, Transmit Output differential pair.	N.C.		Not supported
PCIE_CLK_REF+ PCIE_CLK_REF-	PCI Express Reference Clock for Lanes 0 to 3.	N.C.		Not supported
PCE_WAKE#	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	N.C.		Not supported

Table 11 ExpressCard Support Pins Descriptions

Signal	Description	I/O	PU/PD	Comment
EXEC_CPPE[0..1]#	ExpressCard capable card request.	N.C.		Not supported
EXEC_RST[0..1]#	ExpressCard Reset	N.C.		Not supported

Table 12 Audio Codec Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
AC_RST#	CODEC Reset	O 3.3V		
AC_SYNC	Serial Bus Synchronization.	O 3.3V	PU 10k 3.3V	AC_SYNC is a boot strap signal (see note below)
AC_BIT_CLK	12.228 MHz Serial Bit Clock from CODEC.	O 3.3V		
AC_SDOUT	Audio Serial Data Output to CODEC.	O 3.3V	PU 10k 3.3V	AC_SDOUT is a boot strap signal (see note below)
AC_SDIN0	Audio Serial Data Input from CODEC0.			Optional, contact congatec technical support for more information about this signal.
AC_SDIN1	Audio Serial Data Input from CODEC0.			Not supported
AC_SDIN2	Audio Serial Data Input from CODEC0.	I 3.3V		
CODECSET	Disable onboard Audio Codec.	I 3.3V	PD 10k	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 6.8 of this user's guide.

Table 13 USB Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
USBP4	USB Port 4, data + or D+	N.C.		Not supported
USBP4#	USB Port 4, data - or D-	N.C.		Not supported
USBP5	USB Port 5, data + or D+	N.C.		Not supported
USBP5#	USB Port 5, data - or D-	N.C.		Not supported

Table 14 Miscellaneous Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
GND	Ground. All GND pins should be connected to the carrier board ground plane.	P		
5V_SB	Additional Power input for the internal suspend and power-control circuitry. This Signal is connected to XTX-Connector X4/Pin3. Refer to XTX Specification for further details.	P		
VCC	5V Power Input. All VCC pins should be connected to the carrier board 5 Volt power plane.	P		
SUS_STAT#	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3V	PD 1k	SUS_STAT# is a boot strap signal (see note below)
SLP_S3#	S3 Sleep Control: This signal shuts off power to all non-critical systems when in S3 (Suspend to Ram), S4 or S5 states.	O 3.3VSB	PU 10k 3.3VSB	
SLP_S5#	S5 Sleep Control: This signal shuts off power to all non-critical systems when in S5 (Soft Off) state.	O 3.3V	PU 10k 3.3VSB	Only supported on hardware revisions B.0 and later.
PCI_CLKRUN#	PCI Clock Run: This signal is used to support PCI Clock Run protocol. It connects to PCI devices that need to request clock re-start, or prevention of clock stopping.	N.C.		Not supported
PCI_GNT#A	reserved	N.C.		Not supported
PCI_REQ#A	reserved	N.C.		Not supported
FAN_PWMOUT	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM.	O 5V		
FAN_TACHOIN	Fan tachometer input.	I 5V		
WDTRIG	Watchdog Trigger Signal.	I 5V	PU 10k 5V	Trigger source should have OC output.
PP_TPM	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V		Trusted Platform Module chip is optional.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 6.8 of this user's guide.

6.4 X2 Connector Pinout

The following table includes a reference column describing the corresponding ETX standard X2 connector pinout.

Table 15 X2 Connector Pinout

Pin	XTX™ Signal	*ETX® Reference*	Pin	XTX™ Signal	*ETX® Reference*
1	GND	GND	2	GND	GND
3	PCIE_CLK_REF+ (*)	SD14	4	SATA0_RX+ (*)	SD15
5	PCIE_CLK_REF- (*)	SD13	6	SATA0_RX- (*)	MASTER#
7	GND	SD12	8	GND	DREQ7
9	PCIE3_TX+ (*)	SD11	10	SATA0_TX- (*)	DACK7#
11	PCIE3_TX- (*)	SD10	12	SATA0_TX+ (*)	DREQ6
13	GND	SD9	14	5V_SB	DACK6#
15	PCIE3_RX+ (*)	SD8	16	SATA1_RX+ (*)	DREQ5
17	PCIE3_RX- (*)	MEMW#	18	SATA1_RX- (*)	DACK5#
19	VCC	MEMR#	20	5V_SB	DREQ0
21	EXC1_CPPE# (*)	LA17	22	SATA1_TX- (*)	DACK0#
23	EXC1_RST# (*)	LA18	24	SATA1_TX+ (*)	IRQ14
25	USBP5 (*)	LA19	26	GND	IRQ15
27	USBP5# (*)	LA20	28	SATA2_RX+ (*)	IRQ12
29	GND	LA21	30	SATA2_RX- (*)	IRQ11
31	PCIE2_TX+ (*)	LA22	32	SUS_STAT#	IRQ10
33	PCIE2_TX- (*)	LA23	34	PCI_CLKRUN# (*)	IO16#
35	GND	GND	36	GND	GND
37	PCIE2_RX+ (*)	SBHE#	38	SATA2_TX- (*)	M16#
39	PCIE2_RX- (*)	SA0	40	SATA2_TX+ (*)	OSC
41	EXC0_CPPE# (*)	SA1	42	GND	BALE
43	EXC0_RST# (*)	SA2	44	SATA3_RX+ (*)	TC
45	USBP4 (*)	SA3	46	SATA3_RX- (*)	DACK2#
47	USBP4# (*)	SA4	48	WDTRIG	IRQ3
49	SLP_S3#	SA5	50	SATALED# (*)	IRQ4
51	VCC	VCC	52	VCC	VCC
53	PCIE1_RX- (*)	SA6	54	SATA3_TX- (*)	IRQ5
55	PCIE1_RX+ (*)	SA7	56	SATA3_TX+ (*)	IRQ6
57	GND	SA8	58	IL_SATA# (*)	IRQ7
59	PCIE1_TX- (*)	SA9	60	PP_TPM	SYSCLK
61	PCIE1_TX+ (*)	SA10	62	RESERVED	REFSH#
63	PCE_WAKE# (*)	SA11	64	PCI_GNT#A (*)	DREQ1
65	SLP_S5#	SA12	66	PCI_REQ#A (*)	DACK1#

Pin	XTX™ Signal	*ETX® Reference*	Pin	XTX™ Signal	*ETX® Reference*
67	GND	GND	68	GND	GND
69	PCIE0_RX- (*)	SA13	70	RESERVED	DREQ3
71	PCIE0_RX+ (*)	SA14	72	RESERVED	DACK3#
73	GND	SA15	74	VCC	IOR#
75	PCIE0_TX- (*)	SA16	76	RESERVED	IOW#
77	PCIE0_TX+ (*)	SA18	78	RESERVED	SA17
79	CODECSET	SA19	80	VCC	SMEMR#
81	AC_RST#	IOCHRDY	82	AC_SDOUT	AEN
83	VCC	VCC	84	VCC	VCC
85	AC_SYNC	SD0	86	AC_SDIN0	SMEMW#
87	AC_SDIN1 (*)	SD2	88	AC_SDIN2	SD1
89	AC_BIT_CLK	SD3	90	FAN_TACHOIN	NOWS#
91	LPC_AD0	DREQ2	92	FAN_PWMOUT	SD4
93	LPC_AD1	SD5	94	LPC_FRAME#	IRQ9
95	LPC_AD2	SD6	96	LPC_DRQ0#	SD7
97	LPC_AD3	IOCHK#	98	LPC_DRQ1#	RSTDRV
99	GND	GND	100	GND	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-XLX.

6.5 X3 Connector Signal Descriptions

Table 16 Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC, ±5%	P		External supply
GND	Power Ground	P		External supply
N.C.	Not connected	N.A.		Do not connect
LTGIO0	General Purpose I O	N.A.		Not supported

Table 17 CRT Signal Descriptions

Signal	Description of CRT signals	I/O	PU/PD	Comment
HSY	Horizontal Synchronization Pulse	O 3.3V		5V tolerant
VSY	Vertical Synchronization Pulse	O 3.3V		5V tolerant
R	Red channel RGB Analog Video Output	O		Analog output
G	Green channel RGB Analog Video Output	O		Analog output
B	Blue channel RGB Analog Video Output	O		Analog output
DDCK	Display Data Channel Clock	I/O	PU 2k2 5V	
DDDA	Display Data Channel Data	I/O	PU 2k2 5V	

Table 18 TV Signal Descriptions

Signal	Description of TV signals (optional)	I/O	PU/PD	Comment
SYNC	Composite sync	O		Analog output
Y	Luminance for S-Video or Red for SCART	O		Analog output
C	Chrominance for S-Video or Green for SCART	O		Analog output
Comp	Composite Video or Blue for SCART	O		Analog output

Table 19 Keyboard and Infrared Signal Descriptions

Signal	Description of keyboard and infrared signals	I/O	PU/PD	Comment
KBDAT	Keyboard Data	I/O 5V	PU 4k7 5V	
KBCLK	Keyboard Clock	O 5V	PU 4k7 5V	
MSDAT	Mouse Data	I/O 5V	PU 4k7 5V	
MSCLK	Mouse Clock	O 5V	PU 4k7 5V	
IRTX	Infrared Transmit	O 5V		
IRRX	Infrared Receive	I 5V		

Table 20 COM Signal Descriptions

Signal	Description of COM signals	I/O	PU/PD	Comment
DTR1#	Data terminal ready for COM1	O 5V	PU 4k7 5V	DTR1# is a boot strap signal (see note below)
DTR2#	Data terminal ready for COM2	O 5V	PD 100k	
RI1#, RI2#	Ring indicator for COM1/COM2	I 5V	PD 100k	
TXD1, TXD2	Data transmit for COM1/COM2	O 5V	PU 4k7 5V	TXD1 and TXD2 are boot strap signals (see note below)
RXD1, RXD2	Data receive for COM1/COM2	I 5V	PD 100k	
CTS1#, CTS2#	Clear to send for COM1/COM2	I 5V	PD 100k	
RTS1#	Request to send for COM1	O 5V	PD 100k	RTS1# is a boot strap signal (see note below)
RTS2#	Request to send for COM2	O 5V	PD 100k	
DCD1#, DCD2#	Data carrier detect for COM1/COM2	I 5V	PD 100k	
DSR1#, DSR2#	Data set ready for COM1/COM2	I 5V	PD 100k	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 6.8 of this user's guide.

Table 21 LVDS Flat Panel Signals

Signal	Description of LVDS Flat Panel signals	I/O	PU/PD	Comment
BIASON	Controls display contrast voltage ON			Not supported
DIGON	Controls display Power ON	O 5V	PD 10k	
BLON#	Controls display Backlight ON	O 5V		
LCDDO0..19	LVDS channel data 0..19	O LVDS		LVDS 1 channel 18bit therefore LCDDO1..7 are only supported
DETECT#	Panel hot-plug detection	I		Not supported
FPDDC_CLK	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
FPDDC_DAT	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

Table 22 LVDS Interface Pinout

Pin	Signal Name	Signal Mapping	Pin	Signal Name	Signal Mapping
1	GND		2	GND	
3	R		4	B	
5	HSY		6	G	
7	VSY		8	DDCK	
9	DETECT# (*)		10	DDDA	
11	LCDDO[16] (*)	TX2OUTCLK-	12	LCDDO[18] (*)	TX2OUT3-
13	LCDDO[17] (*)	TX2OUTCLK+	14	LCDDO[19] (*)	TX2OUT3+
15	GND		16	GND	
17	LCDDO[13] (*)	TX2OUT1+	18	LCDDO[15] (*)	TX2OUT2+
19	LCDDO[12] (*)	TX2OUT1-	20	LCDDO[14] (*)	TX2OUT2-
21	GND		22	GND	
23	LCDDO[8] (*)	TX1OUT3-	24	LCDDO[11] (*)	TX2OUT0+
25	LCDDO[9] (*)	TX1OUT3+	26	LCDDO[10] (*)	TX2OUT0-
27	GND		28	GND	
29	LCDDO[4]	TX1OUT2-	30	LCDDO[7]	TX1OUTCLK+
31	LCDDO[5]	TX1OUT2+	32	LCDDO[6]	TX1OUTCLK-
33	GND		34	GND	
35	LCDDO[1]	TX1OUT0+	36	LCDDO[3]	TX1OUT1+
37	LCDDO[0]	TX1OUT0-	38	LCDDO[2]	TX1OUT1-
39	VCC		40	VCC	
41	FPDDC_DAT		42	LTGIO0	
43	FPDDC_CLK		44	BLON#	
45	BIASON (*)		46	DIGON	
47	COMP		48	Y	
49	SYNC		50	C	

TX1= Channel 1 transmit
TX2= Channel 2 transmit

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-XLX.

Table 23 TTL Flat Panel Signals

Signal	Description of TTL Flat Panel Signals	I/O	PU/PD	Comment
HSYNC	Horizontal synchronization pulse	O 3.3V		Also referred to as LP (Line Pulse)
VSYNC	Vertical synchronization pulse	O 3.3V		Also referred to as FLM (First Line Marker)
BIASON	N.A.			
DIGON	Controls display Power ON	O 5V	PD 10k	
BLON#	Controls display Backlight ON	O 5V		
R[0..5], B[0..5], G[0..5]	RGB Signals	O 3.3V		
SHFCLK	Panel data clock	O 3.3V		

Table 24 TTL Flat Panel Interface Pinout

TTL Interface Pinout			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT# (*)	10	DDDA
11	B4	12	SHFCLK
13	B5	14	EN
15	GND	16	GND
17	B1	18	B3
19	B0	20	B2
21	GND	22	GND
23	G2	24	G5
25	G3	26	G4
27	GND	28	GND
29	R4	30	G1
31	R5	32	G0
33	GND	34	GND
35	R1	36	R3
37	R0	38	R2
39	VCC	40	VCC
41	FPDDC_DAT	42	VSYNC
43	FPDDC_CLK	44	BLON#
45	HSYNC	46	DIGON
47	COMP	48	Y
49	SYNC	50	C

Table 25 FDC Signal Descriptions

Signal	Description of FDC signals (shared with LPT)	I/O	PU/PD	Comment
FLPY#	Floppy Interface configuration input	N.A.		Not supported, see section 4.3.5 for more information.
RES	N.C.	N.A.		Not available
DENSEL	Density select: low = 250/300Kb/s high = 500/1000Kb/s	O 5V		
INDEX#	Index signal	I 5V		
TRK0#	Track signal	I 5V		
WP#	Write protect signal	I 5V		
RDATA#	Raw data read	I 5V		
DSKCHG#	Disk change	I 5V		
HDSEL#	Head select	O 5V		
DIR#	Direction	O 5V		
STEP#	Motor step	O 5V		
DRV	Drive select	O 5V		
MOT#	Motor select	O 5V		
WDATA#	Raw write data	O 5V		
WGATE#	Write enable	O 5V		

Table 26 Floppy Support Mode Pinout

Floppy Support Mode Pinout			
Pin	**Signal**	**Pin**	**Signal**
51	FLPY# (*)	52	RESERVED
53	VCC	54	GND
55	RESERVED	56	DENSEL
57	RESERVED	58	RESERVED
59	IRRX	60	HDSEL#
61	IRTX	62	RESERVED
63	RXD2	64	DIR#
65	GND	66	GND
67	RTS2#	68	RESERVED
69	DTR2#	70	STEP#
71	DCD2#	72	DSKCHG#
73	DSR2#	74	RDATA#
75	CTS2#	76	WP#
77	TXD2	78	TRK0#
79	RI2#	80	INDEX#
81	VCC	82	VCC
83	RXD1	84	DRV
85	RTS1#	86	MOT
87	DTR1#	88	WDATA#
89	DCD1#	90	WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-XLX.

Table 27 LPT Signal Descriptions

Signal	Description of LPT signals (shared with FDC)	I/O	PU/PD	Comment
LPT	LPT Interface configuration input	N.A.		Not supported, see section 4.3.5 for more information.
STB#	Strobe signal	O 5V		
AFD#	Automatic feed	O 5V		
PD0	Data bus D0	I/O 5V		
PD1	Data bus D1	I/O 5V		
PD2	Data bus D2	I/O 5V		
PD3	Data bus D3	I/O 5V		
PD4	Data bus D4	I/O 5V		
PD5	Data bus D5	I/O 5V		
PD6	Data bus D6	I/O 5V		
PD7	Data bus D7	I/O 5V		
ERR#	LPT error	I 5V		
INIT#	Initiate	O 5V		
SLIN#	Select	O 5V		
ACK#	Acknowledge	I 5V		
BUSY	Busy	I 5V		
PE	Paper empty	I 5V		
SLCT	Power On	I 5V		

Table 28 LPT Support Mode Pinout

Parallel Port Mode Pinout			
Pin	**Signal**	**Pin**	**Signal**
51	LPT (*)	52	RESERVED
53	VCC	54	GND
55	STB#	56	AFD#
57	RESERVED	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2#	80	PD0
81	VCC	82	VCC
83	RXD1	84	ACK#
85	RTS1#	86	BUSY
87	DTR1#	88	PE
89	DCD1#	90	SLCT
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-XLX.

6.6 X4 Connector Signal Descriptions

Table 29 Signal Descriptions

Signal	Description	I/O	Comment
VCC	Power Supply +5VDC, ±5%	I	external supply
GND	Power Ground	I	external supply
N.C.	Not connected	N.A.	Do not connect
PIDE	Refers to Primary IDE channel	I/O	
SIDE	Refers to Secondary IDE channel	I/O	

Table 30 IDE Signal Descriptions

Signal	Description of IDE signals	I/O	PU/PD	Comment
PIDE_D0..15	Primary IDE Data bus	I/O 3.3V		PD 10k on PIDE_D7
PIDE_A0..2	Primary IDE Address bus	O 3.3V		
PIDE_CS1#	Primary IDE chip select channel 0	O 3.3V		
PIDE_CS3#	Primary IDE chip select channel 1	O 3.3V		
PIDE_DRQ	Primary IDE DMA request	I 3.3V	PD 10k	
PIDED_AK#	Primary IDE DMA acknowledge	O 3.3V		
PIDE_RDY	Primary IDE ready	I 3.3V	PU 10k 3.3V	
PIDE_IOR#	Primary IDE IO read	O 3.3V		
PIDE_IOW#	Primary IDE IO write	O 3.3V		
PIDE_INTRQ	Primary IDE interrupt request	I 3.3V	PU 10k 3.3V	
SIDE_D0..15	Secondary IDE Data bus	I/O 3.3V		Not supported
SIDE_A0..2	Secondary IDE Address bus	O 3.3V		Not supported
SIDE_CS1#	Secondary IDE chip select channel0	O 3.3V		Not supported
SIDE_CS3#	Secondary IDE chip select channel1	O 3.3V		Not supported
SIDE_DRQ	Secondary IDE DMA request	I 3.3V	PD 5k6	Not supported
SIDED_AK#	Secondary IDE DMA acknowledge	O 3.3V		Not supported
SIDE_RDY	Secondary IDE ready	I 3.3V	PU 4k7 3.3V	Not supported
SIDE_IOR#	Secondary IDE IO read	O 3.3V		Not supported
SIDE_IOW#	Secondary IDE IO write	O 3.3V		Not supported
SIDE_INTRQ	Secondary IDE interrupt request	I 3.3V	PU 10k 3.3V	Not supported
DASP_S	Secondary IDE Drive active	O		Not supported
PDIAG_S	Secondary IDE Master/Slave negotiation	I		Not supported
HDRST#	Hard Drive reset	O 5V		
CBLID_P#	Not supported	I 3.3V	PU 10k 3.3V	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 6.8 of this user's guide.

Table 31 Ethernet Signal Descriptions

Signal	Description of Ethernet signals	I/O	PU/PD	Comment
TXD#, TXD	Ethernet Twisted Pair transmit signal pair	O		Twisted pair signals for external transformer
RXD#, RXD	Ethernet Twisted Pair receive signal pair	I		Twisted pair signals for external transformer
ACTLED#	Ethernet activity LED	O 3.3V		
LILED#	Ethernet link LED	O 3.3V		
SPEEDLED#	Ethernet speed LED, ON at 100Mb/s	O 3.3V		

Table 32 Power Control Signals

Signal	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	Power good input	I		Also usable as reset input, make low with O.C. to cause reset.
5V_SB	Supply of internal suspend circuit	P		
PS_ON#	Power Save ON	O 5VSB	PU 10k 5VSB	
PWRBTN#	Power Button	I 5VSB	PU 10K 5VSB	

Table 33 Power Management Signals

Signal	Description of Power Management signals	I/O	PU/PD	Comment
RSMRST#	Resume / reset input	I 3.3VSB	PU 10k 3.3VSB	
SMBALRT#	System management bus alert input	I		Not supported
BATLOW#	Battery low input	I 3.3VSB	PU 10k 3.3VSB	
GPE1#	General purpose power management event input 1	I 3.3V	PU 10k 3.3V	
GPE2#	General purpose power management event input 2	I 3.3VSB	PU 5k6 3.3VSB	
EXTSMI#	System management interrupt input	I 3.3VSB	PU 10k 3.3VSB	

Table 34 Miscellaneous Signal Descriptions

Signal	Description of Miscellaneous signals	I/O	PU/PD	Comment
SPEAKER	Speaker output	O		
BATT	Battery supply	I		
I^2CLK	I^2C Bus clock	I/O 5V	PU 4k7 5V	
I^2DAT	I^2C Bus Data	I/O 5V	PU 4k7 5V	
SMBCLK	SM Bus clock	I/O 3.3V	PU 2k2 3.3V	
SMBDATA	SM Bus Data	I/O 3.3V	PU 2k2 3.3V	
KBINH#	Keyboard inhibit	I 5V		
OVCR#	Over current detect for USB	I 3.3V	PU 10k 3.3V	
ROMKBCS#	Do not connect	N.A.		Not available
EXT_PRG	Do not connect	N.A.		Not available
GPCS#	General purpose chip select	O		Not supported

6.7 X4 Connector Pinout

Table 35 Connector X4 Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	SIDE_IOW# (*)	52	PIDE_IOR#
3	5V_SB	4	PWGIN	53	SIDE_DRQ (*)	54	PIDE_IOW#
5	PS_ON#	6	SPEAKER	55	SIDE_D15 (*)	56	PIDE_DRQ
7	PWRBTN#	8	BATT	57	SIDE_D0 (*)	58	PIDE_D15
9	KBINH#	10	LILED#	59	SIDE_D14 (*)	60	PIDE_D0
11	RSMRST#	12	ACTLED#	61	SIDE_D1 (*)	62	PIDE_D14
13	ROMKBCS#	14	SPEEDLED#	63	SIDE_D13 (*)	64	PIDE_D1
15	EXT_PRG	16	I2CLK	65	GND	66	GND
17	VCC	18	VCC	67	SIDE_D2 (*)	68	PIDE_D13
19	OVCR#	20	GPCS# (*)	69	SIDE_D12 (*)	70	PIDE_D2
21	EXTSMI#	22	I2DAT	71	SIDE_D3 (*)	72	PIDE_D12
23	SMBCLK	24	SMBDATA	73	SIDE_D11 (*)	74	PIDE_D3
25	SIDE_CS3# (*)	26	SMBALRT# (*)	75	SIDE_D4 (*)	76	PIDE_D11
27	SIDE_CS1# (*)	28	DASP_S (*)	77	SIDE_D10 (*)	78	PIDE_D4
29	SIDE_A2 (*)	30	PIDE_CS3#	79	SIDE_D5 (*)	80	PIDE_D10
31	SIDE_A0 (*)	32	PIDE_CS1#	81	VCC	82	VCC
33	GND	34	GND	83	SIDE_D9 (*)	84	PIDE_D5
35	PDIAG_S (*)	36	PIDE_A2	85	SIDE_D6 (*)	86	PIDE_D9
37	SIDE_A1 (*)	38	PIDE_A0	87	SIDE_D8 (*)	88	PIDE_D6
39	SIDE_INTRQ (*)	40	PIDE_A1	89	GPE2#	90	CBLID_P#
41	BATLOW#	42	GPE1#	91	RXD#	92	PIDE_D8
43	SIDE_AK# (*)	44	PIDE_INTRQ	93	RXD	94	SIDE_D7 (*)
45	SIDE_RDY (*)	46	PIDE_AK#	95	TXD#	96	PIDE_D7 (*)
47	SIDE_IOR# (*)	48	PIDE_RDY	97	TXD	98	HDRST#
49	VCC	50	VCC	99	GND	100	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-XLX.

6.8 Boot Strap Signals

Table 36 Boot Strap signal Descriptions

Signal	Description of Boot Strap Signals	I/O	PU/PD	Comment
AC_SYNC	Serial Bus Synchronization.	O 3.3V	PU 10k 3.3V	AC_SYNC is a boot strap signal (see caution statement below)
AC_SDOUT	Audio Serial Data Output to CODEC.	O 3.3V	PU 10k 3.3V	AC_SDOUT is a boot strap signal (see caution statement below)
SUS_STAT#	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3V	PD 1k	SUS_STAT# is a boot strap signal (see caution statement below)
DTR1#	Data terminal ready for COM1	O 5V	PU 4k7 5V	DTR1# is a boot strap signal (see caution statement below)
TXD1, TXD2	Data transmit for COM1/COM2	O 5V	PU 4k7 5V	TXD1 and TXD2 are boot strap signals (see caution statement below)
RTS1#	Request to send for COM1	O 5V	PD 100k	RTS1# is a boot strap signal (see caution statement below)
SIDE_A0..2	Secondary IDE Address bus	O 3.3V		SIDE_A0 to A2 are boot strap signals (see caution statement below)

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either XTX™ internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the XTX™ module to malfunction and/or cause irreparable damage to the module.

If it is necessary to drive a TTL input (or another input which sources or sinks significant current) that uses the TXD1 signal, a CMOS-input buffer can be inserted in the signal path so that this line is not pulled up or down by external circuitry during system reset.

7 System Resources

7.1 System Memory Map

Table 37 Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1296MB – 1304MB (logic)	51000000 – 51800000	8MB	GeodeLink Interface Unit
1028MB – 1029MB (logic)	40400000 – 4043FFFF	256kB	VSA (Virtual System Architecture)
(TOM-64kB) – TOM	N.A.	64kB	ACPI reclaim, MPS and NVS area **
(TOM-24MB-64kB) – (TOM-64kB)	N.A.	24 MB	VGA graphics memory and frame buffer *
896 k – 1024 k	E0000 - FFFFF	128 kB	Runtime BIOS
800 k – 896 k	C8000 - DFFFF	96 kB	Upper memory***
640 k – 800 k	A0000 - C7FFF	160 kB	Video memory and BIOS
639 k – 640 k	9FC00 - 9FFFF	1 kB	Extended BIOS data
0 – 639k	00000 - 9FC00	512 kB	Conventional memory

Notes

T.O.M. = Top of memory = max. DRAM installed
** VGA graphics memory can be configured from 2 MB up to 254 MB in setup.*
*** Only if ACPI Aware OS is set to YES in setup.*
**** The UMA area from C8000h – DFFFFh will only be available if Network Boot Support and External HDD Boot Support are not used.*

7.2 I/O Address Assignment

The I/O address assignment of the conga-XLX module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

Table 38 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
0100 - 010F	16 bytes	No	congatec System Control
0170 - 0177	8 bytes	No	Secondary IDE channels
01F0 - 01F7	8 bytes	No	Primary IDE channels
02F8 - 02FF	8 bytes	Note	Serial Port 2 (COM2)
0378 - 037F	8 bytes	Note	Parallel Port 1 (LPT1)
03B0 – 03DF	16 bytes	No	Video system
03F0 - 03F5	6 bytes	No	Floppy channel 1
03F6	1 byte	No	Primary IDE channel command port
03F7	1 byte	No	Primary IDE channel status port
03F8 - 03FF	8 bytes	Note	Serial Port 1 (COM1)
0480 – 04BF	64 bytes	No	Motherboard resources
04D0 – 04D1	2 bytes	No	Motherboard resources
0800 – 087F	128 bytes	No	Motherboard resources
0A00 – 0A0F	16 bytes	No	Motherboard resources
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
6000 - 6008	8 bytes	No	System Management BUS
6100 - 61FF	256 bytes	No	GPIO Subsystem
6200 - 623F	64 bytes	No	MFGP timer register
9D00 - 9D7F	128 bytes	No	Power management register
9C00 - 9C40	128 bytes	No	ACPI register
AC1C - AC1F	4 bytes	No	VSA virtual register port
DC00 - DCFF	256 bytes	No	Ethernet controller registers
DD80 - DEFF	384bytes	No	Audio controller registers
DEA0 - DFFF	96 bytes	No	RAID controller registers
EFF0 – EFFF	16 bytes	No	IDE controller registers

Notes

Default, but can be changed to another address range.

7.3 Interrupt Request (IRQ) Lines

Table 39 IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	N.A.
1	No	Keyboard	N.A.
2	No	Cascade Interrupt from Slave PIC	N.A.
3	Note 1	Serial Port 2 (COM2) / Generic	IRQ3 via SERIRQ
4	Note 1	Serial Port 1 (COM1) / Generic	IRQ4 via SERIRQ
5	Yes	N.A.	IRQ5 via SERIRQ
6	Note 1	Floppy Drive Controller / Generic	IRQ6 via SERIRQ
7	Note 1	Parallel Port 1 (LPT1) / Generic	IRQ7 via SERIRQ
8	No	Real-time Clock	N.A.
9	Note 2	SCI / Generic	IRQ9 via SERIRQ
10	Yes	N.A.	IRQ10 via SERIRQ
11	Yes	N.A.	IRQ11 via SERIRQ
12	Note 1	PS/2 Mouse / Generic	IRQ12 via SERIRQ
13	No	Math processor	N.A.
14	Note 1	IDE Controller 0 (IDE0)	IRQ14
15	No	N.A.	N.A.

In PIC mode, the PCI bus interrupt lines can be routed to any free IRQ.

Notes

1. *Default, but can be changed to another interrupt.*
2. *In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCI interrupt line.*

7.4 Direct Memory Access (DMA) Channels

Table 40 DMA Channels

DMA#	Data Width	Available	Description
0	8 bits	Yes Note 3	
1	8 bits	Yes Note 3	
2	8 bits	Note 1, 3	Floppy Drive Controller
3	8 bits	Note 2, 3	Parallel Port (LPT)
4	16 bits	No	Cascade DMA Controller
5	16 bits	Yes	
6	16 bits	Yes	
7	16 bits	Yes	

Notes

1. *If the corresponding device is disabled in BIOS setup then the DMA channel can be used by customers hardware.*
2. *Not available if Parallel Port is used in ECP mode (Enhanced Parallel Port).*
3. *Only the 8 bit DMA channels 0-3 can be mapped to the LPC bus.*

7.5 PCI Configuration Space Map

Table 41 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	01h	00h	Internal	Host Bridge
00h	01h	01h	Internal	VGA Graphics
00h	01h	02h	Internal	Encryption
00h	0Eh	00h	INTC	VT6421 RAID Controller
00h	0Fh	00h	Internal	ISA Bridge
00h	0Fh	02h	Internal	IDE Controller
00h	0Fh	03h	Internal	Audio Multimedia Device
00h	0Fh	04h	Internal	OHCI Host Controller 0
00h	0Fh	05h	Internal	OHCI Host Controller 1
00h	0F	06h	Internal	UDC Controller
00h	0F	07h	Internal	ODC Controller
00h	10h	00h	INTD	RTL8100C Ethernet Controller

7.6 PCI Interrupt Routing Map

Table 42 PCI Interrupt Routing Map

PCI Bus INT line (see note below)	Geode LX800	Companion CS5536	Ethernet RTL8100C
INTA	x	x	
INTB		x	
INTC		x	
INTD		x	x

Note

These interrupts are available for external devices/slots via the X1 connector.

7.7 PCI Bus Masters

The conga-XLX supports four external PCI Bus Masters. There are no limitations in connecting bus master PCI devices.

Note

If there are two devices connected to the same PCI REQ/GNT pair and they are transferring data at the same time then the latency time of these shared PCI devices can not be guaranteed.

7.8 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

7.9 SM Bus

System Management (SM) bus signals are connected to the AMD Geode™ CS5536 companion device and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

7.10 LPC Bus

Low Pin Count bus signals are connected to the AMD Geode™ CS5536 companion device and are available on the X2 connector of the XTX module. The LPC bus can be used to interface an off-board non-system LPC device like a Super I/O. There is only the configuration base address 4Eh/4Fh available to access an off-board LPC devices. For more information about this subject contact congatec technical support.

8 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

8.1 Starting the BIOS setup program

The BIOS setup program is accessed by pressing the <DEL> key during POST.

8.1.1 Manufacturer Default Settings

Pressing the <End> key repeatedly immediately after power is initiated will result in the manufacturer default settings being loaded for that particular boot sequence and only that boot sequence. This is helpful when a previous BIOS setting is no longer desired.

8.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of main frames, with submenu selections. The main frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured, only the highlighted options can be configured. An option setting can be chosen by pressing the ↑↓Up/Down keys. The actual available setting is displayed on the right side of the option. The bottom line of the frame displays a short help text related to the option. These text messages explain the options and the possible impacts when changing a setting of the selected option in the frame. The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Note

Entries in the option column displayed in bold print indicate BIOS default values.

Key	Description
← → Left/Right	Select a setup item or sub menu.
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select next item.
F1	Display General Help screen.
<L>	Load optimal default settings. (only valid in main menu)
<S>	Save changes without exit setup. (only valid in main menu)
<X>	Save changes and exit setup. (only valid in main menu)
<Q>	Discard changes and exit setup. (only valid in main menu)
ENTER	Set an option of a particular setup item or enter sub menu.
ESC	Confirm changes of the actual menu/submenu and go to next menu.

8.3 Main Menu

When you first enter the BIOS setup, you will enter the 'Main Menu' screen. You can always return to the 'Main Menu' screen by using the ESC key.

The 'Main Menu' screen allows you to configure the system date and time, displays the available submenus and defines the exit procedure. The headline in the 'Main Menu' screen shows the recent BIOS version and build date.

Feature / Submenu	Options	Description
A. Time	Hour:Minute:Second	Specifies the current time. *Note: The time is in 24-hour format.*
B. Date	Day of week, month/day/year	Specifies the current date. *Note: The date is in month-day-year format.*
C: Board Information		Displays the board information submenu.
D. Device Configuration		Displays the device configuration submenu.
E. Power Management		Displays the power management submenu.
F. Performance Control		Displays the performance control submenu.
G. Boot Order		Displays the boot order submenu.
L. Load Defaults		Load the system CMOS defaults of all the setup options.
S. Save Values Without Exit		Save changes made in the BIOS setup without exiting setup.
Q. Exit Without Save		Exit setup without saving any changes made in the BIOS setup.
X. Save values and Exit		Exit setup and reboot so the new system configuration parameters can take effect.

8.4 Board Information

The 'Board Information' screen shows the product revision, board serial number, board controller firmware revision and board statistics.

Feature	Options	Description
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
Boot Counter	no option	Displays the number of boot-ups (max. 16777215).
Running Time	no option	Displays the time the board is running [in h] (max. 65535).
OEM BIOS Version	no option	Displays the OEM BIOS version string that is generated during OEM BIOS modification.

8.5 Device Configuration

Select the 'Device Configuration' submenu from the main setup menu and press enter or press the related letter in front of the menu to enter the 'Device Configuration' Setup screen. This menu is used for setting advanced features.

Submenu	Description
A. Drive Configuration	Set configuration for hard drive and flash devices
B. Graphics Configuration	Set the graphic interface configuration
C. Cache Configuration	Set the L1/L2 cache configuration
D. PCI Configuration	Set the PCI bus configuration
E. I/O Interface Configuration	Set the I/O interface configuration
F. USB Configuration	Set the USB configuration
G. Watchdog Configuration	Set the watchdog configuration
H. Hardware Monitoring	Monitors the system temperature, voltages and the fan speed
I. Boot Screen Configuration	Set the boot screen configuration

8.5.1 Drive Configuration Submenu

Feature	Options	Description
Hard Drive Configuration	**No Option**	
IDE BIOS Support	**Enabled** Disabled	Use this option to enable/disable the INT 13h BIOS services for hard drives. If this option is enabled and an IDE controller isn't present in the system, there may be an extra delay during POST while the procedures attempt to access a device.
DMA/UDMA Support	**Enabled** Disabled	Set to *Enabled* to support DMA/UDMA BIOS support. Set to *Disabled* to force disk drives to use PIO even if DMA-capable.
Force Mode for Drive 1	**Auto** PIO0,1,2,3,4 MDMA0, 1, 2 UDMA0, 1, 2, 3, 4, 5	Set to *AUTO* to let the BIOS auto detect the supported DMA mode. SWDMA = Single Word DMA MWDMA = Multi Word DMA UDMA = Ultra DMA
Force Mode for Drive 2	**Auto** PIO0,1,2,3,4 MDMA0, 1, 2 UDMA0, 1, 2, 3, 4, 5	Set to *AUTO* to let the BIOS auto detect the supported DMA mode. SWDMA = Single Word DMA MWDMA = Multi Word DMA UDMA = Ultra DMA
CD-ROM Boot Support	**Enabled** Disabled	Enables/Disables the CD-ROM boot option. If the CD-ROM boot option is enabled, it will be boot from bootable CD-ROM.
Floppy Boot Support	**Enable** Disable	Enables/Disables the Floppy boot option. If the Floppy boot option is enabled, all the floppy boot option ROM will be loaded and the floppy interface services are available.
External HDD Boot Support	**Enabled** Disabled	Enables/Disables the boot option ROM for the second onboard hard disk controller, which drives the second parallel ATA channel and the two SATA channels. *Note: When set to 'Enabled', the system must be rebooted in order for the SATA device to be visible in the boot option ROM initialization.*
Network Boot Support	Enabled **Disabled**	Disable/Enable PXE network boot support to LAN. *Note: When set to 'Enabled', the system must be rebooted in order for the Intel Boot Agent device to be visible in the Boot Device Priority Menu.*

Notes

Due to the lack of upper memory area space for option ROM initialization, it is not possible to enable external HDD boot support and network boot support at the same time. Only the first detected option ROM will be recognized.

8.5.2 Graphics Configuration Submenu

Feature	Options	Description
Graphic Interface Configuration	No option	
Internal Adapter Mode	**Disabled** Primary Controller Secondary Controller	Mode for internal graphics controller when an external video device is present.
Graphics Memory Size	2 - **24** - 254	Select graphics memory size in MBytes for the graphic system. Use even numbers of MBytes only.
Driver Control Initialization	Enabled **Disabled**	Uses OS driver for all graphics system initialization beyond internal initialization to secondary controller status.
Boot Display Device	**CRT & LFP** CRT only LFP only TV only	Select the display device used during bootup.
Local Flat Panel Type	**Autodetect** QVGA 1x18 VGA 1x18 SVGA 1x18 XGA 1x18 Customized EDID™	Select a predefined LFP type or set to AUTO to let the BIOS auto detect the attached LVDS panel. Auto detection is performed by reading an EDID™ data set via the panel DDC bus. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.*
Backlight Control	0%, 25%, 50%, 75%, **100%**	Set local flat panel backlight control value.
TV Standard	**NTSC** PAL HDTV	Select the TV display standard.
TV Resolution	**Low** Medium High	Select the television resolution. *For NTSC, Low=720x480, Medium=800x600, High=1024x768* *For PAL, Low=720x576, Medium=800x600, High=1024x768* *For HDTV, Low=720x480, Medium=1280x720, High=1920x1080*

8.5.3 Cache Configuration Submenu

Feature	Options	Description
Cache Configuration	No option	
Cache Enable	**Enabled** Disabled	Enables/Disables the L1 and L2 system cache.
L2 Cache Enable	**Enabled** Disabled	Enables/Disables only the L2 system cache.
Cache Mode	**Write-Back** Write Through	Select the cache mode write-back or write-through.
Cache Allocate	Enabled **Disabled**	Select if a cache line should be allocated before write.

8.5.4 PCI Configuration Submenu

Feature	Options	Description
PCI Interrupt Steering	**No Option**	
PCI INTA#	3, 4, 5, 7, 9, **10**, 11, 12, 14, 15	Select fixed IRQ for PCI interrupt line. *Note: Make sure that the selected IRQ is not assigned to a legacy I/O.*
PCI INTB#	3, 4, 5, 7, 9, 10, **11**, 12, 14, 15	Select fixed IRQ for PCI interrupt line. *Note: Make sure that the selected IRQ is not assigned to a legacy I/O.*
PCI INTC#	3, 4, 5, 7, 9, **10**, 11, 12, 14, 15	Select fixed IRQ for PCI interrupt line. *Note: Make sure that the selected IRQ is not assigned to a legacy I/O.*
PCI INTD#	3, 4, 5, 7, 9, 10, **11**, 12, 14, 15	Select fixed IRQ for PCI interrupt line. *Note: Make sure that the selected IRQ is not assigned to a legacy I/O.*

8.5.5 I/O Interface Configuration Submenu

Feature	Options	Description
I/O Interface Configuration Submenu	**No Option**	
Floppy Support	**Enabled** Disabled	Enables/Disables the onboard Super I/O floppy device. *Note: The floppy drive and the parallel port share the same pins on the conga-XLX. Only one device can be driven at any given time. If the floppy drive is to be used, the parallel port must be disabled.*
Keyboard Support	**Enabled** Disabled	Enables/Disables keyboard support. *Note: If the keyboard support is disabled it is not possible to enter system setup. If the keyboard is not used by the application then the POST process can be sped up by disabling keyboard support.*
Serial Port 1	Disabled **3F8/IRQ4** 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Specifies the I/O base address and IRQ of serial port 1.
Serial Port 2	Disabled 3F8/IRQ4 **2F8/IRQ3** 3E8/IRQ4 2E8/IRQ3	Specifies the I/O base address and IRQ of serial port 2.
Serial Port 2 Mode	**Normal** IrDA ASK IR	Specifies the mode for serial port 2.
IR Duplex Mode	Full Duplex **Half Duplex**	Select IRDA full or half duplex function.
IR I/O Pin Select	SINB/SOUTB **IRRX/RTX**	Select the receive and transmit pins for IRDA mode.
Parallel Port Address	**Disabled** 378 278 3BC	Specifies the I/O base address used by the parallel port. *Note: The parallel port and the floppy drive share the same pins on the conga-XLX. Only one device can be driven at any given time. If the parallel port is to be used, the floppy drive must be disabled.*
Parallel Port Mode	**Compatible** Bi-directional EPP 1.7 EPP 1.9 ECP	Specifies the parallel port mode.
Parallel Port IRQ	**None** IRQ5 IRQ7 IRQ9 IRQ10 IRQ11	Specifies the interrupt for the parallel port.
Parallel Port DMA	**None** DMA1 DMA3	Specifies the DMA channel for the parallel port in ECP mode.
External Super I/O Configuration Menu	**Submenu**	Submenu for external Super I/O configuration. *Note: This submenu is only selectable if a external Winbond W83627HG Super I/O is present.*

Feature	Options	Description
LPC DRQ Routing	**Onboard Super I/O** External LPC Device	Select if LPC DRQ line should be routed to the onboard Super I/O or the external LPC Device. If the onboard floppy drive or the ECP parallel port is enabled, the LPC DRQ has to be routed to the onboard Super I/O controller.
Network Controller	Disabled **Enabled**	Enables/Disables the onboard PCI network controller.
System Beeper	Disabled **Enabled**	Enables/Disables the external system beeper.

8.5.6 External Super I/O Configuration Submenu

Feature	Options	Description
External Super I/O Configuration Submenu	**No Option**	
Floppy Support	Enabled **Disabled**	Enables/Disables floppy device of the external Super I/O controller. *Note: The external Floppy only can be used, if the onboard Floppy is disabled. Otherwise the there is a resource conflict.*
Serial Port 1	**Disabled** 3E8/IRQ11 3E8/IRQ10 2E8/IRQ11 2E8/IRQ10	Specifies the I/O base address and IRQ of the serial port 1 of the external Super I/O controller.
Serial Port 2	**Disabled** 3E8/IRQ11 3E8/IRQ10 2E8/IRQ11 2E8/IRQ10	Specifies the I/O base address and IRQ of the serial port 2 of the external Super I/O controller.
Parallel Port	**Disabled** 378 278 3BC	Specifies the I/O base address used by the parallel port of the external Super I/O controller.
Parallel Port Mode	**SPP** EPP 1.7 EPP 1.9 ECP	Specifies the parallel port mode of the external Super I/O controller.
Parallel Port IRQ	Disabled **IRQ5** IRQ7	Specifies the interrupt for the parallel port of the external Super I/O controller.
Parallel Port DMA	Disabled DMA1 **DMA3**	Specifies the DMA channel for parallel port in ECP mode.

Note

This submenu is only available if an external Winbond W83627HG Super I/O controller is present in the system. The configuration base I/O address of the Super I/O has to be 0x4E and 0x4F.

8.5.7 USB Configuration Submenu

Feature	Options	Description
USB 2.0 Configuration	**No Option**	
OHCI	Disabled **Enabled**	Enables/Disables OHCI PCI header
EHCI	Disabled **Enabled**	Enables/Disables EHCI PCI header
UDC	**Disabled** Enabled	Enables/Disables UDC PCI header
Legacy USB Support	**Enabled** Disabled	Enables/Disables legacy USB support for keyboard/mouse emulation and legacy USB boot support. *Note: If legacy USB support is disabled, it is not possible to enter the system Setup program with USB keyboard.*

8.5.8 Watchdog Configuration Submenu

Feature	Options	Description
Watchdog Parameter Configuration	**No Option**	
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Selects the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during bootup by performing a reset.
Runtime Watchdog	**Disabled** One time trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to '*One time trigger*' the watchdog will be disabled after the first trigger. If set to *'Single event'*, every stage will be executed only once, then the watchdog will be disabled. If set to *'Repeated event'* the last stage will be executed repeatedly until a reset occurs.
Delay	see Post Watchdog	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	**NMI** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 1 is reached.
Event 2	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	0.5sec 1sec 2sec 5sec **10sec** 30sec 1min 2min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.

8.5.9 Hardware Monitoring Submenu

Feature	Options	Description
CPU Temperature	no option	Current processor die temperature.
Board Temperature	no option	Current board temperature.
VCore	no option	Current Core voltage reading.
VMemory	no option	Current Memory voltage reading.
+3.3Vin	no option	Current 3.3V reading.
+5Vin	no option	Current 5V reading.
VBAT	no option	Current VBAT reading.
FAN Speed	no option	Current FAN speed.

8.5.10 Boot Screen Configuration Submenu

Feature	Options	Description
Splash Screen	**Disabled** Enabled	*Disabled* displays normal POST diagnostic messages. *Enabled* displays OEM logo instead of POST messages. *Note: The default OEM logo is a dark screen.*
Clear Splash Screen	**Disabled** Enabled	Clear the splash screen after option ROM initialization.
Splash Screen Timeout	**0** - 65535	Determines the time, the splash screen is displayed during option ROM initialization.
Summary Screen	**Disabled** Enabled	Enable/Disable the summary screen during bootup.
Summary Screen Timeout	**0** - 65535	Determines the time, the summary screen is displayed before booting any OS.

8.6 Performance Control

Select the 'Performance Control' submenu from the main setup menu and press enter or press the related letter in front of the menu to enter the 'Performance Control' Setup screen. The menu is used for setting system clocks.

Feature	Options	Description
System Clock Mode	Hardware Strapping **Manual Settings**	Selects if system clocks should be determined by manual settings or by hardware bootup straps.
CPU Clock Speed	333 Mhz 366 Mhz 400 Mhz 433 Mhz 466 Mhz **500 MHz**	Set the CPU clock speed. *Hardware Strapping = CPU Clock Speed: 400MHz*

Note

congatec strongly recommends that when using the 'Manual Settings' option the 'CPU Clock Speed' should be set to the default value, which is 500MHz. If an alternative setting for the 'CPU Clock Speed' must be used then it's recommended that this setting be extensively evaluated in conjunction with the complete system.

8.7 Power Management

Select the 'Power Management' submenu from the 'Main Menu' and press enter or press the related letter in front of the menu to enter the 'Power Management' setup screen. This menu is used for setting ACPI and APM configuration.

Feature	Options	Description
BIOS PM at Bootup	**Disabled** Enabled	BIOS will turn on Legacy PM before booting the OS.
APM Available	**Yes** No	Select APM Interface available for use.
ACPI Available	**Yes** No	Select ACPI Interface available for use.
CPU Clock Gating	Disabled **Enabled**	Set to *Enabled* for power savings.
Chipset Clock Gating	Disabled **Enabled**	Set to *Enabled* for power savings
Active Cooling TP	**Disabled** 40°C 50°C 60°C 70°C	Determines the active cooling trip point for the CPU fan in ACPI mode.
Power Loss Control (see Note 2)	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. *Remain Off* keeps the power off until the power button is pressed. *Turn On* restores power to the computer. *Last State* restores the previous power state before power loss occurred. *Note: Only works with an ATX type power supply.*
Power Button Control	Instant Off **ACPI Mode**	Use ACPI Mode with 4 seconds Soft Off or not.
Suspend Mode Control	**S1-State** S3-State	Determines if the system suspends to S3 or to S1 power save state.
CMB Shutdown Mode	**G3 Mech Off** S5 Soft Off	Determines the shutdown behavior of the Control Method Battery. *G3 Mech Off* switch off all supply voltages. *S5 Soft Off* switch off all supply voltages except 5V Standby.
Watchdog ACPI Event (see Note 1)	**Shutdown** Restart Sleep	Selects the event that is initiated by the watchdog APCI event (see note 1 below).
GPE1 Function	**No Function** Lid Switch	Determines the functionality of GPE1 (pin 42 of X4) *Note: Resume with LID switch is only available from S1 state.*
GPE2 Function	**No Function** Sleep Button	Determines the functionality of GPE2 (pin 89 of X4) *Note: Sleep button option in ACPI mode is only available when Suspend Mode Control is set to S3 state.*

Note 1

In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

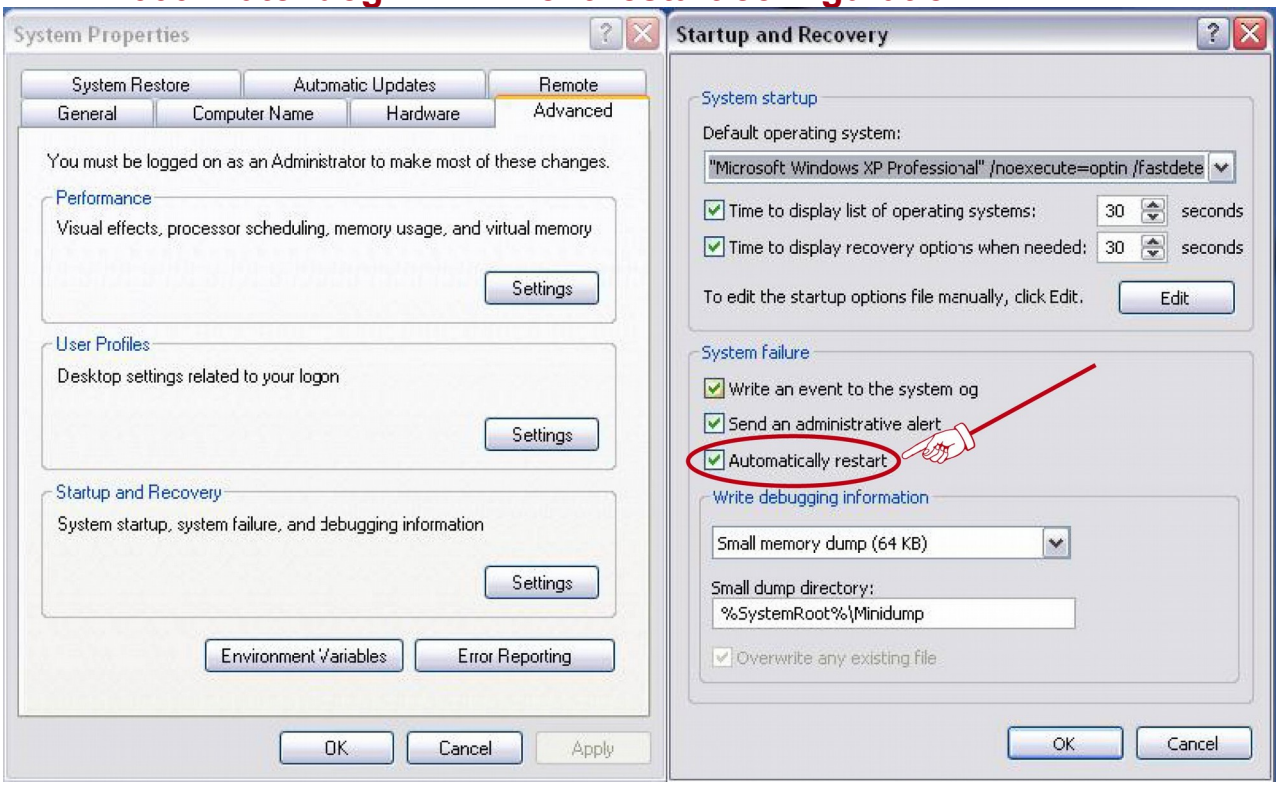
For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP/2000 there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very brief blue-screen the system will restart.

You can enable this setting buy going to the "System Properties" dialog box and choosing the "Advanced" tab. Once there choose the "Settings" button for the "Startup and Recovery" section. This will open the "Startup and Recovery" dialog box. In this dialog box under "System failure" there are three check boxes that define what Windows will do when a fatal error has been detected. In order to ensure that the system restarts after a 'Watchdog ACPI Event" that is set to 'Restart', you must make sure that the check box for the selection "Automatically restart" has been checked. If this option is not selected then Windows will remain at a blue-screen after a 'Watchdog ACPI Event" that has been configured for 'Restart' has been generated. The following is a Windows screen-shot showing the proper configuration.

Win XP/2000 Watchdog ACPI Event restart configuration



Note 2

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed*

that the system was switched off properly.

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

3. *Unlike other module designs available in the embedded market, a CMOS battery is not required by congatec modules to support the 'Power Loss Control' feature.*

8.8 Boot Device Priority

Feature	Options	Description
Boot Order (Device Order 1-6)	None Floppy Disk CD-ROM Drive Hard Drive USB Hard Drive/Flash Drive USB Floppy Disk USB CD-ROM Drive Network Drive	Determines the boot order for each device. The default boot order is: 1. None 2. CD-ROM Drive 3. Hard Drive 4. USB Floppy Disk 5. USB Hard Drive/Flash Disk 6. USB CD-ROM Drive 7. Network Boot

9 Additional BIOS Features

The conga-XLX uses an Insyde XpressROM based congatec Embedded BIOS that is stored in the Firmware Hub (FWH) and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as X800R115, where X800 is the congatec internal project name, R is the identifier for a BIOS ROM file, 1 is the so called feature number and 10 is the major and minor revision number.

9.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

10 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Audio Codec '97 Component Specification, Version 2.3 (AC '97)	http://www.intel.com/design/chipsets/audio/
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.2	http://www.pcisig.com/specifications
PCI Express Base Specification, Revision 1.0a	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 1.0a	http://www.serialata.org