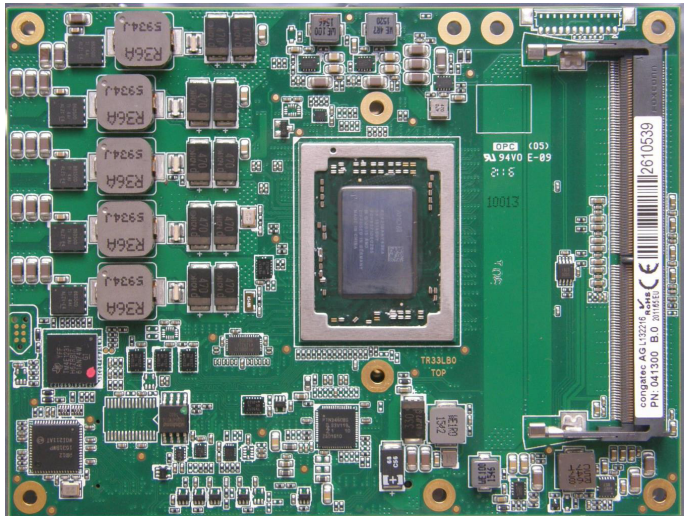


COM Express™ conga-TR3

3rd Generation AMD Embedded R- and G-Series SoC

User's Guide

Revision 1.2

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2016.02.02	AEM	• Preliminary release
0.2	2016.03.22	AEM	• Updated the whole document.
1.0	2016.07.26	BEU	• Updated form factors in section 1 "Introduction" • Updated section 2.5 "Power Consumption", 2.7 "Environmental Specifications" and 4 "Cooling Solutions" • Added section 10 "System Resources", 11 "BIOS Setup Description" and 12 "Additional BIOS Features" • Final release
1.1	2016.08.30	BEU	• Updated title page • Added Brown Falcon variant in section 1 "Introduction" • Added Brown Falcon PEG and DDI information in section 2.1 "Feature List" • Updated section 2.5 "Power Consumption" • Added Brown Falcon variant in section 2.5 "Power Consumption" • Added SATA MUX switch in section 3 "Block Diagram" • Added Brown Flacon PEG information in section 6 "Connector Subsystems Rows A, B, C, D" and in section 6.2.2 "PCI Express Graphics (PEG)" • Added Brown Falcon DDI information in section 6 "Connector Subsystems Rows A, B, C, D" and in section 6.2.3 "Digital Display Interface" • Added SATA Switch options and note in section 6.1.1 "Serial ATA™ (SATA)" • Added Wake on USB restriction note in section 8.5 "USB Host Controller" • Updated PEG note in section 9.3 "C-D Connector Signal Descriptions" • Updated DDI note in section 9.3 "C-D Connector Signal Descriptions"
1.2	2016.09.21	BEU	• Updated Com Express™ types in section 1 "Introduction" • Updated caution in section 4.3 "Heatspreader Dimensions" • Removed image in section 6 "Connector Rows A - B, C - D" • Added note about USB limitations in sections 6.1.2 "USB 2.0", 6.2.4 "USB 3.0" and 8.5 "USB Host Controller" • Added note about PXE limitation in section 6.1.4 "Gigabit Ethernet" • Added note about required graphic driver in sections 6.1.10 "LVDS" and 6.2.3 "Digital Display Interface"

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-TR3. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide
COM Express™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

Disclaimer

The information contained within this user's guide, including but not limited to any product specification, is subject to change without notice.

congatec AG provides no warranty with regard to this user's guide or any other information contained herein and hereby expressly disclaims any implied warranties of merchantability or fitness for any particular purpose with regard to any of the foregoing. congatec AG assumes no liability for any damages incurred directly or indirectly from any technical or typographical errors or omissions contained herein or for discrepancies between the product and the user's guide. In no event shall congatec AG be liable for any incidental, consequential, special, or exemplary damages, whether based on tort, contract or otherwise, arising out of or in connection with this user's guide or any other information contained herein or the use thereof.

Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Copyright Notice

congatec AG has made every attempt to ensure that the information in this document is accurate yet the information contained within is supplied "as-is".

Trademarks

Product names, logos, brands, and other trademarks featured or referred to within this user's guide, or the congatec website, are the property of their respective trademark holders. These trademark holders are not affiliated with congatec AG, our products, or our website.

Warranty

congatec AG makes no representation, warranty or guaranty, express or implied regarding the products except its standard form of limited warranty (“Limited Warranty”) per the terms and conditions of the congatec entity, which the product is delivered from. These terms and conditions can be downloaded from www.congatec.com. congatec AG may in its sole discretion modify its Limited Warranty at any time and from time to time.

The products may include software. Use of the software is subject to the terms and conditions set out in the respective owner’s license agreements, which are available at www.congatec.com and/or upon request.

Beginning on the date of shipment to its direct customer and continuing for the published warranty period, congatec AG represents that the products are new and warrants that each product failing to function properly under normal use, due to a defect in materials or workmanship or due to non conformance to the agreed upon specifications, will be repaired or exchanged, at congatec’s option and expense.

Customer will obtain a Return Material Authorization (“RMA”) number from congatec AG prior to returning the non conforming product freight prepaid. congatec AG will pay for transporting the repaired or exchanged product to the customer.

Repaired, replaced or exchanged product will be warranted for the repair warranty period in effect as of the date the repaired, exchanged or replaced product is shipped by congatec, or the remainder of the original warranty, whichever is longer. This Limited Warranty extends to congatec’s direct customer only and is not assignable or transferable.

Except as set forth in writing in the Limited Warranty, congatec makes no performance representations, warranties, or guarantees, either express or implied, oral or written, with respect to the products, including without limitation any implied warranty (a) of merchantability, (b) of fitness for a particular purpose, or (c) arising from course of performance, course of dealing, or usage of trade.

congatec AG shall in no event be liable to the end user for collateral or consequential damages of any kind. congatec shall not otherwise be liable for loss, damage or expense directly or indirectly arising from the use of the product or from any other cause. The sole and exclusive remedy against congatec, whether a claim sound in contract, warranty, tort or any other legal theory, shall be repair or replacement of the product only.

Certification

congatec AG is certified to DIN EN ISO 9001 standard.

Technical Support

congatec AG technicians and engineers are committed to providing the best possible technical support for our customers so that our products can be easily used and implemented. We request that you first visit our website at www.congatec.com for the latest documentation, utilities and drivers, which have been made available to assist you. If you still require assistance after visiting our website then contact our technical support department by email at support@congatec.com

Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
T.O.M.	Top of memory = max. DRAM installed
HDA	High Definition Audio
I/F	Interface
N.C.	Not connected
N.A.	Not available
cBC	congatec Board Controller
TBD	To be determined

Contents

List of Tables

1 Introduction

COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express™ modules are available in following form factors:

- Mini 84mm x 55mm
- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x110mm

Table 1 COM Express™ 2.1 pinout types

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports	USB 2.0/ USB 3.0	Display Interfaces
Type 1	A-B	Up to 6			1	8 / 0	VGA, LVDS
Type 2	A-B C-D	Up to 22	32 bit	1	1	8 / 0	VGA, LVDS,PEG/SDVO
Type 3	A-B C-D	Up to 22	32 bit		3	8 / 0	VGA,LVDS,PEG/SDVO
Type 4	A-B C-D	Up to 32		1	1	8 / 0	VGA,LVDS,PEG/SDVO
Type 5	A-B C-D	Up to 32			3	8 / 0	VGA,LVDS,PEG/SDVO
Type 6	A-B C-D	Up to 24			1	8 / 4	VGA,LVDS,PEG, 3x DDI
Type 10	A-B	Up to 4			1	8 / 0	1x DDI

conga-TR3 modules utilize the Type 6 pinout definition and are COM Express 2.1 Compliant. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are a legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 6 pinout provides the ability to offer PCI Express, Serial ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

conga-TR3 Options Information

The conga-TR3 is available in four variants. This user's guide describes these variants. The table below shows the different configurations available. Check the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Table 2 conga-TR3 Options

Part-No.	041300	041301	041302	041320
SoC	AMD Embedded RX-421BD	AMD Embedded RX-418GD	AMD Embedded RX-216GD	AMD Embedded GX-217GI
CPU Freq.	2.1/3.4 GHz Quad Core	1.8/3.2 GHz Quad Core	1.6/3.0 GHz Dual Core	1.7/2.0 GHz Dual Core
L2 Shared Cache	2 MB	2 MB	1 MB	1 MB
Memory (DDR4)	2133 MT/s dual channel	2133 MT/s dual channel	1600 MT/s dual channel	1600 MT/s dual channel
GPU Freq / Compute Unit	800 MHz / 8 CU	800 MHz / 6 CU	800 MHz / 4 CU	758 MHz / 4 CU
Graphics Engine	AMD Radeon™ R7 Graphics	AMD Radeon™ R6 Graphics	AMD Radeon™ R5 Graphics	AMD Radeon™ R6 Graphics
PCIe	3 PCIe Gen 3 ports	3 PCIe Gen 3 ports	3 PCIe Gen 3 ports	3 PCIe Gen 3 ports
PEG	1 PEG Gen 3 port (x8 lanes)	1 PEG Gen 3 port (x8 lanes)	1 PEG Gen 3 port (x8 lanes)	1 PEG Gen 3 port (x4 lanes)
USB 3.0	Up to 4 ports	Up to 4 ports	Up to 4 ports	Up to 4 ports
DDI	Dual-mode DP 1.2	Dual-mode DP 1.2	Dual-mode DP 1.2	Dual-mode DP 1.2
LVDS/eDP	LVDS	LVDS	LVDS	LVDS
SoC TDP/cTDP	15 / 12-35 W	15 / 12-35 W	15 / 12-15 W	15 / 12-15 W

2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 6 (Basic size 95 x 125mm). Compliant with COM Express 2.1 specification.	
SoC	3rd Generation AMD Embedded R-Series (FP4) SoC, with TDP ranging from 12-35W	
Memory	SO-DIMM DDR4 up to 2133 MT/s. Supports up to 32GB with 2x 16GB SO-DIMM modules (ECC and non-ECC). Sockets located top and bottom side of module.	
Chipset	Integrated in the SoC	
Audio	High Definition Audio (HDA) interface	
Ethernet	1 Gigabit Ethernet support via the onboard Intel® Ethernet Controller i211.	
Graphics Options	AMD Radeon 3rd Generation GCN, Unified Video Decoder 6 (4K H.265 and H.264), Video Compression Engine 3.1 (4K H.264 encode), OpenGL 4.4, OpenCL®2.0, DirectX®12, full HSA support, up to three independent displays.	
	LVDS (Integrated flat panel interface with 25-112MHz single/dual-channel Transmitter). Supports: - Single-channel LVDS interface: 1 x 18 bpp or 1 x 24 bpp. - Dual-channel LVDS interface : 2 x 18 bpp or 2 x 24 bpp. - VESA standard or JEIDA data mapping - Automatic Panel Detection via Embedded Panel Interface based on VESA EDID™ 1.3. - Resolution up to 1920x1200 in dual channel LVDS mode. Optional eDP interface (assembly option) **NOTE:** Either eDP or LVDS signals supported. Both not supported.	1 PEG Gen 3 port (x8 Merlin Falcon / x4 Brown Falcon) 2 dedicated DDIs (Digital Display Interfaces) with support for - 2 DisplayPort 1.2 (resolution up to 4k @ 60Hz). - 2 HDMI 2.0 port (requires external level shifter) - 2 DVI port (requires external level shifter). 1 Optional DDI (assembly option) **NOTE:** To support HDMI/DVI, an external level shifter (e.g PTN 3360D) needs to be implemented on the user's carrier board. Max. two simultaneous HDMI display outputs in all assembly variants. Merlin Falcon has 3x DDI, but Brown Falcon only 2x DDI.
Peripheral Interfaces	2 Serial ATA® (6 Gb/s) 3 PCI Express® 3.0 ports (8 GT/s). 4 USB 2.0 4 USB 3.0/2.0 2 UART 2 ExpressCard	LPC Bus SDIO interface (shared with GPIOs I²C Bus, Fast Mode, multimaster SM Bus SPI
BIOS	AMI Aptio® UEFI 5.x firmware; 8 MByte serial SPI with congatec Embedded BIOS features	
Security	Optional TPM 1.2/2.0	
Power Management	ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).	
cBC	Multi-stage watchdog, manufacturing and board information, board statistics, I2C bus, Power loss control.	

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 11 of this user's guide to determine what options are available on your particular module.

2.2 Supported Operating Systems

The conga-TR3 supports the following operating systems.

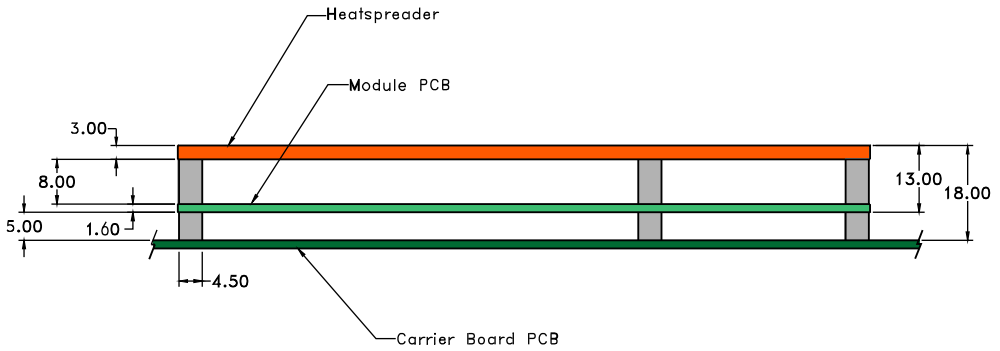
- Microsoft® Windows® 10
- Microsoft® Windows® 10 IOT enterprise
- Microsoft® Windows® 8.1
- Microsoft® Windows® 8.1 Embedded Standard
- Microsoft® Windows® 7
- Microsoft® Windows® 7 Embedded Standard
- Linux

Note

To improve the graphic performance of conga-TR3 after installing Microsoft® Windows® Operating System, congatec AG recommends the installation of AMD catalyst driver.

2.3 Mechanical Dimensions

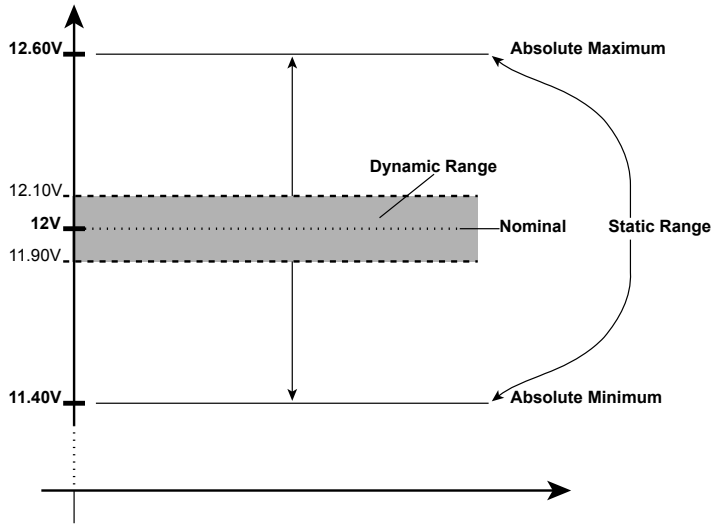
- 95.0 mm x 125.0 mm (3.74" x 4.92")
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm.



2.4 Supply Voltage Standard Power

- 12V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Table 4 Electrical Characteristics

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured using the following test setup:

- conga-TR3 COM
- modified carrier board to measure the power consumption of the COM
- product specific cooling solution with the highest cooling capacity
- running Windows 7 (64 bit)

Note

All peripherals were powered externally and therefore did not influence the measured values.

The power consumption values were recorded during the following S-states:

Table 5 System State Description

System State	Description
S0: Minimum value	COM set to lowest frequency mode (LFM) with minimum core voltage during desktop idle. The CPU was stressed to its maximum frequency in this S-state.
S0: Maximum value	COM set to highest frequency mode (HFM/Turbo Boost). The CPU was stressed to its maximum frequency in this S-state.
S0: Peak value	The worst case power consumption value shows the peak value over a short period of time. Highest power spike during the measurement of "S0: Maximum value". This value should be taken into consideration when designing the system's power supply to ensure that the power supply is sufficient during worst case scenarios
S3	COM is powered by VCC_5V_SBY.
S5	COM is powered by VCC_5V_SBY.

Processor Information

The tables below provide additional information about the power consumption data for each of the conga-TR3 variants offered. The values are recorded at various operating modes.

Table 6 AMD Embedded RX-421BD 2.1/3.2GHz Quad Core 2MB L2 Cache (28nm)

Part No. 041300	Hardware revision A.0 / BIOS revision TR3R016				
Memory Size	2x 4GB				
Power State	S0: Min	S0: Max	S0: Peak	S3	S5
Power consumption	0.24 A /2.85 W	4.33 A /51.93 W	8.6 A /103.2 W	0.08 A /0.41 W	0.07 A /0.35 W

Table 7 AMD Embedded RX-418GD 1.8/3.2GHz Quad Core 2MB L2 Cache (28nm)

Part No. 041301	Hardware revision A.0 / BIOS revision TR3R016				
Memory Size	2x 4GB				
Power State	S0: Min	S0: Max	S0: Peak	S3	S5
Power consumption	0.25 A /3 W	4.33 A /52.01 W	7.76 A /93.06 W	0.08 A /0.41 W	0.07 A /0.35 W

Table 8 AMD Embedded RX-216GD 1.6/3.0GHz Dual Core 1MB L2 Cache (28nm)

Part No. 041302	Hardware revision A.0 / BIOS revision TR3R016				
Memory Size	2x 4GB				
Power State	S0: Min	S0: Max	S0: Peak	S3	S5
Power consumption	0.4 A /4.78 W	3.72 A /44.63 W	5.27 A /63.21 W	0.08 A /0.41 W	0.06 A /0.32 W

Table 9 AMD Embedded GX-217GI 1.7/2.0GHz Dual Core 1MB L2 Cache (28nm)

Part No. 041320	Hardware revision A.0 / BIOS revision TR3R016				
Memory Size	2x 4GB				
Power State	S0: Min	S0: Max	S0: Peak	S3	S5
Power consumption	T.B.D	T.B.D	T.B.D	T.B.D	T.B.D

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

2.6 Supply Voltage Battery Power

- 2.3V - 3.5V DC
- Typical 3V DC

2.6.1 CMOS Battery Power Consumption

Table 10 CMOS Battery Power Consumption

RTC: measured with conga-TR3/421BD	Voltage	Current
-10°C	3V DC	2,19 µA
20°C	3V DC	2,84 µA
70°C	3V DC	4,77 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

2.7 Environmental Specifications

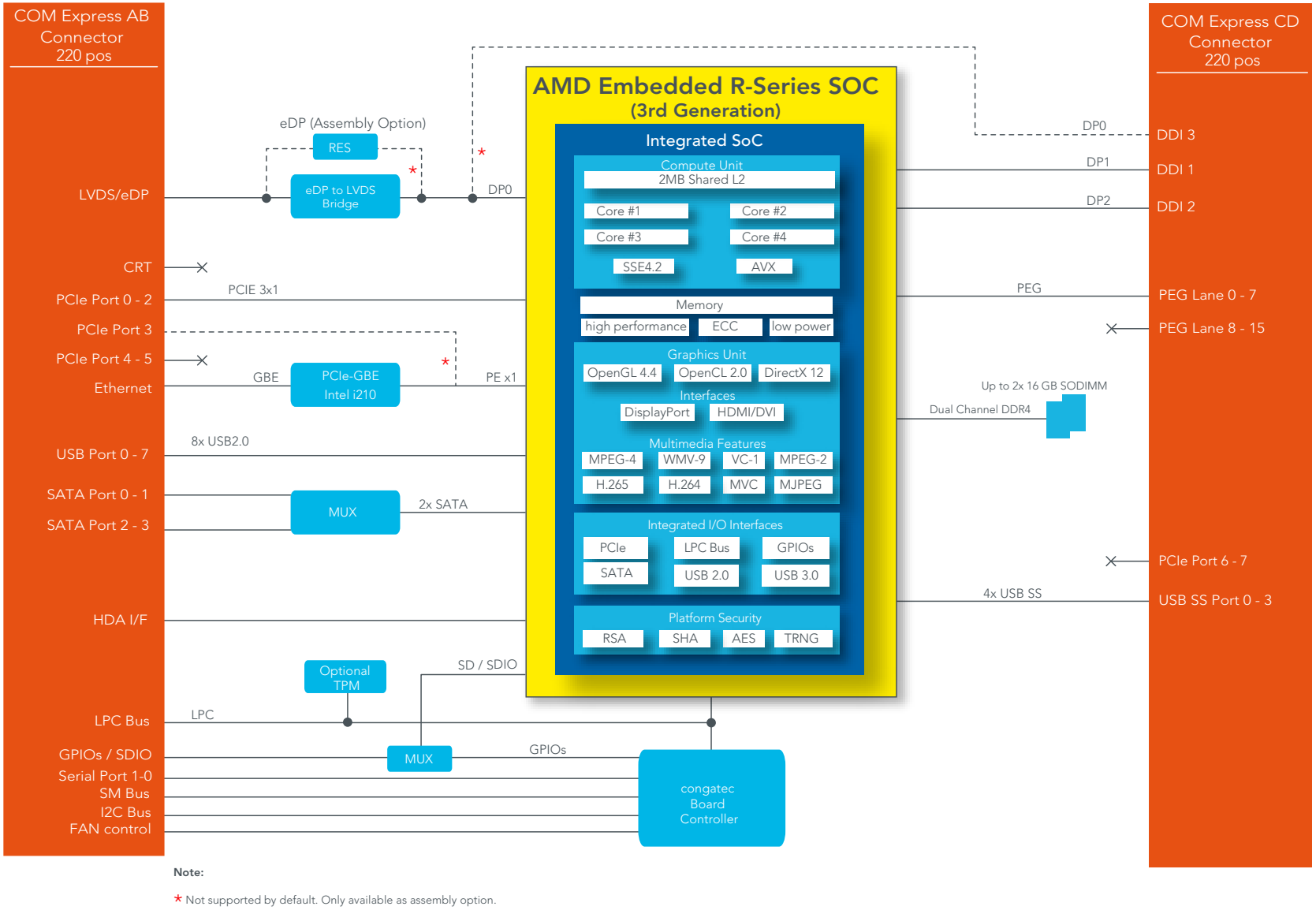
Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



Note:

* Not supported by default. Only available as assembly option.

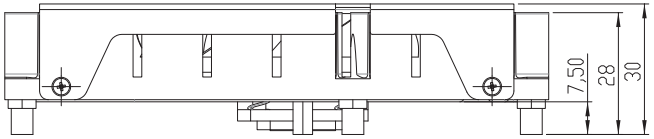
4 Cooling Solutions

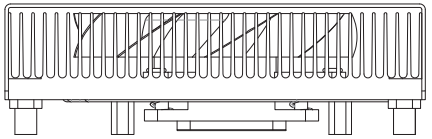
congatec AG offers three cooling solutions for the conga-TR3:

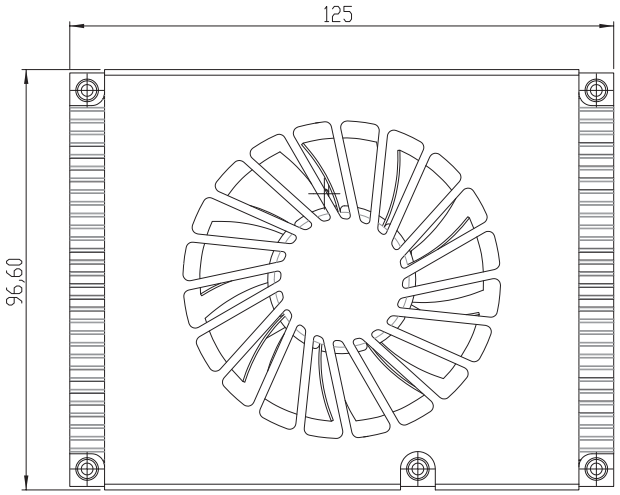
- Active cooling solution (CSA)
- Passive cooling solution (CSP)
- Heatspreader

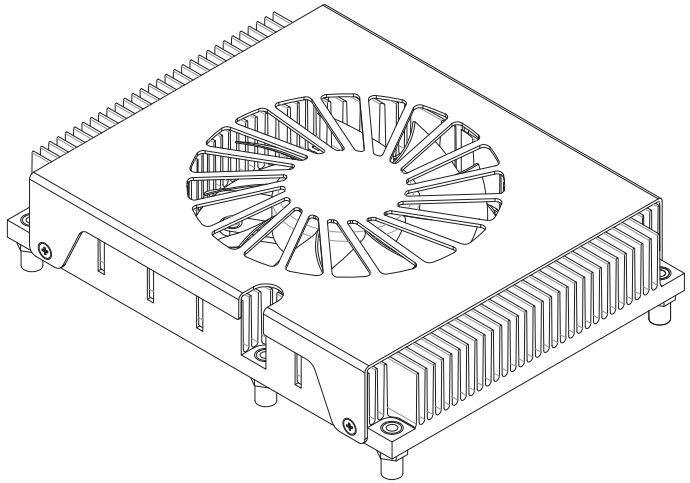
The dimensions of the cooling solutions are shown below and all measurements are in millimeters. The maximum torque specification for heatspreader screws is 0.3 Nm. Mechanical system assembly mounting shall follow the valid DIN/ISO specifications..

4.1 CSA Dimensions

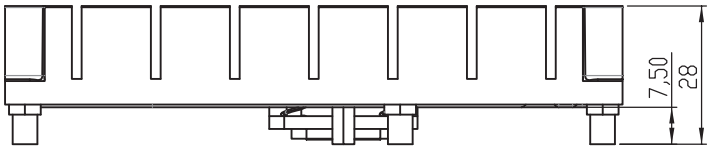


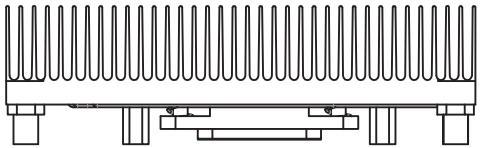


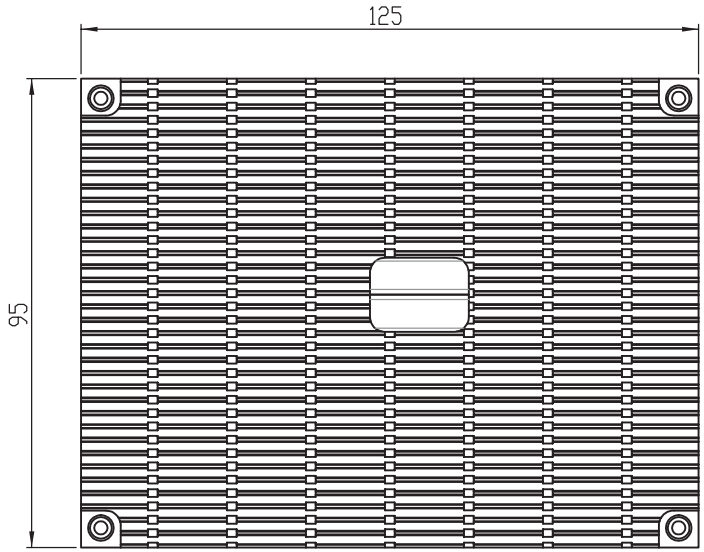


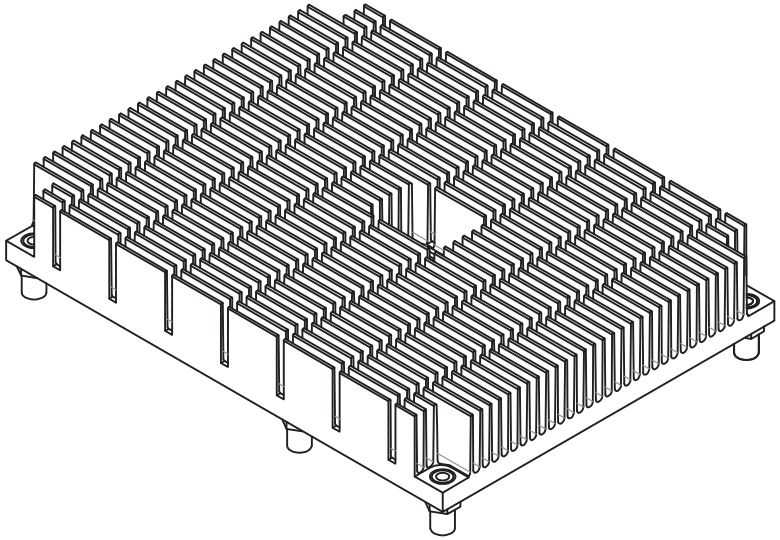


4.2 CSP Dimensions





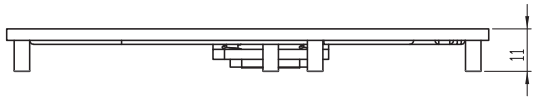


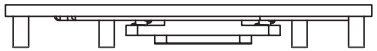


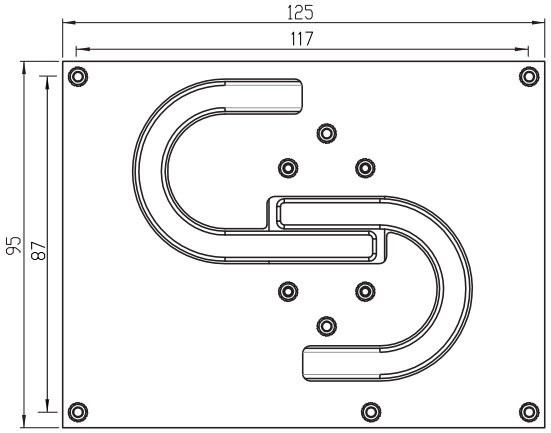
4.3 Heatspreader Dimensions

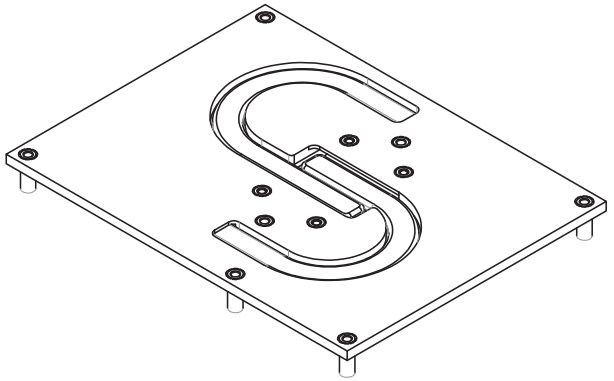
The heatspreader acts as a thermal coupling device to the module and is thermally coupled to the CPU via a thermal gap filler. On some modules, it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis thereby using the whole chassis as a heat dissipater.









Note

The gap pad material used on all heatspreaders contains silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.

Caution

The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.

For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.

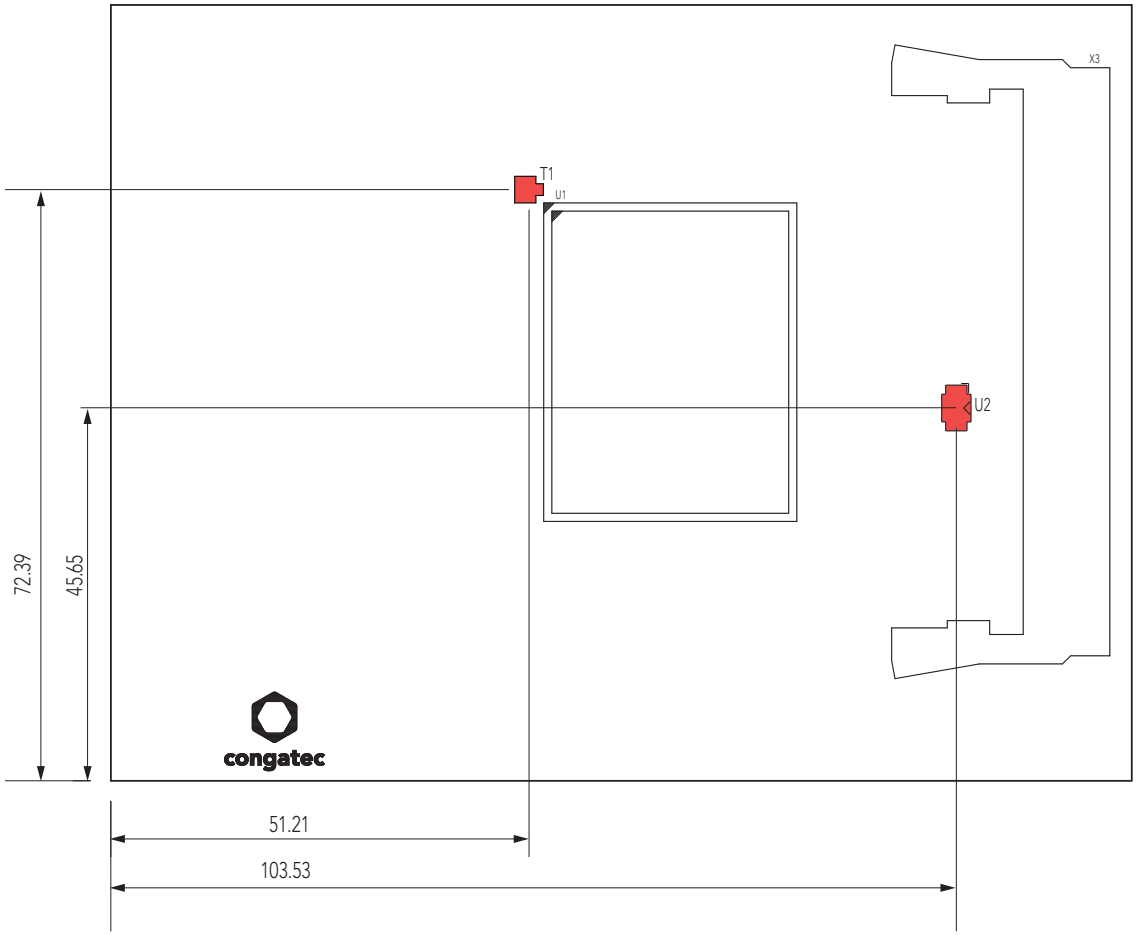
For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.

Also, do not exceed the maximum torque specified for the screws. Doing so may damage the module or/and the carrier board.

5 Onboard Temperature Sensor

Board Temperature Sensor:

Onboard the conga-TR3 is a sensor that measures the temperature of the board. The board sensor is located at the top of the conga-TR3 and is defined in CGOS API as CGOS_TEMP_BOARD. The sensor positions are designated as U2 and T1 as shown below:



All dimensions in mm

6 Connector Rows A - B, C - D

The conga-TR3 is connected to the carrier board via two 220-pin connectors (COM Express Type 6 pinout). These connectors are broken down into four rows (rows A-B and C-D).

6.1 Primary Connector Rows A and B

The following subsystems can be found on the primary connector rows A and B.

6.1.1 Serial ATA™ (SATA)

The conga-TR3 offers two SATA ports on the A-B connector rows. These ports are Gen 3 compliant, capable of up to 6.0 Gb/s transfer rate. Any of the ports can be configured to a lower transfer rate of 3.0 Gb/s or 1.5 Gb/s for saving power.

SATA Switch options:

- Port 0 + 1
- Port 0 + 3
- Port 2 + 1
- Port 2 + 3

The SATA controller supports three modes of operation - Native IDE, AHCI and Legacy IDE.

Note

Port combinations are COM Express ports. The conga-TR3 does not support RAID.

6.1.2 USB 2.0

The conga-TR3 offers eight USB 2.0 ports on the A-B connector rows. Four of the USB 2.0 ports can be combined with USB SuperSpeed signals to create USB 3.0 ports. The USB 2.0 ports support USB 1.1 and 2.0 compliant devices. For more information on how the USB host controllers are routed, see section 8.5.

Note

USB Ports 0-3 do not support Wake on USB from S3. USB Ports 5-6 are not powered during S3. Only USB Port 4 and 7 work during installation.

6.1.3 High Definition Audio (HDA) Interface

The conga-TR3 provides high definition audio interface. This interface supports multiple codec configurations on a single board as long as all codecs operate on the same voltage. The conga-TR3 supports up to three external HDA codecs. AC'97 audio codecs are not supported on the conga-TR3.

Note

COM Express modules only support up to three data inputs (AC_SDIN[0:2]) as described in COM Express Specification 2.0.

6.1.4 Gigabit Ethernet

The conga-TR3 offers Gigabit Ethernet with the integration of Intel i211 Ethernet Controller. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MDI0± to GBE0_MDI3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

Note

The GBE0_LINK# output is only active during a 100Mbit or 1Gbit connection. It is not active during a 10Mbit connection. This is a limitation of Ethernet controller since it only has 3 LED outputs - ACT#, LINK100# and LINK1000#.

The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TR3.

Network Booting (PXE) is not possible with D-Link Switch Model No. DGS-1008D.

6.1.5 LPC Bus

conga-TR3 offers the Low Pin Count (LPC) bus via the integrated controller hub. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific baseboard using this bus. Many devices are available for this cost-efficient, low-speed interface designed to support low bandwidth and legacy devices.

The LPC host bus controller supports one master DMA devices. See section 10.1.1 for more information about the LPC Bus.

Note

The conga-TR3 supports optional TPM 1.2/2.0 devices.

6.1.6 I²C Bus Fast Mode

The I²C bus is implemented through the congatec board controller and is accessed through the congatec CGOS driver and API. The controller provides a fast mode multi-master I²C bus that has maximum I²C bandwidth.

6.1.7 PCI Express™

The controller hub integrated in the AMD R-Series SoC provides four x1 general purpose PCIe ports. The conga-TR3 offers three of these ports on the A-B connector. The fourth PCIe port (port 3) is routed to the Intel i211 Ethernet controller for gigabit Ethernet support. This port can optionally be routed to the A-B connector if the Ethernet interface is not required. This option however requires a customized conga-TR3 variant (assembly option). The PCIe ports on the A-B connector are PCI Express™ Gen. 3 compliant and can be configured as 3 x1 or 1 x2 + 1 x1 links.

6.1.8 ExpressCard™

The conga-TR3 supports the implementation of ExpressCards, which require the dedication of one USB port or a x1 PCI Express link for each ExpressCard used.

6.1.9 VGA

The conga-TR3 does not support VGA interface.

6.1.10 LVDS

The conga-TR3 offers an LVDS interface on the A-B connector. The single/dual channel LVDS interface is provided by routing the onboard eDP to LVDS bridge device (NXP PTN3460) to one of the dedicated DisplayPort interfaces (DP0) of the R-Series SoC.

The eDP to LVDS bridge processes incoming DisplayPort stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format. The bridge supports single and dual channel signalling with color depths of 18 bits or 24 bits per pixel and pixel clock frequency up to 112 MHz. It also supports automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3, with resolution up to 1920x1200 in dual LVDS mode.

Note

For Windows 8.1 32bit, install the graphic driver version: 16.15.2001-16307a-300833C-AES through the device manager. For Ubuntu, upgrade to release version 15.10 and update to the latest graphic driver version to enable clone displays and & LVDS panels.

6.1.11 General Purpose Input/Output

The conga-TR3 offers general purpose inputs and outputs for custom system design. These GPIOs are multiplexed with SD/SDIO signals and are controlled by the cBC.

Note

The GPIO/SD selection is done via the BIOS setup menu.

6.1.12 Serial Ports/UART Interfaces

Two TTL compatible two wire ports are available on Type 6 COM Express modules. These pins are designated SER0_TX, SER0_RX, SER1_TX and SER1_RX. Data out of the module is on the _TX pins. Hardware handshaking and hardware flow control are not supported. The module asynchronous serial ports are intended for general purpose use and for use with debugging software that make use of the "console redirect" features available in many operating systems.

The conga-TR3 offers two UART interfaces via the congatec Board Controller. The UART controllers integrated in the cBC support up to 1MBit/s and can operate in low-speed, full-speed and high-speed modes. The UART interfaces are routed to the AB connector and require congatec driver to function.

Note

The UART interfaces do not support legacy COM port emulation.

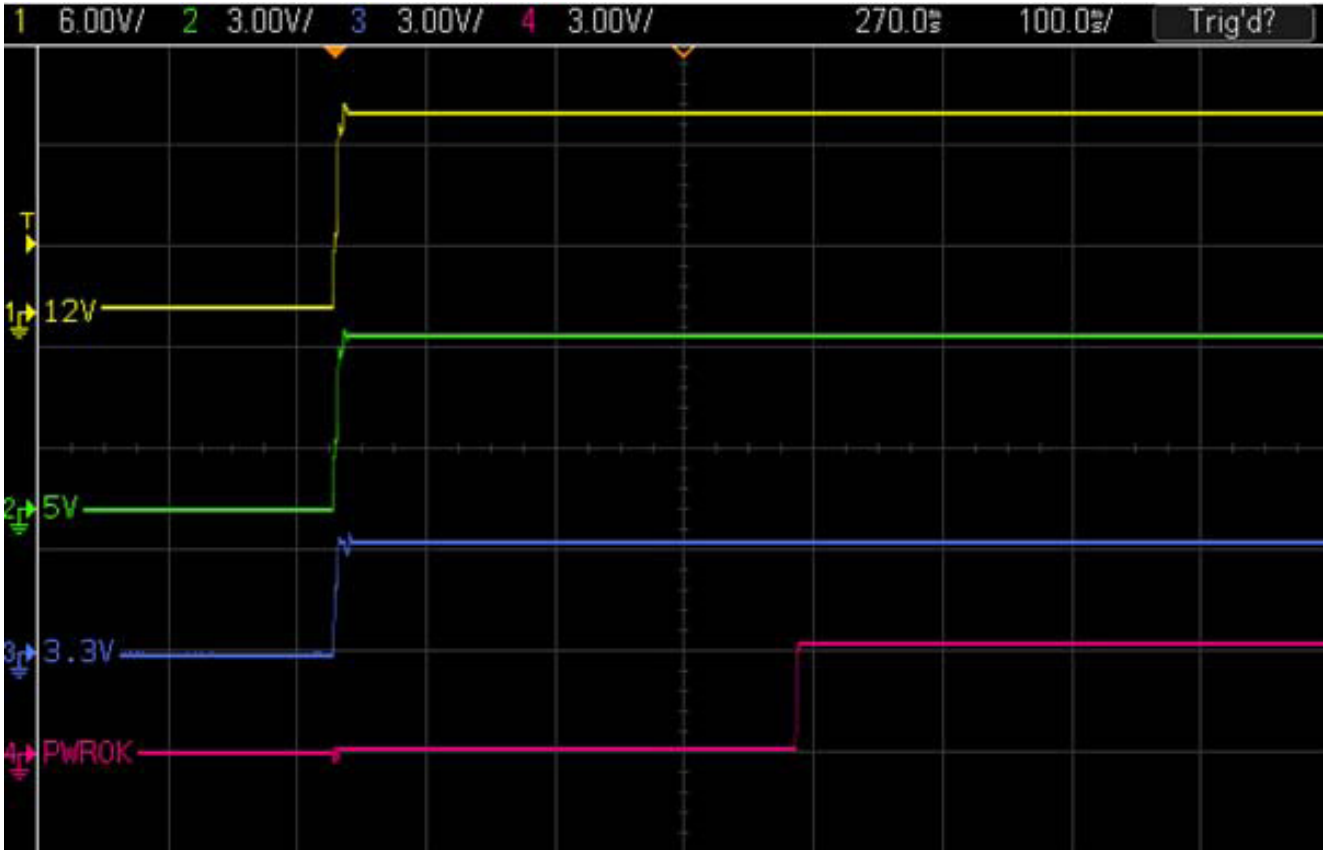
6.1.13 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. The PWR_OK is a 3.3V signal according to the COM Express Specification. The use of this input is optional.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. Although the PWR_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

A sample screenshot is shown below:



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the "power good" signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, it must be ensured that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-TR3 module is capable of generating it's own power good through the use of an internal monitor on the +12V ± 5% input voltage and/or the internal power supplies. The conga-TR3 also provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-TR3's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

12 volt input power is the sole operational power source for the conga-TR3. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-TR3 application:

- It has also been noticed that on some occasions, problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

6.1.14 Power Management

ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).

6.2 Secondary Connector Rows C and D

The secondary connector rows C-D have the following subsystems:

6.2.1 PCI Express™

The conga-TR3 does not offer PCI Express lanes on the C-D connector. For more information on supported PCI Express lanes, see section 6.1.7.

6.2.2 PCI Express Graphics (PEG)

The conga-TR3 Merlin variants support a x8 PEG interface. The default configuration of the PEG interface is 1 x8 link. The interface can be configured as a 2 x4 link via the setup menu. The Brown Falcon variant supports a x4 PEG interface.

6.2.3 Digital Display Interface

The conga-TR3 offers two dedicated Digital Display Interfaces (SoC DP1 and DP2) on the C-D connector by default. These interfaces support dual-mode DisplayPort 1.2 only. To support HDMI/DVI, an external level shifter e.g PTN3360D should be implemented on the user's carrier board. The conga-TR3 Merlin Falcon variants can support a third DDI interface on the C-D connector but only as an assembly option (customized variant). The customized variant with the optional DDI interface (third DDI interface) does not support LVDS/eDP interface.

The conga-TR3 supports up to three independent displays (a maximum of two independent HDMI/DVI displays only). Any combination of DisplayPort, HDMI/DVI and LVDS is possible as shown in the table below:

Table 11 Digital Display Interface

Display 1	Display 2	Display 3	Display 1 Max. Resolution	Display 2 Max. Resolution	Display 3 Max. Resolution
DP	DP	LVDS	3840x2160 @ 60Hz	3840x2160 @ 60Hz	1920x1200 @ 60Hz
DP	HDMI/DVI	LVDS	3840x2160 @ 60Hz	4096x2160 @ 24Hz 1920x1200 @ 60Hz	1920x1200 @ 60Hz
HDMI/DVI	HDMI/DVI	LVDS	4096x2160 @ 24Hz 1920x1200 @ 60Hz	4096x2160 @ 24Hz 1920x1200 @ 60Hz	1920x1200 @ 60Hz

Note

For Windows 8.1 32bit, install the graphic driver version: 16.15.2001-16307a-300833C-AES through the device manager. For Ubuntu, upgrade to release version 15.10 and update to the latest graphic driver version to enable clone displays and & LVDS panels.

The maximum HDMI resolution of 4096x2160 at 60 Hz is possible but requires a re-timer. The DVI resolutions are 1920x1200 @60Hz with reduced blanking and 1600x1200 @60Hz with VESA standard timing.

6.2.3.1 DisplayPort (DP)

The conga-TR3 offers two dual-mode DisplayPort 1.2 interfaces on the C-D connector. These interfaces support all mandatory features of the VESA DisplayPort Standard versions 1.2 including Multi-Stream Transport (MST) for monitor daisy-chaining, stereoscopic 3D frame transport, maximun bit rate of 5.4 Gbps and maximum display resolution of 3840x2160 at 60 Hz.Supported audio formats are linear PCM, Dolby Digital (AC-3), Dolby TrueHD, DTS, DTS-HD Master Audio and up to 8 channels.

6.2.3.2 HDMI

The conga-TR3 offers two HDMI interfaces on the C-D connector. The interfaces are based on HDMI 2.0 specification with support for 3D, 4K, Deep Color, maximum display resolution of 4096x2160 at 60Hz (re-timer is required for 4k @ 60Hz). Supported audio formats are AC-3 Dolby Digital, Dolby TrueHD, DTS-HD, DTS-HD Master Audio.

Note

Customized variants equipped with the third DDI interface (optional DDI interface) support only two independent HDMI/DVI displays.

To support the HDMI interface, an external level translator/shifter (e.g PTN3360D) should be implemented on the user's baseboard.

6.2.3.3 DVI

The conga-TR3 offers two single-link DVI interfaces on the C-D connector. These interfaces support maximum display resolutions of 1920x1200 at 60 Hz with reduced blanking or 1600x1200 at 60 Hz with VESA standard timing.

Note

To support the DVI interface, an external level translator/shifter (e.g PTN3360D) should be implemented on the user's baseboard.

6.2.4 USB 3.0

The conga-TR3 offers four USB SuperSpeed TX/RX differential signals on the COM Express CD connector to support four USB 3.0 ports (USB 0-3). Each USB 3.0 port requires corresponding USB 2.0 differential pairs for USB 3.0 support. The xHCI controller provided by the SoC's controller hub controls these ports and allows data transfers of up to 5 Gb/s with SuperSpeed, high-speed, full-speed and low-speed traffic support. For more information about how the USB host controllers are routed, see section 8.5.

Note

USB Ports 0-3 do not support Wake on USB from S3. USB Ports 5-6 are not powered during S3. Only USB Port 4 and 7 work during installation.

7 Additional Features

7.1 congatec Board Controller (cBC)

The conga-TR3 is equipped with Texas Instruments Tiva™ TM4E1231H6ZRB microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

7.1.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

7.1.2 Fan Control

The conga-TR3 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

A four wire fan must be used to generate the correct speed readout.

The congatec COM Express Type 6 and Type 10 modules use a Push-Pull output for the fan_pwm signal instead of the open drain output specified in the COM Express specification. Although this does not comply with the COM Express specification 2.0, the benefits are obvious. The Push-Pull output optimizes the power consumed by the fan_pwm signal without functional change.

7.1.3 Power Loss Control

The cBC has full control of the power-up of the module and can be used to specify the behavior of the system after an AC power loss condition. Supported modes are "Always On", "Remain Off" and "Last State".

7.1.4 Watchdog

The conga-TR3 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-TR3 does not support external hardware triggering. For more information about the Watchdog feature, see the BIOS setup description in section 10.4.2 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

Note

The conga-TR3 module does not support the watchdog NMI mode.

7.2 OEM BIOS Customization

The conga-TR3 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

7.2.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

7.2.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

7.2.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

7.2.4 OEM BIOS Code/Data

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table (OA2.0), Windows 8 OEM activation (OA3.0), verb tables for HDA codecs, PCI/PCIe opROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

7.2.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

7.3 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-TR3 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

7.4 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

7.5 Security Features

The conga-TR3 can be equipped optionally with a "Trusted Platform Module" (TPM 1.2/2.0). This TPM 1.2/2.0 includes coprocessors to calculate efficient hash and RSA algorithms with key lengths up to 2,048 bits as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity and confidence levels.

7.6 Suspend to Ram

The Suspend to RAM feature is available on the conga-TR3.

8 conga Tech Notes

The conga-TR3 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

8.1 AHCI

The Integrated controller hub provides hardware support for Advanced Host Controller Interface (AHCI), a new programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

8.2 AMD Processor Features

8.2.1 AMD64 Technology

- AMD64 technology instruction-set extensions
- 64-bit integer registers, 48-bit virtual addresses, and 40-bit physical addresses
- Sixteen 64-bit integer registers
- Sixteen 128-bit SSE/SSE2/SSE3/SSE4a registers

For more information about AMD64 Technology, visit http://www.amd.com.

8.2.2 Power Management

- Multiple low-power states
- AMD AllDay™ power technology
- System Management Mode (SMM)
- ACPI-compliant, including support for processor performance states (P-states)
- Supports processor power states C0, C1, C1E, C6, and CC6
- Supports sleep states including S0, S3, S4, and S5
- PCIe® core power gating
- PCIe speed power policy
- AMD Turbo CORE technology 3.0 with per core power gating

For more information about AMD64 Technology, visit http://www.amd.com.

8.2.3 AMD Virtualization™ Technology

- SVM pause count capability
- SVM disable and lock
- Rapid virtualization indexing (nested paging)
- Improved world-switch speed

For more information about AMD64 Technology, visit http://www.amd.com.

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

8.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-TR3 ACPI thermal solution offers three different cooling policies:

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points. If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

8.4 ACPI Suspend Modes and Resume Events

conga-TR3 supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 11.4.6 “ACPI Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Windows 7, Windows 8.1, Windows 10 and Linux

This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

Table 12 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S3-S5.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
WAKE#	Wakes uncondionally from S3.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check ‘Allow this device to bring the computer out of standby’.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

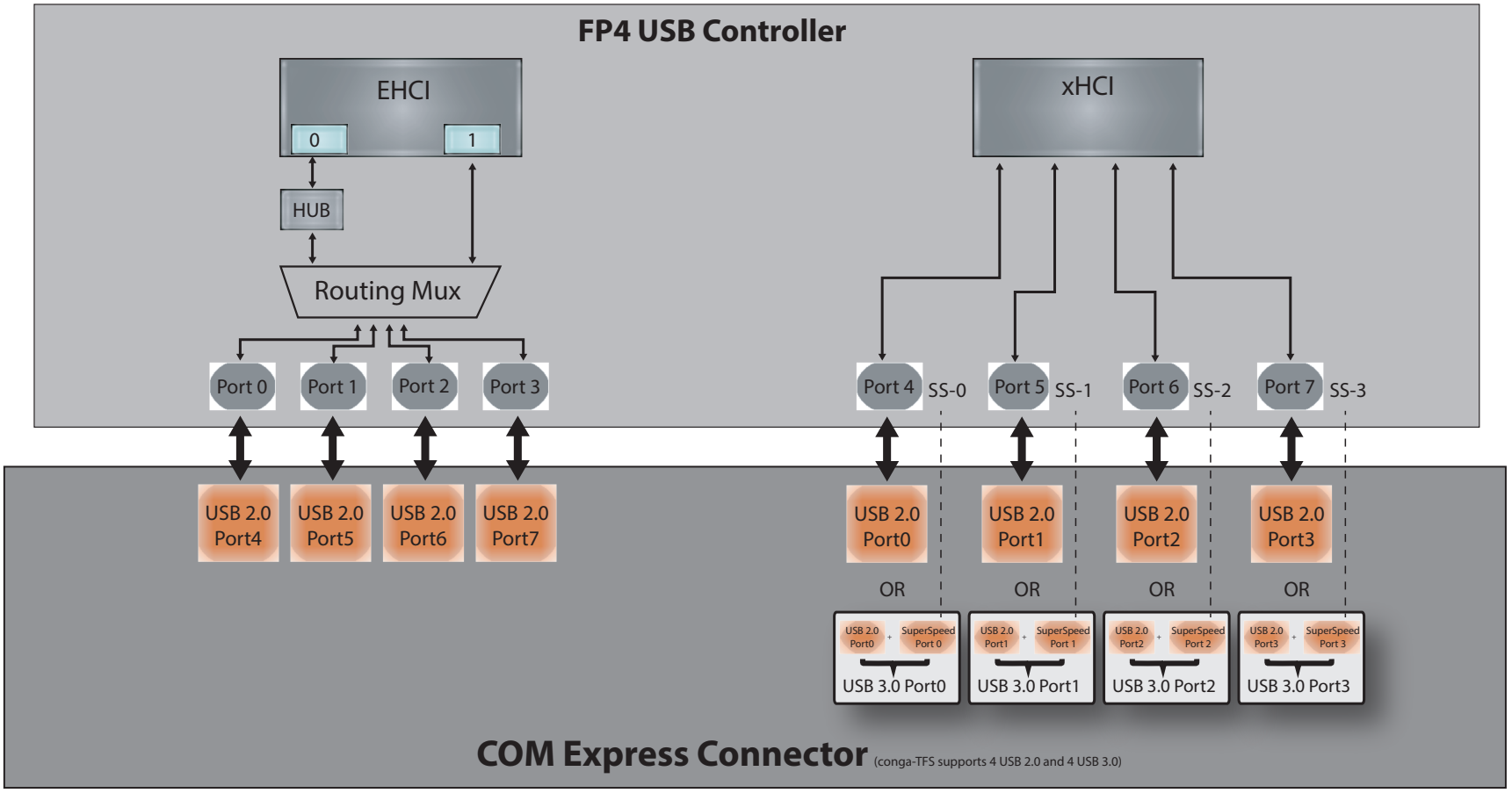
8.5 USB Host Controller

The conga-TR3 offers up to four USB 2.0 and four USB 3.0/2.0 ports. The integrated controller hub in the SoC supports these ports with one xHCI and one EHCI controller. The routing diagram of the controllers is shown below:

Note

USB Ports 0-3 do not support Wake on USB from S3. USB Ports 5-6 are not powered during S3. Only USB Port 4 and 7 work during installation.

Routing Diagram



9 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type 6 connectors used for congatec AG modules. The pinout of the modules complies with COM Express Type 6 Rev. 2.1.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Table 13 Signal Tables Terminology Descriptions

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PU	Implemented pull-up resistor
PD	Implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O 3.3VSB	Bi-directional signal 3.3V tolerant active in standby state
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
P	Power Input
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification
PEG	PCI Express Graphics
SATA	In compliance with Serial ATA specification, Revision 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

9.1 A-B Connector Signal Descriptions

Table 14 High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	High Definition Audio Reset: This signal is the master hardware reset to external codec(s).	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SYNC	A29	High Definition Audio Sync: This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_BITCLK	A32	High Definition Audio Bit Clock Output: This signal is a 24.000MHz serial data clock generated by the High Definition Audio controller.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SDOUT	A33	High Definition Audio Serial Data Out: This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for High Definition Audio.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SDIN[2:0]	B28-B30	High Definition Audio Serial Data In [0]: These signals are serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for High Definition Audio.	I 3.3VSB	PD 47K	AC'97 codecs are not supported.

Table 15 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.			Not connected

	1000	100	10
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
MDI[2]+/-	B1_DC+/-		
MDI[3]+/-	B1_DD+/-		

Note

The GBE0_LINK# output is only active during a 100Mbit or 1Gbit connection. It is not active during a 10Mbit connection. This is a limitation of Ethernet controller since it only has 3 LED outputs, ACT#, LINK100# and LINK1000#. The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TR3 module.

Table 16 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Not supported.
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Not supported.
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Not supported.
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Not supported.
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V		

Table 17 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Not connected by default.
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Not connected by default.
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Not connected
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Not connected
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Not connected
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Not connected
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 18 ExpressCard Support Pins Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request.	I 3.3VSB	PU 10k 3.3VSB	
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3V		

Table 19 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V	PU 50k 3.3V	LPC_DRQ1# is not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/OD 3.3V	PU 50k 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		

Table 20 USB 2.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

Table 21 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10K	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10K	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	OD 3.3V	PU 2.2K 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/OD 3.3V	PU 2.2K 3.3V	

Table 22 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10K 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB	PD 100K	
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or left as no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or left as no-connect

Table 23 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/OD 3.3V	PU 2.2K 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/OD 3.3V	PU 2.2K 3.3VSB	
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.	O OD 3.3V	PU 47K 3.3V	Signal is driven to logic 1 only. External PD is required.
FAN_TACHIN	B102	Fan tachometer input.	I OD	PU 47K 3.3V	Requires a fan with two-pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 10K	Trusted Platform Module chip is optional (assembly option).

Note

The congatec COM Express Type 6 and Type 10 modules use a Push-Pull output for the fan_pwm signal instead of the open drain output specified in the COM Express specification. Although this does not comply with the COM Express specification 2.0, the benefits are obvious. The Push-Pull output optimizes the power consumed by the fan_pwm signal without functional change.

Table 24 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3V		
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3V		
GPO2	B57	General purpose output pins. Shared with SD_WP. Input to COM Express, output from SD	O 3.3V		
GPO3	B63	General purpose output pins. Shared with SD_CD. Input to COM Express, output from SD	O 3.3V		
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3V	PU 10K 3.3V	

Table 25 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on rising edge.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V	PU 10K 3.3V	
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		Not supported
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10K 3.3VSB	

Signal	Pin #	Description	I/O	PU/PD	Comment
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10K 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 10k 3.3V	
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10k 3.3V	Not supported
SMB_CK	B13	System Management Bus bidirectional clock line.	I/O 3.3VSB	PU 2.2K 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line.	I/O OD 3.3VSB	PU 2.2K 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3VSB	PU 10K 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch.	I 3.3V	PU 47K 3.3VSB	
SLEEP	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I 3.3V	PU 47K 3.3VSB	

Table 26 Serial/UART Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O 3.3V		Signal is driven to logic 1 only. External PD is required.
SER1_TX	A101	General purpose serial port transmitter	O 3.3V		Signal is driven to logic 1 only. External PD is required.
SER0_RX	A99	General purpose serial port receiver	I 3.3V	PU 47K 3.3V	
SER1_RX	A102	General purpose serial port receiver	I 3.3V	PU 47K 3.3V	

Table 27 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

9.2 A-B Connector Pinout

Table 28 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4- (*)	B56	PCIE_RX4- (*)
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+ (*)	B58	PCIE_RX3+ (*)
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3- (*)	B59	PCIE_RX3- (*)
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# (*)	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	eDP_TX2+ / LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	eDP_TX2- / LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	eDP_TX1+ / LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	eDP_TX1- / LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	eDP_TX0+ / LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	eDP_TX0- / LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+ (*)	B22	SATA3_TX+(*)	A77	eDP / LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX-(*)	B23	SATA3_TX-(*)	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP / LVDS_BKLT_EN
A25	SATA2_RX+ (*)	B25	SATA3_RX+ (*)	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX- (*)	B26	SATA3_RX- (*)	A81	eDP_TX3+ / LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	eDP_TX3- / LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2	A83	eDP_ AUX+ / LVDS_I2C_CK	B83	eDP / LVDS_BKLT_CTRL
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	A84	eDP_AUX- / LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA_BITCLK	B32	SPKR	A87	eDP_HPD	B87	VCC_5V_SBY
A33	AC/HDA_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED (*)
A35	THRMTRIP# (*)	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN (*)

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU (*)
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC (*)
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC (*)
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK (*)
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT (*)
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+ (*)	B52	PCIE_RX5+ (*)	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5- (*)	B53	PCIE_RX5- (*)	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+ (*)	B55	PCIE_RX4+ (*)	A110	GND (FIXED)	B110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-TR3.

9.3 C-D Connector Signal Descriptions

Table 29 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		Not supported

Table 30 USB 3.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX0-	C3		I		
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX0-	D3		O		
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX1-	C6		I		
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX1-	D6		O		
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX2-	C9		I		
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX2-	D9		O		
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX3-	C12		I		
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX3-	D12		O		

Table 31 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs.	I PCIE		PEG_RX8± - PEG_RX15± lanes are not supported.
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+	D52	PCI Express Graphics Transmit Output differential pairs.	O PCIE		PEG_TX8± - PEG_TX15± lanes are not supported.
PEG_TX0-	D53				
PEG_TX1+	D55				
PEG_TX1-	D56				
PEG_TX2+	D58				
PEG_TX2-	D59				
PEG_TX3+	D61				
PEG_TX3-	D62				
PEG_TX4+	D65				
PEG_TX4-	D66				
PEG_TX5+	D68				
PEG_TX5-	D69				
PEG_TX6+	D71				
PEG_TX6-	D72				
PEG_TX7+	D74				
PEG_TX7-	D75				
PEG_TX8+	D78				
PEG_TX8-	D79				
PEG_TX9+	D81				
PEG_TX9-	D82				
PEG_TX10+	D85				
PEG_TX10-	D86				
PEG_TX11+	D88				
PEG_TX11-	D89				
PEG_TX12+	D91				
PEG_TX12-	D92				
PEG_TX13+	D94				
PEG_TX13-	D95				
PEG_TX14+	D98				
PEG_TX14-	D99				
PEG_TX15+	D101				
PEG_TX15-	D102				
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I		Not supported.

Note

conga-TR3 supports only up to x8 PCI Express Graphics (PEG).

Table 32 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with SDVO1_RED+, DP1_LANE0+ and TMDS1_DATA2+. Multiplexed with SDVO1_RED-, DP1_LANE0- and TMDS1_DATA2-.	O PCIE		
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with SDVO1_GRN+, DP1_LANE1+ and TMDS1_DATA1+. Multiplexed with SDVO1_GRN-, DP1_LANE1- and TMDS1_DATA1-.	O PCIE		
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with SDVO1_BLU+, DP1_LANE2+ and TMDS1_DATA0+. Multiplexed with SDVO1_BLU-, DP1_LANE2- and TMDS1_DATA0-.	O PCIE		
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with SDVO1_CK+, DP1_LANE3+ and TMDS1_CLK+. Multiplexed with SDVO1_CK-, DP1_LANE3- and TMDS1_CLK-.	O PCIE		
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	Multiplexed with SDVO1_INT+. Multiplexed with SDVO1_INT-.			Not supported
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	Multiplexed with SDVO1_TVCLKIN+. Multiplexed with SDVO1_TVCLKIN-.			Not supported
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	Multiplexed with SDVO1_FLDSTALL+. Multiplexed with SDVO1_FLDSTALL-.			Not supported
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD.	I 3.3V	PD 100K	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with SDVO1_CTRLCLK, DP1_AUX+ and HMDI1_CTRLCLK. DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE OD 3.3V	PD100K	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with SDVO1_CTRLDATA, DP1_AUX- and HDMI1_CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE I/OD 3.3V	PU 100K 3.3V	
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+ and TMDS2_DATA2+. Multiplexed with DP2_LANE0- and TMDS2_DATA2-.	O PCIE		
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+ and TMDS2_DATA1+. Multiplexed with DP2_LANE1- and TMDS2_DATA1-.	O PCIE		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+ and TMDS2_DATA0+. Multiplexed with DP2_LANE2- and TMDS2_DATA0-.	O PCIE		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+ and TMDS2_CLK+. Multiplexed with DP2_LANE3- and TMDS2_CLK-.	O PCIE		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD.	I 3.3V	PD 100K	
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+ and HDMI2_CTRLCLK. DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	I/O PCIE OD 3.3V	PD 100K	
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/OD 3.3V	PU 100K 3.3V	

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+. Multiplexed with DP3_LANE0- and TMDS3_DATA2-.	O PCIE		Not supported by default
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+. Multiplexed with DP3_LANE1- and TMDS3_DATA1-.	O PCIE		Not supported by default
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+. Multiplexed with DP3_LANE2- and TMDS3_DATA0-.	O PCIE		Not supported by default
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+. Multiplexed with DP3_LANE3- and TMDS3_CLK-.	O PCIE		Not supported by default
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD.	I 3.3V	PD 100K	Not supported by default
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK. DP AUX+ function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high	I/O PCIE OD 3.3V	PD 100k	Not supported by default
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA. DP AUX- function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.	I/O PCIE I/OD 3.3V	PU 100k	Not supported by default
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	Not supported by default

Note

The conga-TR3 supports two DDI interfaces by default. A third DDI interface (optional DDI) can be supported for Merlin Falcon variants via assembly option (customized variant). Customized variants with 3 DDI interfaces do not support LVDS/eDP port. Additionally, they can only support two independent HDMI/DVI displays.

The DDI interfaces support dual-mode DisplayPort. To support HDMI/DVI, an external level shifter (PTN3360D) should be implemented on the user's carrier board.

Table 33 HDMI/DVI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS1_CLK + TMDS1_CLK -	D36 D37	HDMI/DVI TMDS Clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
TMDS1_DATA0+ TMDS1_DATA0-	D32 D33	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
TMDS1_DATA1+ TMDS1_DATA1-	D29 D30	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-..	O PCIE		
TMDS1_DATA2+ TMDS1_DATA2-	D26 D27	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
HDMI1_HPD	C24	HDMI/DVI Hot-plug detect. Multiplexed with DDI1_HPD.	I PCIE	PD 100K	
HDMI1_CTRLCLK	D15	HDMI/DVI I²C Control Clock Multiplexed with DDI1_CTRLCLK_AUX+	OD 3.3V	PD 100K	2.2k to 3.3V Pull-up must be implemented on the carrier board.
HDMI1_CTRLDATA	D16	HDMI/DVI I²C Control Data Multiplexed with DDI1_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	2.2k to 3.3V Pull-up must be implemented on the carrier board.
TMDS2_CLK + TMDS2_CLK -	D49 D50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-.	O PCIE		
TMDS2_DATA0+ TMDS2_DATA0-	D46 D47	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-.	O PCIE		
TMDS2_DATA1+ TMDS2_DATA1-	D42 D43	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-.	O PCIE		
TMDS2_DATA2+ TMDS2_DATA2-	D39 D40	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-..	O PCIE		
HDMI2_HPD	D44	HDMI/DVI Hot-plug detect. Multiplexed with DDI2_HPD	I PCIE	PD 100K	
HDMI2_CTRLCLK	C32	HDMI/DVI I²C Control Clock Multiplexed with DDI2_CTRLCLK_AUX+	OD 3.3V	PD 100K	2.2k to 3.3V Pull-up must be implemented on the carrier board.
HDM12_CTRLDATA	C33	HDMI/DVI I²C Control Data Multiplexed with DDI2_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	2.2k to 3.3V Pull-up must be implemented on the carrier board.
TMDS3_CLK + TMDS3_CLK -	C49 C50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		Not supported by default.
TMDS3_DATA0+ TMDS3_DATA0-	C46 C47	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		Not supported by default.
TMDS3_DATA1+ TMDS3_DATA1-	C42 C43	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-..	O PCIE		Not supported by default.
TMDS3_DATA2+ TMDS3_DATA2-	C39 C40	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		Not supported by default.
HDMI3_HPD	C44	HDMI/DVI Hot-plug detect. Multiplexed with DDI3_HPD.	I PCIE	PD 100K	Not supported by default.
HDMI3_CTRLCLK	C36	HDMI/DVI I²C Control Clock Multiplexed with DDI3_CTRLCLK_AUX+	OD 3.3V	PD 100K	2.2k to 3.3V Pull-up should be implemented on the carrier board.

Signal	Pin #	Description	I/O	PU/PD	Comment
HDMI3_CTRLDATA	C37	HDMI/DVI I²C Control Data Multiplexed with DDI3_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	2.2k to 3.3V Pull-up should be implemented on the carrier board.

Note

Customized conga-TR3 variants equipped with the optional DDI interface support only two independent HDMI/DVI displays.

To support the HDMI interface, an external level translator/shifter (e.g. PTN3360D) should be implemented on the user's baseboard.

Table 34 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE3+ DP1_LANE3-	D36 D37	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
DP1_LANE2+ DP1_LANE2-	D32 D33	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
DP1_LANE1+ DP1_LANE1-	D29 D30	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		
DP1_LANE0+ DP1_LANE0-	D26 D27	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
DP1_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI1_HPD.	I 3.3V	PD 100K	
DP1_AUX+	D15	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100K	
DP1_AUX-	D16	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100K 3.3V	
DP2_LANE3+ DP2_LANE3-	D49 D50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		
DP2_LANE2+ DP2_LANE2-	D46 D47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		
DP2_LANE1+ DP2_LANE1-	D42 D43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		
DP2_LANE0+ DP2_LANE0-	D39 D40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR0+ and DDI1_PAIR0-	O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
DP2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI2_HPD.	I 3.3V	PD 100K	
DP2_AUX+	C32	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100K	
DP2_AUX-	C33	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100K 3.3V	
DP3_LANE3+ DP3_LANE3-	C49 C50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		Not supported by default.
DP3_LANE2+ DP3_LANE2-	C46 C47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		Not supported by default.
DP3_LANE1+ DP3_LANE1-	C42 C43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-.	O PCIE		Not supported by default.
DP3_LANE0+ DP3_LANE0-	C39 C40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		Not supported by default.
DP3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI3_HPD.	I 3.3V	PD 100K	Not supported by default.
DP3_AUX+	C36	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP3_AUX-	C37	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	

Table 35 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# / TYPE1# / TYPE0# / X / X / X / Pinout Type 1 NC / NC / NC / Pinout Type 2 NC / NC / GND / Pinout Type 3 (no IDE) NC / GND / NC / Pinout Type 4 (no PCI) NC / GND / GND / Pinout Type 5 (no IDE, no PCI) GND / NC / NC / Pinout Type 6 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.	PDS	TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard. The conga-TR3 is based on the COM Express Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.
TYPE10#	A97	Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed. TYPE10# / NC / Pinout R2.0 PD / Pinout Type 10 pull down to ground with 4.7k resistor 12V / Pinout R1.0 This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7k resistor.	PDS	Not connected to indicate "Pinout R2.0".

Table 36 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

9.4 C-D Connector Pinout

Table 37 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1-	D56	PEG_TX1-
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+	D58	PEG_TX2+
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2-	D59	PEG_TX2-
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PEG_RX3+	D61	PEG_TX3+
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PEG_RX3-	D62	PEG_TX3-
C8	GND	D8	GND	C63	RSVD	D63	DDPC_CTRLCLK (*)
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	RSVD	D64	DDPC_CTRLDATA (*)
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	PEG_RX4+	D65	PEG_TX4+
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4-	D66	PEG_TX4-
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RSVD	D67	GND
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	PEG_RX5+	D68	PEG_TX5+
C14	GND	D14	GND	C69	PEG_RX5-	D69	PEG_TX5-
C15	DDI1_PAIR6+ (*)	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	DDI1_PAIR6- (*)	D16	DDI1_CTRLDATA_AUX-	C71	PEG_RX6+	D71	PEG_TX6+
C17	RSVD	D17	RSVD	C72	PEG_RX6-	D72	PEG_TX6-
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	PEG_RX7+	D74	PEG_TX7+
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	PEG_RX7-	D75	PEG_TX7-
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+ (*)	D22	PCIE_TX7+ (*)	C77	RSVD	D77	RSVD
C23	PCIE_RX7- (*)	D23	PCIE_TX7- (*)	C78	PEG_RX8+ (*)	D78	PEG_TX8+ (*)
C24	DDI1_HPD	D24	RSVD	C79	PEG_RX8- (*)	D79	PEG_TX8- (*)
C25	DDI1_PAIR4+ (*)	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	DDI1_PAIR4- (*)	D26	DDI1_PAIR0+	C81	PEG_RX9+ (*)	D81	PEG_TX9+ (*)
C27	RSVD	D27	DDI1_PAIR0-	C82	PEG_RX9- (*)	D82	PEG_TX9- (*)
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD
C29	DDI1_PAIR5+ (*)	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	DDI1_PAIR5- (*)	D30	DDI1_PAIR1-	C85	PEG_RX10+ (*)	D85	PEG_TX10+ (*)
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- (*)	D86	PEG_TX10- (*)
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-	C88	PEG_RX11+ (*)	D88	PEG_TX11+ (*)
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11- (*)	D89	PEG_TX11- (*)
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+ (*)	D36	DDI1_PAIR3+	C91	PEG_RX12+ (*)	D91	PEG_TX12+ (*)

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C37	DDI3_CTRLDATA_AUX- (*)	D37	DDI1_PAIR3-	C92	PEG_RX12- (*)	D92	PEG_TX12- (*)
C38	DDI3_DDC_AUX_SEL (*)	D38	RSVD	C93	GND	D93	GND
C39	DDI3_PAIR0+ (*)	D39	DDI2_PAIR0+	C94	PEG_RX13+ (*)	D94	PEG_TX13+ (*)
C40	DDI3_PAIR0- (*)	D40	DDI2_PAIR0-	C95	PEG_RX13- (*)	D95	PEG_TX13- (*)
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+ (*)	D42	DDI2_PAIR1+	C97	RVSD	D97	RSVD
C43	DDI3_PAIR1- (*)	D43	DDI2_PAIR1-	C98	PEG_RX14+ (*)	D98	PEG_TX14+ (*)
C44	DDI3_HPD (*)	D44	DDI2_HPD	C99	PEG_RX14- (*)	D99	PEG_TX14- (*)
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+	C101	PEG_RX15+ (*)	D101	PEG_TX15+ (*)
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-	C102	PEG_RX15- (*)	D102	PEG_TX15- (*)
C48	RSVD	D48	RSVD	C103	GND	D103	GND
C49	DDI3_PAIR3+ (*)	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3- (*)	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+	D52	PEG_TX0+	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0-	D53	PEG_TX0-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV# (*)	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+	D55	PEG_TX1+	C110	GND (FIXED)	D110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-TR3.

10 System Resources

10.1 I/O Address Assignment

The I/O address assignment of the conga-TR3 module is functionally identical with a standard PC/AT.

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

10.1.1 LPC Bus

On the conga-TR3, the PCIExpress Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCIExpress Bus not the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus. On the conga-TR3 the following I/O address ranges are sent to the LPC Bus:

Table 38 I/O address ranges to LPC Bus

ParallelPort0	378h-37Fh
ParallelPort1	778h-77Fh
ParallelPort2	278h-27Fh
ParallelPort3	678h-67Fh
ParallelPort4	3BCh-3BFh
ParallelPort5	7BCh-7BFh
SerialPort0	3F8h-3FFh
SerialPort1	2F8h-2FFh
SerialPort2	220h-227h
SerialPort3	228h-22Fh
SerialPort4	238h-23Fh
SerialPort5	2E8h-2EFh
SerialPort6	338h-33Fh
SerialPort7	3E8h-3EFh

AudioPort0	230h-233h
AudioPort1	240h-253h
AudioPort2	260h-273h
AudioPort3	280h-293h
KbcPort	60h, 64h
BoardController	E00h-FFFh

Some of these ranges are not available if a Super I/O is used on the carrier board or are occupied by the COMExpress on module UARTs if these are enabled in setup. The I/O range E38h to EBFh is always used by on module LPC devices.

Otherwise the above listed ranges are available for customer use.

If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

10.2 PCI Configuration Space Map

Table 39 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Root Complex
00h	00h	02h	N.A.	IOMMU
00h	01h	00h	Internal	Integrated Graphics Controller (IGD)
00h	01h	01h	Internal	HDMI / DisplayPort HDA Controller
00h	02h	00h	N.A.	PCIe Host Bridge
00h (see Note 1)	02h	01h	Internal	PCIe Bridge 0
00h (see Note 1)	02h	02h	Internal	PCIe Bridge 1
00h (see Note 1)	02h	03h	Internal	PCIe Bridge 2
00h (see Note 1)	02h	04h	Internal	PCIe Bridge 3
00h (see Note 1)	02h	05h	Internal	PCIe Bridge 4
00h	03h	00h	Internal	PEG Host Bridge
00h (see Note 2)	03h	01h	Internal	PEG Bridge 0
00h (see Note 2)	03h	02h	Internal	PEG Bridge 1

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	08h	00h	Internal	AMD PSP Controller
00h	09h	00h	N.A	AMD Audio Controller Host Bridge
00h	09h	02h	Internal	AMD Audio Controller
00h	10h	00h	Internal	XHCI Host Controller
00h	11h	00h	Internal	Serial ATA Controller
00h	12h	00h	Internal	EHCI Host Controller
00h	14h	00h	N.A.	SMBus Host Controller
00h	14h	03h	N.A.	PCI to LPC Bridge
00h	14h	07h	Internal	SD Controller
00h	18h	00h	N.A.	Chipset Configuration Registers
00h	18h	01h	N.A.	Chipset Configuration Registers
00h	18h	02h	N.A.	Chipset Configuration Registers
00h	18h	03h	N.A.	Chipset Configuration Registers
00h	18h	04h	N.A.	Chipset Configuration Registers
00h	18h	05h	N.A.	Chipset Configuration Registers
01h (see Note 3)	00h	00h	Internal	Onboard Gigabit LAN Controller
02h (see Note 3)	00h	00h	Internal	PCI Express Port 0
03h (see Note 3)	00h	00h	Internal	PCI Express Port 1
04h (see Note 3)	00h	00h	Internal	PCI Express Port 2
05h (see Note 3)	00h	00h	Internal	PCI Express Port 3
06h (see Note 3)	00h	00h	Internal	PCI Express Graphics Port 0
07h (see Note 3)	00h	00h	Internal	PCI Express Graphics Port 1

Note

1. *The PCI Express Ports may only be visible if the PCI Express Port is set to "Enabled" in the BIOS setup program and a device is attached to the corresponding PCI Express port on the carrier board.*

2. *The PCI Express Graphics Ports may only be visible if the PCI Express Graphics Port is set to "Enabled" in the BIOS setup program and a device is attached to the corresponding PCI Express port on the carrier board.*

3. *The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

10.3 PCI Interrupt Routing Map

Table 40 PCI Interrupt Routing Map #1

PIRQ	VGA	HDA (HDMI/DP)	XHCI	EHCI	AMD PSP	SDIO	SATA	LAN	HDA (Main)	PEG Port 0	PEG Port 1
A		40				16		40			48
B											49
C			18	18							50
D	43				11		19		43		51
E										44	
F										45	
G										46	
H										47	

Table 41 PCI Interrupt Routing Map #2

PIRQ	PCI-EX Root Bridge 0	PCI-EX Root Bridge 1	PCI-EX Root Bridge 2	PCI-EX Root Bridge 3	PCI-EX Root Bridge 4	PEG Root Bridge 0	PEG Root Bridge 1	PCI-EX Port 0	PCI-EX Port 1	PCI-EX Port 2	PCI-EX Port 3
A									32		40
B						49			33		41
C							50		34		42
D									35		45
E								28		36	
F	45	45	45	45	45			29		37	
G								30		38	
H								31		39	

Note

Given numbers specify the APIC interrupt numbers assigned to the respective devices.

10.4 I²C

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

10.5 SM Bus

System Management (SM) bus signals are connected to the AMD Chipset and the SM bus is not intended to be used by off-board non-system management devices.. For more information about this subject contact congatec technical support.

11 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

11.1 Entering the BIOS Setup Program

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

11.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used, a selection will be displayed immediately after POST allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

11.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

Main	Advanced	Chipset	Security	Boot	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

11.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main screen reports BIOS, processor, memory and board information and is used to configure the system date and time.

Feature	Options	Description
Main BIOS Version	No option	Displays the main BIOS version.
OEM BIOS Version	No option	Displays the additional OEM BIOS version.
Build Date	No option	Displays the date the BIOS was built
Product Revision	No option	Displays the hardware revision of the board.
Serial Number	No option	Displays the serial number of the board.
BC Firmware Rev.	No option	Displays the revision of the congatec board controller.
MAC Address	No option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	No option	Displays the number of boot-ups. (max. 16777215).
Running Time	No option	Displays the time the board is running [in hours max. 65535].
Memory Information	No option	
Total Memory	No option	Displays the total amount of installed memory.
System Date	Day of week, month/day/year	Specifies the current system date. **Note:** The date is in month-day-year format.
System Time	Hour:Minute:Second	Specifies the current system time. **Note:** The time is in 24-hour format.

11.3.1 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Save & Exit	Save & Exit
	Graphics				
	Hardware Monitoring				
	Watchdog				
	Module Serial Ports				
	Trusted Platform Module				
	RTC Wake Settings				
	Memory				
	Chipset				
	SATA				
	ACPI				
	Super IO				
	Serial Port Console Redirection				
	CPU				
	PCI Express				
	CSM and Option ROMs				
	Info Report				
	NVMe				
	SDIO				
	USB				
	Diagnostic Settings				
	PC Speaker				
	Intel(R) I211 Gigabit Network Connection				

11.3.2 Graphics Submenu

Feature	Options	Description
Primary Graphics Device	IGD **PEG/PCIe**	Select primary graphics adapter to be used during boot up. IGD: Internal Graphics Device. PEG/PCIe: Try to use external PEG or PCI Express Graphics Device. If not present, IGD is used.
Integrated Graphics Device	**Auto** Disabled Force	Deactivate IGD or select framebuffer configuration mode. In auto mode, the framebuffer size will be defined based on the amount of physical memory present. Force mode will enable IGD regardless of external GPU present or not.
IGD Framebuffer Size	32M 64M 128M **256M** 512M 1G	Only visible if IGD is set to forced configuration. Set fixed graphics framebuffer size for IGD. The graphics driver might allocate additional memory.
LFP/DDI0 Interface	Disabled **LFP** DDI0 Auto Selection DDI0 Force HDMI/DVI	Enable or disable the local flat panel (LFP) or Digital Display Interface 0 (DDI0). Availability of LFP or DDI0 depends on board part number. See DDI1 Interface description below to understand DDI0 settings.
Always Try Auto Panel Detect	No **Yes**	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel . Only if no external EDID data set can be found, the data set selected under 'Local Flat Panel Type' will be used as fallback data set.

Feature	Options	Description
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x800 1x18 (01Eh) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. **Note:** Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.
Backlight Inverter Type	**None** PWM I2C	Select the type of backlight inverter. PWM = Use module PWM output signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.
PWM Inverter Frequency (Hz)	**200** – 40000	Only visible if Backlight Inverter Type is set to PWM. Set the PWM inverter frequency in Hertz.
Backlight Setting	0% 10% 25% 40% 50% 60% 75% 90% **100%**	Actual backlight value in percentage of the maximum setting.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Setting	**No** Yes	Allow to invert backlight control values if required for the actual I2C type backlight hardware controller.

Feature	Options	Description
LVDS SSC	**Disabled** 0.5% 1.0% 1.5% 2.0% 2.5%	Configure LVDS spread spectrum clock modulation depth using center spreading and a fixed modulation frequency of 32.9kHz
Remove EDID Established Timings	**Yes** No	Modify EDID data to remove established timings (bytes 0x23 – 0x25), which aren't required for LVDS panels. This modification will only be applied for EDID data stored on flash.
Remove EDID Standard Timings	**Yes** No	Modify EDID data to remove standard timings (bytes 0x26 – 0x35), which aren't required for LVDS panels. This modification will only be applied for EDID data stored on flash.
Ensure EDID Vsync Pulse Width >=3	**Yes** No	Modify EDID data to ensure Vsynce Pulse Width (byte 0x40) is at least 3, which is required for LVDS panels. This modification will only be applied for EDID data stored on flash.
DDI1 Interface	Disabled **Auto Selection** Force HDMI/DVI	Configure the digital display interface 1. Display Port or HDMI/DVI supported and automatically detected and configured, or HDMI/DVI mode can be forced.
DDI2 Interface	Disabled **Auto Selection** Force HDMI/DVI	Configure the digital display interface 2. Display Port or HDMI/DVI supported and automatically detected and configured, or HDMI/DVI mode can be forced.

11.3.3 Hardware Monitoring Submenu

Feature	Options	Description
CPU Temperature	No option	Displays the actual module CPU temperature in °C.
Board Temperature	No option	Displays the actual module board temperature in °C.
DC Input Voltage Standard	No option	Displays the actual voltage of DC power supply.
5V Standby	No option	Displays the actual voltage of the 5V standby power supply.
DC Input Current	No option	Displays the module input current from DC power suply.
CPU Fan Speed	No option	Displays the actual CPU Fan Speed in RPM.
Fan PWM Frequency Mode	Low Frequency **High Frequency**	Select fan PWM base frequency mode. Low frequency: 11.0Hz-88.2Hz High frequency: 1kHz-63kHz
Fan PWM Frequency	**31 Khz**	Select fan PWM base frequency.
Default Fan Speed	Default: **60%** 10 – 100%	Default fan speed to be set after the OS takes fan control.

Feature	Options	Description
Automatic Fan Speed Control	**Enabled** Disabled	Enable or disable automatic fan speed control performed by board controller.
Fan Control Temperature	**CPU Temperature** Board Temperature	Select the temperature sensor used for fan speed control.
Lower Temperature Limit	Default: **50 C** 10 – 90 C	Lower limit of temperature-based fan control range.
Upper Temperature Limit	Default: **80 C** 10 – 90 C	Upper limit of temperature-based fan control range.
Minimum fan speed	Default: **40 %** 0 – 100%	Fan speed to be set if the temperature is below the lower limit
Mid Range Bottom Fan Speed	Default: **60 %** 0 – 100%	Fan speed to be set if the temperature is within the lower area of control range
Mid Range Top Fan Speed	Default: **80 %** 0 – 100%	Fan speed to be set if the temperature is within the upper area of control range
Maximum fan speed	Default: **100 %** 0 – 100%	Fan speed to be set if the temperature is above the upper limit

11.3.4 Watchdog Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog For User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One-time Trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to 'One-time Trigger' the watchdog will be disabled after the first trigger. If set to 'Single Event', every stage will be executed only once, then the watchdog will be disabled. If set to 'Repeated Event' the last stage will be executed repeatedly until a reset occurs.

Feature	Options	Description
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event see note below.
Event 2	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion. For Restart: An ACPI fatal error is reported to the OS.

11.3.5 Module Serial Ports

Feature	Options	Description
Serial Port 0	**Disabled** Enabled	Enable or disable module serial port 0.
I/O Base Address	3F8h 2F8h 220h 228h 238h 2E8h 338h **3E8h**	Set serial port base address.
Interrupt	None IRQ3 IRQ4 IRQ5 IRQ6 **IRQ10** IRQ11 IRQ14 IRQ15	Set serial port interrupt.
PNP ID	None PNP0501 **CGT0501**	Set serial port ACPI ID.
Baudrate	**2400** 4800 9600 19200 38400 57600 115200	Set serial port initial baudrate.
Serial Port 1	**Disabled** Enabled	Enable or disable module serial port 1.
I/O Base Address	3F8h 2F8h 220h 228h 238h **2E8h** 338h 3E8h	Set serial port base address.

Feature	Options	Description
Interrupt	None IRQ3 IRQ4 IRQ5 IRQ6 IRQ10 **IRQ11** IRQ14 IRQ15	Set serial port interrupt.
PNP ID	None PNP0501 CGT0501 **CGT0502**	Set serial port ACPI ID.
Baudrate	**2400** 4800 9600 19200 38400 57600 115200	Set serial port initial baudrate.

11.3.6 Trusted Platform Module 1.2 Submenu

Feature	Options	Description
Security Device Support	**Disable** Enable	Enable or disable BIOS support for security device.
TPM State	**Disabled** Enabled	Enable or disable TPM 1.2 chip. **Note:** System might restart several times during POST to acquire target state.
Pending operation	**None** TPM Clear	Perform selected TPM 1.2 chip operation. **Note:** System might restart several times during POST to perform selected operation.
TPM Enabled Status	No option	Enabled or Disabled.
TPM Active Status:	No option	Activated or Deactivated.
TPM Owner Status:	No option	Owned or Unowned.

11.3.7 Trusted Platform Module 2.0 Submenu

Feature	Options	Description
Security Device Support	**Disable** Enable	Enable or disable BIOS support for security device.
Active PCR banks	No option	List of active PCR banks
Available PCR banks	No option	List of available PCR banks
SHA-1 PCR Bank	**Enabled** Disabled	Enable or disable SHA-1 PCR bank. This is a default PCRs compatible with TPM 1.2 and supported by Windows 8.1 and newer OSes.
SHA-256 PCR Bank	Enabled **Disabled**	Enable or disable SHA-256 PCR bank. This is new PCRs specific to released TPM 2.0 standard. Supported only by Windows 10 and newer OSes.
Pending operation	**None** TPM Clear	Perform selected TPM 2.0 chip operation. **Note:** System might restart several times during POST to perform selected operation.
Platform Hierarchy	**Enabled** Disabled	Enable or disable TPM 2.0 platform hierarchy.
Storage Hierarchy	**Enabled** Disabled	Enable or disable TPM 2.0 storage hierarchy.
Endorsement Hierarchy	**Enabled** Disabled	Enable or disable TPM 2.0 endorsement hierarchy.
TPM2.0 UEFI Spec Version	**TCG_2** TCG_1_2	Compatible UEFI specification version, SHA256 PCRs will not be exposed if TCG_1_2 is selected.

Note

There are 2 different TPM menus, one for TPM 1.2 and another one is for TPM 2.0. Correct menu will be shown once TPM 1.2 or TPM 2.0 device is detected. UEFI OS must be used if TPM 2.0 support is required.

11.3.8 RTC Wake Submenu

Feature	Options	Description
RTC Wake Mode	**Disabled** Wake from S5 only Wake from S4 and S5 Wake from S3, S4 and S5	Enable system to wake from specified Sx states using RTC alarm.
Wake up hour		Specify wake up hour.
Wake up minute		Specify wake up minute.
Wake up second		Specify wake up second.

11.3.9 Memory Submenu

Feature	Options	Description
Memory Clock	**Auto** 1333 Mhz 1600 Mhz 1866 Mhz 2133 Mhz	Set upper memory frequency limit. Auto is a maximum values supported by SoC and SPD data of inserted memory modules.
Bank Interleaving	**Enabled** Disabled	Enable or disable DRAM bank interleaving.
Channel Interleaving	**Enabled** Disabled	Enable or disable DRAM channel interleaving.
Memory Clear	**Enabled** Disabled	Enable or disable memory clear on reset.
ECC Support	**Enabled** Disabled	Enable or disable ECC support. ECC can be enabled only if all inserted memory modules are supporting it.
Dimm0	No option	Size, current speed and SPD max speed of DIMM 0 module
Dimm1	No option	Size, current speed and SPD max speed of DIMM 1 module

11.3.10 Chipset Submenu

Feature	Options	Description
Chipset Power Saving Features	**Enabled** Disabled	Enable or disable chipset power saving.
Spread Spectrum Clocking	**Enabled** Disabled	Enable or disable spread spectrum of chipset's PLL. Required to be enabled for full USB 3.0 compliance. System generates additional soft reset after each hard reset or power-on to enable SSC.
Spread Spectrum Level	-0.362% **-0.375%** -0.400% -0.425% -0.450% -0.475%	Select spread spectrum level, if previous option is enabled.
HPET	**Enabled** Disabled	Enabled or disable High Performance Event Timer.
IOMMU	**Enabled** Disabled	Enable or disable IO Memory-Mapping Unit.

Feature	Options	Description
Isolate SMBus Segments	Never During POST **Always**	Allows isolation of off-module SMBus from internal SMBus.

11.3.11 SATA Submenu

Feature	Options	Description
SATA Controller	Disabled **Enabled**	Enable or disable the onboard SATA controller.
SATA Mode Selection	Legacy IDE Native IDE **AHCI**	Select onboard SATA controller mode. Select legacy IDE mode if your OS doesn't allow interrupt sharing.
SATA Hot-Removal Support	**Disabled** Enabled	Enable or disable hot removal of SATA devices (AHCI mode only)
SATA Port 0 State	**Enabled** Disabled	Enable or disable SATA port 0.
Speed Limit	**Auto** Gen1 Gen2	Select max. SATA speed generation for the selected port. Auto = up to Gen3
ESATA Support	**Disabled** Enabled	Enabled or disable ESATA and hotplug (AHCI mode only) support.
SATA Port 1 State	**Enabled** Disabled	Enable or disable SATA port 1.
Speed Limit	**Auto** Gen1 Gen2	Select max. SATA speed generation for the selected port. Auto = up to Gen3
ESATA Support	**Disabled** Enabled	Enabled or disable ESATA and hotplug (AHCI mode only) support.
SATA Port 0	No option	SATA drive 0 information.
SATA Port 1	No option	SATA drive 1 information.

11.3.12 ACPI Submenu

Feature	Options	Description
Hibernation Support	Disabled **Enabled**	Enable or disable system ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.

Feature	Options	Description
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend.
Critical Trip Point	**Disabled** 70C 80C 90C 95C 100C 105C 110C 115C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Active Trip Point	**Disabled** 20C 30C 40C 50C 60C 70C 80C 90C 95C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Trip Point	**Disabled** 60C 70C 80C 90C 95C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.
Lid Support	**Disabled** Enabled	Configure COM Express LID# signal to act as ACPI lid.
Sleep Button Support	**Disabled** Enabled	Configure COM Express SLEEP# signal to act as ACPI sleep button.

11.3.13 Super I/O Submenu

Feature	Options	Description
SIO Clock	**24MHz** 48MHz	Select Super I/O base clock.
PS/2 Keyboard/Mouse Support	**Disabled** Enabled	Enable or disable PS/2 Keyboard/Mouse controller support.

Feature	Options	Description
Serial Port 0	Disabled **Enabled**	Enable or disable serial port 0.
Device Settings	IO=3F8h; IRQ=4;	Fixed configuration of serial port 0 if enabled.
Serial Port 1	Disabled **Enabled**	Enable or disable serial port 1.
Device Settings	IO=2F8h; IRQ=3;	Fixed configuration of serial port 1 if enabled.
Parallel Port	Disabled Enabled	Enable or disable parallel port.
Device Settings	IO=378h; IRQ=7;	Fixed configuration of the parallel port if enabled.
Device Mode	**Standard Parallel** Mode EPP Mode ECP Mode EPP Mode & ECP Mode	Set the parallel port mode.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

11.3.14 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
▶Console Redirection Settings	Submenu	Opens console redirection configuration sub menu.
COM1 Console Redirection	**Disabled** Enabled	Enable or disable serial port 1 console redirection.
▶Console Redirection Settings	Submenu	Opens console redirection configuration sub menu.

11.3.14.1 Console Redirection Settings Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.

Feature	Options	Description
Baudrate	9600 19200 38400 57600 **115200**	Select baud rate.
Data Bits	7 **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Enabled** Disabled	Select whether serial redirection should be continued after POST.

11.3.15 CPU Submenu

Feature	Options	Description
▶CPU Information	No option	Submenu with various information about CPU and caches
AMD PowerNow! Support	Disabled **Enabled**	Enable or disable support for AMD PowerNow! technology. Allows operating systems to control CPU performance states.
Startup P-State Adjustment	**P-State 0** P-State 1 P-State 2	Select the maximum CPU performance state to be set at power up. Higher numbers mean lower performance. P-state 0 is the highest performance state.
ACPI P-State Adjustment	**P-State 0** P-State 1 P-State 2	Select the maximum CPU performance state the operating system should support. Higher numbers mean lower performance. P-state 0 is the highest performance state.
NX Support	Disabled **Enabled**	Enable or disable the 'no-execute' page protection function.
CPU Virtualization	Disabled **Enabled**	When enabled, a Virtual Machine Manager (VMM) can utilize the integrated hardware virtualization support.
C6 Support	**Disabled** Enabled	Enable or disable CPU C6 low power state support.
Core Performance Boost	Auto **Disabled**	Control usage of boosted P-States, i.e. P-States above the standard CPU P-State limit. Availability depends on CPU revision and type, actual usage on total CPU/GPU chip power consumption.
SMU TDP Configuration	**Auto** 12 W 15 W 25 W 35 W	Configure System Management Unit to keep CPU below selected TDP level. Auto means maximum TDP settings should be obtained from CPU.

11.3.16 PCI Express Submenu

Feature	Options	Description
PCI Settings		
PCI Latency Timer	**32** 64 96 128 160 192 224 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.

Feature	Options	Description
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate SERR#.
Generate EXCD0/1_PERST#	Disabled 1ms 5ms **10ms** 50ms 100ms 150ms 200ms 250ms	Select whether and how long the COM Express EXCD0_PERST# and EXCD1_PERST# pins should be driven low during POST.
▶PCI Express Settings	Submenu	PCI Express device and link settings.
▶PCI Express Port Control	Submenu	Configure PCI Express and PEG ports.
▶PIRQ Routing & IRQ Reservation	Submenu	Manual PIRQ routing and interrupt reservation for legacy devices.

11.3.16.1 PCI Express Settings Submenu

Feature	Options	Description
Relaxed Ordering	**Disabled** Enabled	Enable or disable PCI Express device relaxed ordering.
Extended Tag	**Disabled** Enabled	If enabled a device may use an 8-bit tag filed as a requester.
No Snoop	Disabled **Enabled**	Enable or disable PCI Express device 'No Snoop' option.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum payload of PCI Express devices or allow system BIOS to select the value.

Feature	Options	Description
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum read request size of PCI Express devices or allow system BIOS to select the value.
ASPM	**Disabled** Enabled	Enabled or disable PCI Express Active State Power Management.
Extended Synch	**Disabled** Enabled	If enabled, the generation of extended PCI Express synchronization patterns is allowed.
Link Training Retry	Disabled 2 3 **5**	Defines numer of retry attempts software will take to retrain the link if the previous training attempt was unsuccessful.
Link Training Timeout (us)	Default: **100** 10 – 10000	Defines number of microseconds software will wait before polling the link training bit in the link status register. Value ranges from 10us to 10000us.
Unpopulated Links	**Keep link on** Disabled	Disable unpopulated links to conserve power or keep them on.
Restore PCIE Registers	Enabled **Disabled**	On non-PCI Express aware operating systems some devices may not be re-initialized correctly after S3. Setting this node to Enabled restores PCI Express configuration on S3 resume. Warning: Enabling this may cause issues with other hardware after S3 resume.

11.3.16.2 PCI Express Port Control Submenu

Feature	Options	Description
PCI Express Port Organization	**4 x1 Ports** 1 x2 + 2 x1 Porst 1 x4 Port	Select PCI Express port layout
PCIe Port 1	Disabled **Enabled**	Enable or disable PCIe port 1.
Link Speed	**Max supported** Gen3 Gen2 Gen1	Select PCIe port 1 link speed. Max supported = link speed determined by PCIe device. GenX = force GenX speed
ASPM Mode Control	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Select ASPM mode for current PCIe port

Feature	Options	Description
Hotplug Mode Control	**Disabled** Enabled	Enable or disable hotplug on current PCIe port.
PCIe Port 2	Disabled **Enabled**	Enable or disable PCIe port 2.
Link Speed	**Max supported** Gen3 Gen2 Gen1	Select PCIe port 2 link speed. Max supported = link speed determined by PCIe device. GenX = force GenX speed
ASPM Mode Control	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Select ASPM mode for current PCIe port
Hotplug Mode Control	**Disabled** Enabled	Enable or disable hotplug on current PCIe port.
PCIe Port 3	Disabled **Enabled**	Enable or disable PCIe port 3.
Link Speed	**Max supported** Gen3 Gen2 Gen1	Select PCIe port 3 link speed. Max supported = link speed determined by PCIe device. GenX = force GenX speed
ASPM Mode Control	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Select ASPM mode for current PCIe port
Hotplug Mode Control	**Disabled** Enabled	Enable or disable hotplug on current PCIe port.
PCIe Port 4	Disabled **Enabled**	Enable or disable PCIe port 4.
Link Speed	**Max supported** Gen3 Gen2 Gen1	Select PCIe port 4 link speed. Max supported = link speed determined by PCIe device. GenX = force GenX speed
ASPM Mode Control	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Select ASPM mode for current PCIe port
Hotplug Mode Control	**Disabled** Enabled	Enable or disable hotplug on current PCIe port.
PEG Port Organization	**1 x8 Port** 2 x4 Ports	Select PEG port(s) layout

Feature	Options	Description
PEG Port 1	Disabled **Enabled**	Enable or disable PEG port 1.
Link Speed	**Max supported** Gen3 Gen2 Gen1	Select PEG port 1 link speed. Max supported = link speed determined by PCIe device. GenX = force GenX speed
ASPM Mode Control	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Select ASPM mode for current PCIe port
Hotplug Mode Control	**Disabled** Enabled	Enable or disable hotplug on current PCIe port.
PEG Port 2	Disabled **Enabled**	Enable or disable PEG port 2.
Link Speed	**Max supported** Gen3 Gen2 Gen1	Select PEG port 2 link speed. Max supported = link speed determined by PCIe device. GenX = force GenX speed
ASPM Mode Control	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Select ASPM mode for current PCIe port
Hotplug Mode Control	**Disabled** Enabled	Enable or disable hotplug on current PCIe port.

11.3.16.3 PIRQ Routing & IRQ Reservation Submenu

Feature	Options	Description
PIRQA	**Auto** IRQ3 IRQ4 IRQ10 IRQ11 IRQ14 IRQ15	Set interrupt for selected PIRQ. Please refer to the board's resource list for a detailed list of devices connected to the respective PIRQ. **NOTE:** These settings will only be effective while operating in PIC (non-IOAPIC) interrupt mode.
PIRQB	Same as PIRQA	Same as PIRQA
PIRQC	Same as PIRQA	Same as PIRQA
PIRQD	Same as PIRQA	Same as PIRQA

Feature	Options	Description
PIRQE	Same as PIRQA	Same as PIRQA
PIRQF	Same as PIRQA	Same as PIRQA
PIRQG	Same as PIRQA	Same as PIRQA
PIRQH	Same as PIRQA	Same as PIRQA
Reserve Legacy Interrupt 1	**None** IRQ3 IRQ4 IRQ10 IRQ11 IRQ14 IRQ15	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.
Reserve Legacy Interrupt 2	Same as Reserve Legacy Interrupt 1	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.

11.3.17 UEFI Network Stack Submenu

Feature	Options	Description
UEFI Network Stack	**Disabled** Enabled	Enable or disable the UEFI network stack.
IPv4 PXE Support	Disabled **Enabled**	Enable IPv4 PXE boot support. If disabled IPv4 PXE boot option will not be created.
IPv6 PXE Support	Disabled **Enabled**	Enable IPv6 PXE boot support. If disabled IPv6 PXE boot option will not be created.
PXE Boot Wait Time	Default: **1** 0 – 5	Time in seconds waiting for ESC keypress to abort the PXE boot.
Media Detect Count	Default: **1** 0 – 50	Number of times the boot media will be checked for presence.

11.3.18 CSM and Option ROM Submenu

Feature	Options	Description
CSM Support	**Enabled** Disabled	Controls the execution of the CSM module. Only disable for pure UEFI operating system support.

Feature	Options	Description
GateA20 Active	**Upon Request** Always	Gate A20 control. Upon Request: Gate A20 can be disabled using BIOS services. Always: Do not allow disabling Gate A20. This option is useful when any runtime code is executed above 1MB.
Option ROM Messages	**Force BIOS** Keep Current	Set display mode for option ROMs.
INT19 Trap Response	**Immediate** Postponed	BIOS reaction on INT19 trapping by Option ROM Immediate: Execute the trap right away. Postponed: Execute the trap during legacy boot.
Boot Option Filter	**UEFI and Legacy** Legacy Only UEFI Only	Controls which devices / boot loaders the system should boot to.
PXE Option ROM Launch Policy	**Do Not Launch** UEFI ROM Only Legacy ROM Only UEFI and Legacy	Controls the execution of UEFI and legacy PXE option ROMs. UEFI Option ROM will be executed only if UEFI Network Stack is enabled too.
Storage Option ROM Launch Policy	**Do Not Launch** UEFI ROM Only Legacy ROM Only	Controls the execution of UEFI and legacy mass storage device option ROMs
Video Option ROM Launch Policy	Do Not Launch UEFI ROM Only **Legacy ROM Only**	Controls the execution of UEFI and legacy video option ROMs
Other Option ROM Launch Policy	**UEFI ROM Only** Legacy ROM Only	Controls the execution of option ROMs for PCI / PCI Express devices other than network, mass storage or video.

11.3.19 Info Report Submenu

Feature	Options	Description
POST Report	**Enabled** Disabled	Enable or disable reporting of connected devices during POST.
Delay Time	Default: **1** 0 – 10 Until pressed ESC	Select POST report delay.
Info Error Message	**Disabled** Enabled	Add information on detected errors to POST report
Summary Screen	**Disabled** Enabled	Show system summary screen before booting legacy or UEFI OS.

Feature	Options	Description
Delay Time	Default: **5** 0 – 10 Until pressed ESC	Select summary screen delay.

11.3.20 NVMe Submenu

Feature	Options	Description
Detected NVMe devices	No option	List of detected NVMe devices

11.3.21 SDIO Submenu

Feature	Options	Description
SD Controller	Disabled **Auto** Ver2.0 Ver3.0	Select SD controller configuration. Disabled = Controller is disabled, module GPIOs are available. Auto = SD 2.0 mode with low-speed cards support. Ver2.0 = SD 2.0 mode Ver3.0 = SD 3.0 mode.
SD Access Mode	**Advanced DMA** DMA PIO	Select BIOS SD device access and boot mode. Advanced DMA = Access SD device in ADMA mode. DMA = Access SD device in DMA mode. PIO = Access SD device in PIO mode.

11.3.22 USB Submenu

Feature	Options	Description
▶ USB Controllers and Ports	Submenu	Configure USB ports and controllers.
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI OS driver.
EHCI Hand-off	**Disabled** Enabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable or disable USB mass storage BIOS support.

Feature	Options	Description
External USB Controller Support	Disabled **Enabled**	Enable or disable BIOS support for external USB controllers.
Overcurrent Protection	**Disabled** Enabled	Enable or disable USB overcurrent detection for all ports.
USB Transfer Timeout	1 sec 5sec 10 sec **20 sec**	Timeout value for legacy USB control, bulk and interrupt transfers.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device start unit command timeout.
Device Power-Up Delay Selection	**Auto** Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power-Up Delay Value	Default: **5** 1 – 40	Actual power-up delay value in seconds.
USB Mass Storage Device Name (Auto detected USB mass storage devices are listed here dynamically)	**Auto** Floppy Forced FDD Hard Disk CD-ROM	Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. **Note:** The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly. Select AUTO to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. Forced FDD allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. Hard Disk allows the device to be emulated as hard disk. CDROM assumes the CD.ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

11.3.22.1 USB Controllers and Ports Submenu

Feature	Options	Description
XHCI Controller	Disabled **Enabled**	Enable or disable the XHCI (USB 3.0) host controller.
XHCI Port 0	Disabled **Enabled**	Enable or disable XHCI port 0.
XHCI Port 1	Disabled **Enabled**	Enable or disable XHCI port 1.

Feature	Options	Description
XHCI Port 2	Disabled **Enabled**	Enable or disable XHCI port 2.
XHCI Port 3	Disabled **Enabled**	Enable or disable XHCI port 3.
EHCI Controller	Disabled **Enabled**	Enable or disable the EHCI (USB 2.0) host controller.
EHCI Hub Root Port	Disabled **Enabled**	Enable or disable EHCI hub root port.
Hub Port 0	Disabled **Enabled**	Enable or disable the current USB hub port.
Hub Port 1	Disabled **Enabled**	Enable or disable the current USB hub port.
Hub Port 2	Disabled **Enabled**	Enable or disable the current USB hub port.
Hub Port 3	Disabled **Enabled**	Enable or disable the current USB hub port.
EHCI Debug Port	Disabled **Enabled**	Enable or disable the EHCI debug port.

11.3.23 Diagnostic Settings Submenu

Feature	Options	Description
Relay Interface	**Disabled** I2C SMBus BC Diagnostic Console	Select post code redirection relay interface used for debugging.
Primary Port Addr. Lowbyte (Dec)	Default: **128** 0 - 255	Select primary port address low byte as decimal.
Primary Port Addr. Highbyte (Dec)	**0** - 255	Select primary port address high byte as decimal.
Relay Device Address (Dec)	Default: **226** 0 - 255	Select relay device address (I2C or SMBus mode only)
BC Diagnostic Console Interface	**Disabled** BC AUX Port BC COM Port 0 BC COM Port 1	Select BC diagnostic console interface.

Feature	Options	Description
Parity Bit	**No Parity** Even Parity Odd Parity	Select parity of BC diagnostic console interface.
Stop Bits	**1 Stop Bit** 2 Stop Bits	Select stop bits count of BC diagnostic console interface.
Data Bits	**8 Data Bits** 7 Data Bits 6 Data Bits 5 Data Bits	Select data bits count of BC diagnostic console interface.
Baudrate	1200 Baud 2400 Baud 4800 Baud **9600 Baud** 19200 Baud 38400 Baud	Select baudrate of of BC diagnostic console interface.

11.3.24 PC Speaker Configuration Submenu

Feature	Options	Description
Debug Beeps	Disabled **Enabled**	Enable or disable general debug / status beep generation.
Input Device Debug Beeps	**Disabled** Enabled	Enable or disable input device debug beeps.
Output Device Debug Beeps	**Disabled** Enabled	Enable or disable output device debug beeps.
USB Driver Beeps	**Disabled** Enabled	Enable or disable USB driver beeps.

11.3.25 Intel® I211 Gigabit Network Connection Submenu

Feature	Options	Description
► NIC Configuration	Submenu	Opens the NIC Configuration submenu.
Blink LEDs	Default: **0** 0 - 15	The Ethernet activity LEDs will blink as many seconds as entered.
UEFI Driver	No option	Displays the UEFI Driver version.
Adapter PBA	No option	Displays the Adapter PBA.

Feature	Options	Description
Chip Type	No option	Displays the type of Ethernet chip.
PCI Device ID	No option	Displays the PCI Device ID of the Ethernet controller.
PCI Address	No option	Displays the PCI Bus:Device:Function number of the Ethernet controller.
Link Status	No option	Displays the Link Status.
MAC Address	No option	Displays the MAC Address.

11.3.25.1 NIC Configuration Submenu

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake On LAN	Disabled **Enabled**	Enables the server to be powered on using an in-band magic packet.

11.4 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

11.4.1 Security Settings

Feature	Options	Description
BIOS Password	Enter password	Specifies the BIOS and setup administrator password.
BIOS Update & Write Protection	**Disabled** Enabled	congatec flash software will require BIOS password to perform write or erase operations.
HDD Security Configuration		
List of all detected hard disks supporting the security feature set	Select device to open device security configuration submenu	
▶Secure Boot Menu	Submenu	

11.4.1.1 BIOS Security Features

BIOS Password/ BIOS Write Protection

A BIOS password protects the BIOS setup program from unauthorized access. This ensures that end users cannot change the system configuration without authorization. With an assigned BIOS password, the BIOS prompts the user for a password on a setup entry. If the password entered is wrong, the BIOS setup program will not launch.

The congatec BIOS uses a SHA256 based encryption for the password, which is more secured than the original AMI encryption. The BIOS password is case sensitive with a minimum of 3 characters and a maximum of 20 characters. Once a BIOS password has been assigned, the BIOS activates the grayed out 'BIOS Update and Write Protection' option. If this option is set to 'enabled', only authorized users (users with the correct password) can update the BIOS. To update the BIOS, use the congatec system utility cgutlcmd.exe with the following syntax:

```
CGUTLCMD BFLASH <BIOS file> /BP: <password> where <password> is the assigned BIOS password.
```

For more information about "Updating the BIOS" refer to the congatec system utility user's guide, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

With the BIOS password protection and the BIOS update and write protection, the system configuration is completely secured. If the BIOS is password protected, you cannot change the configuration of an end application without the correct password.

Note

Use cgutlcmd.exe version 1.5.3 or later.

Built in BIOS recovery is disabled in the congatec BIOS firmware to prevent the BIOS from updating itself due to the user pressing a special key combination or a corrupt BIOS being detected. congatec considers such a recovery update a security risk because the BIOS internal update process bypasses the implemented BIOS security explained above.

Only the congatec utility interface to the SMI handler of the BIOS flash update is enabled. Other interfaces to the SMI handler are disabled to prevent non congatec tools from writing to the BIOS flash. As a result of this restriction, flash utilities supplied by AMI or Intel will not work .

UEFI Secure Boot

Secure Boot is a security standard defined in UEFI specification 2.3.1 that helps prevent malicious software applications and unauthorized operating systems from loading during system start up process. Without secure boot enabled (not supported or disabled), the computer simply hands over control to the bootloader without checking whether it is a trusted operating system or malware. With secure boot supported and enabled, the UEFI firmware starts the bootloader only if the bootloader's signature has maintained integrity and also if one of the following conditions is true:

- The bootloader was signed by a trusted authority that is registered in the UEFI database.
- The user has added the bootloader's digital signature to the UEFI database. The BIOS provides the key management setup sub-menu for this purpose.

Note

The congatec BIOS by default enables CSM (Compatibility Support Module) and disables secure boot because most of the industrial computers today boot in legacy (non-UEFI) mode. Since secure boot is only enabled when booting in native UEFI mode, you must therefore disable the CSM (compatibility support module) in the BIOS setup to enable Secure Boot.

A full description of secure boot is beyond the scope of this users guide. For more information about how secure boot leverages signature databases and keys, see the secure boot overview in the windows deployment options section of the Microsoft TechNet Library at http://technet.microsoft.com.

11.4.1.2 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to 'lock' and 'unlock' drives using the security password. A 'locked' drive will be detected by the system, but no data can be accessed. Accessing data on a 'locked' drive requires the proper password to 'unlock' the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within four attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

Note

If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

11.4.2 Boot Settings Configuration

Feature	Options	Description
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. **Note:** The default OEM logo is a dark screen.
Setup Prompt Timeout	Default: **1** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot (not recommended), 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	**Type Based** UEFI Standard	Select boot option priority selection method.
Boot Option Sorting Method	UEFI First **Legacy First**	Set boot option sorting method. UEFI First: Try all UEFI boot options before first legacy boot option. Legacy First: Try all legacy boot options before first UEFI boot option.
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if "UEFI Standard" priority list control is selected. If "Type Based" priority list control is enabled only 8 boot devices can be prioritized.)	Disabled SATA 0 Drive SATA 1 Drive NVMe Storage USB Harddisk USB CDROM Other USB Device SD Card Storage Local Area Network Firmware-based Bootloader Other Device	This view is only available when in the default "Type Based" mode. When in "UEFI Standard" mode you will only see the devices that are currently connected to the system.
Battery Support	**Auto (Battery Manager)** Battery-Only On I2C Bus Battery-Only On SMBus	Battery system support selection. Select ' Battery-Only On I2C Bus' for battery-only systems using I2C bus and ' Battery-Only On SMBus' for battery-only systems using SMBus. Select 'Auto' for systems equipped with a real battery system manager (connected via I2C or SMBus).
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. **Note:** Only works with an ATX type power supply.
AT Shutdown Mode	System Reboot **Hot S5**	Determines the behavior of an AT-powered system after a shutdown.

Feature	Options	Description
UEFI Fast Boot	**Disabled** Enabled	Enable or disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS / legacy boot options.
SATA Support	**Last Boot HDD Only** All SATA Devices	Select which SATA device to be initialized in fast boot mode.
VGA Support	Auto **UEFI Driver**	If set to Auto, the legacy video option ROM will be installed for legacy OS boot; boot logo will NOT be shown during POST. For UEFI OS boot the UEFI GOP driver will be installed.
USB Support	Disabled **Full Init** Partial Init	If set to Disabled, no USB device will be available before OS boot. If set to Partial Init, specific USB ports/devices will NOT be available before OS boot. If set to Enabled, all USB devices will be available during POST and after OS boot.
PS/2 Device Support	Disabled **Enabled**	If set to Disabled, PS/2 devices will be skipped.
Network Stack Driver Support	**Disabled** Enabled	If set to Disabled, UEFI network stack driver installation will be skipped.
Redirection Support	**Disabled** Enabled	If set to Disabled, console redirection driver installation will be skipped.
UEFI Screenshot Driver	**Disabled** Enabled	Enable or disable UEFI screenshot driver. If enabled, user can take BIOS Setup and UEFI applications screenshots by pressing LCtrl+LAlt+F12. Screenshots will be saved on the first writable FS in PNG format.

Note

1.The term 'AC power loss' stands for the state when the module loses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.

2.Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.

11.5 Save & Exit Menu

Select the Save & Exit tab from the setup menu with the <Arrow> keys to enter the Save & Exit setup screen.

11.5.1 Save & Exit Configuration

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
Generate Menu Layout File	Press to generate MLF file for MPFA-based setup visibility and text control. The file will be stored on the first writable FS found. MLF file generation is a slow process, please do not interrupt it or the resulting file may be corrupted.
Boot Override	
List of all boot devices currently detected	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to "Device Based".

12 Additional BIOS Features

The conga-TR3 uses a congatec/AMI AptioV UEFI 2.4 that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, UEFI shell command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as TR33R1xx where

- TR33 is the project code
- R is the identifier for a BIOS ROM file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The conga-TR3 BIOS binary size is 8 MB.

12.1 Supported Flash Devices

The conga-TR3 supports the following flash devices:

- Spansion S25FL064K0SMFI01 (8 MB)
- Winbond W25Q64CVSSIG (8 MB)
- Winbond W25Q64FVSSIG (8 MB)

The flash devices listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.

12.2 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS. For more information about "Updating the BIOS" please refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

13 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.3	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0	http://www.serialata.org
PICMG® COM Express Module™ Base Specification	http://www.picmg.org/
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications