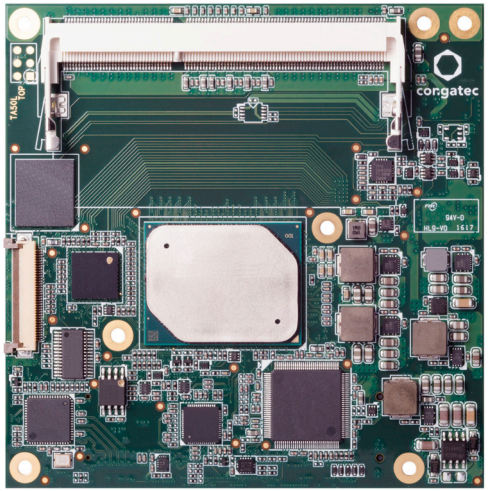

COM Express™ conga-TCA5

COM Express Type 6 Compact module based on the Intel® Atom™, Pentium™ and Celeron® Apollo Lake SoC

User's Guide

Revision 1.1

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2017.03.23	AEM	• Preliminary release
1.0	2017.10.04	AEM	• Removed Android from supported OS in section 2.2 "Supported Operating Systems" • Updated security features in table 1 "Feature Summary" and section 6.5 "Security Features" • Updated tables 5 "Power Consumption Values" and 6 "CMOS Battery Power Consumption" • Updated section 4 "Block Diagram" • Added content to sections 9 "System Resources", 10 "BIOS Description" and 11 "Additional BIOS Features" • Official release
1.1	2018.03.19	AEM	• Updated "Electrostatic Sensitive Device" information on page 3. • Removed Windows 7, 8 and Embedded Compact from the list of supported OS in section 2.2 "Supported Operating Systems" • Updated section 4 "Block Diagram" • Added caution in section 5.1.4 "USB 2.0" • Updated section 5.1.8 "UART"

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-TCA5. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide
COM Express™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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The following symbols are used in this user's guide:

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Caution

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Note

Notes call attention to important information that should be observed.

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Terminology

Term	Description
GB	Gigabyte
GHz	Gigahertz
kB	Kilobyte
MB	Megabyte
Mbit	Megabit
kHz	Kilohertz
MHz	Megahertz
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
DDC	Display Data Channel
SoC	System On Chip
LVDS	Low-Voltage Differential Signaling
Gbe	Gigabit Ethernet
eMMC	Embedded Multi-media Controller
HDA	High Definition Audio
cBC	congatec Board Controller
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

Contents

List of Tables

1 Introduction

1.1 COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express™ modules are available in following form factors:

- Mini 84mm x 55mm
- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x110mm

Table 1 COM Express™ 2.1 pinout types

Types	Connector Rows	PCIe Lanes	PCI	IDE	SATA Ports	LAN ports	USB 2.0/ USB 3.0	Display Interfaces
Type 1	A-B	Up to 6		-	4	1	8 / 0	VGA, LVDS
Type 2	A-B C-D	Up to 22	32 bit	1	4	1	8 / 0	VGA, LVDS, PEG/SDVO
Type 3	A-B C-D	Up to 22	32 bit	-	4	3	8 / 0	VGA,LVDS, PEG/SDVO
Type 4	A-B C-D	Up to 32		1	4	1	8 / 0	VGA,LVDS, PEG/SDVO
Type 5	A-B C-D	Up to 32		-	4	3	8 / 0	VGA,LVDS, PEG/SDVO
Type 6	A-B C-D	Up to 24		-	4	1	8 / 4*	VGA,LVDS/eDP, PEG, 3x DDI
Type 10	A-B	Up to 4		-	2	1	8 / 0	LVDS/eDP, 1xDDI

** The SuperSpeed USB ports (USB 3.0) are not in addition to the USB 2.0 ports. Up to 4 of the USB 2.0 ports can support SuperSpeed USB.*

The conga-TCA5 modules use the Type 6 pinout definition and comply with COM Express 2.1 specification. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 6 pinout provides the ability to offer PCI Express, Serial ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

1.2 Options Information

The conga-TCA5 is available in six variants (two commercial and four industrial). The table below shows the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Table 2 Commercial Variants

Part-No.	048530	048531
Processor	Intel® Celeron® N3350 Dual Core 1.1 GHz	Intel® Pentium® N4200 Quad Core, 1.1 GHz
L2 Cache	2 MB	2 MB
Burst Frequency	2.3 GHz	2.5 GHz
Graphics	Intel® HD Graphics 500	Intel® HD Graphics 505
GFX Base/Burst	200 MHz / 650 MHz	200 MHz / 750 MHz
Memory (DDR3L)	1866 M/T Dual Channel	1866 M/T Dual Channel
LVDS	Single/Dual 18/24 bpp	Single/Dual 18/24 bpp
Optional VGA	Yes	Yes
Default PCIe Lanes	3x PCIe lanes	3x PCIe lanes
DDI	DP 1.2 / HDMI 1.4b / DVI	DP 1.2 / HDMI 1.4b / DVI
eMMC (SLC/MLC)	Up to 32 GB MLC (optional)	Up to 32 GB MLC (optional)
SD Card	Yes	Yes
Max. TDP	6 W	6 W

Table 3 Industrial Variants

Part-No.	048510	048511	048512	048513 (with PCIe Switch)
Processor	Intel® Atom™ x7-E3950 Quad Core, 1.6GHz	Intel® Atom™ x5-E3940 Quad Core, 1.6GHz	Intel® Atom™ x5-E3930 Dual Core, 1.3GHz	Intel® Atom™ x7-E3950 Quad Core, 1.6GHz
L2 Cache	2 MB	2MB	2MB	2 MB
Burst Frequency	2.0 GHz	1.8 GHz	1.8 GHz	2.0 GHz
Graphics	Intel® HD Graphics 505	Intel® HD Graphics 500	Intel® HD Graphics 500	Intel® HD Graphics 505
GFX Base/Burst	500 MHz / 650 Mhz	400 MHz / 600 MHz	400 MHz / 550 MHz	500 MHz / 650 Mhz
Memory (DDR3L)	1866 M/T Dual Channel	1866 M/T Dual Channel	1866 M/T Dual Channel	1600MT/s dual channel
LVDS	Single/Dual 18/24 bpp	Single/Dual 18/24 bpp	Single/Dual 18/24 bpp	Single/Dual 18/24 bpp
Optional VGA	Yes	Yes	Yes	Yes
Default PCIe Lanes	3x PCIe lanes	3x PCIe lanes	3x PCIe lanes	5x PCIe lanes
DDI	DP 1.2 / HDMI 1.4b / DVI	DP 1.2 / HDMI 1.4b / DVI	DP 1.2 / HDMI 1.4b / DVI	DP 1.2 / HDMI 1.4b / DVI
eMMC (SLC/MLC)	Up to 32 GB MLC (optional)	Up to 32 GB MLC (optional)	Up to 32 GB MLC (optional)	Up to 32 GB MLC (optional)
SD Card	Yes	Yes	Yes	Yes
Max. TDP	12 W	9 W	6.5 W	12 W

2 Specifications

2.1 Feature List

Table 1 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 6 Rev. 2.1 (Compact size 95 x 95 mm)	
Processor	Intel® Atom™, Pentium® and Celeron SoC	
Memory	Two memory sockets (located on the top and bottom side). Supports - SO-DIMM non-ECC DDR3L modules - Data rates up to 1866 MT/s - Maximum 8 GB capacity	
congatec Board Controller	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, hardware monitoring, fan control, I2C bus, Power loss control	
Chipset	Integrated in SoC	
Audio	High Definition Audio interface with support for multiple codecs	
Ethernet	Gigabit Ethernet (Intel® i210-IT / i211-AT controller)	
Graphics Options	Next Generation Intel® HD (500/505). Supports: - API (DirectX 12, OpenGL 4.3, OpenCL 2.0, OpenGL ES 3.0) - Intel® QuickSync & Clear Video Technology HD (hardware accelerated video decode/encode/processing/transcode) - Up to 3 independent displays (must be two DDI's (DP, HDMI/DVI) and one eDP/LVDS)	
	1x LVDS *1 2x DDIs *2 with support for: - 2x DisplayPort++ (DisplayPort 1.2a) - 2x HDMI 1.4b*3 - 2x DVI port *3 - Resolutions up to 4K	**Optional Interface (assembly option)**: - 1x eDP 1.3 *1 - 1x VGA *2 **NOTE**: *1 *Variants that feature optional eDP interface do not support LVDS* *2 *Variants that feature optional VGA interface support only 1x DDI* *3 *Requires an external level shifter on the carrier board*
Peripheral Interfaces	USB Interfaces: - 4x USB 2.0 - 4x USB 3.0/2.0 Buses - LPC - I²C (fast mode, multi-master) - SMB - SPI	2x SATA® (6 Gbps) 2x UART GPIOs 3x PCI Express® Gen. 3 lanes *1 *2 **NOTE**: *1 *5x PCIe lanes for variants that feature PCIe switch* *2 *4x PCIe lanes for variants without Gigabit Ethernet controller and PCIe switch*
BIOS	AMI Aptio® UEFI 5.x firmware, 8 or 16 MByte serial SPI with congatec Embedded BIOS features	
Storage	Optional eMMC 5.0 onboard flash, with up to 32 GB storage capacity	

Power Management	ACPI 4.0 compliant with battery support. Also supports Suspend to RAM (S3) and Intel AMT 10 Configurable TDP Ultra low standby power consumption, Deep Sx
Security	Firmware TPM 2.0 (Intel® PTT) Discrete LPC TPM 2.0 (Infineon SLB9665) or LPC TPM 1.2 (Infineon SLB9660) support via assembly option

Note

Some of the features mentioned above are optional (assembly option). To determine the features on your particular module, compare the part number of your module to the options information list on page 11 and 12. For more information, contact congatec support.

2.2 Supported Operating Systems

The conga-TCA5 supports the following operating systems

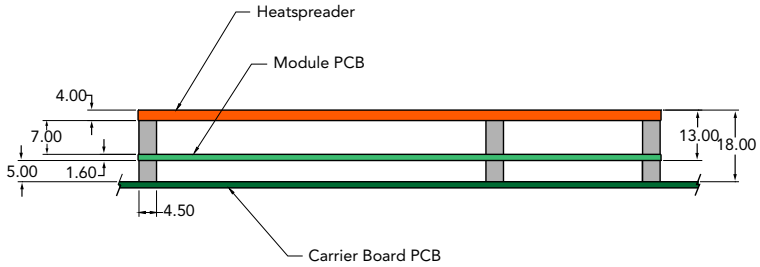
- Microsoft® Windows® 10 Enterprise (64-bit)
- Microsoft® Windows® 10 IoT Core (32/64-bit)
- Linux 3.x/4.x
- Yocto 2.x

Note

Microsoft® recommends a minimum storage capacity of 16 GB for Windows 32-bit OS and 20 GB for 64-bit OS. congatec does not offer installation support for systems which do not meet the recommended storage capacity.

2.3 Mechanical Dimensions

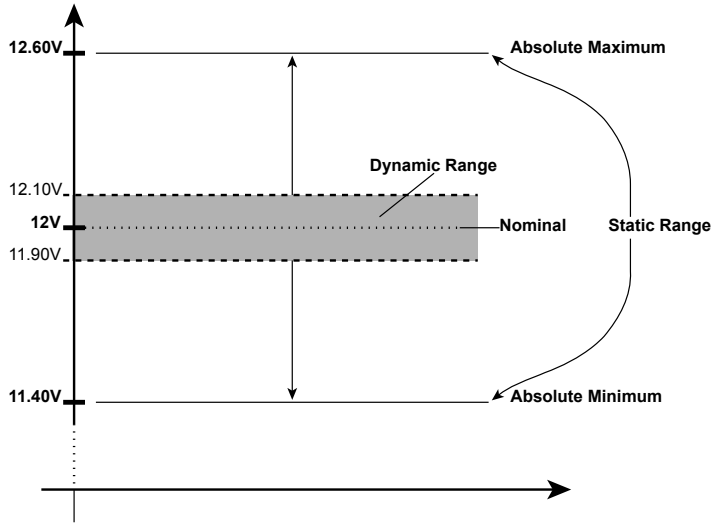
- 95.0 mm x 95.0 mm (3.75" x 3.75")
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm



2.4 Supply Voltage Standard Power

- 12V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-TCA5 COM
- modified congatec carrier board
- conga-TCA5 cooling solution
- Microsoft Windows 10 (64 bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool

Table 4 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle.	The CPU was stressed to its maximum frequency.
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency.
S0: Peak value	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.
S3	COM is powered by VCC_5V_SBY.	
S5	COM is powered by VCC_5V_SBY.	

Note

1. *The fan and SATA drives were powered externally.*

2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Table 5 Power Consumption Values

The tables below provide additional information about the power consumption data for each of the conga-TCA5 variants offered. The values are recorded at various operating modes.

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (Amp.)				
					Variant	Cores	Freq/Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5
048510	2 x 4 GB	A.1	R117	Windows 10	Intel® Atom™ x7-E3950	4	1.6 / 2.0	0.14	1.66	1.85	0.07	0.06
048511	2 x 4 GB	A.0	R117	Windows 10	Intel® Atom™ x5-E3940	4	1.6 / 1.8	0.16	1.34	1.44	0.12	0.10
048512	2 x 4 GB	A.0	R117	Windows 10	Intel® Atom™ x5-E3930	2	1.3 / 1.8	0.11	0.97	1.02	0.12	0.10
048513	2 x 4 GB	A.0	R117	Windows 10	Intel® Atom™ x7-E3950 (with PCIe Switch)	4	1.6 / 2.0	0.23	1.75	1.92	0.12	0.11
048530	2 x 4 GB	A.0	R117	Windows 10	Intel® Celeron™ N3350	2	1.1 / 2.3	0.12	1.05	1.53	0.08	0.06
048531	2 x 4 GB	A.0	R117	Windows 10	Intel® Pentium® N4200	4	1.1 / 2.5	0.12	1.04	1.85	0.11	0.10

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 6 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	2.17 µA
20°C	3V DC	2.37 µA
70°C	3V DC	3.37 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider also the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec AG website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-TCA5.*

2.7 Environmental Specifications

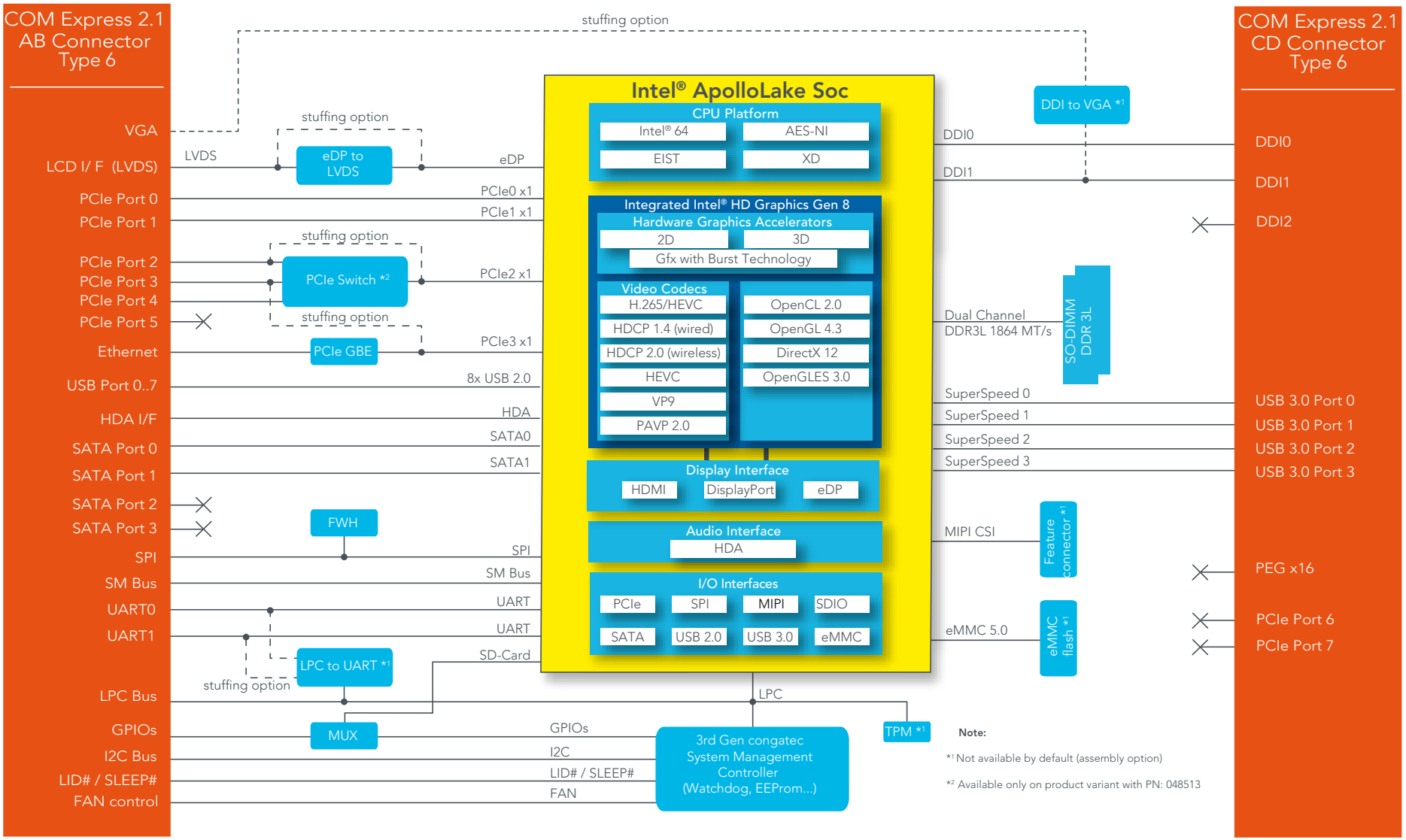
Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation: -40° to 60°C	Storage: -45° to +85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



4 Cooling Solutions

congatec AG offers the following cooling solutions for the conga-TCA5 commercial and industrial variants:

- Passive cooling solution (CSP)
- Heatspreader

The heatspreader acts as a thermal coupling device to the module and is thermally coupled to the CPU via a thermal gap filler. On some modules, it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis thereby using the whole chassis as a heat dissipater.

The dimensions of the cooling solutions are shown below. All measurements are in millimeters. The mechanical system assembly mounting shall follow the valid DIN/ISO specifications. The recommended maximum torque specification for all screws is 0.3 Nm.

Note

The gap pad material used on all congatec heatspreaders contains silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.

Caution

The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.

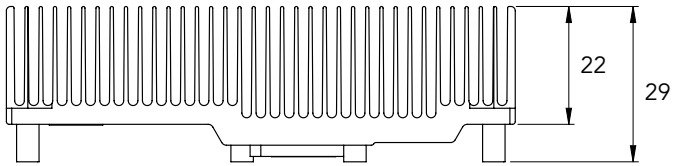
For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.

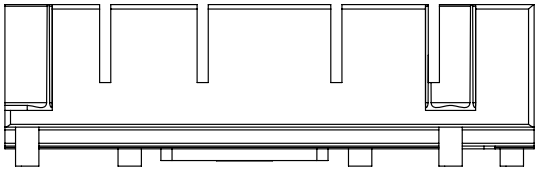
For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.

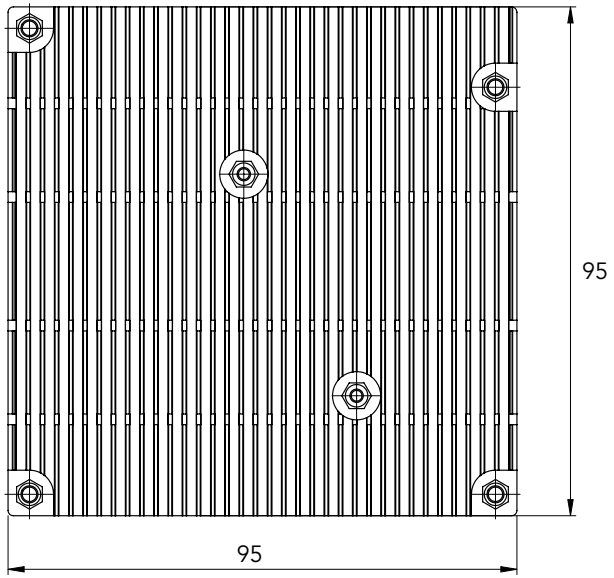
Also, do not exceed the maximum torque specified for the screws. Doing so may damage the module or/and the carrier board.

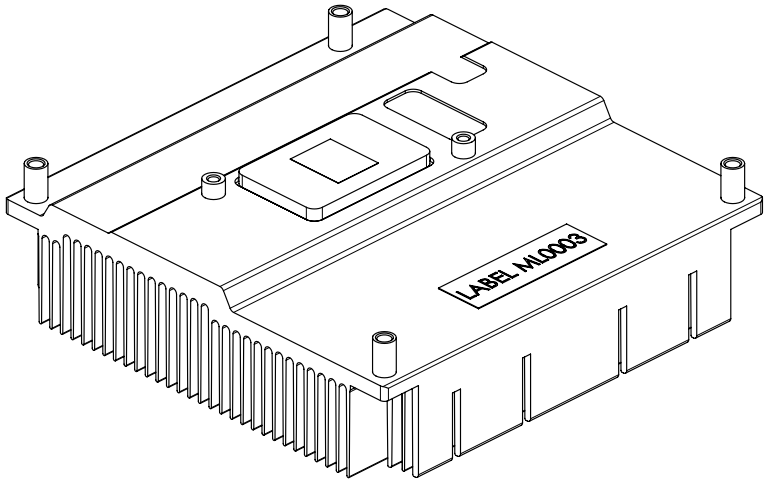
4.1 CSP Dimensions

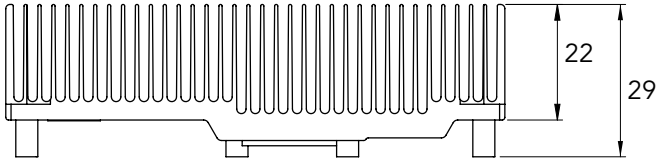
Commercial Variant

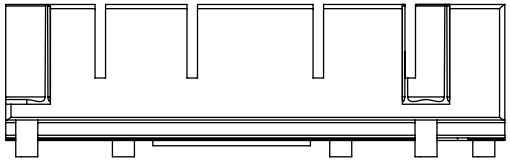


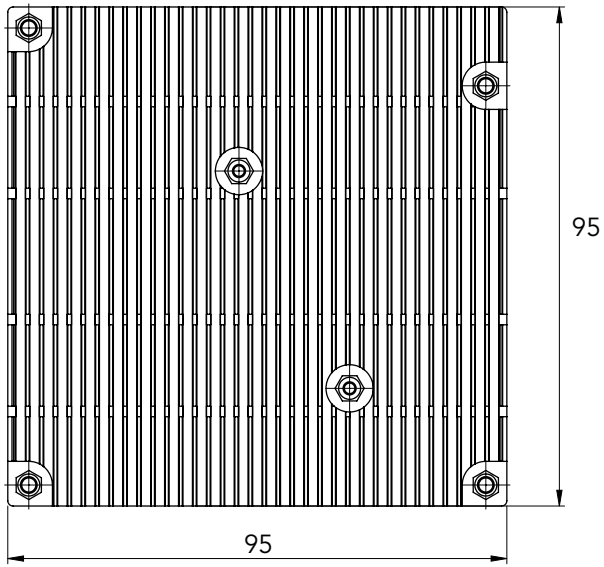


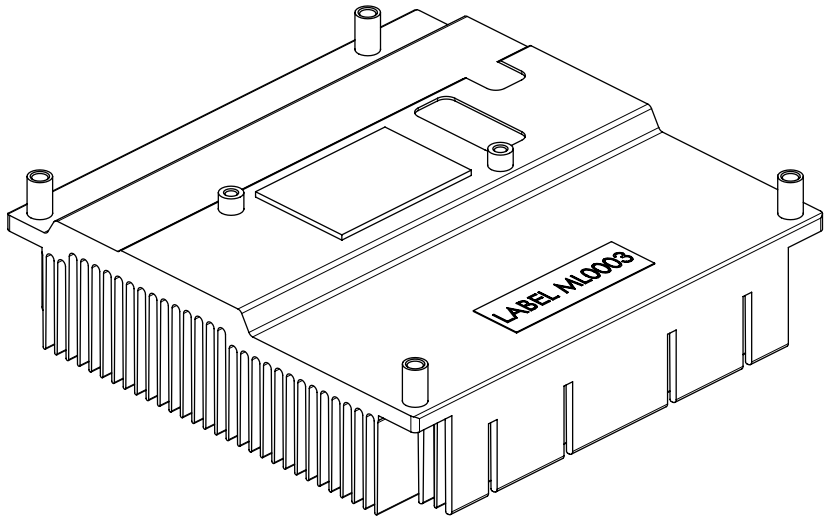






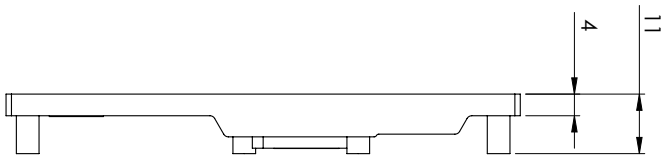


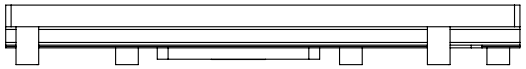


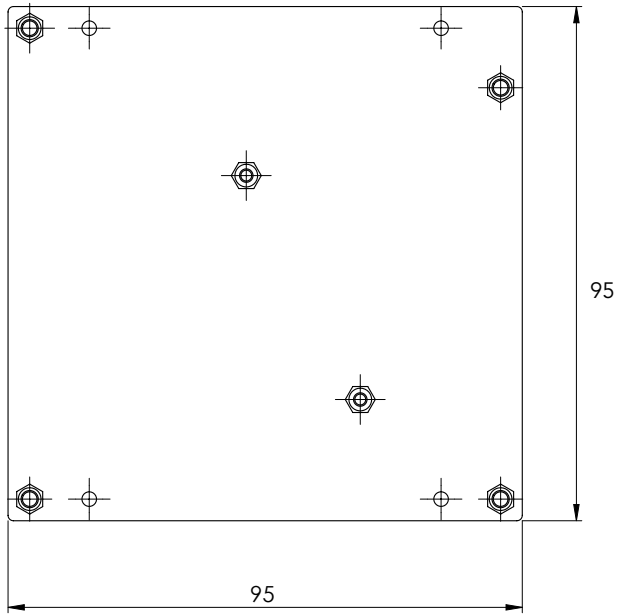


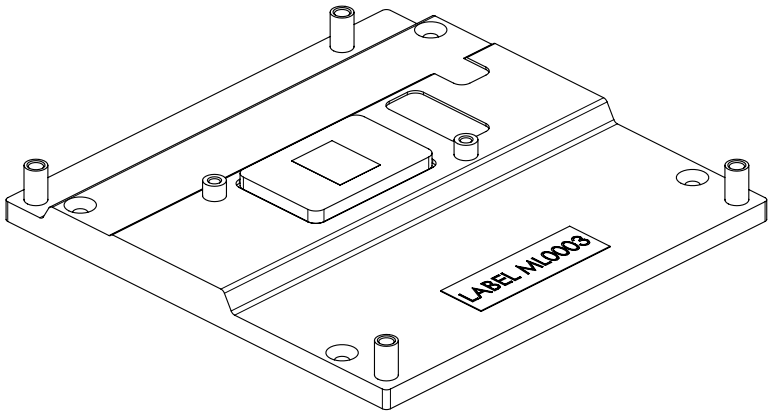
4.2 Heatspreader Dimensions

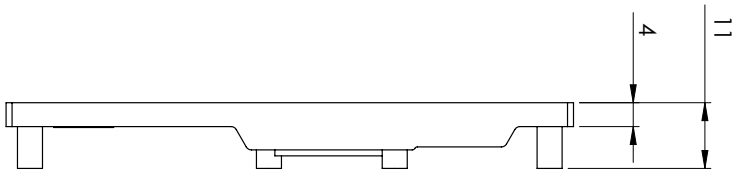
Commercial Variant

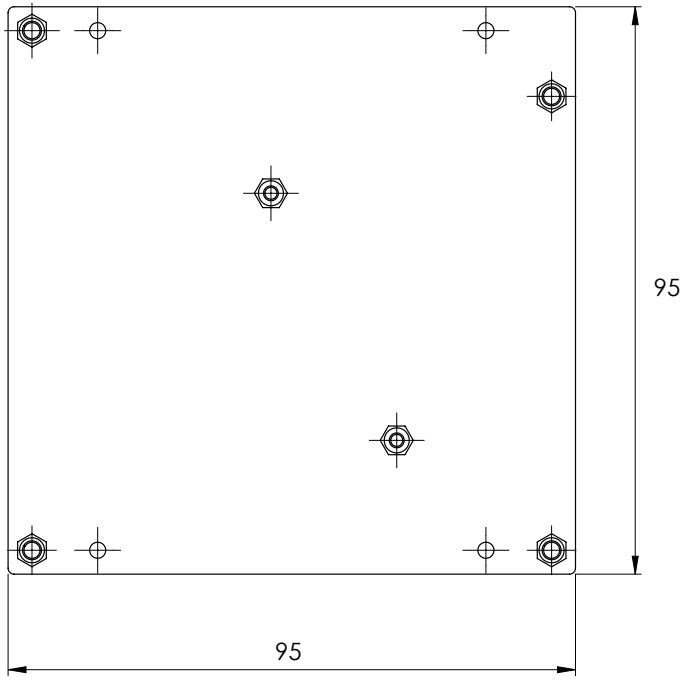


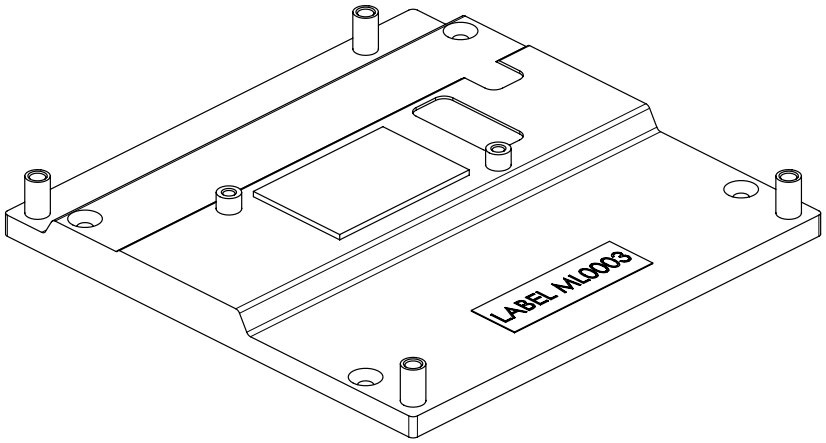












5 Connector Rows

The conga-TCA5 is connected to the carrier board via two 220-pin connectors (COM Express Type 6 pinout). These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

5.1 Primary Connector Rows A and B

The following subsystems can be found on the primary connector rows A and B.

5.1.1 PCI Express™

The conga-TCA5 offers three PCI Express™ lanes on the A-B connector. The lanes support:

- up to 5 GT/s (Gen 2) speed
- a 3 x1 link configuration
- an optional 1 x2 + 1 x1 link configuration (requires a special/customized BIOS firmware)

Note

Variants equipped with PCIe switch support up to five PCIe lanes.

5.1.2 Gigabit Ethernet

The conga-TCA5 offers a Gigabit Ethernet interface via an onboard Intel® i210-IT / i211-AT Gigabit Ethernet controller. The interface supports full-duplex operation at 10/100/1000 Mbps and half-duplex operation at 10/100 Mbps.

Note

The GBE0_LINK# output is only active during a 100 megabit or 1 gigabit connection. It is not active during a 10 megabit connection. This is a limitation of Ethernet controller, since it only has 3 LED outputs - ACT#, LINK100# and LINK1000#. The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TCA5 module.

5.1.3 SATA

The conga-TCA5 offers two SATA interfaces (SATA 0-1) on the A-B connector. The interfaces support:

- independent DMA operation
- data transfer rates up to 6.0 Gbps
- AHCI mode
- Hot-plug detect

Note

The interface does not support IDE mode.

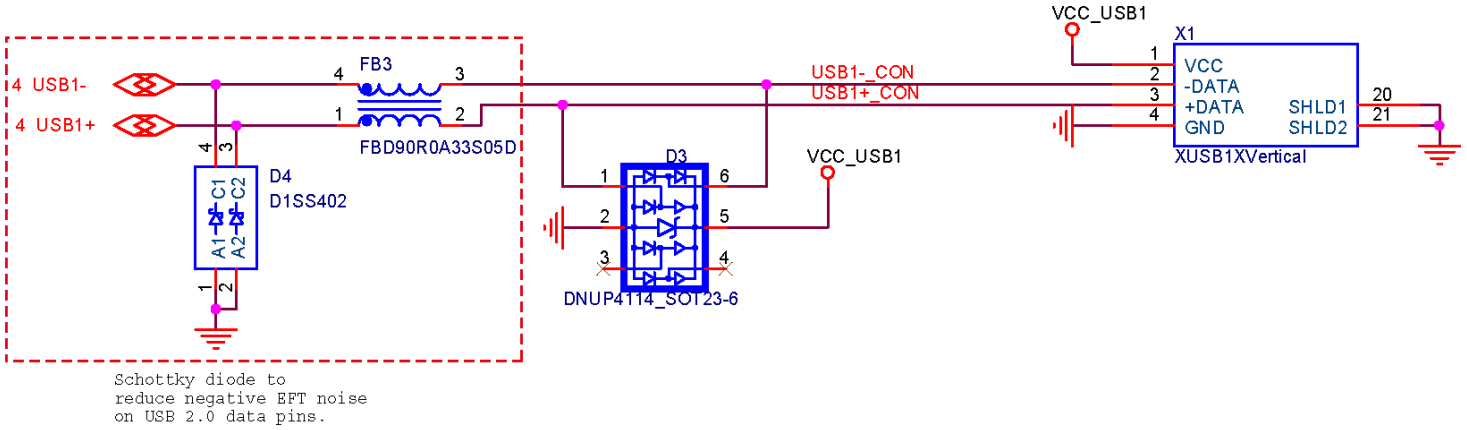
5.1.4 USB 2.0

The conga-TCA5 offers up to eight USB 2.0 interfaces on the A-B connector. The xHCI host controller in the PCH supports these interfaces with High-Speed, Full-Speed and Low-Speed USB signaling. The controller complies with USB standard 1.1 and 2.0.

For more information on how the ports are routed, see section 7.3 "USB Port Mapping".

Caution

To pass the Electrical Fast Transient (EFT) test, you must add a schottky diode (1SS402 or equivalent) to all USB2.0 data lanes routed to a connector on your carrier board. The schottky diode must be placed before the common-mode choke as shown below.



5.1.5 LVDS

The conga-TCA5 offers an LVDS interface with optional eDP overlay on the AB connector. The LVDS interface provides LVDS signals by default, but can optionally support eDP signals (assembly option). For more information, contact congatec technical center.

The LVDS interface supports:

- single or dual channel LVDS (color depths of 18 bpp or 24 bpp)
- integrated flat panel interface with clock frequency up to 112 MHz
- VESA and OpenLDI LVDS color mappings
- automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3
- resolution up to 1920x1200 in dual LVDS bus mode

Note

The LVDS/eDP interface supports either LVDS or eDP signals. Both signals are not supported simultaneously.

5.1.6 VGA

The Intel Apollo Lake SoC does not natively support VGA interface. However, the conga-TCA5 can support this interface by integrating an optional DisplayPort to VGA adapter chip.

Note

For VGA support, you need a customized conga-TCA5 variant.

5.1.7 High Definition Audio (HDA) Interface

The conga-TCA5 provides an interface that supports HDA audio codecs.

5.1.8 UART

The conga-TCA5 provides two UART ports routed from the SoC by default. These interfaces support up to 3.68 Mbps (high-speed mode). They do not support hardware handshake and flow control. Optionally, the UART ports can be routed from an LPC controller (Exar XR28V382) instead.

Note

The UART ports routed from the SoC cannot be used under Windows because Intel does not provide the necessary driver. The UART ports routed from the SoC can only be used under Linux. The UART ports routed from the LPC controller (Exar XR28V382) can also be used under Windows 10 without a special driver.

5.1.9 ExpressCard™

The conga-TCA5 supports the implementation of ExpressCards, which requires the dedication of one USB port and a x1 PCI Express link for each ExpressCard used.

5.1.10 SD Card

The conga-TCA5 offers a 4-bit SD interface for SD/MMC cards on the A-B connector. The SD signals are multiplexed with GPIO signals and controlled by the congatec Board controller. The SD card controller in the Storage Control Cluster of the SoC supports the SD interface with up to 832 Mbps data rate using 4 parallel data lines.

5.1.11 GPIOs

The conga-TCA5 offers General Purpose Input/Output signals on the AB connector.

5.1.12 LPC Bus

The conga-TCA5 offers the LPC (Low Pin Count) bus on the A-B connector. For information about the decoded LPC addresses, see section 9.1.1.

Note

All conga-TCA5 CPUs run the LPC bus at 25 MHz.

5.1.13 I²C Bus

The I²C bus is implemented through the congatec board controller (Texas Instruments Tiva™ TM4E1231H6ZRB) and accessed through the congatec CGOS driver and API. The controller provides a fast-mode multi-master I²C bus that has the maximum I²C bandwidth.

5.1.14 SPI

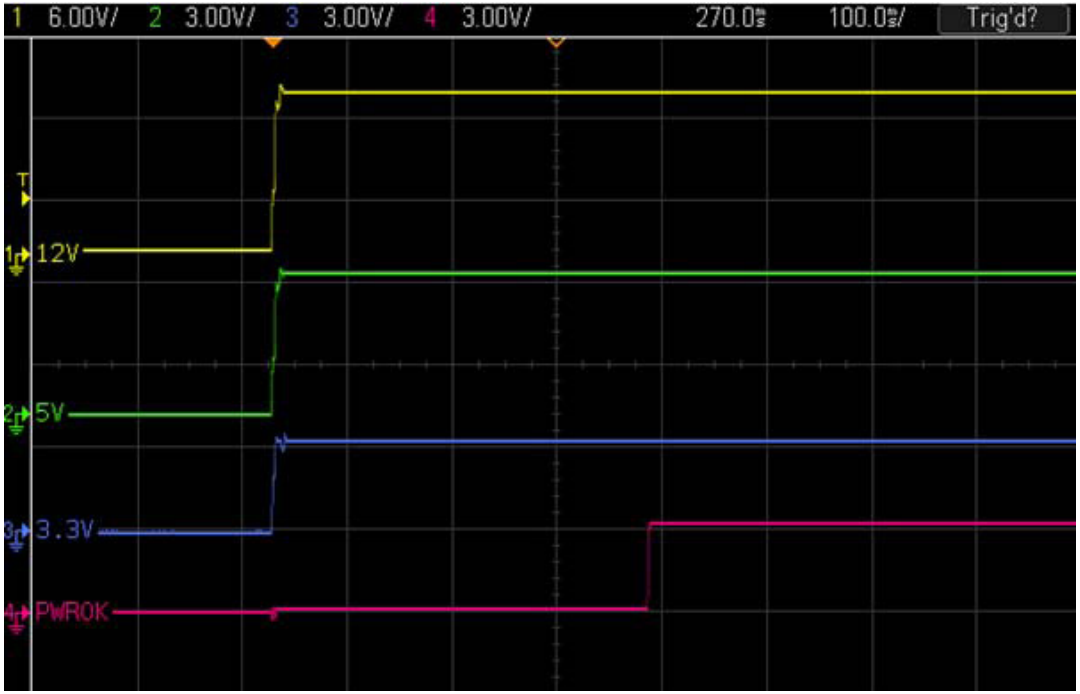
The conga-TCA5 supports SPI interface. This interface makes it possible to boot from an external SPI flash (alternative interface for the BIOS flash device).

5.1.15 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. See screenshot below.



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The conga-TCA5 supports the controlling of ATX-style power supplies. If you do not use an ATX power supply, do not connect the conga-TCA5 pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# on the conga-TCA5.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

12 volt input power is the sole operational power source for the conga-TCA5. The remaining necessary voltages are generated internally on the module using onboard voltage regulators.

A carrier board designer should be aware of the following important information when designing a power supply for a conga-TCA5 application:

- We noticed that occasionally problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. This problem is rare but has been observed in some mobile power supply applications. To ensure that this problem does not occur, observe the power supply rise waveform with an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. Do this during the power supply qualification phase to ensure that the above mentioned problem does not occur in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document “ATX12V Power Supply Design Guide V2.2”.

5.1.16 Power Management

ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).

5.2 Secondary Connector Rows C and D

The following sub-systems can be found on the secondary connector rows C and D.

5.2.1 USB 3.0

The conga-TCA5 offers two RX and two TX differential signal pairs on the CD connector to support two USB 3.0 ports (USB 0 -1). The xHCI host controller provided by the SoC's controller hub controls these ports and allows data transfers of up to 5 Gbps with SuperSpeed, highspeed, full-speed and low-speed traffic support. For more information about how the USB host controllers are routed, see section 7.5.

Note

Each USB 3.0 port should be paired with corresponding USB 2.0 differential data pairs on the carrier board.

5.2.2 Digital Display Interface

The conga-TCA5 supports:

- up to two Digital Display Interfaces (digital port B and C)
- dual mode (DP++) on each interface
- the configuration of each interface as DisplayPort or HDMI/DVI
- audio on DP and HDMI interfaces
- an optional VGA interface on the DDI digital port C, via a DP to VGA adapter IC *1
- up to three independent displays (default display combinations must be 2 x DDI and 1 x LVDS) *2

The table below shows the conga-TCA5 display combinations. This table does not apply to customized variants equipped with optional VGA interface

Table 2 Display Combination

Display 1 (DDI Port B)	Display 2 (DDI Port C)	Display 3	Display 1 Max. Resolution	Display 2 Max. Resolution	Display 3 Max. Resolution
HDMI 1.4	HDMI 1.4	eDP	3840 x 2160 @ 30 Hz, 24 bpp	3840 x 2160 @ 30 Hz, 24 bpp	4096 x 2160 @ 60 Hz, 24 bpp
DP	DP	eDP	4096 x 2160 @ 60 Hz, 24bpp	4096 x 2160 @ 60 Hz, 24bpp	4096 x 2160 @ 60 Hz, 24 bpp
HDMI 1.4	DP	eDP	3840 x 2160 @ 30 Hz, 24 bpp	4096 x 2160 @ 60 Hz, 24bpp	4096 x 2160 @ 60 Hz, 24 bpp

Note

*[*1] Requires a customized conga-TCA5 variant*

*[*2] Assembly option combinations: 1 x DDI + 1 x eDP / LVDS + 1 x DDI / VGA*

5.2.2.1 HDMI

HDMI (High-Definition Multimedia Interface) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. It encodes the video data into TMDS for digital transmission. It is also backward-compatible with the single-link DVI (Digital Visual Interface) carrying digital video.

The congaTCA5 supports up to two dedicated HDMI interfaces.

Note

See table 2 above for possible display combinations.

5.2.2.2 DVI

Similar to HDMI, DVI uses TMDS to transmit data but unlike the HDMI, it does not support audio and CEC. The congaTCA5 supports up to two dedicated DVI interfaces.

Note

See table 2 above for possible display combinations.

5.2.2.3 DisplayPort (DP)

The conga-TCA5 supports up to two DP interfaces. The interfaces are available on the CD connector.

Note

See table 2 above for possible display combinations.

6 Additional Features

6.1 Onboard Interfaces

6.1.1 Optional eMMC 5.0

The conga-TCA5 offers an optional eMMC 5.0 flash onboard, with up to 32 GB capacity.

6.1.2 Low Voltage Memory (DDR3L)

The SoC on the conga-TCA5 supports low voltage system memory interface. The memory interface I/O voltage is 1.35V and supports unbuffered DDR3L SO-DIMMs. With this low voltage system memory interface on the processor, the conga-TCA5 offers a system optimized for lowest possible power consumption. The reduction in power consumption due to lower voltage subsequently reduces the heat generated.

6.1.3 congatec Board Controller (cBC)

The conga-TCA5 is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRBI microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

6.1.3.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.1.3.2 General Purpose Input/Output

The conga-TCA5 offers general purpose inputs and outputs for custom system design. These GPIOs are multiplexed with SD signals and are controlled by the cBC.

6.1.3.3 Fan Control

The conga-TCA5 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

1. *Use a four-wire fan to generate the correct speed readout.*

2. *For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express Design Guide.*

6.1.3.4 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

6.1.3.5 Watchdog

The conga-TCA5 is equipped with a multi stage watchdog solution that is triggered by software. The conga-TCA5 does not support external hardware triggering because the COM Express™ Specification does not provide support for external hardware triggering of the Watchdog.

For more information, see the BIOS setup description in section 10.4.2 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

Note

The conga-TCA5 module does not support the watchdog NMI mode.

6.1.3.6 I²C Bus

The conga-TCA5 supports I²C bus. Thanks to the I²C host controller in the cBC the I²C bus is multimaster capable and runs at fast mode.

6.2 OEM BIOS Customization

The conga-TCA5 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

6.2.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.2.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.2.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.2.4 OEM BIOS Code/Data

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table (OA2.0), Windows 8 OEM activation (OA3.0), verb tables for HDA codecs, PCI/PCIe opROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.2.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.3 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec AG defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addition to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-TCA5 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

6.4 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website.

6.5 Security Features

The conga-TCA5 has a firmware TPM 2.0 (Intel® PTT). Follow the steps below to enable or disable the firmware TPM 2.0:

- enter the BIOS setup menu (see section 10.1 "Navigating the BIOS Setup Menu")
- navigate to **Advanced Setup** menu
- navigate to **Platform Trust Technology** submenu and press ENTER
- enable or disable fTPM

Note

1. *The conga-TCA5 supports discrete LPC TPM 2.0 (Infineon SLB9665) or discrete LPC TPM 1.2 (Infineon SLB9660) via assembly option.*
2. *Always disable fTPM (firmware TPM) if you use a discrete TPM.*

6.6 Suspend to Ram

The Suspend to RAM feature is available on the conga-TCA5.

7 conga Tech Notes

The conga-TCA5 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the system resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Description section.

7.1 Intel® Apollo Lake SoC Features

7.1.1 Processor Core

The SoC features Dual or Quad Out-of-Order Execution processor cores. The cores are grouped into Dual-Core modules with each module sharing a 1 MB L2 cache (512 KB per core). Some of the features supported by the core are:

- Intel 64 architecture
- Intel Streaming SIMD Extensions
- Support for Intel VTx-2 and VT-d
- Thermal management support vial Intel Thermal Monitor
- Uses Power Aware Interrupt Routing
- Uses 14 nm process technology

Note

Intel Hyper-Threading technology is not supported (four cores execute four threads)

7.1.1.1 Intel Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel® VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

7.1.1.2 AHCI

The SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

Legacy Mode

When operating in legacy mode, the SATA controllers need two legacy IRQs (14 and 15) and are unable to share these IRQs with other devices. This is because the SATA controllers emulate the primary and secondary legacy IDE controllers.

Native Mode

Native mode allows the SATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources. This means they can be configured anywhere within the system. When either SATA controller 1 or 2 runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system. Setting "Native IDE" mode in the BIOS setup program will automatically enable Native mode. See section 10.4.9 for more information about this. Running in native mode frees up interrupt resources (IRQs 14 and 15) and decreases the chance that there may be a shortage of interrupts when installing devices.

Note

If your operating system supports native mode then congatec AG recommends you enable it.

7.1.1.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-TCA5 ACPI thermal solution offers two different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.2 ACPI Suspend Modes and Resume Events

The conga-TCA5 BIOS supports S3 (Suspend to RAM). The BIOS does not support S4 (Suspend to Disk) even though the following operating systems support it (S4_OS = Hibernate):

- Windows 7, Windows 8.1, Windows 10 and Linux

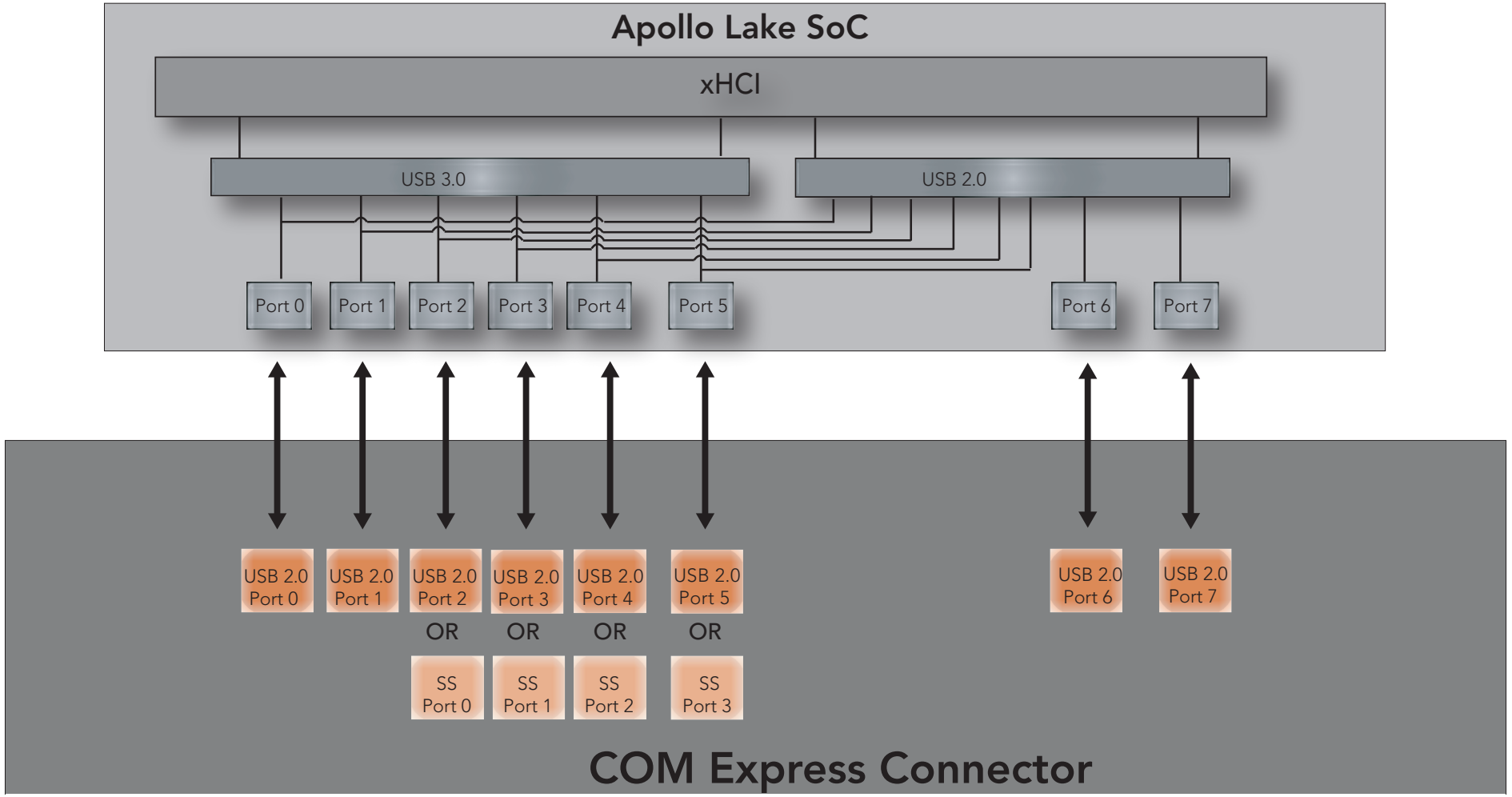
For more information about ACPI, see section 10.4.5 "ACPI Configuration Submenu".

Table 7 Wake Events

The table below lists the events that wake the system from S3.

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S3-S5.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
WAKE#	Wakes unconditionally from S3.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

7.3 USB Port Mapping



8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type 6 connectors used for congatec AG modules. The pinout of the modules complies with COM Express Type 6 Rev. 2.1.

The table below describes the terminology used in this section. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors. Only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 3 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
SATA	In compliance with Serial ATA specification, Revision 3.0
REF	Reference voltage output. May be sourced from a module power plane
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

8.1 A-B Connector Signal Descriptions

Table 4 Intel® High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	**Intel® High Definition Audio Reset:** This signal is the master hardware reset to external codec(s).	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SYNC	A29	**Intel® High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_BITCLK	A32	**Intel® High Definition Audio Bit Clock Output:** This signal is a 24.000MHz serial data clock generated by the Intel® High Definition Audio controller.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SDOUT	A33	**Intel® High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mbps for Intel® High Definition Audio.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SDIN0	B29-B30	**Intel® High Definition Audio Serial Data In 0:** This signal is the serial TDM data input from the codec(s). This serial input is single-pumped for a bit rate of 24 Mbps for Intel® High Definition Audio.	I 3.3V	2k2 PD	AC'97 codecs are not supported. AC/HDA_SDIN[2:1] signals are not supported.

Table 5 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		Twisted pair signals for external transformer.
			1000	100	10			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.				O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.				O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.				O 3.3VSB		

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.			Not connected

Table 6 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA 3 specification, up to 6 Gbps
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA 3 specification, up to 6 Gbps
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA 3 specification, up to 6 Gbps
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA 3 specification, up to 6 Gbps
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Not supported
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Not supported
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Not supported
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Not supported
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	I/O 3.3v		

Table 7 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0.
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Not supported
PCIE_CLK_ REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 8 ExpressCard Support Pins Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE#	A49	ExpressCard 0 capable card request.	I 3.3V	PU 100k 3.3V	
EXCD0_PERST#	A48	ExpressCard 0 Reset	O 3.3V		
EXCD1_CPPE#	B48	ExpressCard 1 capable card request	I 3.3V	PU 100k 3.3V	
EXCD1_PERST#	B47	ExpressCard 1 Reset	O 3.3V		

Table 9 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V		Not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3V		
LPC_CLK	B10	LPC clock output - 25MHz nominal	O 3.3V		

Table 10 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1

Signal	Pin #	Description	I/O	PU/PD	Comment
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board..

Table 11 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not supported by default
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not supported by default
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not supported by default
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		Not supported by default
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		Not supported by default
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O OD 5V		Not supported by default
VGA_I2C_DAT	B96	DDC data line.	I/O OD 5V		Not supported by default

Note

The optional VGA interface requires a customized variant

Table 12 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10k	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10k	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V	PD 10k	
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V		
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V		

Table 13 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 100k 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	+ 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10k 3.3VSB	Carrier shall pull to GND or leave no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10k 3.3VSB	Carrier shall pull to GND or leave no-connect.

Table 14 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O 3.3V	PU 2k2 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O 3.3V	PU 2k2 3.3VSB	
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V	PU10K	
FAN_TACHIN	B102	Fan tachometer input.	I OD	PU 51k 3.3V	Requires a fan with a two pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V		Trusted Platform Module chip is optional.

Note

For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express Design Guide.

Table 15 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3V		
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3V		
GPO2	B57	General purpose output pins. Shared with SD_WP. Output from COM Express, input to SD	O 3.3V		
GPO3	B63	General purpose output pins. Shared with SD_CD. Output from COM Express, input to SD	O 3.3V		
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode

Table 16 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low.	I 3.3VSB	PU 10k 3.3 VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V	PU 100k 3.3VSB	Connected via series diode to onboard voltage monitor
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON#") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		

Signal	Pin #	Description	I/O	PU/PD	Comment
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		Not supported by chipset. Shorted with SUS_S4#.
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 16k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 16k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10k 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 100k 3.3V	
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V		
SMB_CK	B13	System Management Bus bidirectional clock line.	I/O 3.3VSB	PU 2k2 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line.	I/O OD 3.3VSB	PU 2k2 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3VSB	PU 10k 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch.	I OD 3.3V	PU 100k 3.3VSB	
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3V	PU 100k 3.3VSB	

Table 17 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O 3.3V		
SER1_TX	A101	General purpose serial port transmitter	O 3.3V		
SER0_RX	A99	General purpose serial port receiver	I 3.3V	51k 3.3V	
SER1_RX	A102	General purpose serial port receiver	I 3.3V	51k 3.3V	

Table 18 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

8.2 A-B Connector Pinout

Table 19 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0# *1	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# *1	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF *1	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+ *1	B22	SATA3_TX+ *1	A77	LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX- *1	B23	SATA3_TX- *1	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+ *1	B25	SATA3_RX+ *1	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX- *1	B26	SATA3_RX- *1	A81	LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2 *1	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1 *1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA_BITCLK	B32	SPKR	A87	RSVD	B87	VCC_5V_SBY
A33	AC/HDA_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED *2
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN *2
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU *2
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC *2
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC *2
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK *2
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT *2
A42	USB2-	B42	USB3-	A97	TYPE10# *1	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+ *1	B52	PCIE_RX5+ *1	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5- *1	B53	PCIE_RX5- *1	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

*1 *Not supported on conga-TCA5*

*2 *Supported via an assembly option (customized variant).*

8.3 C-D Connector Signal Descriptions

Table 20 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		Not supported.
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		Not supported.
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		Not supported.
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		Not supported.

Table 21 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX0-	C3		I		
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX0-	D3		O		
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX1-	C6		I		
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX1-	D6		O		
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX2-	C9		I		.
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX2-	D9		O		
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX3-	C12		I		
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX3-	D12		O		

Table 22 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs. *Note: Can also be used as PCI Express Receive Input differential pairs 16 through 31 known as PCIE_RX[16-31] + and -.*	I PCIE		Not supported.
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+ PEG_TX0- PEG_TX1+ PEG_TX1- PEG_TX2+ PEG_TX2- PEG_TX3+ PEG_TX3- PEG_TX4+ PEG_TX4- PEG_TX5+ PEG_TX5- PEG_TX6+ PEG_TX6- PEG_TX7+ PEG_TX7- PEG_TX8+ PEG_TX8- PEG_TX9+ PEG_TX9- PEG_TX10+ PEG_TX10- PEG_TX11+ PEG_TX11- PEG_TX12+ PEG_TX12- PEG_TX13+ PEG_TX13- PEG_TX14+ PEG_TX14- PEG_TX15+ PEG_TX15-	D52 D53 D55 D56 D58 D59 D61 D62 D65 D66 D68 D69 D71 D72 D74 D75 D78 D79 D81 D82 D85 D86 D88 D89 D91 D92 D94 D95 D98 D99 D101 D102	PCI Express Graphics Transmit Output differential pairs. *Note: Can also be used as PCI Express Transmit Output differential pairs 16 through 31 known as PCIE_TX[16-31] + and -.*	O PCIE		Not supported.
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I		Not supported.

Note

PCI Express Graphics is not supported on conga-TCA5 modules

Table 23 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with SDVO1_RED+, DP1_LANE0+ and TMDS1_DATA2+. Multiplexed with SDVO1_RED-, DP1_LANE0- and TMDS1_DATA2-.	O PCIE		Only TMDS/DP option, no SDVO.
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with SDVO1_GRN+, DP1_LANE1+ and TMDS1_DATA1+. Multiplexed with SDVO1_GRN-, DP1_LANE1- and TMDS1_DATA1-.	O PCIE		Only TMDS/DP option, no SDVO.
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with SDVO1_BLU+, DP1_LANE2+ and TMDS1_DATA0+. Multiplexed with SDVO1_BLU-, DP1_LANE2- and TMDS1_DATA0-.	O PCIE		Only TMDS/DP option, no SDVO.
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with SDVO1_CK+, DP1_LANE3+ and TMDS1_CLK+. Multiplexed with SDVO1_CK-, DP1_LANE3- and TMDS1_CLK-.	O PCIE		Only TMDS/DP option, no SDVO.
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	Multiplexed with SDVO1_INT+. Multiplexed with SDVO1_INT-.			Not supported due to missing SDVO support.
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	Multiplexed with SDVO1_TVCLKIN+. Multiplexed with SDVO1_TVCLKIN-.			Not supported due to missing SDVO support.
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	Multiplexed with SDVO1_FLDSTALL+. Multiplexed with SDVO1_FLDSTALL-.			Not supported due to missing SDVO support.
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD.	I 3.3V	PD 100k	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with SDVO1_CTRLCLK, DP1_AUX+ and HDMI1_CTRLCLK. DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PD100k @ DP mode, PU 2.49k 3.3V @ HDMI/DVI mode	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with SDVO1_CTRLDATA, DP1_AUX- and HDMI1_CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PU 100k 3.3V@ DP mode, PU 2.49k 3.3V @ HDMI/DVI mode	
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+ and TMDS2_DATA2+. Multiplexed with DP2_LANE0- and TMDS2_DATA2-.	O PCIE		
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+ and TMDS2_DATA1+. Multiplexed with DP2_LANE1- and TMDS2_DATA1-.	O PCIE		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+ and TMDS2_DATA0+. Multiplexed with DP2_LANE2- and TMDS2_DATA0-.	O PCIE		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+ and TMDS2_CLK+. Multiplexed with DP2_LANE3- and TMDS2_CLK-.	O PCIE		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD.	I 3.3V	PD 100k	

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+ and HDMI2_CTRLCLK. DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PD100k @ DP mode, PU 3.3k 3.3V @ HDMI/DVI mode	
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3V	PU 100k 3.3V@ DP mode, PU PU 3.3k 3.3V @ HDMI/DVI mode	
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_ AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+. Multiplexed with DP3_LANE0- and TMDS3_DATA2-.	O PCIE		Not connected
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+. Multiplexed with DP3_LANE1- and TMDS3_DATA1-.	O PCIE		Not connected
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+. Multiplexed with DP3_LANE2- and TMDS3_DATA0-.	O PCIE		Not connected
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+. Multiplexed with DP3_LANE3- and TMDS3_CLK-.	O PCIE		Not connected
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD.	I 3.3V		Not connected
DDI3_CTRLCLK_AUX+	C36	DP3_AUX+	I/O PCIE		Not connected
DDI3_CTRLDATA_AUX-	C37	DP3_AUX-	I/O PCIE		Not connected
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_ AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V		Not connected

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.5 of this user's guide.

Table 24 HDMI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS1_CLK + TMDS1_CLK -	D36 D37	HDMI/DVI TMDS Clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
TMDS1_DATA0+ TMDS1_DATA0-	D32 D33	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
TMDS1_DATA1+ TMDS1_DATA1-	D29 D30	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-..	O PCIE		
TMDS1_DATA2+ TMDS1_DATA2-	D26 D27	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
HDMI1_HPD	C24	HDMI/DVI Hot-plug detect. Multiplexed with DDI1_HPD.	I PCIE	PD 100k	
HDMI1_CTRLCLK	D15	HDMI/DVI I²C Control Clock Multiplexed with DDI1_CTRLCLK_AUX+	I/O OD 3.3V	PU 3.3k 3.3V	
HDMI1_CTRLDATA	D16	HDMI/DVI I²C Control Data Multiplexed with DDI1_CTRLDATA_AUX-	I/O OD 3.3V	PU 3.3k 3.3V	
TMDS2_CLK + TMDS2_CLK -	D49 D50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-.	O PCIE		
TMDS2_DATA0+ TMDS2_DATA0-	D46 D47	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-.	O PCIE		
TMDS2_DATA1+ TMDS2_DATA1-	D42 D43	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-.	O PCIE		
TMDS2_DATA2+ TMDS2_DATA2-	D39 D40	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-..	O PCIE		
HDMI2_HPD	D44	HDMI/DVI Hot-plug detect. Multiplexed with DDI2_HPD	I PCIE	PD 100k	
HDMI2_CTRLCLK	C32	HDMI/DVI I²C Control Clock Multiplexed with DDI2_CTRLCLK_AUX+	I/O OD 3.3V	PU 3.3k 3.3V	
HDM12_CTRLDATA	C33	HDMI/DVI I²C Control Data Multiplexed with DDI2_CTRLDATA_AUX-	I/O OD 3.3V	PU 3.3k 3.3V	
TMDS3_CLK + TMDS3_CLK -	C49 C50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		Not supported
TMDS3_DATA0+ TMDS3_DATA0-	C46 C47	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		Not supported
TMDS3_DATA1+ TMDS3_DATA1-	C42 C43	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-..	O PCIE		Not supported
TMDS3_DATA2+ TMDS3_DATA2-	C39 C40	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		Not supported

Signal	Pin #	Description	I/O	PU/PD	Comment
HDMI3_HPD	C44	HDMI/DVI Hot-plug detect. Multiplexed with DDI3_HPD.	I PCIE	PD100k	Not supported
HDMI3_CTRLCLK	C36	HDMI/DVI I²C Control Clock Multiplexed with DDI3_CTRLCLK_AUX+	I/O OD 3.3V	PD100k	Not supported
HDMI3_CTRLDATA	C37	HDMI/DVI I²C Control Data Multiplexed with DDI3_CTRLDATA_AUX-	I/O OD 3.3V	PU 100k	Not supported

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.5 of this user's guide.

Table 25 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE3+ DP1_LANE3-	D36 D37	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
DP1_LANE2+ DP1_LANE2-	D32 D33	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
DP1_LANE1+ DP1_LANE1-	D29 D30	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		
DP1_LANE0+ DP1_LANE0-	D26 D27	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
DP1_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI1_HPD.	I 3.3V	PD 1M	
DP1_AUX+	D15	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP1_AUX-	D16	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	
DP2_LANE3+ DP2_LANE3-	D49 D50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		
DP2_LANE2+ DP2_LANE2-	D46 D47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		
DP2_LANE1+ DP2_LANE1-	D42 D43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		
DP2_LANE0+ DP2_LANE0-	D39 D40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR0+ and DDI1_PAIR0-	O PCIE		
DP2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI2_HPD.	I 3.3V	PD 100k	

Signal	Pin #	Description	I/O	PU/PD	Comment
DP2_AUX+	C32	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP2_AUX-	C33	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	
DP3_LANE3+ DP3_LANE3-	C49 C50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		
DP3_LANE2+ DP3_LANE2-	C46 C47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		
DP3_LANE1+ DP3_LANE1-	C42 C43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-.	O PCIE		
DP3_LANE0+ DP3_LANE0-	C39 C40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		
DP3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI3_HPD.	I 3.3V	PD 100k	
DP3_AUX+	C36	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP3_AUX-	C37	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k	

Note

1. *Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.5 of this user's guide.*

2. *The third DP interface is available only if LVDS is not used.*

Table 26 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# / TYPE1# / TYPE0# / X / X / X / Pinout Type 1 NC / NC / NC / Pinout Type 2 NC / NC / GND / Pinout Type 3 (no IDE) NC / GND / NC / Pinout Type 4 (no PCI) NC / GND / GND / Pinout Type 5 (no IDE, no PCI) GND / NC / NC / Pinout Type 6 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.	PDS	TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard. The conga-TCA5 is based on the COM Express Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.
TYPE10#	A97	Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed. TYPE10# NC – Pinout R2.0 PD – Pinout Type 10 pull down to ground with 4.7k resistor 12V – Pinout R1.0 This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7k resistor.	PDS	Not connected to indicate "Pinout R2.0".

Table 27 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

8.4 C-D Connector Pinout

Table 28 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1- *1	D56	PEG_TX1- *1
C2	GND	D2	GND	C57	TYPE1# *1	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+ *1	D58	PEG_TX2+ *1
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2- *1	D59	PEG_TX2- *1
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PEG_RX3+ *1	D61	PEG_TX3+ *1
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PEG_RX3- *1	D62	PEG_TX3- *1
C8	GND	D8	GND	C63	RSVD	D63	RSVD
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	RSVD	D64	RSVD
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	PEG_RX4+ *1	D65	PEG_TX4+ *1
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4- *1	D66	PEG_TX4- *1
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RSVD	D67	GND
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	PEG_RX5+ *1	D68	PEG_TX5+ *1
C14	GND	D14	GND	C69	PEG_RX5- *1	D69	PEG_TX5- *1
C15	DDI1_PAIR6+ *1	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	DDI1_PAIR6- *1	D16	DDI1_CTRLDATA_AUX-	C71	PEG_RX6+ *1	D71	PEG_TX6+ *1
C17	RSVD	D17	RSVD	C72	PEG_RX6- *1	D72	PEG_TX6- *1
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	PCIE_RX6+ *1	D19	PCIE_TX6+ *1	C74	PEG_RX7+ *1	D74	PEG_TX7+ *1
C20	PCIE_RX6- *1	D20	PCIE_TX6- *1	C75	PEG_RX7- *1	D75	PEG_TX7- *1
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+ *1	D22	PCIE_TX7+ *1	C77	RSVD	D77	RSVD
C23	PCIE_RX7- *1	D23	PCIE_TX7- *1	C78	PEG_RX8+ *1	D78	PEG_TX8+ *1
C24	DDI1_HPD	D24	RSVD	C79	PEG_RX8- *1	D79	PEG_TX8- *1
C25	DDI1_PAIR4+ *1	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	DDI1_PAIR4- *1	D26	DDI1_PAIR0+	C81	PEG_RX9+ *1	D81	PEG_TX9+ *1
C27	RSVD	D27	DDI1_PAIR0-	C82	PEG_RX9- *1	D82	PEG_TX9- *1
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD
C29	DDI1_PAIR5+ *1	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	DDI1_PAIR5- *1	D30	DDI1_PAIR1-	C85	PEG_RX10+ *1	D85	PEG_TX10+ *1

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- *1	D86	PEG_TX10- *1
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-	C88	PEG_RX11+ *1	D88	PEG_TX11+ *1
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11- *1	D89	PEG_TX11- *1
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+ *1	D36	DDI1_PAIR3+	C91	PEG_RX12+ *1	D91	PEG_TX12+ *1
C37	DDI3_CTRLDATA_AUX- *1	D37	DDI1_PAIR3-	C92	PEG_RX12- *1	D92	PEG_TX12- *1
C38	DDI3_DDC_AUX_SEL *1	D38	RSVD	C93	GND	D93	GND
C39	DDI3_PAIR0+ *1	D39	DDI2_PAIR0+	C94	PEG_RX13+ *1	D94	PEG_TX13+ *1
C40	DDI3_PAIR0- *1	D40	DDI2_PAIR0-	C95	PEG_RX13- *1	D95	PEG_TX13- *1
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+ *1	D42	DDI2_PAIR1+	C97	RVSD	D97	RSVD
C43	DDI3_PAIR1- *1	D43	DDI2_PAIR1-	C98	PEG_RX14+ *1	D98	PEG_TX14+ *1
C44	DDI3_HPD *1	D44	DDI2_HPD	C99	PEG_RX14- *1	D99	PEG_TX14- *1
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+ *1	D46	DDI2_PAIR2+	C101	PEG_RX15+ *1	D101	PEG_TX15+ *1
C47	DDI3_PAIR2- *1	D47	DDI2_PAIR2-	C102	PEG_RX15- *1	D102	PEG_TX15- *1
C48	RSVD	D48	RSVD	C103	GND	D103	GND
C49	DDI3_PAIR3+ *1	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3- *1	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+ *1	D52	PEG_TX0+ *1	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0- *1	D53	PEG_TX0- *1	C108	VCC_12V	D108	VCC_12V
C54	TYPE0# *1	D54	PEG_LANE_RV# *1	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+ *1	D55	PEG_TX1+ *1	C110	GND (FIXED)	D110	GND (FIXED)

Note

*1 *Not supported on the conga-TCA5.*

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-TCA5 module is functionally identical with a standard PC/AT. The table below shows the most important addresses and the addresses that differ from the standard PC/AT configuration.

Table 8 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
03B0 - 03CF	32 bytes	No	Video system
0400 - 047F	128 bytes	No	Motherboard resources
0500 - 05FF	256 bytes	No	Motherboard resources
0680 - 069F	20 bytes	No	Motherboard resources
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
0D00 - F000		See note	PCI / PCI Express bus

Note

The BIOS assigns PCI and PCI Express I/O resources from F000h downwards. Devices that are not compliant to PnP, PCI or PCI Express must not use any I/O resource in this address range.

9.1.1 LPC Bus

On the conga-TCA5, the internal PCI bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI bus (only specified I/O ranges are forwarded to the LPC bus).

With the default settings in the congatec Embedded BIOS, the following I/O address ranges are forwarded to the LPC bus:

80h - 8Fh (via LPC Generic I/O Range 1)

A00h - A1Fh (via LPC Generic I/O Range 4)

The following I/O decode ranges are fixed to the LPC Bus:

2Eh - 2Fh
4Eh - 4Fh
200h - 20Fh
2F8h - 2FFh
3F8h - 3FFh
378h - 37Fh
778h - 77Fh
3F0h - 3F5h
3F7h, 60h, 62h, 64h, 66h

Parts of these ranges are not available if a Super I/O is used on the carrier board. If a Super I/O is not implemented on the carrier board, then all these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 9 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Device ID	Description and Device ID
00h	00h	00h	0x5AF0	Host Bridge
00h	02h	00h	0x5A84	Graphics and Display
00h	0Dh	00h	0x5A92	Primary to SideBand Bridge
00h	0Dh	01h	0x5A94	PMC (Power Management Controller)
00h	0Dh	02h	0x5A96	Fast SPI
00h	0Dh	03h	0x5AEC	Shared SRAM
00h	0Eh	00h	0x5A98	HDA
00h	0Fh	00h	0x5A9A	Simple Communication Controller 0
00h	0Fh	01h	0x5A9C	Simple Communication Controller 1
00h	0Fh	02h	0x5A9E	Simple Communication Controller 2
00h	012h	00h	0x5AE3	SATA
00h	013h	00h	0x5AD8	PCIe - A0
00h	013h	01h	0x5AD9	PCIe - A1 *1
00h	013h	02h	0x5ADA	PCIe - A2 *1
00h	013h	03h	0x5ADB	PCIe - A3 *1
00h	014h	00h	0x5AD6	PCIe -B0
00h	015h	00h	0x5AA8	USB-Host (xHCI)
00h	015h	01h	0x5AAA	USB-Host (xDCI)
00h	016h	00h	0x5AAC	I2C 0 *2

00h	016h	01h	0x5AAE	I2C 1 *2
00h	016h	02h	0x5AB0	I2C 2 *2
00h	016h	03h	0x5AB2	I2C 3 *2
00h	017h	00h	0x5AB4	I2C 4 *2
00h	017h	00h	0x5AB6	I2C 5 *2
00h	017h	00h	0x5AB8	I2C 6 *2
00h	017h	00h	0x5ABA	I2C 7 *2
00h	018h	00h	0x5ABC	SoC UART 0 *2
00h	018h	01h	0x5ABE	SoC UART 1 *2
00h	018h	02h	0x5AC0	SoC UART 2 *2
00h	018h	03h	0x5AEE	SoC UART 3 *2
00h	019h	00h	0x5AC2	SPI 0 *2
00h	019h	01h	0x5AC4	SPI 1 *2
00h	019h	02h	0x5AC6	SPI 2 *2
00h	01Bh	00h	0x5ACA	SD Card
00h	01Ch	01h	0x5ACC	eMMC
00h	01Fh	00h	0x5AE8	LPC Bus
00h	01Fh	01h	0x5AD4	SM Bus
02h	00h	00h	0x1539	Intel PCIe Ethernet Network on Module

Note

*1 *To view these ports, attach a device to the corresponding PCI Express port or set the PCI Express port in the BIOS setup menu to "Enabled".*

*2 *Disabled by default in the BIOS Setup menu.*

9.3 I²C Bus

No onboard resource is connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.4 SM Bus

The System Management (SM) bus signals are connected to the Intel Apollo Lake SoC and is not intended to be used by off-board non-system management devices. For more information about this subject, contact congatec technical support.

9.5 congatec System Sensors

The conga-TCA5 offers the following sensors and monitors:

- temperature sensors
  - CPU temperature based on CPU Digital Thermal Sensor
  - Board temperature sensor located on the Board Controller
- voltage sensors
  - 5V standard voltage sensor
  - 5V standby voltage sensor
- current sensor
- fan monitor

The sensors and monitors are accessible through CGOS interface, and also visible on the "Health Monitor"submenu in the BIOS Setup:

10 BIOS Setup Description

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-TCA5 is identified as TCA50R1xx, where:

- R is the identifier for a BIOS ROM file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The TCA50 binary size is 8 MB.

10.3 Updating the BIOS

OEMs often use BIOS updates to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS. The conga-TCA5 uses a congatec/AMI AptioEFI firmware, which is stored in an onboard flash ROM chip and can be updated using the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line, Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

10.4 Supported Flash Devices

The conga-TCA5 supports the following flash devices:

- Winbond W25Q64CVSSIG (8 MB)
- Macronix MX25U6473FM2I-10G (8 MB)
- GigaDevice GD25LB64CSIG (8 MB)

The flash devices listed above can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.

11 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.3	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0	http://www.serialata.org
PICMG® COM Express Module™ Base Specification	http://www.picmg.org/
PCI Express Base Specification, Revision 1.0a	http://www.pcisig.com/specifications