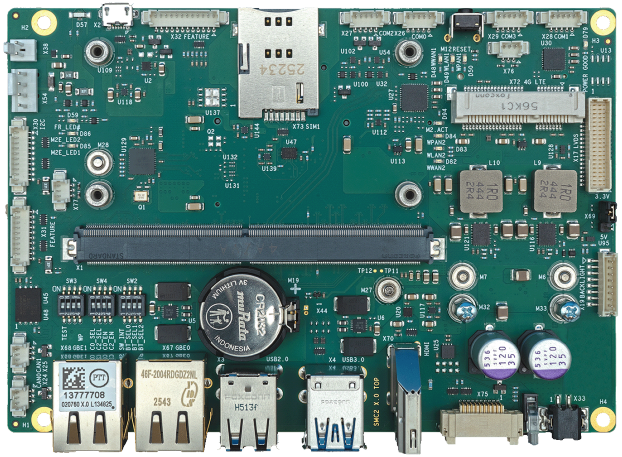

conga-SMC2/Edge-ARM

Detailed description of the congatec SMARC 3.5“ application carrier board

User’s Guide

Revision 0.01 (Preliminary)

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.01	2026-03-27	BEU	• Preliminary release

Preface

This user's guide provides information about the components, features and connectors available on the conga-SMC2/Edge-ARM carrier board.

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Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Connector Type

Describes the connector on the congatec SMARC 3.5" carrier board.

Link to connector layout diagram

This link icon is located in the top left corner of each page. It provides a direct link to the connector layout diagram on page 11 of this document.

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Terminology

Term	Description
ARM	Advanced RISC Machines
CAN	Controller Area Network
cBC	congatec Board Controller
CSI	Camera Serial Interface
DP	DisplayPort
eDP	Embedded DisplayPort
eSPI	Enhanced Serial Peripheral Interface
GbE	Gigabit Ethernet
GHz	Gigahertz
GPIO	General Purpose Input Output
HDA	High Definition Audio
I²C Bus	Inter-Integrated Circuit Bus
kB	Kilobyte
kHz	Kilohertz
LVDS	Low Voltage Differential Signalling
MB	Megabyte
Mbit	Megabit
MHz	Megahertz
N.A.	Not available
N.C.	Not connected
OTG	On-The-Go
PCH	Platform Controller Hub
PCIe	PCI Express
SATA	Serial ATA
SDIO	Secure Digital Input Output
SMBus	System Management Bus
SPI	Serial Peripheral Interface
USB	Universal Serial Bus

Contents

List of Tables

1 Introduction

1.1 SMARC Concept

The Standardization Group for Embedded Technologies e.V (SGET) defined the SMARC standard for small form factor computer modules that target low power, low cost and high performance applications. The SMARC connector and interfaces are optimized for high-speed communication, and are suitable for ARM SoCs and low power x86 SoCs.

The SMARC standard bridges the gap between the COM Express standard and the Qseven standard by offering most of the interfaces defined in the COM Express specification at a lower power. With a footprint of 82 mm x 50 mm or 82 mm x 80 mm, the SMARC standard promotes the design of highly integrated, energy-efficient systems.

Due to its small size and lower power demands, PC appliance designers can design low cost devices as well as explore a huge variety of product development options—from compact space-saving designs to fully functional systems. This solution allows scalability, product diversification and faster time to market.

1.2 conga-SMC2/Edge-ARM

The conga-SMC2/Edge-ARM carrier board is designed for ARM modules based on the SMARC 2.1 Specification. With a footprint of 82 mm × 50 mm, the conga-SMC2/Edge-ARM provides most of the functional requirements for any SMARC application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, USB 3.0/2.0, and Gigabit Ethernet.

By combining the scalability of SMARC modules, the conga-SMC2/Edge-ARM carrier board provides manufacturers and developers with a platform to jump-start the development of ARM-based SMARC systems. This helps to reduce product design cycle and encourages rapid innovation in system design, to meet the ever-changing needs of the market.

The conga-SMC2/Edge-ARM is an ideal platform for developing ARM-based embedded systems because of the various features and capabilities it offers.

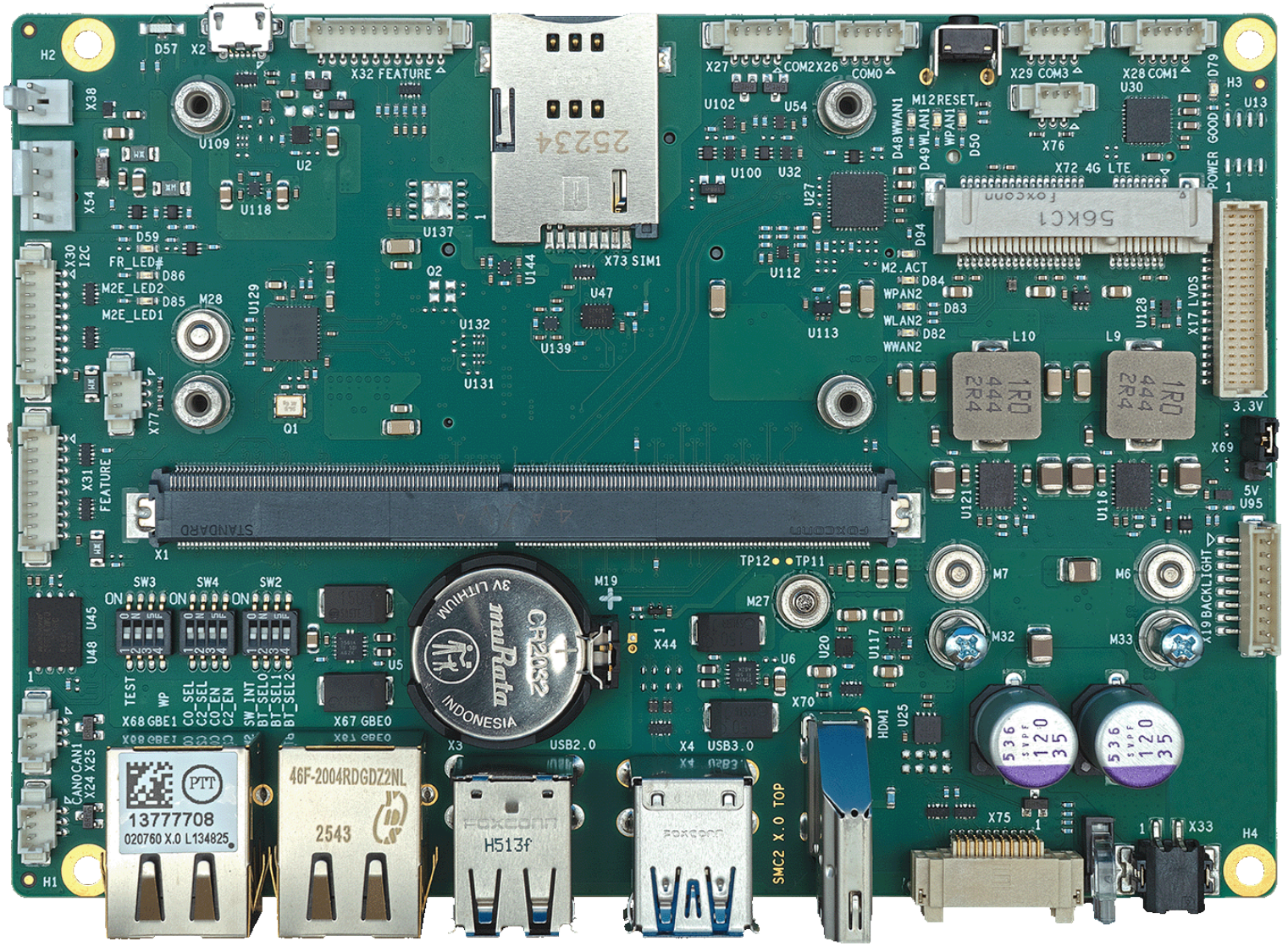
1.2.1 Order Number

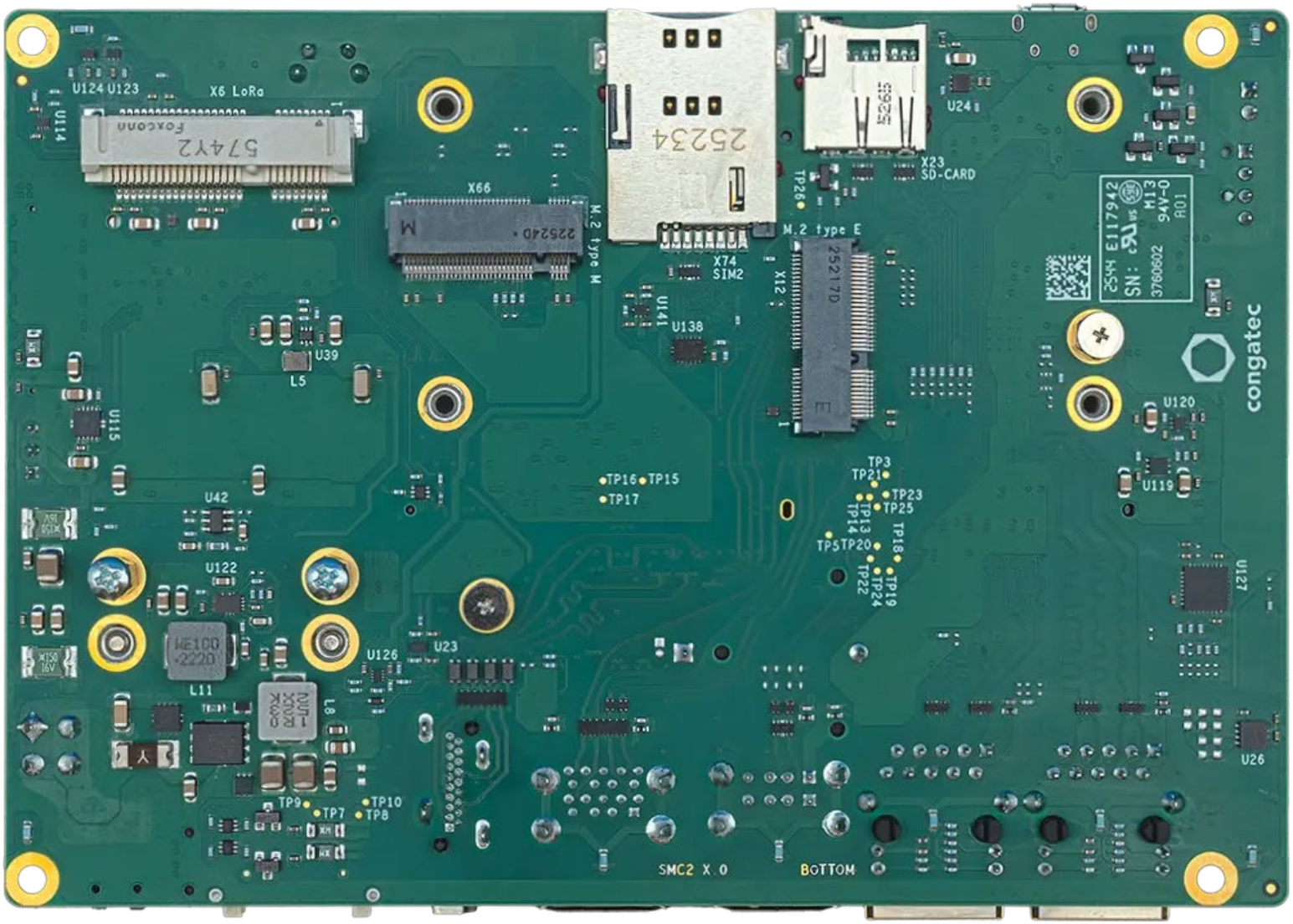
Table 1 Order Description

Part Number	Product Name	Description
020760	conga-SMC2/Edge-ARM	3.5" carrier board for SMARC-based ARM modules

2 Board Overview

The connector layout picture shows each connector and its name designator. Jumpers and their respective pins are also shown. Select the Adobe 'Zoom-In-Tool' and zoom in on a given component to see its designator.





3 Specifications

3.1 Feature List

Table 2 Feature Summary

Form factor	3.5" Application Carrier Board	
Board Variant	Support for SMARC modules on ARM	
Internal Connectors and Features	1x LVDS 18/24bit single/dual channel LVDS 1x Backlight power via pin header for LVDS 1x M.2 Key E 2230 (PCIe, USB 2.0) 1x M.2 Key M 2242 (PCIe) (optional) 2x miniPCIe connector (USB only) 2x SIM sockets 1x eSIM (optional) 1x CAN (plus second CAN1 as option) 2x RS-232/422/485 on pin header (optional)	2x RS-232 on pin header (optional) 1x Feature connector (Power, Reset, Sleep, LID) 1x Feature connector (Charger, Batlow, WD) (optional) 1x I^2C GP and I^2C PM (optional) 1x RTC battery holder (CR2032) 1x FAN header (optional) 2x Dual Color LED 1x microSD slot (optional)
External Connectors	2x GbE RJ45 2x USB 2.0 2x USB 3.0 1x HDMI 1x External DC Input 1x Industrial I/O connector (CAN0, 1x RS-232, 1x RS-232/422/485, 8x GPIO) 1x SW Reset button 1x USB OTG	
Power Specification	DC In (12–24 V Wide Range Carrier Board Supply)	
Security	Trusted Platform Module (TPM 2.0)	
Temperature Range	Operating Temp.: -40°C … +85°C Storage Temp.: -40°C … +85°C	
Humidity	Operating Hum.: 10% - 85% r. H. non cond. Storage Hum.: 5% - 85% r. H. non cond.	
Size	approx. 146 mm × 102 mm	
Order Information	PN 020760 conga-SMC2/Edge-ARM	

Note

1. *The module must also support the features for them to function. Refer to the module's user's guide for information about supported features.*

2. *The carrier board is designed for cooling solutions with bore-hole standoffs.*

3.2 Mechanical Dimensions

The conga-SMC2/Edge-ARM has the following dimensions:

- length of 146 ± 0.1 mm
- width of 102 ± 0.1 mm

Note

3D models of congatec products are available at www.congatec.com/login. These models indicate the overall length, height and width of each product. If you need login access, contact your local sales representative.

3.3 Environmental Specifications

Temperature	Operation: -40°C to +85°C	Storage: -40° to +85°C
Relative Humidity	Operation: 10% to 85%	Storage: 5% to 85%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heat spreader, the maximum operating temperature refers to any measurable spot on the heat spreader's surface.

Humidity specifications are for non-condensing conditions.

Note

For long term storage of the conga-SMC2/Edge-ARM (more than six months), keep the conga-SMC2/Edge-ARM in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

We do not recommend storing the conga-SMC2/Edge-ARM for more than five years under these conditions.

4 Connector Description

Table 3 SMARC Edge Finger Connector Pinout

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
		S1	N.C.
P1	SMB_ALERT#_1V8	S2	N.C.
P2	GND	S3	GND
P3	N.C.	S4	N.C.
P4	N.C.	S5	N.C.
P5	GBE1_SDP	S6	N.C.
P6	GBE0_SDP	S7	N.C.
P7	N.C.	S8	N.C.
P8	N.C.	S9	N.C.
P9	GND	S10	GND
P10	N.C.	S11	N.C.
P11	N.C.	S12	N.C.
P12	GND	S13	GND
P13	N.C.	S14	N.C.
P14	N.C.	S15	N.C.
P15	GND	S16	GND
P16	N.C.	S17	GBE1_MDI0+
P17	N.C.	S18	GBE1_MDI0-
P18	GND	S19	GBE1_LINK100#
P19	GBE0_MDI3-	S20	GBE1_MDI1+
P20	GBE0_MDI3+	S21	GBE1_MDI1-
P21	GBE0_LINK100#	S22	GBE1_LINK1000#
P22	GBE0_LINK1000#	S23	GBE1_MDI2+
P23	GBE0_MDI2-	S24	GBE1_MDI2-
P24	GBE0_MDI2+	S25	GND
P25	GBE0_LINK_ACT#	S26	GBE1_MDI3+
P26	GBE0_MDI1-	S27	GBE1_MDI3-
P27	GBE0_MDI1+	S28	GBE1_CTREF
P28	GBE0_CTREF	S29	N.C.

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P29	GBE0_MDI0-	S30	N.C.
P30	GBE0_MDI0+	S31	GBE1_LINK_ACT#
P31	SPI0_CS1#	S32	N.C.
P32	GND	S33	N.C.
P33	SDIO_WP	S34	GND
P34	SDIO_CMD	S35	USB4+
P35	SDIO_CD#	S36	USB4-
P36	SDIO_CLK	S37	N.C.
P37	SDIO_PWREN	S38	N.C.
P38	GND	S39	N.C.
P39	SDIO_D0	S40	N.C.
P40	SDIO_D1	S41	N.C.
P41	SDIO_D2	S42	N.C.
P42	SDIO_D3	S43	N.C.
P43	SPI0_CS0#	S44	N.C.
P44	SPI0_CLK	S45	N.C.
P45	SPI0_DIN	S46	N.C.
P46	SPI0_DOUT	S47	GND
P47	GND	S48	I2C_CLK
P48	N.C.	S49	I2C_DAT
P49	N.C.	S50	N.C.
P50	GND	S51	N.C.
P51	N.C.	S52	N.C.
P52	N.C.	S53	N.C.
P53	GND	S54	N.C.
P54	ESPI_CS0#	S55	USB5_EN_OC#
P55	ESPI_CS1#	S56	ESPI_IO2
P56	ESPI_CLK	S57	ESPI_IO3
P57	ESPI_IO1	S58	ESPI_RESET#
P58	ESPI_IO0	S59	USB5+
P59	GND	S60	USB5-
P60	USB0+	S61	GND
P61	USB0-	S62	USB3_SSTX+

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P62	USB0_EN_OC#	S63	USB3_SSTX-
P63	USB0_VBUS_DET	S64	GND
P64	USB0_OTG_ID	S65	USB3_SSRX+
P65	USB1+	S66	USB3_SSRX-
P66	USB1-	S67	GND
P67	USB1_EN_OC#	S68	USB3+
P68	GND	S69	USB3-
P69	USB2+	S70	GND
P70	USB2-	S71	USB2_SSTX+
P71	USB2_EN_OC#	S72	USB2_SSTX-
P72	N.C.	S73	GND
P73	N.C.	S74	USB2_SSRX+
P74	USB3_EN_OC#	S75	USB2_SSRX-
	Key		Key
P75	PCIE_A_RST#	S76	PCIE_B_RST#
P76	USB4_EN_OC#	S77	N.C.
P77	PCIE_B_CLKREQ#	S78	N.C.
P78	PCIE_A_CLKREQ#	S79	N.C.
P79	GND	S80	GND
P80	N.C.	S81	N.C.
P81	N.C.	S82	N.C.
P82	GND	S83	GND
P83	PCIE_A_CLK+	S84	PCIE_B_CLK+
P84	PCIE_A_CLK-	S85	PCIE_B_CLK-
P85	GND	S86	GND
P86	PCIE_A_RX+	S87	PCIE_B_RX+
P87	PCIE_A_RX-	S88	PCIE_B_RX-
P88	GND	S89	GND
P89	PCIE_A_TX+	S90	PCIE_B_TX+
P90	PCIE_A_TX-	S91	PCIE_B_TX-
P91	GND	S92	GND

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P92	HDMI0_D2+	S93	N.C.
P93	HDMI0_D2-	S94	N.C.
P94	GND	S95	N.C.
P95	HDMI0_D1+	S96	N.C.
P96	HDMI0_D1-	S97	N.C.
P97	GND	S98	N.C.
P98	HDMI0_D0+	S99	N.C.
P99	HDMI0_D0-	S100	N.C.
P100	GND	S101	GND
P101	HDMI0_CLK+	S102	N.C.
P102	HDMI0_CLK-	S103	N.C.
P103	GND	S104	USB3_OTG_ID
P104	HDMI0_HPD	S105	N.C.
P105	HDMI0_DDC_CLK	S106	N.C.
P106	HDMI0_DDC_DAT	S107	LCD1_BKLTEN
P107	DP1_AUX_SEL	S108	LVDS1_CLK+
P108	GPIO0/CAM0_PWR#	S109	LVDS1_CLK-
P109	GPIO1/CAM1_PWR#	S110	GND
P110	GPIO2/CAM0_RST#	S111	LVDS1_D0+
P111	GPIO3/CAM1_RST#	S112	LVDS1_D0-
P112	GPIO4/HDA_RST#	S113	N.C.
P113	GPIO5/PWMO	S114	LVDS1_D1+
P114	GPIO6/TACHIN	S115	LVDS1_D1-
P115	GPIO7	S116	LCD1_VDD_EN
P116	GPIO8	S117	LVDS1_D2+
P117	GPIO9	S118	LVDS1_D2-
P118	GPIO10	S119	GND
P119	GPIO11	S120	LVDS1_D3+
P120	GND	S121	LVDS1_D3-
P121	PM_I2C_CLK	S122	LCD1_BKLT_PWM
P122	PM_I2C_DAT	S123	GPIO13
P123	BOOT_SEL0#	S124	GND
P124	BOOT_SEL1#	S125	LVDS0_D0+

P-PIN	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P125	BOOT_SEL2#	S126	LVDS0_D0-
P126	RESET_OUT#	S127	LCD0_BKLTEN
P127	RESET_BTN#	S128	LVDS0_D1+
P128	PWRBTN#	S129	LVDS0_D1-
P129	SER0_TX	S130	GND
P130	SER0_RX	S131	LVDS0_D2+
P131	SER0_RTS	S132	LVDS0_D2-
P132	SER0_CTS	S133	LCD0_VDD_EN
P133	GND	S134	LVDS0_CLK+
P134	SER1_TX	S135	LVDS0_CLK-
P135	SER1_RX	S136	GND
P136	SER2_TX	S137	LVDS0_D3+
P137	SER2_RX	S138	LVDS0_D3-
P138	SER2_RTS	S139	LVDS_DDC_CLK
P139	SER2_CTS	S140	LVDS_DDC_DAT
P140	SER3_TX	S141	LCD0_BKLT_PWM
P141	SER3_RX	S142	GPIO12
P142	GND	S143	GND
P143	CAN0_TX	S144	N.C.
P144	CAN0_RX	S145	WDT_OUT#
P145	CAN1_TX	S146	PCIE_WAKE#
P146	CAN1_RX	S147	+V3_RTC
P147	+V5A	S148	LID_BTN#
P148	+V5A	S149	SLP_BTN#
P149	+V5A	S150	VIN_PWRBAD#
P150	+V5A	S151	CHARGING#
P151	+V5A	S152	CHARGER_PRSNT#
P152	+V5A	S153	CARRIER_STBY#
P153	+V5A	S154	CARRIER_PWRON
P154	+V5A	S155	FORCE_RECOV#
P155	+V5A	S156	BATLOW#
P156	+V5A	S157	TEST#
		S158	GND

4.1 Power

This section describes the power input requirements, power connector, power status LED, and the CMOS battery connector.

4.1.1 Power Input Specification

The conga-SMC2/Edge-ARM requires a DC power supply that meets the specifications shown below.

Table 4 Power Input Specification

Parameter	Specification	Onboard Protection
Input Voltage	12 V – 24 V DC ±5 %	Reverse voltage protection
Maximum Current	Up to 8 A	15 A non-resettable fuse

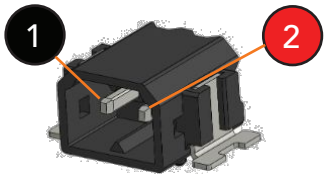
4.1.2 Power Input Connector (X33)

X33 connector provides the system power input.

Table 5 X33

Pin	Description
1	GND
2	+12–24 V ± 5 %

X33



Connector Type

X33: Phoenix PTSM, 2-pin, 2.50 mm pitch

4.1.3 System States LED (D57)

D57 bicolor LED indicates the system states.

Table 6 D57

LED	LED Status	ACPI State	Description
D57	Green - On	S0	System is powered on and running
	Red - On	Pseudo G3	Deep sleep with minimum power consumption
	Green - Blinking	S3-S5	Standby or suspend to RAM / disk

4.1.4 Power Fail LED (D79)

D79 LED indicates a problem with the power supply.

Table 7 D79

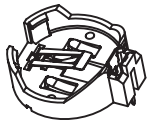
LED	LED Status	Description
D79	Red - On	Power supply issue detected

4.1.5 RTC/CMOS Battery Holder (M19)

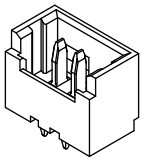
M19 battery holder supports a CR2032 coin-cell battery to maintain the real-time clock (RTC) and CMOS settings.

Optional X44 header supports an external RTC/CMOS battery.

M19



X44



Warning

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Connector Type

M19: CR2032 battery holder

X44: Optional PicoBlade header, 2-pin, 1.25 mm pitch (Molex 53047-0210); mating connector: Molex 51021-0200

4.2 Display Interfaces

This section describes the display interfaces.

4.3 LVDS

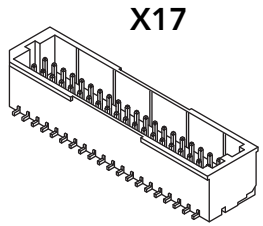
This section describes the LVDS interface.

4.3.1 LVDS Header (X17)

X17 header supports a dual-channel LVDS panel.

Table 8 X17

Pin	Signal	Pin	Signal
1	VCC (fused, 1.5 A)	2	VCC (fused, 1.5 A)
3	VCC (fused, 1.5 A)	4	VCC (fused, 1.5 A)
5	VCC_EDID (3.3 V; fused, 0.5 A)	6	GND
7	I2C_LCD_CK (EDID_CLK)	8	I2C_LCD_DAT (EDID_DATA)
9	N.C.	10	LCD0_VDD_EN (enable for external VCC source; 3.3 V or 5 V level output via jumper X69)
11	GND	12	GND
13	LVDS0_0-	14	LVDS0_1-
15	LVDS0_0+	16	LVDS0_1+
17	GND	18	GND
19	LVDS0_2-	20	LVDS0_CK-
21	LVDS0_2+	22	LVDS0_CK+
23	GND	24	GND
25	LVDS0_3-	26	LVDS1_0-
27	LVDS0_3+	28	LVDS1_0+
29	GND	30	GND
31	LVDS1_1-	32	LVDS1_2-
33	LVDS1_1+	34	LVDS1_2+
35	GND	36	GND
37	LVDS1_CK-	38	LVDS1_3-
39	LVDS1_CK+	40	LVDS1_3+



Note

LVDS0 is the primary (ODD) LVDS channel and LVDS1 is the secondary (EVEN) LVDS channel.

Connector Type

X17: Header, 40-pin, 1 mm pitch (JST BM40B-SRDS-G-TF); mating connector: JST SHDR-40V-S-B

4.3.1.1 LCD Control Voltage Selection (X69)

X69 jumper selects the LCD control signal voltage level used by the LVDS interface.

Table 9 X69

Jumper	LCD Control Voltage
1-2	5 V
2-3	3.3 V (default)

This voltage level affects signals such as LCD0_VDD_EN, LVDS_BKLT_EN, and LVDS_BKLT_CTRL.

Connector Type

X69: 2.54 mm jumper

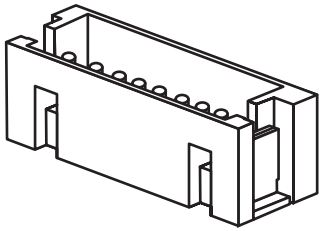
4.3.2 Backlight Power Header (X19)

X19 header supports LCD backlight inverters.

Table 10 X19

Pin	Signal	Description
1	12 V	Backlight inverter power (resettable fuse, 1.5 A hold @ 25°C)
2	12 V	Backlight inverter power (resettable fuse, 1.5 A hold @ 25°C)
3	GND	Ground
4	GND	Ground
5	LVDS_BKLT_EN	Backlight enable (3.3 V or 5 V level output via jumper X69)
6	LVDS_BKLT_CTRL	Backlight control (3.3 V or 5 V level output via jumper X69)
7	5 V	Backlight inverter power (resettable fuse, 1.5 A hold @ 25°C)
8	5 V	Backlight inverter power (resettable fuse, 1.5 A hold @ 25°C)

X19



Connector Type

X19: 2 mm, 8-pin crimp style connector (JST B8B-ZR-SM4-TF)

4.4 HDMI Port (X70)

X70 port supports HDMI® when the attached module provides **native HDMI®** signals.

Connector Type

X70: HDMI® port

4.5 microSD Card Slot (X23, optional)

Optional X23 slot supports microSD cards.

Connector Type

X23: Optional microSD card slot

4.5.1 microSD Card Slot Write Protection Selection (SW3.4)

SW3.4 DIP switch controls write protection of the SD card slot X23.

Table 11 SW3.4

Switch	Configuration	Description
SW3.4	OFF	SD card write protection **enabled**
	ON	SD card write protection **disabled** (default)

4.6 TPM 2.0 (U127)

The onboard OPTIGA™ TPM SLB 9672 FW16 (U127) provides TPM 2.0 support via SPI0.

4.7 I²C / SMBus (X30, optional)

Optional X30 header supports I²C and SMBus signals.

X30

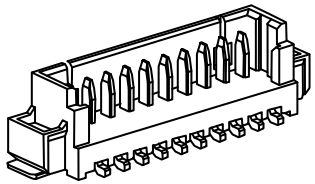


Table 12 X30

Pin	Signal	Description
1	N.C.	Not connected
2	I2C_GP_DAT	General-purpose I²C data
3	GND	Ground
4	I2C_GP_CK	General-purpose I²C clock output
5	1.8 V	Runtime power output (resettable fuse, 500 mA)
6	SMB_ALERT_1V8#	SMBus alert signal from external device (open-drain output required)
7	I2C_PM_DAT/SMB_DAT	Power management I²C data or SMBus data (x86 variant)
8	GND	Ground
9	I2C_PM_CK/SMB_CLK	Power management I²C clock output or SMBus clock output (x86 variant)
10	1.8 V	Standby power output (resettable fuse, 500 mA)

Note

All signal lines operate at 1.8 V logic level.

Connector Type

X30: Optional PicoBlade header, 10-pin, 1.25 mm pitch (Molex 053398-1071); mating connector: Molex 051021-1000

4.8 Serial Ports

This section describes the serial interfaces.

4.8.1 COM 0 / 2 Header (X26 / X27, optional)

Optional X26 header supports COM port 0.

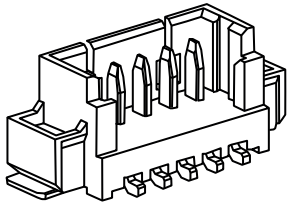
Optional X27 header supports COM port 2.

Both ports support **RS-232 or RS-422/RS-485 voltage levels**.

Table 13 X26, X27

Pin	RS232	RS422/RS485	Description
1	GND	GND	Ground
2	TXD	TX-	Transmit Data/Transmit Data -
3	RTS#	TX+	Request to Send/Transmit Data +
4	CTS#	RX+	Clear to Send/Receive Data +
5	RXD	RX-	Receive Data/Receive Data -

X26/X27



Note

1. *If termination is required, use a cable adapter or external circuitry with integrated 120 Ω bus termination.*
2. *RS-485 mode supports TX output control and RX echo cancellation if the attached module provides an active-low RTS# signal.*
3. *For 2-wire RS-485 operation, connect pin 2 to pin 5 and pin 3 to pin 4 externally.*
4. *The SMARC SER2 signals are routed to COM port 2 (X27) and the M.2 Key E card (X12).*

Connector Type

X26, X27: Optional PicoBlade header, 5-pin, 1.25 mm pitch (Molex 053398-0571); mating connector: Molex 051021-0500

4.8.1.1 Serial Communication Standard Selection (SW4)

SW4 DIP switch selects the serial communication standard for COM port 0 and COM port 2.

Table 14 SW4

Switch	Configuration	Description
SW4.1	OFF	COM 0 RS-422/RS-485 standard
	ON	COM 0 RS-232 standard (default)
SW4.2	OFF	COM 2 RS-422/RS485 standard
	ON	COM 2 RS-232 standard (default)
SW4.3	OFF	COM 0 RS-485 standard with echo cancellation
	ON	COM 0 RS-422 standard (default)
SW4.4	OFF	COM 2 RS-485 standard with echo cancellation
	ON	COM 2 RS-422 standard (default)

4.8.2 COM 1 / 3 Header (X28 / X29, optional)

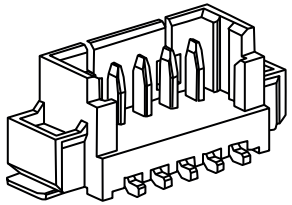
Optional X28 header supports COM port 1. Optional X29 header supports COM port 3.

Both ports support **RS-232 voltage levels only** and **do not provide hardware flow control**.

Table 15 X28, X29

Pin	Signal	Description
1	GND	Ground
2	TXD	Transmit data
3	N.C.	Not connected
4	N.C.	Not connected
5	RXD	Receive data

X28/X29



Connector Type

X28, X29: Optional PicoBlade header, 5-pin, 1.25 mm pitch (Molex 053398-0571); mating connector: Molex 051021-0500

4.9 CAN

This section describes the CAN interfaces.

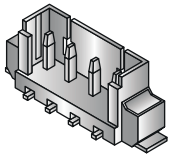
4.9.1 CAN Bus 0 Header (X24)

X24 header supports CAN bus 0.

Table 16 X24

X24 - CAN 0	
Pin	Signal
1	CAN0_H
2	CAN0_L
3	GND

X24/X25



Note

The CAN bus does **not include onboard 120 Ω** termination resistors. If termination is required, use a cable adapter or external circuitry with integrated **120 Ω bus termination**.

Connector Type

X24: PicoBlade header, 3-pin, 1.25 mm pitch; mating connector: Molex 051021-0300

4.9.2 CAN Bus 1 Header (X25, optional)

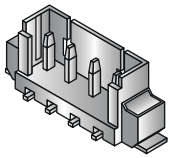
Optional X25 header supports CAN bus 1.

Table 17 X25

X25 - CAN 1

Pin	Signal
1	CAN1_H
2	CAN1_L
3	GND

X24/X25



Note

The CAN bus does **not include onboard 120 Ω** termination resistors. If termination is required, use a cable adapter or external circuitry with integrated **120 Ω bus termination**.

Connector Type

X25: Optional PicoBlade header, 3-pin, 1.25 mm pitch; mating connector: Molex 051021-0300

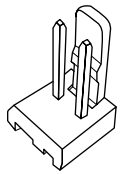
4.9.3 Auxiliary Power Header (X38, optional)

Optional X38 header supports auxiliary power for external CAN devices or a fan.

Table 18 X38

Pin	Signal
1	GND
2	+12 VDC (fused, 500 mA)

X38



Connector Type

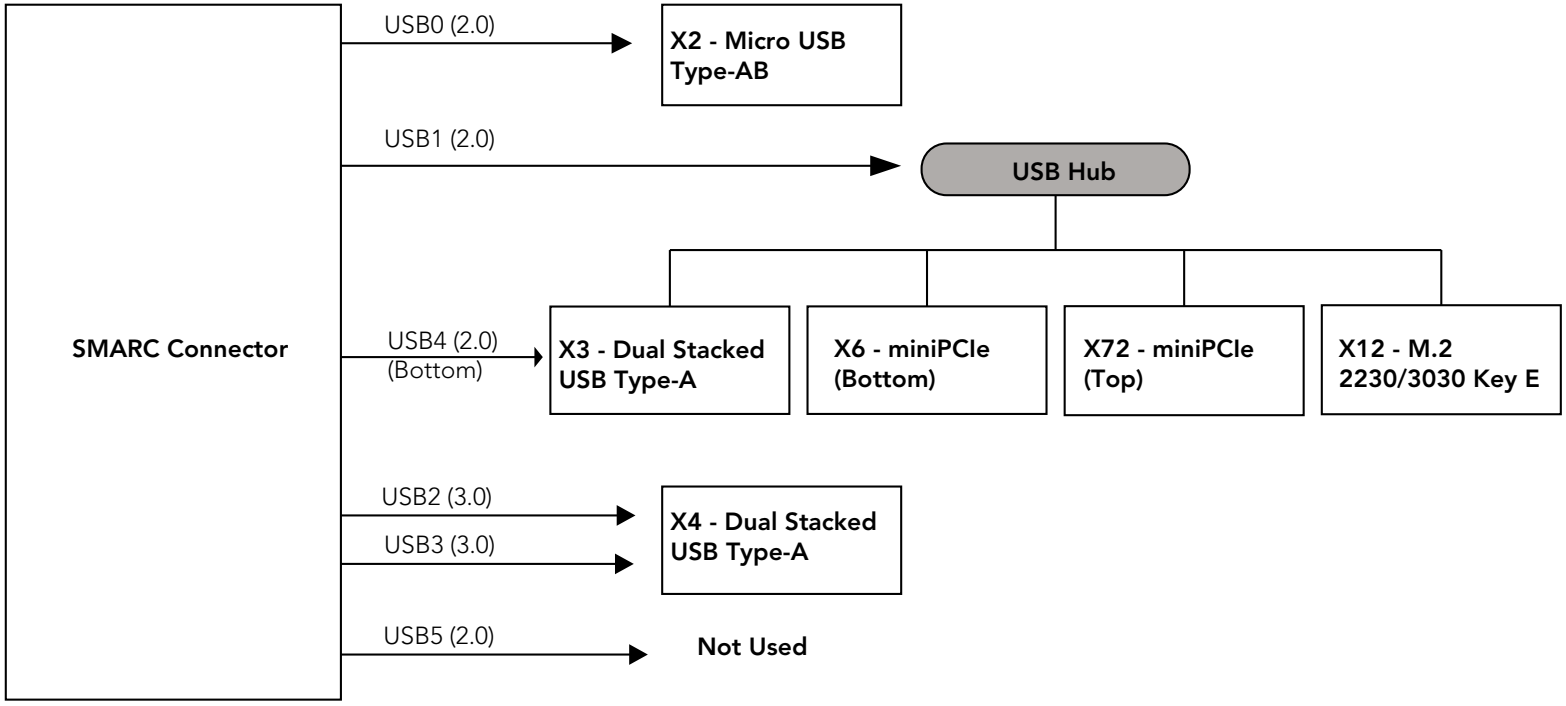
X38: Header, 2-pin, 2.54 mm pitch (Molex 2227-2021); mating connector: Molex 2695

4.10 USB

Following USB ports are provided:

- Micro USB Type-AB (X2)
- Dual-stacked USB 2.0 Type-A (X3)
- Dual-stacked USB 3.0 Type-A (X4)

The USB signals are routed to the following interfaces.



4.10.1 Micro USB Port (X2)

X2 connector supports micro USB Type-AB devices with USB On-The Go (OTG) capability.

Connector Type

X2: Micro USB Type-AB port

4.10.2 USB 2.0 Dual-Stacked Ports (X3)

X3 connector supports two USB 2.0 devices:

- The bottom port is connected directly to the SMARC USB4 interface.
- The top port is connected to the SMARC USB1 interface through an onboard USB hub.

Each port supports up to **500 mA** output current.

Connector Type

X3: Dual-stacked USB Type-A ports

4.10.3 USB 3.0 Dual-Stacked Ports (X4)

X4 connector supports two USB 3.0 devices.

Each port supports up to **1 A** output current.

Connector Type

X4: USB Type-A ports

4.11 PCIe

This section describes the miniPCIe card sockets and the wireless disable header available on the conga-SMC2/Edge-ARM.

4.11.1 miniPCIe Card Socket (X6)

X6 socket, located on the **bottom side** of the board, supports **full-size** miniPCIe cards.

Only USB 2.0 signals are available on this connector.

Table 19 D48, D49, D50

LED	LED Status	Description
D48	Yellow - Blinking	WWAN activity
D49	Yellow - Blinking	WLAN activity
D50	Yellow - Blinking	WPAN activity

Connector Type

X6: miniPCIe card socket

4.11.2 miniPCIe Card Socket (X72)

X72 socket, located on the **top side** of the board, supports **full-size** miniPCIe cards.

Only USB 2.0 signals are available on this connector.

Table 20 D82, D83, D84

LED	LED Status	Description
D82	Yellow - Blinking	WWAN activity
D83	Yellow - Blinking	WLAN activity
D84	Yellow - Blinking	WPAN activity

Connector Type

X72: miniPCIe card socket

4.11.3 miniPCIe Wireless Disable (X76)

X76 header provides wireless disable signals for both miniPCIe card sockets.

Table 21 X76

Pin	Signal	Description
1	MPCIE1_WDIS#	Connected to miniPCIe card socket X6 (bottom side)
2	GND	Ground
3	MPCIE2_WDIS#	Connected to miniPCIe card socket X72 (top side)

Connector Type

X76: PicoBlade header, 3-pin, 1.25 mm pitch

4.12 SIM

This section describes the two SIM card slots and optional eSIM connected to the **UIM interface of miniPCIe card socket X72**.

4.12.1 SIM Interface Selection

Only **one SIM interface can be active at a time**. GPIO 8 and GPIO 9 select the active SIM interface.

Table 22 Active SIM Interface Selection

GPIO 8	GPIO 9	Active Interface
0	X	SIM Card Slot X73 (top side)
1	0	SIM Card Slot X74 (bottom side)
1	1	eSIM (optional)

Note

On the conga-SMX8-Plus module, GPIO 8 and GPIO 9 must be configured as outputs. In the default software configuration, these GPIOs are configured as inputs with internal pull-up resistors.

4.12.2 SIM Card Slot (X73)

X73 slot, located on the **top side** of the board, supports SIM cards in 2FF format.

Connector Type

X73: SIM card slot

4.12.3 SIM Card Slot (X74)

X74 slot, located on the **bottom side** of the board, supports SIM cards in 2FF format.

Connector Type

X74: SIM card slot

4.12.4 eSIM (U137, optional)

Optional eSIM (U137, ST4SIM-111M) provides a SIM interface for cellular cards connected to miniPCIe card socket X72.

See section 4.12.1 "SIM Interface Selection" to select the active SIM interface.

4.13 M.2

This section describes the two optional M.2 card sockets.

4.13.1 M.2 2230/3030 Key E Card Socket (X12)

X12 socket supports M.2 2230/3030 Key E wireless cards.

The socket provides **USB 2.0** and **SMARC PCIe_A** signals.

Optionally, the socket can also provide SDIO, SER2, and I2C signals.

Table 23 D85, D88

LED	LED Status	Description
D85	Yellow - Blinking	WLAN activity
D88	Yellow - Blinking	BT activity

Connector Type

X12: Optional M.2 2230/3030 Key E card socket

4.13.1.1 M.2 2230/3030 Key E Card Wireless Disable Header (X77)

X77 header supports wireless disable signals for the M.2 2230/3030 Key E card socket X12.

Table 24 X77

Pin	Signal	Description
1	W_DISABLE1#	Disable WLAN (pull-up should be on module)
2	GND	Ground
3	W_DISABLE2#	Disable BT (pull-up should be on module)

Connector Type

X77: PicoBlade header, 3-pin, 1.25 mm pitch

4.13.2 M.2 2242 Key M Card Socket (X66, optional)

Optional X66 socket supports M.2 2242 Key M mass storage cards when the attached module provides **SMARC PCIe_B** signals.

Table 25 D94

LED	LED Status	Description
D94	Red - Blinking	Device activity

Connector Type

X66: Optional M.2 2242 Key M card socket

4.14 Gigabit Ethernet (X67 / X68)

X67 and X68 ports support Gigabit Ethernet (GbE) devices.

The software definable pins for the GbE interfaces are connected to pins 6 and 7 of the X31 connector.

These pins may be used for:

- Precision Time Protocol (PTP) clock synchronization
- Hardware control functions
- Software-defined signaling

Table 26 X67, X68

LED Location	LED Color	Signal
Left	Yellow	GBEx_LINK_ACT#
Right	Orange	GBEx_LINK100# / GBEx_LINK_MID#
	Green	GBEx_LINK1000# / GBEx_LINK_MAX#

Note

The yellow LED blinks to indicate link activity and remains steadily lit when a link is established with no activity.

Connector Type

X67, X68: RJ45

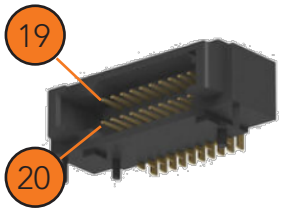
4.15 I/O Header (X75)

X75 header supports various general-purpose I/O and communication signals.

Table 27 X75

Pin	Signal	Pin	Signal
20	GPIO9 / SIM selection	19	GPIO8 / SIM selection
18	GPIO7	17	GPIO4 / Button (M12)
16	GPIO3	15	GPIO2
14	GPIO1	13	GPIO0

X75



12	+3.3 V standby power output (resettable fuse, 0.5 A)	11	+3.3 V runtime power output (resettable fuse, 0.5 A)
10	GND	9	GND
8	COM1_RX	7	COM1_TX
6	COM0_RX-	5	COM0_TX-
4	COM0_RX+	3	COM0_TX+
2	CAN0_L	1	CAN0_H

Connector Type

X75: Header, 2x10-pin, 1.00 mm pitch (Samtec T1M-10-GF-DH)

4.16 GPIO Function Overview

GPIOs are assigned to shared functions as shown in the table below.

Table 28 GPIO0 to GPIO13

GPIO #	SMARC Signal	SMARC pin	Primary Usage	Secondary Usage	Note	Pull-up / Pull-down
GPIO 0	GPIO0 / CAM0_PWR#	P108	GPIO on I/O connector X75	TP7 - JTAG TDO		
GPIO 1	GPIO1 / CAM1_PWR#	P109	GPIO on I/O connector X75	TP8 - JTAG TDI		
GPIO 2	GPIO2 / CAM0_RST#	P110	GPIO on I/O connector X75	TP9 - JTAG TCK		
GPIO 3	GPIO3 / CAM1_RST#	P111	GPIO on I/O connector X75	TP10 - JTAG TMS		
GPIO 4	GPIO4 / HDA_RST#	P112	Button M12	GPIO on I/O connector X75		10 kΩ pull-up to 1V8S
GPIO 5	GPIO5 / PWM_OUT	P113	FAN_PWMOUT			
GPIO 6	GPIO6 / TACHIN	P114	FAN_TACHIN			
GPIO 7	GPIO7	P115	GPIO on I/O connector X75			
GPIO 8	GPIO8	P116	SIM selection 1	GPIO on I/O connector X75		1 MΩ pull-down
GPIO 9	GPIO9	P117	SIM selection 2	GPIO on I/O connector X75		1 MΩ pull-down
GPIO 10	GPIO10	P118	Front LED1 red		Active high	100 kΩ pull-down
GPIO 11	GPIO11	P119	Front LED1 green		Active high	100 kΩ pull-down
GPIO 12	GPIO12	S142	Front LED2 green		Active high	100 kΩ pull-down
GPIO 13	GPIO13	S123	Front LED2 yellow		Active high	100 kΩ pull-down

Note

All GPIO signals listed in this section use 1.8 V logic levels.

4.16.1 GPIO Status LEDs (D87, D88)

D87 and D88 bicolor LEDs indicate the logic level of GPIOs 10 to 13 as shown in the table below.

Table 29 D87, D88

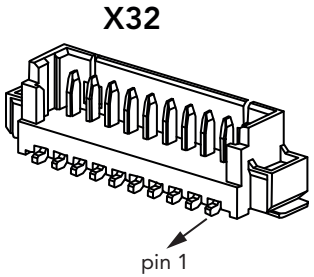
LED	LED Status	Description
D87	Red on	GPIO 10 high
D87	Green on	GPIO 11 high
D88	Green on	GPIO 12 high
D88	Yellow on	GPIO 13 high

4.17 Front Panel Header (X32)

X32 header supports front panel signals such as lid switch, sleep, reset and power button signals, as well as system status LEDs.

Table 30 X32

Pin	Signal Name	Description
1	LID#	Lid switch input
2	GND	Ground
3	SLEEP#	Sleep / hibernation request
4	GND	Ground
5	RESET_IN#	System reset input
6	GND	Ground
7	POWER_BTN#	Power button input
8	GND	Ground
9	PWR_LED (anode)	Power status LED (series resistor included)
10	GND (cathode)	LED cathode
11	PWR_LED (anode)	Alternative LED anode (series resistor included)
12	N.C.	Not connected



Note

The behavior of the control signals (sleep, reset, power button, lid switch) depends on their software configuration.

Connector Type

X32: Header, 12-pin, 1.25 mm pitch (Molex 53398-1271; mating connector: Molex 051021-1200

4.18 Bootloader Source Selection (SW2.2 to SW2.4)

SW2.2 to SW2.4 DIP switches control the BOOT_SEL0 to BOOT_SEL2 signals for bootloader source selection.

Table 31 SW2.2 to SW2.4

Switch	Configuration	Description
SW2.2	OFF	BOOT_SEL0 left unforced (default)
	ON	BOOT_SEL0 forced low
SW2.3	OFF	BOOT_SEL1 left unforced (default)
	ON	BOOT_SEL1 forced low
SW2.4	OFF	BOOT_SEL2 left unforced (default)
	ON	BOOT_SEL2 forced low

4.19 Force Recovery Selection (SW2.1)

SW2.1 DIP switch enables **force recovery mode**.

For more information, refer to the module manual.

Table 32 SW2.1

Switch	Configuration	Description
SW2.1	OFF	Normal operation (default)
	ON	Force recovery mode

Table 33 D59

LED	LED Status	Description
D59	Green - On	Force recovery mode enabled

4.20 Test Mode Selection (SW3.1)

SW3.1 DIP switch controls the TEST# signal for test mode selection.

This mode is intended for **congatec internal use only**.

Table 34 SW3.1

Switch	Configuration	Description
SW3.1	OFF	Normal operation (default)
	ON	Force test mode by holding TEST# low

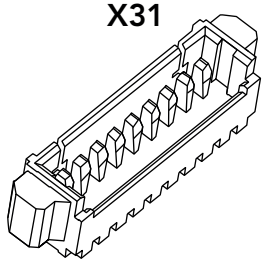
4.21 Feature Header (X31, optional)

Optional X31 header supports management and miscellaneous system signals.

Table 35 X31

Pin	Signal Name	I/O Level	Description
1	CARRIER_STBY#	1.8 V	Input indicating the system is in suspend state (active low)
2	RESET_OUT#	1.8 V	System reset output for external active devices
3	BATLOW#	1.8 V to 5 V	Input indicating the battery is low (open-drain)
4	WDT_TIME_OUT#	1.8 V	Watchdog timer output (active only during runtime)
5	GND		Ground
6	GBE0_SDP	3.3 V	Output signal for hardware implementation of Precision Time Protocol (PTP)
7	GBE1_SDP	3.3 V	Output signal for hardware implementation of Precision Time Protocol (PTP)
8	CHARGING#	1.8 V to 5 V	Input indicating the battery is charging (active low, open-drain output required)
9	CHARGER_PRSNT#	1.8 V to 5 V	Input indicating the presence of a battery charger (open-drain output required)
10	VCC	3.3 V	Standby power output (resettable fuse, 500 mA)

X31



Connector Type

X31: Optional PicoBlade header, 10-pin, 1.25 mm pitch (Molex 053261-1071); mating connector: Molex 051021-1000

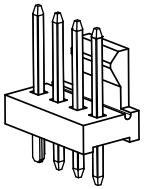
4.22 Fan (X54, optional)

Optional X54 header supports 3-pin or 4-pin 12V fans. The recommended maximum power rating for the fan is **4 W**.

Table 36 X54

Pin	Signal
1	GND
2	12V (resettable fuse, 500mA)
3	FAN_TACHOIN
4	FAN_CTRL

X54



Note

1. *The connector and pinout comply with the 4-Wire Pulse Width Modulation (PWM) Controlled Fans Specification, Revision 1.3.*
2. *FAN_TACHOIN fan output shall provide two pulses per revolution.*
3. *The fan must pull up the FAN_CTRL signal to high logic level.*

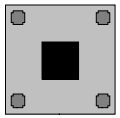
Connector Type

X54: Optional header, 4-pin, 2.54mm pitch

4.23 Button (M12)

M12 button is connected to SMARC GPIO4.

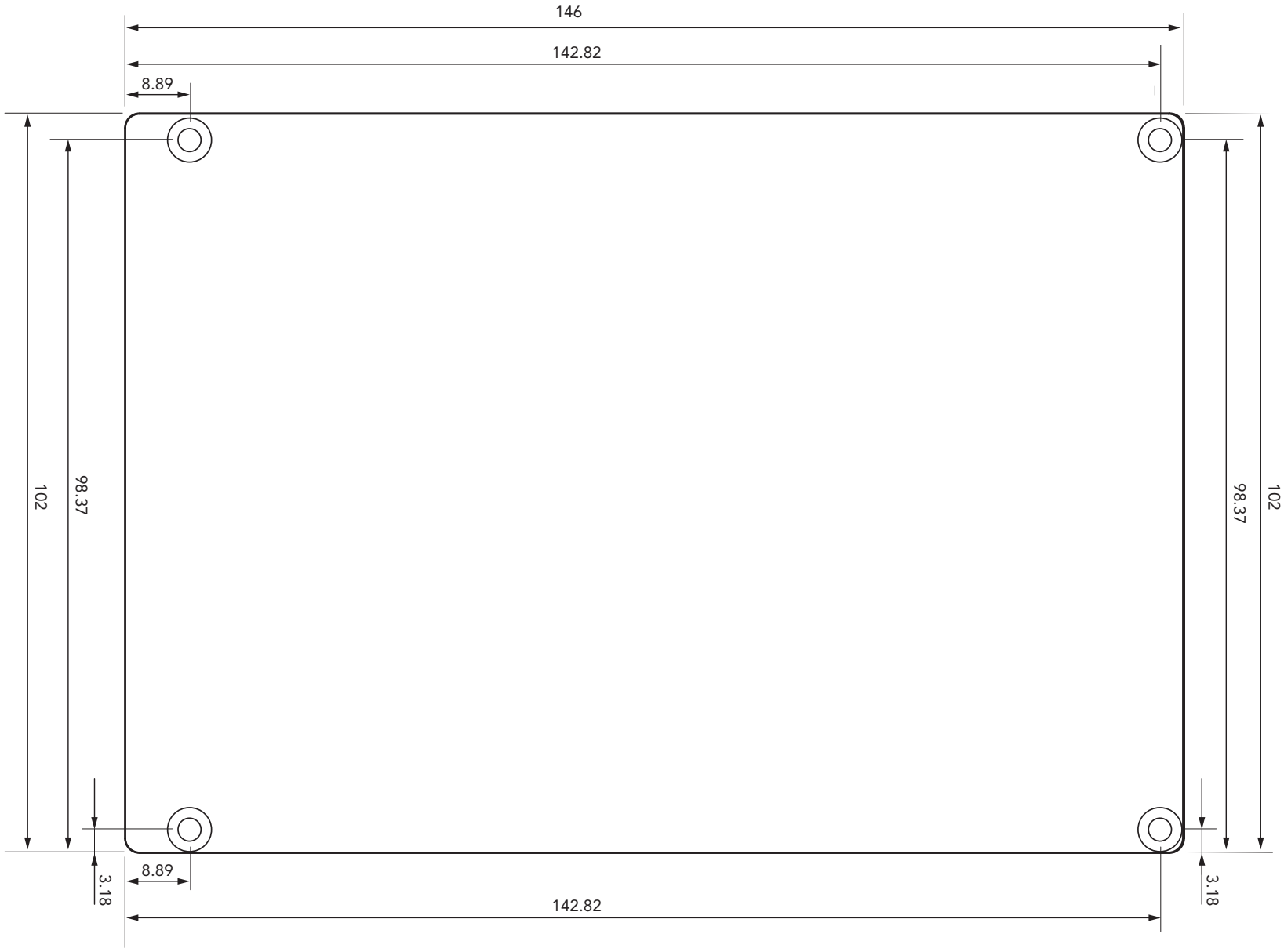
M12



Note

The function depends on the software configuration.

5 Mechanical Drawing



All dimensions are in millimeters.