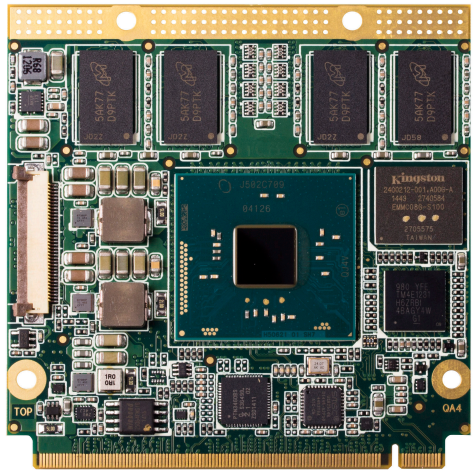

Qseven® conga-QA4

Qseven module based on the Intel® Pentium® and Celeron® Braswell SoC

User's Guide

Revision 1.4

congatec

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2016.03.29	AEM	• Preliminary release
1.0	2016.07.06	AEM	• Removed MIPI support from section 2.1 "Feature List". • Added power consumption values in section 2.5 "Power Consumption" • Updated section 2.7 "Environmental Specifications" and section 4.2 "Heatspreader Dimensions" • Deleted section 6.1.1 "MIPI-CSI 2.0" • Corrected USB interface configurations in section 7.3 "xHCI and EHCI Port Mapping" • Added sections 9 "System Resources", 10 "BIOS Setup Description" and 11 "Additional BIOS Features" • Official release
1.1	2017.06.21	AEM	• Updated section 3 "Block Diagram" • Updated the features supported by the SATA host controller in section 5.4 "SATA" • Added a note in table 9 "USB Signal Descriptions" that USB_OTG is not supported • Updated section 10 "BIOS Setup Description"
1.2	2018.12.21	AEM	• Updated the information about handling electrostatic sensitive devices in preface section • Deleted Microsoft® Windows ® Embedded Compact 7 from section 2.2 "Supported Operating Systems" • Added power consumption values for PN:015214 in table 4 "Power Consumption Values" • Updated sections 2.5 "Power Consumption" and 2.6 "Supply Voltage Battery Power" • Added sub-sections to section 11 "Additional BIOS Features" and updated section 11.4 "Supported Flash Devices"
1.3	2019.01.07	BEU	• Updated table references throughout the document • Updated section 4 "Cooling Solutions" • Updated reference to power supply design guide in section 5.13 "Power Control" • Updated section 6.1 "eMMC 4.5" • Added note about min. pulse width to several button signals in table 25 and 26 • Updated supported flash device in section 11.4 "Supported Flash Devices" • Updated section 12 "Industry Specifications"
1.4	2021.04.15	BEU	• Updated display interfaces in table 1, 2, 10, 20, 27 and section 3 "Block Diagram", 5 "Connector Subsystems", 5.9 "Digital Display Interface", 5.9.1 "DP++ Port" • Deleted section 5.9.2 "HDMI" and 5.9.3 "DVI", 12 "Industry Specifications"

Preface

This user's guide provides information about the components, features, connector and BIOS Setup menus available on the conga-QA4. It is one of three documents that should be referred to when designing a Qseven® application. The other reference documents that should be used include the following:

Qseven® Design Guide
Qseven® Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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Terminology

Term	Description
GB	Gigabyte
GHz	Gigahertz
kB	Kilobyte
MB	Megabyte
Mbit	Megabit
kHz	Kilohertz
MHz	Megahertz
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
DDC	Display Data Channel
SoC	System On Chip
LVDS	Low-Voltage Differential Signaling
Gbe	Gigabit Ethernet
eMMC	Embedded Multi-media Controller
HDA	High Definition Audio
cBC	congatec Board Controller
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

Contents

List of Tables

1 Introduction

1.1 Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector. The pinout remains the same regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The Qseven® evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose what are suitable for their application. Qseven® applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no need to redesign the carrier board.

This document describes the features available on the Qseven® evaluation carrier board. Additionally, the schematics for the Qseven® evaluation carrier board can be found on the congatec website.

1.2 conga-QA4 Options Information

The conga-QA4 is available in six variants. The table below shows the different configurations available.

Table 1 conga-QA4 (Commercial Variants)

Part-No	015210	015211	015212	015213	015214	015215
Processor	Intel® Pentium® N3710 (Quad Core, 1.60 GHz)	Intel® Celeron® N3160 (Quad Core, 1.60 GHz)	Intel® Celeron® N3060 (Dual Core, 1.60 GHz)	Intel® Celeron® N3010 (Dual Core, 1.04 GHz)	Intel® Atom® X5-E8000 (Quad Core, 1.04 GHz)	Intel® Pentium® N3710 (Quad Core, 1.60 GHz)
CPU Burst Freq.	2.56 GHz	2.24 GHz	2.48 GHz	2.24 GHz	2.00 GHz	2.56 GHz
L2 Cache	2MB	2MB	2MB	2MB	2MB	2MB
Onboard Memory	4GB 1600MT/s DDR3L dual channel	2GB 1600MT/s DDR3L dual channel	2GB 1600MT/s DDR3L dual channel	2GB 1600MT/s DDR3L single channel	2GB 1600MT/s DDR3L single channel	4GB 1600MT/s DDR3L dual channel
Graphics	Intel® HD Graphics 405	Intel® HD Graphics 400	Intel® HD Graphics 400	Intel® HD Graphics 400	Intel® HD Graphics	Intel® HD Graphics 405
GFX Normal/Burst	400 MHz/ 700 MHz	320 MHz/ 640 MHz	320 MHz/ 600 MHz	320 MHz/ 600 MHz	320 Mhz / NA	400 MHz/ 700 MHz
LVDS/eDP	LVDS (Single/Dual, 18/24bit)	LVDS (Single/Dual, 18/24bit)	LVDS (Single/Dual, 18/24bit)	LVDS (Single/Dual, 18/24bit)	LVDS (Single/Dual, 18/24bit)	eDP
Default USB Configuration	5 USB 2.0 + 1 USB 3.0	5 USB 2.0 + 1 USB 3.0	8 USB 2.0	8 USB 2.0	8 USB 2.0	5 USB 2.0 + 1 USB 3.0
DDI	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)
eMMC	16GB	16GB	8GB	8GB	8GB	16GB
SD Card	Yes	Yes	Yes	Yes	Yes	Yes
Max. TDP/SDP	6W/4W	6W/4W	6W/4W	4W/3W	5W	6W/4W

2 Specifications

2.1 Feature List

Table 2 Feature Summary

Form Factor	Based on Qseven® form factor specification revision 2.0	
Processor	Intel® Pentium® N3710 Intel® Celeron® N3160, N3060, N3010 Intel® Atom® X5-E8000	
Memory	Single or dual channel non-ECC DDR3L onboard memory interface with up to 8 GB and data rates up to 1600 MT/s. Variants equipped with Intel® Celeron® N3000, N3010 and Intel® Atom® X5-E8000 feature single channel memory interface. For more information, see Table 1.	
Chipset	Integrated in the SoC	
Onboard Storage	eMMC 4.51 onboard flash up to 64 GB	
Audio	High Definition Audio (HDA) interface with support for multiple codecs	
Ethernet	Gigabit Ethernet via the onboard Intel® Ethernet controller I211.	
Graphics Options	Intel® HD Graphics Gen. 8 LP with support for DirectX11.1, OpenGL 4.2, OpenCL 1.2, OpenGLES 3.0, full HW acceleration with H.265/HEVC decoding and H.264 encoding, MPEG2, MVC, VC-1, WMV9, JPEG and support for three independent displays.	
	Flat LVDS (Integrated flat panel interface with 25-112MHz single/dual-channel LVDS Transmitter). Supports: - Single channel LVDS interface: 1 x 18 bpp or 1 x 24 bpp. - Dual channel LVDS interface : 2 x 18 bpp or 2 x 24 bpp. - VESA LVDS color mappings - Automatic Panel Detection via Embedded Panel Interface based on VESA EDID™ 1.3. - Resolution up to 1920x1200 in dual LVDS bus mode. Optional eDP interface (assembly option) **NOTE**: Either eDP or LVDS signals supported, not both signal types simultaneously.	1x DDI with support for DP++ (DP/HDMI™/DVI) **NOTE**: The conga-QA4 does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.
Peripheral Interfaces	2x Serial ATA® up to 6Gb/s 3x PCI Express® Gen2 links up to 5.0 GT/s per lane. USB Interfaces: - 8x USB 2.0 or - 5x USB 2.0 + 1 USB 3.0 or - 2x USB 2.0 + 2 USB 3.0 or	1x SD/MMC UART SPI Bus LPC Bus I²C Bus
BIOS Features	AMI Aptio® UEFI 5.x firmware; 8 MByte serial SPI with congatec Embedded BIOS features (OEM Logo, OEM CMOS Defaults, LCD Control, Display Auto Detection, Backlight Control, Flash Update)	
Power Management	ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).	
congatec Board Controller	Multi Stage Watchdog, non-volatile User Data Storage, Manufacturing and Board Information, Board Statistics, BIOS Setup Data Backup, I²C bus (fast mode, 400 kHz, multi-master), Power Loss Control	

2.2 Supported Operating Systems

The conga-QA4 supports the following operating systems:

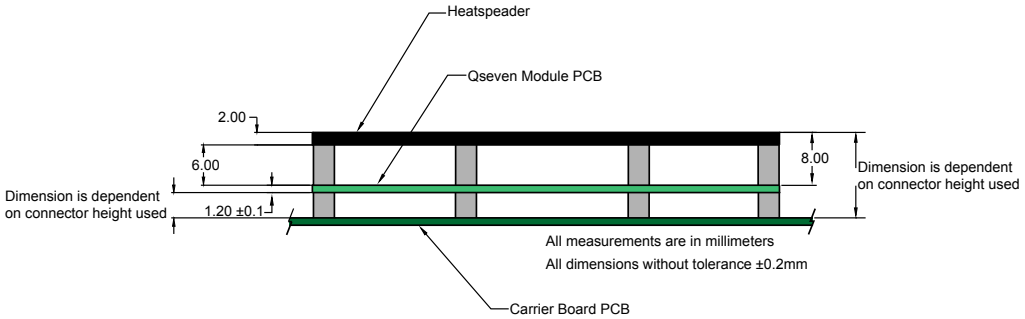
- Microsoft® Windows® 10
- Microsoft® Windows® 8
- Microsoft® Windows® Embedded Standard 8
- Microsoft® Windows® 7
- Microsoft® Windows® Embedded Standard 7
- Linux
- Android

Note

The conga-QA4 requires a minimum storage capacity of 16 GB (32-bit) or 20 GB (64-bit) for Windows 7/8/10 or WES 7/8 installation. congatec AG will not offer support for systems that do not meet the minimum requirement.

2.3 Mechanical Dimensions

- 70.0 mm x 70.0 mm
- The Qseven™ module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12 mm thick.

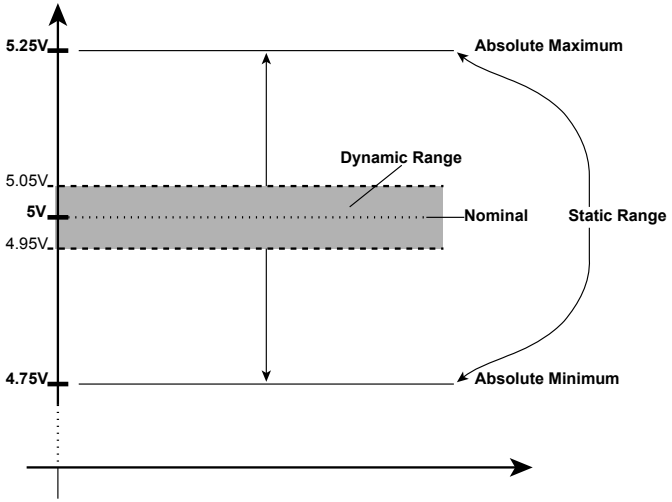


Rear View of Qseven Module

2.4 Supply Voltage Standard Power

- 5V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Characteristics			Min.	Typ.	Max.	Units	Comment
5V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV_{PP}	0-20MHz
	Current						
5V_SB	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple				± 50	mV_{PP}	

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

Note

For information about the input power sequencing of the Qseven® module, refer to the Qseven® specification.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-QA4 COM
- modified congatec carrier board
- conga-QA4 cooling solution
- Microsoft Windows 7 (64-bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool

Table 3 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle.	The CPU was stressed to its maximum frequency.
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency.
S0: Peak value	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.
S3	COM is powered by VCC_5V_SBY.	
S5	COM is powered by VCC_5V_SBY.	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Table 4 Power Consumption Values

The table below provide additional information about the power consumption data for each of the conga-QA4 variants offered. The values are recorded at various operating mode.

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64-bit)	CPU			Current (A)				
					Variant	Cores	Freq/Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5
015210	4 GB	A.1	QA40R011	Windows 7	Intel® Pentium® N3710	4	1.60 / 2.56	0.20	1.17	1.68	0.07	0.06
015211	2 GB	A.1	QA40R011	Windows 7	Intel® Celeron® N3160	4	1.60 / 2.24	0.16	1.10	1.26	0.07	0.06
015212	2 GB	A.0	QA40R011	Windows 7	Intel® Celeron® N3060	2	1.60 / 2.48	0.17	0.92	1.17	0.11	0.10
015213	2 GB	A.0	QA40R011	Windows 7	Intel® Celeron® N3010	2	1.04 / 2.24	0.19	0.64	1.05	0.11	0.11
015214	2 GB	A.1	QA40R011	Windows 7	Intel® Atom™ x5-E8000	4	1.04 / 2.00	0.17	0.76	0.80	0.07	0.06

Note

1. *With fast input voltage rise time, the inrush current may exceed the measured peak current.*
2. *All recorded power consumption values are approximate and only valid for the controlled environment described earlier.*

2.6 Supply Voltage Battery Power

Table 5 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	1.63 µA
20°C	3V DC	2.01 µA
70°C	3V DC	11.91 µA

Note

1. *Do not use the CMOS battery power consumption value listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec AG website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-QA4*

2.7 Environmental Specifications

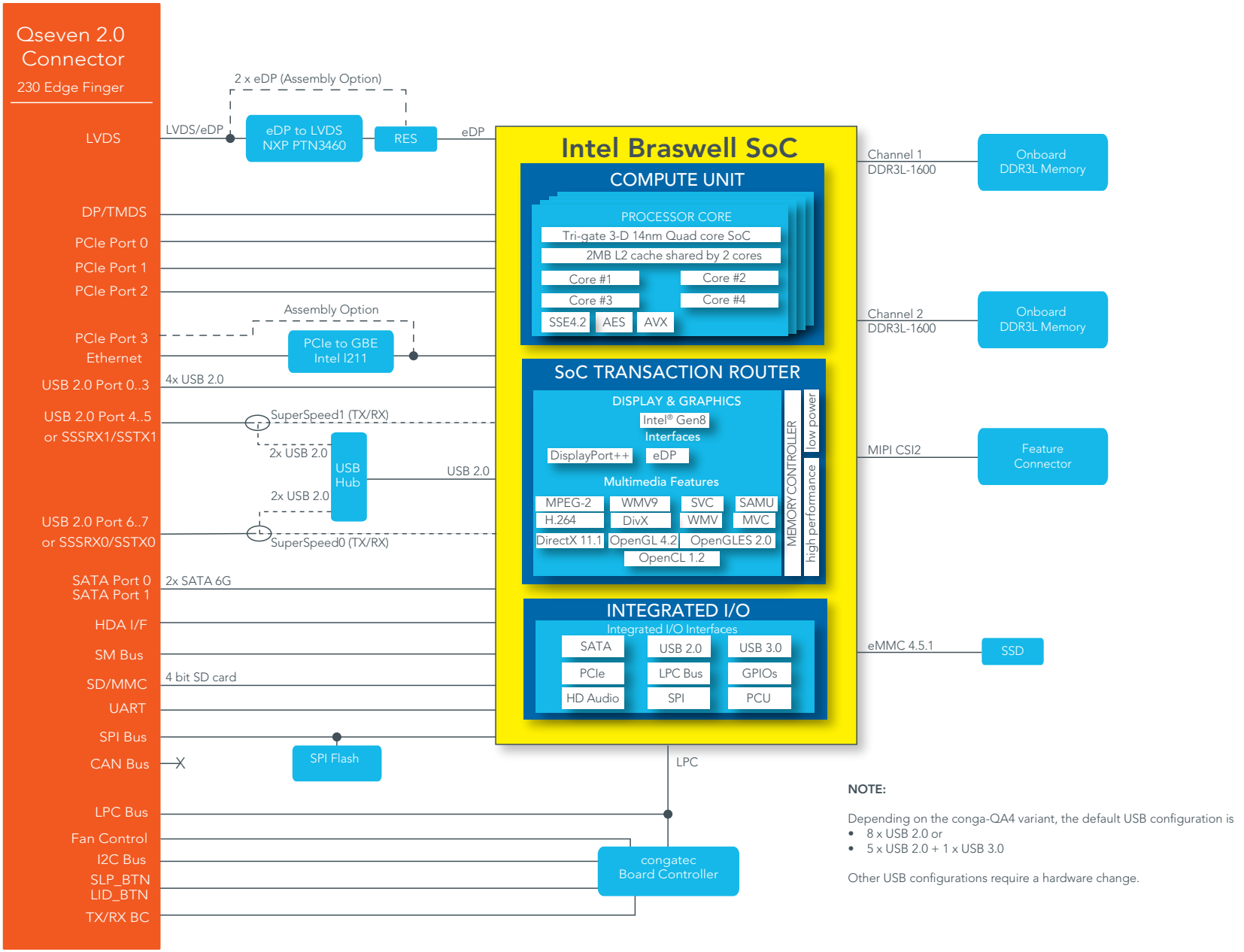
Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



NOTE:

Depending on the conga-QA4 variant, the default USB configuration is

- 8 x USB 2.0 or
- 5 x USB 2.0 + 1 x USB 3.0

Other USB configurations require a hardware change.

4 Cooling Solutions

congatec AG offers the cooling solutions listed in Table 6 for conga-QA4. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 6 Cooling Solution Variants

	Cooling Solution	Part No	Description
1	HSP	015191	Heatspreader with 2.7 mm bore-hole standoff.
		015190	Heatspreader with M2.5 mm threaded standoff.
2	CSP	015193	Passive cooling with 2.7 mm bore-hole standoffs.
		015192	Passive cooling with M2.5 mm threaded standoffs.

Note

1. *We recommend a maximum torque of 0.4 Nm for the mounting screws and to start with the two screws furthest from the CPU die.*

2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

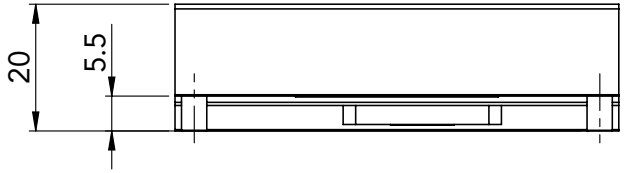
Caution

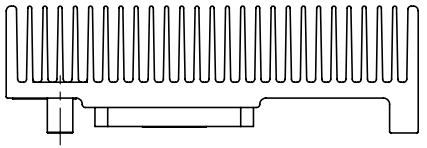
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

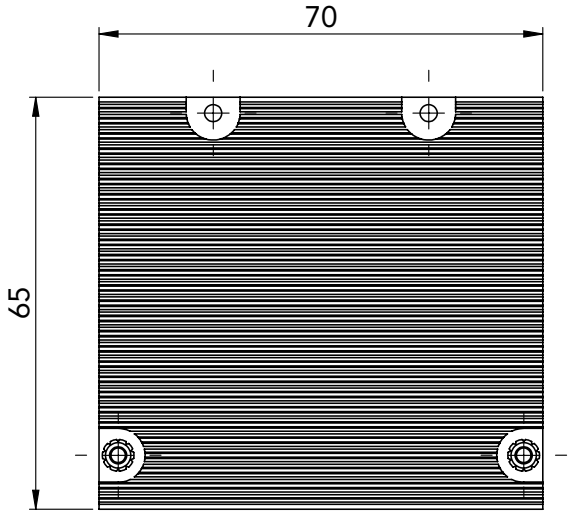
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

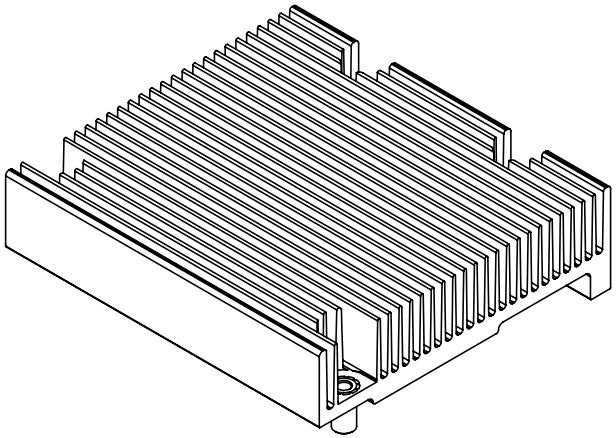
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

4.1 CSP Dimensions

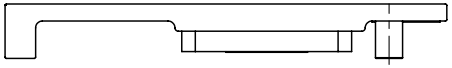


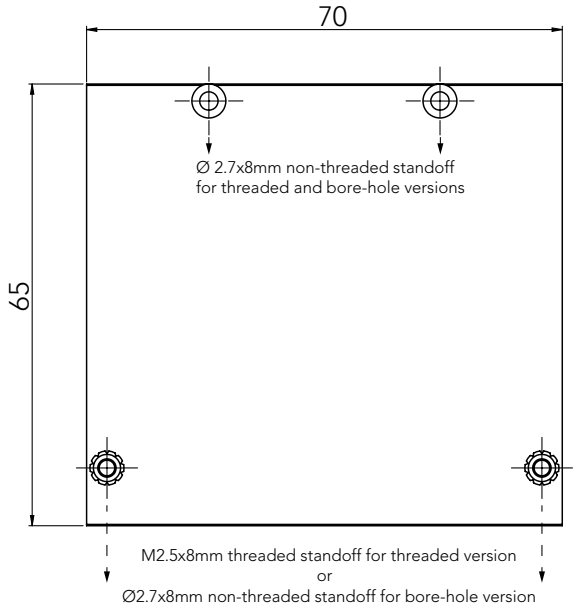


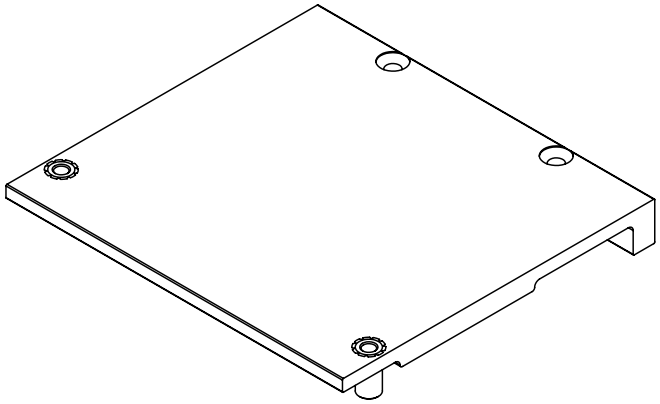




4.2 HSP Dimensions

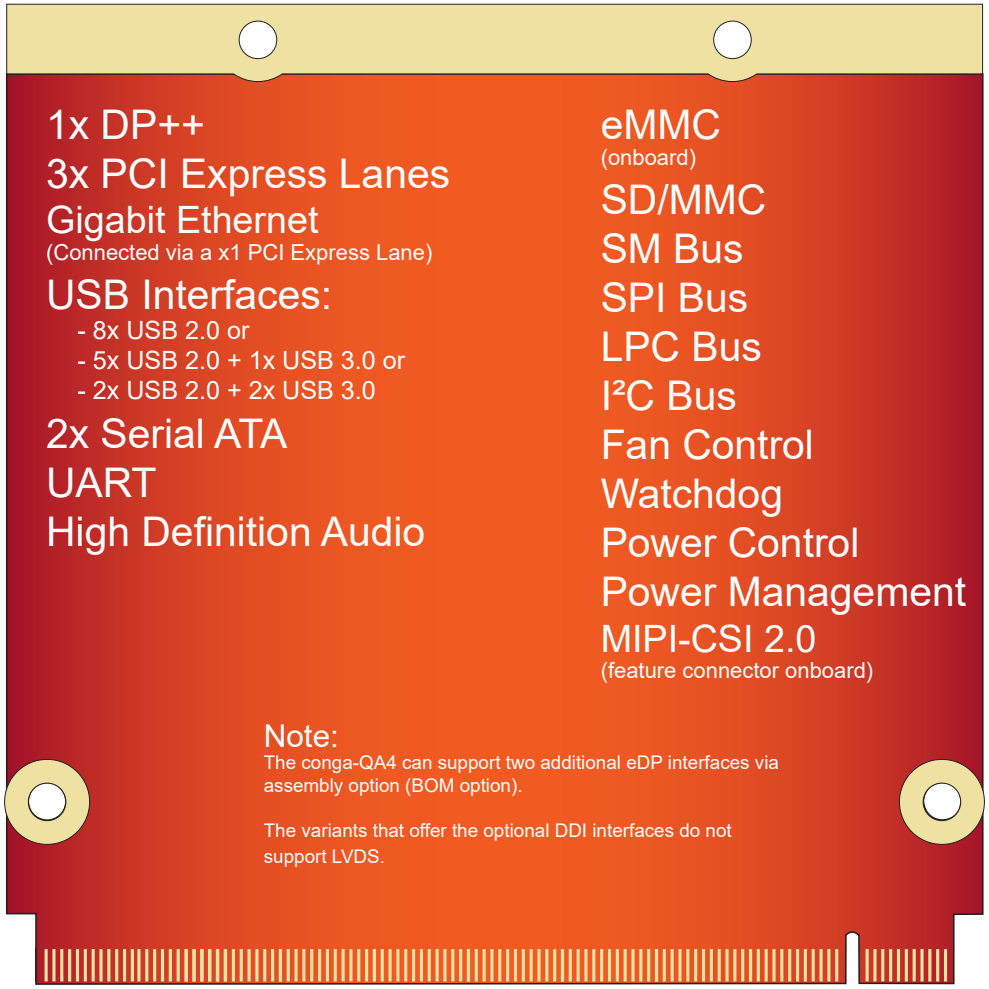






5 Connector Subsystems

The conga-QA4 is based on the Qseven® standard and therefore has 115 edge fingers on the top and bottom side of the module that mate with the 230-pin card-edge MXM connector located on the carrier board. This connector is able to interface the available signals of the conga-QA4 with the carrier board peripherals.



5.1 PCI Express™

The conga-QA4 offers 3 PCIe lanes externally on the Edge finger. The lanes are Gen 2 compliant and offer support for full 5 Gb/s bandwidth in each direction per x1 link. Default configuration for the lanes is 3 x1 link. A 1 x2 + 1 x1 link configuration is also possible but requires a special/ customized BIOS firmware. Contact congatec technical support for more information about this subject.

The PCI Express interface is based on the PCI Express Specification 2.0 with Gen 1 (2.5Gb/s) and Gen 2 (5 Gb/s) speed. For more information refer to the conga-QA4 pinout table in section 8 “Signal Descriptions and Pinout Tables.” .

5.2 ExpressCard™

The conga-QA4 does not support ExpressCard.

5.3 Gigabit Ethernet

The conga-QA4 offers a Gigabit Ethernet interface on the edge finger via the onboard Intel® I211 Gigabit Ethernet controller. This controller is connected to the Intel® Braswell SoC through the fourth PCI Express lane. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be routed to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

5.4 SATA

The conga-QA4 offers 2 SATA interfaces on the edge finger via a SATA host controller integrated in the Braswell SoC. The SATA host controller supports DMA auto-activate feature, hot-plug detect, AHCI operations and data transfer rates up to 6 Gb/s (Gen. 3).

For more information, refer to section 10 “BIOS Setup Description”.

5.5 Universal Serial Bus

The conga-QA4 offers up to 8 USB ports (up to two USB 3.0 and four USB 2.0). Four of these ports (USB0-3) are routed directly from the SoC to the Qseven connector. The other four (USB4-7) are routed to the the connector via a 4-port USB hub.

5.5.1 USB 2.0

The conga-QA4 offers up to 8 USB 2.0 interfaces on the Edge finger. These interfaces are provided by routing four of the five High Speed ports provided by the Braswell SoC directly to the edge finger. The fifth port provided by the SoC is routed to the edge finger via a USB hub, thereby providing additional four USB ports. These additional ports can be reused with SuperSpeed signals to create USB 3.0 ports.

The xHCI host controller in the SoC supports these interfaces with high-speed, full-speed and low-speed USB signalling.

Note

Each conga-QA4 variant offers a specific USB configuration by default (see section 1.2). For non-default USB configuration, you need a customized conga-QA4 variant.

5.5.2 USB 3.0

The conga-QA4 offers up to two USB SuperSpeed differential signals (SSTX0/SSRX0 and SSTX1/SSRX1) on the edge finger for USB 3.0 support. The SSTX0/SSRX0 differential signals can be combined with USB port 0 to create a USB 3.0 port while the TX1/RX1 differential signals can be combined with USB port 1 to create an additional USB 3.0 port.

The SuperSpeed signals are controlled by the xHCI host controller in the SoC. The host controller allows data transfers of up to 5 Gb/s and supports SuperSpeed, high-speed, full-speed and low-speed USB signalling. See section 7.3 for more information about xHCI port mapping.

Note

Each conga-QA4 variant offers a specific USB configuration by default (see section 1.2). For non-default USB configuration, you need a customized conga-QA4 variant.

5.6 SD Card

The conga-QA4 offers a 4-bit SD interface for SD/MMC cards on the Edge finger. The SD card controller in the Storage Control Cluster of the SoC supports the SD interface with up to 832 Mb/s data rate using 4 parallel data lines.

5.7 UART

The conga-QA4 offers a UART interface on the edge connector. The UART signals are routed from the onboard SoC. For more information, see Table 12.

5.8 High Definition Audio (HDA)

The conga-QA4 provides a High Definition Audio interface. This interface supports the connection of HDA audio codecs.

5.9 Digital Display Interface

The conga-QA4 offers one dedicated Digital Display Interface (Braswell DDI2) on the Qseven connector. This interface supports DP++. The conga-QA4 can optionally support two additional eDP interfaces but this option requires a hardware change (assembly option).

The conga-QA4 supports up to three independent displays as shown below:

Table 7 Display Combination

	Display 1		Display 2		Display 3	
	External	Max. Resolution	Internal/External	Max. Resolution	Internal/External	Max. Resolution
Option 1 (Default)	DP	3840x2160* @ 30Hz or 2560x1600 @ 60Hz	LVDS (up to 2x 24 bit)	1920x1200 @ 60Hz (dual LVDS mode)	N/A	N/A
Option 2	DP	3840x2160* @ 30Hz or 2560x1600 @ 60Hz	eDP (BOM Option)	2560x1440 @ 60Hz	eDP (BOM Option)	2560x1440 @ 60Hz

** Supports 8-bit color depth only*

Note

Customized variants with optional DDI interfaces do not support LVDS.

5.9.1 DP++ Port

DisplayPort is an open, industry standard digital display interface, that has been developed within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

The conga-QA4 offers a DisplayPort interface on the Qseven connector by default but can optionally support additional two DisplayPort interfaces via an assembly option (BOM option).

Note

See Table 7 above for possible display combinations.

5.9.2 LVDS/eDP

The conga-QA4 offers a single/dual channel LVDS/eDP interface on the edge finger. The interface is provided by routing the onboard PTN3460 eDP to LVDS bridge to the DDI port 1 of the Braswell SoC. The bridge processes the incoming DisplayPort stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format.

The LVDS/eDP interface supports single and dual channel signalling with color depths of 18 bits or 24 bits per pixel and pixel clock frequency up to 112 MHz. It also supports automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3, with resolution up to 1920x1200 in dual LVDS bus mode. The interface is designed by default to provide only LVDS signals. However, this interface can support eDP signals via assembly option (BOM option). For more information, contact congatec technical support.

5.10 LPC

The conga-QA4 offers the Low Pin Count (LPC) bus. The LPC bus is similar to a serialized ISA bus but with fewer signals. Due to the software compatibility with the ISA bus, it is easy to implement I/O extensions such as additional serial ports on an application specific baseboard using the LPC bus. Many devices are available for this cost-efficient, low-speed interface designed to support low bandwidth and legacy devices.

5.11 SPI

The conga-QA4 offers the SPI interface on the edge finger connector. The interface is only used to boot a BIOS from an SPI Flash device placed on the carrier board.

5.12 I²C Bus

The conga-QA4 supports I2C bus. Thanks to the I2C host controller in the cBC, the I²C bus is multi-master capable and runs at fast mode.

5.13 Power Control

The conga-QA4 supports ATX-style power supplies control. In order to do this the power supply must provide a constant source of VCC_5V_SB power. The AT-style power supply (5V only) is also supported. In this case, the conga-QA4's pin PWRBTN# should be left unconnected, pin SUS_S3# should control the main power regulators on the carrier board (+3.3V...) and pins VCC_5V_SB should be connected to the 5V input power rail according to the Qseven specification.

PWGIN

PWGIN (pin 26) can be connected to an external power good circuit. This input is optional and should be left unconnected when not used. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies, the conga-QA4 module is capable of generating its own power good.

SUS_S3#

The SUS_S3# (pin 18) signal is an active-low output that can be used to control the main 5V rail of the power supply for module and all other main power supplies on carrier board. In order to accomplish this, the signal must be inverted with an inverter/transistor that is supplied by standby voltage (ATX-style) or system input voltage (AT-style) and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 20) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3.3V_SB using a 10k resistor. When PWRBTN# is asserted, it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Note

To initiate an ACPI event, the Braswell SoC expects a rising edge on the PWRBTN# signal.

Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-QA4. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-QA4 application:

- It has also been noticed that on some occasions, problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush current on the conga-QA4 VCC_5V_SB power rail can go up as high as 6.6A and as high as 12.8A on the conga-QA4 VCC power rail within a short time (approx 100µs) and with a voltage rise time of 100µs.

Sufficient decoupling capacitance must be implemented to ensure proper power-up sequencing.

Note

For more information about power control event signals refer to the Qseven® specification.

5.14 Power Management

ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3). No support for legacy APM.

6 Additional Features

6.1 eMMC 4.5

The conga-QA4 offers an optional eMMC 4.5 flash onboard the Intel Atom variants, with up to 64 GB capacity. Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology. The performance of the newer eMMC may vary depending on the eMMC technology.

Note

For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions.

6.2 congatec Board Controller (cBC)

The conga-QA4 is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRBI microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

6.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.2.2 Fan Control

The conga-QA4 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

6.2.3 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are "Always On", "Remain Off" and "Last State".

6.2.4 Watchdog

The conga-QA4 is equipped with a multi stage watchdog solution that can be triggered by software of external hardware. For more information about the watchdog feature, see the BIOS setup description in section 10.4.1 of this document and the application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

6.3 OEM BIOS Customization

The conga-QA4 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

6.3.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.3.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.3.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.3.4 OEM BIOS Code/Data

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table (OA2.0), Windows 8 OEM activation (OA3.0), verb tables for HDA codecs, PCI/PCIe opROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.3.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-QA4 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

6.5 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

6.6 Suspend to RAM

The Suspend to RAM feature is available on the conga-QA4.

7 conga Tech Notes

The conga-QA4 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the system resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

7.1 Intel Braswell SoC Features

7.1.1 Processor Core

The Intel Braswell Soc features Dual or Quad Out-of-Order Execution processor cores. The cores are sub-divided into dual-core modules with each module sharing a 1 MB L2 cache (512 KB per core). Some of the features supported by the core are:

- Intel 64 architecture
- Support for Intel VT-x
- Power management features
- Thermal management system
- Security and cryptography technologies
- Uses 14 nm process technology

Note

Intel Hyper-Threading technology is not supported (four cores execute four threads)

7.1.1.1 Intel Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel® VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

7.1.1.2 AHCI

The Braswell SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

7.1.1.3 IDE Mode (Native Vs. Legacy)

Legacy Mode

When operating in legacy mode, the SATA controllers need two legacy IRQs (14 and 15) and are unable to share these IRQs with other devices. This is because the SATA controllers emulate the primary and secondary legacy IDE controllers.

Native Mode

Native mode allows the SATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources. This means they can be configured anywhere within the system. When either SATA controller 1 or 2 runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system. Setting "IDE Mode" in the BIOS setup program will automatically enable Native mode. See section 10.4.12 for more information about this. Running in native mode frees up interrupt resources (IRQs 14 and 15) and decreases the chance that there may be a shortage of interrupts when installing devices.

Note

If your operating system supports native mode then congatec AG recommends you enable it.

7.1.1.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-QA4 ACPI thermal solution offers three different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.2 ACPI Suspend Modes and Resume Events

The conga-QA4 supports S3 (Suspend to RAM). For more information about S3 wake events see section 10.4.6 "ACPI Configuration Submenu".

Table 8 Wake Events

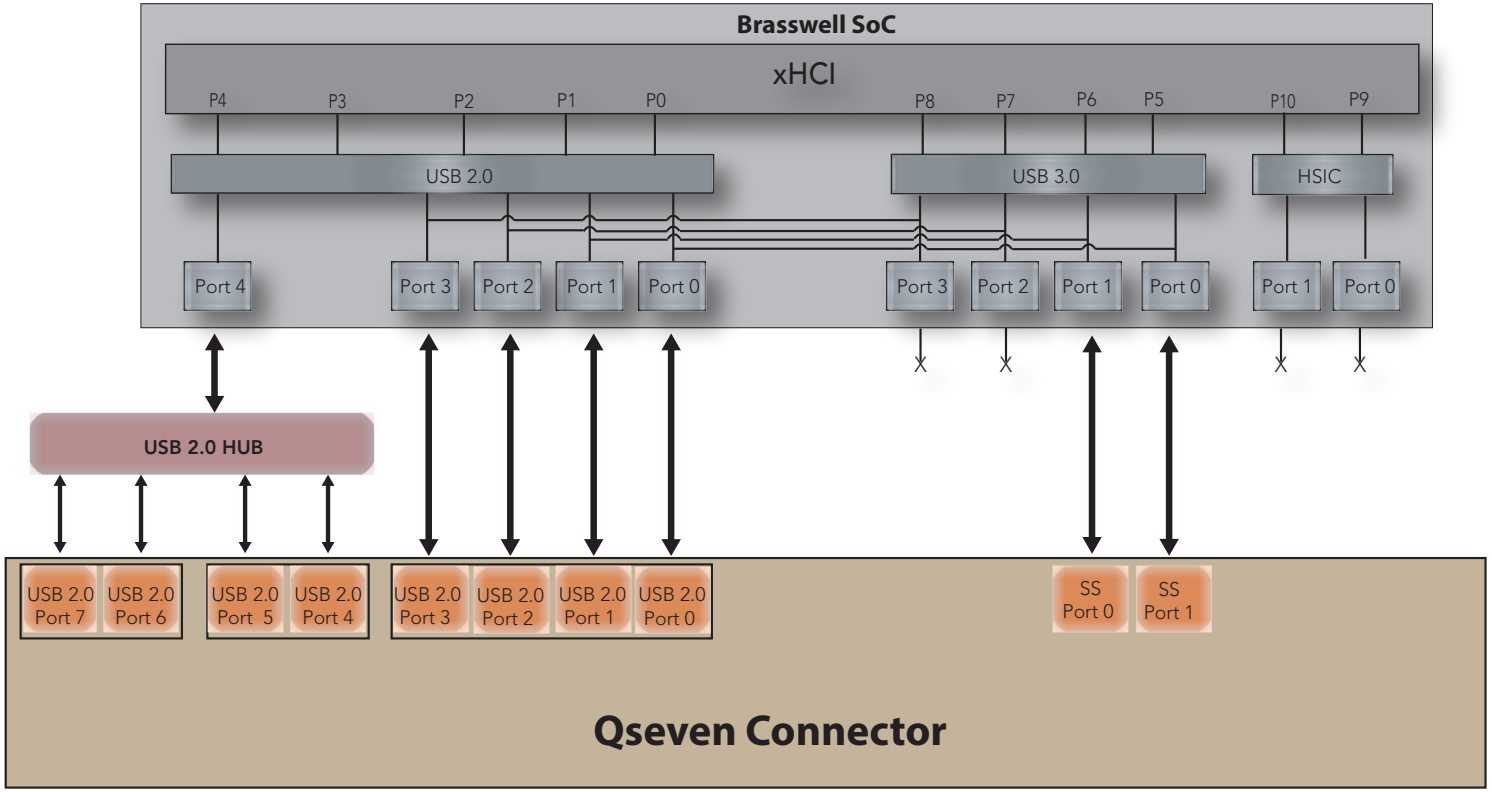
The table below lists the events that wake the system from S3.

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

Note

The BIOS does not support S4 (Suspend to Disk).

7.3 xHCI and EHCI Port Mapping



NOTE:

Possible USB configurations are:

(*) Up to 8x USB 2.0
(*) Up to 5x USB 2.0 and 1x USB 3.0
(*) Up to 2x USB 2.0 and 2x USB 3.0

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on Qseven® module's edge fingers.

Table 9 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

Not all the signals described in this section are available on all conga-QA4 variants. Use the article number of the module and refer to Table 1 to determine the options available on the module.

Table 9 Signal Tables Terminology Descriptions

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PP	Push Pull
I/O	Bi-directional Input/Output Pin
P	Power Input
NA	Not applicable
NC	Not Connected
PCIE	PCI Express differential pair signals
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus
SATA	Serial Advanced Technology Attachment
SPI	Serial Peripheral Interface bus
LVDS	Low-Voltage Differential Signaling
TMDS	Transition Minimized Differential Signaling differential pair signals
CMOS	Logic input or output

Table 10 Edge Finger Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Power Ground	2	GND	Power Ground
3	GBE_MDI3-	Gigabit Ethernet MDI3-	4	GBE_MDI2-	Gigabit Ethernet MDI2-
5	GBE_MDI3+	Gigabit Ethernet MDI3+	6	GBE_MDI2+	Gigabit Ethernet MDI2+
7	GBE_LINK100#	100 Mbps link speed	8	GBE_LINK1000#	1000 Mbps link speed
9	GBE_MDI1-	Gigabit Ethernet MDI1-	10	GBE_MDI0-	Gigabit Ethernet MDI0-
11	GBE_MDI1+	Gigabit Ethernet MDI1+	12	GBE_MDI0+	Gigabit Ethernet MDI0+
13	GBE_LINK#	Gigabit Ethernet Link indicator	14	GBE_ACT#	Gigabit Ethernet Activity indicator
15	GBE_CTREF (*)	Reference voltage for GBE	16	SUS_S5#	S5 (Soft OFF) – shutdown state
17	WAKE#	External system wake event	18	SUS_S3#	S3 (Suspend to RAM) – SLP
19	SUS_STAT#	Suspend status	20	PWRBTN#	Power button
21	SLP_BTN#	Sleep button	22	LID_BTN#	LID button
23	GND	Power Ground	24	GND	Power Ground
25	GND	Power Ground	26	PWGIN	Power good input
27	BATLOW#	Battery low input	28	RSTBTN#	Reset button input
29	SATA0_TX+	Serial ATA Channel 0 TX+	30	SATA1_TX+	Serial ATA Channel 1 TX+
31	SATA0_TX-	Serial ATA Channel 0 TX-	32	SATA1_TX-	Serial ATA Channel 1 TX-
33	SATA_ACT#	Serial ATA Activity	34	GND	Power Ground
35	SATA0_RX+	Serial ATA Channel 0 RX+	36	SATA1_RX+	Serial ATA Channel 1 RX+
37	SATA0_RX-	Serial ATA Channel 0 RX-	38	SATA1_RX-	Serial ATA Channel 1 RX-
39	GND	Power Ground	40	GND	Power Ground
41	BIOS_DISABLE# /BOOT_ALT#	BIOS Module disable Boot Alternative Enable	42	SDIO_CLK	SDIO Clock Output
43	SDIO_CD#	SDIO Card Detect	44	SDIO_LED	SDIO LED
45	SDIO_CMD	SDIO Command/Response	46	SDIO_WP	SDIO Write Protect
47	SDIO_PWR#	SDIO Power Enable	48	SDIO_DAT1	SDIO Data Line 1
49	SDIO_DAT0	SDIO Data Line 0	50	SDIO_DAT3	SDIO Data Line 3
51	SDIO_DAT2	SDIO Data Line 2	52	SDIO_DAT5 (*)	SDIO Data Line 5
53	SDIO_DAT4 (*)	SDIO Data Line 4	54	SDIO_DAT7 (*)	SDIO Data Line 7
55	SDIO_DAT6 (*)	SDIO Data Line 6	56	USB_DRIVE_VBUS (*)	USB power enable pin for USB Port 1
57	GND	Power Ground	58	GND	Power Ground
59	HDA_SYNC / I2S_WS	HD Audio/AC'97 Synchronization. Multiplexed with I2S Word Select from Codec	60	SMB_CLK / GP1_I2C_CLK	SMBus Clock line. Multiplexed with General Purpose I²C bus #1 clock line
61	HDA_RST# / I2S_RST#	HD Audio/AC'97 Codec Reset. Multiplexed with I2S Codec Reset	62	SMB_DAT / GP1_I2C_DAT	SMBus Data line. Multiplexed with General Purpose I²C bus #1 data line.
63	HDA_BITCLK / I2S_CLK	HD Audio/AC'97 Serial Bit Clock. Multiplexed with I2S Serial Data Clock from Codec.	64	SMB_ALERT#	SMBus Alert input
65	HDA_SDI (**) / I2S_SDI	HD Audio/AC'97 Serial Data In. Multiplexed with I2S Serial Data Input from Codec	66	GP0_I2C_CLK	General Purpose I2C Bus No 0 clock line

Pin	Signal	Description	Pin	Signal	Description
67	HDA_SDO / I2S_SDO	HD Audio/AC'97 Serial Data Out. Multiplexed with I2S Serial Data Output from Codec	68	GP0_I2C_DAT	General Purpose I2C Bus No 0 data line
69	THRM#	Thermal Alarm active low	70	WDTRIG#	Watchdog trigger signal
71	THRMTRIP#	Thermal Trip indicates an overheating condition	72	WDOUT	Watchdog event indicator
73	GND	Power Ground	74	GND	Power Ground
75	USB_P7- / USB_SSTX0-	USB Port 7 Differential Pair- . Multiplexed with Superspeed USB transmit differential pair-	76	USB_P6- / USB_SSRX0-	USB Port 6 Differential Pair-. Multiplexed with Superspeed USB transmit differential pair-
77	USB_P7+ / USB_SSTX0+	USB Port 7 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+	78	USB_P6+ / USB_SSRX0+	USB Port 6 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+
79	USB_6_7_OC#	Over current detect input 6/7 USB	80	USB_4_5_OC#	Over current detect input 4/5 USB
81	USB_P5- / USB_SSTX1-	USB Port 5 Differential Pair-	82	USB_P4- / USB_SSRX1-	USB Port 4 Differential Pair-
83	USB_P5+ / USB_SSTX1+	USB Port 5 Differential Pair+	84	USB_P4+ / USB_SSRX1+	USB Port 4 Differential Pair+
85	USB_2_3_OC#	Over current detect input 2/3 USB	86	USB_0_1_OC#	Over current detect input 0/1 USB
87	USB_P3-	USB Port 3 Differential Pair-	88	USB_P2-	USB Port 2 Differential Pair-
89	USB_P3+	USB Port 3 Differential Pair+	90	USB_P2+	USB Port 2 Differential Pair+
91	USB_VBUS (*)	USB VBUS pin	92	USB_ID (*)	USB ID pin
93	USB_P1-	USB Port 1 Differential Pair-	94	USB_P0-	USB Port 0 Differential Pair-
95	USB_P1+	USB Port 1 Differential Pair+	96	USB_P0+	USB Port 0 Differential Pair+
97	GND	Power Ground	98	GND	Power Ground
99	eDP0_TX0+ / LVDS_A0+	eDP Primary Channel 0+ LVDS Primary channel 0+	100	eDP1_TX0+ / LVDS_B0+	eDP Secondary channel 0+ LVDS Secondary channel 0+
101	eDP0_TX0- / LVDS_A0-	eDP Primary channel 0- LVDS Primary channel 0-	102	eDP1_TX0- / LVDS_B0-	eDP Secondary channel 0- LVDS Secondary channel 0-
103	eDP0_TX1+ / LVDS_A1+	eDP Primary channel 1+ LVDS Primary channel 1+	104	eDP1_TX1+ / LVDS_B1+	eDP Secondary channel 1+ LVDS Secondary channel 1+
105	eDP0_TX1- / LVDS_A1-	eDP Primary channel 1- LVDS Primary channel 1-	106	eDP1_TX1- / LVDS_B1-	eDP Secondary channel 1- LVDS Secondary channel 1-
107	eDP0_TX2+ / LVDS_A2+	eDP Primary channel 2+ LVDS Primary channel 2+	108	eDP1_TX2+ / LVDS_B2+	eDP Secondary channel 2+ LVDS Secondary channel 2+
109	eDP0_TX2- / LVDS_A2-	eDP Primary channel 2- LVDS Primary channel 2-	110	eDP1_TX2- / LVDS_B2-	eDP Secondary channel 2- LVDS Secondary channel 2-
111	LVDS_PPEN	LVDS Power enable	112	LVDS_BLEN	LVDS Backlight enable
113	eDP0_TX3+ / LVDS_A3+	eDP Primary channel 3+ LVDS Primary channel 3+	114	eDP1_TX3+ / LVDS_B3+	eDP Secondary channel 3+ LVDS Secondary channel 3+
115	eDP0_TX3- / LVDS_A3-	eDP Primary channel 3- LVDS Primary channel 3-	116	eDP1_TX3- / LVDS_B3-	eDP Secondary channel 3- LVDS Secondary channel 3-
117	GND	Power Ground	118	GND	Power Ground
119	eDP0_AUX+ / LVDS_A_CLK+	eDP Primary Auxilliary channel+ LVDS Primary channel CLK+	120	eDP1_AUX+ / LVDS_B_CLK+	eDP Secondary Auxiliary channel CLK+ LVDS Secondary channel CLK+

Pin	Signal	Description	Pin	Signal	Description
121	eDP0_AUX- / LVDS_A_CLK-	eDP Primary Auxilliary channel- LVDS Primary channel CLK-	122	eDP1_AUX- / LVDS_B_CLK-	eDP Secondary Auxiliary channel CLK- LVDS Secondary channel CLK-
123	LVDS_BLT_CTRL / GP_PWM_OUT0	PWM Backlight brightness General Purpose PWM Output	124	GP_1-Wire_Bus (*)	General Purpose 1-wire bus interface
125	LVDS_DID_DAT / GP_I2C_DAT	DDC Display ID Data line DDC based control signal (data) for optional TMDS	126	eDP0_HPD# / LVDS_BLC_DAT	Can be used as eDP primary hotplug detect
127	LVDS_DID_CLK / GP_I2C_CLK	DDC Display ID Clock line DDC based control signal (clk) for optional TMDS	128	eDP1_HPD# / LVDS_BLC_CLK	Can be used as eDP secondary hotplug detect
129	CAN0_TX (*)	CAN TX Output for CAN Bus Channel 0	130	CAN0_RX (*)	CAN RX Input for CAN Bus Channel 0
131	DP_LANE3+ / TMDS_CLK+	DisplayPort differential pair line lane 3. Multiplexed with TMDS differential pair clock+	132	RSVD (Differential)	Reserved
133	DP_LANE3- / TMDS_CLK-	DisplayPort differential pair line lane 3. Multiplexed with TMDS differential pair clock-	134	RSVD (Differential)	Reserved
135	GND	Power Ground	136	GND	Power Ground
137	DP_LANE1+ / TMDS_LANE1+	DisplayPort differential pair line lane 1 Multiplexed with TMDS differential pair lane1	138	DP_AUX+	DisplayPort auxiliary channel
139	DP_LANE1- / TMDS_LANE1-	DisplayPort differential pair line lane 1 Multiplexed with TMDS differential pair lane1	140	DP_AUX-	DisplayPort auxiliary channel
141	GND	Power Ground	142	GND	Power Ground
143	DP_LANE2+ / TMDS_LANE0+	DisplayPort differential pair line lane 2	144	RSVD (Differential)	Reserved
145	DP_LANE2- / TMDS_LANE0-	DisplayPort differential pair line lane 2	146	RSVD (Differential)	Reserved
147	GND	Power Ground	148	GND	Power Ground
149	DP_LANE0+ / TMDS_LANE2+	DisplayPort differential pair line lane 0 Multiplexed with TMDS differential pair lane2	150	HDMI_CTRL_DAT	DDC based control signal (data) for TMDS device.
151	DP_LANE0- / TMDS_LANE2-	DisplayPort differential pair line lane 0 Multiplexed with TMDS differential pair lane2	152	HDMI_CTRL_CLK	DDC based control signal (clock) for TMDS device.
153	DP_HDMI_HPD#	Hot plug detection for TMDS	154	DP_HPD#	Hot plug detection for DP
155	PCIE_CLK_REF+	PCI Express Reference Clock+	156	PCIE_WAKE#	PCI Express Wake event
157	PCIE_CLK_REF-	PCI Express Reference Clock-	158	PCIE_RST#	Reset Signal for external devices
159	GND	Power Ground	160	GND	Power Ground
161	PCIE3_TX+ (*)	PCI Express Channel 3 Output+	162	PCIE3_RX+ (*)	PCI Express Channel 3 Input+
163	PCIE3_TX- (*)	PCI Express Channel 3 Output-	164	PCIE3_RX- (*)	PCI Express Channel 3 Input-
165	GND	Power Ground	166	GND	Power Ground
167	PCIE2_TX+	PCI Express Channel 2 Output+	168	PCIE2_RX+	PCI Express Channel 2 Input+
169	PCIE2_TX-	PCI Express Channel 2 Output-	170	PCIE2_RX-	PCI Express Channel 2 Input-
171	UART0_TX	Serial Data Transmitter	172	UART0_RTS#	Handshake signal, ready to receive data
173	PCIE1_TX+	PCI Express Channel 1 Output+	174	PCIE1_RX+	PCI Express Channel 1 Input+
175	PCIE1_TX-	PCI Express Channel 1 Output-	176	PCIE1_RX-	PCI Express Channel 1 Input-
177	UART0_RX	Serial Data Receiver	178	UART0_CTS#	Handshake signal, ready to send data

Pin	Signal	Description	Pin	Signal	Description
179	PCIE0_TX+	PCI Express Channel 0 Output+	180	PCIE0_RX+	PCI Express Channel 0 Input+
181	PCIE0_TX-	PCI Express Channel 0 Output-	182	PCIE0_RX-	PCI Express Channel 0 Input-
183	GND	Power Ground	184	GND	Power Ground
185	LPC_AD0	LPC Interface Address Data 0	186	LPC_AD1	LPC Interface Address Data 1
187	LPC_AD2	LPC Interface Address Data 2	188	LPC_AD3	LPC Interface Address Data 3
189	LPC_CLK	LPC Interface Clock	190	LPC_FRAME#	LPC frame indicator
191	SERIRQ (**)	Serialized interrupt	192	LPC_LDRQ# (*)	LPC DMA request
193	VCC_RTC	3V backup cell input	194	SPKR /GP_PWM_OUT2	Output for audio enunciator General Purpose PWM Output
195	FAN_TACHOIN	Fan tachometer input General Purpose Timer In	196	FAN_PWMOUT	Fan speed control (PWM) General Purpose PWM Output
197	GND	Power Ground	198	GND	Power Ground
199	SPI_MOSI (**)	SPI Master serial output/Slave serial input	200	SPI_CS0# (**)	SPI Chip Select 0 Output
201	SPI_MISO (**)	SPI Master serial input/Slave serial output signal	202	SPI_CS1# (*)	SPI Chip Select 1 Output
203	SPI_SCK (**)	SPI Clock Output	204	MFG_NC4	Do not connect on carrier board
205	VCC_5V_SB	+5VDC,Standby ±5%	206	VCC_5V_SB	+5VDC Standby ±5%
207	MFG_NC0	Do not connect on carrier board	208	MFG_NC2	Do not connect on carrier board
209	MFG_NC1	Do not connect on carrier board	210	MFG_NC3	Do not connect on carrier board
211	VCC	Power supply +5VDC ±5%	212	VCC	Power supply +5VDC ±5%
213	VCC	Power supply +5VDC ±5%	214	VCC	Power supply +5VDC ±5%
215	VCC	Power supply +5VDC ±5%	216	VCC	Power supply +5VDC ±5%
217	VCC	Power supply +5VDC ±5%	218	VCC	Power supply +5VDC ±5%
219	VCC	Power supply +5VDC ±5%	220	VCC	Power supply +5VDC ±5%
221	VCC	Power supply +5VDC ±5%	222	VCC	Power supply +5VDC ±5%
223	VCC	Power supply +5VDC ±5%	224	VCC	Power supply +5VDC ±5%
225	VCC	Power supply +5VDC ±5%	226	VCC	Power supply +5VDC ±5%
227	VCC	Power supply +5VDC ±5%	228	VCC	Power supply +5VDC ±5%
229	VCC	Power supply +5VDC ±5%	230	VCC	Power supply +5VDC ±5%

Note

The signals marked with asterisk symbol (*) are not supported on the conga-QA4.

On Braswell SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

Bidirectional level shifters have limited driving strength. congatec therefore recommends to route these signals as short as possible.

Table 11 PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0.
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	I PCIE		Not connected by default
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Not connected by default
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock for Lanes 0 to 3.	O PCIE		
PCIE_WAKE#	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I 3.3VSB	PU 10k 3.3VSB	
PCIE_RST#	158	Reset Signal for external devices.	O 3.3V		

Table 12 UART Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
UART0_TX	171	Serial Data Transmitter	O 3.3V		
UART0_RX	177	Serial Data Reciever	I 3.3VSB		
UART0_CTS#	178	Handshake signal, ready to send data	I 3.3VSB		
UART0_RTS#	172	Handshake signal, ready to receive data	O 3.3V		

Table 13 Ethernet Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GBE_MDI0+ GBE_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI1+ GBE_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI2+ GBE_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI3+ GBE_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_CTREF	15	Reference voltage for carrier board Ethernet magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		Not connected
GBE_LINK#	13	Ethernet controller 0 link indicator, active low.	O 3.3VSB PP		
GBE_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB PP		
GBE_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB PP		
GBE_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 3.3VSB PP		

Note

The conga-QA4 can drive GbE LEDs with up to 10mA.

Table 14 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	O 3.3V		up to 10mA

Table 15 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_P0+ USB_P0-	96 94	Universal Serial Bus Port 0 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Can be combined with USB_SSRX0 and USB_SSTX0 signals to create a USB 3.0 port.
USB_P1+ USB_P1-	95 93	Universal Serial Bus Port 1 differential pair. This port may be optionally used as USB client port.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Can be combined with USB_SSRX1 and USB_SSTX1 signals to create a USB 3.0 port..
USB_P2+ USB_P2-	90 88	Universal Serial Bus Port 2 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P3+ USB_P3-	89 87	Universal Serial Bus Port 3 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P4+ USB_P4- USB_SSRX1+ USB_SSRX1-	84 82	Universal Serial Bus Port 4 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path.	I/O I		USB 2.0 compliant. Backwards compatible to USB 1.1. AC coupled off module. **Note:** These pins carry either SuperSpeed or USB 2.0 signals depending on the conga-QA4 variant.
USB_P5+ USB_P5- USB_SSTX1+ USB_SSTX1-	83 81	Universal Serial Bus Port 5 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path	I/O O		USB 2.0 compliant. Backwards compatible to USB 1.1. AC coupled off module. **Note:** These pins carry either SuperSpeed or USB 2.0 signals depending on the conga-QA4 variant.
USB_P6+ USB_P6- USB_SSRX0+ USB_SSRX0-	78 76	Universal Serial Bus Port 6 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path	I PCIE		USB 2.0 compliant. Backwards compatible to USB 1.1. AC coupled off module **Note:** These pins carry either SuperSpeed or USB 2.0 signals depending on the conga-QA4 variant.
USB_P7+ USB_P7- USB_SSTX0+ USB_SSTX0-	77 75	Universal Serial Bus Port 7 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path	O PCIE		USB 2.0 compliant. Backwards compatible to USB 1.1 AC coupled on module. **Note:** These pins carry either SuperSpeed or USB 2.0 signals depending on the conga-QA4 variant.
USB_0_1_OC#	86	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	I 3.3VSB	PU 10k 3.3VSB	
USB_2_3_OC#	85	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	I 3.3VSB	PU 10k 3.3VSB	
USB_4_5_OC#	80	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	I 3.3VSB	PU 10k 3.3VSB	
USB_6_7_OC#	79	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	I 3.3VSB	PU 10k 3.3VSB	
USB_ID*	92	USB ID pin. Configures the mode of the USB Port 1. Refer to the Qseven Design guide for further details.	O Analog		

USB_VBUS#*	91	USB VBUS pin 5V tolerant VBUS resistance to be placed on the module VBUS capacitance to be placed on the carrier board	I 5V Passive Analog		
USB_DRIVE_VBUS*	56	USB power enable pin for USB Port 1. Enables the power for the USB-OTG port on the carrier	O 3.3V CMOS		

Note

**The Intel Braswell SoC does not support USB_OTG functionality*

Table 16 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	43	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I/O 3.3V	PU 100k 3.3V	
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	O 3.3V		
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O 3.3V OD/PP	PU 20k 3.3V	
SDIO_LED	44	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	O 3.3V		Braswell SD Card controller does not provide any SDIO_LED signal. SDIO_LED signal is therefore generated by a logic gate. LED blinking might differ from blinking behavior of other modules.
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I/O 3.3V	PU 100k 3.3V	
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O 3.3V		
SDIO_DAT0 SDIO_DAT1 SDIO_DAT2 SDIO_DAT3 SDIO_DAT4 SDIO_DAT5 SDIO_DAT6 SDIO_DAT7	49 48 51 50 53 52 55 54	SDIO Data lines. These signals operate in push-pull mode.	I/O 3.3V OD/PP	PU 20k 3.3V	Only 4-bit SDIO interface. SDIO_DAT[7:4] are not connected

Note

The 20k pull-ups on the Data and CMD lines are internal Braswell pull-ups. The pull-ups are disabled once a high speed transfer is established.

Table 17 HDA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST# I2S_RST#	61	HD Audio Codec Reset. Multiplexed with I2S Codec Reset.	O 3.3V		
HDA_SYNC I2S_WS	59	HD Audio Serial Bus Synchronization. Multiplexed with I2S Word Select from Codec.	O 3.3V		
HDA_BITCLK I2S_CLK	63	HD Audio 24 MHz Serial Bit Clock from Codec. Multiplexed with I2S Serial Data Clock from Codec.	O 3.3V		
HDA_SDO I2S_SDO	67	HD Audio Serial Data Output to Codec. Multiplexed with I2S Serial Data Output from Codec.	O 3.3V		
HDA_SDI (**) I2S_SDI	65	HD Audio Serial Data Input from Codec. Multiplexed with I2S Serial Data Input from Codec.	I 3.3V	PD 100k	

On Intel Braswell SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

Bidirectional level shifters have limited driving strength. congatec therefore recommends to route these signals as short as possible.

Table 18 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_PPEN	111	Controls panel power enable.	O 3.3V	PD 10k	
LVDS_BLEN	112	Controls panel Backlight enable.	O 3.3V	PD 10k	
LVDS_BLT_CTRL /GP_PWM_OUT0	123	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V	PD 10k	
LVDS_A0+ LVDS_A0- eDP0_TX0+ eDP0_TX0-	99 101	LVDS primary channel differential pair 0. Display Port primary channel differential pair 0.	O LVDS		eDP/DDI signals are AC coupled on the module
LVDS_A1+ LVDS_A1- eDP0_TX1+ eDP0_TX1-	103 105	LVDS primary channel differential pair 1. Display Port primary channel differential pair 1.	O LVDS		eDP/DDI signals are AC coupled on the module
LVDS_A2+ LVDS_A2- eDP0_TX2+ eDP0_TX2-	107 109	LVDS primary channel differential pair 2. Display Port primary channel differential pair 2.	O LVDS		eDP/DDI signals are AC coupled on the module
LVDS_A3+ LVDS_A3- eDP0_TX3+ eDP0_TX3-	113 115	LVDS primary channel differential pair 3. Display Port primary channel differential pair 3.	O LVDS		eDP/DDI signals are AC coupled on the module

LVDS_A_CLK+ LVDS_A_CLK- eDP0_AUX+ eDP0_AUX-	119 121	LVDS primary channel differential pair clock lines. Display Port primary auxiliary channel.	O LVDS		eDP/DDI signals are AC coupled on the module
LVDS_B0+ LVDS_B0- eDP1_TX0+ eDP1_TX0-	100 102	LVDS secondary channel differential pair 0. Display Port secondary channel differential pair 0.	O LVDS		eDP/DDI signals are AC coupled on the module
LVDS_B1+ LVDS_B1- eDP1_TX1+ eDP1_TX1-	104 106	LVDS secondary channel differential pair 1. Display Port secondary channel differential pair 1.	O LVDS		eDP/DDI signals are AC coupled on the module
LVDS_B2+ LVDS_B2- eDP1_TX2+ eDP1_TX2-	108 110	LVDS secondary channel differential pair 2. Display Port secondary channel differential pair 2.	O LVDS		eDP/DDI signals are AC coupled on the module
LVDS_B3+ LVDS_B3- eDP1_TX3+ eDP1_TX3-	114 116	LVDS secondary channel differential pair 3. Display Port secondary channel differential pair 3.	O LVDS		eDP/DDI signals are AC coupled on the module
LVDS_B_CLK+ LVDS_B_CLK- eDP1_AUX+ eDP1_AUX-	120 122	LVDS secondary channel differential pair clock lines. Display Port secondary auxiliary channel.	O LVDS		eDP/DDI signals are AC coupled on the module
LVDS_DID_CLK /GP2_I2C_CLK	127	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus clock line.	I/O 3.3V OD	PU 2.49k 3.3V	Used as DDI1_DDC_SCL for variants that do not support LVDS.
LVDS_DID_DAT /GP2_I2C_DAT	125	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus data line.	I/O 3.3V OD	PU 2.49k 3.3V	Used as DDI1_DDC_SDA for variants that do not support LVDS.
LVDS_BLC_CLK eDP1_HPD#	128	Control clock signal for external SSC clock chip. If the primary functionality is not used, it can be used as an embedded DisplayPort secondary Hotplug detection.	I/O 3.3V OD	PU 10k 3.3V	Not supported on variants that provide LVDS. (e)DP1_HPD# for variants that do not support LVDS.
LVDS_BLC_DAT eDP0_HPD#	126	Control data signal for external SSC clock chip. If the primary functionality is not used, it can be used as an embedded DisplayPort primary Hotplug detection.	I/O 3.3V OD	PU 10k 3.3V	Not supported on variants that provide LVDS. (e)DP0_HPD# for variants that do not support LVDS.

Table 19 DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP_LANE3+ DP_LANE3-	131 133	DisplayPort differential pair lines lane 3 (Shared with TMDS_CLK+ and TMDS_CLK-)	O PCIE		AC coupled on module.
DP_LANE2+ DP_LANE2-	143 145	DisplayPort differential pair lines lane 2 (Shared with TMDS_LANE0+ and TMDS_LANE0-)	O PCIE		AC coupled on module.
DP_LANE1+ DP_LANE1-	137 139	DisplayPort differential pair lines lane 1 (Shared with TMDS_LANE1+ and TMDS_LANE1-)	O PCIE		AC coupled on module.
DP_LANE0+ DP_LANE0-	149 151	DisplayPort differential pair lines lane 0 (Shared with TMDS_LANE2+ and TMDS_LANE2-)	O PCIE		AC coupled on module.
DP_AUX+ DP_AUX-	138 140	Auxiliary channel used for link management and device control. Differential pair lines.	I/O PCIE		
DP_HPD#	154	Hot plug detection signal that serves as an interrupt request.	I 3.3V	PU 100k 3.3V.	Supports open drain and PushPull driver. Onboard PU is protected with a diode

Note

The DisplayPort signals are shared with TMDS signals.

Table 20 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	
TMDS_CLK+ TMDS_CLK-	131 133	TMDS differential pair clock lines. (Shared with DP_LANE3- and DP_LANE3+)	O TMDS		Passive level shifter shall use PD 620R.
TMDS_LANE0+ TMDS_LANE0-	143 145	TMDS differential pair lines lane 0. (Shared with DP_LANE2- and DP_LANE2+)	O TMDS		Passive level shifter shall use PD 620R.
TMDS_LANE1+ TMDS_LANE1-	137 139	TMDS differential pair lines lane 1. (Shared with DP_LANE1- and DP_LANE1+)	O TMDS		Passive level shifter shall use PD 620R.
TMDS_LANE2+ TMDS_LANE2-	149 151	TMDS differential pair lines lane 2. (Shared with DP_LANE0- and DP_LANE0+)	O TMDS		Passive level shifter shall use PD 620R.
HDMI_CTRL_CLK	152	DDC based control signal (clock) for TMDS device.	I/O 3.3V OD	PU 2.49k 3.3V	Level shifter FET and 2.2k PU to 5V shall be placed between module and TMDS connector.
HDMI_CTRL_DAT	150	DDC based control signal (data) for TMDS device.	I/O 3.3V OD	PU 2.49k 3.3V	Level shifter FET and 2.2k PU to 5V shall be placed between module and TMDS connector.
DP_HDMI_HPD#	153	Hot plug active low detection signal that serves as an interrupt request.	I 3.3V	PU 100k 3.3V	Supports open drain and PushPull Driver. Onboard PU is protected with a diode

Note

The conga-QA4 does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.

Table 21 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	185 186 187 188	Multiplexed Command, Address and Data (LPC_AD[0..3])	I/O 3.3V		
LPC_FRAME#	190	LPC frame indicates the start of a new cycle or the termination of a broken cycle.	I/O 3.3V		
LPC_LDRQ#	192	LPC DMA request.	I/O 3.3V	PU 10k	Not supported.
LPC_CLK	189	LPC clock	I/O 3.3V		25 MHz by default.
SERIRQ (**)	191	Serialized Interrupt.	I/O 3.3V		

Note

On Intel Braswell SoC, the signal marked with asterisks (**) has a voltage level that is different from the level defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

Bidirectional level shifters have limited driving strength. congatec therefore recommends to route these signals as short as possible.

The conga-QA4 does not support GPIOs on the LPC interface.

Table 22 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_MOSI (**)	199	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	O 3.3VSB		
SPI_MISO (**)	201	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	I 3.3VSB		
SPI_SCK (**)	203	SPI clock output.	O 3.3VSB		
SPI_CS0# (**)	200	SPI chip select 0 output.	O 3.3VSB		
SPI_CS1#	202	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	O 3.3VSB		Not connected

Note

The SPI interface is for external BIOS only.

On Intel Braswell SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

Bidirectional level shifters have limited driving strength. congatec therefore recommends to route these signals as short as possible.

Table 23 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	129	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	O 3.3V		Not connected
CAN0_RX	130	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	I 3.3V		Not connected

Table 24 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	211-230	Power Supply +5VDC ±5%.	P		
VCC_5V_SB	205-206	Standby Power Supply +5VDC ±5%.	P		
VCC_RTC	193	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.5 - 3.3 V).	P		
GND	1, 2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198	Power Ground.	P		

Table 25 Power Control Signal Descriptions

Signal	Pin #	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	26	High active input for the Qseven® module indicates that power from the power supply is ready.	I 5V	PU 1M 5V	
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	

Table 26 Power Management Signal Descriptions

Signal	Pin #	Description of Power Management signals	I/O	PU/PD	Comment
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB OD	PU 10k 3.3VSB	
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	I 3.3VSB	PU 10k 3.3VSB	
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	I 3.3VSB	PU 10k 3.3VSB	
SUS_STAT#	19	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3VSB		
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	O 3.3VSB		
SUS_S5#	16	S5 State: This signal indicates S4 or S5 (Soft Off) state.	O 3.3VSB		
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	

Table 27 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	I 3.3V	PU 10k 3.3V	
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	O 3.3V		
GP0_I2C_CLK	66	Clock line of I²C bus.	I/O 3.3V OD	PU 2.49k 3.3V	
GP0_I2C_DAT	68	Data line of I²C bus.	I/O 3.3V OD	PU 2.49k 3.3V	
GP1_SMB_CLK	60	Clock line of System Management Bus.	I/O 3.3VSB OD	PU 10k 3.3VSB	10k PU in isolated state. 2k0 PU in connected state.
GP1_SMB_DAT	62	Data line of System Management Bus.	I/O 3.3VSB OD	PU 10k 3.3VSB	10k PU in isolated state. 2k0 PU in connected state.
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	I/O 3.3VSB OD	PU 10k 3.3VSB	10k PU in isolated state. 2k0 PU in connected state.
SPKR /GP_PWM_OUT2	194	Primary functionality is output for audio enunciator, the "speaker" in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		

BIOS_DISABLE# /BOOT_ALT#	41	Module BIOS disable input signal. Pull low to disable module's onboard BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a bootloader.	I 3.3VSB	PU 10k 3.3VSB	
RSVD	132,134, 144, 146, 154	Do not connect	NC		
GP_1-Wire_Bus	124	General Purpose 1-Wire bus interface.	I/O 3.3V		Not connected

Table 28 Manufacturing Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
MFG_NC0	207	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC1	209	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC2	208	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC3	210	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC4	204	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes.	NA	NA	

Note

The carrier board must not drive the MFG_NC-pins or have pull-up or pull-down resistors implemented for these signals.

Table 29 Thermal Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I 3.3V	PU 100k 3.3V	
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off).	O 3.3V		

Table 30 Fan Control Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT	196	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. .	O 3.3V	PU 10k 3.3V	
FAN_TACHOIN	195	Primary functionality is fan tachometer input.	I 3.3V	PU 10k 3.3V	

Table 31 Onboard Camera Interface Signal Descriptions

Signal	Pin #	Description	I/O Type	Comment
CAM_PWR	1	3.3V +/- 5% supply voltage to power the camera device	3.3V O	
CAM_PWR	2	3.3V +/- 5% supply voltage to power the camera device	3.3V O	
CAM0_CSI_D0+	3	CSI2 Camera 0 Data Lane 0+	I	
CAM0_CSI_D0-	4	CSI2 Camera 0 Data Lane 0-	I	
GND	5			Ground
CAM0_CSI_D1+	6	CSI2 Camera 0 Data Lane 1+	I	
CAM0_CSI_D1-	7	CSI2 Camera 0 Data Lane 1-	I	
GND	8			Ground
CAM0_CSI_D2+	9	CSI2 Camera 0 Data Lane 2+	I	
CAM0_CSI_D2-	10	CSI2 Camera 0 Data Lane 2-	I	
CAM0_RST#	11	Camera 0 Reset (low active)	CMOS 1.8V	
CAM0_CSI_D3+	12	CSI2 Camera 0 Data Lane 3+	I	
CAM0_CSI_D3-	13	CSI2 Camera 0 Data Lane 3-	I	
GND	14			Ground
CAM0_CSI_CLK+	15	CSI2 Camera 0 Differential Clock+ (Strobe)	I	
CAM0_CSI_CLK-	16	CSI2 Camera 0 Differential Clock- (Strobe)	I	
GND	17			Ground
CAM0_I2C_CLK	18	Camera 0 Control Interface, CLK. (I²C like interface)	CMOS 1.8V OD	
CAM0_I2C_DAT	19	Camera 0 Control Interface, DATA. (I²C like interface)	CMOS 1.8V OD	

CAM0_ENA#	20	Camera 0 Enable (low active)	CMOS 1.8V	
MCLK	21	Master Clock. May be used by Cameras to drive it's internal PLL Frequency range: 6...27 MHz	CMOS 1.8V O	
CAM1_ENA#	22	Camera 1 Enable (low active)	CMOS 1.8V	
CAM1_I2C_CLK	23	Camera 1 Control Interface, CLK. (I²C like interface)	CMOS 1.8V OD	
CAM1_I2C_DAT	24	Camera 1 Control Interface, DATA. (I²C like interface)	CMOS 1.8V OD	
GND	25			Ground
CAM1_CSI_CLK+	26	CSI2 Camera 1 Differential Clock+ (Strobe)	I	
CAM1_CSI_CLK-	27	CSI2 Camera 1 Differential Clock- (Strobe)	I	
GND	28			Ground
CAM1_CSI_D0+	29	CSI2 Camera 1 Data Lane 0+	I	
CAM1_CSI_D0-	30	CSI2 Camera 1 Data Lane 0-	I	
CAM1_RST#	31	Camera 1 Reset (low active)	CMOS 1.8V	
CAM1_CSI_D1+	32	CSI2 Camera 1 Data Lane 1+	I	
CAM1_CSI_D1-	33	CSI2 Camera 1 Data Lane 1-	I	
GND	34			Ground
CAM0_GPIO	35	GPIO for Camera 0	CMOS 1.8V	
CAM1_GPIO	36	GPIO for Camera 1	CMOS 1.8V	

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-QA4 module is functionally identical with a standard PC/AT. The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.1.1 LPC Bus

On the conga-QA4, the Platform Controller Hub (PCH) acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCH and the LPC Bus.

Table 32 IO Space Ranges

Some fixed I/O space ranges seen by the processor are listed below:

Device	IO Address
8259 Master	20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39h, 3Ch-3Dh
8254s	40h-43h, 50h-53h
Ps2 Control	60h, 64h
NMI Controller	61h, 63h, 65h, 67h
RTC	70h-77h
Port 80h /LPC Bus	80h-8Fh
Init Register	92h
8259 Master	A0h- A1h, A4h-A5h, A8h-A9h, Ach-ADh, B0h-B1h, B4h-B5h, B8h-B9h, BCh-BDh, 4D0h-4D1h
PCU UART	3F8h-3FFh
Reset Control	CF9h
Active Power Management	B2h-B3h

Some of these ranges are used by a Super I/O if implemented on the carrier board or are occupied by the Qseven on-module UARTs if these are enabled in the setup. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 33 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	SoC Transaction Router
00h	02h	00h	Graphics and Display
00h	03h	00h	IPS Camera
00h	10h	00h	MMC Port[3]
00h	12h	00h	SD Port[3]
00h	13h	00h	SATA
00h	14h	00h	xHCI USB
00h	18h	00h	Serial I/O DMA[3]
00h	18h	03h	I2C Port 3[3]
00h	18h	04h	I2C Port 4[3]
00h	1Ah	00h	Trusted Execution Engine
00h	1Bh	00h	HD Audio
00h	1Ch	00h	PCI Express Root Port 0[1]
00h	1Ch	01h	PCI Express Root Port 1[1]
00h	1Ch	02h	PCI Express Root Port 2[1]
00h	1Ch	03h	PCI Express Root Port 3[1]
00h	1Eh	00h	Serial I/O DMA 2[3]
00h	1Eh	03h	Serial I/O HSUART Port 1[3]
00h	1Fh	00h	LPC: Bridge to Intel Legacy Block
00h	1Fh	03h	SMBus Port
03h	00h	00h	Intel® I211 Ethernet Network

Note

[1] The PCI Express Ports are visible only if they are set to "Enabled" in the BIOS setup program and a device is attached to the corresponding PCI Express port on the carrier board.

[2] The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on the actual configuration of the hardware.

[3] Disabled by default in the BIOS setup.

9.3 PCI Interrupt Routing Map

Table 34 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line [1]	APIC Mode IRQ	Graphic	SD Card	SATA	XHCI	eMMC 4.5 Port	TXE	HD Audio	PCI-EX Root Port 0	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	SMBus Port	I211 Ethernet Network
A	INTA	16	x	x	x	x	x	x	x	x					x [2]
B	INTB	17									x			x	x [3]
C	INTC	18										x			x [4]
D	INTD	19											x		x [5]
E		20													
F		21													
G		22													
H		23													

Note

[1] *These interrupt lines are virtual (message based).*

[2] *Interrupt used by single function PCI Express devices (INTA).*

[3] *Interrupt used by multifunction PCI Express devices (INTB).*

[4] *Interrupt used by multifunction PCI Express devices (INTC).*

[5] *Interrupt used by multifunction PCI Express devices (INTD).*

9.4 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.5 SM Bus

System Management (SM) bus signals are connected to the Intel® Brasswell SoC and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject, contact congatec technical support.

10 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

10.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <ESC> key during POST.

10.1.1 Boot Selection Popup

Press the <F11> key during POST to access the Boot Selection Popup menu. A selection menu displays immediately after POST, allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

10.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar, left frame and right frame. The menu bar is shown below:

Main	Advanced	Chipset	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

10.3 Main Setup Screen

When you first enter the BIOS setup, you will see the main setup screen. The main setup screen reports BIOS, processor, memory and board information and is for configuring the system date and time. You can always return to the main setup screen by selecting the 'Main' tab.

Feature	Options	Description
Main BIOS Version	No option	Displays the main BIOS version.
OEM BIOS Version	No option	Displays the additional OEM BIOS version.
Build Date	No option	Displays the date the BIOS was built.
Product Revision	No option	Displays the hardware revision of the board.
Serial Number	No option	Displays the serial number of the board.
BC Firmware Revision	No option	Displays the firmware revision of the congatec board controller.
MAC Address	No option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	No option	Displays the number of boot ups. **Note:** The value is limited to 16777215.
Running Time	No option	Displays the board-runtime in hours. **Note:** The value is limited to 65535.
Access Level	No option	Displays the user's privilege level.
Microcode Patch	No option	Displays the processor's microcode revision.
Total Memory	No option	Displays total amount of low voltage DDR3 on the system.

Feature	Options	Description
Intel® GOP Driver	No option	Displays the GOP driver version.
Sec RC Version	No option	Displays the SEC revision.
TXE FW Version	No option	Displays the Trusted Execution Environment (TXE) firmware revision.
System Language	English	Displays the default system language.
System Date	Day of week, month/day/year	Specifies the current system date **Note:** The date is in month/day/year format.
System Time	Hour:Minute:Second	Specifies the current system time. **Note:** The time is in 24-hour format.

10.4 Advanced Setup

Select the advanced tab from the setup menu to enter the advanced BIOS setup screen. The menu is used for setting advanced features and only features described within this user's guide are listed.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Watchdog				
	Hardware Health Monitoring				
	Graphics				
	Intel® I210 Gigabit Network				
	Driver Health				
	Trusted Computing				
	RTC Wake				
	Module Serial Ports				
	Reserve Legacy Interrupt				
	ACPI				
	Super IO				
	Serial Port Console Redirection				
	CPU				
	PPM Configuration				
	Thermal Configuration				
	SATA				
	LPSS & SCC Configuration				
	PCI & PCI Express				
	UEFI Network Stack				

10.4.1 Watchdog Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Set the timeout value for the POST watchdog. The watchdog is only active during the POST of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup of the boot selection menu or while waiting for the setup password.
Runtime Watchdog	**Disabled** One-time Trigger Single Event Repeated Event	Select the operating mode of the runtime watchdog: 'One-time Trigger' - Disables watchdog after first trigger. 'Single Event' - Executes every stage only once before the watchdog is disabled. 'Repeated Event' - Executes last stage repeatedly until reset. **Note:** This watchdog will be initialized just before the operating system starts booting.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	The runtime watchdog is delayed for the selected time. **Note:** Use this feature to ensure that the operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Select the type of event that will be generated when timeout 1 is reached.

Feature	Options	Description
Event 2	**Disabled** ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 3 is reached.
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Set the timeout value for the first stage watchdog event.
Timeout 2	Same as 'Timeout 1'	Same as 'Timeout 1'.
Timeout 3	Same as 'Timeout 1'	Same as 'Timeout 1'.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. This feature performs a critical but orderly operating system shutdown or restart.

Note

In ACPI mode, it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason, the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the operating system to shut down properly.

For Restart: An ACPI fatal error is reported to the OS.

10.4.2 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	No option	Displays the CPU temperature in °C.
Board Temperature	No option	Displays the board temperature in °C.
5V Standard	No option	Displays the actual voltage of the 5V standard power supply.
5V Standby	No option	Displays the actual voltage of the 5V standby power supply.
Input Current (5V Standard)	No option	Displays the actual current of the 5V Standard power supply.
CPU Fan Speed	No option	Displays the CPU fan speed in RPM.
Fan PWM Frequency Mode	Low Frequency **High Frequency**	Select fan PWM base frequency mode: 'Low frequency' - 35.3Hz. 'High frequency' - 22.5kHz.
Fan PWM Frequency (kHz)	1 - 63	Select fan PWM base in kHz. Default: 31 **Note:** This feature is only visible in high frequency mode.
Fan PWM Speed Settings	0% 10% 25% 40% 50% 60% 75% 90% **100%**	Set maximum fan speed during boot up in percentage of the supported maximum fan speed.

10.4.3 Graphics Submenu

Feature	Options	Description
Active LFP Configuration	No Local Flat Panel **Integrated LVDS**	Select the active local flat panel (LFP) configuration.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes', the BIOS will use the EDID™ data set in an external EEPROM to configure the LFP. In case it cannot be found, the data set selected under 'Local Flat Panel Type' will be used.
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x18 (01Fh) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x800 1x18 (01Eh) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 2x24 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose 'Auto' to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID™ data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. **Note:** Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.
Backlight Inverter Type	None **PWM** I2C	Select the type of backlight inverter: 'PWM' - IGD PWM signal. 'I2C' - I2C backlight inverter device connected to the video I²C bus.
PWM Inverter Polarity	**Normal** Inverted	Select PWM inverter polarity. **Note:** This feature is only visible if the 'Backlight Inverter Type' is set to 'PWM'.
PWM Inverter Frequency (Hz)	**200** - 40000	Set the PWM inverter frequency in Hz. **Note:** This feature is only visible if the 'Backlight Inverter Type' is set to 'PWM'.
Backlight Setting	0% 10% 25% 40% 50% 60% 75% 90% **100%**	Set backlight value in percentage of the maximum setting.

Feature	Options	Description
Inhibit Backlight	**No** Permanent Until End Of POST	Select whether the backlight enable signal should be activated when the panel is activated, remain inhibited until the end of BIOS POST, or remain inhibited permanently.
Force LVDS Backlight	**No** Yes	If set to "Yes", this feature forces LVDS enable and LVDS VDD signals unconditionally
LVDS SSC	**Disabled** 0.5% 1.0% 1.5% 2.0% 2.5%	Select LVDS spread-spectrum clock modulation depth. **Note:** This feature performs center spreading with a fixed modulation frequency of 32.9kHz.
Digital Display Interface 1	**Auto Selection** Disabled DisplayPort HDMI™/DVI	Select the output type of the DDI 1.

10.4.4 Intel® I211 Gigabit Network Connection Submenu

Feature	Options	Description
► NIC Configuration	Submenu	Configure Boot Protocol, Wake on LAN, Link Speed and VLAN.
Blink LEDs	**0**	Identify the physical network port by blinking the associated LED.
UEFI Driver	No option	Displays the UEFI Driver version.
Adapter PBA	No option	Displays the Adapter PBA.
Chip Type	No option	Displays the type of the Chip.
PCI Device ID	No option	Displays the PCI Device ID.
Bus:Device:Function	No option	
Link Status	**Disconnected**	Displays the Link Status.
MAC Address	No option	Displays the MAC Address.

10.4.4.1 NIC Configuration Submenu

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Set the port speed used for the selected boot protocol.
Wake on LAN	**Enabled** Disabled	Enable or disable the Wake on LAN (WOL) feature

10.4.5 Driver Health Submenu

Feature	Options	Description
▶Intel® PRO/1000	Submenu	Displays health status for the drivers/controllers connected to the system.

10.4.6 Trusted Computing Submenu

Feature	Options	Description
Security Device Support	Disabled **Enabled**	Enable or disable TPM support. **Note:** Please restart your system for the change to take effect.
User Confirmation	Disabled **Enabled**	Enable or disable user confirmation requests for certain transactions.
TPM State	**Disabled** Enabled	Enable or disable TPM chip. **Note:** The system may restart several times during POST to acquire the target state.
Pending operation	**None** Enable Take Ownership Disable Take Ownership TPM Clear	Perform selected TPM chip operation. **Note:** The system may restart several times during POST to perform the selected operation.

10.4.7 RTC Wake Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable this feature to wake the system from S5 using the RTC alarm.
Wake up hour	**0** - 23	Specify the wake up hour. For example: Enter "3" for 3am and "15" for 3pm.
Wake up minute	**0** - 59	Specify the wake up minute.
Wake up second	**0** - 59	Specify the wake up second.

10.4.8 Module Serial Ports Submenu

Feature	Options	Description
Serial Port 0	**Disabled** Enabled	Enable or disable the module's serial port 0.

10.4.9 Reserve Legacy Interrupt Submenu

Feature	Options	Description
Reserve Legacy Interrupt 1, 2, 3	**None** IRQ3 IRQ4 IRQ5 IRQ6 IRQ10 IRQ11 IRQ14 IRQ15	Use this feature to reserve the interrupt for a legacy bus device. **Note:** The selected interrupt will not be assigned to a PCI/PCIe device.

10.4.10 ACPI Submenu

Feature	Options	Description
Enable ACPI Auto Configuration	**Disabled** Enabled	Enable or disable BIOS ACPI auto configuration
Enable Hibernation	Disabled **Enabled**	Enable or disable the system's ability to hibernate (OS S4 sleep state). **Note:** If you want to use this feature, please ensure that the operating system supports it.

Feature	Options	Description
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend.
Lock Legacy Resources	**Disabled** Enabled	Enable this feature to lock legacy resources.
LID Support	Disabled **Enabled**	If this feature is enabled, COM Express LID# signal acts as ACPI lid.
Sleep Button Support	Disabled **Enabled**	If this feature is enabled, COM Express SLEEP# signal acts as ACPI sleep button.

10.4.11 Super IO Submenu

Feature	Options	Description
Super IO Chip	No option	Displays super IO chip.
SIO Clock	24 MHz **48 MHz**	Set super IO base clock.
▶Serial Port 1 Configuration	Submenu	Serial port 1 submenu.
▶Serial Port 2 Configuration	Submenu	Serial port 2 submenu.
▶Parallel Port Configuration	Submenu	Parallel port submenu.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

10.4.11.1 Serial Port 1 Configuration Submenu

Feature	Options	Description
Serial Port	Disabled **Enabled**	Enable or disable serial port (COM).
Device Settings	No option	Displays current device settings.
Change Settings	**Auto** IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11, 12; DMA;	Select an optimal settings for super IO device.

10.4.11.2 Serial Port 2 Configuration Submenu

Feature	Options	Description
Serial Port	**Enabled** Disabled	Enable or disable serial port (COM).
Change Settings	**Use Automatic Settings** IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11, 12; DMA	Select serial port 2 configuration.
Device Mode	**Standard Serial Port Mode** IrDA Active pulse 1.6 uS IrDA Active pulse 3/16 bit time ASKIR Mode	Select the serial port mode.

10.4.11.3 Parallel Port Configuration Submenu

Feature	Options	Description
Parallel Port	Enabled **Disabled**	Enable or disable parallel port (LPT/LPTE).

10.4.12 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
▶Console Redirection Settings	Submenu	Opens console redirection configuration submenu.
▶Legacy Console Redirection Settings	Submenu	Opens 'Legacy Console Redirection Settings' submenu.
Serial Port for Out-of-Band Management / EMS Console Redirection	**Disabled** Enabled	Enable or disable 'Serial Port for Out-of-Band Management / Windows Emergency Management Services'.
▶Console Redirection Settings	Submenu	Opens 'Console Redirection Settings' submenu.

Note

The serial port console redirection can be enabled only if an external Super I/O offering UARTs has been implemented on the carrier board

10.4.12.1 Console Redirection Settings Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Set the terminal type.
Baudrate	9600 19200 38400 57600 **115200**	Set baud rate.
Data Bits	7 **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Set parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Set flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable or disable the VT-UTF8 combination key support for ANSI/VT100 terminals.
Recorder Mode	**Disabled** Enabled	Enable this feature to only send text output over the terminal. **Note:** This feature is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enable or disable extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Select the number of rows and columns for the legacy operating system redirection.
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select the function key and keypad for Putty.
Redirection After BIOS POST	**Enabled** Disabled	If BootLoader is selected, Legacy console redirection is disabled before booting to Legacy OS. Default value is 'Always Enable' which means Legacy console redirection is enabled for Legacy OS.

10.4.12.2 Legacy Console Redirection Settings Submenu

Empty.

10.4.12.3 Console Redirection Settings Out-of-Band Management Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ **VT-UTF8** ANSI	Set the terminal type.
Baudrate	9600 19200 38400 57600 **115200**	Set the baud rate.
Flow Control	**None** Hardware RTS/CTS Sotware Xon/Xoff	
Data Bits	**8**	Set the number of data bits.
Parity	**None**	Set the parity.
Stop Bits	**1**	Set the number of stop bits.

10.4.13 CPU Configuration Submenu

Feature	Options	Description
▶Socket 0 CPU Information	Submenu	Socket specific CPU information.
CPU Speed	No option	Displays the CPU clock frequency.
64-bit	No option	Displays 64-bit support information.
Limit CPUID Maximum	**Disabled** Enabled	If enabled, the processor limits the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. If disabled, the processor returns the actual maximum CPUID input value of the processor when queried. **Note:** Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Bi-directional PROCHOT	Disabled **Enabled**	If enabled, external agents can drive PROCHOT# to throttle the processor. If disabled, a processor thermal sensor trips (either core), the PROCHOT# will be driven.
Intel® Virtualization Technology	Disabled **Enabled**	Enable or disable support for the Intel virtualization technology.

Feature	Options	Description
Power Technology	Disable **Energy Efficient** Custom	Select the power technology schema for the CPU.
EIST	Disabled **Enabled**	Enable or disable Enhanced Intel SpeedStep Technology (EIST).
Turbo Mode	Disabled **Enabled**	Enable or disable turbo mode.
P-State Coordination	**HW_ALL** SW_ALL SW_ANY	Set P-state coordination type.
Package C State Limit	**C1** C3 C6 C7	Set package C-state limit.

10.4.13.1 Socket 0 CPU Information Submenu

Feature	Options	Description
CPU Name	No option	Displays the socket specific CPU name.
CPU Signature	No option	Displays the CPU signature number.
Microcode Patch	No option	Displays the CPU microcode patch number.
Max CPU Speed	No option	Displays the maximal CPU clock frequency.
Min CPU Speed	No option	Displays the minimal CPU clock frequency.
Processor Cores	No option	Displays the number of CPU core on Socket CPU.
Intel® HT Technology	No option	Displays the Intel® HT Technology support information.
Intel® VT-x Technology	No option	Displays the Intel VT-x technology support information.
L1 Data Cache	No option	Displays the Socket L1 data cache information.
L1 Code Cache	No option	Displays the Socket L1 code cache information.
L2 Cache	No option	Displays the Socket L2 cache information.
L3 Cache	No option	Displays the Socket L3 cache information.

10.4.14 PPM Configuration Submenu

Feature	Options	Description
EIST	Disabled **Enabled**	Enable or disable Enhanced Intel SpeedStep Technology (EIST).
CPU C state Report	Disabled **Enabled**	Enable or disable CPU state report to OS.
Max CPU C state	C7 C6 **C1**	Select maximum CPU C-state supported by the CPU.
SOix	**Disabled** Enabled	Enable or disable CPU SOix state support.

10.4.15 Thermal Configuration

Feature	Options	Description
DTS	Enabled **Disabled**	Enable or disable Digital Thermal Sensor (DTS).
Critical Trip Point	0 - **90**	Set the temperature of the ACPI critical trip point at which the operating system will shut the system off.
OS Hibernate Temperature	0 - 110	Set the temperature that causes the operating system to trigger the system to hibernate. Default: 85
Passive Trip Point	0 - 90	Set the temperature of the ACPI passive trip point at which the operating system will begin throttling the processor. Default: 85
Full Speed Fan Trip Point	0 - 90	Set the temperature at which the fan is activated at full speed. Default: 80
Half Speed Fan Trip Point	0 - 90	Set the temperature at which the fan is activated at half speed. Default: 60
Fan Hysteresis	0 - **7**	Set number of degrees for the temperature to decrease before the fan is switched off again.

10.4.16 SATA Submenu

Feature	Options	Description
SATA Controller	**Enabled** Disabled	Enable or disable SATA onboard SATA controller(s).
SATA Mode Selection	**AHCI**	Select SATA controller mode.
SATA Interface Speed	Gen1 **Gen2** Gen3	Select SATA Interface Speed. **Note:** CHV A1 always with Gen1 Speed.
SATA Test Mode	Enabled **Disabled**	Enable only during verification measurements.

Feature	Options	Description
Aggressive LPM Support	**Enabled** Disabled	Enable PCH to aggressively enter link power state.
►Software Feature Mask Configuration	Submenu	
SATA Port 0	**Enabled** Disabled	Enable or disable SATA port 0.
Spin Up Device	Enabled **Disabled**	If enabled for any ports, staggered spin up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
Device Sleep Support	Enabled **Disabled**	Enable or disable device sleep support on that port.
SATA Port 1	**Enabled** Disabled	Enable or disable SATA port 1.
Spin Up Device	Enabled **Disabled**	If enabled for any ports, staggered spin up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise, all drives spin up at boot.
Device Sleep Support	Enabled **Disabled**	Enable or disable device sleep support on that port.

10.4.16.1 Software Feature Mask Configuration Submenu

Feature	Options	Description
HDD Unlock	**Enabled** Disabled	If enabled, indicates that the HDD password unlock in the operating system is enabled.
LED Locate	**Enabled** Disabled	If enabled, indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS.

10.4.17 LPSS & SCC Configuration Submenu

Feature	Options	Description
SCC eMMC Support	**ACPI Mode** PCI Mode Disabled	Enable or disable SCC eMMC support.
eMMC Secure Erase	Enabled **Disabled**	Enable or disable eMMC secure erase support.
SCC SDIO Support (D17:F0)	ACPI Mode PCI Mode **Disabled**	Enable or disable SCC SDIO support

Feature	Options	Description
SCC SD Card Support (D18:F0)	**ACPI Mode** PCI Mode Disabled	Enable or disable SCC SD card support.
SD Card 1.8v Switching Delay	**0** - 999ms	Set SD card 1.8v switching delay.
SD Card 3.3v Discharge Delay	0 - 999ms	Set SD card 3.3v discharge delay. Default: 250
LPSS with GPIO Devices Support	Disabled **Enabled**	If this feature is disabled, all LPSS devices are disabled.
LPSS DMA #1	**ACPI Mode** PCI Mode Disabled	Enable or disable LPSS DMA #1 support.
LPSS DMA #2	**ACPI Mode** PCI Mode Disabled	Enable or disable LPSS DMA #2 Support.
LPSS I2C #3	**ACPI Mode** PCI Mode Disabled	Enable or disable LPSS I2C #3 Support.
Runtime D3 Support	**Enabled** Disabled	Enable or disable Runtime D3 Support.
LPSS I2C #4	ACPI Mode PCI Mode **Disabled**	Enable or disable LPSS I2C #4 Support.
LPSS HSUART #1	**ACPI Mode** PCI Mode Disabled	Enable or disable LPSS HSUART #1 Support.

10.4.18 PCI & PCI Express

Feature	Options	Description
PCI Bus Driver Version	No option	Displays PCI bus driver version.
PCI Latency Timer	**32 PCI Bus Clocks** 64 PCI Bus Clocks 96 PCI Bus Clocks 128 PCI Bus Clocks 160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	Select the value to be programmed into PCI latency timer register.
PCI-X Latency Timer	32 PCI Bus Clocks **64 PCI Bus Clocks** 96 PCI Bus Clocks 128 PCI Bus Clocks 160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	Select the value to be programmed into PCI latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate SERR#.
Above 4G Decoding	**Disabled** Enabled	Enable this feature to decode 64-bit capable devices in Above 4G address space. **Note:** Please ensure that the system supports 64-bit PCI decoding if you want to use this feature.
Don't Reset VC-TC Mapping	**Disabled** Enabled	If the system has virtual channels, software can reset the traffic class mapping through virtual channels to its default state. **Note:** Enabling this feature will not modify VC resources.

10.4.19 UEFI Network Stack

Feature	Options	Description
Network Stack	Enabled **Disabled**	Enable or disable the UEFI network stack.
IPv4 PXE Support	**Enabled** Disabled	If this feature is disabled, IPV4 PXE boot option will not be created.
IPv6 PXE Support	**Enabled** Disabled	If this feature is disabled, IPV6 PXE boot option will not be created.
PXE boot wait time	**0** - 5	Set wait time to press ESC key to abort the PXE boot.
Media detect count	**1** - 50	Set the number of times to check for the presence of media.

10.4.20 CSM & Option ROM Control Submenu

Feature	Options	Description
CSM Support	**Enabled** Disabled	Enable or disable the compatibility support module.
CSM16 Module Version	No option	Displays CSM module version number.
Gate A20 Active	**Upon Request** Always	Configure legacy gate A behavior.
Option ROM Messages	**Force BIOS** Keep Current	Enable or disable option ROM message.
INT19 Trap Response	**Immediate** Postponed	Set BIOS reaction on INT19 trapping: 'Immediate' - Executes the trap right away. 'Postpone' - Executes the trap during legacy boot.
Boot Option Filter	**UEFI and Legacy** Legacy Only UEFI Only	Select which devices / boot loaders the system should boot to.
Network	Do not launch **UEFI only** Legacy only	Select the execution of UEFI and legacy Network option ROMs.
Storage	Do not launch **UEFI only** Legacy only	Select the execution of UEFI and legacy Storage option ROMs.
Video	Do not launch UEFI only **Legacy only**	Select the execution of UEFI and legacy Video option ROMs

Feature	Options	Description
Other PCI Devices	**UEFI only** Legacy only Do not launch	Select the execution of UEFI and legacy option ROMs for any PCI device other than network, video and storage.

10.4.21 Info Report Configuration

Feature	Options	Description
POST Report	**Disabled** Enabled	Enable or disable POST report support.
Delay Time	0 - 10 Until Press ESC	Set POST report time in seconds or to wait until ESC key is pressed.
Error Message Report	**Disabled** Enabled	Enable or disable error message support.
Summary Screen	**Disabled** Enabled	Enable or disable summary screen.
Delay Time	0-10 Until Press ESC	Set summary screen from 0 to 10 seconds or select to wait till ESC key is pressed.

10.4.22 NVMe Submenu

Feature	Options	Description
NVMe controller and Drive Information	No option	

10.4.23 USB Submenu

Feature	Options	Description
USB Module Version	No option	Displays the version of the USB module.
USB Controllers	No option	Displays the available USB controllers.
USB Devices	No option	Displays the detected USB devices.
Legacy USB Support	**Enabled** Disabled Auto	'Enable' - Enables legacy USB support. 'Disable' - Keeps USB devices available only for EFI applications and BIOS setup. 'Auto' - Disables legacy support if no USB devices are connected.
xHCI Hand-off	Enabled **Disabled**	This is a workaround for operating systems without xHCI hand-off support. **Note:** If this feature is enabled, the xHCI ownership change should be claimed by xHCI operating system driver.

Feature	Options	Description
USB Mass Storage Driver Support	Disabled **Enabled**	Enable or disable mass storage driver support.
Port 60/64 Emulation	Disabled **Enabled**	Enable or disable I/O port 60h/64h emulation support. **Note:** Enable this feature for the complete USB keyboard legacy support for non-USB aware operating systems.
USB Transfer Timeout	1 sec 5 sec 10 sec **20 sec**	Set the timeout value for control, bulk, and interrupt transfers.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	Set USB legacy mass storage device start unit command timeout.
Device Power-Up Delay Selection	**Auto** Manual	Select whether the delay time for a USB device to report itself properly to the host controller should be set automatically or manually. If set to 'Auto', the delay is 100ms for a root port or the value is derived from the hub descriptor for a hub port.
Device Power-Up Delay Value	0 - 40	Set power-up delay value in seconds. Default: 5
SanDisk Cruzer Micro 8.01	**Auto** Floppy Forced FDD Hard Disk CD-ROM	Select mass storage device emulation type: 'Auto' - Enumerates devices according to their media format. **Note:** Drives without media will be emulated according to the drive type.

10.4.24 Platform Trust Technology

Feature	Options	Description
fTPM	**Disable** Enable	Enable or disable Trusted Platform Module (TPM) support.

10.4.25 Security Configuration

Feature	Options	Description
TXE HMRFPO	Enable **Disable**	Enable or disable Host ME Region Flash Protection Overwrite (HMRFPO).
TXE Firmware Update	**Enabled** Disabled	Enable or disable firmware update.
TXE EOP Message	**Enabled** Disabled	Enable or disable TXE End of Post (EOP) Message.

10.4.26 Intel® RMT Configuration Submenu

Feature	Options	Description
Intel® RMT Support	**Disabled** Enabled	If this feature is enabled, the Intel® Ready Mode Technology (RMT) SSDT table will be loaded.

10.4.27 PC Speaker Submenu

Feature	Options	Description
Debug Beeps	Disabled **Enabled**	Enable or disable general debug/status beep generation.
Input Device Debug Beeps	**Disabled** Enabled	Enable or disable input device debug beep generation.
Output Device Debug Beeps	**Disabled** Enabled	Enable or disable output device debug beep generation.
USB Driver Beeps	**Disabled** Enabled	Enable or disable USB driver beeps.

10.5 Chipset Setup

Select the 'Chipset' tab from the setup menu to enter the chipset setup screen.

Main	Advanced	Chipset	Boot	Security	Save & Exit
		Processor (Integrated Components)			
		Platform Controller Hub (PCH)			

10.5.1 Processor (Integrated Components) Submenu

Feature	Options	Description
▶Intel IGD Configuration	Submenu	
▶Graphics Power Management Control	Submenu	
▶Memory Configuration Options	Submenu	
Total Memory	No option	Displays the total amount of memory detected by the system
Memory Slot 0	No option	Displays the memory detected by the system on slot 0
Memory Slot 1	No option	Displays the memory detected by the system on Slot 1

Max TOLUD	**2 GB** 3 GB	Select maximum value of TOLUD.

10.5.1.1 Intel® IGD Configuration Submenu

Feature	Options	Description
Internal Graphics Device	**Enabled** Disabled	Enable or disable Internal Graphics Device (IGD).
IGD Turbo	**Auto** Enabled Disabled	Select the IGD turbo feature: 'Auto' - Enables IGD turbo only when SOC steeping is B0 or above.
GFX Boost	Enabled **Disabled**	Enable or disable GFX boost.
PAVC	Disabled **Enabled**	Enable or disable Protected Audio Video Control (PAVC).
PR3	Disabled **Enabled**	Enable or disable PR3. This is a feature for Win 10 only.
DVMT Pre-Allocated	**32M** 64M 96M 128M 160M 192M 224M 256M 288M 320M 352M 384M 416M 448M 480M 512M	Select DVMT 5.0 pre-allocated (fixed) graphics memory size used by the IGD.
DVMT Total Gfx Mem	128MB **256MB** Max	Select DVMT 5.0 total graphic memory size used by the IGD.
Aperture Size	128MB **256MB** 512MB	Select the aperture size.
GTT Size	2MB **4MB** 8MB	Select the GTT size.

Feature	Options	Description
IGD Thermal	Enabled **Disabled**	Enable or disable IGD thermal.
Spread Spectrum clock	**Enabled** Disabled	Enable or disable spread spectrum clock.
WOPCMSZ	**1MB** 2MB 4MB 8MB	Set the size for WOPCMSZ.
ISP Enable/Disable	**Enabled** Disabled	Enable or disable ISP PCI device selection.
ISP PCI Device Selection	ISP PCI Device as B0D2F0 **ISP PCI Device as B0D3F0** ISP PCI Device as B0D3F0 with Virtual ISP B0D2F0	Default setting for ISP for Windows boot is PCI B0D2F0. Default setting for Linux boot is B0D3F0.
PUNIT Power Configuration	Disabled **Enabled**	Enable or disable PUNIT power configuration.
Svid Configuration	**Platform Defaults** Svid Config 0 Svid Config 1 Svid Config 3 Svid Config 4 BSW I2C PMIC Config	Select the right SVID configuration.

10.5.1.2 Graphics Power Management Control Submenu

Feature	Options	Description
RC6 (Render Standby)	**Enabled** Disabled	Enable or disable render standby support.
Power Meter Lock	**Enabled** Disabled	Enable or disable power meter lock.

10.5.1.3 Memory Configuration Options Submenu

Feature	Options	Description
Rank Margin Tool EV Mode	**Disabled** Enabled	Enable or disable rank margin tool print out message support.
DDR DVFS	Disabled **Enabled**	Enable or disable DDR dynamic voltage and frequency scaling in MRC.
Memory Frequency Override	**Disabled** Enabled	Enable to allow override of memory frequency parameters that are automatically obtained from DDR3 DIMM SPD. **Note:** May cause memory instability if the selected frequency is not supported by the memory device. This option has no effect on systems configured without 'UseDimmSpd' option.
Frequency A selection	Auto 800 1067 **1600** 800(SKU333) 1000(SKU333) 1333(SKU333) 900(SKU360) 1800(SKU360) 933(SKU373) 1866(SKU373)	Select frequency A selection.
Frequency B selection	Auto **1067** 800(SKU333) 1000(SKU333) 900(SKU360) 933(SKU373)	Select frequency B selection (minimum DDR DVFS frequency).
Auto Detect LPDDR3 DRAM	Disabled **Enabled**	Enable or disable automatic detection of LPDDR3 DRAM parameters.
LPDDR3 Chip Select	**1 Rank** 2 Ranks	Select LPDDR3 chip rank **Note:** 'Auto Detect' must be disabled to use this option.
Channel selection	Auto, **Single**, Dual	Select number of channels.
Channel Selection Bit 3:0	0 - 9 A - F	Set channel selection bit 3:0. Default: 2
Channel Selection 4	0 - 9 A - F	BMISC Channel select 4 for channel hashing. Default: 1
Bank Address Hashing	Disabled **Enabled**	Enable or disable bank address hashing.
Rank Select Interleaving	Disabled **Enabled**	Enable or disable rank select interleaving.
Dynamic Self Refresh	Disabled **Enabled**	Enable or disable PUNIT driven DUNIT DDR dynamic self refresh.

Feature	Options	Description
DRAM PM5	Disabled **Enabled**	Enable or disable DRAM PM5 PUNIT configuration.
DDR3 2N Mode	**Disabled** Enabled	Enable to set the DDR3 mode to 2N. 1N mode is used by default.
RX Power Training	**Enabled** Disabled	Enable or disable RX Power Training.
TX Power Training	**Enabled** Disabled	Enable or disable TX Power Training.
MRC Fast Boot	**Enabled** Disabled	Enable or disable MRC fast boot. If disabled, forces MRC training.
Scrambler	**Enabled** Disabled	Enable or disable scrambler.
DRP Lock	Disabled **Enabled**	Enable or disable DRP lock.
REUT Lock	Disabled **Enabled**	Enable or disable REUT lock.
RH Prevention	**Disabled** Enabled	This feature prevents specific row hammer attacks. **Note:** If enabled, this function increases the average time between sending REF commands to DRAM.

10.5.2 Platform Controller Hub (PCH) Submenu

Feature	Options	Description
▶ Security Configuration	Submenu	Security Configuration Submenu.
▶ Azalia Configuration	Submenu	Azalia HD Audio Submenu.
▶ USB Configuration	Submenu	USB Submenu.
▶ PCI Express Configuration	Submenu	PCI Express Configuration Submenu.
Serial IRQ Mode	Quiet **Continuous**	Select IRQ Serial Mode.
CLKRUN# Logic	Enable **Disable**	Enable the CLKRUN# logic to stop the LPC clocks when possible. Requires Serial IRQ Mode to be set to Quiet as well.
Isolate SMBus Segments	**Never** During POST Always	Isolate the off-module/external SMBus segment from the on-module SMBus segment. This feature is a workaround for non spec conform external SMBus devices.

10.5.2.1 Security Configuration Submenu

Feature	Options	Description
RTC Lock	Disabled **Enabled**	Enable or disable bytes 38h-3Fh in the upper and lower 128-byte bank of RTC RAM lockdown.
Global SMI Lock	**Enabled** Disabled	Enable or disable SMI lock.

10.5.2.2 Azalia Configuration Submenu

Feature	Options	Description
LPE Audio Support	**Disabled** PCI Mode ACPI Mode	Select LPE audio support.
Audio Controller	**Enabled** Disabled	Enable or disable audio controller.
Azalia Vci Enable	**Enabled** Disabled	Enable or disable Azalia Vci.
Azalia Docking Support Enable	Enabled **Disabled**	Enable or disable Azalia Docking support.
Azalia PME Enable	**Enabled** Disabled	Enable or disable Azalia PME support.
Azalia HDMI™ Codec	**Enabled** Disabled	Enable or disable Azalia HDMI™ codec.
HDMI™ Port B	**Enabled** Disabled	Enable or disable HDMI™ port B audio.
HDMI™ Port C	**Enabled** Disabled	Enable or disable HDMI™ port C audio.
HDMI™ Port D	**Enabled** Disabled	Enable or disable HDMI™ port D audio.

10.5.2.3 USB Configuration Submenu

Feature	Options	Description
xHCI Mode	**Enabled** Disabled	Mode of xHCI controller operation.
SSIC Support Enable	**Disabled** Enabled	Enable or disable SSIC support.
SSIC Init Sequence	**SSIC Initialization Sequence 1** SSIC Initialization Sequence 2	Select sequence 1 for Windows. Select sequence 2 for Android.
SSIC Port 1	Enabled **Disabled**	Enable or disable SSIC port 1.
SSIC Port 2	Enabled **Disabled**	Enable or disable SSIC port 2.
HSIC Port 1	**Enabled** Disabled	Enable or disable HSIC port 1.
HSIC Port 2	**Enabled** Disabled	Enable or disable HSIC port 2.
USB2 PHY Power Gating	**Auto** Disabled Enabled	Select USB2 PHY power gating.
USB3 PHY Power Gating	**Auto** Disabled Enabled	Select USB3 PHY power gating.

10.5.2.4 PCI Express Configuration Submenu

Feature	Options	Description
▶ PCIE Express Root Port 1	Submenu	
▶ PCIE Express Root Port 2	Submenu	
▶ PCIE Express Root Port 3	Submenu	
▶ PCIE Express Root Port 4	Submenu	
▶ PCIE Express S0ix Settings	Submenu	
Native PCI Express Support	Disabled **Enabled**	Enable or disable native operating system PCIe support

10.5.2.5 PCIE Express Root Port 1,2,3 & 4

Feature	Options	Description
PCI Express Root Port 1	**Enabled** Disabled	Enable or disable the PCIe root port.
ASPM	Auto **Disabled** L0s, L1s, L0sL1	Select PCIe Active State Power Management (ASPM) setting.
URR	**Disabled** Enabled	Enable or disable PCIe Unsupported Request Reporting (URR).
FER	**Disabled** Enabled	Enable or disable PCIe device Fatal Error Reporting (FER).
NFER	**Disabled** Enabled	Enable or disable PCIe device Non-Fatal Error Reporting (NFER).
CER	**Disabled** Enabled	Enable or disable PCIe device Correctable Error Reporting (CER).
SEFE	**Disabled** Enabled	Enable or disable root PCIe System Error on Fatal Error (SEFE).
SENFE	**Disabled** Enabled	Enable or disable root PCIe System Error on Non-Fatal Error (SENFE).
SECE	**Disabled** Enabled	Enable or disable root PCIe System Error on Correctable Error (SECE).
PME SCI	Disabled **Enabled**	Enable or disable PCIe Power Management Event (PME) SCI.
Ext Sync	**Disabled** Enabled	Enable or disable express ext sync.
PCIe Speed	**Auto** Gen2 Gen1	Set PCIe speed. **Note:** Always use CHV A1 with Gen 1 speed.
Detect Non-compliant Device	**Disabled** Enabled	Enable this feature to detect some non-compliant PCIe devices on the PEG port. **Note:** POST takes more time if this feature is enabled.
L1 Substates	Disabled L1.1 L1.2 **L1.1 & L1.2**	Select PCIe L1 substates setting.
Non-Common Clock With SSC Enabled Mode	Enabled **Disabled**	Enable this feature if the root port is operating at non-common clock.
Transmitter Half Swing	Enabled **Disabled**	Enable or disable transmitter half swing.
Tx Eq Deemphasis Selection	3.5dB, **6dB**	Set the level of de-emphasis for an upstream component.

10.5.2.6 PCIE Express S0ix Settings Submenu

Feature	Options	Description
D0 S0ix Policy	**PCIe RC shall be in D3** S0i1 is the deepest S0ix state PCIe RC in in D0 when entering S0ix Reserved	Set PCIe D0 S0ix policy.
Evaluate CLKREQ State	**Enabled** Disabled	Enable or disable evaluation of CLKREQ state.
CLKREQ# Enable	**CLKREQ# [0]** CLKREQ# [1] CLKREQ# [2] CLKREQ# [3]	Evaluate CLKREQ# [x] during PCIe in D0 S0ix entry and exit criteria checking.
S0ix LTR Threshold (Latency Scale)	1ns 32ns **1024ns** 32,768ns 1,048,576ns 33,554,321ns	Set PCIe S0ix LTR threshold for latency scale..
PCIe LTR Threshold (Latency Value)	**150**	Set the PCIe S0ix LTR threshold latency value. This value is multiplied by the latency scale.

10.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

10.6.1 Security Settings

Feature	Options	Description
BIOS Password	No options	Set BIOS password.
BIOS Lock	**Enabled** Disabled	Enable or disable the BIOS lock feature
BIOS Update and Write Protection	**Disabled** Enabled	Enable or disable BIOS update
▶Secure Boot Menu	Submenu	Customizable secure boot settings.

10.6.2 Secure Boot Menu

Feature	Options	Description
System Mode	No options	Shows system mode.
Secure Boot	No options	Shows secure boot status.
Vendor Keys	No options	Shows vendor keys status.
Secure Boot	**Disabled** Enabled	Secure boot can be enabled if the system is running in user mode with enrolled Platform Key (PK) and when CSM function is disabled.
Secure Boot Mode	Standard **Custom**	Select secure boot mode.
▶Key Management	Submenu	

10.6.2.1 Key Management Submenu

Feature	Options	Description
Provision Factory Default Keys	**Disabled** Enabled	Enable this feature to install factory default secure boot keys when system is in setup mode.
▶Enroll all Factory Default Keys		Force system to user mode and install all factory default keys.
▶Platform Key(PK)		
▶Key Exchange Keys		
▶Authorized Signatures		
▶Forbidden Signatures		
▶Authorized TimeStamps		

10.7 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.7.1 Boot Settings Configuration

Feature	Options	Description
Setup Prompt Timeout	0 - 65535	Set number of seconds to wait for setup activation key. Default: 1 '65535' - Waits indefinetly (0xFFFF). '0' - Does not wait (not recommended).
Bootup NumLock State	**On** Off	Set the keyboard numlock state.
Quiet Boot	**Disabled** Enabled	'Disabled' - Displays normal POST diagnostic messages. 'Enabled' - Displays OEM logo instead of POST messages. **Note:** The default OEM logo is a dark screen.
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Set boot priority: 'Device Based' - Set boot priority from a list of currently detected devices. 'Type Based' - Set boot priority from a list of device types even if they are not connected yet.
Boot Option Sorting Method	**Legacy First** UEFI First	Set boot option sorting method: 'Legacy First' - Tries all legacy boot option first before first UEFI boot option. 'UEFI First' - Tries all UEFI boot options before first legacy boot option.
Power Loss Control	**Remain Off** Turn On Last State	Select the mode of operation if an AC power loss occurs: 'Remain Off' - Keeps the power off until the power button is pressed. 'Turn On' - Restores power to the computer. 'Last State' - Restores the previous power state before power loss occurred. **Note:** Please chose an ATX type power supply if you want to use this feature.
AT Shutdown Mode	System Reboot **Hot S5**	Select the behavior of an AT-powered system after a shutdown.
System Off Mode	**G3/Mech Off** S5/Soft Off	Select the system state after a shutdown if a battery system is connected.
Fast Boot	**Disabled** Enabled	Enable this feature to boot with a minimum set of devices. **Note:** This feature has no effect on BBS / legacy boot options.

Feature	Options	Description
1st Boot Device	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk **USB CDROM** Other USB Device Onboard LAN External LAN Firmware-based Bootloader Other Device	
2nd Boot Device	Disabled SATA 0 Drive SATA 1 Drive **USB Harddisk** USB CDROM Other USB Device Onboard LAN External LAN Firmware-based Bootloader Other Device	
3rd Boot Device	Disabled **SATA 0 Drive** SATA 1 Drive USB Harddisk USB CDROM Other USB Device Onboard LAN External LAN Firmware-based Bootloader Other Device	
4th Boot Device	Disabled SATA 0 Drive **SATA 1 Drive** USB Harddisk USB CDROM Other USB Device Onboard LAN External LAN Firmware-based Bootloader Other Device	

Feature	Options	Description
5th Boot Device	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk USB CDROM **Other USB Device** Onboard LAN External LAN Firmware-based Bootloader Other Device	
6th Boot Device	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk USB CDROM Other USB Device Onboard LAN External LAN Firmware-based Bootloader **Other Device**	
7th Boot Device	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk USB CDROM Other USB Device **Onboard LAN** External LAN Firmware-based Bootloader Other Device	
8th Boot Device	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk USB CDROM Other USB Device Onboard LAN External LAN **Firmware-based Bootloader** Other Device	

Note

The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.

Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.

10.8 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen. You can display a Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
Boot Override	
List of all boot devices currently detected	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to "Device Based".

11 Additional BIOS Features

11.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

11.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-QA4 is identified as QA40R1xx where:

- QA40 is the project name
- R is the identifier for a BIOS ROM file
- 1 is the feature number
- xx is the major and minor revision number.

The binary size of conga-QA4 BIOS is 8MB.

11.3 Updating the BIOS

OEMs often use BIOS updates to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS. The conga-QA4 uses a congatec/AMI AptioEFI firmware, which is stored in an onboard flash ROM chip and can be updated using the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line, Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

11.4 Supported Flash Devices

The conga-QA4 supports the following flash devices:

- Winbond W25Q64JVSSIQ (8MB)

The flash device listed above has been tested and can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.