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XTX™
conga-X915

Intel® Pentium® M or Celeron® M processor with an Intel® 915 or 910 chipset

User's Guide

Revision 1.5

Revision History

Revision	Date (dd.mm.yy)	Author	Changes
0.1	24.10.05	GDA	Initial release
1.0	23.12.05	GDA	Official release. Updates throughout User's Guide.
1.1	23.06.06	GDA	Updated power consumption tables. Added BIOS Setup Data Backup overview section 5.3.1. Added Performance Control information to section 6.4. Added ACPI resume events table to section 6.6.
1.2	17.11.06	GDA	Added sections 1.4 Electrical Characteristics and 1.4.1 Supply Voltage Ripple. Updated section 1.6 Supply Voltage Battery Power, section 1.7 Environmental Specifications, section 3.1 Heatspreader Dimensions diagram, section 5.3.1 BIOS Setup Data Backup Overview diagram. Updated complete BIOS Setup Description section. Added description for PP_TPM pin 60 on X2 connector.
1.3	13.02.07	GDA	Added Electrostatic Sensitive Device information. Removed processor core voltage values from power consumption tables. Added caution statement to section 3 Heatspreader.
1.4	02.07.07	GDA	Changed all references of 82915GM to 82915GME and removed TV-Out support references, TV-Out is no longer supported on conga-X915. TV-Out is only available via SDVO. Removed conga-915/760 Pentium M 2.0GHz article number 058480 from the user's guide. This variant is no longer available. Added information about conga-X915/CM600 eco article number 013410 to user's guide. Added information about center mounting hole to 'Caution' statement in section 3 Heatspreader. Added information to 'Caution' statement in section 4.1.4 Onboard Generated Supply Voltage. Added information to section 4.2.4 PCI Express about x4 mode. Added note about floppy cable to section 4.3.5 Parallel Port/Floppy Interface. Updated section 8 System Resources and section 9 BIOS Setup Description.
1.5	13.11.09	GDA	Improved section 1.4.1 and added section 1.4.2. Added section 5.7 'congatec Battery Management Interface'. Added 'Note' to section 7 'Signal Descriptions and Pinout Tables'. Added LVDS signal mapping to table 22 LVDS Interface Pinout. Updated 'System Resources' and 'BIOS Setup Description' sections.

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-X915. It is one of four documents that should be referred to when designing an XTX™ application. The other reference documents that should be used include the following:

XTX™ Design Guide
XTX™ Specification
ETX® Design Guide

The links to these documents can be found on the congatec AG website at www.congatec.com

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This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols are used in this user's guide:



Warning

Warnings indicate conditions that, if not observed, can cause personal injury.



Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.



Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHZ	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
PCI-EX	PCI Express
SATA	Serial ATA
PATA	Parallel ATA
T.O.M.	Top of memory = max. DRAM installed
HDA	High Definition Audio
I/F	Interface
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

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- AMIBIOS8_HDD_Security.pdf
- AMIBIOS8-Flash-Recovery-Whitepaper.pdf
- AMIBIOS8_SerialRedirection.pdf
- AMIBIOS8 Setup User's Guide

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ETX® Concept and XTX™ Extension

The ETX® concept is an off the shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific baseboard. ETX® modules have a standardized form factor of 95mm x 114mm and have specified pinouts on the four system connectors that remain the same regardless of the vendor. The ETX® module provides most of the functional requirements for any application. These functions include, but are not limited to, graphics, sound, keyboard/mouse, IDE, Ethernet, parallel, serial and USB ports. Four ruggedized connectors provide the baseboard interface and carry all the I/O signals to and from the ETX® module.

Baseboard designers can utilize as little or as many of the I/O interfaces as deemed necessary. The baseboard can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly ETX® applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class ETX® modules. Simply unplug one module and replace it with another, no redesign is necessary.

XTX™ is an expansion and continuation of the well-established and highly successful ETX® standard. XTX™ offers the newest I/O technologies on this proven form factor. Now that the ISA bus is being used less and less in modern embedded applications congatec AG offers an array of different features on the X2 connector than those currently found on the ETX® platform. These features include new serial high speed buses such as PCI Express™ and Serial ATA®. All other signals found on connectors X1, X3, and X4 remain the same in accordance to the ETX® standard (Rev. 2.7) and therefore will be completely compatible. If the embedded PC application still requires the ISA bus then an ISA bridge can be implemented on the application specific baseboard or the readily available LPC bus located on the XTX™ module may be used. Contact congatec technical support for details.

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Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device



All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

conga-X915 Options Information

The conga-X915 is available in six different optional variants. This user's guide describes all of these options. Below you will find an order table showing the different configurations that are currently offered by congatec AG. Check the table for the Part no./Order no. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Part-No.	013410	098634	023557	015789	075643	012041
CPU	Celeron M 600MHz	373 Celeron M 1GHz	Celeron M eco 1GHz	373 eco Celeron M 1GHz	738 Pentium M 1.4GHz	745 Pentium M 1.8GHz
Cache	512 kByte	512 kByte	0 kByte	512 kByte	2 MByte	2 MByte
SATA	2x	2x	2x	2x	2x	2x
SDVO	Yes	Yes	Yes	Yes	Yes	Yes
USB 2.0	6x	6x	6x	6x	6x	6x
PCI Express	4x	4x	4x	4x	4x	4x
Suspend to RAM (S3)	Yes	Yes	Yes	Yes	Yes	Yes
Chipset	82910GMLE	82915GME	82915GME	82910GMLE	82915GME	82915GME

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1 Specifications

1.1 Feature List

Table 1 Feature Summary

Form Factor	ETX® standard (Rev. 2.7) with XTX™ extension
Processor	Intel® Celeron® M 600MHz ULV with 512-kbyte L2 cache (ultra low voltage) Intel® Celeron® M 373 1.0GHz with 512-kbyte L2 cache (Ultra Low Voltage) Intel® Celeron® M 1.0GHz with 0-kbyte L2 cache (Ultra Low Voltage) Intel® Pentium® M 738 1.4GHz with 2-MByte L2 cache (Low Voltage) Intel® Pentium® M 745 1.8GHz with 2-MByte L2 cache
Memory	SO-DIMM DDR2 up to 2-GByte
Chipset	Graphics and Memory Controller Hub (GMCH) Intel® 82915GME or 82910GMLE Intel® I/O Controller Hub 82801FBM (ICH6M)
Audio	Realtek ALC 655 AC'97 Rev. 2.3 compatible.
Ethernet	ICH6M with PHY Intel® 82562
Graphics Options	Intel® Graphics Media Accelerator 900 with max.224MByte Dynamic Video Memory Technology (DVMT 3.0) as well as Dual independent display support. • CRT Interface 400 MHz RAMDAC Resolutions up to 2048x1536 @ 70Hz (QXGA) • Flatpanel Interface (integrated) 2x25-112MHz LVDS Transmitter Supports all 1x18, 2x18, 1x24, 2x24 Bit TFT configurations (current chipset revisions support 24Bit modes although not officially stated by Intel®) Supports both conventional (FPDI) and non-conventional (LDI) color mappings Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3) Resolutions 640x480 up to 1600x1200 (UXGA) only up to 1400x1050 (SXGA) for 82910GMLE • Motion Video Support Up- and Downscaling High definition content decode H/W motion compensation Subpicture support Dynamic bob and weave • AUX Output 2 x Intel compliant SDVO ports (serial DVO) 200MPixel/sec each Supports external DVI, TV and LVDS transmitter
Super I/O	Winbond 83627HG
Peripheral Interfaces	• 2x Serial ATA® • 4x x1 PCI Express® Lanes • PCI Bus Rev. 2.3 • 6x USB 2.0 (EHCI) • LPC Bus (no ISA Bus) • 1x EIDE (UDMA-66/100) • PS/2 Keyboard, Mouse • I²C Bus, Fast Mode (400 kHz) multimaster • Floppy (shared with LPT) • LPT (EEP/ECP, shared with floppy) • 2 x COM Ports, TTL Level • 1 x IrDA Port • AC'97/HDA (High Definition Audio codecs) Digital Audio interface
BIOS	Based on AMIBIOS8®-1MByte Flash BIOS with congatec Embedded BIOS features
Power Management	ACPI 2.0 compliant with battery support. Also supports Suspend to RAM (S3).

Note

Some of the features mentioned in the Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 7 of this user's guide to determine what options are available on your particular module.

1.2 Supported Operating Systems

The conga-X915 supports the following operating systems.

- Microsoft® Windows® XP/2000
- Microsoft® Windows ®XP Embedded
- Microsoft® Windows® CE 5.0 / 6.0
- Linux
- QNX

1.3 Mechanical Dimensions

- 95.0 mm x 114.0 mm (3.75” x 4.5”)
- Height approx. 12mm (0.4”)

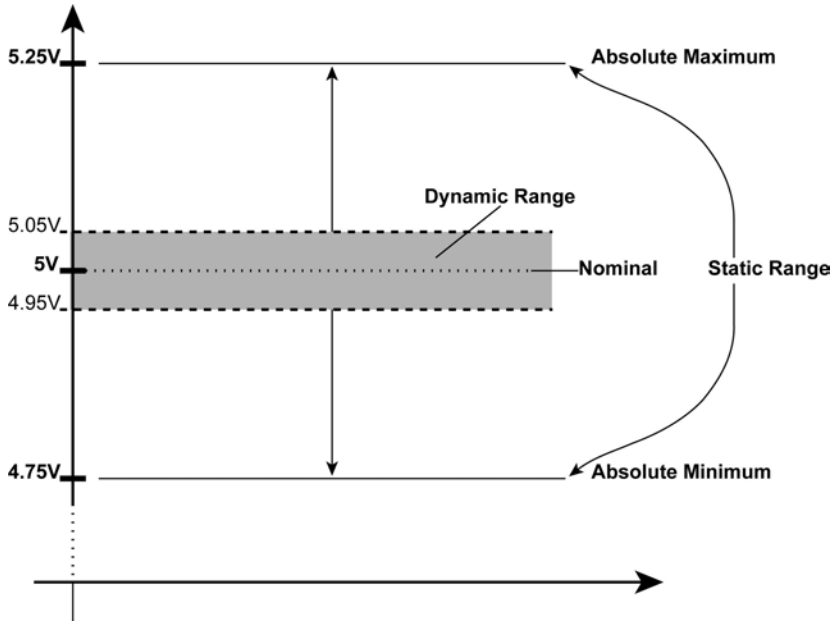
1.4 Electrical Characteristics

Characteristics			Min	Typ	Max	Units	Comment
5V	Voltage	+/-5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	100	mV_{pp}	0-20MHz
	Current	See section 1.5 'Power Consumption' for supply current information.					
5V_SB	Voltage	+/-5%	4.75	5.00	5.25	Vdc	
	Current			250		mA	

1.4.1 Supply Voltage Ripple

- Maximum 100mV peak to peak over a frequency band of 10Hz to 20MHz.

The dynamic range shall not exceed the static range.



1.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum rise time of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

1.5 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The XTX module was mounted into a special baseboard. This special baseboard does not have any power consuming components mounted on it. It provides one connector for a CRT monitor connection, a PS/2 keyboard and mouse connection, and an IDE device connection. The baseboard is powered by a Direct Current (DC) power supply that is set to output 5 Volts and is connected directly to the special baseboard. Additionally, positive and negative sense lines are connected to the baseboard in order to measure the current consumption of the module. This current consumption value is displayed by the DC power supply's readout and this is the value that is recorded as the power consumption measurement. All recorded values are approximate.

All external peripheral devices, such as the hard drive, are externally powered so that they do not influence the power consumption value that is measured for the module. This ensures the value measured reflects the true power consumption of the module and only the module. A keyboard is used to configure the module and then it is

disconnected before the measurement is recorded. If the keyboard remained connected, an additional current consumption of approximately 10 mA is noticed.

Each module was measured while running Windows XP Professional with SP2 (service pack 2) and the “Power Scheme” was set to “Portable/Laptop”. This setting ensures that Pentium M processors run in LFM (lowest frequency mode) with minimal core voltage during desktop idle. Celeron M processors do not support this feature and always run at the same core voltage even during desktop idle. The screen resolution was set to 800x600 32bit High Color. Each module was tested while using a swissbit® DDR2 PC2-4200-444 512MB memory module. Using different sizes of RAM will cause slight variances in the measured results. Power consumption values were recorded during the following stages:

Windows XP Professional SP2

- Desktop Idle (600MHz or 800MHz for Pentium M, Maximum frequency for Celeron M)
- 100% CPU workload (see note below)
- Windows XP Professional Standby Mode (requires setup node “Suspend Mode” in the BIOS to be configured to S1 POS (Power On Suspend))
- Suspend to RAM (requires setup node “Suspend Mode” in BIOS to be configured to S3 STR (Suspend to RAM))

Note

A software tool was used to stress the CPU to 100% workload.

Processor Information

In the following power tables there is some additional information about the processors. Intel® offers processors that are considered to be low power consuming. These processors can be identified by their voltage status. Intel uses the following terms to describe these processors. If none of these terms are used then the processor is not considered to be low power consuming.

LV=Low voltage
ULV=Ultra low voltage

When applicable, the above mentioned terms will be added to the power tables to describe the processor. For example:

Celeron M 1.0GHz 512kB L2 cache
ULV 90nm

Intel® also describes the type of manufacturing process used for each processor. The following term is used:

nm=nanometer

The manufacturing process description is included in the power tables as well. See

example below. For information about the manufacturing process visit Intel®'s website.

Celeron M 1.0GHz 512kB L2 cache
ULV **90nm**

1.5.1 conga-X915 Celeron M 600MHz 512kB L2 cache

With 512MB memory installed

conga-X915 Art. No. 013410	Celeron M 600MHz 512kB L2 cache LV 90nm Layout Rev. P915LE0 /BIOS Rev. P915R115			
Memory Size	512MB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Standby	Suspend to Ram (S3)
Power consumption (measured in Amperes/Watts)	1.7 A/8.5 W	2.5 A/12.5 W	1.5 A/7.5 W	0.1 A/0.5 W

Note

The conga-X915/CM600 eco article number 013410 is equipped with an Intel® 82910GMLE chipset. Other conga-X915 standard variants are equipped with an Intel® 82915GME chipset with the exception of the conga-X915/373 eco article number 015789. It also features an Intel® 82910GMLE chipset.

1.5.2 conga-X915 Celeron M 1.0GHz without cache

With 512MB memory installed

conga-X915 Art. No. 023557	Celeron M 1.0GHz without cache ULV 90nm Layout Rev. P915LF3 /BIOS Rev. P915R117			
Memory Size	512MB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Standby	Suspend to Ram (S3)
Power consumption (measured in Amperes/Watts)	1.8 A/9 W	2.7 A/13.5 W	1.7 A/8.5 W	0.1 A/0.5 W

1.5.3 conga-X915 Celeron M 1.0GHz 512kB L2 cache

With 512MB memory installed

conga-X915 Art. No. 098634	Celeron M 1.0GHz 512kB L2 cache ULV 90nm Layout Rev. P915LB1 /BIOS Rev. P915R112			
Memory Size	512MB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Standby	Suspend to Ram (S3)
Power consumption (measured in Amperes/Watts)	1.4-1.5 A/7-7.5 W	2.3 A/11.5 W	1.5 A/7.5 W	0.1 A/0.5 W

1.5.4 conga-X915 Celeron M 1.0GHz 512kB L2 cache

With 512MB memory installed

conga-X915 Art. No. 015789	Celeron M 1.0GHz 512kB L2 cache ULV 90nm Layout Rev. P915LB1 /BIOS Rev. P915R112			
Memory Size	512MB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Standby	Suspend to Ram (S3)
Power consumption (measured in Amperes/Watts)	1.4-1.5 A/7-7.5 W	2.3 A/11.5 W	1.5 A/7.5 W	0.1 A/0.5 W

Note

The conga-X915/373 eco article number 015789 is equipped with an Intel® 82910GMLE chipset. Other conga-X915 standard variants are equipped with an Intel® 82915GME chipset with the exception of the conga-X915/CM600 eco article number 013410. It also features an Intel® 82910GMLE chipset.

1.5.5 conga-X915 Pentium M 1.4GHz 2MB L2 cache

With 512MB memory installed

conga-X915 Art. No. 075643	Pentium M 1.4GHz 2MB L2 cache LV 90nm Layout Rev. P915LB3 /BIOS Rev. P915R113			
Memory Size	512MB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle @ 600MHz	100% workload	Standby	Suspend to Ram (S3)
Power consumption (measured in Amperes/Watts)	1.5-1.6 A/7.5-8 W	3.5 A/17.5 W	1.6 A/8 W	0.1 A/0.5 W

1.5.6 conga-X915 Pentium M 1.8GHz 2MB L2 cache

With 512MB memory installed

conga-X915 Art. No. 012041	Pentium M 1.8GHz 2MB L2 cache 90nm Layout Rev. P915LB3 /BIOS Rev. P915R113			
Memory Size	512MB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle @ 600MHz	100% workload	Standby	Suspend to Ram (S3)
Power consumption (measured in Amperes/Watts)	1.5 A/7.5 W	6.0 A/30 W	1.6 A/8 W	0.1 A/0.5 W

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

1.6 Supply Voltage Battery Power

- 2.0V-3.6V DC
- Typical 3.0V

1.6.1 CMOS Battery Power Consumption

RTC @ 20ºC	Voltage	Current
Integrated in the southbridge	3V DC	2.50 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

1.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%



Caution

The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

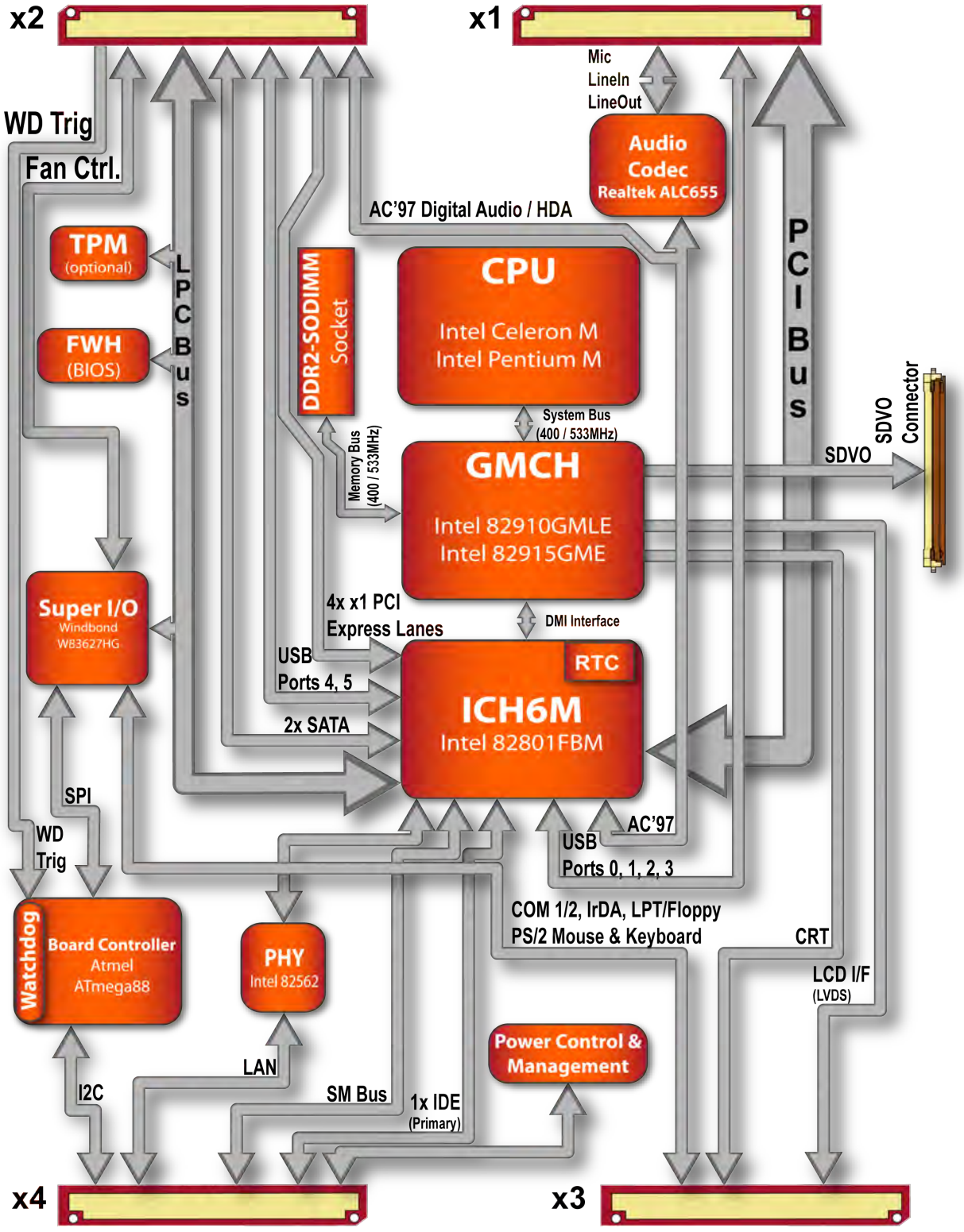
congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.

If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

For more information about operating a congatec module without heatspreader contact congatec technical support.

Humidity specifications are for non-condensing conditions.

2 Block Diagram



3 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module. It is a 2mm thick aluminum plate.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.



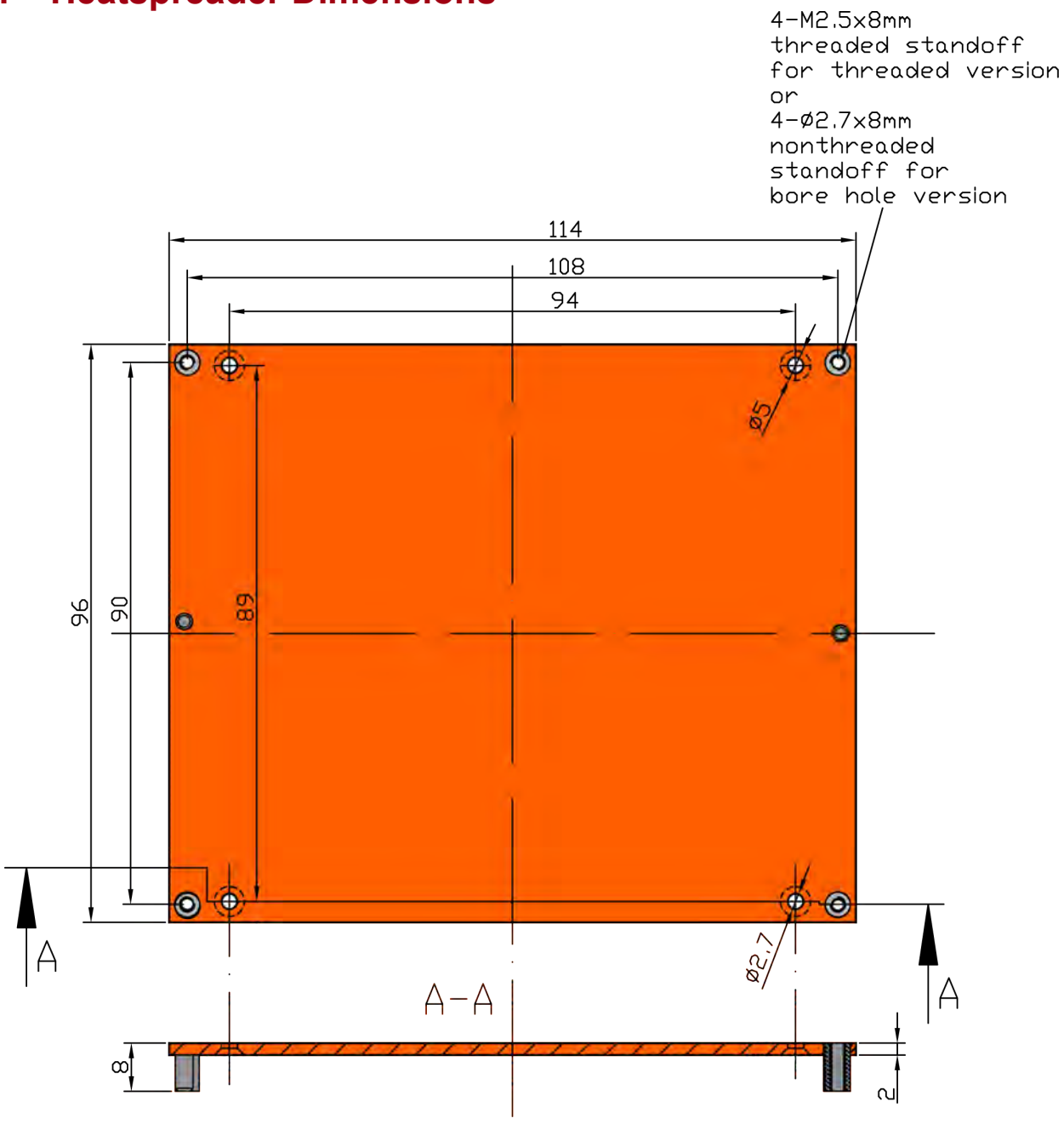
Caution

The center mounting hole on the heatspreader must be used to ensure that all components that are required to make contact with heatspreader do so. Failure to utilize the center mounting hole will result in improper contact between these components and heatspreader thereby reducing heat dissipation efficiency.

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

For more information about this subject refer to Application Note AN14_ETX_XTX_Mounting_Solutions.pdf that can be found on the congatec website.

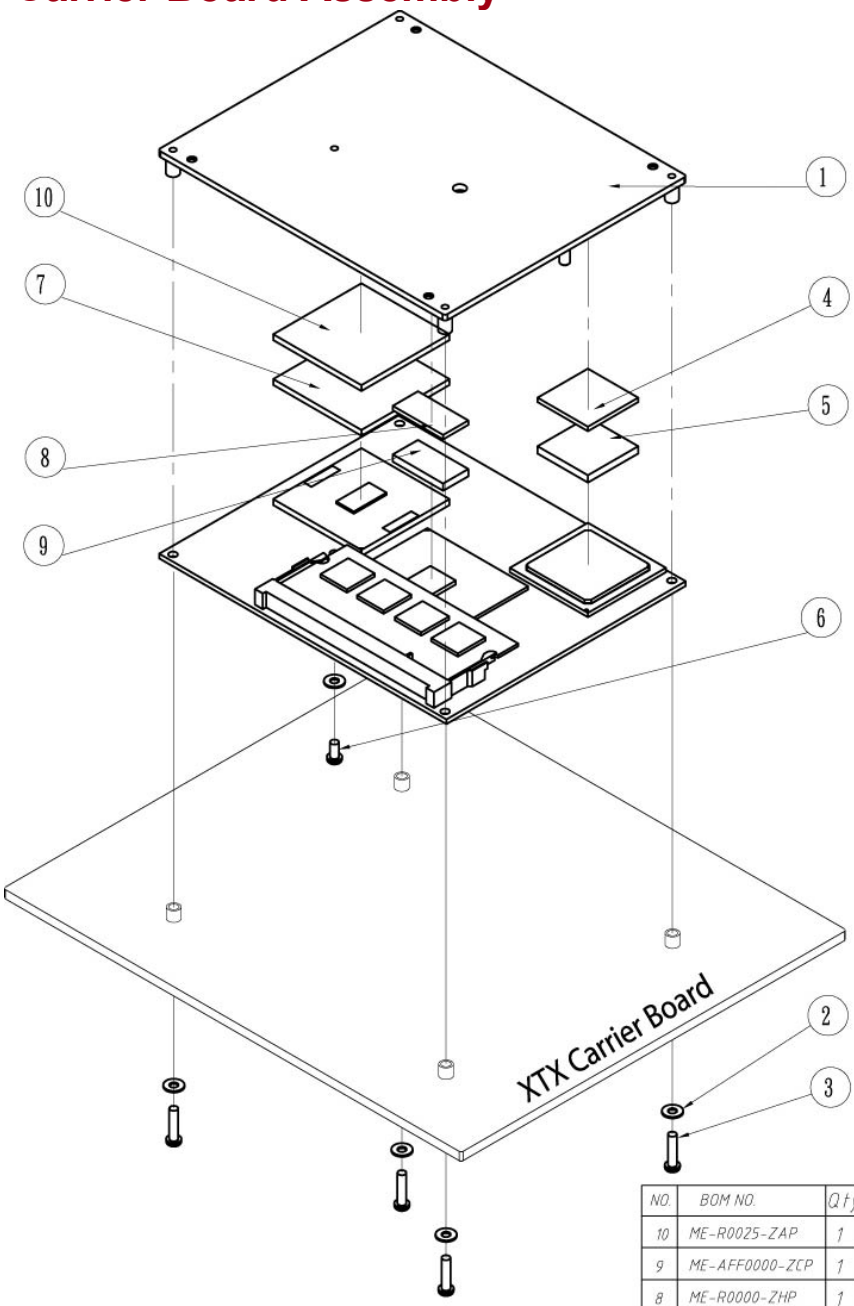
3.1 Heatspreader Dimensions



Note

All measurements are in millimeters. Torque specification for heatspreader screws is 0.5 Nm.

3.2 Exploded view of Threaded XTX Heatspreader, Module and Carrier Board Assembly



NO.	BOM NO.	Qty	PARTS NAME	REMARK
10	ME-R0025-ZAP	1	THERMAL PAD	
9	ME-AFF0000-ZCP	1	COPPER	
8	ME-R0000-ZHP	1	THERMAL PAD	
7	ME-AFF0001-ZCP	1	COPPER	
6	ME-SMR2.5X5N	1	MACHINE SCREW	
5	ME-AFF0002-ZCP	1	COPPER	
4	ME-R0002-ZHP	1	THERMAL PAD	
3	ME-SMR2.5X12N	5	MACHINE SCREW	
2	ME-WA0000-N	5	WASHER	
1	ME-AAL0003-YOP	1	HEATSPREADER	

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4 Connector Subsystems

X connector Subsystems (top view)



top view

In this view the connectors are seen "through" the module.

4.1 Connector X1

The following subsystems can be found on connector X1.

4.1.1 PCI Bus

The implementation of the PCI bus complies with PCI specification Rev. 2.3 and ETX® specification Rev. 2.7

4.1.2 USB

The conga-X915 offers 3 UHCI USB host controllers and one EHCI USB host controller via the Intel® 82801FBM (ICH6M) south bridge. These controllers comply with USB standard 1.1 and 2.0. Four of the six available USB ports are located on the X1 connector and all four of these ports support the connection of USB 2.0 compliant devices. For more information about how the USB host controllers are routed see section 6.7.

4.1.3 Audio

The conga-X915 is equipped with a Realtek ALC655 PCI audio controller. It is AC97 2.2 specification compliant and legacy audio SB16™ compatible.

Note

The USB and Audio controllers are PCI bus devices. The BIOS allocates the necessary system resources when configuring the PCI devices.

4.1.4 Onboard Generated Supply Voltage

Pins 12, 16 and 24 on the X1 connector provide the ability to connect external devices to the modules onboard generated supply voltage (3.3V±5%). 3.3V external devices can be connected to these pins but must not exceed a maximum external load of 500mA. For more information about this feature contact congatec AG technical support.

Caution

Do not connect pins 12, 16 and 24 to a 3.3V external power supply. This will cause a current cross-flow and may result in either a system malfunction and/or damage to the external power supply and the module.

4.2 Connector X2 (XTX™ Extension)

congatec AG has chosen to replace the outdated ISA bus, currently found on ETX® modules X2 connector, with the latest technologies available in todays market. This implementation is called XTX™. The XTX™ extension is an enhancement of the highly successful ETX® standard and provides consumers the ability to equip their embedded applications with the latest technology while still utilizing the ETX® standard form factor.

The following subsystems can be found on connector X2.

4.2.1 LPC

As a part of the replacement to the no longer supported ISA bus, conga-X915 offers the LPC (Low Pin Count) bus through the use of Intel® 82801FBM (ICH6M) south bridge. There are already many devices available for this Intel defined bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific baseboard using this bus.

4.2.2 USB 2.0

The conga-X915 offers two additional USB ports, via the Intel® 82801FBM (ICH6M) south bridge, that are connected to the X2 connector. These ports are both USB 1.1 and 2.0 compliant. For more information about how the USB host controllers are routed see section 6.7.

4.2.3 Serial ATA™

Two Serial ATA150 connections are provided via the Intel® 82801FBM (ICH6M). Serial ATA is an enhancement of the parallel ATA therefore offering higher performance. As a result of this enhancement the traditional restrictions of parallel ATA are overcome with respect to speed and EMI. Serial ATA starts with a transfer rate of 150 Mbytes/s and can be expanded up to 600 Mbytes/s in order to accommodate future developments. Serial ATA is completely protocol and software compatible to parallel ATA.

4.2.4 PCI Express™

The conga-X915 offers 4 x1 PCI Express lanes via the Intel® 82801FBM (ICH6M), which can be configured to support PCI Express edge cards or ExpressCards. Additionally, these lanes can be statically configured as 4 x1 or 1 x4. AC_SYNC and AC_SDOUT can be used to switch PCI Express channels 0-3 between x1 and x4 mode. If both signals are each pulled-up (using 1KΩ resistors) to 3.3V at the rising edge of PWROK then x4 mode is enabled. x1 mode is used by default if these resistors are not populated. The PCI Express interface is based on the *PCI Express Specification 1.0a.*

4.2.5 ExpressCard™

The conga-X915 supports the implementation of ExpressCards, which requires the dedication of one USB port and one PCI Express lane for each ExpressCard used.

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4.2.6 AC'97 / HDA (High Definition Audio) Digital Audio

The conga-X915 provides an interface that supports the connection of AC'97 digital audio codecs as well as HDA audio codecs. For more information about this interface consult the XTX Design Guide.

4.2.7 Extended System Management

conga-X915 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) Output. Additionally there is an input signal called FAN_TACHOIN that provides the ability to monitor the system fan's RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason a two pulse per revolution fan, or similar hardware solution, is recommended. These features are implemented by the Winbond W83627HG super I/O.

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4.3 Connector X3

The following subsystems can be found on connector X3. The implementation of all the subsystems comply with ETX® specification 2.7. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

4.3.1 Graphics

The conga-X915 graphics are driven by an Intel® Graphics Media Accelerator 900 engine, which is incorporated into the Intel® 82915GME/82910GMLE chipset found on the conga-X915.

4.3.2 LCD

The Intel® 82915GME/82910GMLE chipset, found on the conga-X915, offers an integrated dual channel LVDS interface supported on Display Pipe B only.

4.3.3 Serial Ports (1 and 2)

The conga-X915 offers two serial interfaces (TTL) that are provided by the I/O controller, which is a Winbond W83627HG super I/O located on the conga-X915.

4.3.4 Serial Infrared Interface

Serial port 2 can be configured as a serial infrared interface. The Infrared (IrDA) function provides point-to-point (or multi-point to multi-point) wireless communication, which can operate under various transmission protocols including IrDA SIR. This feature is also implemented by the onboard Winbond W83627HG super I/O.

4.3.5 Parallel Port/Floppy Interface

The parallel port/floppy interface can be configured as either a conventional LPT parallel port or a floppy-disk drive port. This is software implemented and can be configured in the BIOS setup program. See section 9.4.6 of this document for information about configuring the parallel port/floppy interface.

Note

When using the onboard floppy interface the floppy drive must be connected via a non-twisted floppy cable versus a twisted cable. The floppy drive will not function when connected via a twisted floppy cable.

4.3.6 Keyboard/Mouse

The implementation of these subsystems comply with ETX® specification 2.7.

4.4 Connector X4

The following subsystems can be found on connector X4. The implementation of all the subsystems comply with ETX® specification 2.7. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

4.4.1 IDE

The IDE host adapter is capable of UDMA-100 operation. Only the Primary IDE channel is supported.

4.4.2 Ethernet

Ethernet interface is provided by an Intel® 82562 integrated Fast Ethernet NIC controller. The controller is IEEE 802.3u, 10/100Base-Tx fast Ethernet compatible. The interface provides single-ended differential signals that have to be routed through an Ethernet transformer.

4.4.3 I²C Bus 400kHz

The I²C bus is implemented through the use of ATMEL ATmega88 microcontroller. It provides a Fast Mode (400kHz max.) multi-master I²C Bus that has maximum I²C bandwidth.

4.4.4 Power Control

PWGIN

PWGIN (pin 4 on the X4 connector) can be connected to an external power good circuit or it may also be utilized as a manual reset input. In order to use PWGIN as a manual reset the pin must be grounded through the use of a momentary-contact pushbutton switch. When external circuitry asserts this signal, it's necessary that an open-drain driver drives this signal causing it to be held low for a minimum of 15ms to initiate a reset. Using this input is optional. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies the conga-X915 module is capable of generating its own power-on reset.

The conga-X915 provides support for controlling ATX-style power supplies. In order to do this the power supply must provide a constant source of 5V power. When not using an ATX power supply then the conga-X915's pins PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

PS_ON#

The PS_ON (pin 5 on the X4 connector) signal is an active-low output that turns on the main outputs of an ATX-style power supply. This open-collector signal can be pulled up

to the 5V_SB supply voltage through the use of a 1K resistor. Usually there is a pull-up resistor internally implemented in the power supply itself yet it is also good practice to implement a footprint for the pull-up resistor in the baseboard circuitry.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 7 on the X4 connector) is used to connect to a momentary-contact, active-low pushbutton input while the other terminal on the pushbutton must be connected to ground. This signal is XTX™ internally pulled up to 5V_SB using a 4k7 resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-X915. The remaining necessary voltages are internally generated on the module using onboard power supplies. A baseboard designer should be aware of the following important information when designing a power supply for a conga-X915 application:

- As mentioned earlier in section 4.1.4 the conga-X915 is capable of generating an onboard 3.3V supply with an output current that is limited to 500mA. If an external device requires more then this 500mA limit then it's necessary to design a 3.3V supply into the baseboard.



Caution

It is not possible to connect an external 3.3V supply to the onboard generated 3.3V supply pins on the conga-X915 module. This will cause a current cross-flow and may result in either a system malfunction and/or damage to the external power supply and the module.

- Sometimes when designing baseboards, baseboard designers choose to fuse power to some external devices such as keyboards or USB devices by using solid-state or polyswitch overcurrent protection devices. This results in the protective devices typically only opening after they pass several times their rated current for long periods of time. When the application power supply is incapable of generating the necessary current needed to open these protective devices it's possible that the application crashes as a result of an external fault and therefore will reduce the applications reliability as well as make a fault diagnosis of the application difficult.

- It has also been noticed that on some occasions problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't

arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document “ATX12V Power Supply Design Guide V2.2”.

4.4.5 Power Management

APM 1.2 compliant. ACPI 2.0 compliant with battery support. Also supports Suspend to RAM (S3).

5 Additional Features

5.1 Watchdog

The conga-X915 is equipped with a multi stage watchdog. This solution can be triggered by software and external OEM hardware (input pin is pin 48 on the X2 connector called WDTRG#). For more information about the Watchdog feature see the BIOS setup description section 9.4.13 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

5.2 Onboard Microcontroller

The conga-X915 is equipped with an ATMEL Atmega88 microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

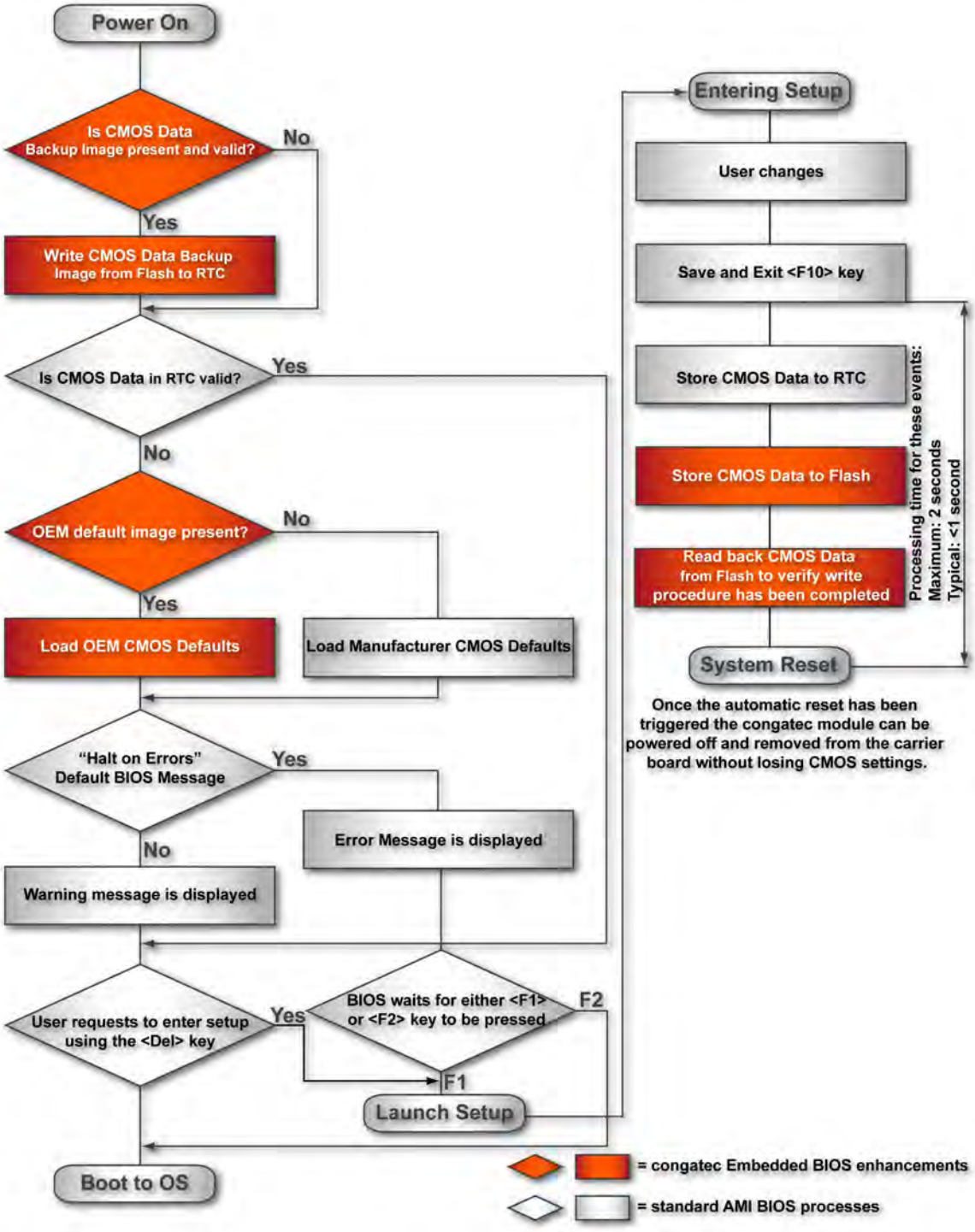
5.3 Embedded BIOS

The conga-X915 is equipped with congatec Embedded BIOS and has the following features:

- ACPI Power Management
- ACPI Battery Support
- Supports Customer Specific CMOS Defaults
- Multistage Watchdog
- User Data Storage
- Manufacturing Data and Board Information
- OEM Splash Screen
- Flat Panel Auto Detection
- BIOS Setup Data Backup (see section 5.3.1)
- Fast Mode I²C Bus
- Console Redirection and BIOS Update (flashing BIOS) via Serial Port

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5.3.1 Simplified Overview of BIOS Setup Data Backup



The above diagram provides an overview of how the BIOS Setup Data is backed up on congatec modules. OEM default values mentioned above refer to customer specific CMOS settings created using the congatec System Utility tool.

Once the BIOS Setup Program has been entered and the settings have been changed, the user saves the settings and exits the BIOS Setup Program using the F10 key feature. After the F10 function has been invoked, the CMOS Data is stored in a dedicated non-volatile CMOS Data Backup area located in the BIOS Flash Memory chip as well as RTC. The CMOS Data is written to and read back from the CMOS Data Backup area in order to verify that the write procedure was successful. Once verified the F10 Save and Exit function continues to perform some minor processing tasks and finally reaches an automatic reset point, which instructs the module to reboot. After the Automatic Reset has been triggered the congatec module can be powered off and, if need be, removed from the baseboard without losing the new CMOS settings.

5.4 SDVO

Two SDVO (Serial Digital Video Output) ports are supported via a connector located on the bottom side of conga-X915. These ports support the connection of external transmitters such as DVI, TV-Out, and LVDS. For more information about the pinout of the connector (X6) see section 7.8 of this document.

5.5 Security Features

The conga-X915 can be equipped optionally with a “Trusted Platform Module“ (TPM 1.2). This TPM 1.2 includes co-processors to calculate efficient hash and RSA algorithms with key lengths up to 2,048 bits as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity and confidence levels.

5.6 Suspend to RAM (S3)

The Suspend to RAM feature is available on the conga-X915.

5.7 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-X915 BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM² User’s Guide

6 conga Tech Notes

The conga-X915 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

6.1 Comparison of I/O APIC to 8259 PIC Interrupt mode

I/O APIC (Advanced Programmable Interrupt controller) mode deals with interrupts differently than the 8259 PIC.

The method of interrupt transmission used by APIC mode is implemented by transmitting interrupts through the system bus and they are handled without the requirement of the processor to perform an interrupt acknowledge cycle.

Another difference between I/O APIC and 8259 PIC is the way the interrupt numbers are prioritized. Unlike the 8259 PIC, the I/O APIC interrupt priority is independent of the actual interrupt number.

A major advantage of the I/O APIC found in the chipset of the conga-X915 is that it's able to provide more interrupts, a total of 24 to be exact. It must be mentioned that the APIC is not supported by all operating systems. In order to utilize the APIC mode it must be enabled in the BIOS setup program before the installation of the OS and it only functions in ACPI mode. You can find more information about APIC in the IA-32 Intel Architecture Software Developer's Manual, Volume 3 in chapter 8.

Note

You must ensure that your operating system supports APIC mode in order to use it.

6.2 Native vs. Compatible IDE mode

6.2.1 Compatible Mode

When operating in compatible mode, the SATA and PATA (Parallel ATA) controller together need two legacy IRQs (14 and 15) and are unable to share these IRQs with other devices. This is a result of the fact that the SATA and PATA controller emulate legacy IDE controllers.

6.2.2 Native Mode

Native mode allows the SATA and PATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources, which means it can be configured anywhere within the system. When either the SATA or PATA controller runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system. Setting Enhanced mode in the

BIOS setup program will automatically enable Native mode as Native mode is a subset of Enhanced mode. See section 9.4.8 for more information about this.

Running in native mode frees up interrupt resources (IRQs 14 and 15) and decreases the chance that there may be a shortage of interrupts when installing devices.

Note

If your operating system supports native mode then congatec AG recommends you enable it.

6.3 Thermal Monitor and Catastrophic Thermal Protection

Pentium/Celeron M processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature, that the Intel Thermal Monitor uses to activate the TCC, cannot be configured by the user nor is it software visible.

The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel Speedstep transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.

Note

The maximum operating temperature for Pentium/Celeron M processors is 100°C. TM2 mode should be used for Intel Pentium M processors and is only supported by Intel Pentium M processors, it is not supported by Intel Celeron M processors.

Two modes are supported by the Thermal Monitor to activate the TCC. They are called Automatic and On-Demand. In order for the processor to operate within specification, the Intel Thermal Monitor Automatic Mode must be enabled through a setup node in the BIOS. No additional hardware, software, or handling routines are necessary when using Automatic Mode.

Note

To ensure that the TCC is active for only short periods of time thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel Pentium/Celeron M processor's respective datasheet can provide you with more information about this subject.

THERMTRIP# signal is used by Intel's Pentium/Celeron M processors for catastrophic thermal protection. If the processor's silicon reaches a temperature of approximately 125°C then the processor signal THERMTRIP# will go active and the system will automatically shut down to prevent any damage to the processor as a result of overheating. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

Note

In order for THERMTRIP# to be able to automatically switch off the system it is necessary to use an ATX style power supply.

6.4 Processor Performance Control

Pentium M processors run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it's not being fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting found in the control panel option applet.

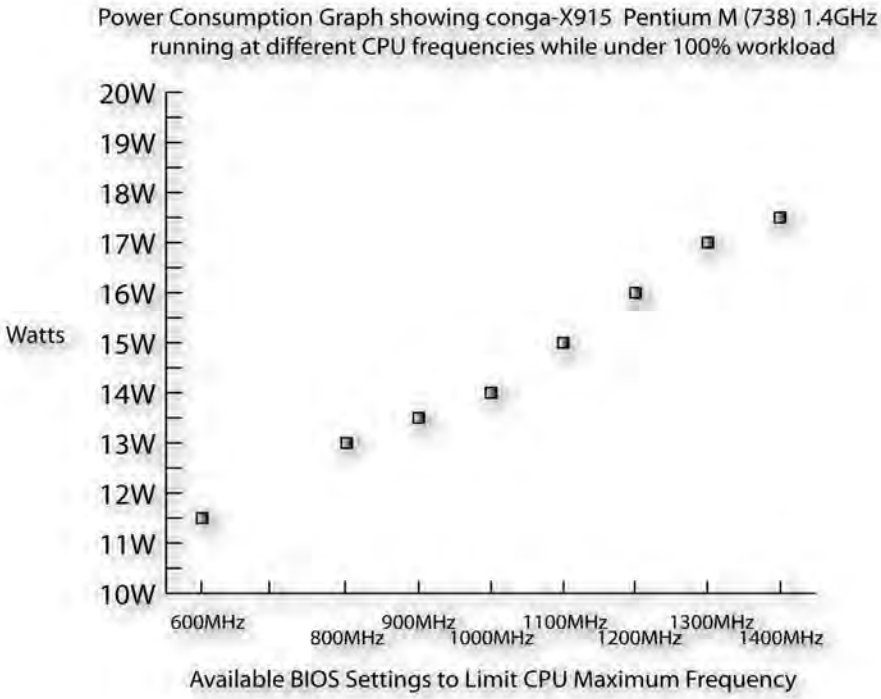
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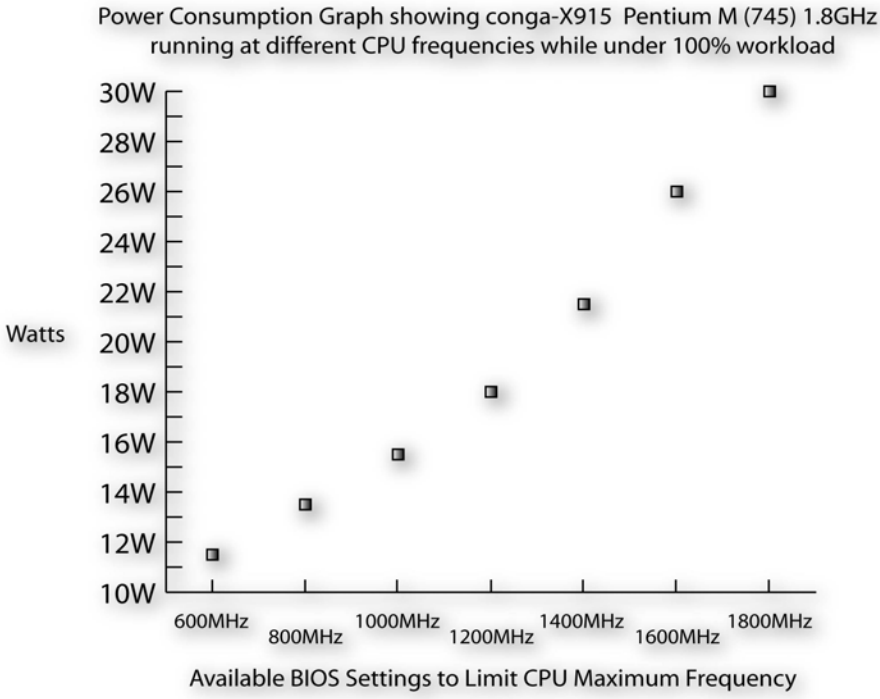
If the "Home/Office" or "Always On" power scheme is selected when using Windows operating systems then the processor will always run at the highest performance state. For more information about this subject see chapter 8 of the ACPI Specification Revision 2.0c, which can be found at www.acpi.info. Also visit Microsoft's website and search for the document called "Windows Native Processor Performance Control".

The congatec BIOS allows you to limit the maximum processor frequency. This can be useful if the maximum performance is not required or if the maximum processor performance state dissipates too much power and heat.

In the 'CPU Configuration' submenu of the 'BIOS Setup Program' you'll find the node for 'Max. Frequency' limitation. For each Pentium M processor the BIOS lists the supported frequencies. If a lower frequency than the maximum one is selected, the processor will never run at frequencies above this setting.

The following graphs provide examples of how each maximum frequency limitation setting, found in the 'BIOS Setup Program', affects power consumption of different Pentium M processors.





Celeron M processors do not support Enhanced Intel® SpeedStep® technology. They always run at a fixed frequency. In order to limit the performance and power consumption of Celeron M processors, the congatec BIOS offers 'On-Demand Clock

Modulation' support in the 'CPU Configuration' sub menu of the 'BIOS Setup Program'. When 'On-Demand Clock Modulation' is enabled, the processor clock is throttled using the duty cycle determined in setup. Keep in mind that the 'On-Demand' clock modulation duty cycle indicates that the clock on to clock off interval ratio. This means that when set to 75% the clock is running 75% of the overall time and this leads to a performance decrease of approximately 25%.

On the conga-X915 variant that is equipped with a Celeron M 800MHz cacheless CPU (article number 098636), the power consumption decreases approximately 0.7W when set to 75% duty cycle and 1.5W when set to 50% duty cycle.

6.5 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-X915 ACPI thermal solution offers three different cooling policies.

- Passive Cooling

  When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the “passive cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- Active Cooling

  During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the “active cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

- Critical Trip Point

  If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the “critical trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Notes

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled according to the formula below.

$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

- *ΔP is the performance delta*
- *T_t is the target temperature = critical trip point.*
- *The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants. These constants are set to fixed values for the conga-X915:*
- *TC1= 1*
- *TC2= 5*
- *TSP= 5 seconds*

See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

6.6 ACPI Suspend Modes and Resume Events

conga-X915 supports the S1 (POS= Power On Suspend) state and S3 (STR= Suspend to Ram). For more information about S3 wake events see section 9.4.1 “ACPI Configuration Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Win2K
- WinXP

The following table lists the “Wake Events” that resume the system from both S1 or S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S1-S5.
GPE1#	Only if configured as Lid Switch in the ACPI setup menu. Additionally the lid button has to be activated using the Windows Power Options. The best way to use it is to go to Standby (see note below) on lid button press and wake from Standby (see note below) on lid button release.
GPE2#	Set GPE2 Function node to Sleep Button in the ACPI setup menu or set Resume On Ring to Enabled in the Power setup menu.
Onboard LAN Event	Device driver must be configured for Wake On LAN support. For configuration go to Device Manager, Network Adapters, Intel(R) PRO/100 VE Network Connection and launch properties. Power Management: Allow this device to bring the computer out of standby. Advanced->Wake on LAN Options->Properties: Enable PME:Enabled Wake On Link Settings: Forced

Wake Event	Conditions/Remarks
	Wake On Settings: Wake on Magic & Directed Using this configuration the system will wake from Standby (see note below) in case a magic packet or a directed packet is sent. Directed packet: e.g. ping to last IP / MAC address. If there is no network cable connected to the system when it goes to Standby (see note below) mode, the system will wake from Standby (see note below) as soon as a cable is connected.
SMBALERT#	Wakes unconditionally from S1-S5.
PCI Express WAKE#	Wakes unconditionally from S1-S3.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S1, no special action must be taken for a USB Mouse/Keyboard Event to be used as a Wake Event. When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event.. USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu. Under Windows XP add following registry entries: Add this key: HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\usb Under this key add the following value: „USBBIOSx“=DWORD:00000000 *Note that Windows XP disables USB wakeup from S3, so this entry has to be added to re-enable it.* Configure USB keyboard/mouse to be able to wake up the system: In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'. *Note: When the standby state is set to S3 in the ACPI setup menu, the power management tab for USB keyboard /mouse devices only becomes available after adding the above registry entry and rebooting to allow the registry changes to take affect.*
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu.
Watchdog Power Button Event	Wakes unconditionally from S1-S5.
PS/2 Mouse/Keyboard Event	Only can be used as a Wake Event when in S1 mode.

Note

The above list has been verified using a Windows XP SP2 ACPI enabled installation.

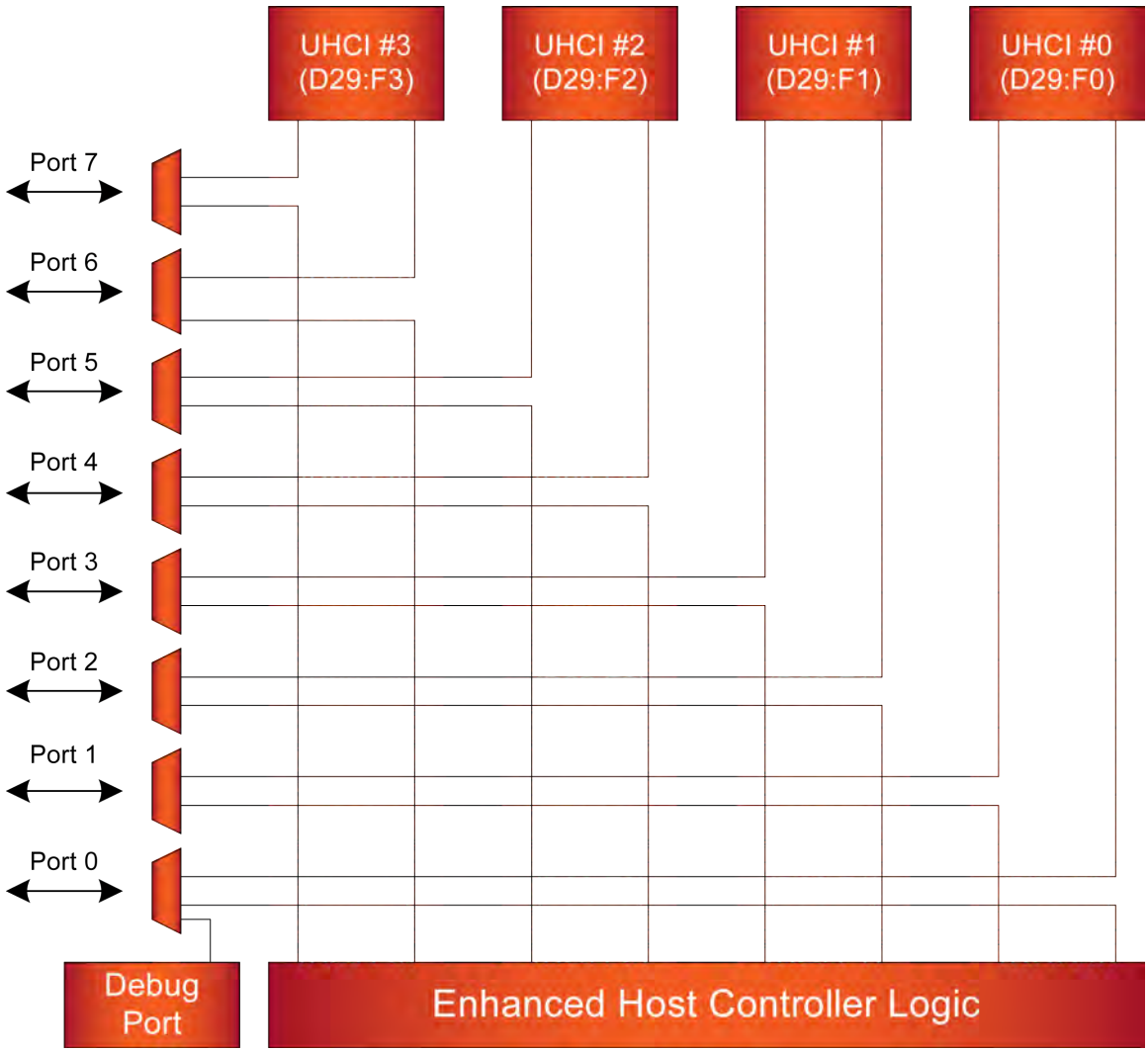
When using Windows XP, Standby mode is either an S1 state or S3 state depending on what has been selected in the ACPI Configuration Menu in the BIOS setup program. For more information about this see section 9.4.1 of this document.

6.7 USB 2.0 EHCI Host Controller Support

The 8 USB ports are shared between an EHCI host controller and the 4 UHCI host controllers. Only 6 (USB ports 0-5) of the available 8 USB ports and only 3 (UHCI 0-2) of the available 4 UHCI host controllers are supported on the conga-X915.

Within the EHC functionality there is a port-routing logic that executes the mixing between the two different types of host controllers (EHCI and UHCI). This means that when a USB device is connected the routing logic determines who owns the port. If the device is not USB 2.0 compliant, or if the software drivers for EHCI support are not installed, then the UHCI controller owns the ports.

Routing Diagram:



7 Signal Descriptions and Pinout Tables

The following section describes the signals found on the four X connectors located on the bottom of the module. X1, X3, and X4 connectors are ETX® standard compliant while the X2 connector complies with the XTX™ extension specification. Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a XTX® module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 2 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
SATA	In compliance with Serial ATA specification, Revision 1.0a
LVDS	Low Voltage Differential Signal-350mV nominal; 450mV maximum differential signal
TPM	Trusted Platform Module

7.1 X1 Connector Signal Descriptions

Table 3 Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC ±5%	P		External supply
GND	Power Ground	P		External supply
3V	Power Supply +3.3VDC	P		See section 4.1.4
N.C.	Not Connected	N.A.		Do not connect
SERIRQ	Serial Interrupt request	I 3.3V	PU 10K 3.3V	

Table 4 PCI Signal Descriptions

Signal	Description of PCI Bus Signals	I/O	PU/PD	Comment
PCICLK1..4.	Clock output	O 3.3V		
REQ0..3#	Bus request	I 3.3V	PU 8k2 3.3V	REQ1..3# is a boot strap signal (see note below) 5V Tolerant
GNT0..3#	Bus grant	O 3.3V		
AD0..31	Address/Data bus lines	I/O 3.3V		5V Tolerant
CBE0..3#	Bus command/byte enables	I/O 3.3V		5V Tolerant
PAR	Bus parity	I/O 3.3V		5V Tolerant
SERR#	Bus system error	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
GPERR#	Bus grant parity error	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
PME#	Bus power management event	I/O 3.3VSB		
LOCK#	Bus lock	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
DEVSEL#	Bus device select	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
TRDY#	Bus target ready	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
IRDY#	Bus initiator ready	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
STOP#	Bus stop	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
FRAME#	Bus frame	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
PCIRST#	Bus reset	O 3.3V		Asserted during system reset
INTA#	Bus interrupt A	I 3.3V	PU 10K 3.3V	5V Tolerant
INTB#	Bus interrupt B	I 3.3V	PU 10K 3.3V	5V Tolerant
INTC#	Bus interrupt C	I 3.3V	PU 10K 3.3V	5V Tolerant
INTD#	Bus interrupt D	I 3.3V	PU 10K 3.3V	5V Tolerant

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.9 of this user's guide.

Table 5 USB Signal Descriptions

Signal	Description of USB Signals	I/O	PU/PD	Comment
USB0	USB Port 0, data + or D+	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB0#	USB Port 0, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB1	USB Port 1, data + or D+	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB1#	USB Port 1, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB2	USB Port 2, data + or D+	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB2#	USB Port 2, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB3	USB Port 3, data + or D+	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB3#	USB Port 3, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1

Table 6 Audio Signal Descriptions

Signal	Description of Audio Signals	I/O	PU/PD	Comment
SNDL	Line-Level stereo output left	O		Analog output (1 Vrms)
SNDR	Line-Level stereo output right	O		Analog output (1 Vrms)
AUXAL	Auxiliary input A left	I	22k PD	Analog input (1 Vrms)
AUXAR	Auxiliary input A right	I	22k PD	Analog input (1 Vrms)
MIC	Microphone input	I	2k2 PU AudioVref	Analog input (1 Vrms)
ASGND	Analog ground of sound controller	P		
ASVCC	Analog supply of sound controller	P		

7.2 Connector X1 Pinout

Table 7 X1 Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	PCICLK3	4	PCICLK4	53	PAR	54	SERR#
5	GND	6	GND	55	GPERR#	56	Reserved
7	PCICLK1	8	PCICLK2	57	PME#	58	USB2#
9	REQ3#	10	GNT3#	59	LOCK#	60	DEVSEL#
11	GNT2#	12	3V	61	TRDY#	62	USB3#
13	REQ2#	14	GNT1#	63	IRDY#	64	STOP#
15	REQ1#	16	3V	65	FRAME#	66	USB2
17	GNT0#	18	RESERVED	67	GND	68	GND
19	VCC	20	VCC	69	AD16	70	CBE2#
21	SERIRQ	22	REQ0#	71	AD17	72	USB3
23	AD0	24	3V	73	AD19	74	AD18
25	AD1	26	AD2	75	AD20	76	USB0#
27	AD4	28	AD3	77	AD22	78	AD21
29	AD6	30	AD5	79	AD23	80	USB1#
31	CBE0#	32	AD7	81	AD24	82	CBE3#
33	AD8	34	AD9	83	VCC	84	VCC
35	GND	36	GND	85	AD25	86	AD26
37	AD10	38	AUXAL	87	AD28	88	USB0
39	AD11	40	MIC	89	AD27	90	AD29
41	AD12	42	AUXAR	91	AD30	92	USB1
43	AD13	44	ASVCC	93	PCIRST#	94	AD31
45	AD14	46	SNDL	95	INTC#	96	INTD#
47	AD15	48	ASGND	97	INTA#	98	INTB#
49	CBE1#	50	SNDR	99	GND	100	GND

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7.3 X2 Connector Signal Descriptions (XTX™ extension)

Table 8 LPC Interface Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
LPC_AD[0..3]	Multiplexed Command, Address and Data.	I/O 3.3V		
LPC_FRAME#	Frame: Indicates start of a new cycle or termination of a broken cycle.	O 3.3V		
LPC_DRQ[0..1]#	Encoded DMA/Bus Master Request.	I 3.3V		

Table 9 Serial ATA Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA0_TX+ SATA0_TX-	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA1_RX+ SATA1_RX-	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA1_TX+ SATA1_TX-	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA2_RX+ SATA2_RX-	Serial ATA channel 2, Receive Input differential pair.	N.C.		Not supported
SATA2_TX+ SATA2_TX-	Serial ATA channel 2, Transmit Output differential pair.	N.C.		Not supported
SATA3_RX+ SATA3_RX-	Serial ATA channel 3, Receive Input differential pair.	N.C.		Not supported
SATA3_TX+ SATA3_TX-	Serial ATA channel 3, Transmit Output differential pair.	N.C.		Not supported
IL_SATA#	Serial ATA Interlock Switch Input.	I 3.3V	PU 10K 3.3V	
SATALED#	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V	-	SATALED# is a boot strap signal (see note below)

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.9 of this user's guide.

Table 10 PCI Express Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE0_TX+ PCIE0_TX-	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE1_RX+ PCIE1_RX-	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE1_TX+ PCIE1_TX-	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE2_RX+ PCIE2_RX-	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE2_TX+ PCIE2_TX-	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE3_RX+ PCIE3_RX-	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE3_TX+ PCIE3_TX-	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_CLK_REF+ PCIE_CLK_REF-	PCI Express Reference Clock for Lanes 0 to 3.	O PCIE	PD 49.9R	Refer to XTX design guide for additional information
PCE_WAKE#	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I 3.3VSB	PU 1K 3.3VSB	

Note

AC_SYNC and AC_SDOUT can be used to switch PCI Express channels 0-3 between x1 and x4 mode. If both signals are each pulled-up (using 1k Ω resistors) to 3.3V at the rising edge of PWROK then x4 mode is enabled. x1 mode is used by default if these resistors are not populated.

For more information refer to section 7.9 of this user's guide.

Table 11 ExpressCard Support Pins Descriptions

Signal	Description	I/O	PU/PD	Comment
EXEC_CPPE[0..1]#	ExpressCard capable card request.	I 3.3V	PU 8k2 3.3V	
EXEC_RST[0..1]#	ExpressCard Reset	O 3.3V	PU 10k 3.3V	

Table 12 Audio Codec Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
AC_RST#	CODEC Reset	O 3.3V		
AC_SYNC	Serial Bus Synchronization.	O 3.3V		AC_SYNC is a boot strap signal (see note below)
AC_BIT_CLK	12.228 MHz Serial Bit Clock from CODEC.	O 3.3V		
AC_SDOUT	Audio Serial Data Output to CODEC.	O 3.3V		AC_SDOUT is a boot strap signal (see note below)
AC_SDIN[0..2]	Audio Serial Data Input from CODEC0..CODEC2.	I 3.3V	Only AC_SDIN2 is PD 10k	
CODECSET	Disable onboard Audio Codec.	I 3.3V	PD 10k	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module.

AC_SYNC and AC_SDOUT can be used to switch PCI Express channels 0-3 between x1 and x4 mode. If both signals are each pulled-up (using 1k Ω resistors) to 3.3V at the rising edge of PWROK then x4 mode is enabled. x1 mode is used by default if these resistors are not populated.

For more information refer to section 7.9 of this user's guide.

Table 13 USB Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
USBP4	USB Port 4, data + or D+	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USBP4#	USB Port 4, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USBP5	USB Port 5, data + or D+	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USBP5#	USB Port 5, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1

Table 14 Miscellaneous Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
GND	Ground. All GND pins should be connected to the baseboard ground plane.	P		
5V_SB	Additional Power input for the internal suspend and power-control circuitry. This signal is connected to XTX-Connector X4/Pin3. Refer to XTX Specification for further details.	P		
VCC	5V Power Input. All VCC pins should be connected to the baseboard 5 Volt power plane.	P		
SUS_STAT#	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3VSB		
SLP_S3#	S3 Sleep Control: This signal shuts off power to all non-critical systems when in S3 (Suspend to Ram), S4 or S5 states.	O 3.3VSB	PU 10k 3.3VSB	
SLP_S5#	S5 Sleep Control: This signal shuts off power to all non-critical systems when in S5 (Soft Off) state.	O 3.3VSB	PU 10k 3.3VSB	
PCI_CLKRUN#	PCI Clock Run: This signal is used to support PCI Clock Run protocol. It connects to PCI devices that need to request clock re-start, or prevention of clock stopping.	O 3.3VSB	PU 10k 3.3VSB	
PCI_GNT#A	reserved	O 3.3V		
PCI_REQ#A	reserved	I 3.3V	PU 10k 3.3V	
FAN_PWMOUT	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O 5V		
FAN_TACHOIN	Fan tachometer input.	I 5V		Requires a fan with a two pulse output.
WDTRIG	Watch Dog Trigger signal.	I 5V	PU 10k 5V	Trigger source should have OC output.
PP_TPM	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V		Trusted Platform Module chip is optional.

7.4 X2 Connector Pinout

The following table includes a reference column describing the corresponding ETX standard X2 connector pinout.

Table 15 X2 Connector Pinout

Pin	XTX™ Signal	*ETX® Reference*	Pin	XTX™ Signal	*ETX® Reference*
1	GND	GND	2	GND	GND
3	PCIE_CLK_REF+	SD14	4	SATA0_RX+	SD15
5	PCIE_CLK_REF-	SD13	6	SATA0_RX-	MASTER#
7	GND	SD12	8	GND	DREQ7
9	PCIE3_TX+	SD11	10	SATA0_TX-	DACK7#
11	PCIE3_TX-	SD10	12	SATA0_TX+	DREQ6
13	GND	SD9	14	5V_SB	DACK6#
15	PCIE3_RX+	SD8	16	SATA1_RX+	DREQ5
17	PCIE3_RX-	MEMW#	18	SATA1_RX-	DACK5#
19	VCC	MEMR#	20	5V_SB	DREQ0
21	EXC1_CPPE#	LA17	22	SATA1_TX-	DACK0#
23	EXC1_RST#	LA18	24	SATA1_TX+	IRQ14
25	USBP5	LA19	26	GND	IRQ15
27	USBP5#	LA20	28	SATA2_RX+(*)	IRQ12
29	GND	LA21	30	SATA2_RX-(*)	IRQ11
31	PCIE2_TX+	LA22	32	SUS_STAT#	IRQ10
33	PCIE2_TX-	LA23	34	PCI_CLKRUN#	IO16#
35	GND	GND	36	GND	GND
37	PCIE2_RX+	SBHE#	38	SATA2_TX-(*)	M16#
39	PCIE2_RX-	SA0	40	SATA2_TX+(*)	OSC
41	EXC0_CPPE#	SA1	42	GND	BALE
43	EXC0_RST#	SA2	44	SATA3_RX+(*)	TC
45	USBP4	SA3	46	SATA3_RX-(*)	DACK2#
47	USBP4#	SA4	48	WDTRIG	IRQ3
49	SLP_S3#	SA5	50	SATALED#	IRQ4
51	VCC	VCC	52	VCC	VCC
53	PCIE1_RX-	SA6	54	SATA3_TX-(*)	IRQ5
55	PCIE1_RX+	SA7	56	SATA3_TX+(*)	IRQ6
57	GND	SA8	58	IL_SATA#	IRQ7
59	PCIE1_TX-	SA9	60	PP_TPM	SYSCLK
61	PCIE1_TX+	SA10	62	RESERVED	REFSH#
63	PCE_WAKE#	SA11	64	PCI_GNT#A(*)	DREQ1
65	SLP_S5#	SA12	66	PCI_REQ#A(*)	DACK1#

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Pin	XTX™ Signal	*ETX® Reference*	Pin	XTX™ Signal	*ETX® Reference*
67	GND	GND	68	GND	GND
69	PCIE0_RX-	SA13	70	RESERVED	DREQ3
71	PCIE0_RX+	SA14	72	RESERVED	DACK3#
73	GND	SA15	74	VCC	IOR#
75	PCIE0_TX-	SA16	76	RESERVED	IOW#
77	PCIE0_TX+	SA18	78	RESERVED	SA17
79	CODECSET	SA19	80	VCC	SMEMR#
81	AC_RST#	IOCHRDY	82	AC_SDOUT	AEN
83	VCC	VCC	84	VCC	VCC
85	AC_SYNC	SD0	86	AC_SDIN0	SMEMW#
87	AC_SDIN1	SD2	88	AC_SDIN2	SD1
89	AC_BIT_CLK	SD3	90	FAN_TACHOIN	NOWS#
91	LPC_AD0	DREQ2	92	FAN_PWMOUT	SD4
93	LPC_AD1	SD5	94	LPC_FRAME#	IRQ9
95	LPC_AD2	SD6	96	LPC_DRQ0#	SD7
97	LPC_AD3	IOCHK#	98	LPC_DRQ1#	RSTDRV
99	GND	GND	100	GND	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-X915.

7.5 X3 Connector Signal Descriptions

Table 16 Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC, ±5%	P		External supply
GND	Power Ground	P		External supply
N.C.	Not connected	N.A.		Do not connect
LTGIO0	Not connected	N.C.		Not supported

Table 17 CRT Signal Descriptions

Signal	Description of CRT signals	I/O	PU/PD	Comment
HSY	Horizontal Synchronization Pulse	O 3.3V		
VSY	Vertical Synchronization Pulse	O 3.3V		
R	Red channel RGB Analog Video Output	O	PD 150R	Analog output
G	Green channel RGB Analog Video Output	O	PD 150R	Analog output
B	Blue channel RGB Analog Video Output	O	PD 150R	Analog output
DDCK	Display Data Channel Clock	I/O 5V	PU 2k2 5V	
DDDA	Display Data Channel Data	I/O 5V	PU 2k2 5V	

Table 18 TV Signal Descriptions

Signal	Description of CRT signals	I/O	PU/PD	Comment
SYNC	Composite sync	N.C.		Not supported
Y	Luminance for S-Video or Red for SCART	O	PD 150R	Not supported
C	Chrominance for S-Video or Green for SCART	O	PD 150R	Not supported
COMP	Composite Video or Blue for SCART	O	PD 150R	Not supported

Table 19 COM Signal Descriptions

Signal	Description of COM signals	I/O	PU/PD	Comment
DTR1#	Data terminal ready for COM1	O 5V	PU 4k7 5V	DTR1# is a boot strap signal (see note below)
DTR2#	Data terminal ready for COM2	O 5V	PD 100k 5V	
RI1#, RI2#	Ring indicator for COM1/COM2	I 5V	PD 100k 5V	
TXD1, TXD2	Data transmit for COM1/COM2	O 5V	PU 4k7 5V	TXD1 and TXD2 are boot strap signals (see note below)
RXD1, RXD2	Data receive for COM1/COM2	I 5V	PD 100k 5V	
CTS1#, CTS2#	Clear to send for COM1/COM2	I 5V	PD 100k 5V	
RTS1#	Request to send for COM1	O 5V	PD 4k7	RTS1# is a boot strap signal (see note below)
RTS2#	Request to send for COM2	O 5V	PD 100k 5V	
DCD1#, DCD2#	Data carrier detect for COM1/COM2	I 5V	PD 100k 5V	
DSR1#, DSR2#	Data set ready for COM1/COM2	I 5V	PD 100k 5V	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.9 of this user's guide.

Table 20 Keyboard and Infrared Signal Descriptions

Signal	Description of keyboard and infrared signals	I/O	PU/PD	Comment
KBDAT	Keyboard Data	I/O 5V	PU 4k7 5V	
KBCLK	Keyboard Clock	O 5V	PU 4k7 5V	
MSDAT	Mouse Data	I/O 5V	PU 4k7 5V	
MSCLK	Mouse Clock	O 5V	PU 4k7 5V	
IRTX	Infrared Transmit	O 5V		
IRRX	Infrared Receive	I 5V		

Table 21 LVDS Flat Panel Signals

Signal	Description of LVDS Flat Panel signals	I/O	PU/PD	Comment
BIASON	Controls display contrast voltage ON	N.C.		Not supported
DIGON	Controls display Power ON	O 5V	PD 10k	
BLON#	Controls display Backlight ON	O 5V		
LCDDO0..19	LVDS channel data 0..19	O LVDS		
DETECT#	Panel hot-plug detection	N.C.		Not supported
FPDDC_CLK	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
FPDDC_DAT	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

Table 22 LVDS Interface Pinout

Pin	Signal Name	Signal Mapping	Pin	Signal Name	Signal Mapping
1	GND		2	GND	
3	R		4	B	
5	HSY		6	G	
7	VSY		8	DDCK	
9	DETECT# (*)		10	DDDA	
11	LCDDO[16]	TX2OUTCLK-	12	LCDDO[18]	TX2OUT3-
13	LCDDO[17]	TX2OUTCLK+	14	LCDDO[19]	TX2OUT3+
15	GND		16	GND	
17	LCDDO[13]	TX2OUT1+	18	LCDDO[15]	TX2OUT2+
19	LCDDO[12]	TX2OUT1-	20	LCDDO[14]	TX2OUT2-
21	GND		22	GND	
23	LCDDO[8]	TX1OUT3-	24	LCDDO[11]	TX2OUT0+
25	LCDDO[9]	TX1OUT3+	26	LCDDO[10]	TX2OUT0-
27	GND		28	GND	
29	LCDDO[4]	TX1OUT2-	30	LCDDO[7]	TX1OUTCLK+
31	LCDDO[5]	TX1OUT2+	32	LCDDO[6]	TX1OUTCLK-
33	GND		34	GND	
35	LCDDO[1]	TX1OUT0+	36	LCDDO[3]	TX1OUT1+
37	LCDDO[0]	TX1OUT0-	38	LCDDO[2]	TX1OUT1-
39	VCC		40	VCC	
41	FPDDC_DAT		42	LTGIO0 (*)	
43	FPDDC_CLK		44	BLON#	
45	BIASON (*)		46	DIGON	
47	COMP (*)		48	Y (*)	
49	SYNC (*)		50	C (*)	

TX1= Channel 1 transmit
TX2= Channel 2 transmit

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-X915.

Table 23 FDC Signal Descriptions

Signal	Description of FDC signals (shared with LPT)	I/O	PU/PD	Comment
FLPY#	Floppy Interface configuration input	N.A.		Not supported, see section 4.3.6 for more information.
RES	N.C.	N.A.		Not available
DENSEL	Density select: low = 250/300Kb/s high = 500/1000Kb/s	O 5V		
INDEX#	Index signal	I 5V		
TRK0#	Track signal	I 5V		
WP#	Write protect signal	I 5V		
RDATA#	Raw data read	I 5V		
DSKCHG#	Disk change	I 5V		
HDSEL#	Head select	O 5V		
DIR#	Direction	O 5V		
STEP#	Motor step	O 5V		
DRV	Drive select	O 5V		
MOT#	Motor select	O 5V		
WDATA#	Raw write data	O 5V		
WGATE#	Write enable	O 5V		

Table 24 Floppy Support Mode Pinout

Floppy Support Mode Pinout			
Pin	Signal	Pin	Signal
51	FLPY# (*)	52	RESERVED
53	VCC	54	GND
55	RESERVED	56	DENSEL
57	RESERVED	58	RESERVED
59	IRRX	60	HDSEL#
61	IRTX	62	RESERVED
63	RXD2	64	DIR#
65	GND	66	GND
67	RTS2#	68	RESERVED
69	DTR2#	70	STEP#
71	DCD2#	72	DSKCHG#
73	DSR2#	74	RDATA#
75	CTS2#	76	WP#
77	TXD2	78	TRK0#
79	RI2#	80	INDEX#
81	VCC	82	VCC
83	RXD1	84	DRV
85	RTS1#	86	MOT
87	DTR1#	88	WDATA#
89	DCD1#	90	WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-X915.

Table 25 LPT Signal Descriptions

Signal	Description of LPT signals (shared with FDC)	I/O	PU/PD	Comment
LPT	LPT Interface configuration input	N.A.		Not supported, see section 4.3.6 for more information.
STB#	Strobe signal	O 5V		
AFD#	Automatic feed	O 5V		
PD0	Data bus D0	I/O 5V		
PD1	Data bus D1	I/O 5V		
PD2	Data bus D2	I/O 5V		
PD3	Data bus D3	I/O 5V		
PD4	Data bus D4	I/O 5V		
PD5	Data bus D5	I/O 5V		
PD6	Data bus D6	I/O 5V		
PD7	Data bus D7	I/O 5V		
ERR#	LPT error	I 5V		
INIT#	Initiate	O 5V		
SLIN#	Select	O 5V		
ACK#	Acknowledge	I 5V		
BUSY	Busy	I 5V		
PE	Paper empty	I 5V		
SLCT	Power On	I 5V		

Table 26 LPT Support Mode Pinout

Parallel Port Mode Pinout			
Pin	Signal	Pin	Signal
51	LPT (*)	52	RESERVED
53	VCC	54	GND
55	STB#	56	AFD#
57	RESERVED	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2#	80	PD0
81	VCC	82	VCC
83	RXD1	84	ACK#
85	RTS1#	86	BUSY
87	DTR1#	88	PE
89	DCD1#	90	SLCT
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-X915.

7.6 X4 Connector Signal Descriptions

Table 27 Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC, ±5%	P		External supply
GND	Power Ground	P		External supply
N.C.	Not connected	N.A.		Do not connect
PIDE	Refers to Primary IDE channel	I/O		
SIDE	Refers to Secondary IDE channel	N.C.		Not supported

Table 28 IDE Signal Descriptions

Signal	Description of IDE signals	I/O	PU/PD	Comment
PIDE_D0..15	Primary IDE Data bus	I/O 3.3V		5V tolerant
PIDE_A0..2	Primary IDE Address bus	O 3.3V		
PIDE_CS1#	Primary IDE chip select channel 0	O 3.3V		
PIDE_CS3#	Primary IDE chip select channel 1	O 3.3V		
PIDE_DRQ	Primary IDE DMA request	I 3.3V		5V tolerant
PIDED_AK#	Primary IDE DMA acknowledge	O 3.3V		
PIDE_RDY	Primary IDE ready	I 3.3V	PU 4k7 3.3V	5V tolerant
PIDE_IOR#	Primary IDE IO read	O 3.3V		
PIDE_IOW#	Primary IDE IO write	O 3.3V		
PIDE_INTRQ	Primary IDE interrupt request	I 3.3V	PU 8k2 3.3V	5V tolerant
SIDE_D0..15	Secondary IDE Data bus	N.C.		
SIDE_A0..2	Secondary IDE Address bus	N.C.		
SIDE_CS1#	Secondary IDE chip select channel0	N.C.		
SIDE_CS3#	Secondary IDE chip select channel1	N.C.		
SIDE_DRQ	Secondary IDE DMA request	N.C.		
SIDED_AK#	Secondary IDE DMA acknowledge	N.C.		
SIDE_RDY	Secondary IDE ready	N.C.		
SIDE_IOR#	Secondary IDE IO read	N.C.		
SIDE_IOW#	Secondary IDE IO write	N.C.		
SIDE_INTRQ	Secondary IDE interrupt request	N.C.		
DASP_S	Secondary IDE Drive active	N.C.		
PDIAG_S	Secondary IDE Master/Slave negotiation	N.C.		
HDRST#	Hard Drive reset	O 5V		
CBLID_P#	Primary IDE 80 pin cable detect	I 3.3V	PD 10k	

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Table 29 Ethernet Signal Descriptions

Signal	Description of Ethernet signals	I/O	PU/PD	Comment
TXD#, TXD	Ethernet transmit signal pair	O		Signals for external transformer
RXD#, RXD	Ethernet receive signal pair	I		Signals for external transformer
ACTLED#	Ethernet activity LED	O 3.3V		
LILED#	Ethernet link LED	O 3.3V		
SPEEDLED#	Ethernet speed LED, ON at 100Mb/s	O 3.3V		

Table 30 Power Control Signals

Signal	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	Power good input	I		Also usable as reset input, make low with O.C. to cause reset.
5V_SB	Supply of internal suspend circuit	P		
PS_ON#	Power Save ON	O 5VSB	PU 10k 5VSB	
PWRBTN#	Power Button	I 5VSB	PU 10k 5VSB	

Table 31 Power Management Signals

Signal	Description of Power Management signals	I/O	PU/PD	Comment
RSMRST#	Resume / reset input	I 3.3VSB	PU 100k 3.3VSB	
SMBALRT#	System management bus alert input	I 3.3VSB	PU 10k 3.3VSB	
BATLOW#	Battery low input	I 3.3VSB	PU 10k 3.3VSB	
GPE1#	General purpose power management event input 1	I 3.3VSB	PU 10k 3.3VSB	
GPE2#	General purpose power management event input 2	I 3.3VSB	PU 10k 3.3VSB	
EXTSMI#	System management interrupt input	I 3.3VSB	PU 10k 3.3VSB	

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Table 32 Miscellaneous Signal Descriptions

Signal	Description of Miscellaneous signals	I/O	PU/PD	Comment
SPEAKER	Speaker output	O 3.3V		SPEAKER is a boot strap signal (see note below)
BATT	Battery supply	I		
I²CLK	I²C Bus clock	I/O 5V	PU 4k7 5V	
I²DAT	I²C Bus Data	I/O 5V	PU 4k7 5V	
SMBCLK	SM Bus clock	I/O 3.3V	PU 2k2 3.3V	
SMBDATA	SM Bus Data	I/O 3.3V	PU 2k2 3.3V	
KBINH#	Keyboard inhibit	I 5V		
OVCR#	Over current detect for USB	I 3.3VSB	PU 10k 3.3VSB	
ROMKBCS#	Do not connect	N.A.		Not available
EXT_PRG	Do not connect	N.A.		Not available
GPCS#	General purpose chip select	N.C.		Not supported

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.9 of this user's guide.

7.7 X4 Connector Pinout

Table 33 Connector X4 Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	SIDE_IOW#(*)	52	PIDE_IOR#
3	5V_SB	4	PWGIN	53	SIDE_DRQ(*)	54	PIDE_IOW#
5	PS_ON#	6	SPEAKER	55	SIDE_D15(*)	56	PIDE_DRQ
7	PWRBTN#	8	BATT	57	SIDE_D0(*)	58	PIDE_D15
9	KBINH#	10	LILED#	59	SIDE_D14(*)	60	PIDE_D0
11	RSMRST#	12	ACTLED#	61	SIDE_D1(*)	62	PIDE_D14
13	ROMKBCS#(*)	14	SPEEDLED#	63	SIDE_D13(*)	64	PIDE_D1
15	EXT_PRG(*)	16	I2CLK	65	GND	66	GND
17	VCC	18	VCC	67	SIDE_D2(*)	68	PIDE_D13
19	OVCR#	20	GPCS#(*)	69	SIDE_D12(*)	70	PIDE_D2
21	EXTSMI#	22	I2DAT	71	SIDE_D3(*)	72	PIDE_D12
23	SMBCLK	24	SMBDATA	73	SIDE_D11(*)	74	PIDE_D3
25	SIDE_CS3#(*)	26	SMBALRT#	75	SIDE_D4(*)	76	PIDE_D11
27	SIDE_CS1#(*)	28	DASP_S(*)	77	SIDE_D10(*)	78	PIDE_D4
29	SIDE_A2(*)	30	PIDE_CS3#	79	SIDE_D5(*)	80	PIDE_D10
31	SIDE_A0(*)	32	PIDE_CS1#	81	VCC	82	VCC
33	GND	34	GND	83	SIDE_D9(*)	84	PIDE_D5
35	PDIAG_S(*)	36	PIDE_A2	85	SIDE_D6(*)	86	PIDE_D9
37	SIDE_A1(*)	38	PIDE_A0	87	SIDE_D8(*)	88	PIDE_D6
39	SIDE_INTRQ(*)	40	PIDE_A1	89	GPE2#	90	CBLID_P#
41	BATLOW#	42	GPE1#	91	RXD#	92	PIDE_D8
43	SIDE_AK#(*)	44	PIDE_INTRQ	93	RXD	94	SIDE_D7(*)
45	SIDE_RDY(*)	46	PIDE_AK#	95	TXD#	96	PIDE_D7
47	SIDE_IOR#(*)	48	PIDE_RDY	97	TXD	98	HDRST#
49	VCC	50	VCC	99	GND	100	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-X915.

7.8 SDVO Connector X6

Connector and flat foil cable information for the SDVO connector (X6) located on the bottom side of the conga-X915.



- Connector type Hirose 0.5mm Pitch Bottom Contact Type
  Order no. FH12-45S-0.5SH (55)
- FFC type 45 positions, 30cm length, 0.5mm pitch both ends opposite sides
  Manufacturer YOUNGSHIN
  Order No. MCAB45x300B05

Table 34 SDVO Pinout Description

Pin	Signal	Description	PU/PD
1	GND	Ground	
2	SDVOC_BCLKN	Serial Digital Video C clock complement.	
3	SDVOC_BCLKP	Serial Digital Video C clock.	
4	GND	Ground	
5	SDVOC_GREEN#	Serial Digital Video C green complement.	
6	SDVOC_GREEN	Serial Digital Video C green.	
7	GND	Ground	
8	SDVOB_BCLKN	Serial Digital Video B clock complement .	
9	SDVOB_BCLKP	Serial Digital Video B clock.	
10	GND	Ground	
11	SDVOB_GREEN#	Serial Digital Video B green data complement.	
12	SDVOB_GREEN	Serial Digital Video B green data.	
13	GND	Ground	
14	SDVOC_INT#	Serial Digital Video input interrupt complement.	
15	SDVOC_INT	Serial Digital Video input interrupt.	
16	GND	Ground	
17	SDVOB_INT#	Serial Digital Video input interrupt complement.	
18	SDVOB_INT	Serial Digital Video input interrupt.	
19	GND	Ground	
20	SDVOC_BLUE#	Serial Digital Video C blue complement.	
21	SDVOC_BLUE	Serial Digital Video C blue data.	
22	GND	Ground	
23	SDVOC_RED#	Serial Digital Video C red data complement / alpha complement.	
24	SDVOC_RED	Serial Digital Video C red data / SDVO B alpha.	

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Pin	Signal	Description	PU/PD
25	GND	Ground	
26	SDVOB_BLUE#	Serial Digital Video B blue data complement.	
27	SDVOB_BLUE	Serial Digital Video B blue data.	
28	GND	Ground	
29	SDVOB_RED#	Serial Digital Video B red data complement.	
30	SDVOB_RED	Serial Digital Video B red data.	
31	GND	Ground	
32	SDVO_FLDSTALL#	Serial Digital Video field stall complement.	
33	SDVO_FLDSTALL	Serial Digital Video field stall.	
34	GND	Ground	
35	SDVO_TVCLKIN#	Serial Digital Video TV-Out synchronization clock complement.	
36	SDVO_TVCLKIN	Serial Digital Video TV-Out synchronization clock.	
37	GND	Ground	
38	SDVOCTRL_CLK	I²C based control signal (Clock) for SDVO device.	
39	SDVOCTRL_DATA	I²C based control signal (Data) for SDVO device.	SDVOCTRL_DATA is a boot strap signal (see note below)
40	PWRGOOD	PWRGOOD signal	PU 10k 3.3V
41	+5V	Power supply +5V	
42	+5V	Power supply +5V	
43	+5V	Power supply +5V	
44	SDAOUFP1	Custom	
45	SDAOUFP2	Custom	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.9 of this user's guide.

7.9 Boot Strap Signals

Table 35 Boot Strap signal Descriptions

Signal	Description of Boot Strap Signals	I/O	PU/PD	Comment
REQ1..3#	Bus request	I 3.3V	PU 8k2 3.3V	REQ1..3# is a boot strap signal (see caution statement below)
SATALED#	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V		SATALED# is a boot strap signal (see caution statement below)
AC_SYNC	Serial Bus Synchronization.	O 3.3V		AC_SYNC is a boot strap signal (see caution statement below)
AC_SDOUT	Audio Serial Data Output to CODEC.	O 3.3V		AC_SDOUT is a boot strap signal (see caution statement below)
DTR1#	Data terminal ready for COM1	O 5V	PU 4k7 5V	DTR1# is a boot strap signal (see caution statement below)
TXD1, TXD2	Data transmit for COM1/COM2	O 5V	PU 4k7 5V	TXD1 and TXD2 are boot strap signals (see caution statement below)
RTS1#	Request to send for COM1	O 5V	PD 4k7	RTS1# is a boot strap signal (see caution statement below)
SPEAKER	Speaker output	O 3.3V		SPEAKER is a boot strap signal (see caution statement below)
SDVOCTRL_DATA	I²C based control signal (Data) for SDVO device.			SDVOCTRL_DATA is a boot strap signal (see caution statement below)

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either XTX™ internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table with the exception of AC_SYNC, AC_SDOUT and SDVOCTRL_DATA. External resistors may override the internal strap states and cause the XTX™ module to malfunction and/or cause irreparable damage to the module.

AC_SYNC and AC_SDOUT can be used to switch PCI Express channels 0-3 between x1 and x4 mode. If both signals are each pulled-up (using 1k Ω resistors) to 3.3V at the rising edge of PWROK then x4 mode is enabled. x1 mode is used by default if these resistors are not populated.

SDVOCTRL_DATA can be pulled-up (using 5.6KΩ resistor) to 2.5V in order to tell the chipset to run in SDVO mode.

If it is necessary to drive a TTL input (or another input which sources or sinks significant current) that uses the TXD1 signal, a CMOS-input buffer can be inserted in the signal path so that this line is not pulled up or down by external circuitry during system reset.

8 System Resources

8.1 System Memory Map

Table 36 Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(TOM-192kB) – TOM	N.A.	192kB	ACPI reclaim, MPS and NVS area **
(TOM-8MB-192kB) – (TOM-192kB)	N.A.	1 or 8MB	VGA frame buffer *
1024kB – (TOM-8MB-192kB)	100000 – N.A	N.A.	Extended memory
869kB – 1024kB	E0000 - FFFFF	128kB	Runtime BIOS
800kB – 869kB	D0000 - DFFFF	64kB	Upper memory
640kB – 800kB	A0000 - DFFFF	92kB	Video memory and BIOS
639kB – 640kB	9FC00 - 9FFFF	1kB	Extended BIOS data
0 – 639kB	00000 - 9FC00	512kB	Conventional memory

Note

T.O.M. = Top of memory = max. DRAM installed
** VGA frame buffer can be reduced to 1MB in setup.*
*** Only if ACPI Aware OS is set to YES in setup.*

8.2 I/O Address Assignment

The I/O address assignment of the conga-X915 module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

Table 37 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
0100 - 010F	16 bytes	No	congatec System Control
0170 - 0177	8 bytes	No	Secondary IDE channel
01F0 - 01F7	8 bytes	No	Primary IDE channels
02F8 - 02FF	8 bytes	Note 1	Serial Port 2 (COM2)
0376	1 byte	No	Secondary IDE channel command port
0377	1 byte	No	Secondary IDE channel status port
0378 - 037F	8 bytes	Note 1	Parallel Port 1 (LPT1)
03B0 – 03DF	16 bytes	No	Video system
03F0 - 03F5	6 bytes	No	Floppy channel 1
03F6	1 byte	No	Primary IDE channel command port
03F7	1 byte	No	Primary IDE channel status port
03F8 - 03FF	8 bytes	Note 1	Serial Port 1 (COM1)
0480 – 04BF	64 bytes	No	Motherboard resources
04D0 – 04D1	2 bytes	No	Motherboard resources
0800 – 087F	128 bytes	No	Motherboard resources
0A00 – 0A0F	16 bytes	No	Motherboard resources
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
0D00 – FFFF		Note 2	PCI / PCI Express bus

Notes

1. *Default, but can be changed to another address range.*
2. *The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.*

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8.3 Interrupt Request (IRQ) Lines

Table 38 IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Note 1	Serial Port 2 (COM2)	IRQ3 via SERIRQ or PCI BUS INTx
4	Note 1	Serial Port 1 (COM1)	IRQ4 via SERIRQ or PCI BUS INTx
5	Yes		IRQ5 via SERIRQ or PCI BUS INTx
6	Note 1	Floppy Drive Controller	IRQ6 via SERIRQ or PCI BUS INTx
7	Note 1	Parallel Port 1 (LPT1)	IRQ7 via SERIRQ or PCI BUS INTx
8	No	Real-time Clock	Not applicable
9	Note 3	SCI	IRQ9 via SERIRQ or PCI BUS INTx
10	Yes		IRQ10 via SERIRQ or PCI BUS INTx
11	Yes		IRQ11 via SERIRQ or PCI BUS INTx
12	Note 1	PS/2 Mouse	IRQ12 via SERIRQ or PCI BUS INTx
13	No	Math processor	Not applicable
14	Note 1, 2	IDE Controller 0 (IDE0)	IRQ14 or PCI BUS INTx
15	Note 1, 2	IDE Controller 1 (IDE1)	IRQ15 or PCI BUS INTx

In PIC mode, the PCI bus interrupt lines can be routed to any free IRQ.

Notes

1. *Default, but can be changed to another interrupt. If disabled in BIOS setup resource can be used for another purpose.*
2. *If the ATA/IDE configuration is set to enhanced mode in BIOS setup (serial ATA and parallel ATA native mode operation), IRQ14 and 15 are free for PCI/LPC bus.*
3. *In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCI interrupt line.*

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Table 39 IRQ Lines in APIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Note 1	Serial Port 2 (COM2)	IRQ3 via SERIRQ
4	Note 1	Serial Port 1 (COM1)	IRQ4 via SERIRQ
5	Yes		IRQ5 via SERIRQ
6	Note 1	Floppy Drive Controller	IRQ6 via SERIRQ
7	Note 1	Parallel Port 1 (LPT1)	IRQ7 via SERIRQ
8	No	Real-time Clock	Not applicable
9	Note 3	SCI	IRQ9 via SERIRQ, option for SCI
10	Yes		IRQ10 via SERIRQ
11	Yes		IRQ11 via SERIRQ
12	Note 1	PS/2 Mouse	IRQ12 via SERIRQ
13	No	Math processor	Not applicable
14	Note 1, 2	IDE Controller 0 (IDE0)	IRQ14
15	Note 1, 2	IDE Controller 1 (IDE1)	IRQ15
16	No		PIRQA, Integrated VGA Controller, PCI Express Root Port 0, Intel High Definition Audio Controller (Azalia)
17	No		PIRQB, AC'97 Audio, PCI Express Root Port 1
18	No		PIRQC, Parallel ATA Controller in enhanced/native mode, UHCI Host Controller 2, PCI Express Root Port 2
19	No		PIRQD, Serial ATA controller in enhanced/native mode, UHCI Host Controller 1, SMBus Controller, PCI Express Root Port 3
20	Yes		PIRQE, PCI Bus INTA, onboard LAN Controller, option for SCI
21	Yes		PIRQF, PCI Bus INTB
22	Yes		PIRQG, PCI Bus INTC
23	Yes		PIRQH, PCI Bus INTD, UHCI Host Controller 0, EHCI Host Controller

In APIC mode, the PCI bus interrupt lines are connected with IRQ 20, 21, 22 and 23.

Notes

1. *Default but can be changed to another interrupt. If disabled in BIOS setup resource can be used for another purpose.*

2. *If the ATA/IDE configuration is set to enhanced mode in BIOS setup (serial ATA and parallel ATA native mode operation), IRQ14 and 15 are free for PCI/LPC bus.*

3. *In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCI interrupt line.*

8.4 Direct Memory Access (DMA) Channels

Table 40 DMA Channels

DMA#	Data Width	Available	Description
0	8 bits	Yes	
1	8 bits	Yes	
2	8 bits	Note 1	Floppy Drive Controller
3	8 bits	Note 2	Parallel Port (LPT)
4	16 bits	No	Cascade DMA Controller
5	16 bits	Yes	
6	16 bits	Yes	
7	16 bits	Yes	

Notes

1. *If the corresponding device is disabled in BIOS setup then the DMA channel can be used by customers hardware.*

2. *Not available if Parallel Port is used in ECP mode (Enhanced Parallel Port).*

8.5 PCI Configuration Space Map

Table 41 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	02h	00h	Internal	VGA Graphics
00h	02h	01h	N.A.	VGA Graphics
00h	1Bh	00h	Internal	Intel High Definition Audio Controller (Azalia)
00h (Note 1)	1Ch	00h	Internal	PCI Express Root Port 0
00h (Note 1)	1Ch	01h	Internal	PCI Express Root Port 1
00h (Note 1)	1Ch	02h	Internal	PCI Express Root Port 2
00h (Note 1)	1Ch	03h	Internal	PCI Express Root Port 3
00h	1Dh	00h	Internal	UHCI Host Controller 0
00h	1Dh	01h	Internal	UHCI Host Controller 1
00h	1Dh	02h	Internal	UHCI Host Controller 2
00h	1Dh	07h	Internal	EHCI Host Controller
00h	1Eh	00h	Internal	PCI to PCI Bridge
00h	1Eh	01h	Internal	AC97 Audio Controller
00h	1Fh	00h	N.A.	PCI to LPC Bridge
00h	1Fh	01h	Internal	Parallel ATA Controller in enhanced mode
00h	1Fh	02h	Internal	Serial ATA Controller in enhanced mode / Parallel ATA and Serial ATA as combined IDE Controller in compatible mode
00h	1Fh	03h	Internal	SMBus Host Controller
01h (Note 1)	00h	xxh	Internal	PCI Express Port 0
02h (Note 1)	00h	xxh	Internal	PCI Express Port 1
03h (Note 1)	00h	xxh	Internal	PCI Express Port 2
04h (Note 1)	00h	xxh	Internal	PCI Express Port 3
05h (Note 1)	08h	00h	Internal	Onboard LAN Controller
05h (Note 1)	03h	xxh	INTA-INTD	PCI Bus Slot 1
05h (Note 1)	04h	xxh	INTA-INTD	PCI Bus Slot 2
05h (Note 1)	05h	xxh	INTA-INTD	PCI Bus Slot 3
05h (Note 1)	06h	xxh	INTA-INTD	PCI Bus Slot 4

Notes

1. The given bus numbers only apply if all PCI Express Ports are enabled in the BIOS setup. If for example PCI Express Port 2 is disabled then PCI Express Port 3 will be

assigned bus number 2 instead of bus number 3, Port 4 will be assigned bus number 3 and the onboard LAN controller as well as the standard PCI slots will be assigned bus number 4. Furthermore, the respective PCI Express Root Port is hidden if the corresponding PCI Express Port is disabled.

8.6 PCI Interrupt Routing Map

Table 42 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line [1]	APIC Mode IRQ	VGA	Azalia HDA	UHCI 0	UHCI 1	UHCI 2	EHCI	PATA Native	SM Bus	AC97
A		16	x	x							
B		17									x
C		18					x		x		
D		19				x				x	
E	INTA	20									
F	INTB	21									
G	INTC	22									
H	INTD	23			x			x			

Table 43 PCI Interrupt Routing Map (continued)

PIRQ	LAN	SATA Native	PCI-EX Root Port 0	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	PCI-EX Port 0	PCI-EX Port 1	PCI-EX Port 2	PCI-EX Port 3
A			x				x [2]	x [3]	x [4]	x [5]
B				x	x		x [3]	x [4]	x [5]	x [2]
C						x	x [4]	x [5]	x [2]	x [3]
D		x					x [5]	x [2]	x [3]	x [4]
E	x									
F										
G										
H										

Notes

[1] These interrupts are available for external devices/slots on the X1 connector.
[2] Interrupt used by single function PCI Express devices (INTA).
[3] Interrupt used by multifunction PCI Express devices (INTB).
[4] Interrupt used by multifunction PCI Express devices (INTC).
[5] Interrupt used by multifunction PCI Express devices (INTD).

8.7 PCI Bus Masters

The conga X915 supports 4 external PCI Bus Masters. There are no limitations in connecting bus master PCI devices.

Note

If there are two devices connected to the same PCI REQ/GNT pair and they are transferring data at the same time then the latency time of these shared PCI devices can not be guaranteed.

8.8 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

8.9 SM Bus

System Management (SM) bus signals are connected to the Intel® I/O Controller Hub 82801FBM (ICH6M) and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

9 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

9.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> key during POST.

9.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used a message will be displayed during POST stating that the “Boot Selection Popup menu has been selected” and the menu itself will be displayed immediately after POST thereby allowing the operator to choose the boot device to be used.

9.1.2 Manufacturer Default Settings

Pressing the <End> key repeatedly, immediately after power is initiated will result in the manufacturer default settings being loaded for that boot sequence and only that boot sequence. This is helpful when a previous BIOS setting is no longer desired. If you want to change the BIOS settings, or save the manufacturer default settings, then you must enter the BIOS setup program and use the 'Save and Exit' function. This feature is enabled by default. See setup node in the “BIOS Setup Program” section 9.6.1 “Security Settings”.

9.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

Main	Advanced	Boot	Security	Power	Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2/F3	Change Colors of setup screen.
F7	Discard Changes.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

9.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab.

The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24-hour format.*
System Date	Day of week, month/day/year	Specifies the current system date. *Note: The date is in month-day-year format.*
BIOS ID	no option	Displays the BIOS ID.
Processor	no option	Displays the processor type.
CPU Frequency	no option	Displays CPU frequency.
System Memory	no option	Displays the total amount of system memory.
Product Revision	no option	Displays the hardware revision of the board
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215)
Running Time	no option	Displays the time the board is running [in hours max. 65535].

9.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Power	Exit
	ACPI Configuration				
	PCI Configuration				
	Graphics Configuration				
	CPU Configuration				
	Chipset Configuration				
	I/O Interface Configuration				
	Clock Configuration				
	IDE Configuration				
	USB Configuration				
	Keyboard/Mouse Configuration				
	Remote Access Configuration				
	Hardware Health Configuration				
	Watchdog Configuration				

9.4.1 ACPI Configuration Submenu

Feature	Options	Description
ACPI Aware O/S	No **Yes**	Set this value to allow the system to utilize the Intel ACPI (Advanced Configuration and Power Interface). Set to *NO* for non ACPI aware operating system like DOS and Windows NT. Set to *YES* if your OS complies with the ACPI specification (e.g. Windows 2000, XP)
System Off Mode	**G3/Mech Off** S5/Soft Off	Select the actual power down mode when the system performs a shutdown with a congatec battery system connected. *Note: This node is only visible when the system is connected to a congatec battery system.*
ACPI 2.0 Features	**No** Yes	Enable or disable extended ACPI 2.0 features.
Hide AC Device	**No** Yes	Allow to hide the ACPI AC power device. If set to *YES* e.g. The Windows XP device manager will not show a AC power device.
ACPI APIC support	**Enabled** Disabled	Set to enable to include the APIC support table to ACPI.
Suspend mode	**S1 (POS)** S3 (STR)	Select the state used for ACPI system suspend.
Repost Video on S3 Resume	**No** Yes	Determines whether to invoke VGA BIOS post on S3 resume (required by some OSes to re-initialize graphics).
USB Device Wakeup From S3/S4	**Disabled** Enabled	Enable or disable USB device wakeup from S3 and S4 state.
Active Cooling Trip Point	**Disabled** 50, 60, 70, 80, 90°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Cooling Trip Point	Disabled 50, 60, 70, 80, **90**°C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.
Critical Trip Point	Disabled, 80, 85, 90, 95, 100, **105**, 110°C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Watchdog ACPI Event	**Shutdown** Restart	Select the event that is initiated by the watchdog ACPI event. When the watchdog times out a critical but orderly OS shutdown or restart can be performed (see note below).
GPE1 Function	**No Function** Lid Switch	Determines the functionality of GPE1 (pin 42 of X4 connector).
GPE2 Function	**No Function** Sleep Button	Determines functionality of GPE2 (pin 89 of X4 connector).

Note

In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

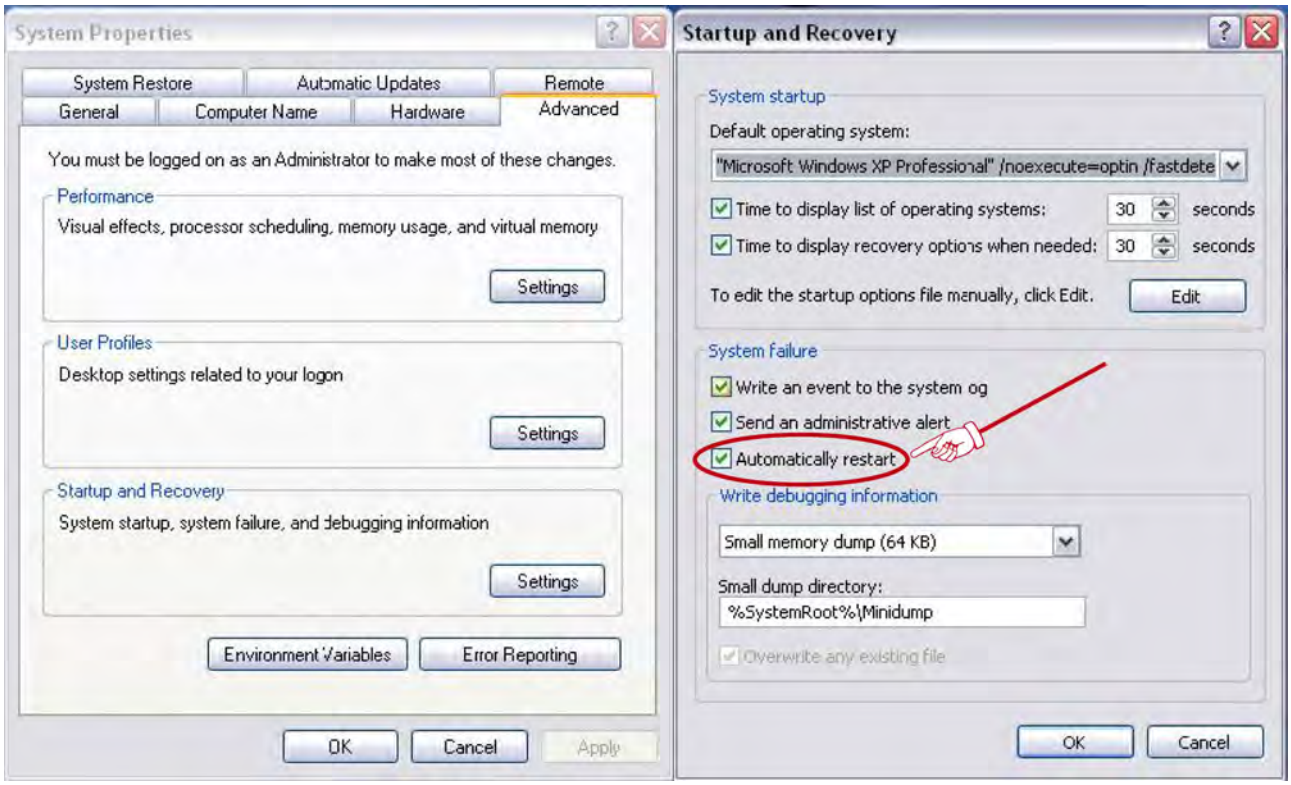
For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP/2000 there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very brief blue-screen the system will restart.

You can enable this setting buy going to the "System Properties" dialog box and choosing the "Advanced" tab. Once there choose the "Settings" button for the "Startup and Recovery" section. This will open the "Startup and Recovery" dialog box. In this dialog box under "System failure" there are three check boxes that define what Windows will do when a fatal error has been detected. In order to ensure that the system restarts after a 'Watchdog ACPI Event" that is set to 'Restart', you must make sure that the check box for the selection "Automatically restart" has been checked. If this option is not selected then Windows will remain at a blue-screen after a 'Watchdog ACPI Event" that has been configured for 'Restart' has been generated. Below is a Windows screen-shot showing the proper configuration.

Win XP/2000 Watchdog ACPI Event restart configuration



9.4.2 PCI Configuration Submenu

Feature	Options	Description
Plug & Play O/S	**No** Yes	Specifies if manual configuration is desired. Set to *NO* for operating systems that do not meet the Plug and Play specification. In this case the BIOS configures all devices in the system. Select *YES* to let the operating system configure PnP devices that are not required for booting.
PCI Latency Timer	32, **64**, 96, ... 248	This option allows you to adjust the latency timer of all devices on the PCI bus.
Allocate IRQ to PCI VGA	**Yes** No	Allow or restrict the BIOS from giving the VGA controller an IRQ resource.
Allocate IRQ to SMBUS HC	**Yes** No	Allow or restrict the BIOS from giving the SMBus controller an IRQ resource.
►PCI IRQ Resource Exclusion	sub menu	Opens PCI IRQ Resource Exclusion sub menu.
►PCI Interrupt Routing	sub menu	Opens PCI Interrupt Routing sub menu.

9.4.2.1 PCI IRQ Resource Exclusion Submenu

Feature	Options	Description
IRQ xx	**Available** Reserved	Allow or restrict the BIOS from giving IRQ resource to PCI/PNP devices. *Note: Assigned IRQ resources are shaded and listed as 'Allocated'.*

9.4.2.2 PCI Interrupt Routing Submenu

Feature	Options	Description
PIRQ xx (devices)	**Auto,** 3, 4, .., 14, 15	Select fixed IRQ for PCI interrupt line or set to AUTO to let the BIOS and operating system route an IRQ. *Note: Make sure that the selected IRQ is not assigned to legacy I/O.*
1st Exclusive PCI IRQ	**None**, [IRQs assigned manually above]	The selected IRQ will only be assigned to the PIRQ line it has been set to manually. PIRQs set to AUTO will not be assigned this IRQ.
2nd Exclusive PCI IRQ	**None**, [IRQs assigned manually above]	The selected IRQ will only be assigned to the PIRQ line it has been set to manually. PIRQs set to AUTO will not be assigned this IRQ.

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9.4.3 Graphics Configuration Submenu

Feature	Options	Description
Primary Video Device	Internal VGA **PCI /Int.VGA**	Select primary video adapter to be used during boot up.
Internal VGA Mode Select	Disabled Enabled, 1MB **Enabled, 8MB**	This option allows you to disable the internal VGA controller or enable it with 1MB or 8MB initial frame buffer size.
Aperture Size Select	**256MB** 128MB	Sets the aperture size for the internal VGA controller.
DVMT Mode Select	Fixed Mode **DVMT Mode** Combo Mode	Select the DVMT mode to be used by the DVMT graphics driver. Fixed Mode: The amount of DVMT memory selected is always allocated by the DVMT graphics driver. DVMT Mode: The DVMT driver only allocates as much memory as required for the current video mode but may allocate memory up to the limit specified in the following node. Combo Mode: The DVMT graphics driver allocates at least 64MB but may allocate up to 128MB if required. DVMT = Dynamic Video Memory Technology
DVMT/FIXED Memory	64MB **128MB**	Amount of DRAM the DVMT graphics driver can or will allocate (depends on DVMT mode selected).
Boot Display Device	**Auto** CRT only SDVO only CRT + SDVO LFP only CRT + LFP	Select the display device(s) used for boot up. LFP = Local Flat Panel (LVDS) *Note: Auto feature only works with a DDC compatible CRT monitor.*
Boot Display Preference	**LFP SDVO-B SDVO-C** LFP SDVO-C SDVO-B SDVO-B SDVO-C LFP SDVO-C SDVO-B LFP	Select order in which devices are checked and enabled as boot display devices in case a combination of LFP and SDVO devices is present.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel. Only if no external EDID data set can be found, the data set selected under 'Local Flat Panel Type' will be used as fall back data set.
Local Flat Panel Type	**Auto** VGA 1x18 (002h) VGA 1x18 (013h) SVGA 1x18 (004h) XGA 1x18 (006h) XGA 2x18 (007h) XGA 1x24 (008h) XGA 2x24 (012h) SXGA 2x24 (00Ah) SXGA 2x24 (018h) UXGA 2x24 (00Ch) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.* VGA = 640x480 SVGA = 800x600 XGA = 1024x768 SXGA = 1280x1024 UXGA = 1600x1200
SDVO Local Flat Panel Type	**Disabled** VGA 1x18 (002h) VGA 1x18 (013h) SVGA 1x18 (004h)	An SDVO local flat panel is a LVDS panel connected to an SDVO LVDS transmitter on one of the SDVO ports.

Feature	Options	Description
	XGA 1x18 (006h) XGA 2x18 (007h) XGA 1x24 (008h) XGA 2x24 (012h) SXGA 2x24 (00Ah) SXGA 2x24 (018h) UXGA 2x24 (00Ch) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	
Local Flat Panel Scaling	**Centering,** Expand Text, Expand Graphics, Expand Text & Graphics	Select whether and how to scale the actual video mode resolution to the local flat panel resolution. This also applies for SDVO local flat panels but only if Boot Display Device is set to SDVO only.
Backlight Control	**Auto**, 0%, 25%, 50%, 75%, 100%	Select local flat panel backlight control value. If set to Auto, the BIOS tries to read the backlight brightness value from the EPI data set.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Control	**No** Yes	Allow to invert backlight control values if required for the actual backlight hardware controller.
SDVO Port B Device	None **DVI** TV CRT LVDS DVI-Analog	Select the SDVO device connected to this port.
SDVO Port C Device	None **DVI** TV CRT LVDS DVI-Analog	Select the SDVO device connected to this port.
SDVO/DVI Hotplug Support	**Disabled** Enabled	If set to Enabled, the Windows XP/2000/Vista graphics drivers will support 'Hotplug' of DVI monitors connected to a DVI SDVO transmitter. This means that a DVI monitor connected while the Windows XP/2000/Vista system is already running will automatically be detected and added to the output display device list.
Display Mode Persistence	**Disabled** Enable	Display mode persistence means that previous display device configurations can be 'remembered' and restored by the system. E.g. a dual view DVI configuration will automatically be restored if both DVI monitors are connected again even if during an earlier boot only one DVI monitor had been connected and was active.

9.4.4 CPU Configuration Submenu

Feature	Options	Description
Processor Info Block	No option	Displays the processor manufacturer, brand, frequency, and cache sizes.
Execute Disable Bit	Disabled **Enabled**	Enable or disable the hardware support for data execution prevention.
Intel SpeedStep tech	Maximum Speed Minimum Speed **Automatic** Disabled	Maximum: CPU speed is set to maximum. Minimum: CPU speed is set to minimum. Automatic: CPU speed is controlled by the operating system. Disabled: No SpeedStep, default CPU speed. *Note: Feature not available for Celeron M CPUs.*
Max. CPU Frequency	(Available options depend on processor)	Allows to reduce the maximum processor frequency. This limits the maximum frequency the CPU can be set to when SpeedStep is set to Automatic or Maximum Speed. Used when the system is AC powered. *Note: Feature not available for Celeron M CPUs.*
Max. CPU Frequency (Battery)	(Available options depend on processor)	Allows to reduce the maximum processor frequency. This limits the maximum frequency the CPU can be set to when SpeedStep is set to Automatic or Maximum Speed. Used when the system is battery powered. *Note: Feature not available for Celeron M CPUs. This feature only visible when system is connected to a congatec compliant battery system.*
On Demand Clock Modulation	**Disabled** 75% 50% 25%	Allows a reduction of the performance of the processor by utilizing clock modulation. The value indicates the CLOCK ON to CLOCK OFF interval ratio. E.g. 75% results in a performance decrease of about 25%. *Note: Feature only available for Celeron M CPUs.*
C2 State Support	Disabled **Enabled**	Enable or disable C2 state for ACPI operating systems.
C3 State Support	Disabled **Enabled**	Enable or disable C3 state for ACPI operating systems.

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9.4.5 Chipset Configuration Submenu

Feature	Options	Description
DRAM Frequency	**Auto** 400MHz	Allow to manually limit the maximum DRAM frequency to 400MHz.
Memory Hole	**Disabled** 15MB-16MB	Enable or disable the memory hole between 15MB and 16MB. If enabled, accesses to this range are forwarded to the LPC / PCI bus.
IOAPIC	Disabled **Enabled**	Enable / Disable ICH6M IOAPIC function.
APIC ACPI SCI IRQ	**Disabled** Enabled	If set to Disabled IRQ9 is used for the SCI. If set to Enabled IRQ20 is used for the SCI.
C4 On C3	**Disabled** Enabled	If enabled the CPU is put to C4 state, when the ACPI OS initiates a transition to C3, for additional power saving at “Desktop Idle Mode”.
DMI Power Management	**Disabled** Enabled	Control whether the DMI link interface between Northbridge and Southbridge can go to a lower power state.
Active State Power Management	**Disabled** Enabled	Enable or disable PCI Express L0s and L1 link power states.
PCI Express Port 0	**Enabled** Disabled	
PCI Express Port 1	**Enabled** Disabled	
PCI Express Port 2	**Enabled** Disabled	
PCI Express Port 3	**Enabled** Disabled	
Reserve PCIE Hotplug Resources	**No** Yes	Reserve I/O and memory resources for empty PCI Express slots. Setting a PCI Express port to Enabled and reserving resources is required for ExpressCard hotplug support on the respective port.
I/O	None **4K** 8K 16K	Number of I/O addresses to reserve for each enabled but empty PCI Express slot.
Memory	None **1MB** 32MB 128MB	Amount of memory to reserve for each enabled but empty PCI Express slot.
Prefetchable Memory	**None** 1MB 32MB 128MB	Amount of prefetchable memory to reserve for each enabled but empty PCI Express slot.

9.4.6 I/O Interface Configuration Submenu

Feature	Options	Description
Onboard Audio Controller	Azalia **AC97** Disabled	Configure onboard audio controller for AC'97 or Azalia (Intel High Definition Audio) mode. *Note: Azalia mode requires an external Azalia codec.*
Onboard Ethernet Controller	**Enabled** Disabled	Enable / Disable the ICH6M onboard Ethernet controller.
Onboard Floppy Controller	**Disabled** Enabled	Enable / Disable the onboard floppy controller.
Floppy A	**Disabled** 360 KB 5¼" 1.2 MB 5¼" 720 KB 3 ½" 1.44 MB 3 ½" 2.88 MB 3 ½"	Select the floppy drive A type. *Note: When using the onboard floppy interface the floppy drive must be connected via a non-twisted floppy cable versus a twisted cable. The floppy drive will not function when connected via a twisted floppy cable.*
Serial Port 1/2 Configuration	Disabled **3F8/IRQ4** **2F8/IRQ3** 3E8/IRQ4 2E8/IRQ3	Specifies the I/O base address and IRQ of serial port 1/2.
Serial Port 2 Mode	**Normal** IrDA ASK IR	Specifies the mode for serial port 2.
IR Duplex Mode	Full Duplex **Half Duplex**	Select IRDA full or half duplex function.
IR I/O Pin Select	SINB/SOUTB **IRRX/RTX**	Select receiver and transmit pins for IRDA mode.
Parallel Port Address	**Disabled** 378 278 3BC	Specifies the I/O base address used by the parallel port.
Parallel Port Mode	**Normal** Bi-directional ECP EPP ECP&EPP	Specifies the parallel port mode.
EPP Version	**1.9** 1.7	Specifies the EPP version.
Parallel Port DMA	DMA0 DMA1 **DMA3**	Specifies the DMA channel for parallel port in ECP mode.
Parallel Port IRQ	IRQ5 **IRQ7**	Specifies the interrupt for the parallel port.
Serial Port 3/4 Configuration	**Disabled** 3F8/IRQ11, 2F8/IRQ10, 3E8/IRQ11, 2E8/IRQ10, 3F8/IRQ10, 2F8/IRQ11, 3E8/IRQ10, 2E8/IRQ11	Specifies the I/O base address and IRQ of serial port 3/4.

9.4.7 Clock Configuration

Feature	Options	Description
Spread Spectrum	**Disabled** Enabled	Enable spread spectrum clock modulation to reduce EMI.

9.4.8 IDE Configuration Submenu

Feature	Options	Description
ATA/IDE Configuration	Disabled **Compatible** Enhanced	Configure the integrated parallel and serial ATA controllers. Disabled: Both controllers are disabled. Compatible: Both controllers operate in legacy or compatible mode. Enhanced: Both controllers operate in enhanced or native mode.
Legacy IDE Channels	SATA Only SATA Pri, PATA Sec PATA Only	Configure the legacy channels in compatible mode.
►Primary IDE Master	sub menu	Reports type of connected IDE device.
►Primary IDE Slave	sub menu	Reports type of connected IDE device.
►Secondary IDE Master	sub menu	Reports type of connected IDE device.
►Secondary IDE Slave	sub menu	Reports type of connected IDE device.
Hard Disk Write Protect	**Disabled** Enabled	If enabled, protects the hard drive from being erased. Disabled allows the hard drive to be used normally. Read, write and erase functions can be performed to the disk.
IDE Detect Time Out (s)	0, 5, 10, ... 30, **35**	Set this option to stop the BIOS from searching for IDE devices within the specified number of seconds. Basically, this allows you to fine-tune the settings to allow for faster boot times. Adjust this setting until a suitable timing can be found that will allow for all IDE disk drives that are attached to be detected.
ATA(PI) 80Pin Cable Detection	**Host&Device** Host Device	Select the mechanism for detecting 80Pin ATA(PI) cable. *Note: The use of an 80-conductor ATA cable is mandatory for running UDMA66 and faster hard disk drives. The standard 40-conductor ATA cable cannot handle the higher speeds.*

9.4.8.1 Primary/Secondary IDE Master/Slave Submenu

Feature	Options	Description
Device	Hard Disk ATAPI CDROM	Displays the type of drive detected. The 'grayed-out' items below are the IDE disk drive parameters taken from the firmware of the IDE disk
Vendor	no option	Manufacturer of the device.
Size	no option	Total size of the device.
LBA Mode	supported not supported	Shows whether the device supports Logical Block Addressing.
Block Mode	number of sectors	Block mode boosts IDE performance by increasing the amount of data transfered. Only 512 byte of data can be transfered per interrupt if block mode is not used. Block mode allows transfers of up to 64 kB per interrupt.
PIO Mode	0, 1, 2, 3, 4	IDE PIO mode programs timing cycles between the IDE drive and the programmable IDE controller. If PIO mode increases, the cycle time decreases.
Async DMA	no option	This indicates the highest Asynchronous DMA Mode that is supported.
Ultra DMA	no option	This indicates the highest Synchronous DMA Mode that is supported.
S.M.A.R.T	no option	Self-Monitoring Analysis and Reporting Technology protocol used by IDE drives of some manufacturers to predict drive failures.
Type	Not Installed **Auto** CD/DVD ARMD	Sets the type of device that the BIOS attempts to boot from after the POST has completed. *Not Installed* prevents the BIOS from searching for an IDE disk. *Auto* allows the BIOS to auto detect the IDE disk drive type. *CD/DVD* specifies that an IDE CD/DVD drive is attached. The BIOS will not attempt to search for other types of IDE disk drives. *ARMD* specifies an ATAPI Removable Media Device. This includes, but is not limited to ZIP and LS-120.
LBA/Large Mode	Disabled **Auto**	Set to *AUTO* to let the BIOS auto detect LBA mode control. Set to Disabled to prevent the BIOS from using LBA mode.
Block (Multi-Sector Transfer)	Disabled **Auto**	Set to *AUTO* to let the BIOS auto detect device support for multi sector transfer. The data transfer to and from the device will occur multiple (the number of sectors, see above) sectors at a time. Set to Disabled to prevent the BIOS from using block mode. The data transfer to and from the device will occur one sector at a time.
PIO Mode	Auto 0, 1, 2, 3, 4	Set to *AUTO* to let the BIOS auto detect the supported PIO mode.
DMA Mode	**Auto** Disabled SWDMA, 1, 2 MWDMA0, 1, 2 UDMA0, 1, 2, 3, 4, 5, 6	Set to *AUTO* to let the BIOS auto detect the supported DMA mode. SWDMA = Single Word DMA MWDMA = Multi Word DMA UDMA = Ultra DMA
S.M.A.R.T	**Auto** Disabled Enabled	Set to *AUTO* to let the BIOS auto detect hard disk drive support. Set to *Disabled* to prevent the BIOS from using SMART feature. Set to *Enabled* to allow the BIOS to use SMART feature on supported hard disk drives.
32Bit Data Transfer	Disabled **Enabled**	Enable/Disable 32-bit data transfers on supported hard disk drives.
ARMD Emulation Type	**Auto** Floppy Hard disk drive	ARMD is a device that uses removable media, such as the LS120, MO (Magneto-optical), or Iomega Zip drives. If you want to boot from media on ARMD, it is required that you emulate boot up from a floppy or hard disk drive. This is essentially necessary when trying to boot to DOS. You can select the type of emulation used if you are booting such a device.

9.4.9 USB Configuration Submenu

Feature	Options	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports **6 USB Ports**	Disable ICH6M USB host controllers. Enable UHCI host controller 0. Enable UHCI host controller 0 + 1. Enable UHCI host controller 0 + 1 + 2.
USB 2.0 Controller	**Enabled** Disabled	Enable the ICH6M USB 2.0 (EHCI) host controller.
Legacy USB Support	Disabled **Enabled** Auto	Legacy USB Support refers to the USB keyboard, USB mouse and USB mass storage device support. If this option is *Disabled*, any attached USB device will not become available until a USB compatible operating system is booted. However, legacy support for USB keyboard will be present during POST. When this option is *Enabled*, those USB devices can control the system even when there is no USB driver loaded. *AUTO* disables legacy support if no USB devices are connected.
USB Legacy POST-Always	**Enabled** Disabled	If set to Enabled, USB legacy support is always available at least during BIOS POST regardless of the main legacy USB support setting. This ensures that the BIOS setup can always be entered and modified using a USB keyboard. Setting this node and the main node Legacy USB Support both to Disabled , completely disables BIOS legacy USB support. This decreases BIOS boot time, but also disables BIOS setup access using a USB keyboard.
USB Keyboard Legacy Support	Disabled **Enabled**	Enable/Disable USB keyboard legacy support. *NOTE: This option has to be used with caution. If the system is equipped with USB keyboard only then the user cannot enter setup to enable the option back.*
USB Mouse Legacy Support	Disabled **Enabled**	Enable/Disable USB mouse legacy support.
USB Storage Device Support	Disabled **Enabled**	Enable/Disable USB mass storage device support.
Port 64/60 Emulation	**Disabled** Enabled	Enable/Disable the “Port 6h/64h” trapping option. Port 60h/64h trapping allows the BIOS to provide full PS/2 based legacy support for USB keyboard and mouse. It provides the PS/2 functionalities like keyboard lock, password setting, scan code selection etc. to USB keyboards.
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configures the USB 2.0 host controller in HiSpeed (480Mbps) or FullSpeed (12Mbps).
BIOS EHCI Hand-Off	**Disabled** Enabled	Enable workaround for OSes without EHCI hand-off support.
USB Beep Message	Disabled **Enabled**	Enable/Disable the beep during USB device enumeration.
USB Stick Default Emulation	Auto **Hard Disk**	Select default USB stick emulation type. Auto selects floppy or hard disk emulation based on the storage size of the USB stick, but the emulation type can be manually reconfigured for each device using the Mass Storage Device Configuration sub menu.
USB Mass Storage Reset Delay	10 Sec 20 Sec 30 Sec 40 Sec	Number of seconds the legacy USB support BIOS routine waits for the USB mass storage device after the start unit command.
►USB Mass Storage Device Configuration	sub menu	Opens sub menu.

9.4.9.1 USB Mass Storage Device Configuration Submenu

Feature	Options	Description
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	Every USB MSD that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. *Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.* Select *AUTO* to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. *Forced FDD* allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. *Hard Disk* allows the device to be emulated as hard disk. *CDROM* assumes the CD.ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

9.4.10 Keyboard/Mouse Configuration Submenu

Feature	Options	Description
Bootup Num-Lock	Off **On**	Specifies the power-on state of the Num-lock feature on the numeric keypad of the keyboard.
Typematic Rate	Slow **Fast**	Specifies the rate at which the computer repeats a key that is held down. *Slow* sets a rate of under 8 times per second. *Fast* sets a rate of over 20 times per second.
PS/2 Mouse Support	Disabled Enabled **Auto**	*Disabled* will prevent the PS/2 mouse port from using system resources and will prevent the port from being active. *Enabled* activates the PS/2 port and the BIOS offers PS/2 mouse support. Use this setting if you always need PS/2 mouse support even when the mouse is not connected at boot-up time. *Auto* lets the BIOS check for a connected PS/2 mouse and enable support if one is connected.

9.4.11 Remote Access Configuration Submenu

Feature	Options	Description
Remote Access	**Disabled** Enabled	Enable/Disable the BIOS remote access feature. *Note: If the systems serial ports are disabled in the 'I/O Interface Configuration' submenu, then Serial Redirection is disabled and 'Remote Access Configuration' menu is unavailable to the users.*
Serial Port Number	**COM1** COM2	Select the serial port you want to use for console redirection. *Note: Only enabled serial ports are presented as an option.*
Serial Port Mode	**115200 8,n,1** 57600 8,n,1 19200 8,n,1	Select the baud rate (transmitted bits per second) you want the serial port to use for console redirection. Note: The terminal program used with Serial Redirection must be set to use exact the same set of communication parameters.
Flow Control	**None** Hardware Software	Select the flow control for Serial Redirection.
Redirection After BIOS POST	Disabled Boot Loader **Always**	With *Disabled* Serial Redirection functionality is disabled at the end of BIOS POST. If set to *Always*, all resources and interrupts associated with Serial Redirection are protected and not released to DOS. This option lets Serial Redirection permanently reside at base memory which allows the DOS console to be redirected. *Note, that graphics output (VGA, SVGA, etc) from DOS programs is not redirected!* If set to *Boot loader*, Serial Redirection is active during the OS boot loader process. This allows boot status messages to be redirected, but Serial Redirection will terminate when the OS loads.
Terminal Type	**ANSI** VT100 VT-UTF8	Select the target terminal type. Escape sequences representing keystrokes are sent to the remote terminal based on these settings.
VT-UTF8 Combination Key Support	**Disabled** Enabled	This option enables VT-UFT8 combination key support for ANSI/ VT100 terminals.
Sredir Memory Display Delay	No Delay **Delay 1 Sec** Delay 2 Sec Delay 4 Sec	Set the delay in seconds to display memory information if serial redirection is enabled.
Serial Port BIOS Update	**Disabled** Enabled	Enable or disable the serial port BIOS update feature. Disabling saves boot time.

9.4.12 Hardware Monitoring Submenu

Feature	Options	Description
H/W Health Function	Disabled **Enabled**	Enable hardware health monitoring device and display the readings.
Board Temperature	no option	Current board temperature.
CPU Temperature	no option	Current processor die temperature.
Fan1 Speed	no option	Current FAN speed.
VcoreA	no option	Current Core A reading.
VcoreB	no option	Current Core B reading.
+3.3Vin	no option	Current 3.3V reading.
+5Vin	no option	Current 5V reading.
+5VSB	no option	Current 5V standby reading.
VRTC	no option	Current VRTC reading.

9.4.13 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset..
Stop Watchdog For User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One time trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to '*One time trigger'* the watchdog will be disabled after the first trigger. If set to *'Single event'*, every stage will be executed only once, then the watchdog will be disabled. If set to *'Repeated event'* the last stage will be executed repeatedly until a reset occurs.
Delay	see Post Watchdog	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	**NMI** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about *ACPI Event* see section 9.4.1 of this user's guide.
Event 2	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	0.5sec 1sec 2sec 5sec **10sec** 30sec 1min 2min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.

9.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.
In the upper part of the screen the Boot setup allows you to prioritize the available boot devices. The lower part of this setup screen shows options related to the BIOS boot.

9.5.1 Boot Device Priority

Feature	Options	Description
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The “Device Based” boot priority list allows you to select from a list of currently detected devices only. The “Type Based” boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the “Device Based” boot priority list might change dynamically in cases when devices are physically removed or added to the system. The “Type Based” boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if device based priority list control is selected. If “Type Based” priority list control is enabled only 8 boot devices can be prioritized.)	Disabled Primary Master Primary Slave Secondary Master Secondary Slave Legacy Floppy USB Harddisk USB CDROM USB Removable Dev. Onboard LAN External LAN PCI Mass Storage PCI SCSI Card Any PCI BEV Device Third Master Third Slave Local BEV ROM	This view is only available when in the default “Type Based” mode. When in “Device Based” mode you will only see the devices that are currently connected to the system. The default boot priority is *Removables 1st, ATAPI CDROM 2nd, Hard Disk 3rd, BEV 4th* (BEV = Boot Entry Vector, e.g. Network or SCSI Option-ROMs).

9.5.2 Boot Settings Configuration

Feature	Options	Description
Quick Boot	Disabled **Enabled**	If *Enabled*, some POST tasks will be skipped to speed-up the BIOS boot process.
Quiet Boot	**Disabled** Enabled	*Disabled* displays normal POST diagnostic messages. *Enabled* displays OEM logo instead of POST messages. *Note: The default OEM logo is a dark screen.*
Boot Display	**Clear** Maintain	Controls the end of POST boot display handling, if Quiet Boot is enabled. If set to *Maintain* the BIOS will maintain the current display contents and graphics video mode used for POST display. If set to *Clear* the BIOS will clear the screen and switch to VGA text mode at end of POST. *Note: This option is only available if Quiet Boot is set to Enabled.*
Automatic Boot List Retry	**Disabled** Enabled	Automatically retry boot list if end of list is reached and no boot device found.
AddOn ROM Display Mode	**Force BIOS** Keep current	Set display mode for Option ROM.
Halt On Error	**Disabled** Enabled	Determines whether the BIOS halts and displays an error message if an error occurs. If set to *Enabled* the BIOS waits for user input.
Hit 'DEL' Message Display	Disabled **Enabled**	Allows/Prevents the BIOS to display the '*Hit Del to enter Setup'* message.
Interrupt 19 Capture	**Disabled** Enabled	Allows/Prevents the option ROMs (such as network controllers) from trapping the boot strap interrupt 19.
PXE Boot to LAN	**Disabled** Enabled	Disable/Enable PXE boot to LAN *Note: When set to 'Enabled', the system has to be rebooted in order for the Intel Boot Agent device to be available in the Boot Device Menu.*
Power Loss Control (see note below)	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. *Remain Off* keeps the power off until the power button is pressed. *Turn On* restores power to the computer. *Last State* restores the previous power state before power loss occurred. *Note: Only works with an ATX type power supply.*

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

3. *Unlike other module designs available in the embedded market, a CMOS battery is not required by congatec modules to support the 'Power Loss Control' feature.*

9.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

9.6.1 Security Settings

Feature	Options	Description
Supervisor Password	Installed Not Installed	Reports if there is a supervisor password set.
User Password	Installed Not Installed	Reports if there is a user password set.
Change Supervisor Password	enter password	Specifies the supervisor password.
User Access Level	No Access View Only Limited **Full Access**	Sets BIOS setup utility access rights for user level.
Boot Selection Popup Menu Access	**Anybody** Setup User Setup Supervisor No Access	Select who can access the boot selection popup menu, when setup passwords are installed.
Change User Password	enter password	Specifies the user password.
Password Check	**Setup** Always	Setup: Check password while invoking setup. Always: Check password also on each boot.
Boot Sector Virus Protection	**Disabled** Enabled	Select *Enabled* to enable boot sector protection. The BIOS displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. If enabled, the following appears when a write is attempted to the boot sector. You may have to type N several times to prevent the boot sector write. *Boot Sector Write!* *Possible VIRUS: Continue (Y/N)?* The following appears after any attempt to format any cylinder, head or sector of any hard disk drive via the BIOS INT13 hard disk drive service: *Format!!!* *Possible VIRUS: Continue (Y/N)?*
HDD Security Freeze Lock	Disabled **Enabled**	If enabled, the BIOS will send the Security Freeze Lock command to each attached hard disk supporting the security command set. This will prevent anybody from setting or changing a hard disk password after POST.
Ask HDD Password on Every Boot	**No** Yes	Select whether the hard disk unlock password has to be entered on each boot. Only applicable if a hard disk user password is installed (see Hard Disk Security).
BIOS Update & Write Protection	**Disabled** Enabled	Only visible if a supervisor password is installed. If enabled the BIOS update and modification utilities will ask for the supervisor password before allowing any write accesses to the BIOS flash part.
END-Key Loads CMOS Defaults	**Yes** No	If set to Yes, the user can force the loading of CMOS defaults by pressing the END key during POST.

9.6.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

9.6.2.1 Hard Disk Security User Password

Feature	Options	Description
Primary/Secondary Master/Slave HDD User Password	enter password	Set or clear the user password for the hard disk. *Note: This option will be shaded if the hard drive does support the Security Mode Feature set but user failed to unlock the drive during BIOS POST.*

9.6.2.2 Hard Disk Security Master Password

Feature	Options	Description
Primary/Secondary Master/Slave HDD Master Password	enter password	Set or clear the master password for the hard disk. *Note: This option will be shaded if the hard drive does support the Security Mode Feature set but user failed to unlock the drive during BIOS POST.*

9.7 Power Setup

Select the Power tab from the setup menu to enter the Power Management setup screen.

Feature	Options	Description
Power Management / APM	Disabled **Enabled**	Set this option to allow or prevent chipset power management and APM (Advanced Power Management).
Suspend Timeout	**Disabled** 1- 60 Min	Specifies the length of time of inactivity the system waits before it enters suspend mode.
Video Power Down Mode	Disabled Standby **Suspend**	Specifies the power state that the video subsystem enters when the BIOS places it in a power saving state after the specified period of display inactivity has expired.
Hard Disk Power Down Mode	Disabled Standby **Suspend**	Specifies the power state that the hard disk drives enter after the specified period of hard drive inactivity has expired.
<Device>	Ignore **Monitor**	Determines whether the device activity is monitored by the power management timer or not.
Resume On Ring	**Disabled** Enabled	Disable / enable RI signal (= GPE2 on pin 89 of X4 connector) to generate a wake event. If enabled wake is possible from all power down states including S5 (Soft Off).
Resume On PME	**Disabled** Enabled	Disable / enable PCI PME to generate a wake event. If enabled wake is possible from all power down states including S5 (Soft Off).
Resume On RTC Alarm	**Disabled** Enabled	Disable / enable RTC to generate a wake event. If enabled wake is possible from all power down states including S5 (Soft Off).
RTC Alarm Date (Days)	**Everyday**, 01....31	Select the day of the month when the event should be generated.
System Time	Hour:Minute:Second	Select the system time when the event should be generated.
Power Button Mode	**On/Off** Suspend	Specifies if the system enters suspend or soft off mode when the power button is pressed.

9.7.1 Exit Menu

Select the Exit tab from the setup menu to enter the Exit setup screen.

You can display an Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup and reboot so the new system configuration parameters can take effect.
Discard Changes and Exit	Exit setup without saving any changes made in the BIOS setup program.
Discard Changes	Discard changes without exiting setup. The option values presented when the computer was turned on are used.
Load CMOS Defaults	Load the CMOS defaults of all the setup options.

10 Additional BIOS Features

The conga-X915 uses a congatec/AMIBIOS that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as P915R1xx, where P915 is the congatec internal project name, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

10.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

10.2 BIOS Recovery

The “BIOS recovery” scenario is recommended for situations when the normal flash update fails and the user can no longer boot back to an OS to restore the system. The code that handles BIOS recovery resides in a section of the flash referred to as “boot block”.

For more information about “BIOS Recovery” refer to application note AN6_BIOS_Recovery.pdf, which can be found on the congatec AG website at www.congatec.com.

10.2.1 BIOS Recovery via Storage Devices

In order to make a BIOS recovery from a floppy disk, CD-ROM (ISO9660) or USB floppy the BIOS file must be copied into the root directory of the storage device and renamed *AMIBOOT.ROM*.

For more information about “BIOS Recovery via Storage Devices” refer to application note AN6_BIOS_Recovery.pdf, which can be found on the congatec AG website at www.congatec.com.

10.2.2 BIOS Recovery via Serial Port

The Serial Flash method allows for boot block recovery by loading a BIOS image via a serial port (COM1). This is can be used by many headless embedded systems which rely on a serial port as a debug and utility console port. This feature is disabled by default. See setup node in the “BIOS Setup Program” section 9.4.11 “Remote Access Configuration Submenu”.

For more information about “BIOS Recovery via Serial Port” refer to application note AN6_BIOS_Recovery.pdf, which can be found on the congatec AG website at www.congatec.com.

10.3 Serial Port and Console Redirection

Serial Redirection allows video and keyboard redirection via a standard RS-232 serial port.

For more information about “Serial Port and Console Redirection” refer to application note AN2_Remote_Control.pdf, which can be found on the congatec AG website at www.congatec.com.

10.4 BIOS Security Features

The BIOS provides both a supervisor and user password. If you use both passwords, the supervisor password must be set first. The system can be configured so that all users must enter a password every time the system boots or when setup is executed.

The two passwords activate two different levels of security. If you select password support you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed.

The supervisor password (supervisor mode) gives unrestricted access to view and change all the setup options. The user password (user mode) gives restricted access to view and change setup options.

If only the supervisor password is set, pressing <Enter> at the password prompt of the BIOS setup program allows the user restricted access to setup.

Setting the password check to 'Always' restricts who can boot the system. The password prompt will be displayed before the system attempts to load the operating system. If only the supervisor password is set, pressing <Enter> at the password prompt allows the user to boot the system.

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10.5 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to 'lock' and 'unlock' drives using the security password. A 'locked' drive will be detected by the system, but no data can be accessed. Accessing data on a 'locked' drive requires the proper password to 'unlock' the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within five attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

11 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Audio Codec '97 Component Specification, Version 2.3 (AC '97)	http://www.intel.com/design/chipsets/audio/
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.2	http://www.pcisig.com/specifications
PCI Express Base Specification, Revision 1.0a	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003	http://www.acpi.info
Information Technology AT Attachment with Packet Interface -5 (ATA/ATAPI-5) Revision 3, February 29, 2000	http://www.t13.org

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