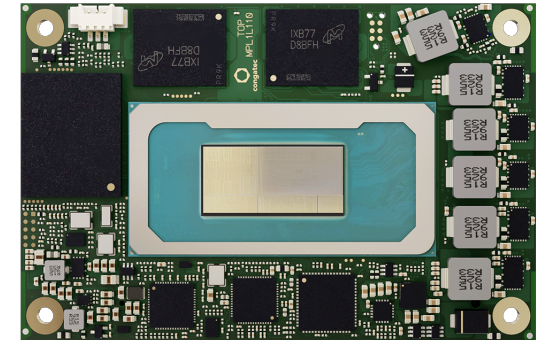




conga-MC1000

COM Express® 3.1 Type 10 Mini Module with Intel® Core Ultra Processors Series 3

User's Guide

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.01	2026-10-15	RVI	Preliminary release

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-MC1000. It is one of three documents that should be referred to when designing a COM Express® application. The other reference documents that should be used include the following:

COM Express® Design Guide
COM Express® Specification

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Terminology

Term	Description
CSA	Active Cooling Solution
CSP	Passive Cooling Solution
DSC	Display Stream Compression
DTR	Dynamic Temperature Range
eDP	Embedded DisplayPort
EU	Execution Unit
DDI	Digital Display Interface
GB	Gigabyte
GbE	Gigabit Ethernet
GHz	Gigahertz
HDA	High Definition Audio
HBR	High Bit Rate
HSP	Heatspreader
kB	Kilobyte
kHz	Kilohertz
LVDS	Low-Voltage Differential Signaling
MB	Megabyte
Mbit	Megabit
MHz	Megahertz
N.A.	Not available
N.C.	Not connected
NVMe	Non-Volatile Memory Express
OEM	Original Equipment Manufacturer
PCIe	PCI Express
PCH	Platform Controller Hub
PEG	PCI Express Graphics
SATA	Serial ATA
SoC	System On Chip
SSD	Solid-state Drive
TBD	To be determined
TBA	To be announced
TCC	Time Coordinated Computing
TDP	Thermal Design Power
TSN	Time Sensitive Networking
UHBR	Ultra High Bit Rate

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1 Introduction

1.1 COM Express® Concept

COM Express® is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express® modules are available in following form factors:

- Mini 84 mm x 55 mm
- Compact 95 mm x 95 mm
- Basic 125 mm x 95 mm
- Extended 155 mm x 110 mm

Table 1 COM Express® 3.1 Pinout Types

Types	Connector Rows	PCIe Lanes	PEG	SATA Ports	LAN ports	USB 2.0/ SuperSpeed USB	USB4	Display Interfaces
Type 6	A-B C-D	Up to 24	1	Up to 4	1 x NBASE-T	Up to 8 / 4 ¹	2	VGA, LVDS/eDP, PEG, 3x DDI
Type 7	A-B C-D	Up to 32	-	Up to 2	1x NBASE-T, 4x 10GBASE-KR	Up to 4 / 4 ¹	-	
Type 10	A-B	Up to 4	-	Up to 2	1x NBASE-T	Up to 8 / 2 ¹	-	LVDS/eDP, 1x DDI

¹ The SuperSpeed USB ports (USB 3.0) are not in addition to the USB 2.0 ports. Up to 4 of the USB 2.0 ports can support SuperSpeed USB.

The conga-MC1000 modules use the Type 10 pinout definition and comply with COM Express® 3.1 specification. They are equipped with single 220-pin high performance connectors that ensure stable data throughput.

The COM integrates all the core components and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

Most importantly, COM Express® modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

1.2 Options Information

The conga-MC1000 is available in eight variants (four commercial and four industrial). The tables below show the different configurations available.

Table 2 Commercial Variants

Part-No.			049903	049905	049906	049907
Processor			Intel® Core™ Ultra 7 356H, 16 Cores	Intel® Core™ Ultra 5 3336H, 12 cores	Intel® Core™ Ultra 5 325, 8 cores	Intel® Core™ Ultra X7 358H, 16 Cores
Total Core	P-Cores		4 Cores	4 Cores	4 Cores	4 Cores
	E-Cores	Normal	8 Cores	4 Cores	-	8 Cores
		Low Power	4 Cores	4 Cores	4 Cores	4 Cores
No of Threads			16	12	8	16
Core Base Frequency	P-Cores		1.9 GHz	1.9 GHz	2.1 GHz	1.9 GHz
	E-Cores	Normal	1.5 GHz	1.5 GHz	1.6 GHz	1.5 GHz
		Low Power	1.5 GHz	1.5 GHz	1.6 GHz	1.5 GHz
Intel® Smart Cache			18 MB	18 MB	12 MB	18 MB
Assured Power (cTDP)	Processor Base Power		25 W	25 W	25 W	25 W
	Min. Assured Power		15 W	15 W	12 W	15 W
	Max. Assured Power		80 W	65 W	55 W	80 W
Maximum Turbo Freq.	P-Cores		4.7GHz	4.6GHz	4.5GHz	4.8GHz
	E-Cores	Normal	3.5 GHz	3.4 GHz	-	3.5 GHz
		Low Power	3.3 GHz	3.2 GHz	3.4 GHz	3.3 GHz
Processor Graphics			Intel® Graphics (4 Xe Cores)	Intel® Graphics (4 Xe Cores)	Intel® Graphics (4 Xe Cores)	Intel® Arc™ B390 GPU (12 Xe Cores)
GFX Max. Dynamic Freq.			2.45 GHz	2.3 GHz	2.45 GHz	2.5 GHz
PCIe Lanes	Max.		20	20	12	12
	NVMe Gen 4 (Assembly Option)		1 x4 NVMe (Assembly option)	1 x4 NVMe (Assembly option)	1 x4 NVMe (Assembly option)	1 x4 NVMe (Assembly option)
Ethernet Controller			Intel® I226-LM	Intel® I226-LM	Intel® I226-LM	Intel® I226-LM
CPU Use Condition ¹			Mobile	Mobile	Mobile	Mobile
CPU Max. Operating Temperature			100°C	100°C	100°C	100°C
Compatible Carrier Board			conga-Eval Carrier3 T10 evaluation carrier board for COM Express® Type 10 modules			

Table 3 Industrial Variants

Part-No.			049910 ²	049911 ²	049912 ²	049913 ²
Processor			Intel® Core™ Ultra 7 366HRE, 16 Cores	Intel® Core™ Ultra 7 365RE, 8 cores	Intel® Core™ Ultra 5 336HRE, 12 Cores	Intel® Core™ Ultra 5 335RE, 8 Cores
Total Core	P-Cores		TBD	TBD	TBD	TBD
	E-Cores	Normal	TBD	TBD	TBD	TBD
		Low Power	TBD	TBD	TBD	TBD
No of Threads			TBD	TBD	TBD	TBD
Core Base Frequency	P-Cores		TBD	TBD	TBD	TBD
	E-Cores	Normal	TBD	TBD	TBD	TBD
		Low Power	TBD	TBD	TBD	TBD
Intel® Smart Cache			TBD	TBD	TBD	TBD
Assured Power (cTDP)	Processor Base Power		TBD	TBD	TBD	TBD
	Min. Assured Power		TBD	TBD	TBD	TBD
	Max. Assured Power		TBD	TBD	TBD	TBD
Maximum Turbo Freq. ³	P-Cores		TBD	TBD	TBD	TBD
	E-Cores	Normal	TBD	TBD	TBD	TBD
		Low Power	TBD	TBD	TBD	TBD
Processor Graphics			TBD	TBD	TBD	TBD
GFX Max. Dynamic Freq.			TBD	TBD	TBD	TBD
PCIe Lanes	Max.		TBD	TBD	TBD	TBD
	NVMe Gen 4 (Assembly Option)		1 x4 NVMe (Assembly option)	1 x4 NVMe (Assembly option)	1 x4 NVMe (Assembly option)	1 x4 NVMe (Assembly option)
Ethernet Controller			Intel® I226-IT	Intel® I226-IT	Intel® I226-IT	Intel® I226-IT
CPU Use Condition ¹			TBD	TBD	TBD	TBD
CPU Max. Operating Temperature			TBD	TBD	TBD	TBD
Compatible Carrier Board			conga-Eval Carrier3 T10 evaluation carrier board for COM Express® Type 10 modules			

**Note**

- ¹. Intel SoC use conditions. For more information, see Intel documentation.
- ². Intel has not yet publicly released the information that are marked as TBD below.
- ³. Disable Turbo mode for industrial use conditions.

2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	COM Express® Mini; Type 10	
Processor	Intel® Core™ Ultra Series 3 Panther Lake-H series	
DRAM	Up to 32GB LPDDR5x soldered down with up to 9600MT/s ; In-band ECC (only on selected product variants)	
Mass Storage	Optional NVMe up to 1 TB capacity SSD	
Graphics	Intel® Arc Graphics with up to 12 Xe cores or Intel® Graphics with up to 4 Xe cores ; Intel® Xe Matrix Extensions	
AI Acceleration	Integrated NPU accelerator up to 50 TOPS ; Up to 180 TOPS platform total	
Display	DDI for DP++ ; single-channel LVDS or optional eDP ; 2x independent displays up to 4k	
Ethernet	2.5 GbE via Intel® i226 Ethernet controller series ; supporting TSN (only on selected product variants)	
Audio	Integrated High Definition Audio (HDA) interface ; Soundwire (optional)	
I/O Interfaces	Up to 4x PCIe Gen4 2x USB 3.2 Gen2 8x USB 2.0 2x SATA 2x UART (RX/TX only)	GPIOs GP SPI LPC SM Bus I²C
Module Management Controller	Module Management Controller Multi Stage Watchdog Non volatile User Data Storage Board Information Board Statistics	I²C bus (fast mode) Power Loss Control Hardware Health Monitoring POST Code Redirection
Security	(Default): Intel PTT 2.0 (Optional): External Trusted Platform Module (TPM 2.0) can be used instead of external Boot SPI	
Embedded BIOS Feature	AMI Aptio® UEFI firmware ; OEM Logo ; OEM CMOS default settings ; LCD Control ; Display Auto Detection ; Backlight Control ; Flash Update	
Power Management	ACPI 6.0 ; wide range power supply 4.75V – 20V ; single supply power	
Operating Systems	Microsoft® Windows® 11 IoT Enterprise ; Microsoft® Windows® 11 ; Linux	
Temperature	Commercial Temp.: Operating 0 °C to 60 °C	Commercial Temp.: Storage -20 °C to 80 °C
Humidity	Operating : 10% to 85% r. H. non cond.	Storage : 5% to 85% r. H. non cond.
Size	84 x 55 mm	

2.2 Supported Operating Systems

The conga-MC1000 supports the following operating systems:

- Microsoft® Windows® 11, Version 25H2
- Microsoft® Windows® 11 IoT Enterprise, Version 25H2
- Yocto 6.0

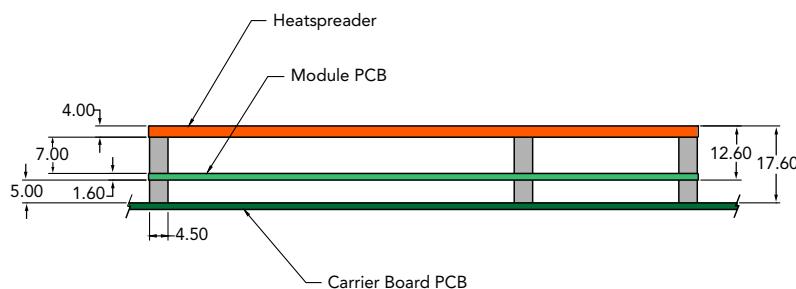


Note

1. The processor supports only 64-bit operating systems.
2. The conga-MC1000 supports only native UEFI Operating Systems. Legacy Operating Systems which require CSM (Compatibility Support Module) as part of the UEFI firmware are not supported anymore.
3. To support Intel® i226 Ethernet controller in Linux by default, you need kernel 5.15 or higher

2.3 Mechanical Dimensions

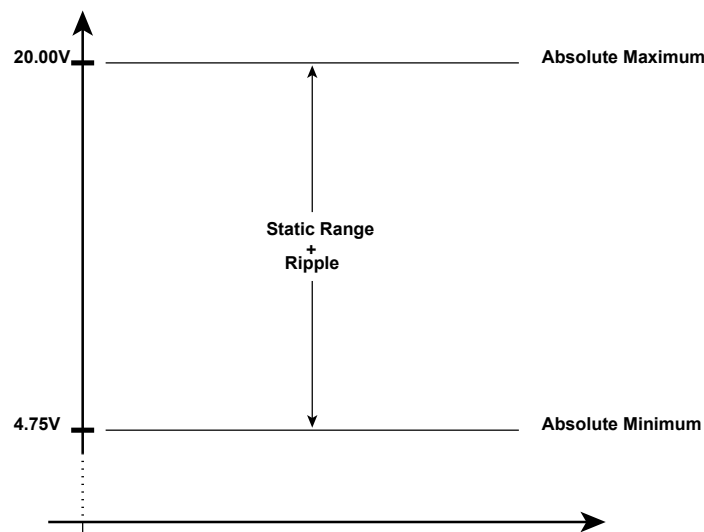
- 84.0mm x 55.0mm
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm.



3D models of congatec products are available at www.congatec.com/login. These models indicate the overall length, height and width of each product. If you need login access, contact your local sales representative.

2.4 Supply Voltage Standard Power

- 4.75V - 20V (Wide input range)



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 10 (single connector, 220 pins).

Table 5 Power Limits on Type 10 Connector

Power Rail	Module Pin Current Capability (A)	Nominal Input (V)	Input Range (V)	Derated Input (V)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (W)	Assumed Conversion Efficiency	Max. Load Power (W)
VCC_12V	6	12	11.4 - 12.6	11.4	+/- 100	68	85%	58
Wide Input	6		4.75-20.0	4.75	+/- 100	28		
VCC_5V_SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values for conga-MC1000 have not been determined at the time of this document's release and will be provided with the final release of this user guide.

The power consumption values are measured with the following setup:

- Input voltage 12 V
- conga-MC1000 COM
- COM Express® Eval Carrier Type 10 Gen 3
- conga-MC1000 cooling solution
- Microsoft Windows 11 (64 bit)



Note

The CPU was stressed to its maximum workload with the Intel® Power and Thermal Analysis Tool.

The power consumption values are recorded during the following system states:

Table 6 Measurement Description

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	COM is powered by VCC_5V_SBY	
S5	COM is powered by VCC_5V_SBY	
S5e	COM is powered by VCC_5V_SBY	



Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement*

The tables below provide additional information about the conga-MC1000 power consumption. The values are recorded at various operating modes.

Table 7 Power Consumption Values

Part-No.	Memory Size	H.W Rev.	BIOS Rev.	CPU		Current (A) @ 12V (S0) or 5V (S3, S5, S5e)					
				Variant	Cores	S0: Min	S0: Max	S0: Peak	S3	S5	S5e
049903	16 GB	A.3	TBD	Intel® Core™ Ultra 7 356H	16	TBD	TBD	TBD	TBD	TBD	TBD
049905	16 GB	A.3	TBD	Intel® Core™ Ultra 5 336H	12	TBD	TBD	TBD	TBD	TBD	TBD
049906	16 GB	A.3	TBD	Intel® Core™ Ultra 5 325	8	TBD	TBD	TBD	TBD	TBD	TBD
049907	16 GB	A.3	TBD	Intel® Core™ Ultra X7 358H	16	TBD	TBD	TBD	TBD	TBD	TBD
049910	32 GB	A.3	TBD	Intel® Core™ Ultra 7 366H	16	TBD	TBD	TBD	TBD	TBD	TBD
049911	16 GB	A.3	TBD	Intel® Core™ Ultra 7 365RE	8	TBD	TBD	TBD	TBD	TBD	TBD
049912	16 GB	A.3	TBD	Intel® Core™ Ultra 5 336HRE	12	TBD	TBD	TBD	TBD	TBD	TBD
049913	16 GB	A.3	TBD	Intel® Core™ Ultra 5 335RE	8	TBD	TBD	TBD	TBD	TBD	TBD



Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 8 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	TBD
20°C	3V DC	TBD
70°C	3V DC	TBD



Note

1. Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.
2. Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).

-
3. Consider also the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to [https://wiki.congatec.com/wiki/RTC_Battery_Lifetime_\(AN09\)](https://wiki.congatec.com/wiki/RTC_Battery_Lifetime_(AN09)).
 4. We recommend to always have a CMOS battery present when operating the conga-MC1000.

2.7 Environmental Specifications

Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to +80°C
Temperature (Industrial variants)	Operation: -40° to 85°C	Storage: -40° to 85°C
Relative Humidity	Operation: 10% to 85%	Storage: 5% to 85%



Caution

The product is designed to operate in the above operating temperature range. It is the system integrator's responsibility to ensure that all components used on or with the product are operated within their individually specified temperature limits. For detailed information regarding the temperature specifications of individual components used on the product, refer to the respective thermal documentation (e.g., Hotspots CTNs) available in the customer login area at www.congatec.com and/or the customer knowledge base wiki.congatec.com. Appropriate cooling measures must be implemented in the final application to ensure proper heat dissipation.

Humidity specifications are for non-condensing conditions.

2.8 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

2.8.1 Module

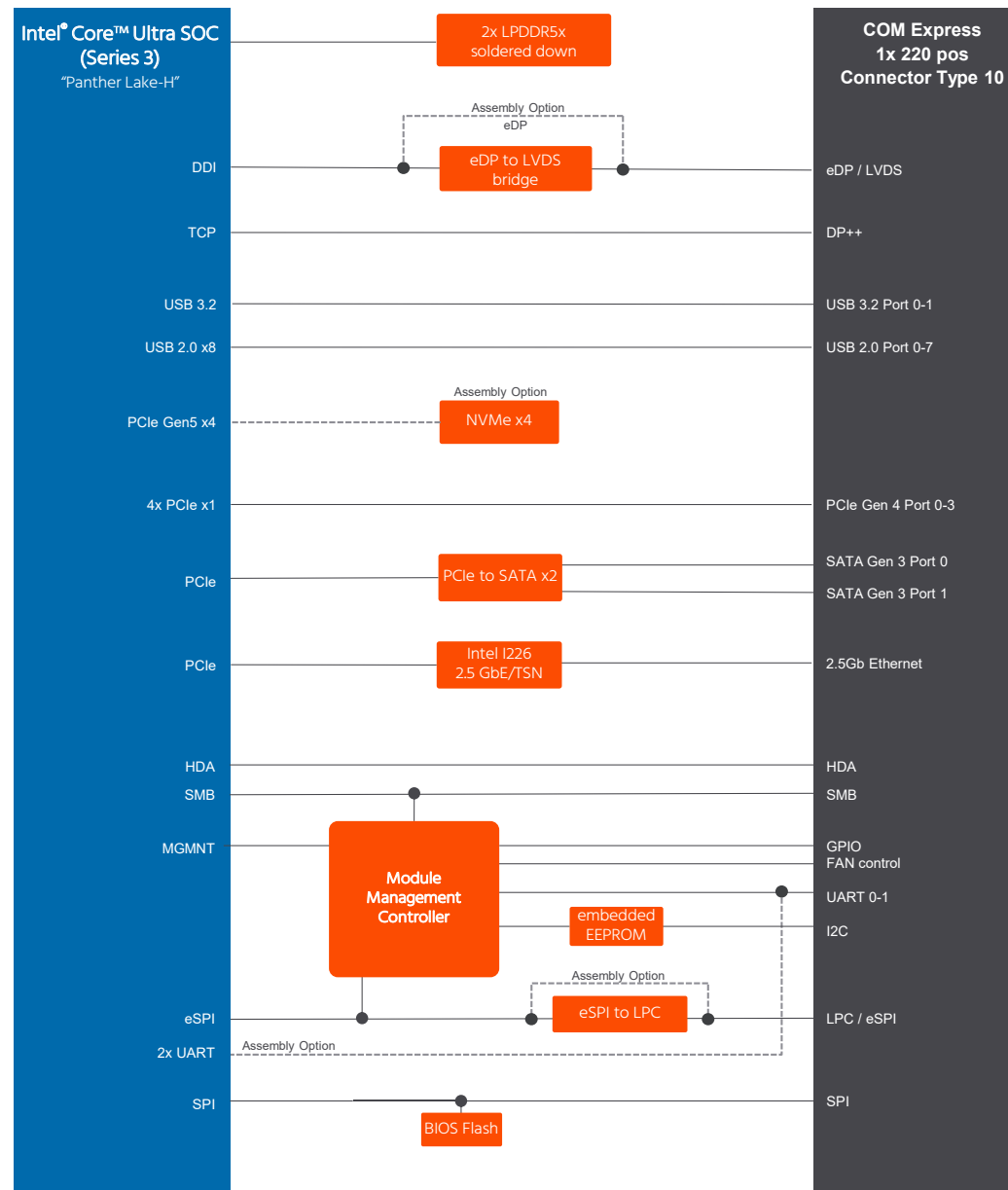
For long-term storage of the conga-MC1000 (more than six months), keep the conga-MC1000 in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.



Note

We do not recommend storing the conga-MC1000 for more than five years under these conditions.

3 Block Diagram



 Assembly Option

4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-MC1000 variants. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

Cooling Solution	Part-No.	Description
HSP	049954	Standard heatspreader for high performance COM Express module conga-MC1000 with H484. All standoffs are with 2.7mm bore hole.
	049955	Standard heatspreader for high performance COM Express module conga-MC1000 with H484. All standoffs are M2.5mm threaded.
	049956	Standard heatspreader for high performance COM Express module conga-MC1000 with H404. All standoffs are with 2.7mm bore hole.
	049957	Standard heatspreader for high performance COM Express module conga-MC1000 with H404. All standoffs are M2.5mm threaded.
CSP	810629	COM Express® Mini Universal Passive Cooler for Heatspreader Mounting
CSA	810630	COM Express® Mini Universal Active Cooler for Heatspreader Mounting



Caution

1. The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.
2. For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.
3. For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.
4. Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.

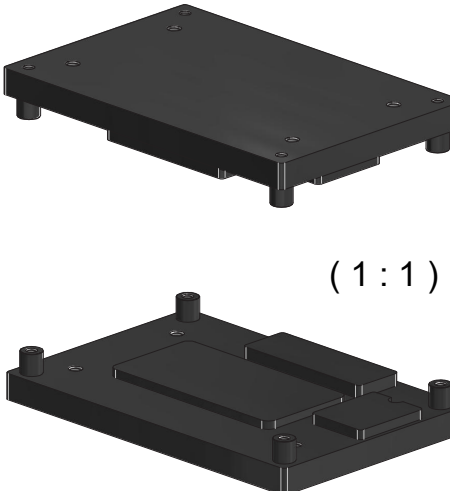
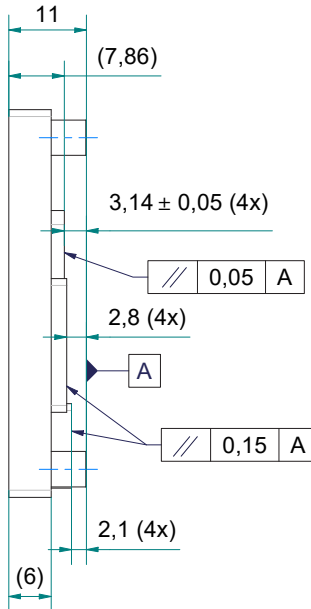
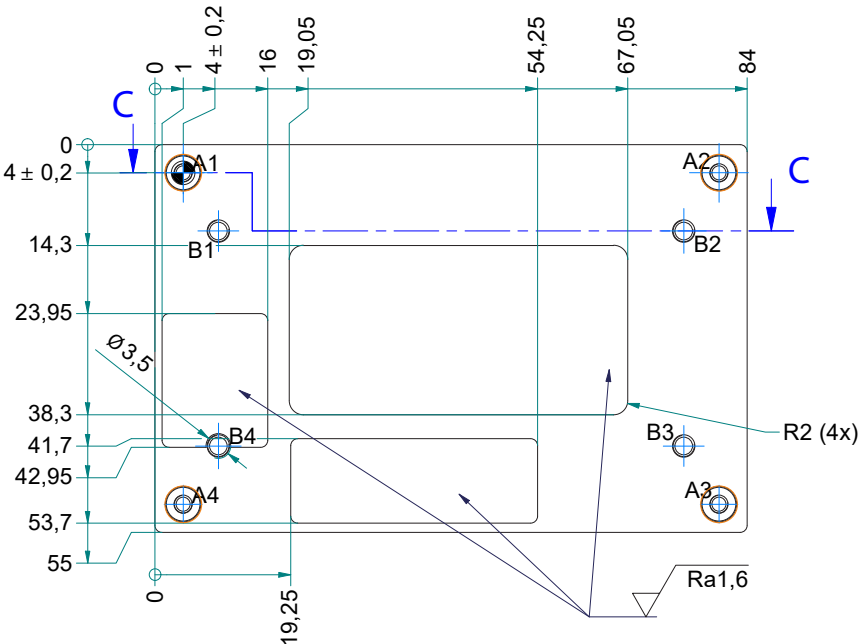


Note

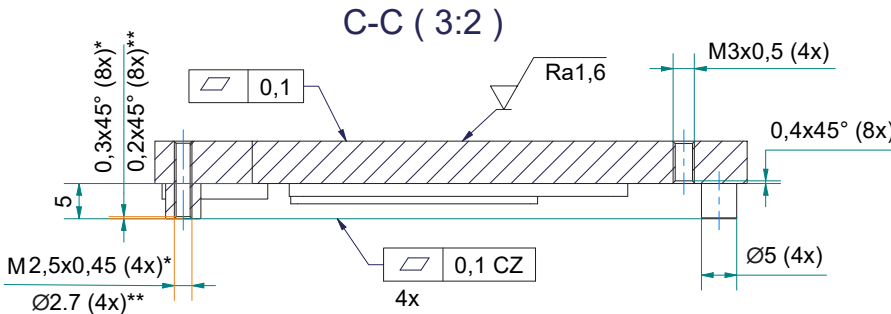
1. We recommend a maximum torque of 0.4 Nm for carrier board mounting screws.
2. The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.
3. For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.

4.1

H484 Variants (Part-No.: 049954, 049955)

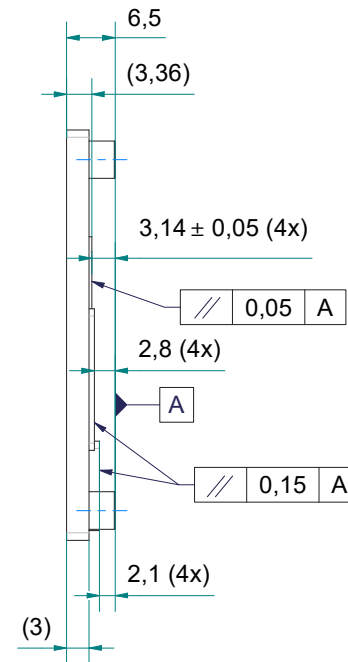
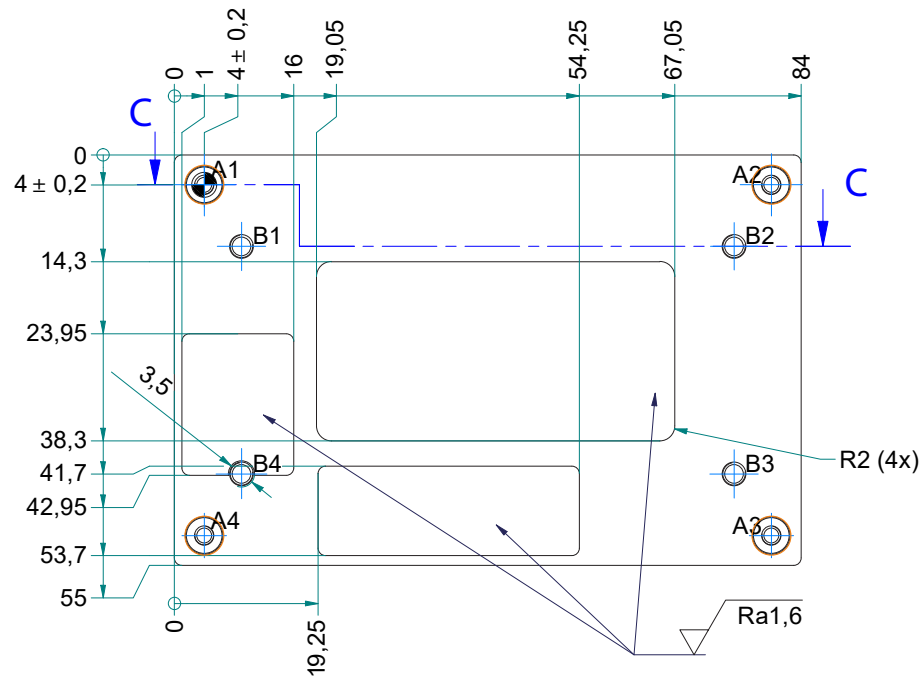


All dimensions are in [mm]
All non-dimensioned radii are R=1mm

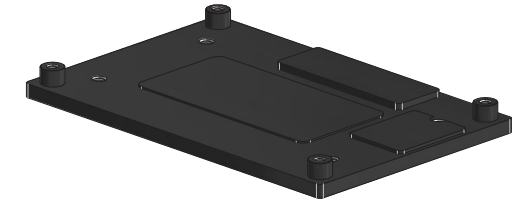


M2.5 x 6 mm threaded standoff for threaded version
or
ø2.7 x 6 mm non-threaded standoff for borehole version

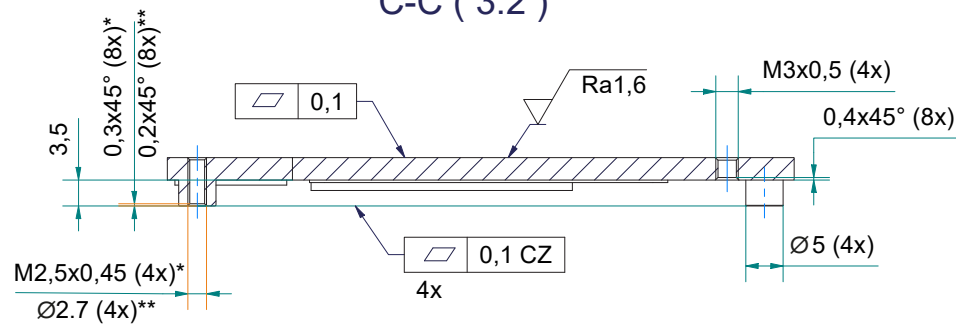
* For threaded version
** For borehole version



(1:1)



C-C (3:2)

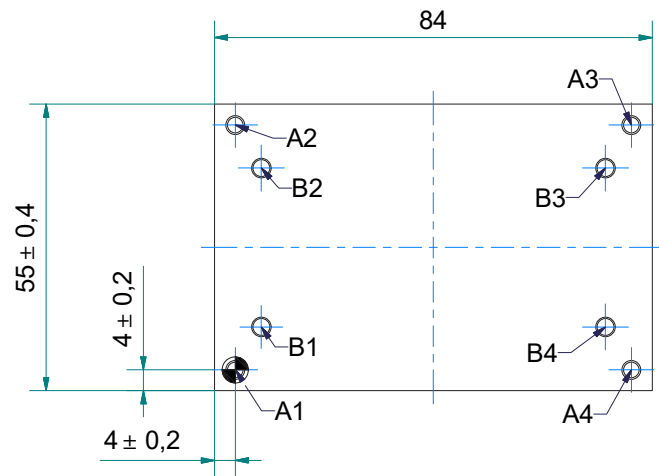


All dimensions are in [mm]
All non-dimensioned radii are R=1mm

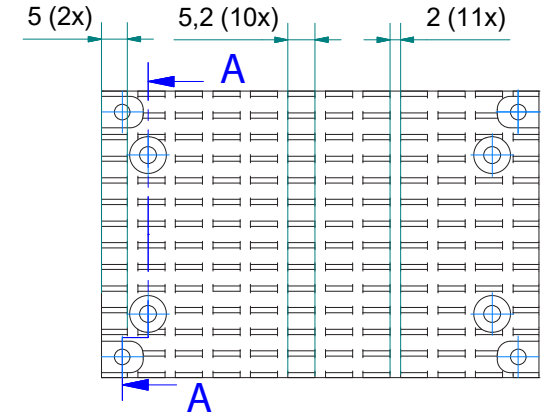
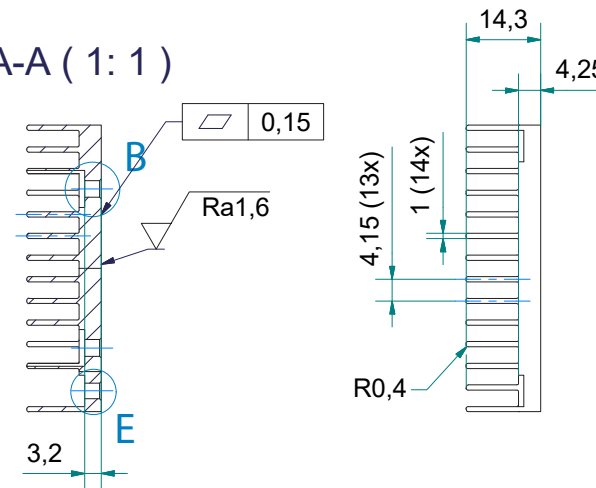
○ M2.5 x 6 mm threaded standoff for threaded version
or
Ø2.7 x 6 mm non-threaded standoff for borehole version

* For threaded version
** For borehole version

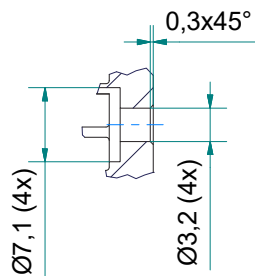
4.2 CSP Dimensions



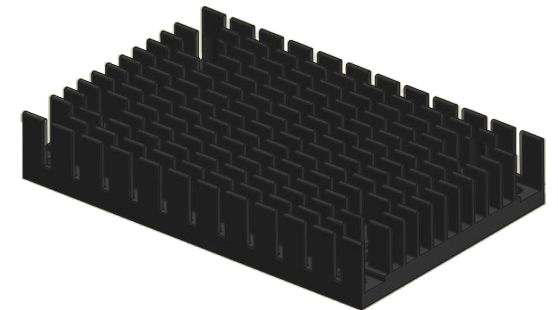
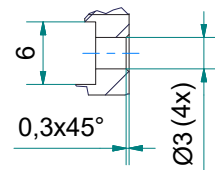
A-A (1 : 1)



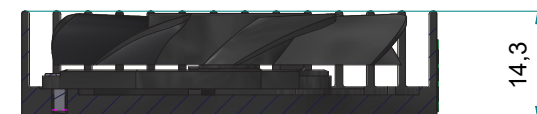
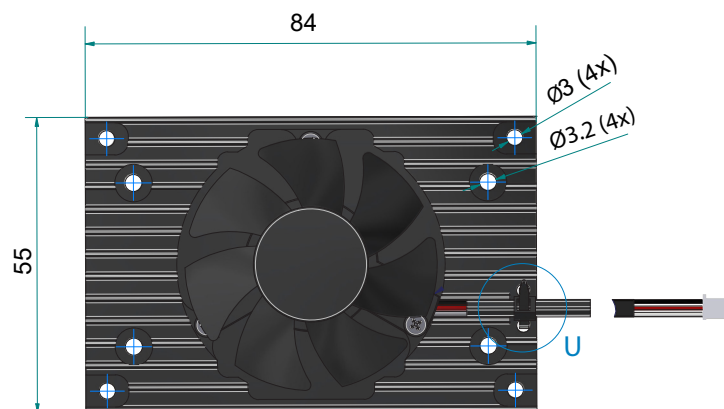
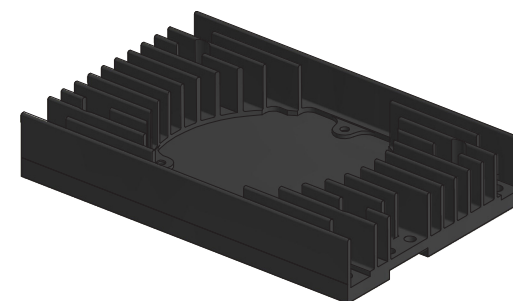
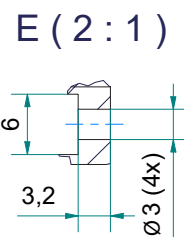
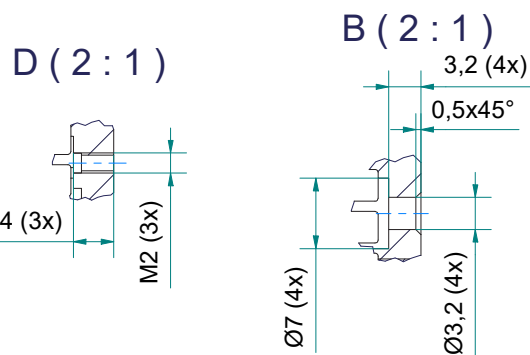
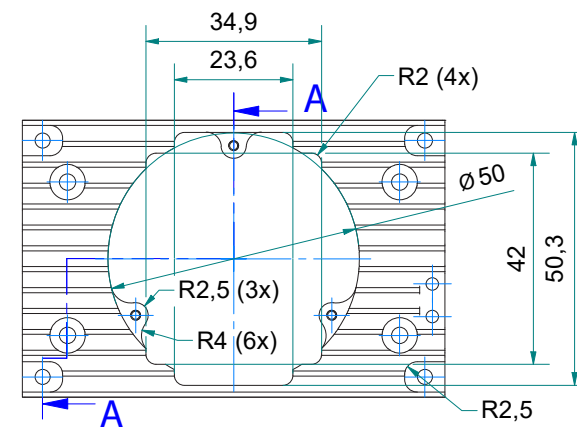
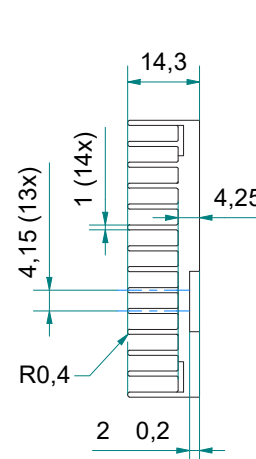
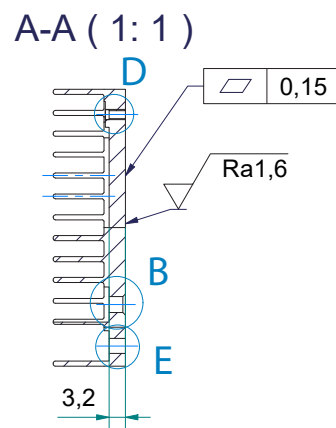
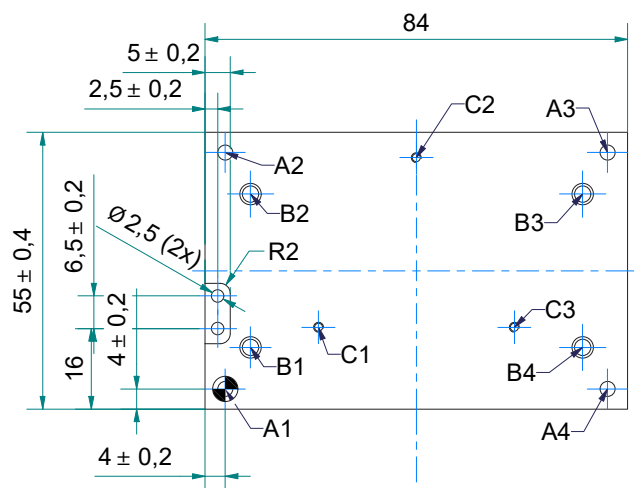
B (2 : 1)



E (2 : 1)



4.3 CSA Dimensions



5 Connector Rows

The conga-MC1000 is connected to the carrier board via a 220-pin connector (COM Express® Type 10 pinout). This connector is broken down into two rows (rows A and B). The following subsystems can be found on conga-MC1000 COM Express® connector rows A and B.

5.1 PCI Express

The conga-MC1000 offers four PCIe® lanes on the COM Express connector. The lanes are Gen 4.0 compliant and offer support for full 32 GT/s bandwidth in each direction per x1 link. Default configuration for the lanes is a 4 x1 link. Other configurations are possible as shown in the table below but require a customized BIOS firmware. Contact congatec technical support for more information.

The PCI Express® interface is based on the PCI Express® Base Specification Revision 6.0. For more information, refer to Table 21 "General Purpose PCI Express® Lanes Signal Descriptions".

Table 10 PCI Express® Options

	x1	x2	x4
Default	4		
Bifurcation Option 1	2	1	
Bifurcation Option 2		2	
Bifurcation Option 3			1



Bifurcation options 1, 2 and 3 require customized BIOS.

5.2 NBASE-T Ethernet

The conga-MC1000 offers a 2.5 Gigabit Ethernet interface via an onboard Intel® i226-LM/IT controller. The interface supports:

- full-duplex operation at 10/100/1000/2500 Mbps ^{1,2}
- half-duplex operation at 10/100 Mbps ^{1,2}
- Time Sensitive Networking ³
- Wake on LAN

The table below describes the LED signals of NBASE-T Ethernet interface.

Table 11 NBASE-T Ethernet LED Description

Signals	Description
GBE0_ACT#	Ethernet controller activity indicator
GBE0_LINK# ^{1,2}	Ethernet controller link indicator
GBE0_LINK_MID# ²	Ethernet controller link indicator for 1000 Mbps (lower link speed)
GBE0_LINK_MAX# ²	Ethernet controller link indicator for 2500 Mbps (maximum link speed)



Note

- ¹ The GBE0_LINK# output is not active during a 10 Mb and 100 Mb connection. It is only active during a 1 Gb or 2.5 Gb connection. This is a limitation of Ethernet controller since it has only three LED outputs.
- ² The GBE0_LINK# signal is a logic AND of the GBE0_LINK_MID# and GBE0_LINK_MAX# signals on the conga-MC1000 module.
- ³ Not supported in Windows Operating Systems.

5.3 SATA

The conga-MC1000 supports two SATA interfaces by default. Since Panther Lake-H platform does not natively support SATA, two port SATA controller (JMICRON® JMB582) is integrated to realize SATA Port 0 and SATA Port 1. The interfaces support:

- SATA specification revision 3.2
- data transfer rates up to 6.0 Gb/s
- Hot-plug detect



Note

- ¹ The SATA controller is multiplexed with a PCIe Gen 4 lane.
- ² The interface does not support legacy mode using I/O space.

5.4 Optional SSD

The conga-MC1000 offers a x4 PCIe Gen 5 port for an optional onboard NVMe SSD (Gen3/4) storage of up to 1 TB. This option is only available on custom variants with BOM modification. For more information, contact your local congatec sales representative.

5.5 USB

The conga-MC1000 offers a total of ten USB ports offering following USB configurations:

- up to eight USB 2.0 ports
- up to two flexible HSIO ports for USB 3.2 Gen 2

5.5.1 USB 2.0

The conga-MC1000 offers up to eight USB 2.0 interfaces on the COM Express connector. The interfaces support:

- USB 2.0 specification
- High-Speed, Full-Speed and Low-Speed USB signaling
- data transfers of up to 480 Mbps

5.5.2 USB 3.2

The conga-MC1000 offers SuperSpeed signals for up to two USB 3.2 ports, each supporting up to USB 3.2 Gen 2x1 (10 Gbps). The xHCI host controller supports:

- USB 3.2 specification
- SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling
- data transfers of up to 10 Gbps for USB 3.2 Gen 2 port
- supports USB debug port on all USB 3.2 capable ports



Note

1. *Ensure the carrier board is designed for USB 3.2 Gen 2 operation and it is recommended to have an onboard USB redriver. For USB 3.2 Gen 2 design considerations, contact congatec technical support center.*
2. *Each USB 3.2 port requires one USB 2.0 port and corresponding USB 3.2 SuperSpeed signals.*
3. *USB dual role is not supported.*

5.6 High Definition Audio (HDA) Interface

conga-MC1000 can support following audio interfaces:

- HD Audio
- SoundWire (Assembly option)

The conga-MC1000 provides HD Audio by default and carrier board audio using HDA codec. SoundWire can be offered as an untested assembly option.



Note

SPKR signal is not supported on the conga-MC1000.

5.7 Digital Display Interface

The conga-MC1000 offers two display interfaces:

- DDI0 supports VESA® DisplayPort™ Standard 2.1 upto 20 Gb/s (UHBR20)
- LVDS_A supports LVDS by default

Optionally, LVDS_A can support eDP instead of LVDS (assembly option).

The supported display combinations are shown below:

Table 12 Display Combination

	DDI0		LVDS_A	
	Display Technology	Max. Resolution	Display Technology	Max. Resolution
Default	DP++	3840 x 2160 @ 240Hz 4096x2160 @ 60 Hz	LVDS (single channel)	1024 x 768 @ 60 Hz
Option	-	-	eDP	4096x2160 @ 60Hz



Note

To support the maximum resolution of the DP++, it is recommended to implement a retimer on the carrier board.

5.7.1 DP++

The conga-MC1000 offers one Dual-mode DisplayPort (DP++) interface at DDI0 with support for:

- VESA® DisplayPort™ Standard 2.1

-
- VESA DSC 1.2b
 - Up to 4096x2160 @ 60 Hz (retimer on carrier board is recommended for 4K)



To support the maximum resolution of the DP++, a retimer is recommended to be implemented on the carrier board.

5.7.2 LVDS/eDP

The conga-MC1000 offers a single channel LVDS interface on the COM Express® connector. The interface is provided by routing the onboard NXP® PTN3460 eDP to LVDS bridge to the eDP port of the SoC. The bridge processes the incoming DisplayPort stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format. The LVDS interface supports:

- ANSI/TIA/EIA-644-A-2001 standard
- Single LVDS bus operation up to 112 mega pixels per second
- Up to 1024 x 768 @ 60Hz resolution in single LVDS bus mode
- Color depth of 18 bits per pixel (bpp) or 24 bpp
- RGB data packing as per JEIDA and VESA data formats
- Pixel clock frequency from 25 MHz to 112 MHz

Optionally, the interface can offer eDP 1.3 (4096x2160 @60Hz) signals instead of LVDS (assembly option).

The eDP interface supports:

- eDP 1.4b specification
- VESA DSC 1.2a
- Spread-Spectrum Clocking



The LVDS/eDP interface does not support both LVDS and eDP signals at the same time.

5.8 UART/CAN

conga-MC1000 offers two standard UART interfaces (UART0 and UART1) via the embedded board controller KSC 2.0 by default. These interfaces comply with UART 16550 protocol and they support up to 115200 bps.

conga-MC1000 does not support CAN interface.



Note

The UART interfaces do not support hardware handshake and flow control.

5.9 LPC Bus/eSPI

The conga-MC1000 offers the LPC bus through an eSPI to LPC bridge. The nominal clock frequency of the bridge is 24 MHz. For information about the decoded LPC addresses, see section 9 "System Resources".

The LPC interface is connected to the Enhanced Serial Peripheral Interface (eSPI) controller of the SoC via a Microchip ECE1200 eSPI to LPC bridge by default. Optionally, the conga-MC1000 can offer eSPI instead of LPC (assembly option).

Based on the configuration used (LPC or eSPI enabled), the ESPI_EN# signal has to be routed properly. ESPI_EN# signals to the module whether LPC or eSPI is used. If ESPI_EN# is unconnected on the carrier, LPC operation is expected. On the contrary for eSPI operation, ESPI_EN# has to be connected to GND on the carrier. To be able to detect the correct mode of operation, the module will implement a pull-up resistor on this signal. The module refuses to boot up if the module and carrier configurations do not match.



Note

The LPC clock frequency is 24 MHz. The LPC_DRQ# signal is not supported.

5.10 General Purpose SPI (GP-SPI)

The conga-MC1000 offers a General Purpose SPI interface via the KSC 2.0 by default and from the PTL-SOC as an assembly option.

To maintain backward compatibility to predecessor designs, it is possible to connect the GSPI interface to COMe Boot SPI pins as an assembly option.

5.11 SPI

The conga-MC1000 offers an onboard Winbond® W25Q256JWPIQ SPI flash.

You can boot the conga-MC1000 from the carrier board if you integrate an off-module flash device (BIOS) on the carrier board. This implementation is especially useful when evaluating a customized BIOS.

5.11.1 BIOS Flash Selection

The boot select pins BIOS_DIS0# and BIOS_DIS1# are configured to load the firmware BIOS from the conga-MC1000 by default. Optionally, you can configure these pins to load the boot firmware from the carrier board flash as described in the table below.

Table 13 BIOS Select Options

BIOS_DIS1#	BIOS_DIS0#	Boot Option
N.C.	N.C.	Boot from module SPI flash (default)
GND	N.C.	Boot from carrier board SPI flash

5.12 I²C Bus

The I²C bus is implemented through the KSC 2.0. The KSC 2.0 provides a fast-mode, multi-master I²C bus with maximum I²C bandwidth.

Table 14 Reserved I²C Addresses

8-bit Device Address	Device	Description
0xA0	Module EEPROM ¹	Module Embedded EEPROM (JIDA EEPROM)
0xAE	Carrier board EEPROM ¹	Reserved for COM Express® carrier board EEPROM
0xC0	eDP-to-LVDS bridge	Internal I2C devices
0xA0	external LVDS EEPROM	
0x20	IMVP9.3 voltage regulator	



Note

1. External user-accessible I2C - available at COMe pins I2C_CK, I2C_DAT

5.13 GPIOs

The conga-MC1000 offers eight General Purpose Input/Output signals on the A-B connector. The GPIOs are controlled by the KSC 2.0.

5.14 SMBus

On conga-MC1000, the System Management Bus is provided by the SoC and can be accessed at the COM express pinout. It is an I²C bus variant for system management functions. SM Bus is routed on the module to the NVMe, COMe Connector, and to the KSC 2.0.

5.15 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. See screenshot below.



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

It is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the “power good” signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, you must make sure that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-MC1000 provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-MC1000's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the COM Express connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the COM Express connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

Input power of 4.75 - 20 volt is the sole operational power source for the conga-MC1000. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-MC1000 application:

- It has also been noticed that on some occasions, problems occur when using a power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush current on the conga-MC1000 VCC_5V_SB power rail is 3A and can go up as high as 3.5 A for 500ms and as high as 2.33 A on VCC power rail (12 V). Sufficient decoupling capacitance must be implemented on the carrier board to ensure proper power-up sequencing.

5.16 Power Management

ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).

6 Additional Features

The following additional features are available on the conga-MC1000.

6.1 KSC 2.0

The conga-MC1000 is equipped with Microchip MEC1521 microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or I²C bus from the x86 core architecture, resulting in higher performance and reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The KSC 2.0 supports the following features:

- Board information
- Watchdog
- Power loss control
- Fan control
- General Purpose SPI (see section 5.10 "General Purpose SPI (GP-SPI)")
- UART (see section 5.8 "UART/CAN")
- I²C bus (see section 5.12 "I²C Bus")
- General Purpose Input/Output (see section 5.13 "GPIOs")
- SMBus (see section 5.14 "SMBus")
- User EEPROM space

6.1.1 Board Information

The KSC 2.0 provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.1.2 Watchdog

The conga-MC1000 is equipped with a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, refer to [https://wiki.congatec.com/wiki/Watchdog_\(AN03\)](https://wiki.congatec.com/wiki/Watchdog_(AN03)).

**Note**

The conga-MC1000 module does not support the watchdog NMI mode.

6.1.3 Power Loss Control

The CPU provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The power loss control feature has two different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition

**Note**

The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.

6.1.4 Fan Control

The conga-MC1000 offers signals for fan control, thereby improving system management. The FAN_PWMOUT signal controls the system fan with PWM (Pulse Width Modulation) while the FAN_TACHIN signal provides the ability to monitor the system's fan RPMs (revolutions per minute).

**Note**

1. *Only a 3-wire fan is supported on the module.*
2. *For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express® Design Guide.*

6.2 OEM BIOS Customization

The conga-MC1000 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS.

The customization features supported are described below:

6.2.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary through AMI SCE Tool. This tool is not supported on the standard BIOS release, thus it requires customized BIOS to enable support for this tool. Contact congatec technical support for more information regarding AMI SCE Tool.

6.2.2 OEM BIOS Code/Data

With the congatec embedded BIOS, it used to be possible for system designers to add their own code to the BIOS POST process. This feature is no longer supported with the new UEFI based firmware.

6.2.3 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.3 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec has defined an interface for the exchange of data between a x86 CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addition to the ACPI-compliant Control Method Battery mentioned above, the latest versions of the conga-MC1000 BIOS and board controller firmware also support the LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface contact your local congatec sales representative.

6.4 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface)

is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide at www.congatec.com.

6.5 Suspend to Ram

The Suspend to RAM feature is available on the conga-MC1000.

7 conga Tech Notes

The Intel® Panther Lake (PTL) processor is a 64-bit, multi-core processor built on Intel® 18A process, N6 and N3E technology. Some of the important features supported by the processor are:

- Intel® Image Processing Unit 7.5 (Intel® IPU 7.5)
- Intel® Neural Processing Unit (Intel® NPU)
- Intel® VT-x and VT-d
- Intel® Turbo Boost Technology 2.0
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)
- Intel® Thread Director
- Intel® Boot Guard
- Intel® SpeedStep Technology
- Intel® Active Management Technology (Intel® AMT)
- Intel® Platform Trust Technology (Intel® PTT)
- Intel® Dynamic Tuning Technology (Intel® DTT)
- Intel® Total Memory Encryption (Intel® TME)
- Intel® Volume Management Device (Intel® VMD)
- Intel® High Definition Audio (HD Audio)
- Intel® Smart Sound Technology (SST)
- Intel® Active Management Technology (AMT)

7.1 Processor Performance Control

7.1.1 Intel® SpeedStep® Technology (EIST)

Intel® processors found on the conga-MC1000 run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® Technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states to efficiently operate the processor when it is not being fully used. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can

be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that the power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

The Intel® Core™ Ultra Series 3 processor family supports Intel® Speed Shift, a new and energy efficient method for frequency control. This feature is also referred to as Hardware-controlled Performance States (HWP). The feature is a hardware implementation of the ACPI defined Collaborative Processor Performance Control (CPPC2) and is supported by newer operating systems (Win 8.1 or newer).

With this feature enabled, the processor autonomously selects performance states based on workload demand and thermal limits while also considering information provided by the OS e.g., the performance limits and workload history.

7.1.2 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology allows processor cores to run faster than the base operating frequency if it is operating below power, current, and temperature specification limits. Intel® Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state. The maximum frequency of Intel® Turbo Boost Technology depends on the number of active cores. The amount of time the processor spends in the Intel® Turbo Boost Technology state depends on the workload and operating environment.

Any of the following can set the upper limit of Intel® Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating within its defined power and thermal limits and the workload demands additional performance, the processor frequency dynamically increases above the base frequency until the upper limit is reached or the maximum achievable frequency for the number of active cores is attained.

For more information about Intel® Turbo Boost Technology, visit the Intel® website.



- Note**
1. *For real-time sensitive applications, disable EIST and Turbo Mode in the BIOS setup to ensure a more deterministic performance.*
 2. *Disable Turbo mode for industrial use condition.*

7.2 Intel® Neural Processing Unit (Intel® NPU)

The Intel® Neural Processing Unit (NPU) is a dedicated hardware accelerator integrated into Intel® Panther Lake processors. It enables high-performance processing for AI applications while maintaining optimized power consumption, making it suitable for embedded, edge, and client platforms. The NPU offloads AI-related tasks from the CPU and GPU, improving overall system efficiency and responsiveness. It consists of a host control subsystem and a deep learning accelerator, which together manage task scheduling and execution. The deep learning accelerator is based on multiple Neural Compute Engine (NCE) tiles that provide scalable parallel processing capabilities. These tiles integrate specialized compute units and local memory to efficiently process neural network operations.

7.3 Adaptive Thermal Monitor and Catastrophic Thermal Protection

Intel® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu "CPU submenu".

The Adaptive Thermal Monitor controls the processor temperature using two methods:

- Adjusting the processor's operating frequency and core voltage (EIST transitions)
- Modulating (start/stop) the processor's internal clocks at a duty cycle of 25% on and 75% off

When activated, the TCC causes both processor core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated. Clock modulation is activated if frequency and voltage adjustments are insufficient. Additional hardware, software driver, or operating system support is not required.

Intel® processors use the THERMTRIP# signal to shut down the system if the processor's silicon reaches a temperature of approximately 125°C. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.



Note

To ensure the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® processor's respective datasheet can provide you with more information about this subject.

7.4 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel® architecture microprocessors and chipsets.

Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) have hardware support in the processor to improve the virtualization performance and robustness.

conga-zones hypervisor supports Intel® VT and is verified on all current congatec x86 hardware.



Note

congatec supports conga-zones hypervisor (formerly RTS Hypervisor).

7.5 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to implement cooling decisions according to the demands of the application.

The conga-MC1000 offers hardware-based support for passive and active cooling. Passive cooling is implemented in the Intel® CPU via the Thermal Control Circuit (TCC) Activation Offset setting in the CPU configuration setup sub-menu. The TCC in the processor is activated at 100°C by default but can be lowered by the Activation Offset—for example, an activation offset of "10" will activate TCC at 90°C. ACPI OS support is not required. See section 7.3 "Adaptive Thermal Monitor and Catastrophic Thermal Protection" for more information

The KSC 2.0 supports active cooling solution. The KSC 2.0 controls the fan's speed based on the temperature readings of the CPU. This feature does not require ACPI OS support. The only software-controlled thermal trip point on conga-MC1000 is the Critical Trip Point.

The active or passive cooling policy should ensure that the CPU temperature does not reach this trip point. However, if the critical trip point is reached, the OS will shut down properly in order to prevent damage to the system.

Use the "critical trip point" setup node in the BIOS setup menu to determine the temperature threshold at which the system shuts down.



Note

The Automatic Critical Trip Point BIOS setting shuts down the system at 5°C above the maximum specified temperature of the processor

7.6 ACPI Suspend Modes and Resume Events

The conga-MC1000 BIOS supports S3 (Suspend to RAM), S4 (Suspend to Disk), S5 (Soft-Off) and S5e (enhanced Soft-Off).

Table 15 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5
Onboard LAN Event	Device driver must be configured to support Wake On LAN.
SMBALERT#	Wakes unconditionally from S3-S5
PCI Express WAKE#	Wakes unconditionally from S3-S5
WAKE#	Wakes unconditionally from S4
PME#	Activate the wake-up capabilities of a PCI device using Windows Device Manager configuration options or set Resume On PME# to "Enabled" in the BIOS setup menu.
USB Mouse/Keyboard Event	When standby mode is set to S4, USB hardware must be powered by standby power source. Set "USB Device Wakeup" from "S4" to "Enabled" in the ACPI section of the BIOS setup menu (if setup node is available in BIOS setup program). In Device Manager, look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.

For the Power and System Management Signals, see Table 31 "Power and System Management Signal Descriptions".

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express® Type 10 connectors used for congatec GmbH modules. The pinout of the modules complies with COM Express® Type 10 Rev. 3.1.

The table below describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express® module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.



Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip’s datasheet.

Table 16 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V
I/O 5V	Bi-directional signal 5V
I 3.3V	Input 3.3V
I 5V	Input 5V
I/O 3.3VSB	Input 3.3V active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output pin
P	Power input pin
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

8.1 COM Express® Connector Pinout

Table 17 COM Express® Connector Pinouts

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND(FIXED)	B1	GND(FIXED)	A56	GP_SPI_CK	B56	GP_SPI_MOSI
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#/ ESPI_CS0# ²	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK_MID#	B4	LPC_AD0/ ESPI_IO_0 ²	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK_MAX#	B5	LPC_AD1/ ESPI_IO_1 ²	A60	GND(FIXED)	B60	GND(FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2/ ESPI_IO_2 ²	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3/ ESPI_IO_3 ²	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#/ ESPI_ALERT0# ²	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#/ ESPI_ALERT1# ²	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK/ ESPI_CK ²	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND(FIXED)	B11	GND(FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF ¹	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND(FIXED)	B70	GND(FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	eDP_TX2+ ² / LVDS_A0+	B71	DDIO_PAIR0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	eDP_TX2- ² / LVDS_A0-	B72	DDIO_PAIR0-
A18	SUS_S4#	B18	SUS_STAT# / ESPI_RESET# ²	A73	eDP_TX1+ ² / LVDS_A1+	B73	DDIO_PAIR1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	eDP_TX1- ² / LVDS_A1-	B74	DDIO_PAIR1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	eDP_TX0+ ² / LVDS_A2+	B75	DDIO_PAIR2+
A21	GND(FIXED)	B21	GND(FIXED)	A76	eDP_TX0- ² / LVDS_A2-	B76	DDIO_PAIR2-
A22	USB_SSRX0-	B22	USB_SSTX0-	A77	eDP_VDD_EN ² / LVDS_VDD_EN	B77	DDIO_PAIR4+ ¹
A23	USB_SSRX0+	B23	USB_SSTX0+	A78	LVDS_A3+	B78	DDIO_PAIR4- ¹

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP_BKLT_EN ² / LVDS_BKLT_EN
A25	USB_SSRX1-	B25	USB_SSTX1-	A80	GND(FIXED)	B80	GND(FIXED)
A26	USB_SSRX1+	B26	USB_SSTX1+	A81	eDP_TX3+/ LVDS_A_CK+	B81	DDIO_PAIR3+
A27	BATLOW#	B27	WDT	A82	eDP_TX3- ² / LVDS_A_CK-	B82	DDIO_PAIR3-
A28	(S)ATA_ACT#	B28	HDA_SDIN2 /SNDW0_CLK ²	A83	eDP_AUX+ ² / LVDS_I2C_CK	B83	eDP_BKLT_CTRL ² / LVDS_BKLT_CTRL
A29	HDA_SYNC	B29	HDA_SDIN1 /SNDW0_DAT ²	A84	eDP_AUX- ² / LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	HDA_RST#	B30	HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND(FIXED)	B31	GND(FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	HDA_BITCLK	B32	SPKR ^{2,3}	A87	eDP_HPD ²	B87	VCC_5V_SBY
A33	HDA_SDOOUT	B33	I2C_CK	A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0# / ESPI_SAFS ¹	B34	I2C_DAT	A89	PCIE_CLK_REF-	B89	DDIO_HPD
A35	THRMTRIP#	B35	THRM#	A90	GND(FIXED)	B90	GND(FIXED)
A36	USB6-	B36	USB7	A91	SPI_POWER	B91	DDIO_PAIR5+ ¹
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	DDIO_PAIR5- ¹
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	DDIO_PAIR6+ ¹
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	DDIO_PAIR6- ¹
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	DDIO_DDC_AUX_SEL
A41	GND(FIXED)	B41	GND(FIXED)	A96	TPM_PP ¹	B96	USB7_HOST_PRSENT
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	DDIO_CTRLCLK_AUX+
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	DDIO_CTRLDATA_AUX-
A45	USB0-	B45	USB1-	A100	GND(FIXED)	B100	GND(FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI_EN# ²	A102	SER1_RX	B102	FAN_TACHIN
A48	RSMRST_OUT#	B48	USB0_HOST_PRSENT ²	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ/ ESPI_CS1# ²	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND(FIXED)	B51	GND(FIXED)	A106	VCC_12V	B106	VCC_12V
A52	RSVD ¹	B52	RSVD ¹	A107	VCC_12V	B107	VCC_12V
A53	RSVD ¹	B53	RSVD ¹	A108	VCC_12V	B108	VCC_12V
A54	GPIO	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	GP_SPI_CS#	B55	GP_SPI_MISO	A110	GND(FIXED)	B110	GND(FIXED)

^{1.} Not connected

^{2.} Assembly option

^{3.} Not supported in the default configuration

8.2 COM Express® Connector Signal Descriptions

Table 18 High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST#	A30	High Definition Audio Reset: This signal is the master hardware reset to external codec(s).	O 3.3V	PD 100kΩ	
HDA_SYNC	A29	High Definition Audio Sync: This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		
HDA_BITCLK	A32	High Definition Audio Bit Clock Output: This signal is a 24.000 MHz serial data clock generated by the Intel® High Definition Audio controller.	O 3.3V	PD 100kΩ	
HDA_SDOUT	A33	High Definition Audio Serial Data Out: This signal is the serial TDM data output to the codec. This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3V		
HDA_SDIN[0]	B30	High Definition Audio Serial Data In [0]: This signal is a serial TDM data input from the codec. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	I/O 3.3V		
HDA_SDIN1 /SNDW0_DAT	B29	High Definition Audio Serial Data In [0]: This signal is a serial TDM data input from the codec. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio. Alternative use as SoundWire bi-directional data line			
HDA_SDIN2 /SNDW0_CLK	B28	High Definition Audio Serial Data In [0]: This signal is a serial TDM data input from the codec. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.			
		Alternative use as SoundWire bi-directional clock line			

Table 19 NBASE-T Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+	A13	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10 Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		Twisted pair signals for external transformer.
GBE0_MDI0-	A12							
GBE0_MDI1+	A10		1000	100	10			
GBE0_MDI1-	A9							
GBE0_MDI2+	A7	MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
GBE0_MDI2-	A6	MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
GBE0_MDI3+	A3	MDI[2]+/-	B1_DC+/-					
GBE0_MDI3-	A2	MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.				O 3.3VSB		
GBE0_LINK_MID#	A4	Gigabit Ethernet Controller 0 100 Mbit/sec link indicator, active low.				O 3.3VSB		

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_LINK_MAX#	A5	Gigabit Ethernet Controller 0 1000 Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.	REF		
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal. See section 4.3.5 "SDP Pins" of the COM Express 3.0 Specification for details.	I/O	PD 10kΩ	Signal is provided by the Intel i226 controller

Table 20 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.2
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.2
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.2
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.2
S_ATA_ACT#	A28	Serial ATA activity indicator, active low.	O 3.3V	PU 10kΩ	

Table 21 General Purpose PCI Express® Lanes Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express lanes.	O PCIE		

Table 22 **USB Signal Descriptions**

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB Port 0 differential data pairs	I/O		
USB1+ USB1-	B46 B45	USB Port 1 differential data pairs	I/O		
USB2+ USB2-	A43 A42	USB Port 2 differential data pairs	I/O		
USB3+ USB3-	B43 B42	USB Port 3 differential data pairs	I/O		
USB4+ USB4-	A40 A39	USB Port 4 differential data pairs	I/O		
USB5+ USB5-	B40 B39	USB Port 5 differential data pairs	I/O		
USB6+ USB6-	A37 A36	USB Port 6 differential data pairs	I/O		
USB7+ USB7-	B37 B36	USB Port 7 differential data pairs	I/O		
USB0_HOST_PRSENT	B48	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.		PD 47 kΩ	
USB7_HOST_PRSENT	B96	Module USB client may detect the presence of a USB host on USB7. A high value indicates that a host is present.		PD 47 kΩ	
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10kΩ 3.3V (S5)	
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10kΩ 3.3V (S5)	
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10kΩ 3.3V (S5)	
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10kΩ 3.3V (S5)	
USB_SSTX0+ USB_SSTX0-	B23 B22	Additional transmit signal differential pairs for the SuperSpeed USB data path. Supports up to SuperSpeed USB 10Gbps.	O USB-SS		
USB_SSTX1+ USB_SSTX1-	B26 B25	Additional transmit signal differential pairs for the SuperSpeed USB data path. Supports up to SuperSpeed USB 10Gbps.	O USB-SS		
USB_SSRX0+ USB_SSRX0-	A23 A22	Additional receive signal differential pairs for the SuperSpeed USB data path. Supports up to SuperSpeed USB 10Gbps.	I USB-SS		
USB_SSRX1+ USB_SSRX1-	A26 A25	Additional receive signal differential pairs for the SuperSpeed USB data path. Supports up to SuperSpeed USB 10Gbps.	I USB-SS		

Table 23 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ eDP_TX2+	A71	LVDS Channel A differential pair 0 Embedded Display Port channel 0 differential pair 2	O LVDS O eDP		
LVDS_A0- eDP_TX2-	A72	LVDS Channel A differential pair 0 Embedded Display Port channel 0 differential pair 2	O LVDS O eDP		
LVDS_A1+ eDP_TX1+	A73	LVDS Channel A differential pair 1 Embedded Display Port channel 0 differential pair 1	O LVDS O eDP		
LVDS_A1- eDP_TX1-	A74	LVDS Channel A differential pair 1 Embedded Display Port channel 0 differential pair 1	O LVDS O eDP		
LVDS_A2+ eDP_TX0+	A75	LVDS Channel A differential pair 2 Embedded Display Port channel 0 differential pair 0	O LVDS O eDP		
LVDS_A2- eDP_TX0-	A76	LVDS Channel A differential pair 2 Embedded Display Port channel 0 differential pair 0	O LVDS O eDP		
LVDS_A3+ LVDS_A3-	A78 A79	LVDS Channel A differential pair 3	O LVDS		
LVDS_A_CK- eDP_TX3-	A81	LVDS Channel A differential clock Embedded Display Port channel 0 differential pair 3	O LVDS O eDP		
LVDS_A_CK- eDP_TX3-	A82	LVDS Channel A differential clock Embedded Display Port channel 0 differential pair 3	O LVDS O eDP		
LVDS_VDD_EN eDP_VDD_EN	A77	Panel power enable	O 3.3V	PD 100kΩ	
LVDS_BKLT_EN eDP_BKLT_EN	B79	Panel backlight enable	O 3.3V	PD 100kΩ	
LVDS_BKLT_CTRL eDP_BKLT_CTRL	B83	Panel backlight brightness control	O 3.3V		
LVDS_I2C_CK eDP_AUX+	A83	DDC lines used for flat panel detection and control. Embedded Display Port AUX channel pair	I/O 3.3V I/O eDP	PU 2.2kΩ 3.3V	
LVDS_I2C_DAT eDP_AUX-	A84	DDC lines used for flat panel detection and control. Embedded Display Port AUX channel pair	I/O 3.3V I/O eDP	PU 2.2kΩ 3.3V	

**Note**

LVDS is enabled by default. eDP is can be selected via BIOS setup.

Table 24 LPC/eSPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3] / eSPI_IO_[0:3]	B4-B7	LPC multiplexed address, command and data bus. eSPI Master Data Input / Outputs.	I/O 3.3V I/O 1.8V		

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_FRAME# / ESPI_CS0#	B3	LPC frame indicates the start of an LPC cycle. eSPI Master Chip Select Outputs Driving Chip Select0# low selects eSPI slave. Each eSPI slave is connected to a dedicated Chip Select # pin.	O 3.3V O 1.8V		
LPC_CLK / ESPI_CLK	B10	LPC clock output (24MHz). This pin provides the reference timing for all the serial input and output operations.	O 3.3V O 1.8V		24MHz
LPC_DRQ[0:1]# / ESPI_ALERT[0:1]#	B8-B9	LPC serial DMA request . eSPI pins used by eSPI slave to request service from the eSPI master.	I 3.3V I 1.8V		
LPC_SERIRQ / ESPI_CS1#	A50	LPC serial interrupt. Low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select pin.	I/O OD 3.3V O 1.8V	PU 8.2kΩ 3.3V (S0)	
SUS_STAT#	B18	Indicates the system will enter a low power state soon. Used to notify LPC devices. Reset eSPI interface for both master and slaves. Typically driven from eSPI master to eSPI slaves.	O 3.3VSB O 1.8V	PD 10kΩ	
ESPI_RESET#				PD 75kΩ	
ESPI_EN#	B47	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The Carrier should only float this line or pull it low.	I 3.3V	PU 20kΩ	If the module and carrier configurations do not match, the module may not boot up.
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10kΩ 3.3VSB	See section 5.11.1 "BIOS Flash Selection"
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. Refer to table 4.15 of the COM Express Module Base Specification 3.1 for strapping options of BIOS disable signals.	I 3.3VSB	PU 10kΩ 3.3VSB	



Note

1. LPC is enabled by default. eSPI is offered as an assembly option.
2. DMA is not supported.

Table 25 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for carrier board SPI.	O 3.3VSB	PU 10kΩ 1.8V (S5)	
SPI_MISO	A92	Master Input Slave Output: SPI output data from carrier board SPI device to module.	I 3.3VSB		
SPI_MOSI	A95	Master Output Slave Input: SPI output data from module to carrier board SPI.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	O 3.3VSB		

**Note**

1. The SPI only supports a BIOS flash device by default. The BIOS flash device must be powered from the standby rail. For other options, see section 5.11 "SPI".
2. Route the SPI signals as short as possible because of their limited drive strength.

Table 26 General Purpose SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GP_SPI_CS#	A55	Chip select from Module SPI Master to Carrier SPI Slave	O 3.3VSB		
GP_SPI_MISO	A95	Data in to Module SPI Master from Carrier SPI Slave "Master In Slave Out"	I 3.3VSB		
GP_SPI_MOSI	A94	Data out from Module SPI Master to Carrier SPI Slave "Master Out Slave In"	O 3.3VSB		
GP_SPI_CK	A56	Clock from Module SPI Master to Carrier SPI Slave	O 3.3VSB		

Table 27 DDI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DDIO_PAIR0+	B71	Multiplexed with DP0_LANE0+	O DP		
DDIO_PAIR0-	B72	Multiplexed with DP0_LANE0-			
DDIO_PAIR1+	B73	Multiplexed with DP0_LANE1+	O DP		
DDIO_PAIR1-	B74	Multiplexed with DP0_LANE1-			
DDIO_PAIR2+	B75	Multiplexed with DP0_LANE2+	O DP		
DDIO_PAIR2-	B76	Multiplexed with DP0_LANE2-			
DDIO_PAIR3+	B81	Multiplexed with DP0_LANE3+	O DP		
DDIO_PAIR3-	B82	Multiplexed with DP0_LANE3-			
DDIO_HPD	B89	Detection of Hot Plug / Unplug and notification of the link layer.	I 3.3V	PD 100kΩ	
DDIO_CTRLCLK_AUX+	B98	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect.	I/O	PD 100kΩ	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access
		I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O OD 3.3V	PD 100kΩ	
DDIO_CTRLDATA_AUX-	B99	DP AUX- function if DDI1_DDC_AUX_SEL is no connect.	I/O	PU 100kΩ 3.3V	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access
		I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high.	I/O OD 3.3V	PU 100kΩ 3.3V	
DDIO_DDC_AUX_SEL	B95	Selects the function of DDIO_CTRLCLK_AUX+ and DDIO_CTRLDATA_AUX-.	I 3.3V	PD 1 MΩ	

Table 28 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter.	O 3.3V		PD expected on carrier board
SER0_RX	A99	General purpose serial port receiver.	I 3.3V		
SER1_TX / CAN_TX	A101	General purpose serial port transmitter (default). TX output for CAN Bus can be enabled via BIOS Setup menu.	O 3.3V		PD expected on carrier board
SER1_RX / CAN_RX	A102	General purpose serial port receiver (default). RX input for CAN Bus can be enabled via BIOS Setup menu.	I 3.3V		

**Note**

1. The SER1 options are described in section 5.8 "UART/CAN".
2. For the correct implementation, see the COM Express® Design Guide.

Table 29 I2C Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I2C port clock output	I/O OD 3.3VSB	PU 2.2 kΩ 3.3VSB	
I2C_DAT	B34	General purpose I2C port data I/O line	I/O OD 3.3VSB	PU 2.2 kΩ 3.3VSB	

Table 30 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V	PD 10 kΩ	Not supported in the default configuration. Support can be added on request.
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PD 10 kΩ	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O 3.3V		12V tolerant
FAN_TACHIN	B102	Fan tachometer input.	I	PU 47 kΩ 3.3V	Requires a fan with a two pulse output. 12V tolerant.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high.	I 3.3V		Not connected

**Note**

For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express® Design Guide.

Table 31 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10kΩ	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low.	I 3.3VSB	PU 10kΩ	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a main power input (VIN) that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3VSB	PD 10kΩ	
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V	PU 10kΩ	
SUS_STAT#	B18	Indicates the system will enter a low power state soon. Used to notify LPC devices. Reset eSPI interface for both master and slaves. Typically driven from eSPI master to eSPI slaves.	O 3.3VSB	PD 10kΩ	SUS_STAT# (default) Assembly option: eSPI
ESPI_RESET#			O 1.8V	PD 75kΩ	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up request signal.	I 3.3VSB	PU 10kΩ	
WAKE1#	B67	General purpose wake up signal. May be used to implement a wake-up request from an external device.	I 3.3VSB	PU 10kΩ	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low.	I 3.3VSB	PU 10kΩ	Assertion may prevent wake from S3-S5 state
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch.	I 3.3VSB	PU 47 kΩ	
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I 3.3VSB	PU 47 kΩ	

Table 32 Thermal Protection Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over temperature situation	I 3.3V	PU 10kΩ	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown	O 3.3V	PU 10kΩ	

Table 33 SM Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line	I/O OD 3.3VSB	PU 3.9k Ω	
SMB_DAT	B14	System Management Bus bidirectional data line	I/O OD 3.3VSB	PU 3.9k Ω	
SMB_ALERT#	B15	System Management Bus Alert - Active low input can be used to generate an SMI# (System Management Interrupt)	I 3.3VSB	PU 10k Ω	

**Note**

The SMBus options are described in section 5.14 "SMBus".

Table 34 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3VSB	PU 100k Ω 3.3V	
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3VSB	PU 100k Ω 3.3V	
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3VSB	PU 100k Ω 3.3V	
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3VSB	PU 100k Ω 3.3V	
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3VSB	PD 100k Ω	
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3VSB	PD 100k Ω	
GPO2	B57	General purpose output pins. Shared with SD_WP. Output from COM Express, input to SD	O 3.3VSB	PD 100k Ω	
GPO3	B63	General purpose output pins. Shared with SD_CD#. Output from COM Express, input to SD	O 3.3VSB	PD 100k Ω	

Table 35 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
TYPE10#	A97	Indicates to the carrier board that a Type 10 module is installed.	PDS	PD 47k Ω	

Table 36 **Power and GND Signal Descriptions**

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: 4.75V to 20V. All available VCC_12V pins on the connector(s) shall be used.	P		The conga-MC1000 is a Type 10 mini module and as such supports a wide power supply range between 4.75V and 20V.
VCC_5V_SBY	B84-B87	Standby power input: +5V nominal. If VCC5V_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real time clock circuit-power input: +3V nominal	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110 B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

9 System Resources

Information regarding the system resources of conga-MC1000 will be published with the final release of this user guide.

10 BIOS Setup Description

The BIOS setup description of the conga-MC1000 can be viewed without having access to the module. A BIOS user guide will be provided in the HTML format, along with the BIOS release package.

The BIOS user guide contains the BIOS setup description of a particular BIOS revision including default settings. The BIOS user guide is in HTML format and can be viewed using any internet browser. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.



Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-MC1000 is identified as MPL1R1xx, where:

- MPL1 is the project name
- R is the identifier for a BIOS ROM file
- 1 is the feature number
- xx is the major and minor revision number.

The binary size of conga-MC1000 BIOS is 32 MByte.

10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-MC1000 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. The utility has three versions—UEFI shell, Win32 command line, and Linux version.

10.4 Supported Flash Devices

The conga-MC1000 supports the following flash device:

- Winbond W25Q256JWPIQ (32MB)

The flash devices listed above can be used on the carrier board for external BIOS support.



For the latest supported flash devices, refer to https://wiki.congatec.com/wiki/Supported_SPI_Flash_Devices_for_BIOS.