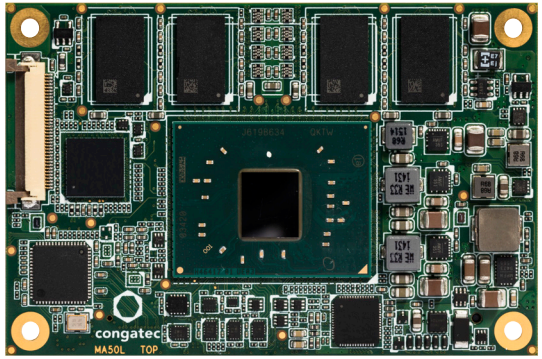

conga-MA5

COM Express® 2.1 Type 10 Mini Module with Intel® Apollo Lake Processors

User's Guide

Revision 1.13

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2017.04.07	BEU	• Preliminary release
1.0	2017.09.21	BEU	• Minor improvements throughout the document • Updated section 2.2 "Supported Operating Systems", 2.4 "Supply Voltage Standard Power", 2.4.1 Electrical Characteristics", 3 "Block Diagram", 5.7.3 "DVI-D", 5.8 "SD Card", 6.1.1 "eMMC 5.0", and 6.7 "Security Features" • Added inrush and maximum currents peaks paragraph to section 5.14 "Power Control" • Added section 5.16 "MIPI CSI-2" • Updated tables 7 "Power Consumption Values", 8 "CMOS Battery Power Consumption", 13 "COM Express Connector Pinouts", 16 "Serial ATA Signal Descriptions", 18 "ExpressCard Support Pins Signal Descriptions", 19 "USB Signal Descriptions", 20 "LVDS Signal Descriptions", 23 "DDI Signal Descriptions", 24 "DisplayPort (DP) Signal Descriptions", 25 "HDMI/DVI Signal Descriptions", 28 "Miscellaneous Signal Descriptions", 29 "Power and System Management Signal Descriptions" • Added fully legacy UART 16550 compliant LPC controller as assembly option • Added content to section 9 "System Resources"and 10 "BIOS Setup Description"
1.1	2018.06.25	BEU	• Added errata as a document to read in the preface section • Updated "Electrostatic Sensitive Device" information on page 3 • Updated security features in table 4 "Feature Summary" • Removed Android from supported OS in section 2.2 "Supported Operating Systems" • Added EFT caution to section 5.4.1 "USB 2.0" • Updated section 5.9 "General Purpose Serial Interface (UART)"
1.2	2018.08.21	BEU	• Minor improvements throughout the document
1.3	2018.10.16	BEU	• Corrected commercial operating temperature in section 2.7 "Environmental Specifications" • Corrected pin A83 and A84 description in table 20 "LVDS Signal Descriptions" • Added voltages and BIOS revision information to table 7 "Power Consumption Values"
1.4	2019.01.18	BEU	• Corrected image in section 2.3 "Mechanical Dimensions"
1.5	2019.04.16	BEU	• Corrected image in section 2.3 "Mechanical Dimensions"
1.6	2020.01.07	BEU	• Removed support for IoT 32-bit OS in section 2.2 " Supported Operating Systems" • Updated section 4 "Cooling Solutions" • Updated reference to power supply design guide in section 5.14 "Power Control" • Updated section 10.3 "Updating the BIOS" • Updated section 10.4 "Supported Flash Devices" • Added note about pulse width to several signals in table 29 • Added reference to BIOS Setup Description application note in section 10 "BIOS Setup Description" • Updated section 11 "Industry Specifications"
1.7	2021.02.19	BEU	• Corrected the storage temperature for industrial variants in section 2.7 “Environmental Specifications”
1.8	2021.04.15	BEU	• Updated display interfaces in table 2, 3, 4, 24, 26 and section 3 "Block Diagram", 5.7 "Digital Display Interface", 5.7.1 "Displayport (DP)" • Deleted sections 5.7.2 "HDMI", 5.7.3 "DVI-D", 11 "Industry Specifications"
1.9	2021.07.06	BEU	• Updated congatec AG to congatec GmbH throughout the document • Added software license information to preface section • Corrected typographical error in section 5.7 "Digital Display Interface" • Updated section 6.4 "congatec Battery Management Interface"

1.10	2023.01.24	BEU	• Updated RoHS statement in the preface section • Changed the discontinued Intel® I211 for commercial variants to Intel® I210 throughout the document • Corrected the USB port that supports dual role from USB0 to USB7 in table 20 "USB Signal Descriptions" • Added that USB port 7 supports dual role to the description in section 5.4 " Universal Serial Bus" • Updated section 6.2.3 "Power Loss Control"
1.11	2023.01.28	BEU	• Corrected mixed up descriptions in table 9 " Cooling Solution Variants"
1.12	2024.01.15	BEU	• Updated title page • Updated RoHS Directive • Added note to section 2.7 "Environmental Specifications" • Added caution and note to section 4 "Cooling Solutions" • Updated section 6.2.3 " Power Loss Control" • Renamed section 9.4 "SM Bus" to "SMBus"
1.13	2025.01.31	RVI	• Updated the preface section • Added a WEEE Compliance Decleration • Added a note to section 2.3 "Mechanical Dimensions" • Added new section 2.8 Storage Specifications • Added a note to section 5.8 "SD Card" • Updated the Table 24 "DDI Signal Descriptions"

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Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-MA5. It is one of four documents that should be referred to when designing a COM Express™ application. This user's guide should be read in conjunction with the document "Errata_congatec_xA5_designs". Click on the document name to download it.

The other reference documents that should be used include the following:

COM Express™ Design Guide
COM Express™ Specification

The links to these documents can be found on the congatec GmbH website at www.congatec.com. Additionally, check the restricted area of the congatec website at www.congatec.com and the website from the respective silicon vendor for relevant documents (e.g., Erratum, PCN, Sighting Reports, etc.).

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Terminology

Term	Description
GB	Gigabyte
GHz	Gigahertz
kB	Kilobyte
MB	Megabyte
Mbit	Megabit
kHz	Kilohertz
MHz	Megahertz
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
DDC	Display Data Channel
SoC	System On Chip
LVDS	Low-Voltage Differential Signaling
GbE	Gigabit Ethernet
eMMC	Embedded MultiMedia Card
MLC	Multi-level Cell
SLC	Single-level Cell
HDA	High Definition Audio
cBC	congatec Board Controller
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

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1 Introduction

COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express™ modules are available in following form factors:

- Mini 84 mm x 55 mm
- Compact 95 mm x 95 mm
- Basic 125 mm x 95 mm
- Extended 155 mm x110 mm

The COM Express Specification Rev 2.1 currently defines seven different pinout types. These are shown in the table below.

Table 1 Types of COM Express™ Pinouts/Features

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports
Type 1	A-B	Up to 6			1
Type 2	A-B C-D	Up to 22	32-bit	1	1
Type 3	A-B C-D	Up to 22	32-bit		3
Type 4	A-B C-D	Up to 32		1	1
Type 5	A-B C-D	Up to 32			3
Type 6	A-B C-D	Up to 24			1
Type 10	A-B	Up to 4			1

conga-MA5 modules use the Type 10 pinout definition. They are equipped with single 220-pin high performance connector that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 3.0, and Gigabit Ethernet. The Type 10 pinout provides the ability to offer PCI Express, Serial ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

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conga-MA5 Options Information

The conga-MA5 is available in five commercial and three industrial variants. The tables below show the different configurations available. Check the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Table 2 conga-MA5 Commercial Variants

Part-No.	048000	048001	048002	048020	048022
Processor	Intel® Atom® x7-E3950 Quad Core 1.6 GHz Burst 2.0 GHz	Intel® Atom® x5-E3940 Quad Core 1.6 GHz Burst 1.8 GHz	Intel® Atom® x5-E3930 Dual Core 1.3 GHz Burst 1.8 GHz	Intel® Pentium® N4200 Quad Core 1.1 GHz Burst 2.5 GHz	Intel® Celeron® N3350 Dual Core 1.1GHz Burst 2.4 GHz
L2 Cache	2 MB	2 MB	2 MB	2 MB	2 MB
Onboard Memory	8 GB 1866 MT/s DDR3L	4 GB 1866 MT/s DDR3L	2 GB 1866 MT/s DDR3L	8 GB 1866 MT/s DDR3L	4 GB 1866 MT/s DDR3L
Graphics	Intel® HD Graphics 505	Intel® HD Graphics 500	Intel® HD Graphics 500	Intel® HD Graphics 505	Intel® HD Graphics 500
GFX Base/Burst Freq.	500/650 Mhz	400/600 MHz	400/550 MHz	200/750 MHz	200/650 MHz
LVDS/eDP	Single Channel LVDS 18/24 bpp	Single Channel LVDS 18/24 bpp	Single Channel LVDS 18/24 bpp	Single Channel LVDS 18/24 bpp	Single Channel LVDS 18/24 bpp
DDI	DP++	DP++	DP++	DP++	DP++
eMMC	Onboard 32 GB MLC	Onboard 16 GB MLC	Onboard 16 GB MLC	Onboard 32 GB MLC	Onboard 16 GB MLC
Ethernet Controller	Intel® I210	Intel® I210	Intel® I210	Intel® I210	Intel® I210
SOC TDP	12 W	9.5 W	6.5 W	6 W	6 W

Table 3 conga-MA5 Industrial Variants

Part-No.	048010	048011	048012
Processor	Intel® Atom® x7-E3950 Quad Core 1.6 GHz Burst 2.0 GHz	Intel® Atom® x5-E3940 Quad Core 1.6 GHz Burst 1.8 GHz	Intel® Atom® x5-E3930 Dual Core 1.3 GHz Burst 1.8 GHz
L2 Cache	2 MB	2 MB	2 MB
Onboard Memory	8 GB 1866 MT/s DDR3L	4 GB 1866 MT/s DDR3L	4 GB 1866 MT/s DDR3L
Graphics	Intel® HD Graphics 505	Intel® HD Graphics 500	Intel® HD Graphics 500
GFX Base / Burst	500/650 MHz	400/600 MHz	400/550 MHz
LVDS / eDP	Single Channel LVDS 18/24 bpp	Single Channel LVDS 18/24 bpp	Single Channel LVDS 18/24 bpp
DDI	DP++	DP++	DP++
eMMC (SLC / MLC)	Onboard 16 GB MLC	Onboard 16 GB MLC	Onboard 16 GB MLC
Ethernet Controller	Intel® I210	Intel® I210	Intel® I210
SOC TDP	12 W	9.5 W	6.5 W

Note

Disable Burst mode for industrial use conditions.

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2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 10 Rev. 2.1 (mini size 84 mm x 55 mm)	
Processor	Intel® Atom®, Pentium® and Celeron® (Codename: Apollo Lake)	
Memory	conga-MA5: Up to 8 GB non-ECC DDR3L onboard memory interface with data rates up to 1866 MT/s.	
Chipset	Integrated in SoC	
Onboard Storage	eMMC 5.0 interface up to 128 GB	
Audio	Intel® High Definition Audio (Intel® HD Audio)	
Ethernet	Onboard Intel® Ethernet Controller I210 connected to SOC PCIe port 4 - connected via one PCI Express® x1 link by default	
Graphics Options	Intel® HD Graphics Gen9-LP supporting DirectX12, OpenGL 4.3, OpenGL ES 3.0, OpenCL 1.2, full HW acceleration for HEVC (H2.65), H2.64, MVC, VP8, VP9, MPEG2, VC-1, WMV9 and JPEG/MJPEG. Dual simultaneous display support.	
	1x DDI1 with support for the following via eDP to LVDS bridge IC: - Single-channel LVDS interface: 1x 18 bpp or 1x 24 bpp. - VESA LVDS color mappings - Automatic Panel Detection via Embedded Panel Interface based on VESA EDID™ 1.3. - Resolution up to 1280x1024 @ 60 Hz in single channel LVDS mode. Optional eDP interface (assembly option) **NOTE:** Either eDP or LVDS signals supported, not both signal types simultaneously.	1x DDI0 with support for DP++ **NOTE**: The conga-MA5 does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.
Peripheral Interfaces	2x SATA 6 Gb/s Up to 4x PCI Express® Gen2 x1 links without LAN (requires custom BIOS) 6x USB 2.0 and 2x USB 3.0/2.0 SD (MMC not supported) 2x UART (LPC to Dual-UART as assembly option)	GPIOs muxed with SD card (not both types simultaneously) SPI Bus (For external BIOS FLASH only) LPC Bus I²C Bus, multimaster SMBus
BIOS	AMI Aptio® UEFI 5.x firmware; 8 MByte serial SPI with congatec Embedded BIOS features (OEM Logo, OEM CMOS Defaults, LCD Control, Display Auto Detection, Backlight Control, Flash Update)	
Power Mgmt.	ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).	
congatec Board Controller	Multi Stage Watchdog, non-volatile User Data Storage, Manufacturing and Board Information, Board Statistics, BIOS Setup Data Backup, I²C bus (fast mode, 400 kHz, multi-master), Power Loss Control	
Security	Integrated Intel® PTT (TPM 2.0). Infineon SLB9665 (LPC TPM 2.0) or SLB9660 (LPC TPM 1.2) available by assembly option.	

Note

Some of the features mentioned in the above Feature Summary are optional and require customized articles. Check the part number of your module and compare it to the options information list on page 14 to determine what options are available on your particular module. For more information, contact congatec support.

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2.2 Supported Operating Systems

The conga-MA5 supports the following operating systems

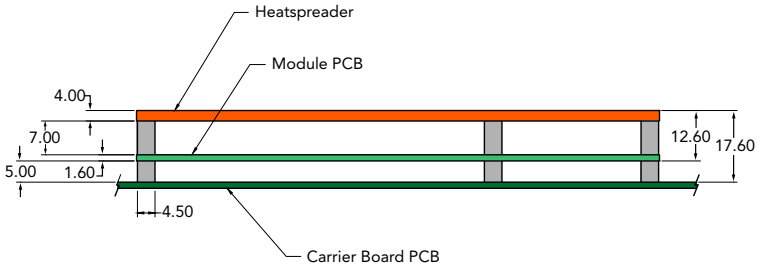
- Microsoft® Windows® 10 Enterprise (64-bit)
- Microsoft® Windows® 10 IoT Core (64-bit)
- Linux 3.x/4.x
- Yocto 2.x

Note

For the installation of Microsoft® Windows® 10 (64-bit), congatec recommends a minimum storage capacity of 20 GB. congatec will not offer technical support for systems with less than 20 GB storage space.

2.3 Mechanical Dimensions

- 84.0mm x 55.0mm
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm.



Note

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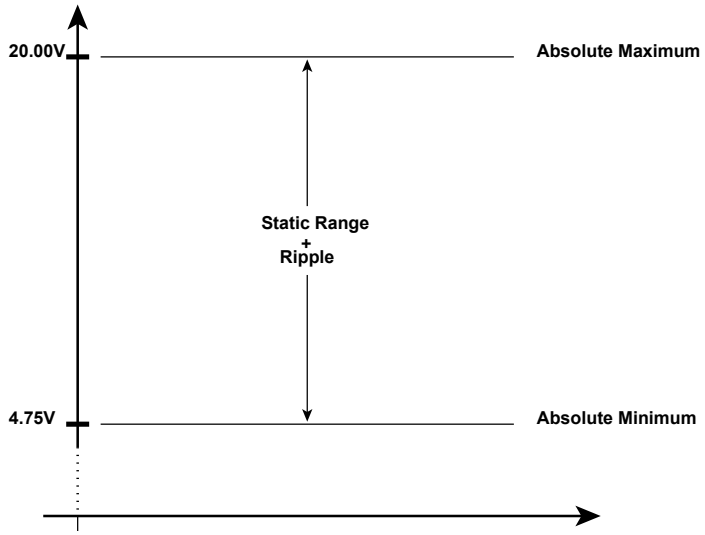
2.4 Supply Voltage Standard Power

- 4.75V - 20V (Wide input range)



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 10 (single connector, 220 pins).

Table 5 Power Limits on Type 10 Connector

Power Rail	Module Pin Current Capability (A)	Nominal Input (V)	Input Range (V)	Derated Input (V)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (W)	Assumed Conversion Efficiency	Max. Load Power (W)
Wide Input	6		4.75-20.0	4.75	+/- 100	28	85%	23.8
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.5-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 95% of nominal within 0.1 ms to 20 ms (0.1 ms ≤ Rise Time ≤ 20 ms). Each DC input voltage must rise from 10% to 90% of its nominal voltage in a smooth, continuous ramp and the slope of the turn-on waveform must be positive.

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2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-MA5 COM
- modified congatec carrier board
- conga-MA5 cooling solution
- Microsoft Windows® 10 (64-bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool.

Table 6 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle.	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency.
S0: Peak value	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.
S3	COM is powered by VCC_5V_SBY.	
S5	COM is powered by VCC_5V_SBY.	

Note

1. *The fan and SATA drives were powered externally.*

2. *All other peripherals except the LCD monitor were disconnected before measurement.*

The tables below provide additional information about the power consumption data for each of the conga-MA5 variants offered. The values are recorded at various operating modes.

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Table 7 Power Consumption Values

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64-bit)	CPU			Current (Amp.) at 12V (S0) or 5V (S3, S5)				
					Variant	Cores	Base / Burst Freq. (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5
048000	8 GB	A.1	M50R019	Windows® 10	Intel® Atom® x7-E3950	4	1.6/2.0	0.14	1.71	1.87	0.10	0.10
048001	4 GB	A.1	M50R019	Windows® 10	Intel® Atom® x5-E3940	4	1.6/1.8	0.12	1.23	1.33	0.11	0.09
048002	2 GB	A.1	M50R019	Windows® 10	Intel® Atom® x5-E3930	2	1.3/1.8	0.12	0.88	0.94	0.12	0.10
048020	8 GB	A.1	M50R019	Windows® 10	Intel® Pentium® N4200	4	1.1/2.5	0.14	1.02	1.95	0.11	0.10
048022	4 GB	A.1	M50R019	Windows® 10	Intel® Celeron® N3350	2	1.1/2.4	0.12	0.91	1.64	0.10	0.09
048010	8 GB	A.1	M50R019	Windows® 10	Intel® Atom® x7-E3950	4	1.6/2.0	0.14	1.71	1.87	0.10	0.10
048011	4 GB	A.1	M50R019	Windows® 10	Intel® Atom® x5-E3940	4	1.6/1.8	0.12	1.23	1.33	0.11	0.09
048012	4 GB	A.1	M50R019	Windows® 10	Intel® Atom® x5-E3930	2	1.3/1.8	0.12	0.88	0.94	0.12	0.10

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 8 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	1.90 µA
20°C	3V DC	2.31 µA
70°C	3V DC	5.46 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider also the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-MA5.*

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2.7 Environmental Specifications

Temperature (commercial variants)	Operation:	0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation:	-40° to 85°C	Storage: -40° to +85°C
Relative Humidity	Operation:	10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heat spreader, the maximum operating temperature refers to any measurable spot on the heat spreader's surface.

Humidity specifications are for non-condensing conditions.

2.8 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

2.8.1 Module

For long-term storage of the conga-MA5 (more than six months), keep the conga-MA5 in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

Note

We do not recommend storing the conga-MA5 for more than five years under these conditions.

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2.8.2 Cooling Solution

The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. For optimal cooling performance, do not store the heatspreaders/cooling solutions at temperatures below -20°C.

Caution

1. *For temperatures between -10°C and -20°C, preheat the heatpipes before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your local sales representative.*

2. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

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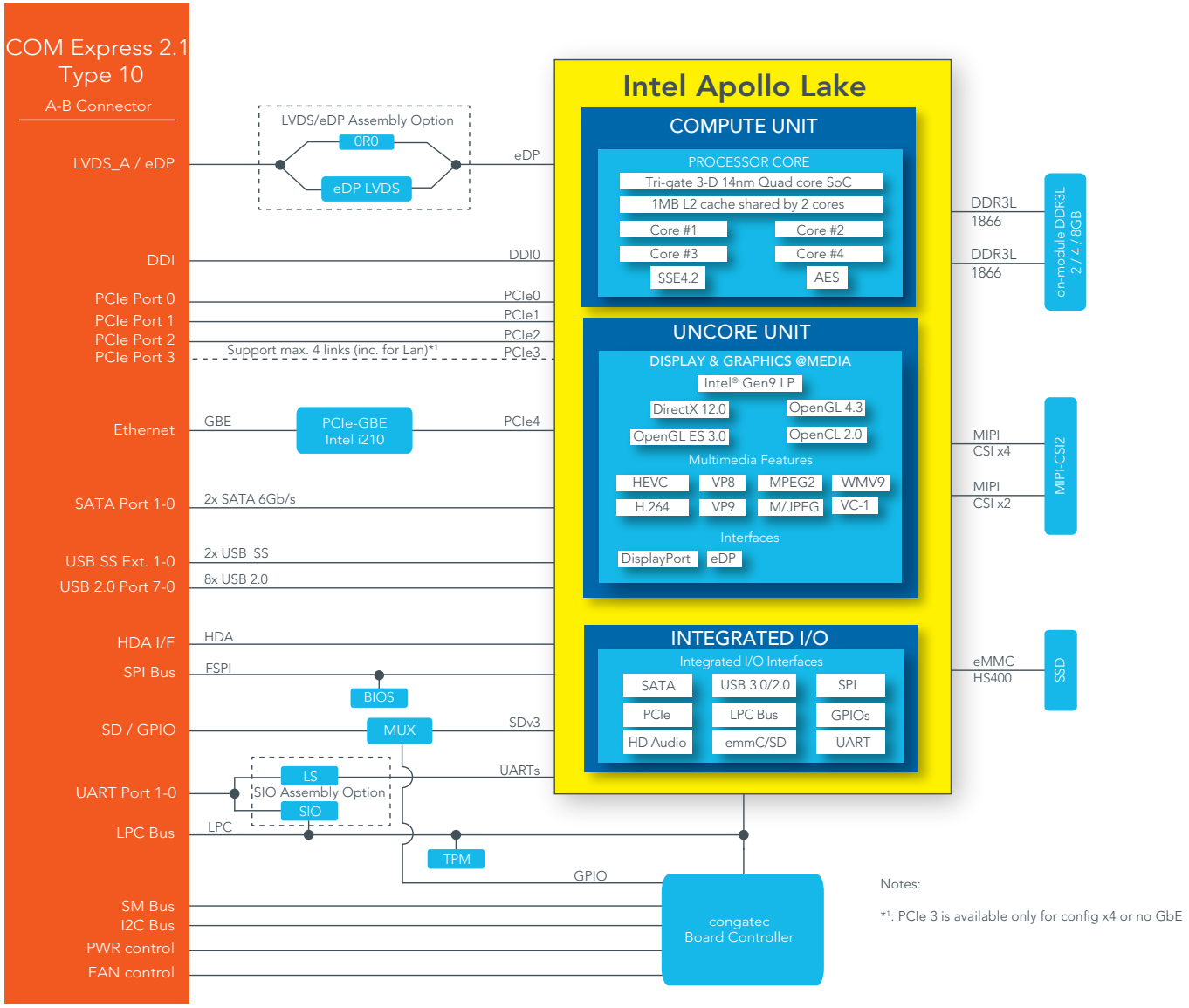
3 Block Diagram



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4 Cooling Solutions

congatec GmbH offers the cooling solutions listed in Table 9 for conga-MA5. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

Cooling Solution	Part No	Description
HSP	048057	Heatspreader for conga-MA5 with open silicon Intel Pentium and Celeron processor. All standoffs are with 2.7mm bore hole
	048056	Heatspreader for conga-MA5 with open silicon Intel Pentium and Celeron processor. All standoffs are M2.5mm thread.
	048053	Heatspreader for conga-MA5 with lidded Intel Atom processor. All standoffs are with 2.7mm bore hole.
	048052	Heatspreader for conga-MA5 with lidded Intel Atom processor. All standoffs are M2.5mm thread.
CSP	048055	Passive cooling solution for conga-MA5 with open silicon Intel Pentium and Celeron processor. All standoffs are with 2.7mm bore hole.
	048054	Passive cooling solution for conga-MA5 with open silicon Intel Pentium and Celeron processor. All standoffs are M2.5mm thread.
	048051	Passive cooling solution for conga-MA5 with lidded Intel Atom processor. All standoffs are with 2.7mm bore hole.
	048050	Passive cooling solution for conga-MA5 with lidded Intel Atom processor. All standoffs are M2.5mm thread.

Caution

1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws.*
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*
3. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

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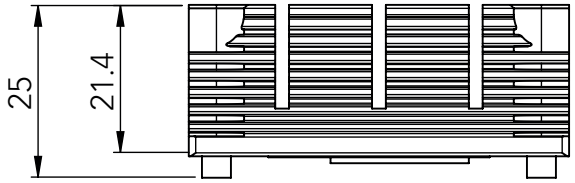
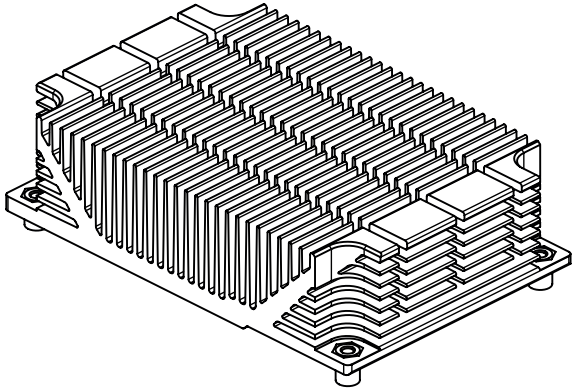
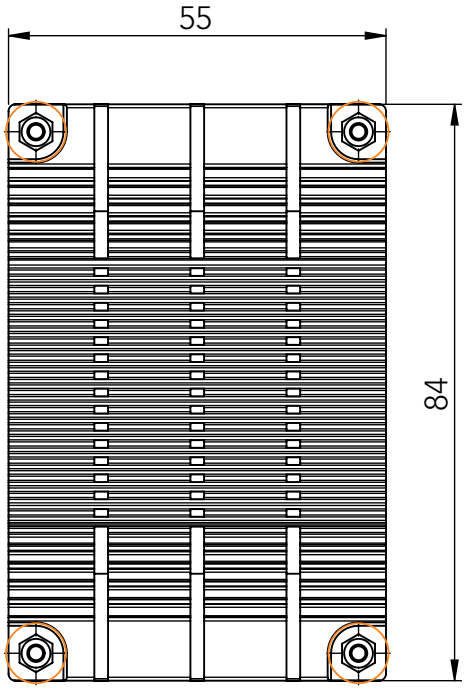
4.1 CSP Dimensions

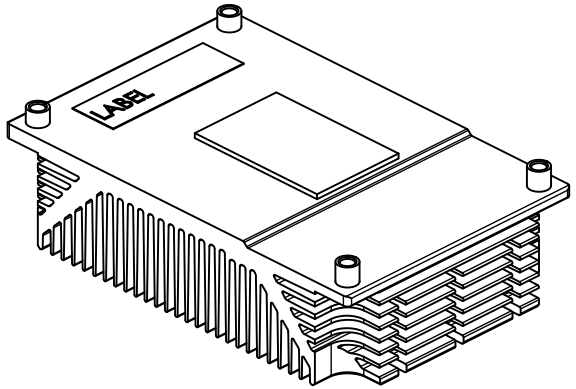
For Lidded Variants





M2.5 x 6 mm threaded standoff for threaded version
or
ø2.7 x 6 mm non-threaded standoff for borehole version





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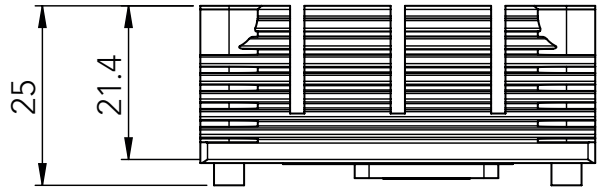
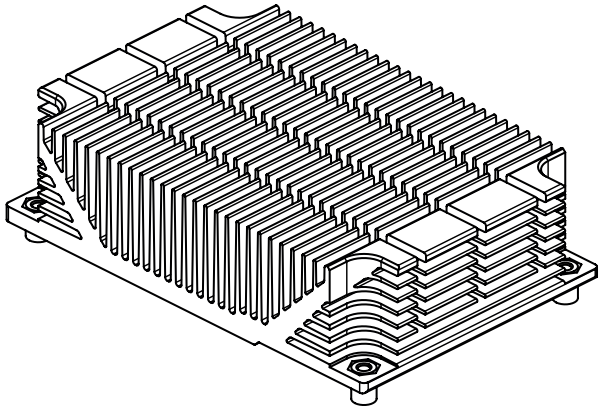
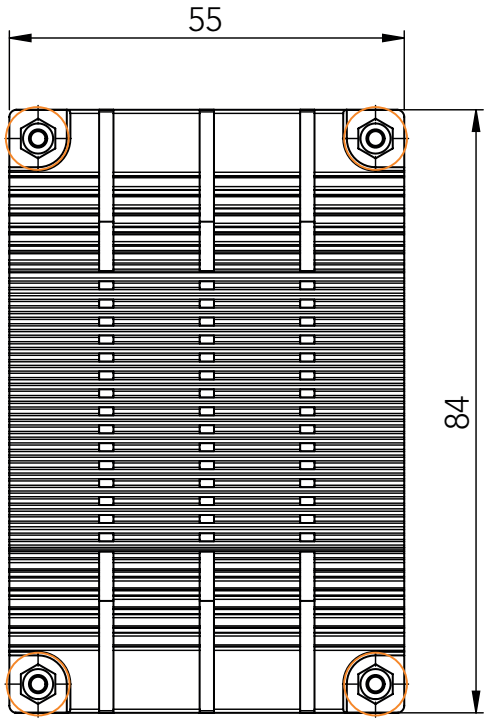
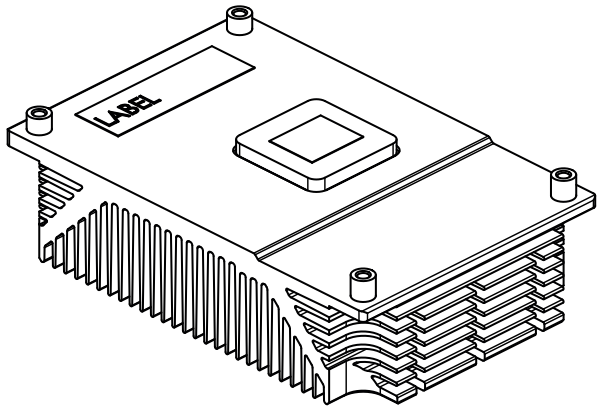
For Bare-die Variants





M2.5 x 6 mm threaded standoff for threaded version
or
ø2.7 x 6 mm non-threaded standoff for borehole version





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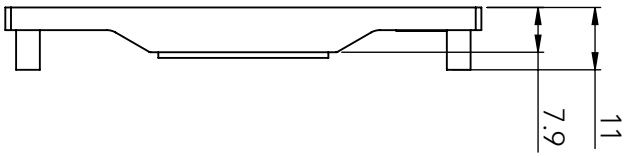
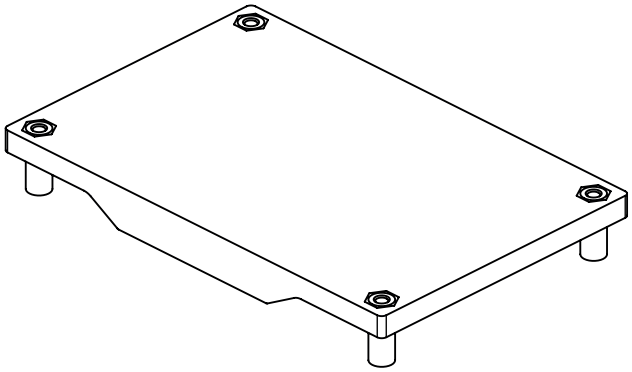
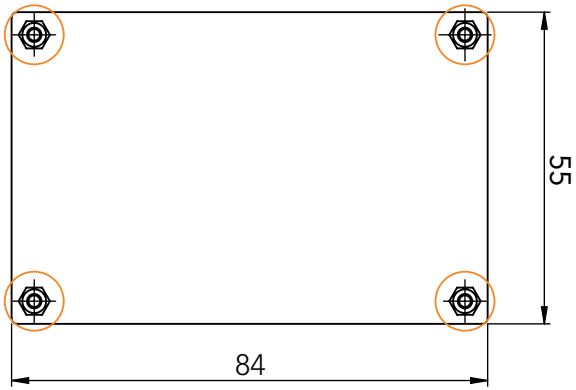
4.2 Heatpsreader Dimensions

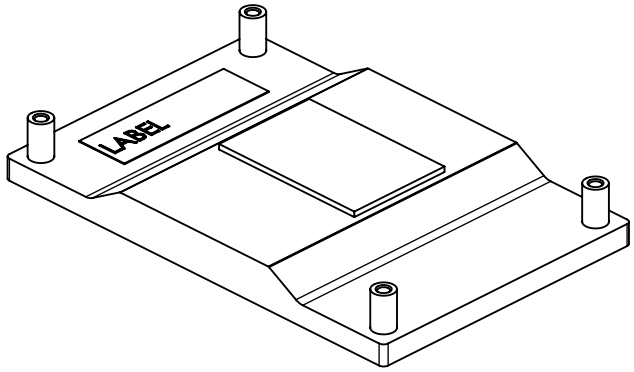
For Lidded Variants





M2.5 x 6 mm threaded standoff for threaded version
or
ø2.7 x 6 mm non-threaded standoff for borehole version





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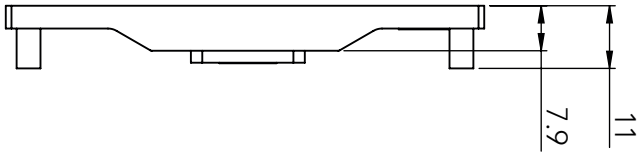
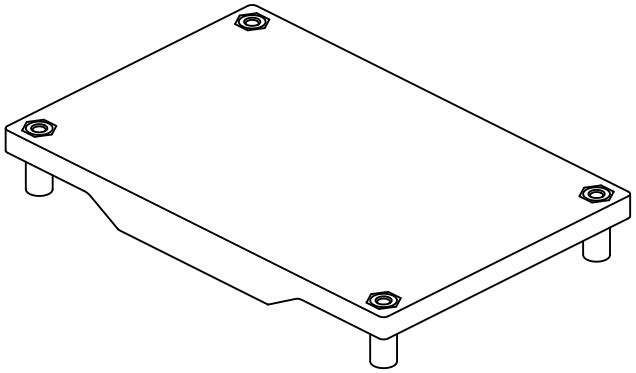
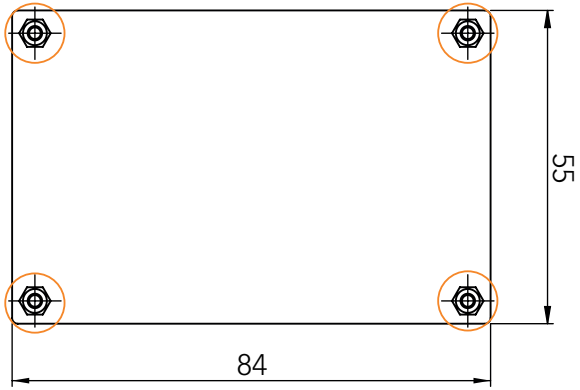
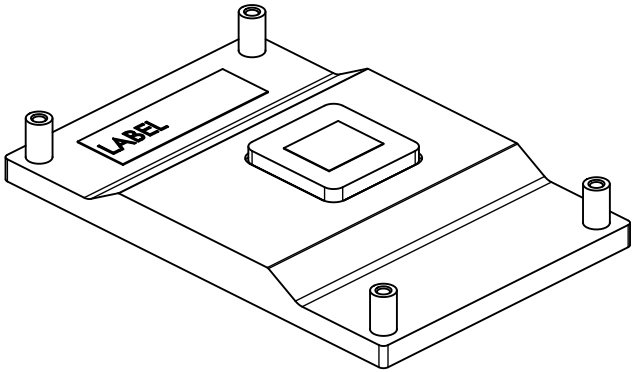
For Bare-die Variants





M2.5 x 6 mm threaded standoff for threaded version
or
ø2.7 x 6 mm non-threaded standoff for borehole version





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5 Connector Subsystems Rows A, B

The conga-MA5 is connected to the carrier board via a 220-pin connector (COM Express Type 10 pinout). This connector is broken down into two rows (rows A and B). The following subsystems can be found on conga-MA5 COM Express connector rows A and B.

5.1 PCI Express™

The conga-MA5 offers up to four PCIe lanes externally on the COM Express connector. The lanes are Gen 2 compliant and offer support for full 5 Gb/s bandwidth in each direction per x1 link. Default configuration for the lanes is 3 x1 link. Other configurations are possible as shown in the table below but require a customized BIOS firmware. Contact congatec technical support for more information.

The PCI Express interface is based on the PCI Express Specification 2.0 with Gen 1 (2.5 Gb/s) and Gen 2 (5 Gb/s) speed. For more information, refer to the conga-MA5 pinout table in section 8 “Signal Descriptions and Pinout Tables” and table 16 "PCI Express Signal Descriptions".

Table 10 PCI Express™ Options

	x1	x2	x4	Gigabit Ethernet
Default	3			Yes
Option 1		2		Yes
Option 2			1	Yes
Option 3	2	1		Yes
Option 4	4			No

Note

The options require a customized BIOS.

5.2 Gigabit Ethernet

The conga-MA5 offers a Gigabit Ethernet interface on the COM Express connector via the onboard Intel® I210 Gigabit Ethernet controller. This controller is connected to the Intel® Apollo Lake SoC through a PCI Express lane.

The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

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5.3 SATA

The conga-MA5 offers two SATA interfaces on the COM Express connector via a SATA host controller integrated in the Intel® Apollo Lake SoC. The controller supports independent DMA operation, AHCI operations and data transfer rates of 1.5 Gb/s, 3.0 Gb/s and 6.0 Gb/s. IDE Mode is not supported.

5.4 Universal Serial Bus

The conga-MA5 offers up to eight USB ports (6x USB 2.0 and 2x USB 3.0/2.0) routed directly from the SoC. One USB 2.0 port (USB7) supports Dual Role.

5.4.1 USB 2.0

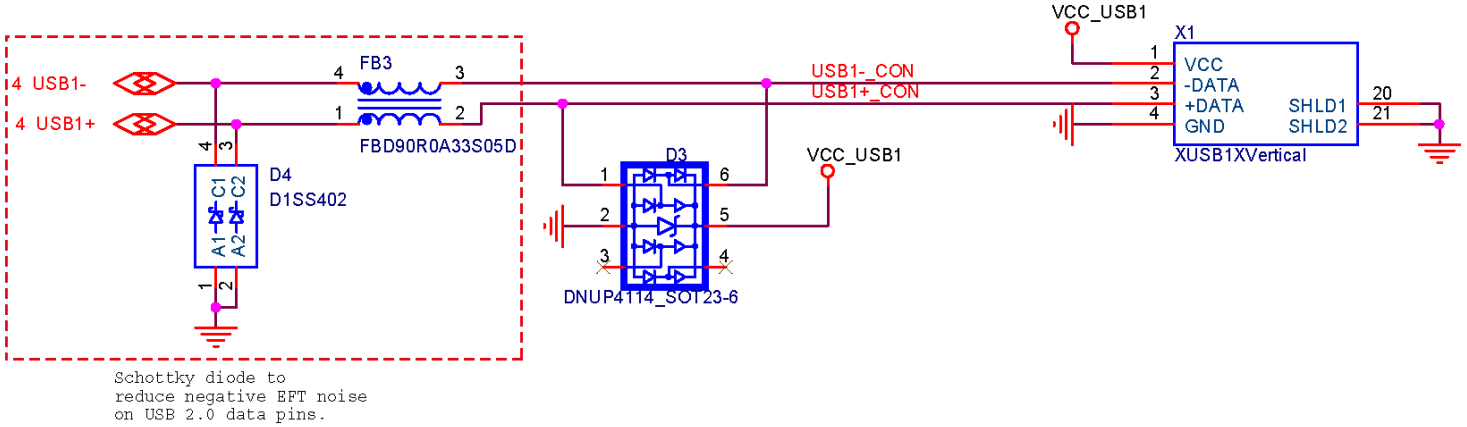
The conga-MA5 offers six USB 2.0 interfaces on the COM Express connector including one USB 2.0 Dual Role port. The xHCI host controller in the SoC complies with USB standard 1.1 and 2.0 with high-speed, full-speed and low-speed USB signalling.

Note

USB Dual Role is only supported under Linux. The port is a standard USB Host port under Windows.

Caution

To pass the Electrical Fast Transient (EFT) test, you must add a schottky diode (1SS402 or equivalent) to all USB2.0 data lanes routed to a connector on your carrier board. The schottky diode must be placed before the common-mode choke as shown below.



5.4.2 USB 3.0

The conga-MA5 offers two USB 3.0 ports on the COM Express connector. Both USB 3.0 ports are controlled by a xHCI host controller in the SoC. The xHCI host controller allows data transfers of up to 5 Gb/s and supports SuperSpeed, high-speed, full-speed and low-speed USB signalling.

5.5 ExpressCard™

The conga-MA5 supports the implementation of ExpressCards, which requires the dedication of one USB port and a x1 PCI Express link for each ExpressCard used.

5.6 High Definition Audio (HDA) Interface

The conga-MA5 provides an interface to connect an HDA audio codec. Only one external HDA codec is supported.

5.7 Digital Display Interface

The conga-MA5 offers two Digital Display Interfaces (DDI0 & DDI1) on the COM Express connector:

- DDI0 supports DisplayPort 1.2
- DDI1 supports LVDS by default

Optionally, DDI1 can support eDP instead (assembly option).

The supported display combinations are shown below:

Table 11 Display Combination

Display 1	Display 2	Display 1 Max. Resolution	Display 2 Max. Resolution
DDI0 (DP++)	DDI1 (LVDS/eDP)	4096x2160 @60 Hz (DP)	1280x1024 @60 Hz (single channel LVDS) 3840x2160 @60 Hz (stuffing optional eDP)
DDI1 (LVDS/eDP)	DDI0 (DP++)	1280x1024 @60 Hz (single channel LVDS) 3840x2160 @60 Hz (stuffing optional eDP)	4096x2160 @60 Hz (DP)

Note

To support the maximum resolution of the DP++, a retimer needs to be implemented on the carrier board.

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5.7.1 DisplayPort (DP)

DisplayPort is an open, industry standard digital display interface, that has been developed within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

5.7.2 LVDS

The conga-MA5 offers a single channel LVDS interface on the COM Express connector. The interface is provided by routing the onboard PTN3460 eDP to the eDP port of the SoC. The bridge processes the incoming DisplayPort stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format. The LVDS interface supports:

- single channel LVDS interface (color depths of 18 bpp or 24 bpp)
- integrated flat panel interface with clock frequency up to 112 MHz
- VESA standard or JEIDA data mapping
- automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3
- resolution up to 1280x1024 @60Hz

The LVDS interface provides LVDS signals by default, but can optionally support eDP 1.3 signals at 3840x2160 @60Hz (assembly option). For more information, contact congatec technical support.

Note

The LVDS/eDP interface supports either LVDS or eDP signals. Both signals are not supported simultaneously. See Table 11 for possible display combinations.

5.8 SD Card

The conga-MA5 offers a 4-bit SD interface connected to the SD v3.01 host controller integrated in the SoC. It supports up to 50 MHz 3.3V signalling. The MMC standard is not supported.

Note

The conga-MA5 supports only default bus speed modes and high bus speed modes (3.3 V). Faster bus speed modes are not supported (1.8V).

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5.9 General Purpose Serial Interface (UART)

The conga-MA5 offers two UART ports routed from the SoC by default. Optionally, the UART ports can be routed from an LPC controller (Exar XR28V382) instead. See *Table 25* for the signal description.

Note

The UART ports routed from the SoC cannot be used under Windows because Intel® does not provide the necessary driver. The UART ports routed from the SoC can only be used under Linux.

The UART ports routed from the LPC controller (Exar XR28V382) can also be used under Windows 10 without a special driver.

5.10 LPC Bus

The conga-MA5 offers the LPC (Low Pin Count) bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals and functionality. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific carrier board using this bus. Only certain devices such as Super I/O or TPM chips can be implemented on the carrier board.

Note

The LPC clock frequency is 25 MHz. The LPC_DRQ# signal is not supported. The SERIRQ# signal is programmable to operate with the cBC.

5.11 SPI Bus

The module integrates a 8 MByte SPI Flash device with SFDP feature for the UEFI BIOS. Optionally, the onboard SPI Flash can be disabled and a carrier board based 3V 8 MByte SPI Flash device with SFDP feature (e.g. W25Q64FVSSIG) can be utilized to boot the module. The SPI clock speed is 25 MHz.

5.12 I²C Bus

The I²C bus is implemented through the congatec board controller. The bus has 2.2k ohm pull-ups resistors on the CLK and DATA signals and is powered from standby 3.3V.

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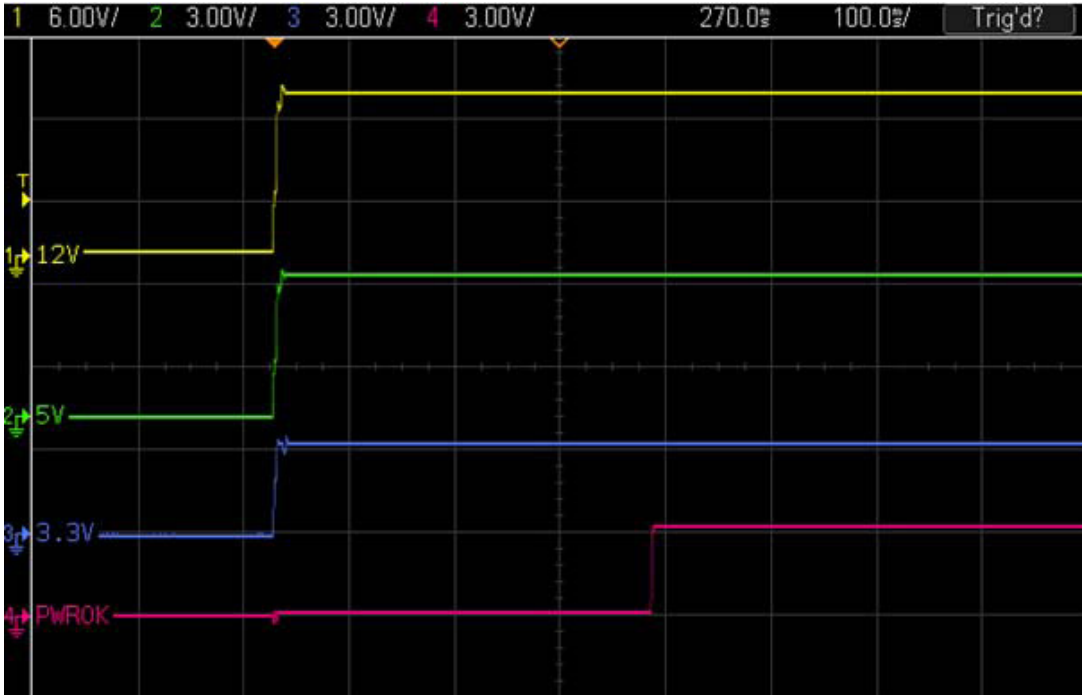
5.13 SMBus

The SM Bus is implemented through the congatec board controller. It is an I²C bus variant for system management functions. The bus is powered from standby 3.3V and has 2.2k ohm pull-ups resistors on the CLK and DATA signals. ALERT# signal has a 10K-ohm pull-up resistor. Optionally, this SM Bus can be connected to the SoC SMBus via an isolation switch controlled in BIOS.

5.14 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. See screenshot below.



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.
It is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

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The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the “power good” signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, you must make sure that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-MA5 provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-MA5's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the COM Express connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the COM Express connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

Input power of 4.75 - 20 volt is the sole operational power source for the conga-MA5. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-MA5 application:

- It has also been noticed that on some occasions, problems occur when using a power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information, see the “Power Supply Design Guide for Desktop Platform Form Factors” document at www.intel.com.

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Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush current on the conga-MA5 VCC_5V_SB power rail can go up as high as 3.58 A and as high as 11.5 A on VCC power rail (12 V) within a short time (approx. 150µs) and with a voltage rise time of 100µs. Sufficient decoupling capacitance must be implemented on the carrier board to ensure proper power-up sequencing.

5.15 Power Management

ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).

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5.16 MIPI CSI-2

The MIPI CSI-2 connector is available as an option for high-volume projects. It requires a specific software implementation—depending on the operating system and camera application. Contact your local sales representative for further details.

The flip-lock actuator of the MIPI CSI-2 connector is fragile and must be handled with care.

Follow these steps to attach the flat-foil cable to the MIPI CSI-2 connector:

1. Remove the cooling solution (if installed).
2. Gently press against both sides of the actuator from below to flip the actuator open.
3. Fully slide the flat-foil cable inside the slot below the actuator. The exposed conductive traces of the flat-foil cable must face up.
4. Gently press against both sides of the actuator from above until the actuator is firmly locked.
5. Install the cooling solution.

Follow these steps to remove the flat-foil cable from the MIPI CSI-2 connector:

1. Remove the cooling solution (if installed).
2. Gently press against both sides of the actuator from below to flip the actuator open.
3. Carefully remove the flat-foil cable.
4. Install the cooling solution.

Caution

Do not try to pull the flat-foil connector out without removing the cooling solution and opening the actuator first. Also, do not use pressure to open the actuator by more than 45°. Otherwise, the connector will be damaged.

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6 Additional Features

6.1 Onboard Interfaces

6.1.1 eMMC 5.0

Optionally, the conga-MA5 offers an onboard eMMC 5.0 flash (MLC) with up to 128 GB storage capacity and an eMMC 5.0 compliant controller. Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology. The performance of the newer eMMC may vary depending on the eMMC technology.

Note

For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions.

6.2 congatec Board Controller (cBC)

The conga-MA5 is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRBI microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

6.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.2.2 Fan Control

The conga-MA5 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express Design Guide.

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6.2.3 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The term "power loss" implies that all power sources, including the standby power are lost (G3 state). Once power loss or shutdown occurs (transition to G3), the board controller continuously monitors the standby power rail. If the standby voltage is no longer detected within 30 seconds, the module considers this as an AC power loss condition. If stable standby voltage is detected within 30 seconds, the cBC assumes that the system was switched off properly.

The power loss control feature has three different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to "ON".*

2. *The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.*

6.2.4 Watchdog

The conga-MA5 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the watchdog; therefore, the conga-MA5 does not support external hardware triggering. For more information about the Watchdog feature, refer to the application note AN3_Watchdog.pdf at www.congatec.com.

6.2.5 General Purpose Input/Output

The conga-MA5 offers general purpose inputs and outputs for custom system designs. These GPIOs are multiplexed with SD signals and are controlled by the cBC.

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6.3 OEM BIOS Customization

The conga-MA5 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support. The customization features supported are described below:

6.3.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.3.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.3.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

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6.3.4 OEM BIOS Code/Data

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader. Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table (OA2.0), Windows 8 OEM activation (OA3.0), verb tables for HDA codecs, PCI/PCIe opROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.3.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec has defined an interface for the exchange of data between a x86 CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addition to the ACPI-compliant Control Method Battery mentioned above, the latest versions of the conga-MA7 BIOS and board controller firmware also support the LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface contact your local congatec sales representative.

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6.5 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website.

6.6 Suspend to Ram

The Suspend to RAM feature is available on the conga-MA5.

6.7 Security Features

The conga-MA5 has an integrated Intel® PTT (TPM 2.0). Additionally, an Infineon SLB9665 (LPC TPM 2.0) or SLB9660 (LPC TPM 1.2) is available by assembly option.

Note

You can enable/disable the integrated Intel® PTT (TPM 2.0) in BIOS Setup: Enter BIOS Setup (see section 10.1 "Navigating the BIOS Setup Menu"), navigate to "Advanced Setup" and then "Platform Trust Technology". Always disable fTPM if you use an external TPM.

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7 conga Tech Notes

The conga-MA5 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help the user to better understand the information found in the system resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Description section.

7.1 Intel® Apollo Lake Features

7.1.1 Processor Core

Some of the features supported by the Intel® Apollo Lake SoC are:

- Quad/Dual Core Processor
  - 2 modules of 2 cores each (for Quad Core Processor)
  - Supporting Out of Order Execution (OOE)
  - Enhanced Intel SpeedStep® Technology
  - Intel® 64 bit Architecture
- Intel® full virtualization architecture supports
  - Intel® VT-x with Extended Page Tables (EPT)
  - Intel® Virtualization Technology for Directed I/O (VT-d)
- Thermal management support via Intel® Thermal Monitor (TM1 and TM2)

Note

Intel® Hyper-Threading technology is not supported (four cores execute four threads)

7.1.1.1 Intel Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel® VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture Intel® VT-x added hardware support in the processor to improve the virtualization performance and robustness.

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Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

7.1.1.2 AHCI

The Apollo Lake SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

7.1.1.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-MA5 ACPI thermal solution offers two different cooling policies:

- Passive Cooling

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- Critical Trip Point

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points. If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

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7.2 ACPI Suspend Modes and Resume Events

conga-MA5 supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 10.4.8 “ACPI Configuration Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Windows® 10 and Linux

This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

Table 12 Wake Events resuming system from S3

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check ‘Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

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8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type 10 connectors used for congatec GmbH modules. The pinout of the modules complies with COM Express Type 10 Rev. 2.1.

The table below describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 13 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V
I/O 5V	Bi-directional signal 5V
I 3.3V	Input 3.3V
I 5V	Input 5V
I/O 3.3VSB	Input 3.3V active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output pin
P	Power input pin
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

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8.1 COM Express Connector Pinout

Table 14 COM Express Connector Pinouts

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND(FIXED)	B1	GND(FIXED)	A56	RSVD	B56	RSVD
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND(FIXED)	B60	GND(FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0# (*)	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# (*)	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND(FIXED)	B11	GND(FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND(FIXED)	B70	GND(FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	eDP_TX2+/LVDS_A0+	B71	DDI0_PAIR0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	eDP_TX2-/LVDS_A0-	B72	DDI0_PAIR0-
A18	SUS_S4#	B18	SUS_STAT#	A73	eDP_TX1+/LVDS_A1+	B73	DDI0_PAIR1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	eDP_TX1-/LVDS_A1-	B74	DDI0_PAIR1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	eDP_TX0+/LVDS_A2+	B75	DDI0_PAIR2+
A21	GND(FIXED)	B21	GND(FIXED)	A76	eDP_TX0-/LVDS_A2-	B76	DDI0_PAIR2-
A22	USB_SSRX0-	B22	USB_SSTX0-	A77	eDP/LVDS_VDD_EN	B77	DDI0_PAIR4+ (*)
A23	USB_SSRX0+	B23	USB_SSTX0+	A78	LVDS_A3+	B78	DDI0_PAIR4- (*)
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP/LVDS_BKLT_EN
A25	USB_SSRX1-	B25	USB_SSTX1-	A80	GND(FIXED)	B80	GND(FIXED)
A26	USB_SSRX1+	B26	USB_SSTX1+	A81	eDP_TX3+/LVDS_A_CK+	B81	DDI0_PAIR3+
A27	BATLOW#	B27	WDT	A82	eDP_TX3-/LVDS_A_CK-	B82	DDI0_PAIR3-
A28	(S)ATA_ACT#	B28	HDA_SDIN2 (*)	A83	eDP_AUX+/LVDS_I2C_CK	B83	eDP/LVDS_BKLT_CTRL
A29	HDA_SYNC	B29	HDA_SDIN1 (*)	A84	eDP_AUX-/LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	HDA_RST#	B30	HDA_SDIN0 (**)	A85	GPI3	B85	VCC_5V_SBY
A31	GND(FIXED)	B31	GND(FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	HDA_BITCLK	B32	SPKR	A87	eDP_HPD	B87	VCC_5V_SBY
A33	HDA_SDOUT	B33	I2C_CK	A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE_CLK_REF-	B89	DD0_HPD
A35	THRMTRIP#	B35	THRM#	A90	GND(FIXED)	B90	GND(FIXED)
A36	USB6-	B36	USB7	A91	SPI_POWER	B91	DDI0_PAIR5+ (*)
A37	USB6+	B37	USB7+	A92	SPI_MISO (**)	B92	DDI0_PAIR5- (*)

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Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	DDI0_PAIR6+ (*)
A39	USB4-	B39	USB5-	A94	SPI_CLK (**)	B94	DDI0_PAIR6- (*)
A40	USB4+	B40	USB5+	A95	SPI_MOSI (**)	B95	DDI0_DDC_AUX_SEL
A41	GND(FIXED)	B41	GND(FIXED)	A96	TPM_PP	B96	USB7_HOST_PRSNT
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS# (**)
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	DDI0_CTRLCLK_AUX+
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	DDI0_CTRLDATA_AUX-
A45	USB0-	B45	USB1-	A100	GND(FIXED)	B100	GND(FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND(FIXED)	B51	GND(FIXED)	A106	VCC_12V	B106	VCC_12V
A52	RSVD	B52	RSVD	A107	VCC_12V	B107	VCC_12V
A53	RSVD	B53	RSVD	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	RSVD	B55	RSVD	A110	GND(FIXED)	B110	GND(FIXED)

Note

The signals marked with asterisk (*) are not supported or connected on the conga-MA5.

On Intel Apollo Lake SoC, the signals marked with asterisks (**) have native voltage levels that are different from the levels defined in the COM Express Specification. To comply with the COM Express Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible. External pull up/down resistors <100k ohm are not allowed on these signals.

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8.2 COM Express Connector Signal Descriptions

Table 15 High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	High Definition Audio Reset: This signal is the master hardware reset to external codec(s).	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SYNC	A29	High Definition Audio Sync: This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_BCLK	A32	High Definition Audio Bit Clock Output: This signal is a 24.000 MHz serial data clock generated by the Intel® High Definition Audio controller.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SDOUT	A33	High Definition Audio Serial Data Out: This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SDIN[0] (**)	B30	High Definition Audio Serial Data In [0]: This signal is a serial TDM data input from the codec. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	I/O 3.3VSB	PD 47K	AC'97 codecs are not supported. HDA_SDIN[2:1] are not connected.

Note

On Intel Apollo Lake SoC, the signals marked with asterisks (**) have native voltage levels that are different from the levels defined in the COM Express Specification. To comply with the COM Express Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

Table 16 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10 Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		Twisted pair signals for external transformer.
			1000	100	10			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.				O 3.3VSB		indicates only LINK100 and LINK1000
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100 Mbit/sec link indicator, active low.				O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000 Mbit/sec link indicator, active low.				O 3.3VSB		

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Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.			Not connected

Table 17 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.1
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.1
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.1
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.1
S_ATA_ACT#	A28	Serial ATA activity indicator, active low.	O 3.3V		Up to 10mA

Table 18 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

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Table 19 ExpressCard Support Pins Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request	I 3.3VSB	PU 10k 3.3V	
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3VSB		

Table 20 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB Port 0 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+ USB1-	B46 B45	USB Port 1 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+ USB2-	A43 A42	USB Port 2 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+ USB3-	B43 B42	USB Port 3 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+ USB4-	A40 A39	USB Port 4 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+ USB5-	B40 B39	USB Port 5 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+ USB6-	A37 A36	USB Port 6 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+ USB7-	B37 B36	USB Port 7 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Supports Dual Role.
USB7_HOST_PRSNT	B96	Module USB client may detect the presence of a USB host on USB7. A high value indicates that a host is present.	I 3.3VSB	PD 1M0	
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

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Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSTX0+ USB_SSTX0-	B23 B22	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O USB-SS		
USB_SSTX1+ USB_SSTX1-	B26 B25	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O USB-SS		
USB_SSRX0+ USB_SSRX0-	A23 A22	Additional receive signal differential pairs for the SuperSpeed USB data path.	I USB-SS		
USB_SSRX1+ USB_SSRX1-	A26 A25	Additional receive signal differential pairs for the SuperSpeed USB data path.	I USB-SS		

Table 21 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ eDP_TX2+	A71	LVDS Channel A differential pair 0 Embedded Display Port channel 0 differential pair 2	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A0- eDP_TX2-	A72	LVDS Channel A differential pair 0 Embedded Display Port channel 0 differential pair 2	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A1+ eDP_TX1+	A73	LVDS Channel A differential pair 1 Embedded Display Port channel 0 differential pair 1	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A1- eDP_TX1-	A74	LVDS Channel A differential pair 1 Embedded Display Port channel 0 differential pair 1	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A2+ eDP_TX0+	A75	LVDS Channel A differential pair 2 Embedded Display Port channel 0 differential pair 0	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A2- eDP_TX0-	A76	LVDS Channel A differential pair 2 Embedded Display Port channel 0 differential pair 0	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A3+	A78	LVDS Channel A differential pair 3	O LVDS		
LVDS_A3-	A79	LVDS Channel A differential pair 3	O LVDS		
LVDS_A_CK+ eDP_TX3+	A81	LVDS Channel A differential clock Embedded Display Port channel 0 differential pair 3	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A_CK- eDP_TX3-	A82	LVDS Channel A differential clock Embedded Display Port channel 0 differential pair 3	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_VDD_EN eDP_VDD_EN	A77	Panel power enable	O 3.3V	PD 100k	LVDS (default) Assembly option: eDP
LVDS_BKLT_EN eDP_BKLT_EN	B79	Panel backlight enable	O 3.3V	PD 100k	LVDS (default) Assembly option: eDP
LVDS_BKLT_CTRL eDP_BKLT_CTRL	B83	Panel backlight brightness control	O 3.3V		LVDS (default) Assembly option: eDP
LVDS_I2C_CK eDP_AUX+	A83	DDC lines used for flat panel detection and control. Embedded Display Port AUX channel pair	I/O 3.3V I/O eDP	LVDS PU 2k2 3.3V	LVDS (default) Assembly option: eDP
LVDS_I2C_DAT eDP_AUX-	A84	DDC lines used for flat panel detection and control. Embedded Display Port AUX channel pair	I/O 3.3V I/O eDP	LVDS PU 2k2 3.3V	LVDS (default) Assembly option: eDP

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Table 22 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V	PU 20k	
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V	PU 20k	
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V		Not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/O OD 3.3V	PU 20k	
LPC_CLK	B10	LPC clock output	O 3.3V		25MHz

Table 23 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS# (**)	B97	Chip select for carrier board SPI.	O 3.3VSB	PU 100k	
SPI_MISO (**)	A92	Master Input Slave Output: SPI output data from carrier board SPI device to module.	I 3.3VSB		
SPI_MOSI (**)	A95	Master Output Slave Input: SPI output data from module to carrier board SPI.	O 3.3VSB	PD 100k	
SPI_CLK (**)	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB	PD 100k	
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	+ 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10k 3.3VSB	Carrier shall pull to GND or leave no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. Ground to select external SPI device. Pull high or leave no-connect to select on-module BIOS flash	I 3.3VSB	PU 10k 3.3VSB	Carrier shall pull to GND or leave no-connect

Note

On Intel Apollo Lake SoC, the signals marked with asterisks (**) have native voltage levels that are different from the levels defined in the COM Express Specification. To comply with the COM Express Specification, the signals are routed through bidirectional level shifters on the module. The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

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Table 24 DDI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI0_PAIR0+ DDI0_PAIR0-	B71 B72	Multiplexed with DP0_LANE0+ and TMDS0_DATA2+ Multiplexed with DP0_LANE0- and TMDS0_DATA2-	O DP		Only DP++ option, no SDVO
DDI0_PAIR1+ DDI0_PAIR1-	B73 B74	Multiplexed with DP0_LANE1+ and TMDS0_DATA1+ Multiplexed with DP0_LANE1- and TMDS0_DATA1-	O DP		Only DP++ option, no SDVO
DDI0_PAIR2+ DDI0_PAIR2-	B75 B76	Multiplexed with DP0_LANE2+ and TMDS0_DATA0+ Multiplexed with DP0_LANE2- and TMDS0_DATA0	O DP		Only DP++ option, no SDVO
DDI0_PAIR3+ DDI0_PAIR3-	B81 B82	Multiplexed with DP0_LANE3+ and TMDS0_CLK+ Multiplexed with DP0_LANE3- and TMDS0_CLK-	O DP		Only DP++ option, no SDVO
DDI0_HPD	B89	Detection of Hot Plug / Unplug and notification of the link layer Multiplexed with DP0_HPD and HDMI0_HPD	I 3.3V	PD 100k	
DDI0_CTRLCLK_AUX+	B98	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect.	I/O	PD 100k @ DP mode	
		TMDS I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O OD 3.3V	PU 5k 3.3V @ TMDS mode	
DDI0_CTRLDATA_AUX-	B99	DP AUX- function if DDI1_DDC_AUX_SEL is no connect.	I/O	PU 100k 3.3V @ DP mode	
		TMDS I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O OD 3.3V	PU 5k 3.3V @ TMDS mode	
DDI0_DDC_AUX_SEL	B95	Selects the function of DDI0_CTRLCLK_AUX+ and DDI0_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	

Note

The conga-MA5 does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.

Table 25 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O 3.3V	3.3V	12 volt tolerant
SER1_TX	A101	General purpose serial port transmitter	O 3.3V	3.3V	12 volt tolerant
SER0_RX	A99	General purpose serial port receiver	I 3.3V	PU 47K 3.3V	12 volt tolerant
SER1_RX	A102	General purpose serial port receiver	I 3.3V	PU 47K 3.3V	12 volt tolerant

Note

For the correct implementation, see the COM Express Design Guide.

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Table 26 I2C Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I2C port clock output	I/O OD 3.3VSB	PU 2.2K 3.3VSB	
I2C_DAT	B34	General purpose I2C port data I/O line	I/O OD 3.3VSB	PU 2.2K 3.3VSB	

Table 27 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PD 10K	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O 3.3V		12V tolerant
FAN_TACHIN	B102	Fan tachometer input.	I	PU 47K 3.3V	Requires a fan with a two pulse output. 12V tolerant.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high.	I 3.3V	PD 10K	

Note

For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express Design Guide.

Table 28 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a main power input (VIN) that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3VSB		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V	PU 10k	
SUS_STAT#	B18	Suspend Status: Indicates the system will enter a low power state soon. Used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3VSB		Same signal as SUS_S5#

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Signal	Pin #	Description	I/O	PU/PD	Comment
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		Same signal as SUS_S4#
WAKE0#	B66	PCI Express wake up request signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement a wake-up request from an external device.	I 3.3VSB	PU 10k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low.	I 3.3VSB	PU 10k 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 47k 3.3VSB	
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 47k 3.3VSB	

Table 29 Thermal Protection Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over temperature situation	I 3.3V	PU 10k 3.3V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown	O 3.3V		

Table 30 SM Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line	I/O OD 3.3VSB	PU 2k2 3.3VSB	
SMB_DAT	B14	System Management Bus bidirectional data line	I/O OD 3.3VSB	PU 2k2 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert - Active low input can be used to generate an SMI# (System Management Interrupt)	I 3.3VSB	PU 10k 3.3VSB	

Table 31 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3V	PU 10K 3.3V	

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Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3V		
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3V		
GPO2	B57	General purpose output pins. Shared with SD_WP. Output from COM Express, input to SD	O 3.3V		
GPO3	B63	General purpose output pins. Shared with SD_CD. Output from COM Express, input to SD	O 3.3V		

Table 32 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	B63	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. Maps to GPO3; used as an input when used for SD card support	I 3.3V	PU 20k	
SDIO_CLK	A93	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz. Maps to GPO0.	O 3.3V		
SDIO_CMD	B54	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Maps to GPO1	O 3.3V	PU 20k	
SDIO_WP	B57	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. Maps to GPO2; used as an input when used for SD card support	I 3.3V	PU 20k	
SDIO_DAT0	A54	SDIO Data line. Operates in push-pull mode and maps to GPI0	IO 3.3V	PU 20k	
SDIO_DAT1	A63	SDIO Data line. Operates in push-pull mode and maps to GPI1	IO 3.3V	PU 20k	
SDIO_DAT2	A67	SDIO Data line. Operates in push-pull mode and maps to GPI2	IO 3.3V	PU 20k	
SDIO_DAT3	A85	SDIO Data line. Operates in push-pull mode and maps to GPI3	IO 3.3V	PU 20k	

Table 33 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
TYPE10#	A97	Indicates to the carrier board that a Type 10 module is installed.	PDS	PD 47k	

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Table 34 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: 4.75V to 20V. All available VCC_12V pins on the connector(s) shall be used.	P		The conga-MA5 is a Type 10 mini module and as such supports a wide power supply range between 4.75 and 20V.
VCC_5V_SBY	B84-B87	Standby power input: +5V nominal. If VCC5V_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real time clock circuit-power input: +3V nominal	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110 B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

Table 35 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	A101	Controller Area Network TX output for CAN Bus channel 0. This pin is shared with SER1_TX	O 3.3V		Not supported
CAN0_RX	A102	Controller Area Network RX input for CAN Bus channel 0. This pin is shared with SER1_RX	I 3.3V		Not supported

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9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-MA5 module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed below.

Table 36 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000h - 00FFh	256 bytes	No	Motherboard resources
03B0h - 03CFh	32 bytes	No	Video system
400h - 47Fh	128 bytes	No	Motherboard resources
500h - 5FFh	256 bytes	No	Motherboard resources
680h - 69Fh	20 bytes	No	Motherboard resources
0CF8h - 0CFBh	4 bytes	No	PCI configuration address register
0CFCh - 0CFFh	4 bytes	No	PCI configuration data register
0D00h - F000h		See note	PCI / PCI Express bus

Note

The BIOS assigns PCI and PCI Express I/O resources from F000h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.1.1 LPC Bus

On the conga-MA5, the internal PCI Bus acts as the substractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Bus, not the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus. With the default settings in the congatec Embedded BIOS, the following I/O address ranges are sent to the LPC Bus:

80h - 8Fh via LPC Generic I/O Range 1
A00h - A1Fh via LPC Generic I/O Range 4

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The following I/O decode ranges are fixed to the LPC Bus:

2Eh - 2Fh
4Eh - 4Fh
200h - 20Fh
2F8h - 2FFh
3F8h - 3FFh
378h - 37Fh
778h - 77Fh
3F0h - 3F5h
3F7h, 60h, 62h, 64h, 66h

Parts of these ranges are not available if Super I/O is used on the carrier board. If Super I/O is not implemented on the carrier board, then all these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 37 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Device ID	Description and Device ID
00h	00h	00h	0x5AF0	Host Bridge
00h	02h	00h	0x5A84	Graphics and Display
00h	0Dh	00h	0x5A92	Primary to SideBand Bridge
00h	0Dh	01h	0x5A94	PMC (Power Management Controller)
00h	0Dh	02h	0x5A96	Fast SPI
00h	0Dh	03h	0x5AEC	Shared SRAM
00h	0Eh	00h	0x5A98	HDA
00h	0Fh	00h	0x5A9A	Simple Communication Controller 0
00h	0Fh	01h	0x5A9C	Simple Communication Controller 1
00h	0Fh	02h	0x5A9E	Simple Communication Controller 2
00h	012h	00h	0x5AE3	SATA
00h	013h	00h	0x5AD8	PCIe -A0
00h	013h	01h	0x5AD9	PCIe -A1 *1
00h	013h	02h	0x5ADA	PCIe -A2 *1
00h	013h	03h	0x5ADB	PCIe -A3 *1
00h	014h	00h	0x5AD6	PCIe -B0
00h	015h	00h	0x5AA8	USB-Host (xHCI)
00h	015h	01h	0x5AAA	USB-Host (xDCI)

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00h	016h	00h	0x5AAC	I2C 0 *2
00h	016h	01h	0x5AAE	I2C 1 *2
00h	016h	02h	0x5AB0	I2C 2 *2
00h	016h	03h	0x5AB2	I2C 3 *2
00h	017h	00h	0x5AB4	I2C 4 *2
00h	017h	00h	0x5AB6	I2C 5 *2
00h	017h	00h	0x5AB8	I2C 6 *2
00h	017h	00h	0x5ABA	I2C 7 *2
00h	018h	00h	0x5ABC	SoC UART 0 *2
00h	018h	01h	0x5ABE	SoC UART 1 *2
00h	018h	02h	0x5AC0	SoC UART 2 *2
00h	018h	03h	0x5AEE	SoC UART 3 *2
00h	019h	00h	0x5AC2	SPI 0 *2
00h	019h	01h	0x5AC4	SPI 1 *2
00h	019h	02h	0x5AC6	SPI 2 *2
00h	01Bh	00h	0x5ACA	SD Card
00h	01Ch	01h	0x5ACC	eMMC
00h	01Fh	00h	0x5AE8	LPC Bus
00h	01Fh	01h	0x5AD4	SM Bus
02h	00h	00h	0x1539	Intel PCIe Ethernet Network on Module

Note

The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.

**1 The PCI Express Ports may only be visible if the PCI Express Port is set to "Enabled" in the BIOS setup program and a device is attached to the corresponding PCI Express port on the carrier board.*

**2 This device is disabled as default in BIOS Setup.*

9.3 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

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9.4 SMBus

System Management (SM) bus signals are connected to the Intel® Apollo Lake SoC and the SMBus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

9.5 congatec System Sensors

conga-MA5 offers several sensors and monitors accessible through CGOS interface and also visible on the health monitor submenu in BIOS setup:

- Two temperature sensors
  - CPU temperature based on CPU digital thermal sensor
  - Board temperature sensor located on the board controller
- Two voltage sensors
  - DC Input voltage sensor
  - 5V standby voltage sensor
- One fan monitor

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10 BIOS Setup Description

The BIOS setup description of the conga-MA5 can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-MA5 is identified as MA50R1xx, where:

- MA5 is the project name
- R is the identifier for a BIOS ROM file
- 1 is the feature number
- xx is the major and minor revision number.

The binary size of conga-MA5 BIOS is 8 MB.

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10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-MA5 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

10.4 Supported Flash Devices

The conga-MA5 supports the following flash device:

- Winbond W25Q64JVSSIQ (8 MB)

The flash devices listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note "AN7_External_BIOS_Update.pdf" on the congatec website at www.congatec.com.

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