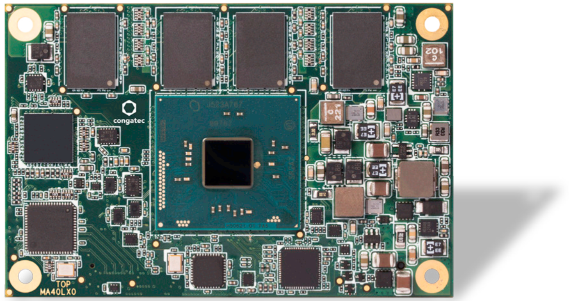

COM Express™ conga-MA4

COM Express Type 10 Mini Module Based On N-Series Intel® Pentium® and Intel® Celeron® SoC

User's Guide

Revision 1.0

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2016.03.07	DGL	• Preliminary release
1.0	2016.08.08	BEU	• Updated section 2.5 "Power Consumption" and 2.6 "Supply Voltage Battery Power" • Renamed section 4 "Heatspreader" to "Cooling Solutions"and updated the section • Added sections 9 "System Resources", 10 "BIOS Setup Description" and 11 "Additional BIOS Features" • Final release

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-MA4. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents are COM Express™ Design Guide and COM Express™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

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ISO 9001 CERTIFICATION TM Intertek

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Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
DDC	Display Data Channel
SoC	System On Chip
LVDS	Low-Voltage Differential Signaling
Gbe	Gigabit Ethernet
eMMC	Embedded Multi-media Controller
MLC	Multi-level Cell
SLC	Single-level Cell
HDA	High Definition Audio
cBC	congatec Board Controller
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

Contents

List of Tables

1 Introduction

COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express™ modules are available in following form factors:

• Mini	84mm x 55mm
• Compact	95mm x 95mm
• Basic	125mm x 95mm
• Extended	155mm x110mm

The COM Express Specification Rev 2.1 currently defines seven different pinout types. These are shown in the table below.

Table 1 Types of COM Express™ Pinouts/Features

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports
Type 1	A-B	Up to 6			1
Type 2	A-B C-D	Up to 22	32 bit	1	1
Type 3	A-B C-D	Up to 22	32 bit		3
Type 4	A-B C-D	Up to 32		1	1
Type 5	A-B C-D	Up to 32			3
Type 6	A-B C-D	Up to 24			1
Type 10	A-B	Up to 4			1

conga-MA4 modules use the Type 10 pinout definition. They are equipped with single 220-pin high performance connector that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 10 pinout provides the ability to offer PCI Express, Serial ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

conga-MA4 Options Information

The conga-MA4 is available in four variants (commercial only). The table below show the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Table 2 conga-MA4 Commercial Variants

Part-No.	047904	047905	047906	047907
Processor	Intel® Pentium® N3710 Quad Core, 1.6GHz, Burst 2.56GHz	Intel® Celeron® N3160 Quad Core, 1.6GHz, Burst 2.24GHz	Intel® Celeron® N3060 Dual Core, 1.6GHz, Burst 2.48GHz	Intel® Celeron® N3010 Dual Core, 1.04 GHz, Burst 2.24GHz
L2 Cache	2 MB	2 MB	2 MB	2 MB
Onboard Memory	4GB DDR3L-1600 dual channel	2GB DDR3L-1600 dual channel	2GB DDR3L-1600 dual channel	2GB DDR3L-1600 single channel
ECC Memory Support	No	No	No	No
Graphics	Intel® HD Graphics Gen 8, 16 EUs	Intel® HD Graphics Gen 8, 12 EUs	Intel® HD Graphics Gen 8, 12 EUs	Intel® HD Graphics Gen 8, 12 EUs
GFX Base/Burst	400/ 700 MHz	320 / 640 MHz	320 / 600 MHz	320 / 600 MHz
LVDS/(eDP 1.4 assy opt)	Single 18 or 24 bpp	Single 18 or 24 bpp	Single 18 or 24 bpp	Single 18 or 24 bpp
DDI	DP 1.1a or HDMI 1.4b / DVI	DP 1.1a or HDMI 1.4b / DVI	DP 1.1a or HDMI 1.4b / DVI	DP 1.1a or HDMI 1.4b / DVI
eMMC (SLC/MLC)	16 GB (MLC)	16 GB (MLC)	16 GB (MLC)	16 GB (MLC)
SD Card	Yes	Yes	Yes	Yes
Max. TDP / SDP	6W / 4W	6W / 4W	6W / 4W	4W / 3W

Part-No.	047908
Processor	Intel® Atom® x5-E8000 Quad Core, 1.04GHz, Burst 2.0 GHz
L2 Cache	2 MB
Onboard Memory	2GB DDR3L-1600 single channel
ECC Memory Support	No
Graphics	Intel® HD Graphics Gen 8, 12 EUs
GFX Base/Burst	320 / 320 MHz
LVDS/(eDP 1.4 assy opt)	Single 18 or 24 bpp
DDI	DP 1.1a or HDMI 1.4b / DVI
eMMC (SLC/MLC)	8 GB (MLC)
SD Card	Yes
Max. TDP / SDP	5W / 4W

2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 10 Rev. 2.1 (mini size 84 x 55 mm)	
Processor	Intel® Pentium® N3710, Intel® Celeron® N3160 / N3060 / N3010 / Intel® Atom™ x5-E8000	
Memory	conga-MA4: Up to 8 GB non-ECC DDR3L onboard memory interface with data rates up to 1600 MT/s.	
Chipset	Integrated in SoC	
Onboard Storage	Optional eMMC 4.51 onboard flash up to 64 GB of MLC	
Audio	High Definition Audio (HDA)/digital audio interface with support for one HDA codec.	
Ethernet	Gigabit Ethernet via the onboard Intel® I211 Gigabit Ethernet controller. Connected to PCIe3 lane.	
Graphics Options	Intel® HD Graphics Gen. 8, full hardware acceleration for MPEG2, H.264, DirectX11.1, DirectX12 for Windows 10, OCL 1.2, OGL 4.2, WMV9 and VC1. Dual simultaneous display support.	
	1x DDI1 (Digital Display Interface 1). Supports the following via eDP to LVDS bridge IC: - Single-channel LVDS interface: 1 x 18 bpp or 1 x 24 bpp. - VESA LVDS color mappings - Automatic Panel Detection via Embedded Panel Interface based on VESA EDID™ 1.3. - Resolution up to 1400x1050 @ 60 Hz in single channel LVDS mode. Optional eDP 1.4 interface supporting up to 2560x 1440 @ 60Hz(assembly option) **NOTE:** Either eDP or LVDS signals supported, not both signal types simultaneously	1x DDI0 (Digital Display Interface 0). Supports - 1x DisplayPort 1.1a. Multiplexed with HDMI/DVI ports. Supports Hot-Plug detect. - 1x HDMI 1.4b port. Multiplexed with DisplayPort (DP)/ DVI. Supports Hot-Plug detect - 1x DVI ports. Multiplexed with HDMI/DP ports. Supports Hot-Plug detect. - Resolution up to 2560x1600@60Hz / 3840x2160@30Hz
Peripheral Interfaces	2x Serial ATA® 3.0 up to 6Gb/s Up to 4x PCI Express® Gen2 links with up to 5.0 GT/s per lane (no GbE assembly option for 4th PCIe lane) 8x USB 2.0 (4x direct from SoC, 4x from 4 port hub) 2x USB 3.0 (direct form SoC) 1x SD/MMC (on module only)	2x UART GPIOs muxed with SD card (not both types simultaneously) SPI Bus (For external BIOS FLASH only) LPC Bus I^2C Bus, multimaster
BIOS	AMI Aptio® V with compliance for UEFI 2.4 Errat B; 8 MByte serial SPI with congatec Embedded BIOS features (OEM Logo, OEM CMOS Defaults, LCD Control, Display Auto Detection, Backlight Control, Flash Update)	
Power Mgmt.	ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).	
congatec Board Controller	Multi Stage Watchdog, non-volatile User Data Storage, Manufacturing and Board Information, Board Statistics, BIOS Setup Data Backup, I^2C bus (fast mode, 400 kHz, multi-master), Power Loss Control	

Note

Some of the features mentioned in the above Feature Summary are optional and require customized articles. Check the part number of your module and compare it to the option information list on page 12 to determine what options are available on your particular module. For more information, contact congatec support.

2.2 Supported Operating Systems

The conga-MA4 supports the following operating systems

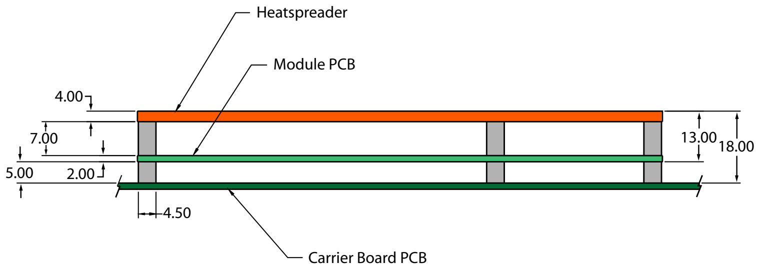
- Microsoft® Windows® 10 Desktop (64b/32b)
- Microsoft® Windows® 8.1 (Pro / WEI 8.1) non-connecteted standby
- Microsoft Windows® 7 (Pro/WES7)
- Linux
- Android Lollipop

Note

For the installation of Windows 7/8/10 32bit and WES7/8, congatec AG recommends a minimum storage capacity of 16 GB. Windows 7/8/10 64bit requires a minimum capacity of 20GB of storage space. congatec will not offer installation support for systems with less than 16 GB storage space for 32bit Windows 7/8/10 and 20GB storage space for 64bit Windows 7/8/10.

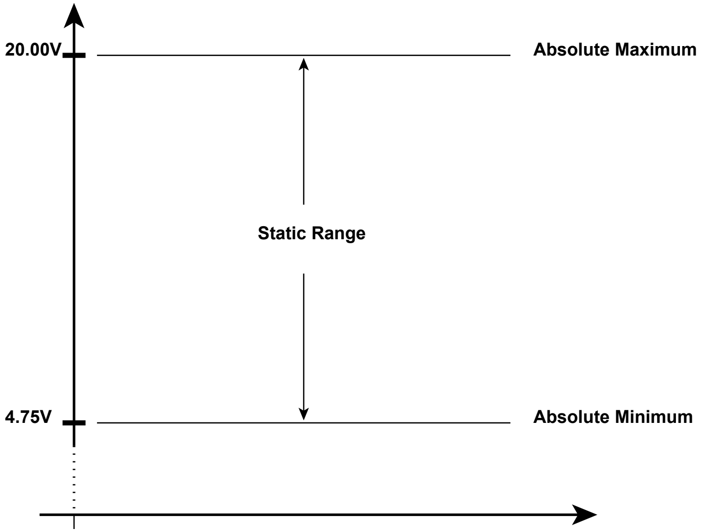
2.3 Mechanical Dimensions

- 84.0 mm x 55.0 mm
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm



2.4 Supply Voltage Standard Power

- 4.75V - 20V (Wide input range)



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 10 (single connector, 220 pins).

Table 4 Power Limits on Type 10 Connector

Power Rail	Module Pin Current Capability (A)	Nominal Input (V)	Input Range (V)	Derated Input (V)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (W)	Assumed Conversion Efficiency	Max. Load Power (W)
Wide Input	6		4.75-20.0	4.75	+/- 100	28	85%	23.8
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 95% of nominal within 0.1 ms to 20 ms (0.1 ms ≤ Rise Time ≤ 20 ms). Each DC input voltage must rise from 10% to 90% of its nominal voltage in a smooth, continuous ramp and the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured using the following test setup:

- conga-MA4 COM
- modified carrier board to measure the power consumption of the COM
- product specific cooling solution with the highest cooling capacity
- running Windows OS

Note

All peripherals were powered externally and therefore did not influence the measured values.

The power consumption values were recorded during the following S-states:

Table 5 System State Description

System State	Description
S0: Minimum value	COM set to lowest frequency mode (LFM) with minimum core voltage during desktop idle. The CPU was stressed to its maximum frequency in this S-state.
S0: Maximum value	COM set to highest frequency mode (HFM/Turbo Boost). The CPU was stressed to its maximum frequency in this S-state.
S0: Peak value	The worst case power consumption value shows the peak value over a short period of time. Highest power spike during the measurement of "S0: Maximum value". This value should be taken into consideration when designing the system's power supply to ensure that the power supply is sufficient during worst case scenarios
S3	COM is powered by VCC_5V_SBY.
S5	COM is powered by VCC_5V_SBY.

Note

All power consumption values except "S0: Peak value" were averaged over a 30 second time period. The peak value is an indicator of the minimum power supply to run the COM.

Processor Information

The tables below provide additional information about the power consumption data for each of the variants .

Table 6 Power Consumption - Intel® Pentium® N3710

Part No. 047904	Intel® Pentium® N3710 1.6 GHz Quad Core 2MB L2 Cache (14nm) Hardware revision A.0 /BIOS revision MA40R009				
Max Turbo Frequency	2.56GHz				
Memory Size	4GB				
Operating System	Windows 7 (64 bit)				
Power State	S0: Min	S0: Max	S0: Peak	S3	S5
Power consumption	0.21 A /2.48 W	1.25 A /15.01 W	1.96 A /23.56 W	0.11 A /0.57 W	0.1 A /0.48 W

Table 7 Power Consumption - Intel® Pentium® N3160

Part No. 047905	Intel® Pentium® N3160 1.6GHz Quad Core 2MB L2 Cache (14nm) Hardware revision A.0 /BIOS revision MA40R009				
Max Turbo Frequency	2.24GHz				
Memory Size	2GB				
Operating System	Windows 7 (64 bit)				
Power State	S0: Min	S0: Max	S0: Peak	S3	S5
Power consumption	0.19 A /2.3 W	1.23 A /14.72 W	1.41 A /16.91 W	0.11 A /0.55 W	0.1 A /0.52 W

Table 8 Power Consumption - Intel® Celeron® N3060

Part No. 047906	Intel® Celeron® N3060 1.6GHz Dual Core 2MB L2 Cache (14nm) Hardware revision A.0 /BIOS revision MA40R009				
Max Turbo Frequency	2.48GHz				
Memory Size	2GB				
Operating System	Windows 7 (64 bit)				
Power State	S0: Min	S0: Max	S0: Peak	S3	S5
Power consumption	0.19 A /2.32 W	1 A /12.05 W	1.16 A /13.94 W	0.11 A /0.54 W	0.1 A /0.5 W

Table 9 Power Consumption - Intel® Celeron® N3010

Part No. 047907	Intel® Celeron® N3010 1.04GHz Dual Core 2MB L2 Cache (14nm) Hardware revision A.0 /BIOS revision MA40R009				
Max Turbo Frequency	2.24GHz				
Memory Size	2GB				
Operating System	Windows 7 (64 bit)				
Power State	S0: Min	S0: Max	S0: Peak	S3	S5
Power consumption	0.18 A /2.2 W	0.84 A /10.07 W	1 A /11.96 W	0.11 A /0.53 W	0.1 A /0.51 W

Table 10 Power Consumption - Intel® Atom™ x5-E8000

Part No. 047908	Intel® Atom™ x5-E8000 1.04GHz Quad Core 2MB L2 Cache (14nm) Hardware revision A.0 /BIOS revision MA40R009				
Max Turbo Frequency	2.0GHz				
Memory Size	2GB				
Operating System	Windows 7 (64 bit)				
Power State	S0: Min	S0: Max	S0: Peak	S3	S5
Power consumption	0.18 A /2.19 W	0.74 A /8.88 W	0.81 A /9.76 W	0.11 A /0.57 W	0.1 A /0.52 W

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Supply power for S3 mode is 5V while all other measured modes are supplied with 12V power. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

2.6 Supply Voltage Battery Power

- 2.0V-3.5V DC

Table 11 Typical 3V DC CMOS Battery Power Consumption

RTC (integrated in the SoC) @	Voltage	Current
-10°C	3V DC	1.98 μA
25°C	3V DC	2.17 μA
70°C	3V DC	3.81 μA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

2.7 Environmental Specifications

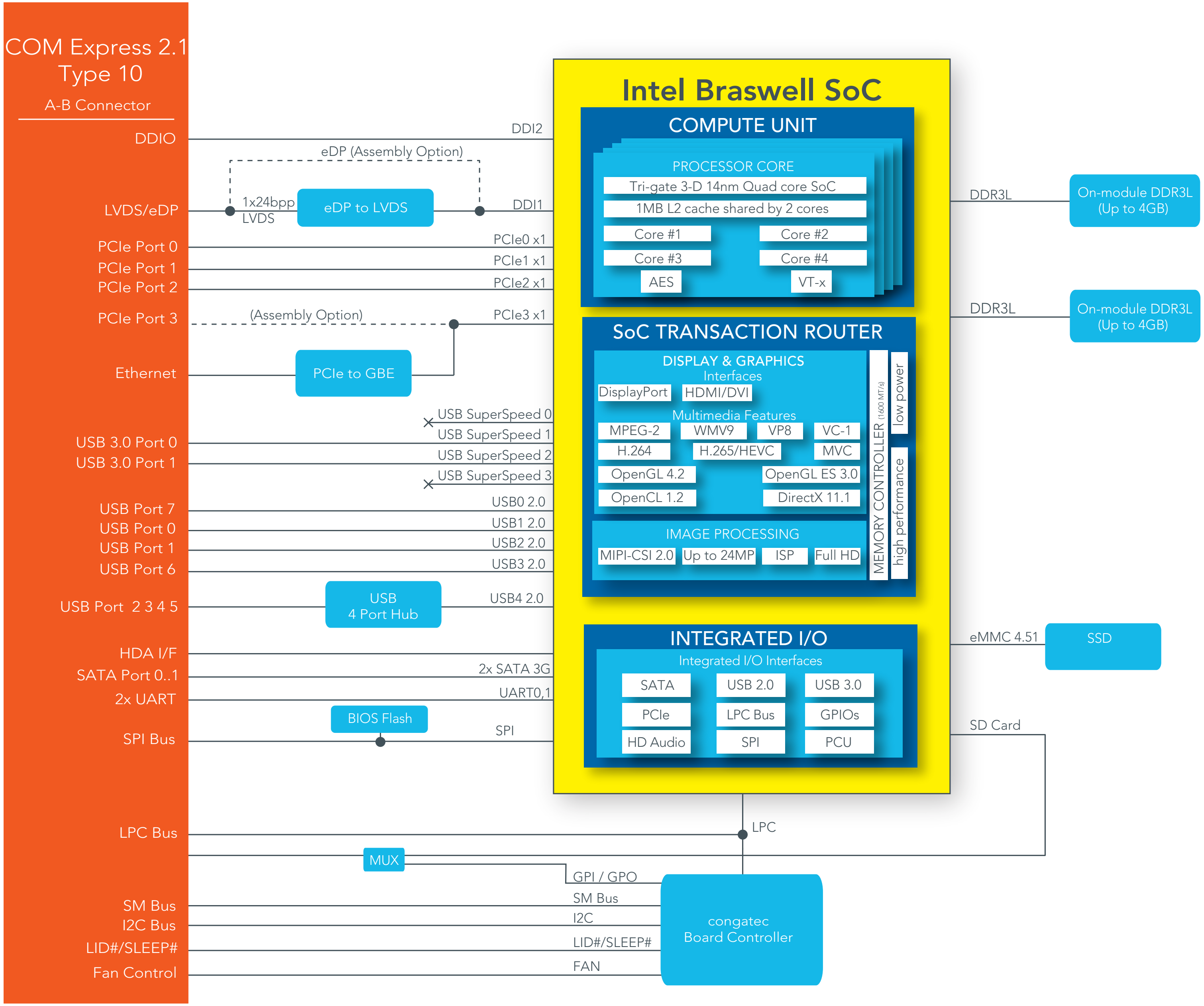
Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



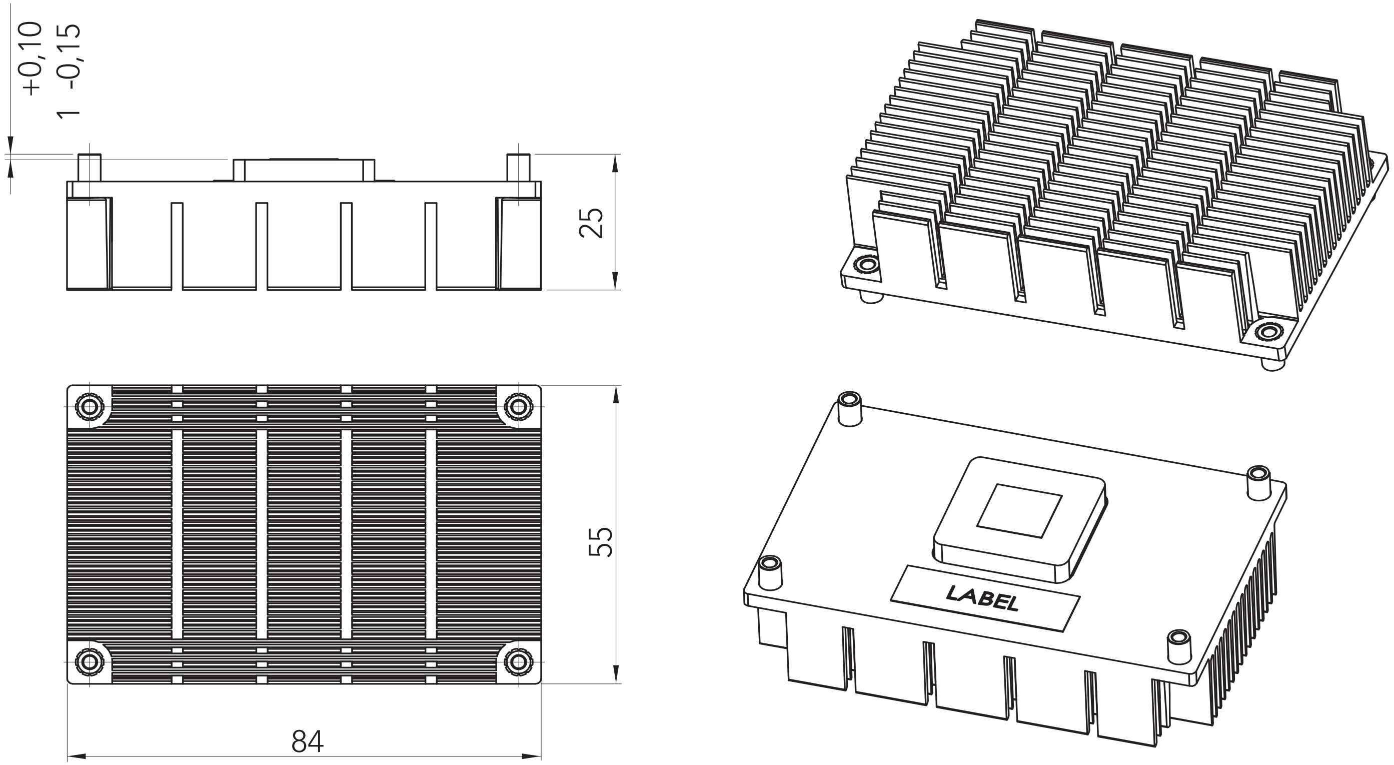
4 Cooling Solutions

congatec AG offers two cooling solutions for the conga-MA4:

- Passive cooling solution (CSP)
- Heatspreader

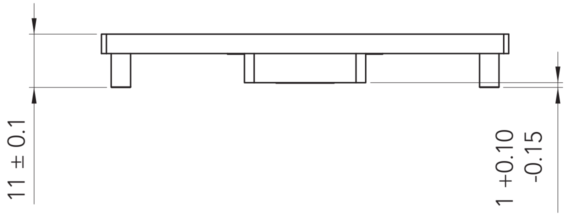
The dimensions of the cooling solutions are shown below. All measurements are in millimeters. The maximum torque specification for heatspreader screws is 0.3 Nm. Mechanical system assembly mounting shall follow the valid DIN/ISO specifications.

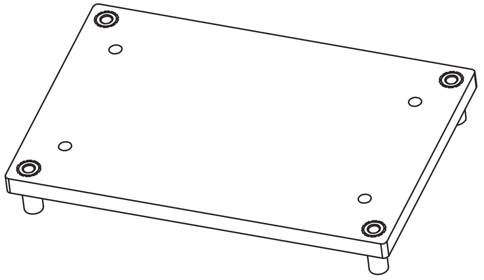
4.1 CSP Dimensions

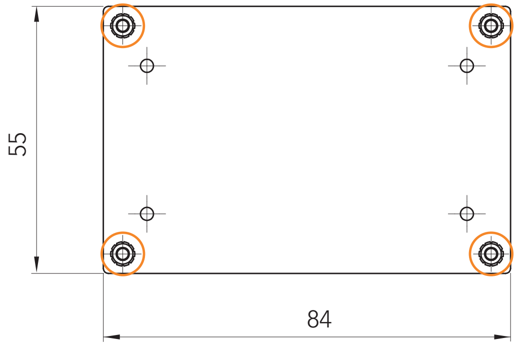


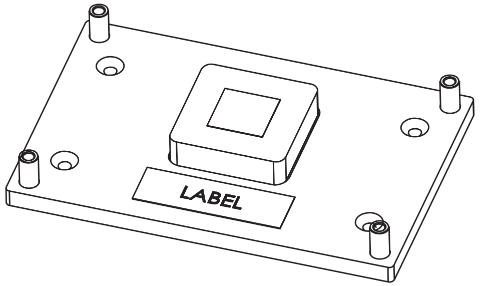
4.2 Heatspreader Dimensions

The heatspreader acts as a thermal coupling device to the module and is thermally coupled to the CPU via a thermal gap filler. On some modules, it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.









◎ M2.5x11mm threaded standoff for threaded version or
Ø2.7x11mm nonthreaded standoff for borehole version

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis thereby using the whole chassis as a heat dissipater.

Note

The gap pad material used on all heatspreaders contains silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.

Caution

The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.

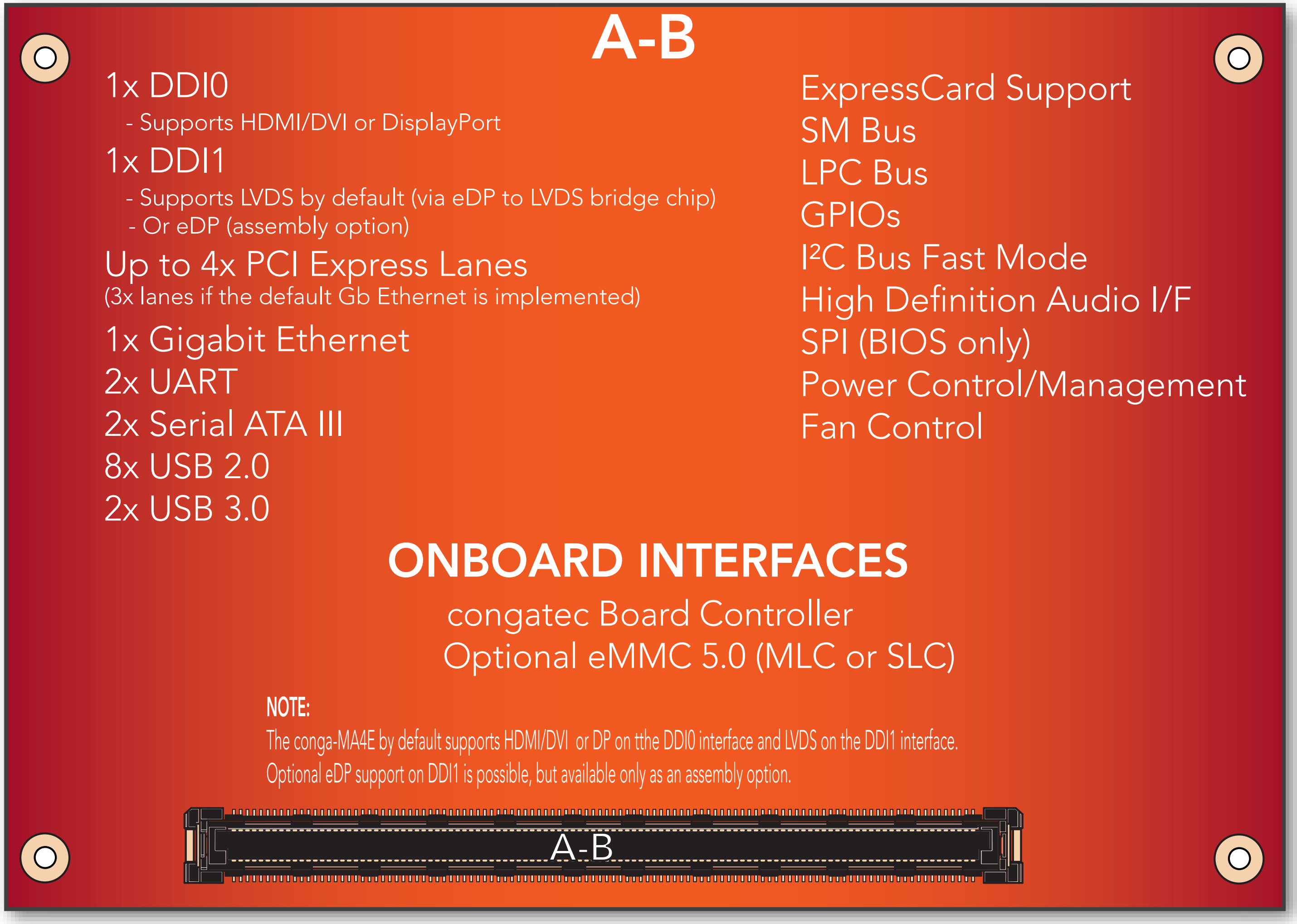
For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.

For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.

Also, do not exceed the maximum torque specified for the screws. Doing so may damage the module or/and the carrier board.

5 Connector Subsystems Rows A, B

The conga-MA4 is connected to the carrier board via a 220-pin connector (COM Express Type 10 pinout). This connector is broken down into two rows (rows A and B).



A-B

1x DDI0
- Supports HDMI/DVI or DisplayPort

1x DDI1
- Supports LVDS by default (via eDP to LVDS bridge chip)
- Or eDP (assembly option)

Up to 4x PCI Express Lanes
(3x lanes if the default Gb Ethernet is implemented)

1x Gigabit Ethernet
2x UART
2x Serial ATA III
8x USB 2.0
2x USB 3.0

ExpressCard Support
SM Bus
LPC Bus
GPIOs
I^{2}C Bus Fast Mode
High Definition Audio I/F
SPI (BIOS only)
Power Control/Management
Fan Control

ONBOARD INTERFACES

congatec Board Controller
Optional eMMC 5.0 (MLC or SLC)

NOTE:
The conga-MA4E by default supports HDMI/DVI or DP on tthe DDI0 interface and LVDS on the DDI1 interface.
Optional eDP support on DDI1 is possible, but available only as an assembly option.

top view

5.1 Connector Rows A and B

The following subsystems can be found on conga-MA4 COM Express connector rows A and B.

5.1.1 PCI Express™

The conga-MA4 by default offers up to 3 PCI Express externally on the connector (PCIe 0-2). It can also offer up to 4 PCI Express on the connector if the fourth PCI express lane (PCIe 3) is not used for Gigabit Ethernet controller. This option is only available as an assembly option.

The default configuration for the lanes on the COM Express connector is 3 x1. A 1 x2 + 1 x1 configuration is also possible but requires special/customized BIOS. The configuration for the assembly option (4 PCI Express lanes) is 4 x1. A 2 x2, 1 x4 or 1 x2 + 2 x1 configuration is also possible but requires special/customized BIOS.

The PCI Express interface is based on the PCI Express Specification 2.0 with Gen 1 (2.5Gb/s) and Gen 2 (5 Gb/s) speed. For more information refer to the conga-MA4 pinout table in section 8 "Signal Descriptions and Pinout Tables" and table 7 "PCI Express Signal Descriptions".

5.1.2 Gigabit Ethernet

The conga-MA4 offers a Gigabit Ethernet interface on the COM Express connector via the onboard Intel® I211 Gigabit Ethernet controller. This controller is connected to the Intel® Braswell SoC through the fourth PCI Express lane.

The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

5.1.3 Serial ATA™ (SATA)

The conga-MA4 offers two SATA interfaces on the COM Express connector via a SATA host controller integrated in the Intel® Braswell SoC. The controller supports independent DMA operation and data transfer rates of 1.5 Gb/s, 3.0 Gb/s and 6.0 Gb/s. It also supports two modes of operation - a legacy mode and AHCI mode. Software that uses legacy mode will not have AHCI capabilities.

For more information, refer to section 10 "BIOS Setup Description".

5.1.4 Universal Serial Bus

The conga-MA4 offers 8x USB 2.0 ports and 2x USB 3.0 ports. The two USB 3.0 ports and four of the USB 2.0 ports (USB 0, USB1, USB6 and USB7) are routed directly from the SoC to the COM Express connector. The other four USB 2.0 ports (USB2, USB3, USB4, & USB5) are routed to the connector via a 4-port USB hub.

5.1.4.1 USB 2.0

The conga-MA4 offers 8 USB 2.0 interfaces on the COM Express connector. The xHCI host controller in the SoC supports these interfaces with high-speed, full-speed and low-speed USB signalling. The xHCI host controller complies with USB standard 1.1 and 2.0. For more information about how the USB host controllers are routed, see section 7.3 "USB Port Mapping".

5.1.4.2 USB 3.0

The conga-MA4 offers two sets of USB 3.0 Super Speed (SS) signals on the COM Express connector.

Both USB 3.0 ports are controlled by a xHCI host controller in the SoC. The xHCI host controller allows data transfers of up to 5 Gb/s and supports SuperSpeed, high-speed, full-speed and low-speed USB signalling. See section 7.3 for more information about USB port mapping.

Note

Either USB 3.0 port can be used as a debug port. All USB 3.0 ports support xHCI debug port functionality.

USB 3.0 ports 0/1 need to be paired with USB 2.0 ports 0/1 on the carrier board.

5.1.5 ExpressCard™

The conga-MA4 supports the implementation of ExpressCards, which requires the dedication of one USB port and a x1 PCI Express link for each ExpressCard used.

5.1.6 High Definition Audio (HDA) Interface

The conga-MA4 provides an interface that supports the connection to an HDA audio codec

5.1.7 Digital Display Interface

The conga-MA4 offers two Digital Display Interfaces (DDI0 & DDI1) on the COM Express connector. The DDI0 supports HDMI/DVI or DisplayPort while the DDI1 supports LVDS by default (via an eDP to LVDS bridge IC) or eDP as an assembly option.

The conga-MA4 supports eDP 1.4, DP 1.1a, DVI or HDMI 1.4b, audio on DP and HDMI, High-bandwidth Digital Content Protection 1.4/2.1 and up to two independent displays. The display combinations supported are shown below:

Table 12 Display Combination

Display 1	Display 2	Display 1 Max. Resolution	Display 2 Max. Resolution
DDI0 (DP,HDMI/DVI)	DDI1 (LVDS/eDP)	2560x1600 @60Hz (HDMI/DVI/DP) 3840x2160 @30Hz (HDMI/DVI/DP)	1400x1050 @60Hz (single channel LVDS) 2560x1440 @60hz (stuffing optional eDP)
DDI1 (LVDS/eDP)	DDI0 (DP,HDMI/DVI)	1400x1050 @60Hz (single channel LVDS) 2560x1440 @60hz (stuffing optional eDP)	2560x1600 @60Hz (HDMI/DVI/DP) 3840x2160 @30Hz (HDMI/DVI/DP)

5.1.7.1 HDMI

High-Definition Multimedia Interface (HDMI) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video.

The conga-MA4 supports one HDMI interface with resolution up to 2560x1600 @60Hz or 3840x2160 @30Hz.

Note

See table 11 above for possible display combinations.

5.1.7.2 DVI

The DVI is similar to HDMI in the way it uses TMDS for transmitting data from transmitter to the receiver but unlike the HDMI, does not support audio and CEC.

The conga-MA4 supports one DVI interface with resolution up to 2560x1600 @60H or 3840x2160 @30Hz.

Note

See table 11 above for possible display combinations.

5.1.7.3 DisplayPort (DP)

DisplayPort is an open, industry standard digital display interface, that has been developed within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

The conga-MA4 supports one DP interface with resolution up to 2560x1600 @60Hz or 3840x2160 @30Hz and one optional eDP port at 2560 x 1440 @ 60Hz..

Note

See table 11 above for possible display combinations.

5.1.8 LVDS

The conga-MA4 offers a 24bpp single channel LVDS interface on the COM Express connector. The interface is provided by routing the onboard PTN3460 to the SoC's second Digital Display Interface (DDI1).

The PTN3460 processes incoming DisplayPort stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format. It supports the single channel signalling on the conga-MA4 with color depths of 18 bits or 24 bits per pixel and pixel clock frequency up to 112 MHz.

5.1.9 SD Card

The conga-MA4 offers a 4-bit SD interface for SD/MMC cards on the COM Express connector. The SD signals are multiplexed with GPIO signals and controlled by the congatec board controller. The SD card controller in the Storage Control Cluster of the SoC supports the SD interface with up to 832 Mb/s data rate using 4 parallel data lines.

5.1.10 General Purpose Serial Interface (UART)

The conga-MA4 offers two UART interfaces. The pins are designated SER0_TX, SER0_RX, SER1_TX and SER1_RX. Data out of the module is on the _TX pins. Hardware handshaking and hardware flow control are not supported. See table 27 "General Purpose Serial Interface Signal Descriptions" for the signal description and connector pin assignments.

5.1.11 LPC Bus

The conga-MA4 offers the LPC (Low Pin Count) bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals and functionality. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific carrier board using this bus. Only certain devices such as Super I/O or TPM chips can be implemented on the carrier board. See section 9.1.1 for more information about the LPC Bus

Note

The Braswell LPC bus operates at 25 MHz - All SKUs

5.1.12 SPI

An SPI interface that supports booting from an external BIOS SPI flash is available on the conga-MA4 via SoC . The interface is implemented on the conga-MA4 as an external alternative interface to the on module BIOS SPI flash device.

5.1.13 I²C Bus

The I²C bus is implemented through the congatec board controller. It provides a fast mode 400 KHz multi-master I²C bus.

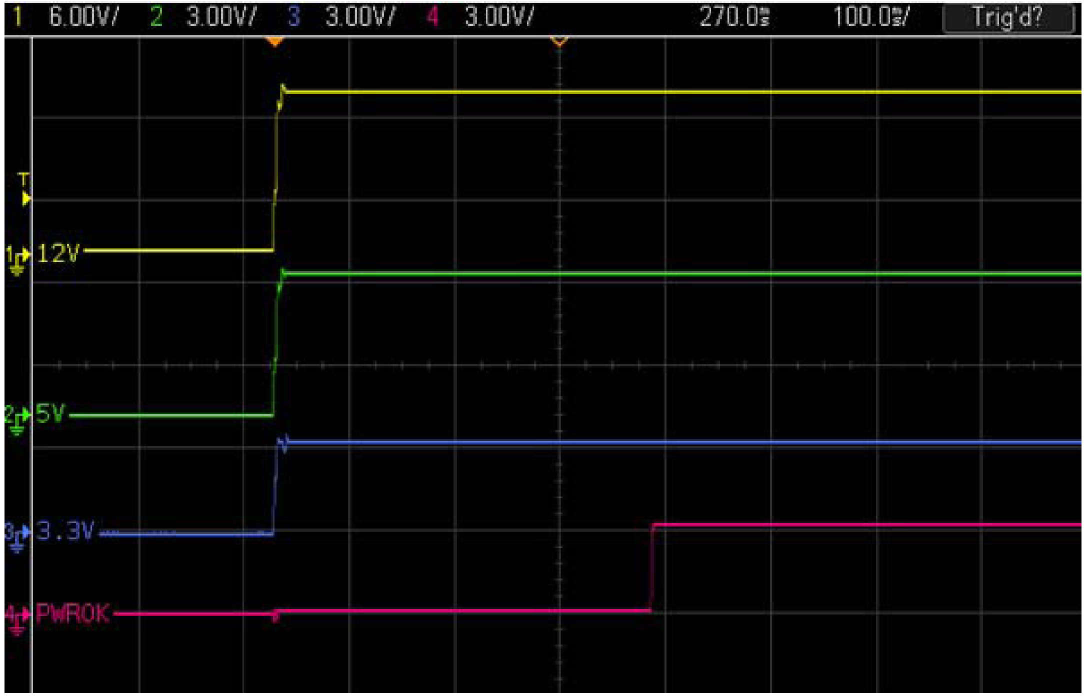
5.1.14 SM Bus

The SM bus is implemented through the congatec board controller. It is an I²C bus variant for system management functions.

5.1.15 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. See screenshot below.



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

It is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the "power good" signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, you must make sure that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-MA4 provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-MA4's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the COM Express connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the COM Express connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

Input power of 4.75 - 20 volt is the sole operational power source for the conga-MA4. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-MA4 application:

- It has also been noticed that on some occasions, problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

5.1.16 Power Management

ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).

6 Additional Features

6.1 Onboard Interfaces

6.1.1 eMMC 4.5.1

The conga-MA4 offers an optional eMMC 5.0 flash (MLC) onboard, with up to 64 GB capacity with a controller that is compliant with eMMC 4.5.1.

6.1.2 congatec Board Controller (cBC)

The conga-MA4 is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRBI microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

6.1.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.1.2.2 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

6.1.2.3 Watchdog

The conga-MA4 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the watchdog; therefore, the conga-MA4 does not support external hardware triggering.

For more information about the Watchdog feature, see the BIOS setup description section 10.4.1 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

6.1.2.4 Fan Control

The conga-MA4 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

A four wire fan must be used to generate the correct speed readout.

The congatec COM Express Type 6 and Type 10 modules use a Push-Pull output for the fan_pwm signal instead of the open drain output specified in the COM Express specification. Although this does not comply with the COM Express specification 2.0, the benefits are obvious. The Push-Pull output optimizes the power consumed by the fan_pwm signal without functional change.

6.1.2.5 General Purpose Input/Output

The conga-MA4 offers general purpose inputs and outputs for custom system design. These GPIOs are multiplexed with SD signals and are controlled by the cBC.

6.1.2.6 I^{2}C Bus

The conga-MA4 offers support for the frequently used I^{2}C bus. Thanks to the I^{2}C host controller in the cBC the I^{2}C bus is multimaster capable and runs at fast mode.

6.1.3 Embedded BIOS

The conga-MA4E is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. These are the most important embedded PC features:

6.1.3.1 CMOS Backup in Non Volatile Memory

A copy of the CMOS memory (SRAM) is stored in the BIOS flash device. This prevents the system from not booting up with the correct system configuration if the backup battery (RTC battery) has failed. Additionally, it provides the ability to create systems that do not require a CMOS backup battery.

6.1.3.2 OEM CMOS Default Settings and OEM BIOS Logo

This feature allows system designers to create and store their own CMOS default configuration and BIOS logo (splash screen) within the BIOS flash device. Customized BIOS development by congatec for these changes is no longer necessary because customers can easily do these changes by themselves using the congatec system utility CGUTIL.

6.1.3.3 OEM BIOS Code

With the congatec embedded BIOS it is even possible for system designers to add their own code to the BIOS POST process. Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table, verb tables for HDA codecs, rare graphic modes and Super I/O controllers.

For more information about customizing the congatec embedded BIOS refer to the congatec System Utility user's guide, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com or contact congatec technical support.

6.1.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-MA4 BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

6.2 API Support (CGOS/EAPI)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

Other COM (Computer on Modules) vendors offer similar driver solutions for these kind of embedded PC features, which are by nature proprietary. All the API solutions that can be found on the market are not compatible to each other. As a result, writing application software that can run on more than one vendor's COM is not so easy. Customers have to change their application software when switching to another COM vendor. EAPI (Embedded Application Programming Interface) is a programming interface defined by the PICMG that addresses this problem. With this unified API, it is now possible to run the same application on all vendor's COMs that offer EAPI driver support. Contact congatec technical support for more information about EAPI.

6.3 Security Features

The conga-MA4 has a fTPM chip which is a firmware based TPM 2.0 compatible implementation an onboard. It also supports a carrier board mounted TPM 1.2 or 2.0 compliant chip, connected via the LPC bus.

6.4 Suspend to Ram

The Suspend to RAM feature is available on the conga-MA4.

7 conga Tech Notes

The conga-MA4 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help the user to better understand the information found in the system resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Description section.

7.1 Intel N-Series Pentium, Celeron and Atom Features

7.1.1 Processor Core

The Intel Braswell SoC features Dual or Quad Out-of-Order Execution processor cores. Both the dual-core and the quad core modules have 2MB L2 cache. Some of the features supported by the core are:

- Intel 64 architecture
- Intel Streaming SIMD Extensions

  Intel VT-x

  Power Aware Interrupt Routing
- Enhanced Intel SpeedStep Technology
- Thermal management support via Intel Thermal Monitor
- Uses 14 nm process technology

Note

Intel Hyper-Threading technology is not supported (four cores execute four threads)

7.1.1.1 SATA-III

The Intel Braswell SoC provides a host controller for 2x SATA-III devices.

Legacy Mode

When operating in legacy mode, the SATA controllers need two legacy IRQs (14 and 15) and are unable to share these IRQs with other devices. This is because the SATA controllers emulate the primary and secondary legacy IDE controllers.

Native Mode

Native mode allows the SATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources. This means they can be configured anywhere within the system. When either SATA controller 1 or 2 runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system. Setting "Native IDE" mode in the BIOS setup program will automatically enable Native mode. See section 10.4.14 for more information about this.

Running in native mode frees up interrupt resources (IRQs 14 and 15) and decreases the chance that there may be a shortage of interrupts when installing devices.

Note

If your operating system supports native mode then congatec AG recommends you enable it.

7.1.1.2 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-MA4 ACPI thermal solution currently offers two different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points. If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.2 ACPI Suspend Modes and Resume Events

conga-MA4 supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 10.4.8 "ACPI Configuration Submenu".

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

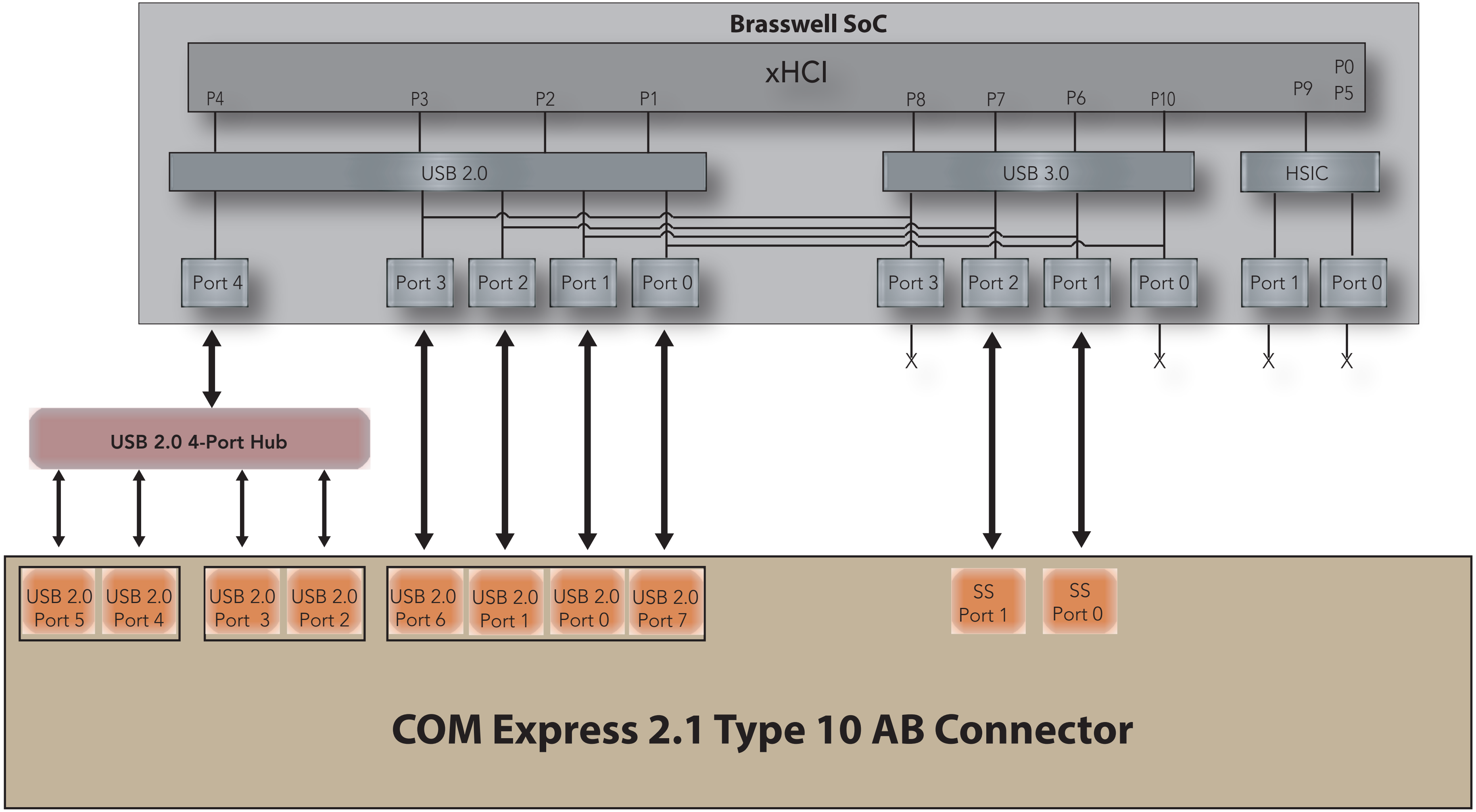
- Windows 8.0/8.1, Windows 10 and Linux

This table lists the "Wake Events" that resume the system from S3 unless otherwise stated in the "Conditions/Remarks" column:

Table 13 Wake Events resuming system from S3

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

7.3 USB Port Mapping



NOTE:

Possible USB configurations are:

(*) Up to 8x USB 2.0
(*) Up to 7x USB 2.0 and 1x USB 3.0
(*) Up to 6x USB 2.0 and 2x USB 3.0

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type 10 connectors used for congatec AG modules. The pinout of the modules complies with COM Express Type 10 Rev. 2.1.

The table below describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 14 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V
I/O 5V	Bi-directional signal 5V
I 3.3V	Input 3.3V
I 5V	Input 5V
I/O 3.3VSB	Input 3.3V active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

8.1 COM Express Connector Pinout

Table 15 COM Express Connector Pinouts

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND(FIXED)	B1	GND(FIXED)	A56	RSVD	B56	RSVD
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND(FIXED)	B60	GND(FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0# (*)	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# (*)	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND(FIXED)	B11	GND(FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND(FIXED)	B70	GND(FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	eDP_TX2+/LVDS_A0+	B71	DDI0_PAIR0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	eDP_TX2-/LVDS_A0-	B72	DDI0_PAIR0-
A18	SUS_S4#	B18	SUS_STAT#	A73	eDP_TX1+/LVDS_A1+	B73	DDI0_PAIR1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	eDP_TX1-/LVDS_A1-	B74	DDI0_PAIR1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	eDP_TX0+/LVDS_A2+	B75	DDI0_PAIR2+
A21	GND(FIXED)	B21	GND(FIXED)	A76	eDP_TX0-/LVDS_A2-	B76	DDI0_PAIR2-
A22	USB_SSRX0-	B22	USB_SSTX0-	A77	eDP/LVDS_VDD_EN	B77	DDI0_PAIR4+ (*)
A23	USB_SSRX0+	B23	USB_SSTX0+	A78	LVDS_A3+	B78	DDI0_PAIR4- (*)
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP/LVDS_BKLT_EN
A25	USB_SSRX1-	B25	USB_SSTX1-	A80	GND(FIXED)	B80	GND(FIXED)
A26	USB_SSRX1+	B26	USB_SSTX1+	A81	eDP_TX3+/LVDS_A_CK+	B81	DDI0_PAIR3+
A27	BATLOW#	B27	WDT	A82	eDP_TX3-/LVDS_A_CK-	B82	DDI0_PAIR3-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2	A83	eDP_AUX+/LVDS_I2C_CK	B83	eDP/LVDS_BKLT_CTRL
A29	AC/HDA_SYNC)	B29	AC/HDA_SDIN1 (*)	A84	eDP_AUX-/LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0 (**)	A85	GPI3	B85	VCC_5V_SBY
A31	GND(FIXED)	B31	GND(FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA_BITCLK	B32	SPKR	A87	eDP_HPD	B87	VCC_5V_SBY
A33	AC/HDA_SDOUT	B33	I2C_CK	A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE_CLK_REF-	B89	DD0_HPD
A35	THRMTRIP#	B35	THRM#	A90	GND(FIXED)	B90	GND(FIXED)
A36	USB6-	B36	USB7	A91	SPI_POWER	B91	DDI0_PAIR5+ (*)

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A37	USB6+	B37	USB7+	A92	SPI_MISO (**)	B92	DDI0_PAIR5- (*)
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	DDI0_PAIR6+ (*)
A39	USB4-	B39	USB5-	A94	SPI_CLK (**)	B94	DDI0_PAIR6- (*)
A40	USB4+	B40	USB5+	A95	SPI_MOSI (**)	B95	DDI0_DDC_AUX_SEL
A41	GND(FIXED)	B41	GND(FIXED)	A96	TPM_PP (*)	B96	RSVD
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS# (**)
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	DDI0_CTRLCLK_AUX+
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	DDI0_CTRLDATA_AUX-
A45	USB0-	B45	USB1-	A100	GND(FIXED)	B100	GND(FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ (**)	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND(FIXED)	B51	GND(FIXED)	A106	VCC_12V	B106	VCC_12V
A52	RSVD	B52	RSVD	A107	VCC_12V	B107	VCC_12V
A53	RSVD	B53	RSVD	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	RSVD	B55	RSVD	A110	GND(FIXED)	B110	GND(FIXED)

Note

The signals marked with asterisk (*) are not supported or connected on the conga-MA4.

On Intel Braswell SoC, the signals marked with asterisks (**) have native voltage levels that are different from the levels defined in the COM Express Specification. To comply with the COM Express Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

8.2 COM Express Connector Signal Descriptions

Table 16 High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	High Definition Audio Reset: This signal is the master hardware reset to external codec(s).	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SYNC	A29	High Definition Audio Sync: This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_BITCLK	A32	High Definition Audio Bit Clock Output: This signal is a 24.000MHz serial data clock generated by the Intel® High Definition Audio controller.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SDOUT	A33	High Definition Audio Serial Data Out: This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SDIN[2:0] (**)	B28-B30	High Definition Audio Serial Data In [0]: These signals are serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	I/O 3.3V	PD 100K	AC'97 codecs are not supported. HDA_SDIN[2:1] are not connected.

Note

On Intel Braswell SoC, the signals marked with asterisks (**) have native voltage levels that are different from the levels defined in the COM Express Specification. To comply with the COM Express Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

Table 17 Gigabit Ethernet Signal Descriptions

<table>
<tr><th>Gigabit Ethernet</th><th>Pin #</th><th colspan="4">Description</th><th>I/O</th><th>PU/PD</th><th>Comment</th></tr>
<tr><td rowspan="6">GBE0_MDI0+
GBE0_MDI0-
GBE0_MDI1+
GBE0_MDI1-
GBE0_MDI2+
GBE0_MDI2-
GBE0_MDI3+
GBE0_MDI3-</td><td rowspan="6">A13
A12
A10
A9
A7
A6
A3
A2</td><td colspan="4">Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:</td><td rowspan="6">I/O Analog</td><td rowspan="6"></td><td rowspan="6">Twisted pair signals for external transformer.</td></tr>
<tr><td></td><td>1000</td><td>100</td><td>10</td></tr>
<tr><td>MDI[0]+/-</td><td>B1_DA+/-</td><td>TX+/-</td><td>TX+/-</td></tr>
<tr><td>MDI[1]+/-</td><td>B1_DB+/-</td><td>RX+/-</td><td>RX+/-</td></tr>
<tr><td>MDI[2]+/-</td><td>B1_DC+/-</td><td></td><td></td></tr>
<tr><td>MDI[3]+/-</td><td>B1_DD+/-</td><td></td><td></td></tr>
<tr><td>GBE0_ACT#</td><td>B2</td><td colspan="4">Gigabit Ethernet Controller 0 activity indicator, active low.</td><td>O 3.3VSB</td><td></td><td></td></tr>
<tr><td>GBE0_LINK#</td><td>A8</td><td colspan="4">Gigabit Ethernet Controller 0 link indicator, active low.</td><td>O 3.3VSB</td><td></td><td></td></tr>
<tr><td>GBE0_LINK100#</td><td>A4</td><td colspan="4">Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.</td><td>O 3.3VSB</td><td></td><td></td></tr>
</table>

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.			Not connected

Table 18 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6

Table 19 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0

PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 20 ExpressCard Support Pins Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request.	I 3.3V	PU 10k 3.3V	
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3V	PU 10k 3.3V	

Table 21 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB Port 0 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Native USB 2.0 port from Braswell SoC
USB1+ USB1-	B46 B45	USB Port 1 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Native USB 2.0 port from Braswell SoC.
USB2+ USB2-	A43 A42	USB Port 2 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Routed via on-module USB hub.
USB3+ USB3-	B43 B42	USB Port 3 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Routed via on-module USB hub.
USB4+ USB4-	A40 A39	USB Port 4 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Routed via on-module USB hub.
USB5+ USB5-	B40 B39	USB Port 5 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Routed via on-module USB hub
USB6+ USB6-	A37 A36	USB Port 6 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Native USB 2.0 port from Braswell SoC.
USB7+ USB7-	B37 B36	USB Port 7 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Native USB 2.0 port from Braswell SoC
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_SSTX0+ USB_SSTX0-	B23 B22	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O PCIe		
USB_SSTX1+ USB_SSTX1-	B26 B25	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O PCIe		.
USB_SSRX0+ USB_SSRX0-	A23 A22	Additional receive signal differential pairs for the SuperSpeed USB data path.	I PCIe		
USB_SSRX1+ USB_SSRX1-	A26 A25	Additional receive signal differential pairs for the SuperSpeed USB data path.	I PCIe		.

Table 22 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ eDP_TX2+	A71	LVDS Channel A differential pair 0 Embedded Display Port channel 0 differential pair 2	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A0- eDP_TX2-	A72	LVDS Channel A differential pair 0 Embedded Display Port channel 0 differential pair 2	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A1+ eDP_TX1+	A73	LVDS Channel A differential pair 1 Embedded Display Port channel 0 differential pair 1	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A1- eDP_TX1-	A74	LVDS Channel A differential pair 1 Embedded Display Port channel 0 differential pair 1	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A2+ eDP_TX0+	A75	LVDS Channel A differential pair 2 Embedded Display Port channel 0 differential pair 0	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A2- eDP_TX0-	A76	LVDS Channel A differential pair 2 Embedded Display Port channel 0 differential pair 0	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A3+	A78	LVDS Channel A differential pair 3			
LVDS_A3-	A79	LVDS Channel A differential pair 3			
LVDS_A_CK+ eDP_TX3+	A81	LVDS Channel A differential clock Embedded Display Port channel 0 differential pair 3	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A_CK- eDP_TX3-	A82	LVDS Channel A differential clock Embedded Display Port channel 0 differential pair 3	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_VDD_EN eDP_VDD_EN	A77	Panel power enable	O 3.3V	PD 10k	LVDS (default) Build-time option: eDP
LVDS_BKLT_EN eDP_BKLT_EN	B79	Panel backlight enable	O 3.3V	PD 10k	LVDS (default) Build-time option: eDP

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_BKLT_CTRL eDP_BKLT_CTRL	B83	Panel backlight brightness control	O 3.3V		LVDS (default) Build-time option: eDP
LVDS_I2C_CK eDP_AUX+	A83	DDC lines used for flat panel detection and control. Embedded Display Port AUX channel pair	O 3.3V	PU 2k2 3.3V	LVDS (default) Build-time option: eDP
LVDS_I2C_DAT eDP_AUX-	A84	DDC lines used for flat panel detection and control. Embedded Display Port AUX channel pair	I/O 3.3V	PU 2k2 3.3V	LVDS (default) Build-time option: eDP

Table 23 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V		Not connected
LPC_SERIRQ (**)	A50	LPC serial interrupt	I/O OD 3.3V		
LPC_CLK	B10	LPC clock output - 33MHz for Braswell-I. 25MHz for Braswell-M and D	O 3.3V		

Note

On Intel Braswell SoC, the signal marked with asterisks (**) has native voltage level from the level defined in the COM Express Specification. To comply with the COM Express Specification, the signal is routed through bidirectional level shifter on the module.

Bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route this signal as short as possible.

Table 24 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS# (**)	B97	Chip select for carrier board SPI.	O 3.3VSB		Carrier shall pull to SPI_POWER when external SPI provided but not used.
SPI_MISO (**)	A92	Master Input Slave Output: SPI output data from carrier board SPI device to module.	I 3.3VSB		
SPI_MOSI (**)	A95	Master Output Slave Input: SPI output data from module to carrier board SPI.	O 3.3VSB		
SPI_CLK (**)	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	+ 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or leave no-connect.

Signal	Pin #	Description	I/O	PU/PD	Comment
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. Ground to select external SPI device. Pull high or leave no-connect to select on-module BIOS flash	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or leave no-connect

Note

On Intel Braswell SoC, the signals marked with asterisks (**) have native voltage levels that are different from the levels defined in the COM Express Specification. To comply with the COM Express Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

Table 25 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI0_PAIR0+ DDI0_PAIR0-	B71 B72	Digital Display Interface 0 Pair 0 differential pairs	O		Only TMDS/DP option, no SDVO
DDI0_PAIR1+ DDI0_PAIR1-	B73 B74	Digital Display Interface 0 Pair 1 differential pairs	O		Only TMDS/DP option, no SDVO
DDI0_PAIR2+ DDI0_PAIR2-	B75 B76	Digital Display Interface 0 Pair 2 differential pairs	O		Only TMDS/DP option, no SDVO
DDI0_PAIR3+ DDI0_PAIR3-	B81 B82	Digital Display Interface 0 Pair 3 differential pairs	O		Only TMDS/DP option, no SDVO
DDI0_HPD	B89	Digital Display Interface Hot Plug Detect	I 3.3V	PD 1M	
DDI0_CTRLCLK_AUX+	B98	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect.	I/O	PD100k @ DP mode	
		HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O OD 3.3V	PU 5k 3.3V @ HDMI/DVI mode	
DDI0_CTRLDATA_AUX-	B99	DP AUX- function if DDI1_DDC_AUX_SEL is no connect.	I/O	PU 100k 3.3V@ DP mode	
		HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O OD 3.3V	PU 5k 3.3V @ HDMI/DVI mode	
DDI0_DDC_AUX_SEL	B95	Selects the function of DDI0_CTRLCLK_AUX+ and DDI0_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	

Note

DDI port enables eDP 1.4, DP 1.1a or HDMI 1.4b

Table 26 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP0_LANE0+ DP0_LANE0-	B71 B72	Uni-directional main link for the transport of isochronous streams and secondary data.	O		
DP0_LANE1+ DP0_LANE1-	B73 B74	Uni-directional main link for the transport of isochronous streams and secondary data.	O		
DP0_LANE2+ DP0_LANE2-	B75 B76	Uni-directional main link for the transport of isochronous streams and secondary data. .	O		
DP0_LANE3+ DP0_LANE3-	B81 B82	Uni-directional main link for the transport of isochronous streams and secondary data.	O		
DP0_HPD	B89	Detection of Hot Plug / Unplug and notification of the link layer.	I 3.3V	PD 1M	
DP0_AUX+	B98	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O	PD 100k	
DP0_AUX-	B99	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O	PU 100k 3.3V	

Table 27 HDMI/DVI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS0_DATA2+ TMDS0_DATA2-	B71 B72	HDMI/DVI TMDS lane 2 differential pair.	O		
TMDS0_DATA1+ TMDS0_DATA1-	B73 B74	HDMI/DVI TMDS lane 1 differential pair.	O		
TMDS0_DATA0+ TMDS0_DATA0-	B75 B76	HDMI/DVI TMDS lane 0 differential pair.	O		
TMDS0_CLK + TMDS0_CLK -	B81 B82	HDMI/DVI TMDS Clock output differential pair.	O		
HDMI0_HPD	B89	HDMI/DVI Hot-plug detect.	I	PD 1M	
HDMI0_CTRLCLK	B98	HDMI/DVI I²C Control Clock	I/O OD 3.3V	PU 5k 3.3V	
HDMI0_CTRLDATA	B99	HDMI/DVI I²C Control Data	I/O OD 3.3V	PU 5k 3.3V	

Table 28 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O 3.3V	PU 5K 3.3V	12 volt tolerant
SER1_TX	A101	General purpose serial port transmitter	O 3.3V	PU 5K 3.3V	12 volt tolerant
SER0_RX	A99	General purpose serial port receiver	I 3.3V	PU 5K 3.3V	12 volt tolerant
SER1_RX	A102	General purpose serial port receiver	I 3.3V	PU 5K 3.3V	12 volt tolerant

Table 29 I2C Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I2C port clock output	I/O OD 3.3V	PU 2.2K 3.3VSB	
I2C_DAT	B34	General purpose I2C port data I/O line	I/O OD 3.3V	PU 2.2K 3.3VSB	

Table 30 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PD 10K	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V		
FAN_TACHIN	B102	Fan tachometer input.	I OD	PU 10K 3.3V	Requires a fan with a two pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. This feature is not implemented on the conga-MA4	I 3.3V		Not connected

Note

The congatec COM Express Type 6 and Type 10 modules use a Push-Pull output for the fan_pwm signal instead of the open drain output specified in the COM Express specification. Although this does not comply with the COM Express specification 2.0, the benefits are obvious. The Push-Pull output optimizes the power consumed by the fan_pwm signal without functional change.

Table 31 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a main power input (VIN) that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V		
SUS_STAT#	B18	Suspend Status: Indicates the system will enter a low power state soon. Used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3VSB		Same signal as SUS_S5#
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		Same signal as SUS_S4#
WAKE0#	B66	PCI Express wake up request signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement a wake-up request from an external device.	I 3.3VSB	PU 100k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low.	I 3.3VSB	PU 10k 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch.	I OD 3.3V	PU 10k 3.3VSB	
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3V	PU 10k 3.3VSB	

Table 32 Thermal Protection Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over temperature situation	I 3.3V	PU 10k 3.3V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown	O 3.3V	PU 10k 3.3V	

Table 33 SM Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidrectional clock line	I/O OD 3.3VSB	PU 10k 3.3VSB	
SMB_DAT	B14	System Management Bus bidrectional data line	I/O OD 3.3VSB	PU 10k 3.3VSB	

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_ALERT#	B15	System Management Bus Alert - Active low input can be used to generate an SMI# (System Management Interrupt)	I 3.3VSB	PU 10k 3.3VSB	

Table 34 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3V	PU 10K 3.3V	
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3V		
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3V		
GPO2	B57	General purpose output pins. Shared with SD_WP. Output from COM Express, input to SD	O 3.3V		
GPO3	B63	General purpose output pins. Shared with SD_CD. Output from COM Express, input to SD	O 3.3V		

Table 35 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	B63	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. Maps to GPO3; used as an input when used for SD card support	I 3.3V		
SDIO_CLK	A93	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz. Maps to GPO0.	O 3.3V		
SDIO_CMD	B54	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Maps to GPO1	O 3.3V		
SDIO_WP	B54	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. Maps to GPO2; used as an input when used for SD card support	I 3.3V		
SDIO_DAT0	A54	SDIO Data line. Operates in push-pull mode and maps to GPI0	IO 3.3V		
SDIO_DAT1	A63	SDIO Data line. Operates in push-pull mode and maps to GPI1	IO 3.3V		
SDIO_DAT2	A67	SDIO Data line. Operates in push-pull mode and maps to GPI2	IO 3.3V		

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_DAT3	A85	SDIO Data line. Operates in push-pull mode and maps to GPI3	IO 3.3V		

Table 36 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE10#	A97	Indicates to the carrier board that a Type 10 module is installed.	PDS	This pin is pulled to ground through a 47K resistor.

Table 37 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: 4.75V to 20V. All available VCC_12V pins on the connector(s) shall be used.	P		The conga-MA4 is a Type 10 mini module and as such supports a wide power supply range between 4.75 and 20V
VCC_5V_SBY	B84-B87	Standby power input: +5V nominal. If VCC5V_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real time clock circuit-power input: +3V nominal	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110 B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

Table 38 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	A101	Controller Area Network TX output for CAN Bus channel 0. This pin is shared with SER1_TX	O 3.3V		Not supported
CAN0_RX	A102	Controller Area Network RX input for CAN Bus channel 0. This pin is shared with SER1_RX	I 3.3V		Not supported

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-MA40 modules are functionally identical with a standard PC/AT.

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.1.1 LPC Bus

The conga-MA40 busses all act in a subtractive decoding configuration. This means that I/O cycles that are not claimed by a bus are then forwarded to the next available bus all the way until the LPC bus is reached. Below is a list of I/O Ranges that are consumed by the embedded devices in the SoC and in the SMSC Super I/O.

Table 39 SoC I/O Range Usage Map

Device	IO Address
8259 Master	20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39h, 3Ch-3Dh,
8254s	40h-43h, 50h-53h
PS2 Control	60h, 64h,
NMI Controller	61h, 63h, 65h, 67h
RTC	70h-77h
Postcode (Port 80h)	80h-8Fh
Init Register	92h
8259 Slave	A0h- A1h, A4h-A5h, A8h-A9h, ACh-ADh, B0h-B1h, B4h-B5h, B8h-B9h, BCh-BDh, 4D0h-4D1h
Legacy PCI Bus	CF8h-CFFh
Reset Control	CF9h
Active Power Management	B2h-B3h
ACPI Base Address	400h - 480h

If the SMSC Super I/O is enabled on the system, the the possible following resources will be decode on the LPC bus.

Table 40 SMSC Super I/O Range Usage Map

Device	IO Address
Parallel Port (LPT) Standard Mode	378h-37Fh or 278h-27F or 3BC-3BFh
Parallel Port (LPT) Enhanced Mode	378h-37Fh and 778h-77Fh or 278h-27Fh and 778h-77Fh or 278h-27Fh and 678h-67Fh or 3BCh-3BFh and 7BCh-7BFh
Serial Port (UART1)	3F8h-3FFh or 2F8h-2FFh or 3E8h-3FFh, 2E8h-2EFh
Serial Port (UART2)	3F8h-3FFh or 2F8h-2FFh or 3E8h-3FFh, 2E8h-2EFh
PS/2 Keyboard/Mouse (KBC)	60h, 64h
Runtime Registers/Power Management Registers	A00h-A80h

Parts of these ranges are not available if a Super I/O is used on the carrier board. If a Super I/O is not implemented on the carrier board then these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 41 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	02h	00h	Internal	VGA Graphics
00h	03h	00h	Internal	ISP Camera
00h	0Bh	00h	Internal	Power Management (P-Unit)
00h	10h	00h	Internal	Storage Control Cluster (MMC Port)
00h	11h	00h	Internal	Storage Control Cluster (SDIO Port)
00h	12h	00h	Internal	Storage Control Cluster (SD Port)
00h	13h	00h	Internal	Serial ATA (SATA) controller
00h	14h	00h	Internal	XHCI USB Controller
00h	15h	00h	Internal	Low Power Engine
00h	18h	00h	Internal	Serial I/O DMA Controller #1
00h	18h	01h	Internal	Serial I/O I2C Port 1
00h	18h	02h	Internal	Serial I/O I2C Port 2
00h	18h	03h	Internal	Serial I/O I2C Port 3
00h	18h	04h	Internal	Serial I/O I2C Port 4
00h	18h	05h	Internal	Serial I/O I2C Port 5
00h	18h	06h	Internal	Serial I/O I2C Port 6

00h	18h	07h	Internal	Serial I/O I2C Port 7
00h	1Ah	00h	Internal	Trusted Execution Engine
00h	1Bh	00h	Internal	HD Audio
00h	1Ch	00h	Internal	PCIe Port 1
00h	1Ch	01h	Internal	PCIe Port 2
00h	1Ch	02h	Internal	PCIe Port 3
00h	1Ch	03h	Internal	PCIe Port 4
00h	1Eh	00h	Internal	Serial I/O DMA Controller #2
00h	1Eh	03h	Internal	High Speed UART Port 1 (HSUART)
00h	1Eh	04h	Internal	High Speed UART Port 2 (HSUART)
00h	1Fh	00h	Internal	LPC
00h	1Fh	03h	Internal	SMBUS

Note

1. *The PCI Express Ports are visible only if a device is attached behind them to the PCI Express Slot on the carrier board*

2. *The Table represents a case when a Single function PCI/PCIe device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

9.3 PCI Interrupt Routing Map

Table 42 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line[1]	APIC Mode IRQ	Intel Graphics	Image Signal Processor (ISP) Camera[6]	Power Management Unit (PUNIT)	Storage Control Cluster (MMC Port)	Storage Control Cluster (SDIO Port)	Storage Control Cluster (SD Port)	Serial ATA (SATA) Controller	XHCI Usb Controller	Low Power Audio Engine
A	INTA	16	X			X					
B	INTB	17		X			X				
C	INTC	18						X			x
D	INTD	19							X		
E		20								X	
F		21			X						X
G		22							x		
H		23									

PIRQ	Serial I/O DMA Controller #1	Serial I/O I2C Port 3	Serial I/O I2C Port 4	Serial I/O I2C Port 4	HD Audio	PCIe Port 1	PCIe Port 2	PCIe Port 3	PCIe Port 4
A						X[4]	X[3]	X[2]	X[5]
B	X					X[5]	X[4]	X[3]	X[2]
C		X				X[2]	X[5]	X[4]	X[3]
D			X			X[3]	X[2]	X[5]	X[4]
E									
F				X					
G					X				
H									

PIRQ	Serial I/O DMA Controller #2	High Speed UART Port 1 (HSUART)	High Speed UART Port 2 (HSUART)	LPC Bridge	SMBUS	I211 Gigabit Ethernet
A						X
B						X
C		X			X	X
D	X		X			X
E						
F						
G						
H						

Note

[1] These interrupt lines are virtual (message based).

[2] Interrupt used by single function PCI Express devices (INTA).

[3] Interrupt used by multifunction PCI Express devices (INTB).

[4] Interrupt used by multifunction PCI Express devices (INTC).

[5] Interrupt used by multifunction PCI Express devices (INTD).

[6] The MA4 does not support the ISP Camera.

9.4 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.5 SM Bus

System Management (SM) bus signals are connected to the Intel Brawell SoC, and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject please contact congatec technical support.

10 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

10.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

10.1.1 Boot Selection Popup

Press the <F11> key during POST to access the Boot Selection Popup menu. A selection menu displays immediately after POST, allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

10.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar, left frame and right frame. The menu bar is shown below:

Main Advanced Chipset Boot Security Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

10.3 Main Setup Screen

When you first enter the BIOS setup, you will see the main setup screen. The main setup screen reports BIOS, processor, memory and board information and is for configuring the system date and time. You can always return to the main setup screen by selecting the 'Main' tab.

Feature	Options	Description
Main BIOS Version	No option	Displays the main BIOS version.
OEM BIOS Version	No option	Displays the additional OEM BIOS version.
Build Date	No option	Displays the date the BIOS was built.
Product Revision	No option	Displays the hardware revision of the board.
Serial Number	No option	Displays the serial number of the board.
BC Firmware Revision	No option	Displays the firmware revision of the congatec board controller.
MAC Address	No option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	No option	Displays the number of boot-ups. (max. 16777215).
Running Time	No option	Displays the time the board is running [in hours max. 65535].
Access Level	No option	Display the privileged level of the user.
Microcode Patch	No option	Displays the processor microcode revision.
Total Memory	No option	Total amount of low voltage DDR3 present on the system.
Intel (R) GOP Driver	No option	Displays the GOP Driver version.
Sec RC Version	No option	Displays the Sec revision.
TXE FW Version	No option	Displays the Trusted Execution Environment firmware revision.
System Language	English	System default language.
System Date	Day of week, month/day/year	Specifies the current system date. **Note:** The date is in month/day/year format.
System Time	Hour:Minute:Second	Specifies the current system time. **Note:** The time is in 24 hour format.

10.4 Advanced Setup

Select the advanced tab from the setup menu to enter the advanced BIOS setup screen. The menu is used for setting advanced features and only features described within this user's guide are listed.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Watchdog				
	Hardware Health Monitoring				
	Graphics				
	Intel(R) I211 Gigabit Network Connection				
	Driver Health				
	Trusted Computing				
	RTC Wake				
	Module Serial Ports				
	Reserve Legacy Interrupt				
	ACPI				
	SCH3116 Super IO Configuration				
	Serial Port Console Redirection				
	CPU				
	PPM Configuration				
	Thermal Configuration				
	SATA				
	LPSS & SCC Configuration				
	PCI & PCI Express				
	UEFI Network Stack				
	CSM & Option ROM Control				
	Info Report Configuration				
	NVMe Configuration				
	SDIO Configuration				
	USB				
	Platform Trust Technology				
	Security Configuration				
	IntelMRT Configuration				
	PC Speaker				
	Driver Health				

10.4.1 Watchdog Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup of the boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One-time Trigger Single Event Repeated Event	Select the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to 'One-time Trigger' the watchdog will be disabled after the first trigger. If set to 'Single Event', every stage will be executed only once, then the watchdog will be disabled. If set to 'Repeated Event' the last stage will be executed repeatedly until a reset occurs.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Select the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event, see note below.
Event 2	**Disabled** ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 3 is reached.

Feature	Options	Description
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Select the timeout value for the first stage watchdog event.
Timeout 2	See above	Select the timeout value for the second stage watchdog event.
Timeout 3	See above	Select the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

In ACPI mode, it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

10.4.2 Hardware Health Monitoring

Feature	Options	Description
CPU Temperature	No option	Displays the actual CPU Temperature in °C.
Board Temperature	No option	Displays the actual Board Temperature in °C
5V Standard	No option	Displays the actual voltage of the 5V standard power supply.
5V Standby	No option	Displays the actual voltage of the 5V standby power supply.
Input Current (5V Standard)	No option	Displays the actual current of the 5V Standard power supply.
CPU Fan Speed	No option	Displays the actual CPU Fan Speed in RPM.
Fan PWM Frequency Mode	Low Frequency **High Frequency**	Select fan PWM base frequency mode. Low frequency: 35.3Hz High frequency: 22.5kHz
Fan PWM Frequency (kHz)	Default: **31** 1 - 63	Select fan PWM base (1kHz-63kHz) (Only visible in high frequency mode)

Feature	Options	Description
Fan PWM Speed Settings	0% 10% 25% 40% 50% 60% 75% 90% **100%**	Boot up fan speed in percent of the maximum supported speed.

10.4.3 Graphics Submenu

Feature	Options	Description
Active LFP Configuration	No Local Flat Panel **Integrated LVDS**	Select the active local flat panel configuration.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel . Only if no external EDID data set can be found, the data set selected under 'Local Flat Panel Type' will be used as fallback data set.
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x18 (01Fh) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x800 1x18 (01Eh) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 2x24 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detects and configures the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. **Note:** Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.
Backlight Inverter Type	None **PWM** I2C	Select the type of backlight inverter used. PWM = Use IGD PWM signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.

Feature	Options	Description
PWM Inverter Polarity	**Normal** Inverted	Select PWM inverter polarity. Only visible if Backlight Inverter Type is set to PWM.
PWM Inverter Frequency (Hz)	**200** - 40000	Set the PWM inverter frequency in Hz. Only visible if Backlight Inverter Type is set to PWM.
Backlight Setting	0% 10% 25% 40% 50% 60% 75% 90% **100%**	Actual backlight value in percent of the maximum setting.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Force LVDS Backlight	**No** Yes	Force LVDS Enable and LVDS VDD Signals unconditionally
LVDS SSC	**Disabled** 0.5% 1.0% 1.5% 2.0% 2.5%	Configure LVDS spread spectrum clock modulation depth. Using center spreading and a fixed modulation frequency of 32.9 kHz.
Digital Display Interface 1	**Auto-Selection** Disabled DisplayPort HDMI/DVI	Select output type of the digital display interface.

10.4.4 Intel® I211Gigabit Network Connection

Feature	Options	Description
► NIC Configuration	Submenu	Configure Boot Protocol, Wake on LAN, Link Speed, and VLAN.
Blink LEDs	**0**	Identify the physical network port by blinking the associated LED.
UEFI Driver	No option	Shows UEFI Driver name.
Adapter PBA	No option	Shows Adapter PBA.
Chip Type	No option	Shows Chip Type.
PCI Device ID	No option	Shows PCI Device ID.
Bus:Device:Function	No option	
Link Status	**Disconnected**	Shows Link Status.

Feature	Options	Description
MAC Address	No option	Shows MAC Address.

10.4.4.1 NIC Configuration

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake On LAN	**Enabled** Disabled	Enables the server to be powered on using an in-band magic packet.

10.4.5 Driver Health Submenu

Feature	Options	Description
► Intel(R) PRO/1000	No option	Provides Health Status for the drivers/Controllers connected to the System

10.4.6 Trusted Computing Submenu

Feature	Options	Description
Security Device Support	Disabled **Enabled**	Enable or disable TPM support. System reset is required after change.
User Confirmation	Disabled **Enabled**	Enable or disable user confirmation requests for certain transactions.
TPM State	**Disabled** Enabled	Enable or disable TPM chip. **Note:** System might restart several times during POST to acquire target state.
Pending operation	**None** Enable Take Ownership Disable Take Ownership TPM Clear	Perform selected TPM chip operation. **Note:** System might restart several times during POST to perform selected operation.

10.4.7 RTC Wake Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour	**0** - 23	Specify wake up hour. For example, enter "3" for 3am and "15" for 3pm.
Wake up minute	**0** - 59	Specify wake up minute.
Wake up second	**0** - 59	Specify wake up second.

10.4.8 Module Serial Ports Submenu

Feature	Options	Description
Serial Port 0	**Disabled** Enabled in PCI Mode Enabled in ACPI mode	Enable or Disable module Serial Port 0. PCI mode is used for legacy operating systems (Windows 7, Linux Distributions). ACPI mode is used for Android, Windows 8/8.1, Windows 10.
Serial Port 1	**Disabled** Enabled in PCI Mode Enabled in ACPI mode	Enable or Disable module Serial Port 0. PCI mode is used for legacy operating systems (Windows 7, Linux Distributions). ACPI mode is used for Android, Windows 8/8.1, Windows 10.

10.4.9 Reserve Legacy Interrupt Submenu

Feature	Options	Description
Reserve Legacy Interrupt 1/2/3	**None** IRQ3 IRQ4 IRQ5 IRQ6 IRQ10 IRQ11 IRQ14 IRQ15	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.

10.4.10 ACPI Submenu

Feature	Options	Description
Enable ACPI Auto Configuration	**Disabled** Enabled	Enable or disable BIOS ACPI Auto Configuration
Enable Hibernation	Disabled **Enabled**	Enable or disable system's ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.

Feature	Options	Description
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend.
Lock Legacy Resources	**Disabled** Enabled	Enable or disable locking of legacy resources.
LID Support	Disabled **Enabled**	Activate ACPI LID button support
Sleep Button Support	Disabled **Enabled**	Activate ACPI sleep button support

10.4.11 SCH3116 Super IO Configuration

Feature	Options	Description
Super IO Chip	No option	Shows Super IO Chip.
▶Serial Port 1 Configuration	Submenu	
▶Serial Port 2 Configuration	Submenu	
▶Parallel Port Configuration	Submenu	

Note

In ACPI mode, it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec

10.4.11.1 Serial Port 1 Configuration

Feature	Options	Description
Serial Port	Disabled **Enabled**	Enable or disable Serial Port (COM).
Device Settings	No option	

Change Settings	**Auto**
	IO=3F8h; IRQ=4 ;
	IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=2E8; IRQ=3,4,5,6,7,9,10,11,12;	

10.4.11.2 Serial Port 2 Configuration

Feature	Options	Description
Serial Port	**Enable** Disable	Enable or disable Serial Port (COM).

Feature	Options	Description
Device Settings	No option	

Change Settings	**Use Automatic Settings**
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12;
		Serial Port 2 configuration options.

Device Mode	**Standard Serial Port Mode** Standard Serial Port Mode IrDA Active Mode ASKIR Mode	Change the Serial Port mode.

10.4.11.3 Parallel Port Configuration

Feature	Options	Description
Parallel Port	Enabled **Disabled**	Enable or disable Parallel Port (LPT/LPTE).
Device Settings	No option	

Change Settings	**Auto**
	IO=378h; IRQ=5;
	IO=378h; IRQ=5,6,7,9,10,11,12;
	IO=278h; IRQ=5,6,7,9,10,11,12;
	IO=3BCh; IRQ=5,6,7,9,10,11,12;
	
	Auto
	IO=378h; IRQ=5; DMA=3;
	IO=378h; IRQ=5,6,7,9,10,11,12; DMA=1,3;
	IO=278h; IRQ=5,6,7,9,10,11,12; DMA=1,3;
	IO=3BCh; IRQ=5,6,7,9,10,11,12; DMA=1,3;
		Serial Port 2 configuration options.
		
		First set of options for EPP or EPP modes.
		
		Second set of options are when ECP modes are selected.

Device Mode	**Standard Printer Mode** SPP Mode EPP-1.9 and SPP Mode EPP-1.7 and SPP Mode ECP Mode ECP and EPP 1.9 Mode ECP and EPP 1.7 Mode	Change the Serial Port mode.

10.4.12 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
▶Console Redirection Settings	submenu	Opens console redirection configuration sub menu.
COM1 Console Redirection	**Disabled** Enabled	Enable or disable serial port 1 console redirection.
▶Console Redirection Settings	Submenu	Opens console redirection configuration sub menu.
COM2 (PC Bus0, Device30, Function3) Console Redirection	**Disabled** Enabled	Enable or disable console redirection for Module Serial Port 0. Only available when Module Serial Port 0 is enabled.
▶Console Redirection Settings	Submenu	Opens console redirection configuration sub menu.
COM2 (PC Bus0, Device30, Function4) Console Redirection	**Disabled** Enabled	Enable or disable console redirection for Module Serial Port 1. Only available when Module Serial Port 1 is enabled.
▶Console Redirection Settings	Submenu	Opens console redirection configuration sub menu.
▶Legacy Console Redirection Settings	Submenu	Legacy Console Redirection Settings
Serial Port for Out-of-Band Management/ EMS Console Redirection	**Disabled** Enabled	Enable or disable Serial Port for Out-of-Band Management/ Windows Emergency Management Services
▶Console Redirection Settings	Submenu	Opens console redirection configuration sub menu.

10.4.12.1 Console Redirection Settings Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select the COM port that legacy serial redirection will be displayed on (DOS).
Baudrate	9600 19200 38400 57600 **115200**	Select baud rate.
Data Bits	7 **8**	Set number of data bits.

Feature	Options	Description
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Enabled** Disabled	If BootLoader is selected then Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legacy console redirection is enable for Legacy OS.

10.4.12.2 Legacy Console Redirection Settings

Feature	Options	Description

Legacy Serial Redirection Port	**COM0**
	COM1
	COM2(PCI Bus0,Dev30,Func3)
	COM3(PCI Bus0,Dev30,Func4)
		Select terminal type.

10.4.12.3 Console Redirection Settings Out-of-Band Management Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ **VT-UTF8** ANSI	Select terminal type.
Baudrate	9600 19200 38400 57600 **115200**	Select baud rate.
Flow Control	**None** Hardware RTS/CTS Sotware Xon/Xoff	
Data Bits	**8**	Set number of data bits.
Parity	**None**	Select parity.
Stop Bits	**1**	Set number of stop bits.

10.4.13 CPU Configuration Submenu

Feature	Options	Description
▶Socket 0 CPU Information	Submenu	Socket Specific CPU Information
CPU Speed	No Option	CPU Clock Frequency
64-bit	No Option	64-Bit support information
Limit CPUID Maximum	**Disabled** Enabled	When enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When disabled, the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Bi-directional PROCHOT	Disabled **Enabled**	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor.
Intel Virtualization Technology	Disabled **Enabled**	Enable or disable support for the Intel virtualization technology.
Power Technology	Disable **Energy Efficient** Custom	Configure the Power technology schema for the CPU.

10.4.13.1 Socket 0 CPU Information Submenu

Feature	Options	Description
CPU Name	No option	Displays socket specific CPU name.
CPU Signature	No option	Displays CPU signature number.
Microcode Patch	No option	Displays the CPU microcode patch number.
Max. CPU Speed	No option	Displays the maximal CPU clock frequency.
Min. CPU Speed	No option	Displays the minimal CPU clock frequency.
Processor Cores	No option	Displays the number of CPU core on Socket CPU.
Intel HT Technology	No option	Displays the Intel HT Technology support information.
Intel VT-x Technology	No option	Displays the Intel VT-x Technology support information.
L1 Data Cache	No option	Displays the Socket L1 data cache information.
L1 Code Cache	No option	Displays the Socket L1 code cache information.
L2 Cache	No option	Displays the Socket L2 data cache information.
L3 Cache	No option	Displays the Socket L3 data cache information.

10.4.14 PPM Configuration Submenu

Feature	Options	Description
EIST	Disabled **Enabled**	Enable or disable Enhanced Intel SpeedStep Technology (EIST).
CPU C state Report	Disabled **Enabled**	Enable/Disable CPU state Report to Operating System.
Max CPU C state	C7 C6 **C1**	Maximal CPU C state supported by the CPU
SOix	**Disabled** Enabled	Enable/Disable CPU SOix state support

10.4.15 Thermal Configuration

Feature	Options	Description
DTS	Enabled **Disabled**	Enable/Disable Digital Thermal Sensor
Critical Trip Point	Default: **95** 0 - 110	Temperature of the ACPI critical Trip Point in which the OS will shut the system off.

Feature	Options	Description
OS Hibernate Temperature	Default: **85** 0 - 110	The temperature that should cause the OS to trigger the system to hibernate.
Passive Trip Point	Default: **85** 0 - 110	Temperature of the ACPI passive Trip Point in which the OS will begin throttling the processor.
Full Speed Fan Trip Point	Default: **80** 0 - 90	Temperature at which the fan device will be activated at full speed.
Half Speed Fan Trip Point	Default: **60** 0 - 90	Temperature at which the fan device will be activated at half speed.
Fan Hysteresis	0 - **7**	The number of degrees below the fan activation threshold that must be reached before turning off the fan.

10.4.16 SATA

Feature	Options	Description
STAT Controller	**Enabled** Disabled	Enable/Disable SATA Device.
SATA Mode Selection	**AHCI**	Determines how SATA controller operates.
SATA Interface Speed	Gen1 **Gen2** Gen3	Select SATA Interface Speed, CHV A1 always with Gen1 Speed.
SATA Test Mode	Enabled **Disabled**	Test Mode.
Aggressive LPM Support	**Enabled** Disabled	Enable PCH to aggressively enter link power state.
►Software Feature Mask Configuration	Submenu	
SATA Port 0	**Enabled** Disabled	Enable/Disable SATA Port.
Spin Up Device	Enabled **Disabled**	If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
Device Sleep Support	Enabled **Disabled**	Enable/Disable Device Sleep Support on that port.
SATA Port 1	**Enabled** Disabled	Enable/Disable SATA Port.
Spin Up Device	Enabled **Disabled**	If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
Device Sleep Support	Enabled **Disabled**	Enable/Disable Device Sleep Support on that port.

10.4.16.1 Software Feature Mask

Feature	Options	Description
HDD Unlock	**Enabled** Disabled	If enabled, indicates that the HDD password unlock in the OS is enabled.
LED Locate	**Enabled** Disabled	If enabled indicates that the LED/SGPIO hardware is attached and ping to locate feature is enable on the OS.

10.4.17 LPSS & SCC Configuration Submenu

Feature	Options	Description
SCC eMMC Support	**ACPI Mode** PCI Mode Disabled	SCC eMMC Support Enable/Disable.
eMMC Secure Erase	Enabled **Disabled**	Enable eMMC secure erase support.
SCC SD Card Support (D18:F0)	**ACPI Mode** PCI Mode Disabled	SCC SD Card Support Enable/Disable.
SD Card 1.8v Switching Delay	**0** - 999 ms	Set SD Card 1.8v Switching Delay.
SD Card 3.3v Discharge Delay	Default: **250** 0 - 999 ms	Set SD Card 3.3v Discharge Delay.
LPSS with GPIO Devices Support	Disabled **Enabled**	Enable/Disable GPIO ACPI Devices Support, disable it will disable all LPSS devices.
LPSS DMA #1	**ACPI Mode** PCI Mode Disabled	Enable/Disable LPSS DMA #1 Support.
LPSS HSUART #1	**ACPI Mode** PCI Mode Disabled	Enable/Disable LPSS HSUART #1 Support. **Note:** LPSS HSUART #1 will not be visiable to an legacy OS unless LPSS DMA#1 is in the same mode.
LPSS HSUART #2	**ACPI Mode** PCI Mode Disabled	Enable/Disable LPSS HSUART #1 Support. **Note:** LPSS HSUART #1 will not be visiable to an legacy OS unless LPSS DMA#1 is in the same mode.

10.4.18 PCI & PCI Express

Feature	Options	Description
PCI Bus Driver Version	No option	Shows PCI Bus Driver Version.

Feature	Options	Description
PCI Latency Timer	**32 PCI Bus Clocks** 64 PCI Bus Clocks 96 PCI Bus Clocks 128 PCI Bus Clocks 160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	Value to be programmed into PCI latency timer register.
PCI-X Latency Timer	32 PCI Bus Clocks **64 PCI Bus Clocks** 96 PCI Bus Clocks 128 PCI Bus Clocks 160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	Value to be programmed into PCI latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or Disable VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate SERR#.
Above 4G Decoding	**Disabled** Enabled	Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).
Don't Reset VC-TC Mapping	**Disabled** **Enabled**	If system has Virtual Channels, Software can reset Traffic Class mapping through Virtual Channels, to its default state. Setting this option to Enabled will not modify VC Resources.

10.4.19 UEFI Network Stack

Feature	Options	Description
Network Stack	Enabled **Disabled**	Enable or disable the UEFI network stack.
IPv4 PXE Support	**Enabled** Disabled	Enable IPv4 PXE boot support. If disabled IPv6 PXE boot option will not be created.
IPv6 PXE Support	**Enabled** Disabled	Enable IPv4 PXE boot support. If disabled IPv6 PXE boot option will not be created.
PXE boot wait time	**0** - 5	Wait time to press ESC to abort PXE Boot.
Media detect count	**1** - 50	Number of times presence of media will be checked.

10.4.20 CSM & Option ROM Control Submenu

Feature	Options	Description
CSM Support	**Enabled** Disabled	Enable the Compatibility Support Module.
CSM16 Module Version	No option	Display CSM Module Version number.
Gate A20 Active	**Upon Request** Always	Configure legacy Gate A behavior.
Option ROM Messages	**Force BIOS** Keep Current	Enable Option ROM message
INT19 Trap Response	**Immediate** Postponed	Define BIOS reaction on INT19 trapping by Option ROM: Immediate executes the trap right away. Postpone executes the trap during legacy boot.
Boot Option Filter	**UEFI and Legacy** Legacy Only UEFI Only	Controls which devices / boot loaders the system should boot to.
Network	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and legacy Network option ROMs.
Storage	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and legacy Storage option ROMs.
Video	Do not launch UEFI only **Legacy only**	Controls the execution of UEFI and legacy Video option ROMs
Other PCI Devices	**UEFI only** Legacy only Do not launch	Controls the execution of UEFI and legacy option ROMs for any other PCI device different to Network, Video and Storage.

10.4.21 Info Report Configuration

Feature	Options	Description
POST Report	**Disabled** Enabled	POST Report Support Enabled/Disabled.
Delay Time	0..10 Until Press ESC	POST Report wait time from 0 to 10 seconds or until Press ESC Key.
Error Message Report	**Disabled** Enabled	Error Message Support Enabled/Disabled.
Summary Screen	**Disabled** Enabled	Summary Screen Support Enabled/Disabled.
Delay Time	0..10 Until Press ESC	Summary Screen wat time from 0 to 10 seconds or until Press ESC Key.

10.4.22 NVMe Configuration

Feature	Options	Description
NVMe controller and Drive Information	No Option	

10.4.23 SDIO Configuration

Feature	Options	Description
SDIO Access Mode	**Auto** ADMA SDMA PIO	Select the mode used to access the SD card.

10.4.24 USB Submenu

Feature	Options	Description
USB Module Version	No option	
USB Controllers	No option	
USB Devices	No option	Displays the detected USB devices.
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and BIOS setup.
xHCI Hand-off	Enabled **Disabled**	This is a workaround for OSes without xHCI hand-off support. The xHCI ownership change should be claimed by xHCI OS driver. Not displayed on BS/BP77.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable Mass Storage Driver Support.
Port 60/64 Emulation	Disabled **Enabled**	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.
USB Transfer Timeout	1 sec 5 sec 10 sec **20 sec**	The timeout value for control, bulk, and interrupt transfers.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device start unit command timeout.
Device Power-Up Delay Selection	**Auto** Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.

Feature	Options	Description
Device Power-Up Delay Value	Default: **5** 0 - 40	Actual power-up delay value in seconds.
SanDisk Cruzer Micro 8.01	**Auto** Floppy Forced FDD Hard Disk CD-Rom	Mass storage device emulation type. 'Auto' enumerates devices according to their media format. Optical drives are emulated as 'CDROM', drives with no media will be emulated according to a drive type.

10.4.25 Platform Trust Technology

Feature	Options	Description
fTPM	**Disabled** Enabled	Enable Trusted Platform Module support.

10.4.26 Security Configuration

Feature	Options	Description
TXE HMRFPO	Enabled **Disabled**	Enable Host ME Region Flash Protection Overwrite.
TXE Firmware Update	**Enabled** Disabled	Enable Firmware update.
TXE EOP Message	**Enabled** Disabled	Enable TXE End of Post Message.

10.4.27 IntelRMT Configuration Submenu

Feature	Options	Description
Intel RMT Support	**Disabled** Enabled	Intel RMT (Ready Mode Technology) SSDT table will be loaded if enabled

10.4.28 PC Speaker Submenu

Feature	Options	Description
Debug Beeps	Disabled **Enabled**	Enable or Disable general debug / status beep generation.

Feature	Options	Description
Input Device Debug Beeps	**Disabled** Enabled	Enable or Disable input device debug beep generation.
Output Device Debug Beeps	**Disabled** Enabled	Enable or Disable output device debug beep generation.
USB Driver Beeps	**Disabled** Enabled	Enable or disable USB driver beeps.

10.5 Chipset Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.5.1 Processor (Integrated Components) Submenu

Feature	Options	Description
►Intel IGD Configuration	Submenu	
►Graphics Power Management Control	Submenu	
►Memory Configuration Options	Submenu	
Total Memory	No option	Total amount of memory detected by the system
Memory Slot 0	No option	Memory detected by the system on Slot 0
Memory Slot 1	No option	Memory detected by the system on Slot 1
Max TOLUD	**2 GB** 3 GB	Maximum value of TOLUD Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

10.5.1.1 Intel IGD Configuration Submenu

Feature	Options	Description
Internal Graphics Device	**Enabled** Disabled	Keep Internal Graphics Device (IGD) enabled based on the setup options.
IGD Turbo	**Auto** Enabled Disabled	Select the IGD Turbo feature, if Auto is selected, IGD Turbo will only be enabled when SOC steeping is B0 or above.
GFX Boost	Enabled **Disabled**	Enable or disable GFX Boost.
PAVC	Disabled **Enabled**	Enable or disable Protected Audio Video Control.

Feature	Options	Description
PR3	Disabled **Enabled**	Enable or disable PR3 (for Win 10 only).
DVMT Pre-Allocated	**32M** 64M 96M 128M 160M 192M 224M 256M 288M 320M 352M 384M 416M 448M 480M 512M	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
DVMT Total Gfx Mem	128MB **256MB** Max	Select DVMT 5.0 Total Graphic Memory size used by the Internal Graphics Device.
Aperture Size	128MB **256MB** 512MB	Select the Aperture Size.
GTT Size	2MB **4MB** 8MB	Select the GTT Size.
IGD Thermal	Enabled **Disabled**	Enable/Disable IGD Thermal.
Spread Spectrum clock	**Enabled** Disabled	Enable/Disable Spread Spectrum clock.
WOPCMSZ	**1MB** 2MB 4MB 8MB	Select the size for WOPCMSZ.
ISP Enable/Disable	**Enabled** Disabled	Enable/Disable ISP PCI Device Selection.
ISP PCI Device Selection	ISP PCI Device as B0D2F0 **ISP PCI Device as B0D3F0** ISP PCI Device as B0D3F0 with Virtual ISP B0D2F0	Default ISP is PCI B0D2F0 for Windows Boot. Linux Boot to select B0D3F0.
PUNIT Power Configuration	Disabled **Enabled**	Enable or disable Punit Power configuration.

Feature	Options	Description
Svid Configuration	**Platform Defaults** Svid Config 0 Svid Config 1 Svid Config 3 Svid Config 4 BSW I2C PMIC Config	Choose the right SVID Config.

10.5.1.2 Graphics Power Management Control Submenu

Feature	Options	Description
RC6 (Render Standby)	**Enabled** Disabled	Check to enable render standby support.
Power Meter Lock	**Enabled** Disabled	Enable or disable Power Meter Lock.

10.5.1.3 Memory Configuration Options Submenu

Feature	Options	Description
Rank Margin Tool EV Mode	**Disabled** Enabled	Enable or disable Rank Margin Tool print out message support.
DDR DVFS	Disabled **Enabled**	Enable or disable DDR Dynamic Voltage and Frequency Scaling in MRC.
Memory Frequency Override	**Disabled** Enabled	Allows override of memory frequency parameters that are automatically obtained from DDR3 DIMM SPD. May cause memory instability if the selected frequency is not supported by the memory device. This option has no effect on systems configured without 'UseDimmSpd' option.

Frequency A selection	Auto
	800
	1067
	1600
	800(SKU333)
	1000(SKU333)
	1333(SKU333)
	900(SKU360)
	1800(SKU360)
	933(SKU373)
	1866(SKU373)
		Frequency A selection.

Feature	Options	Description

Frequency B selection	Auto
	1067
	800(SKU333)
	1000(SKU333)
	900(SKU360)
	933(SKU373)
		Option to select Frequency B (Min DDR DVFS Frequency).

Auto Detect LPDDR3 DRAM	Disabled **Enabled**	Enable or disable automatic detection of LPDDR3 DRAM parameters.
LPDDR3 Chip Select	**1 Rank** 2 Ranks	LPDDR3 Chip Select (Number of Rank) Configuration. Auto Detect must be disabled to use this option.
Channel selection	Auto **Single** Dual	Select number of channels.
Channel Selection Bit 3:0	0 1 **2** 3 4 5 6 7 8 9 A B C D E F	

Feature	Options	Description
Channel Selection 4	0 **1** 2 3 4 5 6 7 8 9 A B C D E F	BMISC Channel select 4 for channel hashing.
Bank Address Hashing	Disabled **Enabled**	Enable or disable Bank Address Hashing.
Rank Select Interleaving	Disabled **Enabled**	Enable or disable Rank Select Interleaving.
Dynamic Self Refresh	Disabled **Enabled**	Enable or disable PUNIT driven DUNIT DDR dynamic self refresh.
DRAM PM5	Disabled **Enabled**	Enable or disable DRAM PM5 PUNIT configuration.
DDR3 2N Mode	Disabled **Enabled**	Set the DDR3 mode to 2N. 1N mode is used by default.
RX Power Training	Disabled **Enabled**	Enable or disable RX Power Training.
TX Power Training	Disabled **Enabled**	Enable or disable TX Power Training.
MRC Fast Boot	Disabled **Enabled**	Enable or disable MRC fast Boot. Forces MRC training to occur when disabled.
Scrambler	Disabled **Enabled**	Enable or disable Scrambler.
DRP Lock	Disabled **Enabled**	DRP Lock.
REUT Lock	Disabled **Enabled**	REUT Lock.
RH Prevention	**Disabled** Enabled	Prevents Row Hammer attacks by increasing the average time between sending REF commands to DRAM.

10.5.2 Platform Controller Hub (PCH) Submenu

Feature	Options	Description
▶Security Configuration	Submenu	Security Configuration settings.
▶Azalia Configuration	Submenu	Azalia HD Audio Submenu.
▶ USB Configuration	Submenu	USB Submenu.
▶ PCI Express Configuration	Submenu	PCI Express Configuration Submenu.
Serial IRQ Mode	Quiet **Continuous**	Configure IRQ Serial Mode
Isolate SMBus Segments	**Never** During POST Always	Allows to isolate the off-module/external SMBus segment from the on-module SMBus segment. This can be a workaround for non spec conform external SMBus devices.

10.5.2.1 Security Configuration

Feature	Options	Description
RTC Lock	Disabled **Enabled**	Enable or disable bytes 38h-3Fh in the upper and lower 128-byte bank of RTC RAM lockdown.
Global SMI Lock	**Enabled** Disabled	Enable or disable SMI lock.

10.5.2.2 Azalia HD Audio

Feature	Options	Description
LPE Audio Support	**Disabled** PCI Mode ACPI Mode	Enable LPE Audio Support.
Audio Controller	**Enabled** Disabled	Enable Audio Controller.
Azalia Vci Enable	**Enabled** Disabled	Enable Azalia Vci.
Azalia Docking Support Enable	Enabled **Disable**	Enable Azalia Docking support.
Azalia PME Enable	**Enabled** Disabled	Enable Azalia PME support.
Azalia HDMI Codec	**Enabled** Disabled	Enable Azalia HDMI Codec
HDMI Port B	**Enabled** Disabled	Enable HDMI Port B Audio.

Feature	Options	Description
HDMI Port C	**Enabled** Disabled	Enable HDMI Port C Audio.
HDMI Port D	**Enabled** Disabled	Enable HDMI Port D Audio.

10.5.2.3 USB Configuration Submenu

Feature	Options	Description
XHCI Mode	**Enable** Disable	Mode of operation of xHCI controller.
SSIC Support Enable	**Disabled** Enabled	Enable or disable SSIC support.
SSIC Init Sequence	**SSIC Initialization Sequence 1** SSIC Initialization Sequence 2	Sequence 1: Windows; Sequence 2: Android.
SSIC Port 1	Enabled **Disabled**	Enables or disables SSIC Port 1.
SSIC Port 2	Enabled **Disabled**	Enables or disables SSIC Port 2.
HSIC Port 1	**Enabled** Disabled	Enables or disables HSIC Port 1.
HSIC Port 2	**Enabled** Disabled	Enables or disables HSIC Port 2.
USB2 PHY Power Gating	**Auto** Disabled Enabled	Configure USB2 PHY Power Gating.
USB3 PHY Power Gating	**Auto** Disabled Enabled	Configure USB3 PHY Power Gating.
USB OTG Support	PCI mode **Disabled**	Enable or disable USB OTG Support.

10.5.2.4 PCI Express Configuration Submenu

Feature	Options	Description
▶PCIE Express Root Port 1	Submenu	
▶PCIE Express Root Port 2	Submenu	
▶PCIE Express Root Port 3	Submenu	
▶PCIE Express Root Port 4	Submenu	
▶PCI Express S0ix Settings	Submenu	

Feature	Options	Description
Native PCI Express Support	Disabled Enabled	Enable or disable native OS PCI Express support.

10.5.2.5 PCI Express Root Port 1,2,3 & 4

Feature	Options	Description
PCI Express Root Port 1	**Enabled** Disabled	Control the PCI Express Root Port.
ASPM	**Auto** Disabled L0s L1 L0sL1	PCI Express Active State Power Management settings.
URR	**Disabled** Enabled	PCI Express Unsupported Request Reporting Enable/Disable.
FER	**Disabled** Enabled	Enable or disable PCI Express device Fatal Error Reporting.
NFER	**Disabled** Enabled	Enable or disable PCI Express device Non-Fatal Error Reporting.
CER	**Disabled** Enabled	Enable or disable PCI Express device Correctable Error Reporting.
SEFE	**Disabled** Enabled	Root PCI Express System Error on Fatal Error Enable/Disable.
SENFE	**Disabled** Enabled	Enable or disable Root PCI Express System Error on Non-Fatal Error.
SECE	**Disabled** Enabled	Root PCI Express System Error on Correctable Error Enable/Disable.
PME SCI	Disabled **Enabled**	Enable or disable PCI Express PME (power management event) SCI.
Ext Sync	**Disabled** Enabled	Enable Express Ext Sync.
PCIe Speed	**Auto** Gen 2 Gen 1	Configure PCIe Speed. CHV A1 always with Gen 1 Speed.
Detect Non-compliant Device	**Disabled** Enabled	Try to detect also a non-compliant PCI Express device. If enabled, it will take more time at POST time.
L1 Substates	Disabled L1.1 L1.2 L1.1 & L1.2	PCI Express L1 Substates settings.

Feature	Options	Description
Non-Common Clock With SSC Enabled Mode	Enabled **Disabled**	Assume the root port is operating at non-common clock with SSC enabled.
Transmitter Half Swing	Enabled **Disabled**	Transmitter Half Swing Enable/Disable.
Tx Eq Deemphasis Selection	3.5dB **6dB**	Select the level of de-dmphasis for an Upstream component.

10.5.2.6 PCI Express S0ix Settings Submenu

Feature	Options	Description
D0 S0ix Policy	**PCIe RC shall be in D3** S0i1 is the deepest S0ix state PCIe RC in in D0 when entering S0ix Reserved	PCIe D0 S0ix Policy.
Evaluate CLKREQ State	**Enabled** Disabled	Enable or disable evaluation of CLKREQ state.
CLKREQ# Enable	**CLKREQ# [0]** CLKREQ# [1] CLKREQ# [2] CLKREQ# [3]	CLKREQ# [x] should be evaluated during PCIe in D0 S0ix entry and exit criteria checking.
S0ix LTR Threshold (Latency Scale)	1ns 32ns **1024ns** 32,768ns 1,048,576ns 33,554,321ns	PCIe S0ix LTR Threshold: Latency Scale.
PCIe LTR Threshold (Latency Value)	**150**	PCIe S0ix LTR Threshold: Latency Value. This value is multiplied by Latency Scale.

10.6 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.6.1 Boot Settings Configuration

Feature	Options	Description
Setup Prompt Timeout	Default: **1** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot (not recommended), 65535 means infinite wait.

Feature	Options	Description
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. **Note:** The default OEM logo is a dark screen.
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The "Device Based" boot priority list allows you to select from a list of currently detected devices only. The "Type Based" boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the "Device Based" boot priority list might change dynamically in cases when devices are physically removed or added to the system. The "Type Based" boot menu is static and can only be changed by the user.
Boot Option Sorting Method	**Legacy First** UEFI First	UEFI First: Try all UEFI boot options before first legacy boot option. Legacy First: Vice versa
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. **Note:** Only works with an ATX type power supply.
AT Shutdown Mode	System Reboot **Hot S5**	Determines the behavior of an AT-powered system after a shutdown.
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
Fast Boot	**Disabled** Enabled	Enable or disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS / legacy boot options.
1st Boot Device	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk **USB CDROM** Other USB Device Onboard LAN External LAN Firmware-based Bootloader Other Device	

Feature	Options	Description
2nd Boot Device	Disabled SATA 0 Drive SATA 1 Drive **USB Harddisk** USB CDROM Other USB Device Onboard LAN External LAN Firmware-based Bootloader Other Device	
3rd Boot Device	Disabled **SATA 0 Drive** SATA 1 Drive USB Harddisk USB CDROM Other USB Device Onboard LAN External LAN Firmware-based Bootloader Other Device	
4th Boot Device	Disabled SATA 0 Drive **SATA 1 Drive** USB Harddisk USB CDROM Other USB Device Onboard LAN External LAN Firmware-based Bootloader Other Device	
5th Boot Device	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk USB CDROM **Other USB Device** Onboard LAN External LAN Firmware-based Bootloader Other Device	

Feature	Options	Description
6th Boot Device	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk USB CDROM Other USB Device Onboard LAN External LAN Firmware-based Bootloader **Other Device**	
7th Boot Device	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk USB CDROM Other USB Device **Onboard LAN** External LAN Firmware-based Bootloader Other Device	
8th Boot Device	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk USB CDROM Other USB Device Onboard LAN External LAN **Firmware-based Bootloader** Other Device	

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

10.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

10.7.1 Security Settings

Feature	Options	Description
BIOS Password	No options	Set BIOS Password.
BIOS Lock	**Enabled** Disabled	Enable or disable the BIOS Lock Enable feature.
BIOS Update and Write Protection	Enabled **Disabled**	Enable or disable BIOS Update
▶Secure Boot Menu	Submenu	Customizable Secure Boot settings.

10.7.1.1 Secure Boot Menu

Feature	Options	Description
System Mode	No options	Shows System Mode.
Secure Boot	No options	Shows Secure Boot status.
Vendor Keys	No options	Shows Vendor Keys status.
Secure Boot	**Disabled** Enabled	Secure Boot can be enabled if the System is running in User mode with enrolled Platform Key(PK) and when CSM function is disabled.
Secure Boot Mode	Standard **Custom**	Secure Boot Mode selection.
▶Key Management	Submenu	

10.7.1.2 Key Management

Feature	Options	Description
Provision Factory Default Keys	**Disabled** Enabled	Install factory default Secure Boot keys when System is in Setup Mode.
▶Enroll all Factory Default Keys		Force System to User Mode and install all Factory Default keys.
▶Platform Key(PK)		
▶Key Exchange Keys		
▶Authorized Signatures		
▶Forbidden Signatures		
▶Authorized TimeStamps		

10.7.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

10.8 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen. You can display a Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
Boot Override	
List of all boot devices currently detected	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to "Device Based".

11 Additional BIOS Features

The conga-MA4 uses a congatec/AMI AptioEFI that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility (version 1.5.0 and later), which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as MA40R1xx. R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

The binary size of MA40R1xx is 8MB.

Note

While some of the variants of the MA4 have single channel memory and others have dual channel memory (see section 2.5.x), the same BIOS will work on all varants of the MA4.

11.1 Supported Flash Devices

The conga-MA4 supports the following flash device:

- Winbond W25Q64FVSSIG (8MB)

The flash device listed above has been tested and can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.

11.2 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

12 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Table 43 Industry Specifications

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.3	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0	http://www.serialata.org
PICMG® COM Express Module™ Base Specification	http://www.picmg.org/
PCI Express Base Specification, Revision 1.0a	http://www.pcisig.com/specifications