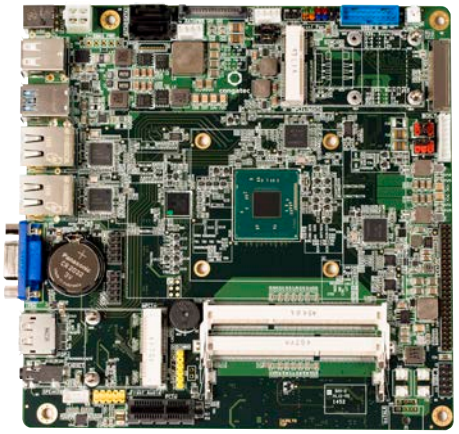


conga-IA3 Thin Mini-ITX SBC

Detailed Description Of The congatec Thin Mini-ITX Based On 3rd Generation Intel Atom/Celeron SoC

User's Guide

Revision 1.2

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2015.04.29	AEM	• Preliminary release
1.0	2016.01.19	AEM	• Corrected the AMI Aptio BIOS version in section 2.1 "Feature List" • Added note about using symmetrical memory modules because of Bay Trail memory limitation • Official release
1.1	2016.04.05	AEM	• Corrected the supported maximum memory capacity from 16 GB to 8 GB • Updated section 4 "Cooling Solution"
1.2	2018.12.07	AEM	• Updated the information about handling electrostatic sensitive devices in preface section • Updated section 5.3.2.3 "Front Panel HD Audio" • Updated section 6.5 "LPC Super I/O Device " • Corrected the jumper and connector table in section 6.5.3" CPU/System Fan Connector & Power Configuration" • Deleted section 9.1 "Supported Flash Devices"

Preface

This user's guide provides information about the components, features and connectors available on the conga-IA3 Thin Mini-ITX Single Board Computer.

Disclaimer

The information contained within this user's guide, including but not limited to any product specification, is subject to change without notice.

congatec AG provides no warranty with regard to this user's guide or any other information contained herein and hereby expressly disclaims any implied warranties of merchantability or fitness for any particular purpose with regard to any of the foregoing. congatec AG assumes no liability for any damages incurred directly or indirectly from any technical or typographical errors or omissions contained herein or for discrepancies between the product and the user's guide. In no event shall congatec AG be liable for any incidental, consequential, special, or exemplary damages, whether based on tort, contract or otherwise, arising out of or in connection with this user's guide or any other information contained herein or the use thereof.

Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Lead-Free Designs (RoHS)

All congatec AG products are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices. They are enclosed in static shielding bags, and shipped enclosed in secondary packaging (protective packaging). The secondary packaging does not provide electrostatic protection.

Do not remove the device from the static shielding bag or handle it, except at an electrostatic-free workstation. Also, do not ship or store electronic devices near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Connector Type

Describes the connector used on the Single Board Computer.

Copyright Notice

congatec AG has made every attempt to ensure that the information in this document is accurate yet the information contained within is supplied "as-is".

Trademarks

Product names, logos, brands, and other trademarks featured or referred to within this user's guide, or the congatec website, are the property of their respective trademark holders. These trademark holders are not affiliated with congatec AG, our products, or our website.

Warranty

congatec AG makes no representation, warranty or guaranty, express or implied regarding the products except its standard form of limited warranty ("Limited Warranty") per the terms and conditions of the congatec entity, which the product is delivered from. These terms and conditions can be downloaded from www.congatec.com. congatec AG may in its sole discretion modify its Limited Warranty at any time and from time to time.

The products may include software. Use of the software is subject to the terms and conditions set out in the respective owner's license agreements, which are available at www.congatec.com and/or upon request.

Beginning on the date of shipment to its direct customer and continuing for the published warranty period, congatec AG represents that the products are new and warrants that each product failing to function properly under normal use, due to a defect in materials or workmanship or due to non conformance to the agreed upon specifications, will be repaired or exchanged, at congatec's option and expense.

Customer will obtain a Return Material Authorization ("RMA") number from congatec AG prior to returning the non conforming product freight prepaid. congatec AG will pay for transporting the repaired or exchanged product to the customer.

Repaired, replaced or exchanged product will be warranted for the repair warranty period in effect as of the date the repaired, exchanged or replaced product is shipped by congatec, or the remainder of the original warranty, whichever is longer. This Limited Warranty extends to congatec's direct customer only and is not assignable or transferable.

Except as set forth in writing in the Limited Warranty, congatec makes no performance representations, warranties, or guarantees, either express or implied, oral or written, with respect to the products, including without limitation any implied warranty (a) of merchantability, (b) of fitness for a particular purpose, or (c) arising from course of performance, course of dealing, or usage of trade.

congatec AG shall in no event be liable to the end user for collateral or consequential damages of any kind. congatec shall not otherwise be liable for loss, damage or expense directly or indirectly arising from the use of the product or from any other cause. The sole and exclusive remedy against congatec, whether a claim sound in contract, warranty, tort or any other legal theory, shall be repair or replacement of the product only.

Certification

congatec AG is certified to DIN EN ISO 9001 standard.

Technical Support

congatec AG technicians and engineers are committed to providing the best possible technical support for our customers so that our products can be easily used and implemented. We request that you first visit our website at www.congatec.com for the latest documentation, utilities and drivers, which have been made available to assist you. If you still require assistance after visiting our website then contact our technical support department by email at support@congatec.com

Terminology

Term	Description
PCI Express (PCIe)	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4 or x16 link.
PCI Express Mini Card	PCI Express Mini Card add-in card is a small size unique form factor optimized for mobile computing platforms.
MMCplus	MMCplus was defined for first time in MMC System Specification v4.0. MMCplus is backward compatible with MMC. MMCplus has 13 pins.
SDIO card	SDIO (Secure Digital Input Output) is a non-volatile memory card format developed for use in portable devices.
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial-interface standard for hard disks
HDA	High Definition Audio
S/PDIF	S/PDIF (Sony/Philips Digital Interconnect Format) specifies a Data Link Layer protocol and choice of Physical Layer specifications for carrying digital audio signals between devices and stereo components.
HDMI	High Definition Multimedia Interface. Supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
LPC	Low Pin-Count: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy device support into a single IC.
I²C Bus	Inter-Integrated Circuit Bus: is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system.
SM Bus	System Management Bus: is a popular derivative of the I²C-bus.
CAN	Controller Area Network
SPI	Serial Peripheral Interface
GBE	Gigabit Ethernet
LVDS	Low-Voltage Differential Signaling
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
PN	Part Number - the part number for placing orders.
N.C	Not connected
N.A	Not available
T.B.D	To be determined

Contents

1 Introduction

1.1 Mini-ITX Concept

The Mini-ITX form factor provides enthusiasts and manufacturers with a standardized ultra compact platform for development. With a footprint of 170mm x170mm, this scalable platform promotes the design of highly integrated, energy efficient systems. Due to its small size, the Mini-ITX form factor enables PC appliance designers not only to design attractive low cost devices but also allows them to explore a huge variety of product development options - from compact space-saving designs to fully functional Information Station and Value PC systems. This helps to reduce product design cycle and encourages rapid innovation in system design, to meet the ever-changing needs of the market.

Additionally, the boards can also be passively cooled, presenting opportunities for fanless designs. The Mini-ITX boards are equipped with various interfaces such as PCI Express, SATA, USB 2.0/3.0, Ethernet, Displays and Audio.

1.2 conga-IA3

The conga-IA3 is a Single Board Computer designed based on the Thin Mini-ITX specification. The conga-IA3 SBC features the Intel 3rd generation Atom/Celeron processors. With maximum 10W TDP processors, the SBC offers Ultra Low Power boards with high computing performance and outstanding graphics. Additionally, the SBC supports dual channel DDR3L up to 1333 MT/s for a maximum system memory capacity of 8 GB, multiple I/O interfaces, up to two independent displays and various congatec embedded features.

With smaller board size and lower height keep-out zones, the conga-IA3 SBC provides manufacturers and enthusiasts with the opportunity to design compact systems for space restricted areas. With appropriate I/O shield, the same conga-IA3 SBC can be used in either a Thin Mini-ITX or a Mini-ITX design.

The various features and capabilities offered by the conga-IA3 makes it ideal for the design of compact, energy efficient, performance-oriented embedded systems.

1.2.1 Options Information

The conga-IA3 is currently available in four variants. This user's guide describes all of these variants. The tables below show the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module

conga-IA3

Part-No.	052300	052301	052310	052311
Processor	Intel® Atom™ E3845 1.91 GHz Quad Core™	Intel® Atom™ E3826 1.46 GHz Dual Core™	Intel® Celeron™ J1900 2.0 GHz Quad Core™	Intel® Celeron™ N2930 1.83 GHz Quad Core™
L2 Cache	2 MByte	1 MByte	2 MByte	2 MByte
Burst Frequency	N/A	N/A	2.41 GHz	2.16 GHz
Memory (DDR3L)	1333 MT/s dual channel	1066 MT/s dual channel	1333 MT/s dual channel	1333 MT/s dual channel
Processor Graphics	Intel® HD Graphics (GT1)	Intel® HD Graphics (GT1)	Intel® HD Graphics (GT1)	Intel® HD Graphics (GT1)
Graphics Base/Burst Freq.	542 / 792 MHz	533 / 667 MHz	688 / 854 MHz	313 / 854 MHz
VGA	No	No	No	No
LVDS	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit
DDI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI	DP / HDMI / DVI
Processor TDP (Max)	10 W	7 W	10 W	7.5 W *

** Scenario Design Power (SDP) of 4.5W*

1.2.2 Optional Accessories/Cables

Accessories	Part No.	Description
conga-IA30/CSP	052351	Passive cooling solution with Thin Mini-ITX height (for conga-IA3)
conga-IA30/Retention Frame	052355	Retention frame for conga-IA3 standard cooling
conga-IA30/IO Bracket Standard Size	052356	IO shield for conga-IA3 with Mini-ITX height
conga-IA30/IO Bracket Thin Size	052357	IO shield for conga-IA3 with Thin Mini-ITX height
DDR3L-SODIMM-1600 (2 GB)	068755	Certified 2 GB DDR3L SODIMM memory module with 1600 MT/s (PC3L-12800S)
DDR3L-SODIMM-1600 (4 GB)	068756	Certified 4 GB DDR3L SODIMM memory module with 1600 MT/s (PC3L-12800S)
DDR3L-SODIMM-1600 (8 GB)	068757	Certified 8 GB DDR3L SODIMM memory module with 1600 MT/s (PC3L-12800S)

Cables	Part No.	Description
cab-ThinMini-ITX-SATA-Power	14000120	Power cable for SATA and micro-SATA devices.
cab-ThinMini-ITX-UART	14000121	UART cable with 2x5 pin female housing and D-Sub Male connector.
cab-ThinMini-ITX-USB2.0-Single	14000122	USB 2.0 cable with 1x5 pin female housing and USB 2.0 Type A female connector.
cab-ThinMini-ITX-USB2.0-Twin	14000123	USB 2.0 cable with Twin USB 2.0 Type A female connector and 2x5 pin Housing.
cab-ThinMini-ITX-USB3.0-Twin	14000124	USB 3.0 cable with Twin USB 3.0 Type A female connector and 2x10 pin Housing.
cab-ThinMini-ITX-LVDS-Open End	14000125	ACES 40 pin LVDS cable with open end.
cab-ThinMini-ITX-BKLT	14000127	CHYAO SHIUNN 8 pin Backlight cable with open end.
cab-ThinMini-ITX-LVDS	14000129	ACES 50204-40 LVDS cable for Thin Mini-ITX.
cab-DP to HDMI	14000128	20 pin male DisplayPort to 19 pin female HDMI
cab-ThinMini-ITX-SATA-Power (50cm lenght)	14000135	50 cm SATA power cable with 2x15 pin female connectors.
cab-ThinMini-ITX-SATA-Power (30cm length)	14000136	30 cm SATA power cable with 2x15 pin female connectors.
SATA III cable (straight/straight)	48000029	30 cm SATA III data cable with straight/straight connectors
SATA III cable (straight/right-angled)	48000030	30 cm SATA III data cable with straight/right-angled connectors

2 Specification

2.1 Feature List

Table 1 Feature Summary

Form Factor	Based on Thin Mini-ITX form factor (170 x 170 mm)	
Processor	Intel® 3rd Generation Atom/Celeron SoC	
Memory	2x SO-DIMM dual channel non-ECC DDR3L memory, up to 1333 MT/s with 8GB maximum capacity. Sockets located top side of module	
cBC	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, I2C bus, Power loss control	
Chipset	Integrated in the SoC	
Audio	Realthek ALC888s 7.1 channel High Definition Audio codec	
Ethernet	2x Gigabit Ethernet support via the onboard Intel® I210/I211 Phy	
Graphics	Intel® HD Graphics with support for DirectX11, OpenGL 3.0, OpenCL 1.2, OpenGLES 2.0, full HW acceleration for decode/encode of MPEG2, H.264, MVC and dual simultaneous display support and support for dual simultaneous displays	
Graphic Interfaces	1x DD1 (DP, HDMI/DVI) and 1x eDP/LVDS	
Back Panel I/O Connectors	1x DisplayPort ++ (DP++). Supports DP/DVI/HDMI - 1x HDMI 1.4: Multiplexed with DisplayPort (DP)/DVI. Hot-plug detect support - 1x DVI: Multiplexed with HDMI/DP ports. Hot-Plug detect support 1x VGA	1x Audio OUT/MIC 2x Gigabit Ethernet (without AMT) 2x USB 2.0 2x USB 3.0 1x DC-IN
Onboard I/O Connectors	1x LVDS (top side) 1x eDP interface (bottom side) 1x Backlight 1x Monitor OFF SATA Interfaces - 2x Standard SATA II (3.0 Gb/s). - 1x mini SATA II (shared with mini PCIe Slot) - 1x SATA power header connector (3.3V, 5V or 12V) PCI Express Interfaces - 1x PCI Express® Slot (x1 Gen 2 link). - 1x Hall size mini PCIe Slot - 1x Full size mini PCIe Slot (shared with mSATA) - optional SIM card slot via connector X6 (Full size mPCIe/mSATA) 2x USB 2.0 2x USB 3.0	1x MicroSD slot (located at the bottom side) 1x Front panel HD audio 1x SPDIF/Digital microphone 1x Stereo speaker Connectors supported via Super IO - 2x COM ports (COM 1 can be used optionally as ccTALK) - 1x CPU fan with selectable voltage - 1x System fan with selectable voltage - 1x Case Open Intrusion Detection header - GPOs on feature connector Feature connector (GPIOs, SPI, SMB, LPC, LID/SLEEP etc) 1x Front panel header (Power button, reset, LEDs etc) 1x optional SBM3 support header 1x Internal power header (12-24V) 1x optional SBM3 power
Other Features	Thermal and voltage monitoring CMOS Battery Beeper congatec Standard BIOS (also possible to boot from an external BIOS by triggering the BIOS_DISABLE# signal on the feature connector)	
BIOS	AMI Aptio® UEFI 5.x firmware, 8/16 MByte serial SPI with congatec Embedded BIOS features	

Power Management	ACPI 4.0 compliant with battery support. Also supports Suspend to RAM (S3) Configurable TDP Ultra low standby power consumption, Deep Sx
Security	Optional discrete Trusted Platform Module "TPM 1.2/2.0", new AES Instructions for faster and better encryption

Note

The conga-IA3 supports only DDR3L memory modules and the memory modules in the sockets must be symmetrical - that is, same raw cards and same memory sizes. This is because the Bay Trail SoC on the conga-IA3 does not support mixed raw cards or same raw cards with mixed memory sizes. Although the conga-IA3 might boot up with asymmetrical memory modules, this may however cause memory errors or instabilities. Therefore use only symmetrical DDR3L memory modules on the conga-IA3 and also make sure the memory module supports the data transfer rate of the particular variant.

In addition, if you use only one memory module then you must insert this memory module only in the first memory slot of the conga-IA3 (top side). Due to the Bay Trail architecture, the conga-IA3 will ignore the second memory socket (bottom side) if the first memory slot is not populated. This means that you cannot boot up the conga-IA3 if the first memory slot is empty. See the Bay Trail datasheet for more information.

2.2 Supported Operating Systems

The conga-IA3 supports the following operating systems.

- Microsoft® Windows® 8
- Microsoft® Windows® 7
- Microsoft® Windows® 7/8 Embedded Standard
- Linux

Note

For the installation of Windows 7/8 and WES7/8, congatec AG requires a minimum storage capacity of 16 GB. congatec will not offer support for systems with less than 16 GB storage space.

2.3 Mechanical Dimensions

- 170 mm x 170 mm
- Height approximately 20 mm

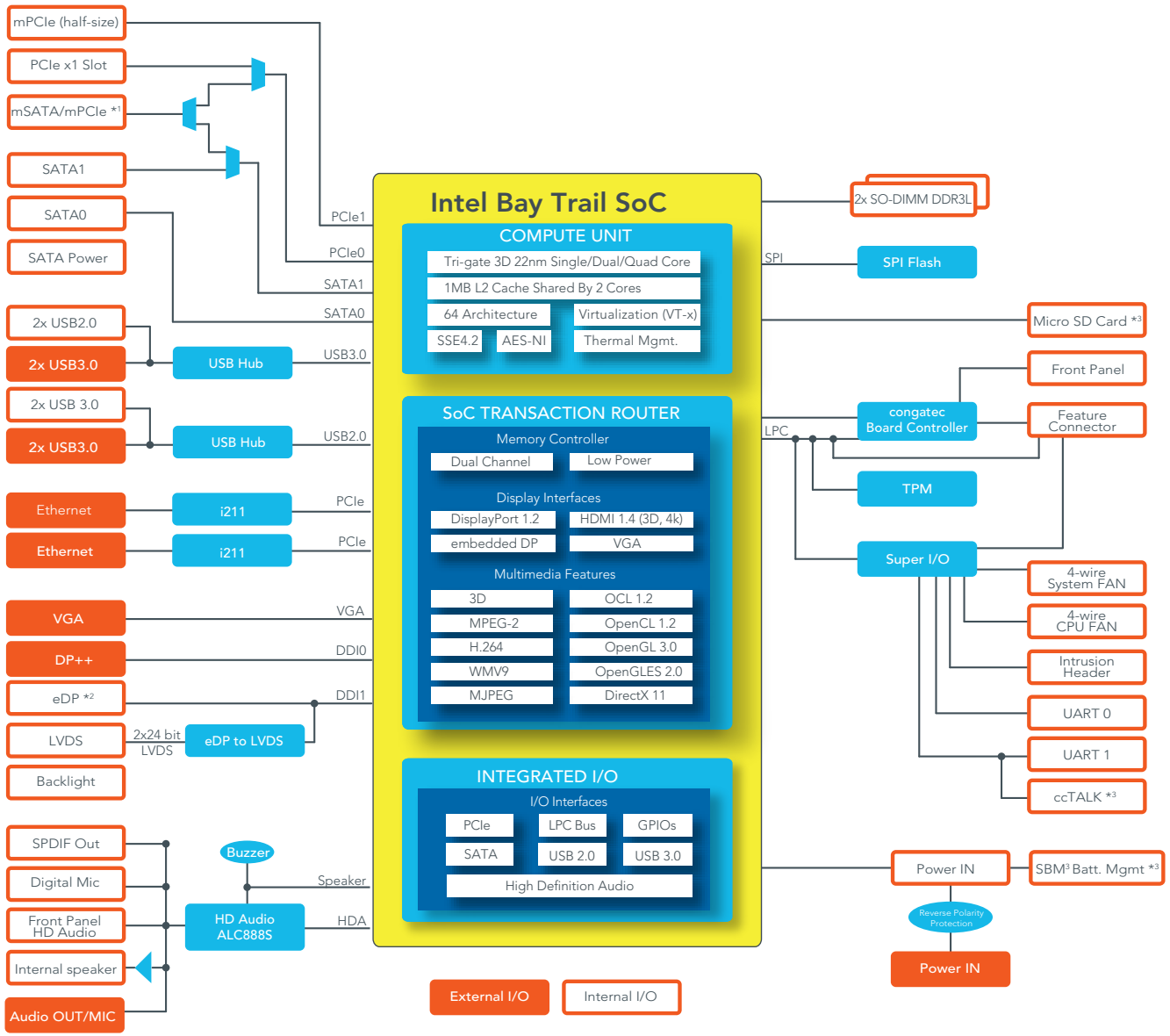
2.4 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Note

The above operating temperatures must be strictly adhered to at all times. Humidity specifications are for non-condensing conditions.

3 Block Diagram



*1 The mSATA/mPCIe connector supports both mPCIe and mSATA devices. The devices are detected automatically.

*2 Located at the bottom side.

*3 Optional feature.

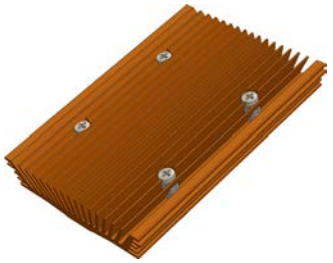
4 Cooling Solution

The conga-IA3 SBC offers Ultra Low Power boards with high computing performance and outstanding graphics. Due to its low power consumption, the SBC generates less heat and therefore requires less active cooling, allowing the use of quieter, lower profile coolers that are better suited to small form factor systems.

Nonetheless, all electronics contain semiconductor devices which have operating temperature ranges that should be adhered to. This means that for reliable operation, the thermal design of the conga-IA3 must be carefully considered. For this reason, it is imperative to provide sufficient air flow to each of the components, to ensure the specified operating temperature of the conga-IA3 is maintained.

congatec AG offers two cooling possibilities for the conga-IA3:

- A congatec passive cooling solution (CSP) in combination with the conga-IA3 retention frame. This cooling solution is adapted to the Thin Mini-ITX height specification and features a Hi-Flow 225UT pressure sensitive, phase change thermal interface. Refer to section 4.2 "Passive Cooling Solution(CSP)" for the dimensions of the congatec CSP.
- The use of a custom cooling solution in combination with the conga-IA3 retention frame.



Passive Cooling Solution (CSP)

Retention Frame

Note

When a passive cooling is used, the end user must ensure that adequate air flow is maintained.

See section 1.2.2 "Optional Accessories/Cables" for the part numbers of the cooling accessories.

4.1 Cooling Installation

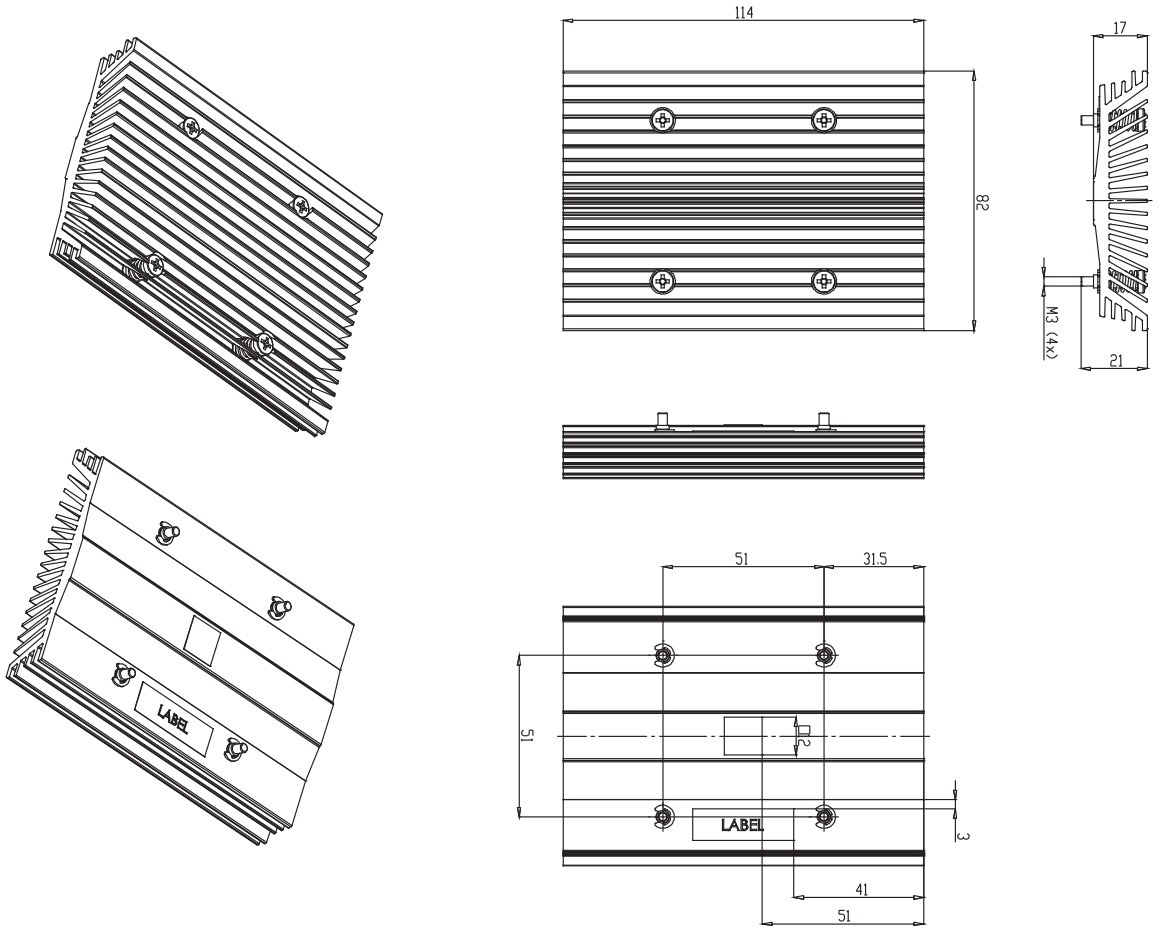
Assembly Instruction:

- Flip over the SBC and locate the position of the CPU
- Place retention frame on the bottom side of the board with insulating foil facing the PCB and standoffs inserted to PCB mounting holes.
- Remove the CSP's protection pull tab foil from the phase changer and carefully place the CSP to the CPU.
- Insert assembling screws.
- Hold the CSP with one hand so that it does not tilt while tightening the screws.
- Slightly tighten each of the four screws so that they hold the CSP in place. To do so, start with one screw and then slightly tighten the other screws in a crossover pattern. All the while keep holding the cooling adapter straight with one hand.
- Now you can fully tighten the screws. Once again start with one and then continue to tighten the other screws in a crossover pattern. All the while keep holding the cooling adapter straight with one hand

Caution

congatec cooling solutions have been specifically designed for use within commercial temperature ranges (0° to 60°C) only. It is the responsibility of the end user to design an optimized thermal solution that meets the needs of their application within the industrial environmental conditions it is required to operate in. Attention must be given to the mounting solution used to mount the cooling solution and SBC into the system chassis.

4.2 Passive Cooling Solution (CSP)



Note

All measurements are in millimeters. Torque specification for cooling solution screws is 0.3 Nm. Mechanical system assembly shall follow the valid DIN/IS0 specifications.

Caution

When using the CSP in a high shock and/or vibration environment, use a thread-locking fluid on the cooling solution screws to ensure the above mentioned torque specification is maintained.

5 Connector Description

5.1 Power Supply

You can power the conga-IA3 SBC with a 12V-24V laptop type DC power supply (on connector X43) or a 4 pin internal power supply (on connector X44).

Additionally, the SBC offers an optional SBM[3] power connector (only BOM option). When this connector (X45) is populated, you can power the SBC with it.

Note

The supplied voltages must be within a tolerance of ± 10%

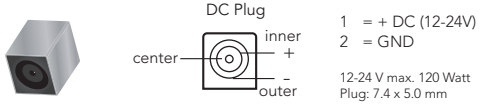
5.1.1 DC Power Jack (Rear I/O)

The conga-IA3 SBC can be powered from a laptop type external power supply connected to the DC power jack on the rear I/O. This power input protects against polarity reversal and over/under voltage.

Connector X43 Pinout Description

Pin	Function
Inner Shell	+12 - 24V
Outer Shell	GND

DC Power Jack - Connector X43



Connector Type

X43 : DC Power Jack, 7.4x5.1mm Diameter

Note

The default conga-IA3 BIOS configuration enables the system to boot-up immediately an external is supplied.

Caution

The absolute maximum rating of the input voltage is 36 volts. Do not exceed this rating or expose the conga-IA3 to the absolute maximum voltage for a prolonged time. Doing so may damage the system or affect system reliability.

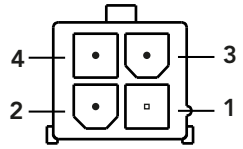
5.1.2 Power Supply (Internal Connector)

The conga-IA3 offers an internal 4-pin power connector. This connector makes it possible to use customized power supply cables/connector and also offers under/over voltage protection to the input voltage.

Connector X44 Pinout Description

Pin	Signal	Description
1	GND	Ground
2	GND	Ground
3	+12V - 24V	Power Supply +12V-24V
4	+12V - 24V	Power Supply +12V-24V

Internal Power Connector X44



Connector Type

X44 : 4 Pos, Pitch 4.2mm Internal Power Connector (PN: 41500079).

Mating Connector: A possible mating connector for X44 is the Molex 39-01-2045.

Note

The default conga-IA3 BIOS configuration enables the system to boot-up immediately an external is supplied.

Caution

The absolute maximum rating of the input voltage is 36 volts. Do not exceed this rating or expose the conga-IA3 to the absolute maximum voltage for a prolonged time. Doing so may damage the system or affect system reliability.

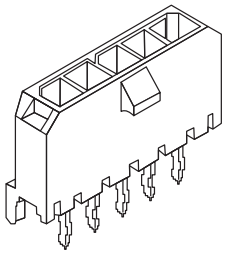
5.1.3 Optional SBM³ Power Connector (Internal Connector)

You can also power the conga-IA3 SBC optionally with an SBM battery kit. The battery kit requires two connections - the SBM battery power on connector X50 and the SBM battery signals on connector X45. The SBM³ feature requires a firmware update.

Connector X50 Pinout Description

Pin	Function
1	+12 - 24V
2	+12 - 24V
3	GND
4	GND
5	NC

SBM3 Power - Connector X50



Connector Type

X50 : 1x5 Pos, 3mm Pitch Micro-FIT

Caution

The absolute maximum rating of the input voltage is 36 volts. Do not exceed this rating or expose the conga-IA3 to the absolute maximum voltage for a prolonged time. Doing so may damage the system or affect system reliability.

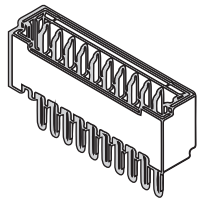
5.1.3.1 Optional SBM3 Signal Connector

As mentioned above, if you need the optional SBM battery power connector (X50), then you need in addition the optional SBM battery signals connector (X45) for adequate communication between the conga-IA3 and the battery kit.

Connector X45 Pinout Description

Pin	Function
1	GND
2	I2C_DAT
3	I2C_CLK
4	BATLOW#
5	SUS_STAT#
6	PM_SLP_S3#
7	PM_SLP_S5#
8	PWRBTN#

SBM3 Signal - Connector X45



Connector Type

X45 : 1x8 Pos, 1.25mm Pitch PicoBlade

5.1.4 PWR_OK Signal

With the PWR_OK signal on the feature connector (X34), the user can control the SBC's start-up process. When this signal is set to low, the SBC is kept in reset until the PWR_OK signal is asserted.

When the signal is asserted (set to high), it indicates to the SBC that the supplied power is stable. The SBC then begins its onboard power-up sequence.

5.1.5 Power Status LEDs

The conga-IA3 provides two LED signals (FP_LED1 and P_LED2) on pins 2 and 4 of the front panel connector X38. The signals indicate the different power states of the conga-IA3. Possible states and corresponding activity of the LEDs are shown below:

Double-Color Power LED

LED State	Description	ACPI State
Off	Power-off	S5
Steady Green	Running	S0
Steady Yellow	Sleeping	S3

Single-Color Power LED

LED State	Description	ACPI State
Off	Sleeping or power-off (not running)	S3, S5
Steady Green	Running	S0

Note

For the front panel pinout description, see section 6.1 "Front Panel Connector".

5.2 CMOS Battery/RTC

The conga-IA3 provides a board mounted battery holder (M29) for CMOS battery. The CMOS battery supplies the necessary power required to maintain the CMOS settings and configuration data in the UEFI flash chip. The specified battery type is CR2032.

M29 (Battery Holder)

Warning

Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

5.3 Audio Interfaces

The conga-IA3 provides audio connectors both internally and on the rear side. The internal audio connectors are stereo speaker, digital microphone/SPDIF and front Panel HD audio. The audio OUT/MIC connector is provided on the rear side.

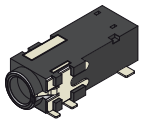
5.3.1 Rear Audio Connectors

The conga-IA3 has a high definition audio codec (Realtek ALC888S) mounted on it. The front channel line output signals and the MIC input signals are routed to connector X48 (audio OUT/MIC) on the rear side. The drivers for this codec can be found in the software section under conga-IA3 on the congatec website at www.congatec.com

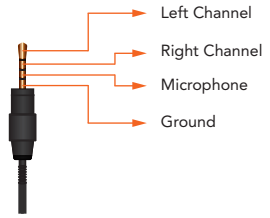
Audio OUT/MIC (Connector X48) Pinout Description

Pin	Plug	Signal	Description
1	Sleeve	A_GND	Analog Ground
2	Tip	FRONT_L	Front Analog Output Left Channel
3	Ring1	FRONT_R	Front Analog Output Right Channel
4	Ring2	MIC1_R/ MIC1_L	1st Microphone Analog Input Right Channel 1st Microphone Analog Input Left Channel
5	NA	SENSE_A	Jack Detect Pin 1
6	NA	SENSE_A	Jack Detect Pin 1

Audio OUT/MIC - Connector X48



Audio Jack



Connector Type

X48: 6 Pin, Single Audio Jack - black color

5.3.2 Internal Audio Connectors

The conga-IA3 provides the stereo speaker, digital microphone/SPDIF and front panel HD audio connectors internally.

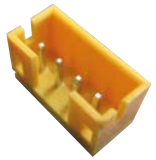
5.3.2.1 Stereo Speaker Header

The first analog line input channels (left and right) of the Realtek ALC888S HDA audio codec are routed via a TPA2012D2 amplifier to internal stereo speaker - connector X19. The amplifier offers a maximum wattage of 2.1W per channel into 4 ohms.

Stereo Speaker (Connector X19) Pinout Description

Pin	Signal	Description
1	OUTL-	Left Channel Negative Differential Output
2	OUTL+	Left Channel Positive Differential Output
3	OUTR-	Right Channel Negative Differential Output
4	OUTR+	Right Channel Positive Differential Output

Stereo Speaker - Connector X19



Connector Type

X19: 2mm Crimp Style Connector with 4 Pos.

Mating Connector: A possible mating connector for X19 is Chyao Shiunn JS-1124-04.

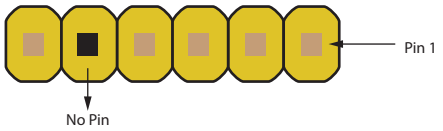
5.3.2.2 Digital Microphone/SPDIF

The digital microphone/SPDIF signals of the Realtek ALC888S HDA audio codec are routed to the internal digital microphone/SPDIF connector X17. This connector offers two power supply pins - 3,3V and 5V. Power Budget of these pins is limited to 500mA.

Internal Digital Microphone/SPDIF (Connector X17) Pinout Description

Pin	Signal	Description
1	+3.3V	3.3V supply
2	DMIC_DATA	Serial data from digital MIC
3	GND	Ground
4	SPDIFO2	Secondary S/PDIF output
5	KEY	No pin
6	+5V	5V supply

Digital MIC/SPDIF - Connector X17



Connector Type

X17: 2.54mm, 1x6 Pos. Header

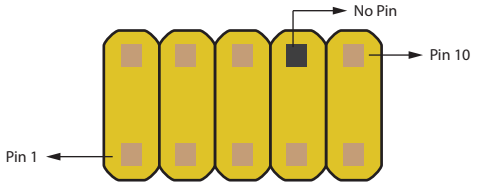
5.3.2.3 Front Panel HD Audio

The front panel HD audio (LINE2 and MIC2) signals of the Realtek ALC888S HDA audio codec are routed to connector X16. The pinout description of the connector is shown below:

Front Panel HD Audio (Connector X16) Pinout Description

Pin	Signal	Description
1	MIC2_L	2nd Analog Stereo Microphone Input - Left Channel
2	GND	Ground
3	MIC2_R	2nd Analog Stereo Microphone Input - Right Channel
4	PRESENCE#	Active low signal that indicates that an Intel HD Audio dongle is connected to the analog header.
5	LINE2_R	2nd Analog Line Input - Right Channel (Headphone)
6	GND_HDA	Audio Ground
7	SENSE_B	Jack Detection Pin 2
8	KEY	No pin
9	LINE2_L	2nd Analog Line Input - Left Channel (Headphone)
10	GND_HDA	Audio Ground

Front Panel Audio - Connector X16



Connector Type

X16: 2.54mm, 2x5 Pin Header

5.4 Communication Bus

The conga-IA3 supports both SMBus and I2C compliant devices.

5.4.1 SMBus

The SMBus signals are available in different locations on the conga-IA3, including the feature connector (X34) described in section 6.13 of this document.

5.4.2 I²C Bus

The congatec Board controller provides I²C signals. These signals are available in different locations on the conga-IA3, including the feature connector (X34) described in section 6.13 of this document.

5.4.3 SPI Bus

The SPI signals are connected to the onboard SPI flash and additionally to the feature connector (X34). The SPI signals on the feature connector provides the ability to boot the conga-IA3 from external flash. This however requires a customized adapter for triggering the BIOS_DISABLE# signal (pin 46) of the feature connector.

Note

The congatec customized adapter for the feature connector is currently for internal use only.

5.5 Universal Serial Bus (USB)

The conga-IA3 provides 8 USB connectors both on the rear side and internally. The rear and internal connectors have 4 USB ports each.

5.5.1 Rear USB Connectors

The conga-IA3 offers a total of four USB ports on the rear side - two USB 2.0 ports on connector X14 and two USB 3.0 ports on connector X15. The USB 2.0 signals on connector X14 are routed directly from the SoC's USB ports 2 and 3. The USB 3.0 signals on connector X15 are routed from the SoC's USB Superspeed and USB port 0 signals via a USB 3.0 hub.

USB 2.0 (Connector X14) Pinout Descriptions

Lower Port			Upper Port		
Pin	Signal	Description	Pin	Signal	Description
A1	+5V	+5V supply	B1	+5V	+5V supply
A2	Data-	Hi-speed differential transceiver (negative)	B2	Data-	Hi-speed differential transceiver (negative)
A3	Data+	Hi-speed differential transceiver (positive)	B3	Data+	Hi-speed differential transceiver (positive)
A4	GND	Ground	B4	GND	Ground

Connector X14

Upper

Lower

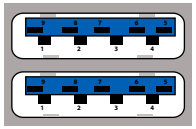
USB 3.0 (Connectors X15) Pinout Descriptions

Lower Port			Upper Port		
Pin	Signal	Description	Pin	Signal	Description
1	+5V	+5V supply	10	+5V	+5V supply
2	Data1-	Hi-speed differential transceiver (negative)	11	Data2-	Hi-speed differential transceiver (negative)
3	Data1+	Hi-speed differential transceiver (positive)	12	Data2+	Hi-speed differential transceiver (positive)
4	GND	Ground	13	GND	Ground
5	SS1_RX-	SuperSpeed receiver differential pair (negative)	14	SS2_RX-	SuperSpeed receiver differential pair (negative)
6	SS1_RX+	SuperSpeed receiver differential pair (positive)	15	SS2_RX+	SuperSpeed receiver differential pair (positive)
7	GND	Ground	16	GND	Ground
8	SS1_TX-	SuperSpeed transmitter differential pair negative)	17	SS2_TX-	SuperSpeed transmitter differential pair (negative)
9	SS1_TX+	SuperSpeed transmitter differential pair (positive)	18	SS2_TX+	SuperSpeed transmitter differential pair (positive)

Connector X15

Upper

Lower



Connector Type

X14,X15: Two Type A, Dual Port USB Connectors

Note

The +5V signals of connector X14 and X15 have a maximum current of 1.2A each.

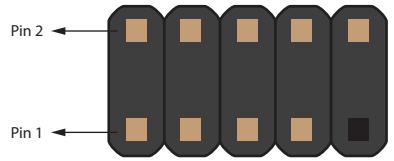
5.5.2 Internal USB Connectors

The conga-IA3 offers 4 USB ports internally - two USB 2.0 ports on connector X12 and two USB 3.0 ports on connector X60. The USB 2.0 signals on connector X12 are routed from the SoC's USB port 1 via a USB 2.0 hub. The USB 3.0 signals on connector X60 are routed from the SoC's USB Superspeed and USB port 0 signals via a USB 3.0 hub.

USB 2.0 Header (Connector X12) Pinout Description

Port 1			Port 2		
Pin	Signal	Description	Pin	Signal	Description
1	+5V	+5V supply	2	+5V	+5V supply
3	Data2-	Hi-speed differential transceiver (negative)	4	Data3-	Hi-speed differential transceiver (negative)
5	Data2+	Hi-speed differential transceiver (positive)	6	Data3+	Hi-speed differential transceiver (positive)
7	GND	Ground	8	GND	Ground
9	No Pin	Empty	10	NC	Not Connected

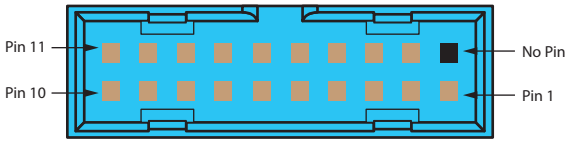
Internal USB 2.0 - Connector X12



USB 3.0 Header (Connectors 60) Pinout Description

Port 1			Port 2		
Pin	Signal	Description	Pin	Signal	Description
1	+5V	+5V supply	11	Data4-	High-speed differential transceiver (-ve)
2	SS3_RX-	SuperSpeed receiver differential pair (-ve)	12	Data4+	High-speed differential transceiver (+ve)
3	SS3_RX+	SuperSpeed receiver differential pair (+ve)	13	GND	Ground
4	GND	Ground	14	SS4_TX+	SuperSpeed transmitter differential pair (+ve)
5	SS3_TX-	SuperSpeed transmitter differential pair (-ve)	15	SS4_TX-	SuperSpeed transmitter differential pair (-ve)
6	SS3_TX+	SuperSpeed transmitter differential pair (+ve)	16	GND	Ground

Internal USB 3.0 - Connector X60



7	GND	Ground	17	SS4_RX+	SuperSpeed receiver differential pair (+ve)
8	Data3+	High-speed differential transceiver (+ve)	18	SS4_RX-	SuperSpeed receiver differential pair (-ve)
9	Data3-	High-speed differential transceiver (-ve)	19	+5V	+5V supply
10	NC	Not Connected	20	No Pin	Empty

Connector Type

X12: 2x5 Pin Header

X60: 2.54mm, 2x10 Pin Header

Note

The +5V signals of connector X12 and X60 have maximum current of 0.5A each.

congatec offers adapter cables for the Internal USB connectors (see section 1.2.2 "Optional Accessories/Cables). For more information, contact congatec technical solution department.

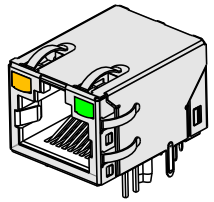
5.6 Ethernet 10/100/1000

The conga-IA3 provides two Gigabit Ethernet ports (connectors X57 and X58) on the rear side. The two Gigabit Ethernet interfaces are supported via the Intel Gigabit Ethernet controller i211. These interfaces do not support the Intel AMT.

Connectors X57/X58 Pinout Description

Pin	Description	10base-T	100Base-T	1000Base-T
1	Transmit Data+ or Bidirectional	TX+	TX+	BI_DA+
2	Transmit Data- or Bidirectional	TX-	TX-	BI_DA-
3	Receive Data+ or Bidirectional	RX+	RX+	BI_DB+
4	Not connected or Bidirectional	nc	nc	BI_DC+
5	Not connected or Bidirectional	nc	nc	BI_DC-
6	Receive Data- or Bidirectional	RX-	RX-	BI_DB+
7	Not connected or Bidirectional	nc	nc	BI_DD+
8	Not connected or Bidirectional	nc	nc	BI_DD-

Gigabit Ethernet - Connector X57/X58



LED Descriptions

LED Left Side	Description
Off	10 Mbps link speed
Green	100 Mbps link speed
Orange	1000 Mbps link speed

LED Right Side	Description
Off	No link
Steady On	Link established, no activity detected
Blinking	Link established, activity detected

Connector Type

X57/X58: 8 Pin RJ45 Connector with Gigabit Magnetic and LEDs.

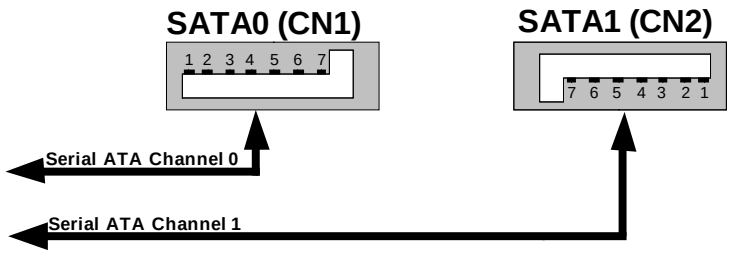
5.7 SATA Interfaces

5.7.1 Standard SATA Ports

The conga-IA3 provides two SATA ports. The SATA ports are routed to connectors CN1/CN2 and support data rates up to 3GB/s. The SATA LED on the front panel connector (X38) is lit when there is activity on any of the SATA interfaces.

Connectors CN1/CN2 Pinout Description.

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND



Connector Type

CN1, CN2: Standard SATA Connector

5.7.2 SATA Power

The conga-IA3 provides an internal SATA power for hard drives on connector X8. This connector supplies 3.3V, 5V and 12V.

Connectors X8 Pinout Description.

Pin	Signal	Pin	Signal
1	+3.3V	9	+5V
2	+3.3V	10	GND
3	+3.3V	11	GND
4	GND	12	GND
5	GND	13	12V
6	GND	14	12V
7	+5V	15	12V
8	+5V		

SATA Power (X8)

Connector Type

X8: 15 Pos. SATA Connector.

Note

The voltage rails +3.3V, +5V and +12V have maximum current of 2 amps each.

5.7.3 Mini SATA

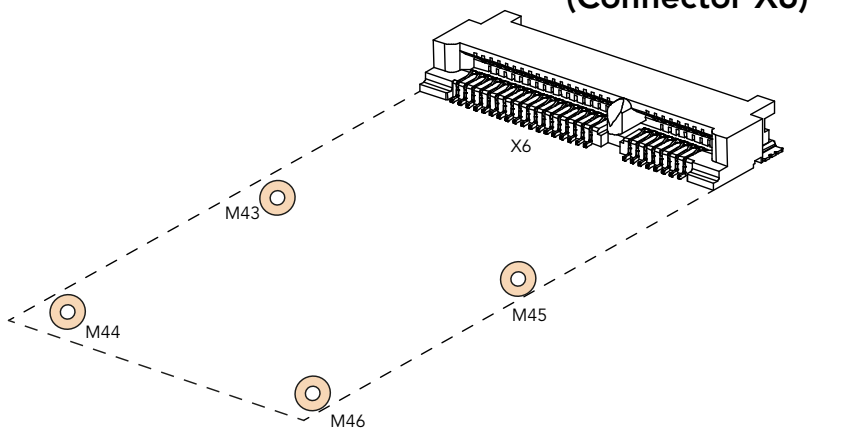
The mini SATA connector X6 on the conga-IA3 is used to connect mSATA devices. This connector also supports mini PCIe devices. When an mSATA or mPCIe device is connected to X6, the conga-IA3 automatically detects the type of device that is attached.

mSATA (Connector X6) Pin Description.

Pin	Signal	Pin	Signal
1	Reserved	2	+3.3V
3	N.C.	4	GND
5	N.C.	6	+1.5V
7	Reserved	8	N.C.

Pin	Signal	Pin	Signal
9	GND	10	N.C.
11	Reserved	12	N.C.
13	Reserved	14	N.C.
15	GND	16	N.C.
17	Reserved	18	GND
19	N.C.	20	Reserved
21	Card_Present *	22	Reserved
23	+B	24	+3.3V
25	-B	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	-A	32	SMB_DATA
33	+A	34	GND
35	GND	36	Reserved
37	GND	38	Reserved
39	+3.3V	40	GND
41	+3.3V	42	N.C
43	Card_Type_Recognition *	44	N.C
45	N.C	46	N.C
47	N.C	48	+1.5V
49	N.C	50	GND
51	N.C.	52	+3.3Vaux
53	GND	54	GND

mSATA/mPCIe Socket (Connector X6)



Connector Type

X6: 0.8mm Pitch, 52 Pos. Mini PCI Socket

Note

** For card presence detection, pin 21 of the mSATA card must be terminated to ground. For card type recognition, pin 43 of the mSATA card must be unconnected.*

5.8 Display Interfaces

The conga-IA3 supports dual simultaneous displays - one Digital Display Interface and one embedded Display or LVDS interface.

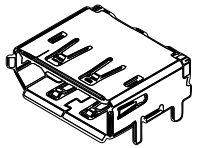
5.8.1 Display Port Interface DP++

The conga-IA3 SBC has one DP++ connector (X26) located at the rear I/O panel. The display port supports the connection of DP, HDMI and DVI displays.

Connectors X26 Pinout Description.

Pin	Signal	Pin	Signal
1	DDI_TX0+	11	GND
2	GND	12	DDI_TX3-
3	DDI_TX0-	13	CONFIG1
4	DDI_TX1+	14	CONFIG2
5	GND	15	DDI_AUX+
6	DDI_TX1-	16	GND
7	DDI_TX2+	17	DDI_AUX-
8	GND	18	DDI_HPD
9	DDI_TX2-	19	GND
10	DDI_TX3+	20	3.3V

DP++ Connector X26



5.8.2 LVDS

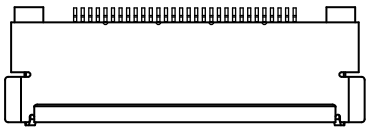
The conga-IA3 offers LVDS interface on connector X32 - a standard 40 pin LVDS connector. The LVDS signals are sourced from the SoC's eDP stream via a multiplexer. Depending on the BIOS setup, the multiplexer routes the eDP stream either directly to the eDP connector X28 or to the LVDS connector X32 via an eDP to LVDS bridge. The multiplexer is configured in the BIOS setup by default to route the eDP signals to the eDP to LVDS bridge. The eDP to LVDS bridge processes and converts the eDP stream to LVDS format.

The LVDS interface is found on the top side of the SBC and supports 24 bit single channel, selectable backlight voltage, VESA color mappings, automatic panel detection and resolution up to 1920x1200 in dual LVDS mode.

Connector X32 Pinout Description

Pin	Signal	Pin	Signal
1	LVDS_A3+	21	N.C.
2	LVDS_A3-	22	EDID_3.3V
3	LVDS_A2+	23	LCD_GND
4	LVDS_A2-	24	LCD_GND
5	LVDS_A1+	25	LCD_GND
6	LVDS_A1-	26	LVDS_A_CLK+
7	LVDS_A0+	27	LVDS_A_CLK-
8	LVDS_A0-	28	BKLT_GND
9	LVDS_B3+	29	BKLT_GND
10	LVDS_B3-	30	BKLT_GND
11	LVDS_B2+	31	EDID_CLK
12	LVDS_B2-	32	eDP_LVDS_BKLT_EN
13	LVDS_B1+	33	eDP_LVDS_BKLT_CTRL
14	LVDS_B1-	34	LVDS_B_CLK+
15	LVDS_B0+	35	LVDS_B_CLK-
16	LVDS_B0-	36	BKLT_PWR
17	EDID_GND	37	BKLT_PWR
18	LCD_VCC	38	BKLT_PWR
19	LCD_VCC	39	N.C
20	LCD_VCC	40	EDID_DATA

LVDS Connector X32



Connector Type

X32: 0.5mm, 40 Pos. ACES Connector.

Mating Connector: Possible mating connectors for X32 are ACES 88441-40 and ACES 50204-40.

Note

congatec offers cables and adapter for the LVDS interface (see section 1.2.2 "Optional Accessories/Cables"). For more information, contact congatec technical solution department.

5.8.3 Embedded Display Port (eDP)

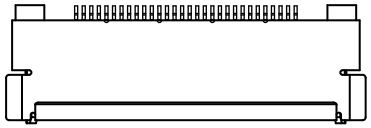
The conga-IA3 provides eDP interface on connector X28 - a standard 40 pin DisplayPort connector. The eDP signals are sourced from the SoC's eDP stream via a multiplexer. Depending on the BIOS setup, the multiplexer routes the eDP stream either directly to the eDP connector X28 on the bottom side of the SBC or to the LVDS connector X32 (top side) via an eDP to LVDS bridge. The multiplexer is by default configured in the BIOS setup to route the eDP signals to the eDP to LVDS bridge.

To route eDP signals to connector X28, change the default BIOS setup.

Connector X28 Pinout Description

Pin	Signal	Pin	Signal
1	N.C.	21	VCC_EDP_FILT
2	GND	22	N.C.
3	eDP_TX3-	23	GND
4	eDP_TX3+	24	GND
5	GND	25	GND
6	eDP_TX2-	26	GND
7	eDP_TX2+	27	eDP_DETECT
8	GND	28	GND
9	eDP_TX1-	29	GND
10	eDP_TX1+	30	GND
11	GND	31	GND
12	eDP_TX0-	32	eDP_LVDS_BKLT_EN
13	eDP_TX0+	33	eDP_LVDS_BKLT_CTRL
14	GND	34	N.C.
15	eDP_AUX+	35	N.C.
16	eDP_AUX-	36	N.C
17	GND	37	BKLT_PWR
18	VCC_EDP_FILT	38	BKLT_PWR
19	VCC_EDP_FILT	39	BKLT_PWR
20	VCC_EDP_FILT	40	N.C.

eDP Connector X28



Connector Type

X28: 0.5mm , 40 Pos. ACES Connector.

Mating Connector: Possible mating connectors for X28 are ACES 88441-40 and ACES 50204-40.

Note

congatec offers cables and adapter for the eDP interface (see section 1.2.2 "Optional Accessories/Cables"). For more information, contact the congatec technical solution department.

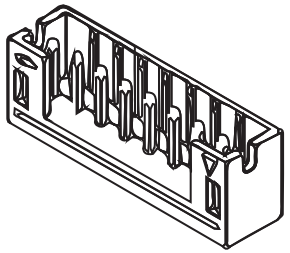
5.8.3.1 Backlight Power Connector

The conga-IA3 provides backlight power on connector X31. The power budget of BKLT_PWR (pins 3 and 4) is limited to 1.5 amps.

Connector X31 Pinout Description

Pin	Signal Name	Description
1	eDP_LVDS_BKLT_EN	Backlight enable
2	eDP_LVDS_BKLT_CTRL	Backlight control
3	BKLT_PWR	Backlight inverter power
4	BKLT_PWR	Backlight inverter power
5	GND	Backlight/Brightness Ground
6	GND	Backlight/Brightness Ground
7	Brightness_Up	Flat panel brightness increase
8	Brightness_Down	Flat panel brightness decrease

Backlight Power - Connector X31



Connector Type

X31: 2mm, 8 Pos. Crimp Style Connectors.

Mating Connector: Possible mating connector for X31 is Chyao Shiunn JS-1124-08.

Note

congatec offers an open-end cable for this interface (see section 1.2.2 "Optional Accessories/Cables"). For more information, contact the congatec technical solution department.

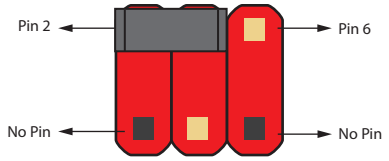
5.8.3.2 Backlight/Panel Power Selection

The conga-IA3 supports different voltages for the panel and backlight. With jumper X29, you can set the panel voltage to 3,3V, 5V or 12V. With jumper X30, you can set the backlight voltage to 5V or 12V.

Connector X29 Pinout Description

Pin	Signal Name
1	No Pin
2	3,3V
3	12V
4	Selected LCD Power
5	No Pin
6	5V

Panel Voltage Selector - Jumper X29

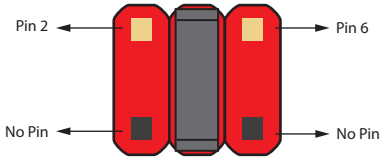


Default Settings:
Pins 2 and 4

Connector X30 Pinout Description

Pin	Signal Name
1	No Pin
2	NC
3	12V
4	Selected Backlight Power
5	No Pin
6	5V

Backlight Voltage Selector - Jumper X30



Default Settings:
Pins 3 and 4

Connector Type

X29, X30: 2.54mm, 2x3 Pos. Connector (without pins 1 and 5)

5.8.3.3 Monitor OFF connector

The monitor OFF connector X51 offers the possibility to switch off the displays attached to LVDS or eDP port.

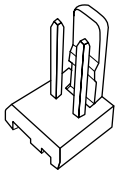
Connector X51 Pinout Description

Pin	Function
1	MONITOR_OFF#
2	GND

Connector Type

X51: 2.54mm, 2 Pos. Molex Connector.

Monitor OFF - Connector X51



5.9 PCI Express

The conga-IA3 provides 3 PCIe interfaces - a x1 PCIe slot on connector X9, a half-size mini PCIe (mPCIe) slot on connector X10 and a full size mini PCIe/mini SATA slot on connector X6. Th

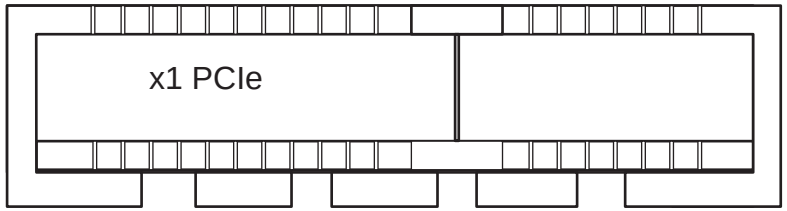
5.9.1 x1 PCIe Slot

The conga-IA3 offers one PCIe x1 slot on connector X9. The SoC's PCIe lane 0 signals are routed to connector X9 (x1 PCIe slot) via a multiplexer and to connector X6 (mini PCIe/mini SATA) via two multiplexers. Connector X9 shares the SoC's PCIe lane 0 with connector X6. The PCIe signals are controlled via the multiplexer. Immediately an mPCIe device is inserted, the multiplexer automatically switches the PCIe lane 0 signals to connector X6.

x1 PCIe Slot (Connector X9) Pinout Description

Pin	Signal	Pin	Signal
B1	+12V	A1	GND
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	SMB_CLK	A5	N.C.
B6	SMB_DAT	A6	N.C.

PCIe Slot (Connector X9)



B7	GND	A7	N.C.
B8	+3.3V	A8	N.C.
B9	N.C.	A9	+3.3V
B10	+3.3V Aux	A10	+3.3V
B11	WAKE#	A11	PCIE_RST#
	Key		
B12	N.C.	A12	GND
B13	GND	A13	PCIE_CLK+
B14	PCIE_TX0+	A14	PCIE_CLK-
B15	PCIE_TX0-	A15	GND
B16	GND	A16	PCIE_RX0+
B17	PRSNT2#	A17	PCIE_RX0-
B18	GND	A18	GND

Connector Type

X9: PCIe x1 Connector

Note

The PCIe x1 slot on connector X9 will not function if you insert a mini PCIe card into the mPCIe slot (connector X6). To use the PCIe x1 slot, do not insert any device into the mPCIe slot.

5.9.2 Mini PCIe (Half Size)

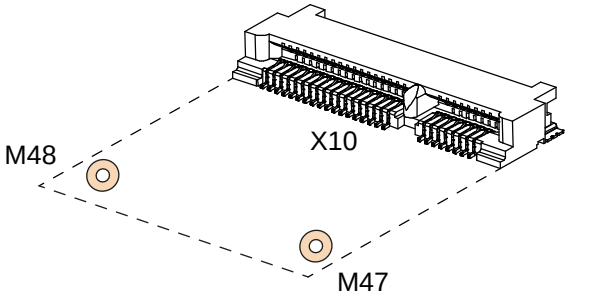
The conga-IA3 is equipped with a PCI Express Mini Card socket. PCI Express Mini Card is a unique small size form factor optimized for mobile computing platforms equipped with communication applications. The small footprint connector can be implemented on SBCs, providing the ability to insert different removable PCI Express Mini Cards. Using this approach gives the flexibility to mount an upgradable, standardized PCI Express Mini Card device to the SBC without additional expenditure of a redesign. The table below lists the default pinout of the PCI Express Mini Card.

mPCIe (Connector X10) Pinout Description

Pin	Signal	Pin	Signal
1	WAKE#	2	+3.3Vaux
3	N.C.	4	GND

Pin	Signal	Pin	Signal
5	N.C.	6	+1.5V
7	CLKREQ#	8	N.C.
9	GND	10	N.C.
11	REFCLK-	12	N.C.
13	REFCLK+	14	N.C.
15	GND	16	N.C.
17	Pull down resistor (1M)	18	GND
19	N.C.	20	W_DISABLE#
21	GND	22	PERST#
23	PERn0	24	+3.3Vaux
25	PERp0	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3Vaux	40	GND
41	+3.3Vaux	42	N.C
43	mSATA_mPCIe_detect	44	N.C
45	CL_CLK	46	N.C
47	CL_DATA	48	+1.5V
49	CL_RST#	50	GND
51	N.C.	52	+3.3Vaux
53	GND	54	GND

mPCIe Socket (Connector X10)



Connector Type

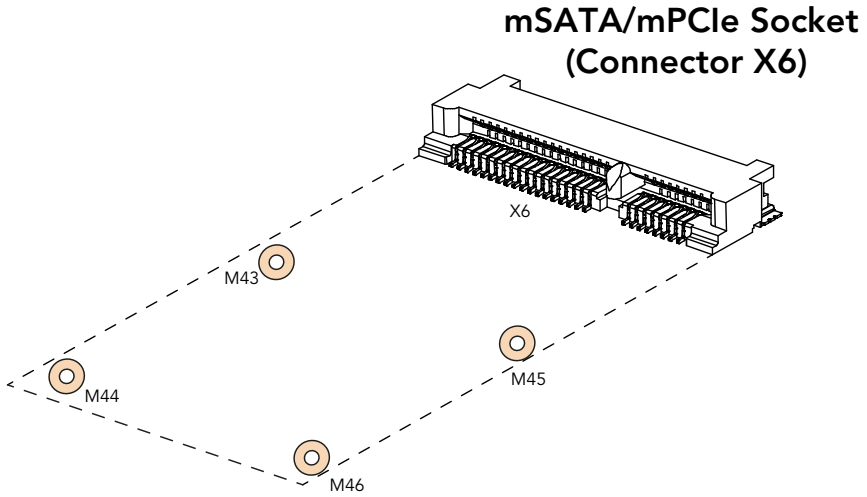
X10: PCIe Mini Card Socket

5.9.3 Mini PCIe (Full Size)

The conga-IA3 offers an mPCIe slot on connector X6. This connector supports both mPCIe and mSATA devices. The PCIe signals are routed from the SoC's PCIe lane 0 to connector X6 (mPCIe/mSATA slot) via two multiplexers. The first multiplexer switches the PCIe signals between the x1 PCIe slot (connector X9) and the mPCIe/mSATA slot (connector X6). The second multiplexer switches the SATA signals between SATA port 1 (connector CN2) and mSATA/mPCIe slot.

When an mPCIe or mSATA device is attached to the mPCIe/mSATA slot (connector X6), the SoC detects the connected device via the signal detect pin (pin 43), sets the communication mode to PCIe or SATA and automatically switches the PCIe/SATA signals to mPCIe/mSATA slot.

See section 5.9.2 "Mini PCIe (Half Size)" for the mini PCIe Pinout Description.



Connector Type

X6: PCIe Mini Card Socket

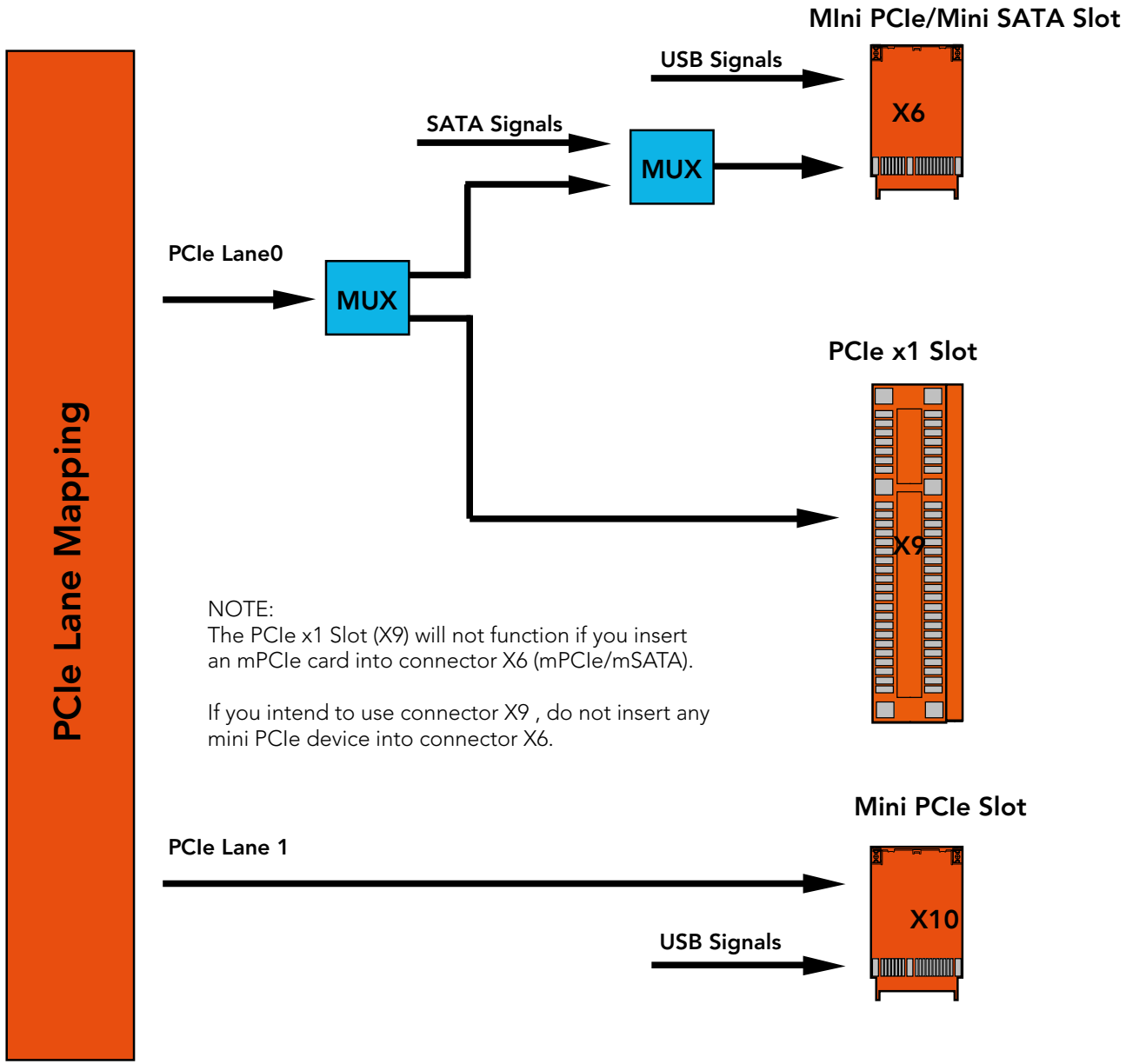
Note

Pins 21 and 43 of the mPCIe card must be terminated to ground for card present detection and card type recognition respectively.

The PCIe x1 slot on connector X9 will not function if you insert a mini PCIe card into the mPCIe slot (connector X6). To make use of the PCIe x1 slot, do not insert any mini PCIe device into the mPCIe slot (connector X6).

5.9.4 PCI Express Routing

The diagram below shows how the PCIe lanes are routed to the PCIe connectors.



6 Additional Features

6.1 Front Panel Connector

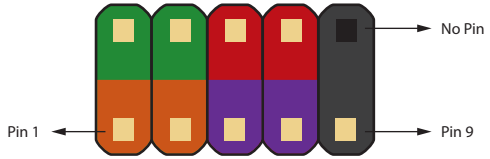
The conga-IA3 SBC supports front panel features such as power button, status LEDs and reset button via connector X38 - a 10-pin internal header. This connector offers one power supply pin (3.3V). The signals FP_LED+ and FP_LED- communicates the system states to two LEDs connected to this header.

See section 5.1.5 “Power Status LED” for the possible states and corresponding activity of the LEDs.

Front Panel (Connector X38) Pinout Description

Pin	Function	Description
1	HDD_POWER_LED+	Hard disk power LED with pull-up resistor to 3.3V.
2	FP_LED+	Power LED (main color)
3	HDD_LED	Hard disk activity LED
4	FP_LED-	Power LED (alternate color)
5	GND	Ground
6	PWRBTN#	Power Button
7	SYS_RST#	Reset Button
8	GND	Ground
9	3.3V	+3.3V power supply (500mA power budget)
10	KEY	No pin

Front Panel - Connector X38



Connector Type

X38: 10 Pin Header

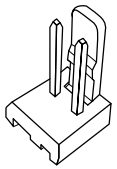
6.2 Case Open Intrusion Connector

The conga-IA3 provides connector X56 for case-open intrusion detection.

Case Open Intrusion (Connector X56) Pinout Description

Pin	Function
1	GND
2	CASEOPEN#

Case Open Intrusion - Connector X56



Connector Type

X56: 2.54mm, 2 Pos Molex Connector.

6.3 Trusted Platform Module – TPM (Optional)

The conga-IA3 SBC can optionally be equipped with a TPM 1.2 compliant security chip. The TPM security chip is connected to the LPC bus provided by the integrated Intel Chipset. The basic TPM chip initialization is performed by the SBC's UEFI Boot firmware.

6.4 congatec Board Controller (cBC)

The conga-IA3 is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRBI microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

6.4.1 Fan Control

The conga-IA3 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

6.4.2 GPIs

The GPI signals are routed to the feature connector (X38) described in section 6.13.

6.4.3 Power Loss Control

The cBC has full control of the power-up of the SBC, therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

6.4.4 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.5 LPC Super I/O Device

The conga-IA3 has an onboard Super I/O controller that provides additional interfaces such as two serial interfaces, optional ccTALK, GPOs, 4-wire CPU and system fans. The Super I/O controller is connected to the LPC Bus of the Intel® SoC.

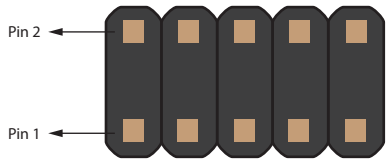
6.5.1 Serial Ports (COM)

The Super IO controller on the conga-IA3 provides two fully featured RS-232 compliant UART interfaces (COM 0 and 1). The COM 1 interface can be optionally used as ccTALK compliant interface. The COM ports can drive up to 115 kbit/s at a maximum cable length of 15 m.

Serial Ports (Connectors X21/X23) Pinout Description

Pin	Signal	Description	Pin	Signal	Description
1	DCD	Data Carrier Detect	6	DSR	Data Set Ready
2	RXD	Received Data	7	RTS	Request to Send
3	TXD	Transmit Data	8	CTS	Clear to Send
4	DTR	Data Terminal Ready	9	RI	Ring Indicator
5	GND	Ground	10	N.C	Not connected

COM 0 & 1 - Connectors X21/X23



Connector Type

X21,X23: 2.54mm Pitch, 2x5 Pin Headers

Note

congatec offers the adapter cable for the COM ports (see section 1.2.2 "Optional Accessories/Cables). For more information, contact congatec technical solution department.

6.5.2 GPOs

The GPO signals are routed to the feature connector (X38) described in section 6.13.

6.5.3 CPU/System Fan Connector & Power Configuration

The conga-IA3 supports the connection of 5V or 12V cooling fans. The signals of the CPU and system fans are routed to 4-pin connectors X35 and X37 respectively. Use jumper X33 to select the CPU fan voltage and jumper X36 to select the system fan voltage.

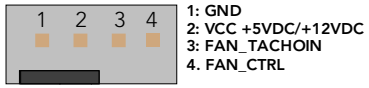
The following tables describe the pinouts and jumper configuration.

X35 CPU FAN Pin	Signal
1	GND
2	VCC +5VDC/+12VDC
3	FAN_TACHOIN
4	FAN_CTRL

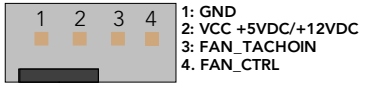
X37 System FAN Pin	Signal
1	GND
2	VCC +5VDC/+12VDC
3	FAN_TACHOIN
4	FAN_CTRL

Jumper X33, X36	Configuration
1 - 2	FAN +12VDC (default)
2 - 3	FAN +5VDC

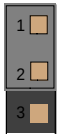
CPU Fan (X35)



SYS Fan (X37)



X33 X36



Connector Type

X35, X37: 4 pin 2.54mm Grid Female Fan Connector.

X33, X36: 2.54mm Grid Jumper.

Note

The maximum power of the CPU fan is approximately 3W while the system fan has a maximum power of approx. 4.5W.

6.6 OEM BIOS Customization

The conga-IA3 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide, which is called CGUTLm1x.pdf and can be found on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

6.6.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.6.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.6.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.6.4 OEM BIOS Code/Data

With the congatec embedded BIOS, it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table (OA2.0), Windows 8 OEM activation (OA3.0), verb tables for HDA codecs, PCI/PCIe opROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.6.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.7 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-IA3 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

6.8 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

6.9 GPIOs

The conga-IA3 SBC provides eight General Purpose Inputs via the congatec board controller and eight General Purpose Outputs via the onboard Super I/O. The GPIO signals are routed to the feature connector X34.

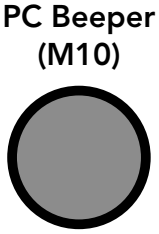
6.10 Thermal/Voltage Monitoring

The conga-IA3 SBC features three temperature sensors - the CPU, memory and board controller sensors.

The board controller can monitor six different voltages which are main power, 5V (runtime), 5V (standby), 1.05V (runtime), VCORE, 3,3V (runtime) and 3,3V (standby).

6.11 Beeper

The board-mounted speaker (M10) provides audible error code (beep code) information during POST.



6.12 External System Wake Event

The conga-IA3 supports LAN, USB, PCIe and PWRBTN driven wake up events.

6.13 Feature Connector

The conga-IA3 provides an internal 50 pol. 2mm pin header as feature connector. The pinout is described below:

Feature Connector X34 Pinout Description

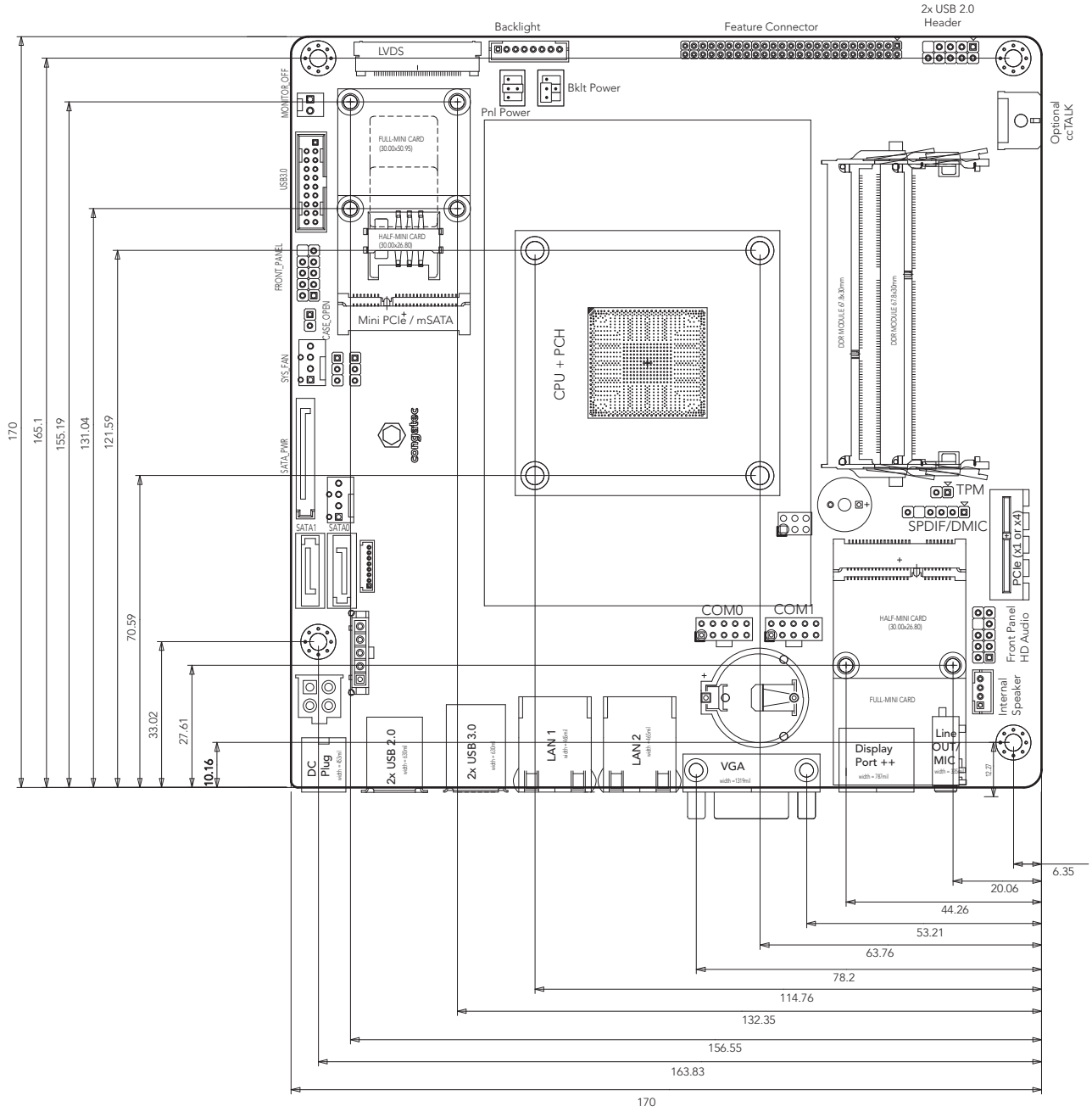
Pin	Signal	Pin	Signal
1	+V5S	2	GND
3	LAD0	4	LAD1
5	LAD2	6	LAD3
7	LFRAME#	8	SERIRQ#
9	LPC_CLK (25MHz)	10	BUF_PLT_RST#
11	SMB_DATA	12	SMB_CLK
13	SMB_ALERT#	14	GND
15	TX_CGBC	16	RX_CGBC
17	GPO0	18	GPO1
19	GPO2	20	GPO3
21	GPO4	22	GPO5
23	GPO6	24	GPO7
25	GPI0	26	GPI1
27	GPI2	28	GPI3
29	GPI4	30	GPI5
31	GPI6	32	GPI7
33	PM_SLP_S3#	34	PM_SLP_S5#
35	PM_SLP_S4#	36	LID_BTN#
37	SLP_BTN#	38	PM_THRM#
39	WDOUT	40	WDTRIG
41	I2C_DAT	42	PWR_OK
43	SPI_CS#	44	I2C_CLK
45	SPI_SO	46	BIOS_DISABLE#
47	SPI_CLK	48	SPI_SI
49	+V5A	50	GND

Feature Connector X34

Connector Type

X34: 2mm, 2 x 25 Pos Header.

7 conga-IA3 Mechanical Drawing



8 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

8.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

8.1.1 Boot Selection Popup

Press the <F11> key during POST to access the Boot Selection Popup menu. A selection menu displays immediately after POST, allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

8.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar, left frame and right frame. The menu bar is shown below:

Main	Advanced	Chipset	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

8.3 Main Setup Screen

When you first enter the BIOS setup, you will see the main setup screen. The main setup screen reports BIOS, processor, memory and board information and is for configuring the system date and time. You can always return to the main setup screen by selecting the 'Main' tab.

Feature	Options	Description
Main BIOS Version	No option	Displays the main BIOS version.
OEM BIOS Version	No option	Displays the additional OEM BIOS version.
Build Date	No option	Displays the date the BIOS was built.
Product Revision	No option	Displays the hardware revision of the board.
Serial Number	No option	Displays the serial number of the board.
BC Firmware Revision	No option	Displays the firmware revision of the congatec board controller.
MAC Address	No option	Displays the MAC address of the onboard Ethernet controller.
MAC Address #2	No option	Displays the MAC address of the second onboard Ethernet controller.
Boot Counter	No option	Displays the number of boot-ups. (max. 16777215).
Running Time	No option	Displays how long the system has been running.
Microcode Patch	No option	Displays the microcode version
Baytrail SoC	No option	D.0 Stepping for Atom CPUs and C.0 for Celeron CPUs.
Total Memory	No option	Total amount of low voltage DDR3 present on the system
System Date	Day of week, month/ day/year	Specifies the current system date Note: The date is in month/day/year format.
System Time	Hour:Minute:Second	Specifies the current system time. Note: The time is in 24 hour format.

8.4 Advanced Setup

Select the advanced tab from the setup menu to enter the advanced BIOS setup screen. The menu is used for setting advanced features and only features described within this user's guide are listed.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Watchdog				
	Graphics				
	Hardware Health Monitoring				
	Trusted Computing				
	RTC Wake				
	Reserve Legacy Interrupt				
	ACPI				
	Super IO				
	Intel(R) Smart Connect Technology				
	Serial Port Console Redirection				
	CPU Configuration				
	PPM Configuration				
	Thermal Configuration				
	IDE Configuration				
	Miscellaneous Configuration				
	SCC Configuration				
	PCI Subsystem Settings				
	Network Stack				
	CSM Configuration				
	Trusted Computing				
	USB				
	Platform Trust Technology				
	Security Configuration				
	Intel(R) I211 Gigabit Network #1				
	Intel(R) I211 Gigabit Network #2				
	Driver Health				

8.4.1 Watchdog Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup of the boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One-time Trigger Single Event Repeated Event	Select the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to 'One-time Trigger' the watchdog will be disabled after the first trigger. If set to 'Single Event', every stage will be executed only once, then the watchdog will be disabled. If set to 'Repeated Event' the last stage will be executed repeatedly until a reset occurs.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Select the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event, see note below.
Event 2	**Disabled** ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 3 is reached.

Feature	Options	Description
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Select the timeout value for the first stage watchdog event.
Timeout 2	See above	Select the timeout value for the second stage watchdog event.
Timeout 3	See above	Select the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

In ACPI mode, it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

8.4.2 Graphics Submenu

Feature	Options	Description
Boot Display Device	VBIOS Default	
CRT	**Enable** Disable	Enable or disable CRT interface
Active LFP	No LVDS **LVDS** eDP	Select the active local flat panel configuration.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel. If no external EDID data set is found, the data set selected under 'Local Flat Panel Type' will then be used as a fallback data set.
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 2x24 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.
Backlight Inverter Type	None **PWM** I2C	Select the type of backlight inverter used. PWM = Use IGD PWM signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.
Digital Display Interface 1 (DDI1)	Disabled **DisplayPort** HDMI/DVI Auto	Select the output type of the digital display interface.
PWM Inverter Frequency (Hz)	**200** - 40000	Set the PWM inverter frequency in Hz. Only visible if 'Backlight Inverter Type' is set to 'PWM'.
PWM Inverter Polarity	**Normal** Inverted	Select PWM inverter polarity. Only visible if 'Backlight Inverter Type' is set to 'PWM' .
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%**	Actual backlight value in percent of the maximum setting.

Feature	Options	Description
Force LVDS Backlight	**No** Yes	Force LVDS Enable and LVDS VDD Signals unconditionally
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
LVDS SSC	**Disabled** Enabled	Configures LVDS Spread Spectrum Clock Modulation (SSC) depth. It uses center spreading and a fixed modulation frequency of 32.9khz.

8.4.3 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	No option	Displays the actual CPU Temperature in °C.
Board Temperature	No option	Displays the actual module board temperature in °C.
TS AMBIENT DXP	No option	Displays the actual module environment temperature in °C.
DIMM DXP	No option	Displays the actual module DIMM DXP Temperature in °C.
3.3V Standard	No option	Displays the actual voltage of the 3.3V standard power supply.
5V Standby	No option	Displays the actual voltage of the 5V standby power supply.
12V Standard	No option	Displays the actual voltage of the 12V standard power supply.
VCORE	No option	Displays the actual voltage of the VCORE power supply.
System Fan Speed	No option	Displays the actual System Fan Speed in RPM.
CPU Fan Speed	No option	Displays the actual CPU Fan Speed in RPM.
System Fan Mode	Smart Mode **PWM Mode**	Configures the System Fan Mode
System Fan PWM Speed Setting	0%, 10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, **100%**	Select minimum/start fan speed to be set when the start temperature of the control slope is reached.
CPU Fan Speed Mode	Smart Mode **PWM Mode**	Configures the CPU Fan Speed Mode
Minimum Fan Speed	0%, 10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, **100%**	Select minimum/start fan speed to be set when the start temperature of the control slope is reached.

8.4.4 Trusted Computing Submenu

Feature	Options	Description
Security Device Support	**Disabled** Enabled	Enable or disable TPM support. System reset is required after change.
User Confirmation	Disabled **Enabled**	Enable or disable user confirmation requests for certain transactions.
TPM State	**Disabled** Enabled	Enable or disable TPM chip. Note: System might restart several times during POST to acquire target state.
Pending operation	**None,** Enable Take Ownership, Disable Take Ownership, TPM Clear	Perform selected TPM chip operation. Note: System might restart several times during POST to perform selected operation.

8.4.5 RTC Wake Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour		Specify wake up hour. For example, enter “3” for 3am and “15” for 3pm.
Wake up minute		Specify wake up minute.
Wake up second		Specify wake up second.

8.4.6 Reserve Legacy Interrupt Submenu

Feature	Options	Description
Reserve Legacy Interrupt 1	None, IRQ3, IRQ4, IRQ5, IRQ6, IRQ10, IRQ11, IRQ14, IRQ15	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.
Reserve Legacy Interrupt 2	Same as Reserve Legacy Interrupt 1	Same as Reserve Legacy Interrupt 1
Reserve Legacy Interrupt 3	Same as Reserve Legacy Interrupt 1	Same as Reserve Legacy Interrupt 1

8.4.7 ACPI Submenu

Feature	Options	Description
Enable ACPI Auto Configuration	Disabled Enabled	Enable or disable BIOS ACPI Auto Configuration
Enable Hibernation	Disabled **Enabled**	Enable or disable system's ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend.
Lock Legacy Resources	**Disabled** Enabled	Enable or disable locking of legacy resources.
LID Support	Disabled **Enabled**	Configure COM Express LID# Signal to act as a ACPI lid.
Sleep Button Support	Disabled **Enabled**	Configure COM Express SLEEP# Signal to act as a ACPI sleep button.

8.4.8 SIO Submenu

Feature	Options	Description
Super IO Chip		NCT6791D
▶Serial Port 1	No option	Serial Port 1 submenu
▶Serial Port 2	No option	Serial Port 2 submenu

8.4.8.1 Serial Port 1 Submenu

Feature	Options	Description
Use this Device	Enable **Disable**	Enable logical device
Logical Device Settings	No option	Show current logical device settings
Possible	**Use Automatic Settings** IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11, 12; DMA;	Serial Port 1 configurations options

8.4.8.2 Serial Port 2 Submenu

Feature	Options	Description
Use this Device	Enable **Disable**	Enable logical device
Logical Device Settings	No option	Show current logical device settings
Possible	**Use Automatic Settings** IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11, 12; DMA;	Serial Port 2 configurations options

8.4.9 Intel(R) Smart Connect Technology Submenu

Feature	Options	Description
ISCT Support	**Disabled** Enabled	Enable or disable Intel(R) Smart Connection Support. When this setup node is set to Disabled, all the other nodes will not be visible.
ISCT Notification Control	Disabled **Enabled**	Enable or Disable ISCT Notification Control.
ISCT WLAN Power Control	Disabled **Enabled**	Enable or Disable ISCT WLAN Power Control.
ISCT WWAN Power Control	Disabled **Enabled**	Enable or Disable ISCT WWAN Power Control
ISCT Sleep Duration Value Format	**Duration in Seconds**	ISCT Sleep Duration in seconds.
ISCT RF Kill Switch Type	Software **Hardware**	Select ISCT RF Kill Switch Type
ISCT RTC Timer Support	**Disabled** Enabled	Enable ISCT RTC Timer

8.4.10 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
►Console Redirection Settings	submenu	Opens console redirection configuration sub menu.
Serial Port for Out-of-Band Management / EMS Console Redirection	**Disabled** Enabled	Enable or disable Serial Port for Out-of-Band Management / Windows Emergency Management Services.
►Console Redirection Settings	Submenu	Opens console redirection configuration sub menu.

8.4.10.1 Console Redirection Settings COM0 Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.
Baudrate	9600, 19200, 38400, 57600, **115200**	Select baud rate.
Data Bits	7, **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enable or disable extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.

Feature	Options	Description
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select Function Key and KeyPad on Putty.

8.4.10.2 Console Redirection Settings Out-of-Band Management Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ **VT-UTF8** ANSI	Select terminal type.
Bits Per Second	9600, 19200, 38400, 57600, **115200**	Select baud rate.
Data Bits	**8**	Set number of data bits.
Parity	**None**	Select parity.
Stop Bits	**1**	Set number of stop bits.

8.4.11 CPU Configuration Submenu

Feature	Options	Description
▶Socket 0 CPU Information	Submenu	Socket specific CPU information.
▶CPU Thermal Configuration	Submenu	CPU thermal configuration options.
CPU Speed	No option	Displays the CPU clock frequency.
64-bit	No option	Displays 64-bit support information.
Limit CPUID Maximum	**Disabled** Enabled	When enabled, the processor limits the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When disabled, the processor returns the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Execute Disable Bit	Disabled **Enabled**	Enable or disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled, certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting OS.
Intel Virtualization Technology	Disabled **Enabled**	Enable or disable support for the Intel virtualization technology.
Power Technology	Disable **Energy Efficient** Custom	Configure the power technology schema for the CPU

8.4.11.1 Socket 0 CPU Information Submenu

Feature	Options	Description
CPU Name	No option	Displays socket specific CPU name
CPU Signature	No option	Displays CPU signature number
Microcode Patch	No option	Displays the CPU microcode patch number
Max. CPU Speed	No option	Displays the maximal CPU clock frequency
Min. CPU Speed	No option	Displays the minimal CPU clock frequency
Processor Cores	No option	Displays the number of CPU core on Socket CPU
Intel HT Technology	No option	Displays the Intel HT Technology support information.
Intel VT-x Technology	No option	Displays the Intel VT-x Technology support information
L1 Data Cache	No option	Displays the Socket L1 data cache information
L1 Code Cache	No option	Displays the Socket L1 code cache information
L2 Cache	No option	Displays the Socket L2 data cache information
L3 Cache	No option	Displays the Socket L3 data cache information

8.4.11.2 CPU Thermal Configuration Submenu

Feature	Options	Description
DTS	Enabled **Disabled**	Enable or Disable CPU Digital Thermal Sensor (DTS). DTS is used on ACPI functions to read the CPU temperature. This value is read from MSR.

8.4.12 PPM Configuration Submenu

Feature	Options	Description
CPU C state Report	Disabled **Enabled**	Enable or disable CPU state Report to Operating System.
Max CPU C state	C7 C6 **C1**	Maximal CPU C state supported by the CPU
SOix	**Disabled** Enabled	Enable or disable CPU SOix state support

8.4.13 Thermal Configuration Submenu

Feature	Options	Description
Critical Trip Point	110 C **105 C** 100 C 90 C 87 C 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Temperature of the ACPI critical Trip Point in which the OS will shut the system off.
Passive Trip Point	110 C 105 C 100 C 95 C **90 C** 87 C 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Temperature of the ACPI passive Trip Point in which the OS will begin throttling the processor.

Note

The conga-IA3 does not support active trip point.

8.4.14 IDE Configuration Submenu

Feature	Options	Description
Serial-ATA (SATA)	**Enabled** Disabled	Enable or disable the onboard SATA controller.
SATA Test Mode	Enabled **Disabled**	Should be set to Disabled. Test Mode is used just for verification measurements.
SATA Speed Support	Gen1 **Gen2**	Indicates the maximum speed the SATA controller can support.
SATA ODD Port	Port 0 ODD Port 1 ODD **No ODD**	Configure which SATA Port is ODD.
SATA Mode	IDE Mode **AHCI Mode**	Configure SATA Port Mode
Serial-ATA Port 0	**Enabled** Disabled	Enable or disable the SATA Port 0.
SATA Port 0 Hot Plug	**Disabled** Enabled	Select hot plug support for SATA Port 0. Not possible in Native IDE mode.
Serial-ATA Port 1	**Enabled** Disabled	Enable or disable the SATA Port 1.
SATA Port 1 Hot Plug	**Disabled** Enabled	Select hot plug support for SATA Port 1. Not possible in Native IDE mode.
SATA Port 0 Information	No Option	Displays Information of device detected on SATA Port 0.
SATA Port 1 Information	No Option	Displays Information of device detected on SATA Port 1.

8.4.15 Miscellaneous Configuration Submenu

Feature	Options	Description
High Precision Timer	**Enabled** Disabled	Enable or disable the high precision event timer.
Boot Timer with HPET Timer	Enabled **Disabled**	Allow boot timer calculation with the high precision event timer.
PCI Express Dynamic Clock Gating	Enabled **Disabled**	Enable dynamic clock gating.

8.4.16 SCC Configuration Submenu

Feature	Options	Description
SCC Device Mode	ACPI Mode PCI Mode	Configure the storage control cluster working mode.
SCC eMMC Support	Enable eMMC 4.5 Support Enable eMMC 4.41 Support **eMMC AUTO MODE** Disable	Enable SCC eMMC support and configure eMMC mode.
SCC 4.5 DDR50 eMMC Support	**Enabled** Disabled	Enable DDR50 eMMC support.
SCC 4.5 HS200 eMMC Support	Enabled **Disabled**	Enable DDR50 eMMC support.
eMMC Secure Erase	Enabled **Disabled**	Enable eMMC secure erase support.
SCC SD Card Support	**Enabled** Disabled	Enable storage control cluster SD Card support
SDR25 Support for SD Card	Enabled **Disabled**	Enable SDR25 Support for SD Card
DDR50 Support for SD Card	**Enabled** Disabled	Enable DDR50 Support for SD Card

8.4.17 PCI Subsystem Setting Submenu

Feature	Options	Description
PCI Bus Driver Version		
PCI Latency Timer	**32,** 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
PCI-X Latency Timer	32, **64,** 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI-X latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate SERR#.
Above 4G Decoding	**Disabled** Enabled	Enable or Disable 64bits capable Devices to be Decoded in Above 4G Address Space (Only if system supports 64 bits PCI Decoding)
SR-IOV Support	**Disabled** Enabled	If system has SR-IOV capable PCIe Devices, this option enables or disables Single Root IO Virtualization support

Feature	Options	Description
▶PCI Express Settings	Submenu	PCI Express Settings Submenu
▶PCI Express GEN 2 Settings	Submenu	PCI Express Settings Submenu

8.4.17.1 PCI Express Setting Submenu

Feature	Options	Description
Relaxed Ordering	**Disabled** Enabled	Enable or disable PCI Express device relaxed ordering.
Extended Tag	**Disabled** Enabled	If enabled a device may use an 8-bit tag filed as a requester.
No Snoop	Disabled **Enabled**	Enable or disable PCI Express device 'No Snoop' option.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum payload of PCI Express devices or allow system BIOS to select the value.
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum read request size of PCI Express devices or allow system BIOS to select the value.
ASPM	**Disabled** Auto Forced L0s	PCI Express Active State Power Management settings.
Extended Synch	**Disabled** Enabled	If enabled, the generation of extended PCI Express synchronization patterns is allowed.
Link Training Retry	Disabled, 2, 3, **5**	Defines number of retry attempts software will take to retrain the link if previous training attempt was unsuccessful.
Link Training Timeout (us)	10-10000 **Default : 100**	Defines number of microseconds software will wait before polling link training bit in the link status register. Value ranges from 10 to 10000 us.
Unpopulated Links	**Keep Link On** Disabled	In order to save power, software will disable unpopulated PCI Express links, if this option is set to disabled.
Restore PCIe Registers	Enabled **Disabled**	On non-PCI Express aware operating systems some devices may not be re-initialized correctly after S3. Setting this node to Enabled restores PCI Express configuration on S3 resume. Warning: Enabling this may cause issues with other hardware after S3 resume.

8.4.18 PCI Express GEN 2 Settings Submenu

Feature	Options	Description
PCI Express GEN2 Device Register Settings		
Completion Timeout	**Default** Shorter Longer Disable	In device Functions that support Completion Timeout programmability, allows system software to modify the Completion Timeout value. 'Default' 50us to 50ms. If 'Shorter' is selected, software will use shorter timeout ranges supported by hardware. If 'Longer' is selected, software will use longer timeout ranges.
ARI Forwarding	**Disabled** Enabled	If supported by hardware and set to 'Enabled', the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type1 Configuration Request into a Type0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. Default value: Disabled
AtomicOp Requester Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this function initiates AtomicOp Requests only if Bus Master Enable bit is in the Command Register Set.
AtomicOp Egress Blocking	**Disabled** Enabled	If supported by hardware and set to 'Enabled', outbound AtomicOp Requests via Egress Ports will be blocked.
IDO Request Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated.
IDO Completion Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated.
LTR Mechanism Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this enables the Latency Tolerance Reporting (LTR) Mechanism.
End-End TLP Prefix Blocking	**Disabled** Enabled	If supported by hardware and set to 'Force to 2.5 GT/s' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.
PCI Express GEN2 Link Register Settings		
Target Link Speed	**Auto** Force to 2.5 GT/s Force to 5.0 GT/s	If supported by hardware and set to 'Force to 2.5 GT/s' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.
Clock Power Management	**Disabled** Enabled	If supported by hardware and set to 'Enabled', the device is permitted to use CLKREQ# signal for power management of Link clock in accordance to protocol defined in appropriate form factor specification.
Compliance SOS	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this will force LTSSM to send SKP Ordered Sets between sequences when sending Compliance Pattern or Modified Compliance Pattern.
Hardware Autonomous Width	**Disabled** Enabled	If supported by hardware and set to 'Disabled', this will disable the hardware's ability to change link width except width size reduction for the purpose of correcting unstable link operation.
Hardware Autonomous Speed	**Disabled** Enabled	If supported by hardware and set to 'Disabled', this will disable the hardware's ability to change link speed except speed rate reduction for the purpose of correcting unstable link operation.

8.4.19 Network Stack

Feature	Options	Description
Network Stack	Enabled **Disabled**	Enable or disable the UEFI network stack.
Ipv4 PXE Support	Enabled **Disabled**	Enable Ipv4 PXE boot support. If disabled IPV4 PXE boot option will not be created.
Ipv6 PXE Support	Enabled **Disabled**	Enable Ipv6 PXE boot support. If disabled IPV6 PXE boot option will not be created.
PXE boot wait time	0-**5**	Wait time to press ESC to abort PXE Boot

8.4.20 CSM Submenu

Feature	Options	Description
Launch CSM	**Enabled** Disabled	Enable the Compatibility Support Module.
CSM16 Module Version	No option	Display CSM Module Version number.
Gate A20 Active	**Upon Request** Always	Configure legacy Gate A behavior.
Option ROM Messages	**Force BIOS** Keep Current	Enable Option ROM message
INT19 Trap Response	**Immediate** Postponed	Define BIOS reaction on INT19 trapping by Option ROM: Immediate executes the trap right away. Postpone executes the trap during legacy boot.
Boot Option Filter	UEFI and Legacy **Legacy Only** UEFI Only	Controls which devices / boot loaders the system should boot to.
Network	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and legacy Network option ROMs.
Storage	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and legacy Storage option ROMs.
Video	Do not launch UEFI only **Legacy only**	Controls the execution of UEFI and legacy Video option ROMs
Other PCI Devices	**UEFI only** Legacy only	Controls the execution of UEFI and legacy option ROMs for any other PCI device different to Network, Video and Storage.

8.4.21 SDIO Submenu

Feature	Options	Description
SDIO Access Mode	**Auto** DMA PIO	Controls the SDIO Access mode to the device.

8.4.22 USB Submenu

Feature	Options	Description
USB Module Version	No option	Displays the version of the USB module.
USB Devices	No option	Displays the detected USB devices.
xHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without xHCI hand-off support. The xHCI ownership change should be claimed by xHCI OS driver.
EHCI Hand-off	**Disabled** Enabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI OS driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable Mass Storage Driver Support.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device start unit command timeout.
USB Transfer Timeout	1 sec 5 sec 10 sec **20 sec**	The timeout value for control, bulk, and interrupt transfers.
Device Power -Up Delay Selection	**Auto** Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power -Up Delay Value	0-40 Default : **5**	Actual power-up delay value in seconds.

8.4.23 Platform Trust Technology

Feature	Options	Description
fTPM	**Disabled** Enabled	Enable Trusted Platform Module support.

8.4.24 Security Configuration

Feature	Options	Description
TXE	**Enabled** Disabled	Enable Trusted Execution Engine.
TXE HMRFPO	Enable **Disable**	Enable Host ME Region Flash Protection Overwrite.
TXE Firmware Update	**Enabled** Disabled	Enable Firmware update.
TXE EOP Message	**Enabled** Disabled	Enable TXE End of Post Message.
TXE Unconfiguration Perform	No option	Execute a TXE unconfiguration command
Intel(R) Anti-Theft Technology Configuration	No option	
Intel(R) AT	Enabled Disabled	Enable Anti-Theft technology.
Intel(R) AT Platform PBA	Enabled **Disabled**	Enable Anti-Theft Platform Pre-boot Authentication.
Intel(R) AT Suspend Mode	Enabled **Disabled**	Enable Anti-Theft Suspend Mode.

8.4.25 Intel(R) Ethernet Connection I210 Submenu

At this submenu additionally to its title the MAC address is displayed at the end of the title.

Feature	Options	Description
► NIC Configuration	submenu	Opens the NIC Configuration submenu.
Blink LEDs	0-15 Default : **0**	The Ethernet LEDs will blink so many seconds long as entered.
UEFI Driver	No option	Displays the UEFI Driver version.
Adapter PBA	No option	Displays the Adapter PBA.
Chip Type	No option	Displays the type of the Chip in which the Ethernet controller is integrated.
PCI Device ID	No option	Displays the PCI Device ID of the Ethernet controller.
Bus:Device:Function	No option	Displays the PCI Bus:Device:Function number of the Ethernet controller.
Link Status	No option	Displays the Link Status.
MAC Address	No option	Displays the MAC Address.

8.4.25.1 NIC Configuration Submenu

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake on LAN	Disabled **Enabled**	Enables Wake on LAN (WOL) feature

8.4.26 Driver Health Submenu

Feature	Options	Description
► Intel(R) PRO/1000	No option	Provides Health Status for the drivers/Controllers connected to the System

8.4.26.1 Intel(R) PRO/1000 Submenu

Feature	Options	Description
Controller Information	No option	Provides Health Status of the controller

8.5 Chipset Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

8.5.1 North Bridge Submenu

Feature	Options	Description
Memory Information		
Total Memory	No option	Total amount of memory detected by the system
Memory Slot 0	No option	Memory detected by the system on Slot 0
Memory Slot 1	No option	Memory detected by the system on Slot 1
Max TOLUD	**Dynamic**, 2 GB, 2.25 GB, 2.5 GB, 2.75 GB, 3 GB,	Maximum value of TOLUD Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.
Aperture Size	128MB **256MB** 512MB	Select Aperture Size

Feature	Options	Description
PAVC	Enable **Disable**	Enable/Disable Protected Audio Video Control

8.5.2 South Bridge Submenu

Feature	Options	Description
▶Azalia HD Audio	Submenu	Azalia HD Audio Submenu.
▶ USB	Submenu	USB Submenu.
▶ PCI Express Configuration	Submenu	PCI Express Configuration Submenu.
High Precision Timer	**Enabled** Disabled	Enable High Precision Event Timer.
Serial IRQ	**Quiet** Continuous	Configure IRQ Serial Mode
Global SMI Lock	**Enabled** Disabled	Enable or Disable SMI Lock
BIOS Read/Write Protection	Enabled **Disabled**	Enable BIOS SPI Region read/write protection.
Isolate SMBus Segments	**Never** During POST Always	Allows isolating the off-module/external SMBus segment from the on-module SMBus segment. This can be a workaround for non spec conform external SMBus devices.

8.5.2.1 Azalia HD Audio

Feature	Options	Description
LPE Audio Support	**Disable** LPE Audio PCI Mode LPE Audio ACPI Mode	Enable LPE Audio Support.
Audio Controller	**Enabled** Disabled	Enable Audio Controller.
Azalia Vci Enable	**Enabled** Disabled	Enable Azalia Vci.
Azalia Docking Support Enable	Enable **Disable**	Enable Azalia Docking support.
Azalia PME Enable	**Enabled** Disabled	Enable Azalia PME support.
Azalia HDMI Codec	**Enabled** Disabled	Enable Azalia HDMI Codec
HDMI Port B	**Enabled** Disabled	Enable HDMI Port B Audio.

Feature	Options	Description
HDMI Port C	Enabled **Disabled**	Enable HDMI Port C Audio.

8.5.2.2 USB Submenu

Feature	Options	Description
USB OTG Support	**Disabled** Enabled	Enable USB OTG support.
USB VBUS	**On** Off	VBUS should be On in Host Mode and it should be Off in OTG device Mode.
XHCI Mode	Enabled Disabled Auto **Smart Auto**	USB3.0 mode support on USB0, USB1, USB2 and USB3 ports Disabled – USB ports will function in USB2.0 mode only. No USB3.0 OS driver required. The USB ports will be routed to EHCI1 controller. Enabled – USB ports will function correctly in BIOS but the ports on which the USB3.0 mode is enabled (see USB0 port USB3.0 item) will not function at all under OS if the USB3.0 OS driver is not installed. USB ports will not function in pre-OS time if USB3.0 Support in BIOS is disabled (see the USB3.0 Support in BIOS item). Auto – USB ports are initially set to operate in USB2.0 Mode and the USB3.0 OS driver (if available) will switch them USB3.0 mode. If USB3.0 OS driver is not available than the ports will function correctly but they will operate in USB2.0 mode. Smart Auto – The BIOS will store the USB mode set by the OS and at next boot the BIOS will set this previously used mode. At G3 boot (first boot after mechanical disconnection of the power supply) the USB ports will function identically as in Auto mode. This mode is not available when Disabled is selected at USB3.0 Support in BIOS item.
USB2 Link Power Management	Disabled **Enabled**	Enable USB2 Link Power Management
USB 2.0(EHCI) Support	**Disabled** Enabled	Control USB EHCI (USB 2.0) functions.
USB Per Port Control	Disabled **Enabled**	Control each of the USB ports (0-3).
USB Port 0	Disabled **Enabled**	Enable Port 0
USB Port 1	Disabled **Enabled**	Enable Port 1
USB Port 2	Disabled **Enabled**	Enable Port 2
USB Port 3	Disabled **Enabled**	Enable Port 3

8.5.2.3 PCI Express Configuration Submenu

Feature	Options	Description
PCIe noncompliance Card	**Not Supported** Supported	Enable PCIe 1.0 Device Support
PCI Express Port 0/1/2/3	Disabled **Enabled**	Enable PCIe Port 0/1/2/3.
ASPM	**Disabled** L0s L1 L0sL1 Auto	PCI Express Active State Power Management settings.
Hot Plug	**Disabled** Enabled	Select hot plug support for PCIe Port
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 0/1/2/3 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
Extra Bus Reserved	0-7 **Default : 0**	Extra bus reserved (0-7) for bridges behind this root bridge.
Reserved Memory	1-20 **Default : 10**	Reserved memory range for this root bridge.
Prefetchable Memory	1-20 **Default : 10**	Prefetchable memory range for this root bridge.
Reserved I/O	0-20 **Default : 4**	Reserved I/O range for this root bridge.

8.6 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

8.6.1 Boot Settings Configuration

Feature	Options	Description
Setup Prompt Timeout	**1** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot (not recommended), 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. Note: The default OEM logo is a dark screen.

Feature	Options	Description
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The "Device Based" boot priority list allows you to select from a list of currently detected devices only. The "Type Based" boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the "Device Based" boot priority list might change dynamically in cases when devices are physically removed or added to the system. The "Type Based" boot menu is static and can only be changed by the user.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. Note: Only works with an ATX type power supply.
AT Shutdown Mode	System Reboot **Hot S5**	Determines the behavior of an AT-powered system after a shutdown.
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
Fast Boot	**Disabled** Enabled	Enable or disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS / legacy boot options.

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

8.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

8.7.1 Security Settings

Feature	Options	Description
Administrator Password	Enter password	Specifies the setup administrator password.
HDD Security Configuration		
List of all detected hard disks supporting the security feature set	Select device to open device security configuration submenu	

8.7.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

8.8 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen. You can display a Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
Boot Override	
List of all boot devices currently detected	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to “Device Based”.

9 Additional BIOS Features

The conga-IA3 uses a congatec/AMI AptioEFI that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility (version 1.5.0 and later), which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as IA32R1xx and IC32R1xx where :

- IA32 is the BIOS for modules with Intel Atom Dual Channel Memory SoC
- IC32 is the BIOS for modules with Intel Celeron Dual Channel Memory SoC
- R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

The binary size of IA32 and IC32 BIOS is 8MB.

9.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility (CGUTLm1x.pdf) on the congatec website at www.congatec.com.

10 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.3	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0	http://www.serialata.org
Intel® Thin Mini-ITX Design Guide (thin-mini-itx-based-pc-system-design-guide-rev-1-2.pdf)	http://www.intel.com
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications