conga-HPC/sILH

COM-HPC® 1.10 Server Size D Module with Next Generation Intel® Ice Lake Processors

User's Guide

Revision 1.02

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.01	2023-07-04	AEM	• Preliminary release
1.00	2024-05-27	AEM	• Updated the title page • Updated section 2.3 "Mechanical Dimensions" • Updated the tables in sections 2.5 "Power Consumption" and 2.6 "Supply Voltage Battery Power" • Added section 2.8 "Storage Specifications" • Added note about the storage of congatec cooling solutions to section 4 "Cooling Solutions" • Added note about MAC address programming to section 5.2 "NBASE-T Ethernet" • Updated section 5.12 "I²C" and section 5.13 "SMBus" • Added section 5.15.1 "inrush and Maximum Current Peaks" • Updated section 6.1.8 "Power Loss Control" • Added note to section 7.1.3 "Intel Turbo Boost Technology" • Added section 9 "System Resources" • Official release
1.01	2024-12-03	AEM	• Added note about 3D models to section 2.3 "Mechanical Dimensions" • Updated the note in section 2.8.2 "Cooling Solution" • Added note to the cooling dimensions in section 4.1 "CSA Dimensions", 4.2 "HSP Dimensions" • Added section 4.5 "Retention Frame Dimensions" • Added note about MAC address programming to section 5.2 "NBASE-T Ethernet" and table 24 "NBASE-T Ethernet Signal Descriptions" • Added a note about PCIe Gen 4 routing to section 5.1.2 "PCIe Gen 4" • Added note about Turbo mode to section 7.1.3 "Intel Turbo Boost Technology"
1.02	2025-02-17	AEM	• Added software licences and WEEE directive to the preface section • Corrected a typographical error in section 1.1 "COM-HPC Concept" • Added new variants with PN:050995 and PN:050996 • Added a note to sections 1.2 "Options Information" and 8.2.2 "Intel® Turbo Boost Technology " • Added a note to section 2.3 "Mechanical Dimensions" • Added new sections 2.8 Storage Specifications • Added a caution to section 4 "Cooling Solutions" • Added section 5.5.3 "IEEE 1588 and Time Synchronization" • Updated the note for ETH0-7_SDP signals in table 22 "Connector J2 Pinout" and table 25 "Ethernet KR and KX Signal Descriptions" • Added a note to section 6.1 "NBASE-T Ethernet"

Preface

This user's guide provides information about the components, features, connectors and system resources available on the conga-HPC/sILH. It is one of three documents that should be referred to when designing a COM-HPC application. The other reference documents that should be used include the following:

- COM-HPC Module Base Specification
- COM-HPC Carrier Design Guide

These documents are available on the PICMG website at www.picmg.org. Additionally, check the restricted area of the congatec website at **www.congatec.com** and the website of the respective silicon vendor for relevant documents (Erratum, PCN, Sighting Reports and others).

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Note

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Terminology

Term	Description
CSA	Active Cooling Solution
CSP	Passive Cooling Solution
DTR	Dynamic Temperature Range
GB	Gigabyte
GHz	Gigahertz
MB	Megabyte
Gbps	Gigabit per second
HSP	Heatspreader
Mbps	Megabit per second
MTps	Megatransfer per second
kHz	Kilohertz
MHz	Megahertz
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
PCH	Platform Controller Hub
SM	System Management
BMC	Baseboard Management Controller
N.C	Not connected
N.A	Not available
RDIMM	Registered Dual In-Line Memory Module
TBD	To be determined
UDIMM	Unregistered Dual In-Line Memory Module

Contents

List of Tables

1 Introduction

1.1 COM-HPC Concept

COM-HPC is an open standard defined specifically for high performance Computer-on-Modules (COMs) for embedded systems. The defined module types are client module with fixed input voltage, client module with variable input voltage and server module with fixed input voltage.

The COM-HPC modules are available in the following form factors:

- Mini 95 mm x 70 mm
- Size A 95 mm x 120 mm
- Size B 120 mm x 120 mm
- Size C 160 mm x 120 mm
- Size D 160 mm x 160 mm
- Size E 200 mm x 160 mm

Table 1 COM-HPC Interface Summary

Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
Ethernet	NBASE-T	1 / 2	1 / 2	1 / 1	
	KR/KX	N.A	0 / 2	2 / 8	
	SGMII	0 / 2	N.A	N.A	
Storage	SATA	0 / 2	0 / 2	0 / 2	Pin is shared with PCIe on mini module
PCIe	Lane 0-47	1 / 16	4 / 48	8 / 48	Two PCIe reference clock output pairs required on mini module
	Lane 48-63	N.A	N.A	0 / 16	
	BMC	N.A	0 / 1	1 / 1	
USB	USB 2.0 Ports 0-7	6 / 8	4 / 8	4 / 8	Ports 0-5 (mini module) or ports 0-3 (server/client module) are used for USB 3.2 and USB4 if implemented.
	USB 3.2 Gen 1 or Gen 2	0 / 5	0 / 4	0 / 2	Requires one SuperSpeed Tx pair and one Rx pair per port
	USB 3.2 Gen 2x2	0 / 4	0 / 4	0 / 2	Requires two SuperSpeed Tx pairs and two Rx pairs per port
	USB4	0 / 4	0 / 4	0 / 2	USB4 ports use USB 3.2 Gen 2x2 ports
SPI	eSPI	0 / 1	0 / 1	0 / 1	
	Boot SPI	1 / 1	1 / 1	1 / 1	
	General Purpose SPI	1 / 1	1 / 1	1 / 1	

Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
BIOS Select	-	1 / 1	1 / 1	1/1	
Display	DDI	0 / 2	1 / 3	N.A	Additional display outputs may be available on the USB4 interface. On mini module, DDI pins are shared with USB4.
	eDP	0 / 1	0 / 1	N.A	
MIPI	DSI	0 / 1	0 / 1	N.A	
	CSI	N.A [1]	0 / 2	N.A	[1] Optional FFC connectors for MIPI-CSI on the mini module.
Audio	SoundWire	0 / 2	0 / 2	N.A	I2S pins may be used for one HDA port or two additional SoundWire ports for a total of up to four SoundWire ports.
	I2S	0 / 1	0 / 1	N.A	
Other Serial Ports	I2C	2 / 3	2 / 2	2 / 2	I2C0 and I2C1 for client and server modules. The mini module supports a third I2C port (I2C2/MDIO (for SGMII PHY setup).
	SMBus	1 / 1	1 / 1	1 / 1	
	IPMB	N.A	0 / 1	0 / 1	
	UART	0 / 2	0 / 2	1 / 2	
GPIO	-		12 / 12	12 / 12	
Miscellaneous	Watchdog Timer	0 / 1	0 / 1	0 / 1	
	Fan (PWM and tachometer)	1 / 1	1 / 1	1 / 1	
FuSa	FuSa set of signals	0 / 1	0 / 1	0 / 1	
Power Rails	VCC	12 / 12	28 / 28	28 / 28	
	VCC_5V-SBY	N.A	0 / 2	0 / 2	The mini module does not have 5V standby pins.
	VCC_RTC	1 / 1	1 / 1	1 / 1	
	GND	All	All	All	All available GND pins shall be used.
Connector	J1	1 / 1	1 / 1	1 / 1	
	J2	N.A	0 / 1	1 / 1	

1.2 The conga-HPC/sILH

The conga-HPC/sILH is a COM-HPC server module with fixed input voltage. The module uses PCB Size D definition and it complies with COM-HPC specification 1.1.

The conga-HPC/sILH is equipped with two high performance connectors that ensure stable data throughput, and support high bandwidth networking. It provides all the core functional requirements for any embedded application when mounted onto an application-specific carrier board.

The conga-HPC/sILH features the next generation Intel® Xeon D-2700 (Ice Lake-D HCC) processors with maximum base TDP of 118 W.

1.3 Options Information

The conga-HPC/sILH is currently available in five variants (two commercial and three industrial). The tables below show the different configurations available.

Table 2 Commercial Variants

Part-No.		050910	050911
Processor		Intel® Xeon® D-2733NT 2.10 GHz 8 Cores	Intel® Xeon® D-2712T 1.9 GHz 4 Cores
Intel® Smart Cache		15 MB	15 MB
Max. Turbo Frequency		3.20 GHz	3.00 GHz
Processor Graphics		N.A	N.A
DDR4 Memory (ECC or Non-ECC)		2667 MTps quad channel (up to 512 GB) [1]	2667 MTps quad channel (up to 512 GB) [1]
Intel QAT		Yes (50 G)	No
Gigabit Ethernet	Mode	50 G	50 G
	Configuration [2]	1x 2.5 GbE 1x 50G; 2x 25 G; 4x 10 G; 5x 10 G; 4x 10 G + 4x 2.5 G; 4x 10 G + 4x 1 G (maximum aggregate bandwidth is 50 Gbps)	
PCIe Lanes	Gen 4	32 lanes	32 lanes
	Gen 3	16 lanes	16 lanes
Processor TDP		80 W	65 W
CPU Use Condition [3]		Industrial (Commercial Temperature)	Industrial (Commercial Temperature)
CPU Tcase	Min.	0°C	0°C
	Max.	83°C	86°C
CPU DTSmax		100°C	100°C
CPU DTR [4]		90°C or 145°C depending on the combined supported high speed ports	
Compatible Carrier Board		conga-HPC/EVAL-Server Evaluation Carrier Board	

Note

1. *Up to 512 GB with LRDIMMs; up to 256 GB with RDIMMs and up to 128 GB with UDIMMs.*
2. *See section 5.3.2 "Possible Ethernet Configurations (50 G SKUs) for more information.*
3. *Intel SoC use conditions. See Intel documentation for more information.*
4. *DTR is 90°C if CPU PCIe 4.0, PCH PCIe 3.0 and SATA 3 ports are supported. DTR is 145°C if CPU PCIe 3.0, PCH PCIe 2.0 and SATA 2 ports are supported (no CPU PCIe 4.0, PCH PCIe 3.0 or SATA 3 support).*

Table 3 Industrial Variants

Part-No.		050900	050901	050902	050995	050996
Processor		Intel® Xeon® D-2796TE 2.0 GHz 20 Cores	Intel® Xeon® D-2775TE 2.0 GHz 16 Cores	Intel® Xeon® D-2752TER 1.8 GHz 12 Cores	Intel® Xeon® D-2796TE 2.0 GHz 20 Cores	Intel® Xeon® D-2775TE 2.0 GHz 16 Cores
Intel® Smart Cache		30 MB	25 MB	20 MB	30 MB	25 MB
Max. Turbo Frequency [1]		3.10 GHz	3.0 GHz	2.8 GHz	3.10 GHz	3.0 GHz
Processor Graphics		N.A	N.A	N.A	N.A	N.A
DDR4 Memory (ECC or Non-ECC)		2933 MTps quad channel (up to 128 GB) [2]	2933 MTps quad channel (up to 128 GB) [2]	2667 MTps quad channel (up to 128 GB) [2]	2933 MTps quad channel (up to 128 GB) [2]	2933 MTps quad channel (up to 128 GB) [2]
Intel QAT		No	No	No	No	No
Gigabit Ethernet	Mode	100 G	100 G	50 G	100 G	100 G
	Configuration [3]	1x 2.5 GbE 1x 100 G; 2x 100 G [4]; 1x 50 G + 1x 10 G; 4x 25 G; 2x 25 G + 4x 10 G; 8x 10G; 4x 10 G (maximum aggregate bandwidth is 100 Gbps)		1x 2.5 GbE 1x 50G; 2x 25 G; 4x 10 G; 5x 10 G; 4x 10G + 4x 2.5 G; 4x 10 G + 4x 1 G (maximum aggregate bandwidth is 50 Gbps)	1x 2.5 GbE 1x 100 G; 2x 100 G [4]; 1x 50 G + 1x 10 G; 4x 25 G; 2x 25 G + 4x 10 G; 8x 10G; 4x 10 G (maximum aggregate bandwidth is 100 Gbps)	
PCIe Lanes	Gen 4	32 lanes	32 lanes	32 lanes	32 lanes	32 lanes
	Gen 3	16 lanes	16 lanes	16 lanes	16 lanes	16 lanes
USB Ports		4x USB 3.0/2.0	4x USB 3.0/2.0	4x USB 3.0/2.0	4x USB 3.0/2.0	4x USB 3.0/2.0
		4x USB 2.0	4x USB 2.0	4x USB 2.0	4x USB 2.0	4x USB 2.0
SATA (6 Gbps)		2	2	2	2	2
Processor TDP		118 W	100 W	77 W	118 W	100 W
CPU Use Condition [5]		Industrial (Extended Temperature)	Industrial (Extended Temperature)	Industrial (Extended Temperature)	Industrial (Extended Temperature)	Industrial (Extended Temperature)
CPU Tcase	Min.	-40°C	-40°C	-40°C	-40°C	-40°C
	Max.	83°C	82°C	86°C	83°C	82°C
CPU DTSmax		102°C	100°C	100°C	102°C	100°C
CPU DTR [6]		90°C or 145°C depending on the combined supported high speed ports				
Compatible Carrier Board		conga-HPC/EVAL-Server Evaluation Carrier Board				

Note

1. *Disable Turbo mode for industrial use conditions.*
2. *Up to 512 GB with LRDIMMs; up to 256 GB with RDIMMs and up to 128 GB with UDIMMs.*
3. *See section 5.3.1 "Possible Ethernet Configurations (100-G SKUs) and section 5.3.2 "Possible Ethernet Configurations (50-G SKUs)" for more information*
4. *Two ports capable of 100 Gbps; however, the maximum aggregate bandwidth is 100 Gbps (applicable for load-balancing or failover)*
5. *Intel SoC use conditions. See Intel documentation for more information.*
6. *DTR is 90°C if CPU PCIe 4.0, PCH PCIe 3.0 and SATA 3 ports are supported. DTR is 145°C if CPU PCIe 3.0, PCH PCIe 2.0 and SATA 2 ports are supported (no CPU PCIe 4.0, PCH PCIe 3.0 or SATA 3 support).*

2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	COM-HPC Size D server module (160 mm x 160 mm)	
Processor	Intel® Xeon processor D-2700 product family SoC	
Chipset	Integrated in the SoC	
Memory [1]	Four memory sockets. Supports - DDR4 ECC and non-ECC DIMM modules - Quad channel (one DIMM per channel) - Data rates up to 2933 MT/s with LRDIMMs and RDIMMs or up to 2666 MT/s with UDIMMs or up to 2400 MT/s with VLP RDIMMs - Maximum 512 GB capacity (128 GB each) with LRDIMM or 256 GB capacity (64 GB each) with RDIMM/VLP RDIMM or 128 GB capacity (32 GB each) with UDIMM	
Ethernet	Gigabit Ethernet with support for: - 1x 2500BASE-T standard interface (Intel i226 with TSN support) - 100 G [2], 50 G [3], 25 G, 10 G, 2.5 G or 1 G (see section 1.3 "Options Information" "Options Information" for more information)	
Graphics	N.A	
Audio	N.A	
Peripheral Interfaces	4x USB 2.0 (up to 4x USB 3.0) 32x PCIe Gen. 4 lanes 16x PCIe Gen. 3 lanes 2x SATA® (6 Gbps) 2x UART (16C550 compatible)	12x GPIOs I²C (fast mode, 400 KHz, multi-master) SMBus eSPI SPI
BIOS	AMI Aptio® V UEFI 2.x firmware 64 MB SPI with congatec Embedded BIOS features	
congatec Board Controller	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, hardware monitoring, fan control, I²C bus, Power loss control	
Optional Features	eMMC 5.1 up to 128 GB (BOM option) Precision Time Protocol (IEEE 1588) Synchronous Ethernet (SyncE support requires a DPLL)	
Power Management	Supports: - ACPI 5.0a compliant with battery support. - Hardware power management - Wake events from the Intel Management Engine	
Security	Discrete Trusted Platform Module 2.0 (Infineon SLB9672XU2/SLB9672VU2) New AES Instructions for faster and better encryption.	

Note

1. *See section 7.3 "Memory Population Rules" for more information.*
2. *Requires the use of four lanes.*
3. *Requires the use of two lanes and supported only in backplane mode.*

2.2 Supported Operating Systems

The conga-HPC/sILH supports the following operating systems.

- Microsoft® Windows® 10 IoT Enterprise LTSC
- Microsoft Windows Server 2019 (1809)
- Linux (Ubuntu 20.04.1 LTS kernel 5.13)
- Yocto Project
- Real Time Systems Hypervisior

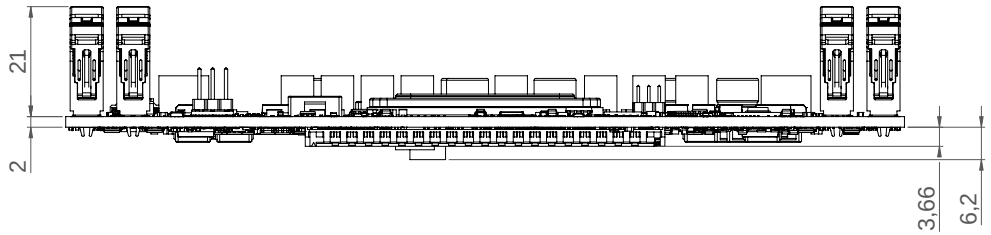
Note

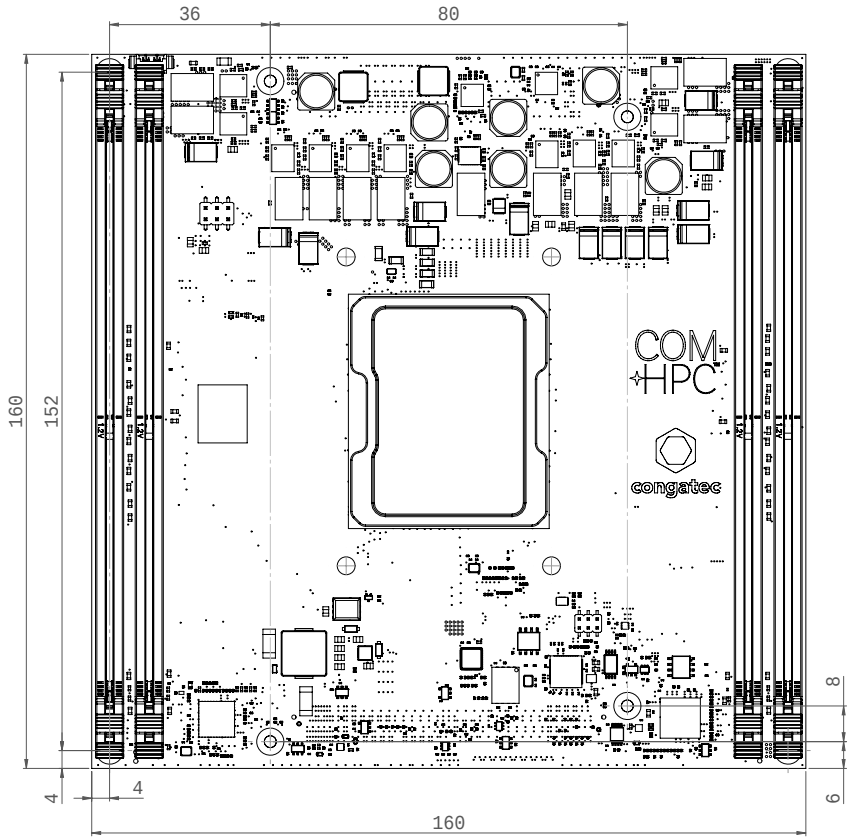
For better system performance, use only 64-bit Operating Systems.

2.3 Mechanical Dimensions

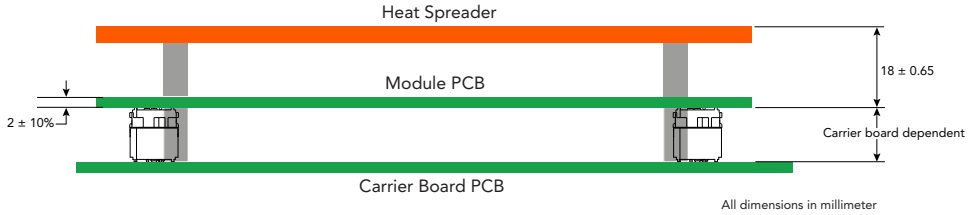
The conga-HPC/sILH has the following dimensions:

- length of 160 mm
- width of 160 mm
- height of 27.6 mm or 29.5 mm depending on variant (21.3 mm top side (DIMM sockets), 2 mm PCB and 4.3 mm or 6.2 mm bottom side)





The overall height specified for a COM-HPC size D assembly (carrier board PCB, module PCB and heatspreader) is shown below:



Note

The 3D models of congatec products are available at www.congatec.com/login. These models indicate the overall length, height and width of each product. If you need login access, contact your local sales representative.

2.4 Supply Voltage Standard Power

The conga-HPC/sILH supports 12 V DC ± 5 % input voltage.

2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for the conga-HPC/sILH (COM-HPC server module with fixed input voltage).

Power Rail	Module Pin Current Capability 20% Derated (A)	Input Range (V)	Minimum Input (V)	Max. Module Input Power at Minimum Input Voltage (W)	Assumed Conversion Efficiency	Max. Module Load Power at Minimum Input Voltage (Watts)
VCC_12V	28 * 1.12 = 31.4	12 ± 5%	11.4	358	85%	304
VCC_5V_SBY	1.12	4.75 - 5.25	4.75	5.32	100%	5.3 (with one VCC_5V_SBY pin) 10.6 (with two VCC_5V_SBY pin)
VCC_RTC	1.12	2.3 - 3.3	2.3			

2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- input voltage +12 V
- conga-HPC/sILH COM
- modified congatec carrier board
- conga-HPC/sILH cooling solution
- Microsoft Windows 10 (64 bit)

Note

The CPU was stressed to its maximum workload.

Table 5 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S5	COM is powered by VCC_SV_SBY	

Note

1. *The fan and SATA drives were powered externally.*

2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Table 6 Power Consumption Values

The table below provides additional information about the conga-HPC/sILH power consumption. The values were recorded at various operating mode.

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (A)			
					Variant	Cores	Freq. /Max. Turbo	S0: Min	S0: Max	S0: Peak	S5
050900	4 x 16 GB	A.3	HEIHR016	Windows 10	Intel® Xeon® D-2796TE	20	2.0 / 3.1 GHz	2.70	9.12	10.60	1.55
050901	4 x 16 GB	A.3	HEIHR016	Windows 10	Intel® Xeon® D-2775TE	16	2.0 / 3.1 GHz	2.68	7.54	8.69	1.56
050902	4 x 16 GB	A.3	HEIHR016	Windows 10	Intel® Xeon® D-2752TER	12	1.8 / 2.8 GHz	2.51	7.63	9.13	1.38
050910	4 x 16 GB	A.3	HEIHR016	Windows 10	Intel® Xeon® D-2733NT	8	2.1 / 3.2 GHz	2.52	8.05	9.54	1.41
050911	4 x 16 GB	A.3	HEIHR016	Windows 10	Intel® Xeon® D-2712T	4	1.9 / 3.0 GHz	2.51	6.59	7.25	1.39

2.6 Supply Voltage Battery Power

Table 7 CMOS Battery Power Consumption (Commercial Variants)

RTC @	Voltage	Current
-10°C	3V DC	1.23 µA
20°C	3V DC	1.45 µA
70°C	3V DC	2.73 µA

Table 8 CMOS Battery Power Consumption (Industrial Variants)

RTC @	Voltage	Current
-50°C	3V DC	2.25 µA
20°C	3V DC	3.23 µA
95°C	3V DC	4.93 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-HPC/sILH.*

2.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to 85°C	(commercial variants)
Temperature	Operation: -40° to 85°C	Storage: -40° to 85°C	(industrial variants)
Relative Humidity	Operation: 10% to 90%	Storage: 5% to 95%	

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

2.8 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

2.8.1 Module

For long-term storage of the conga-HPC/sILH (more than six months), keep the conga-HPC/sILH in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

Note

We do not recommend storing the conga-HPC/sILH for more than five years under these conditions.

2.8.2 Cooling Solution

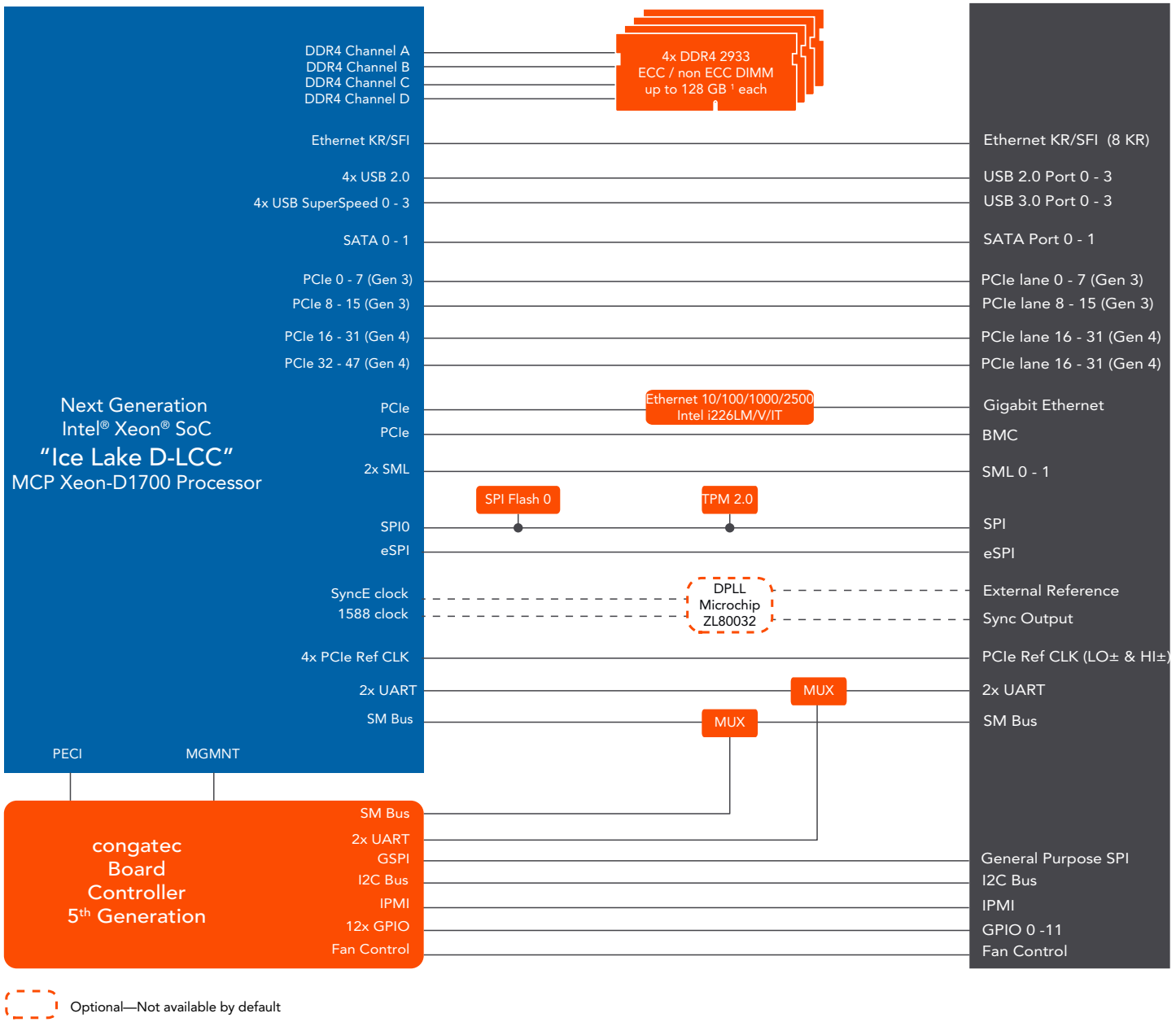
The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. For optimal cooling performance, do not store the heatspreaders/cooling solutions at temperatures below -20°C.

Caution

1. *For temperatures between -10°C and -20°C, preheat the heatpipes before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your local sales representative.*

2. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

3 Block Diagram



[1] Maximum 512 GB capacity (128 GB each) with LRDIMMs or 256 GB capacity (64 GB each) with RDIMMs/VLP RDIMMs or 128 GB capacity (32 GB) with UDIMMs

4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-HPC/sILH. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants and Accessories

	Cooling Solution	Part No	Description
1	CSA	050950	Active cooling solution with integrated heat pipes, 12 V fan, overall height of 32.9 mm and borehole standoffs of Ø2.7 mm
		050951	Active cooling solution with integrated heat pipes, 12 V fan, overall height of 32.9 mm and threaded standoffs of M2.5 mm
2	HSP	050952	Heatspreader with integrated heat pipes, overall height of 11 mm and borehole standoffs of Ø2.7 mm
		050953	Passive cooling solution with integrated heat pipes, overall height of 11 mm and threaded standoffs of M2.5 mm
4	HPA	050954	Heat pipe adapter with borehole standoffs of Ø2.7 mm. Suitable for standard 8 mm heat pipe for optimal heat distribution
		050955	Heat pipe adapter with threaded standoffs of M2.5 mm. Suitable for standard 8 mm heat pipe for optimal heat distribution
5	Retention frame	050956	Rentention frame for the conga-HPC/sILH (required for mounting the CSA, HSP and HPA)

Caution

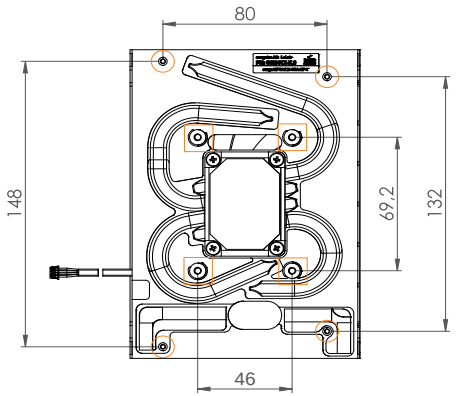
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. If your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. To ensure optimal cooling performance, they should not be stored at temperatures below -20°C. If the storage temperature drops below -10°C, the heatpipes should be pre-heated before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your local sales representative.*
3. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
4. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
5. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

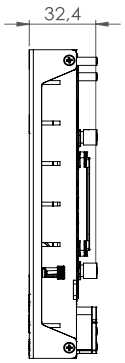
Note

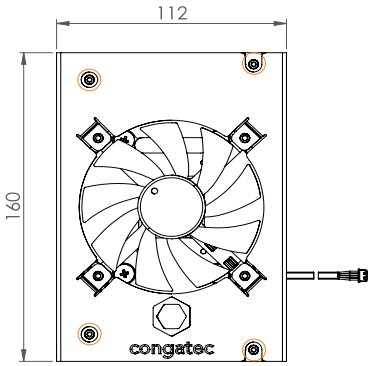
1. *We recommend a maximum torque of 0.5 Nm for M2.5 screws and 1.6 Nm for M3.5 screws.*
2. *To mount the CSA, HSP and HPA, you need the retention frame (PN: 050956). For more information, contact your sales representative*

3. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

4.1 CSA Dimensions

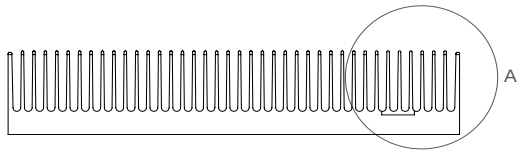






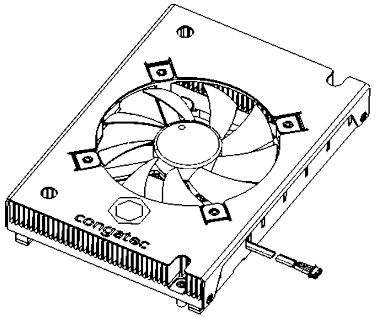
M2.5 threaded standoff
for threaded version
or
ø2.7 non-threaded standoff
for borehole version

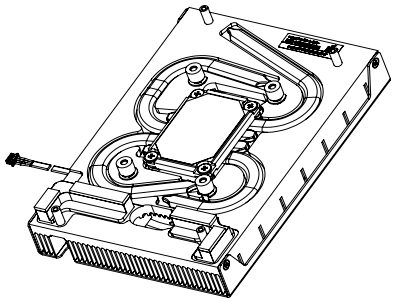
Maximum torque is 0.5 N/m

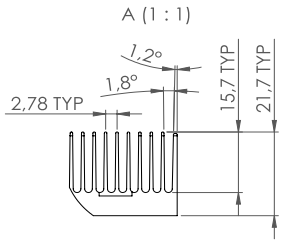


M3.5 screws for mounting
the HSP and module to the
retention frame

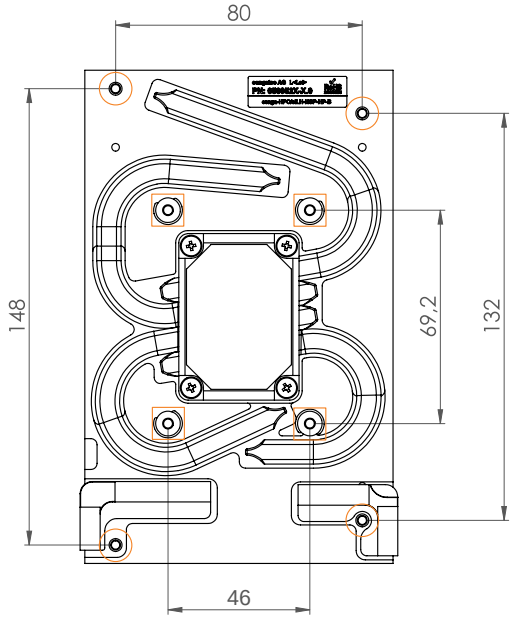
Maximum torque is 1.6 N/m

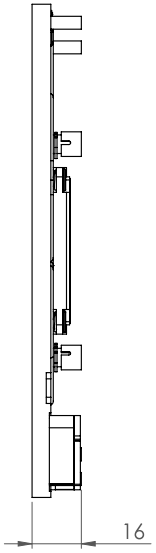


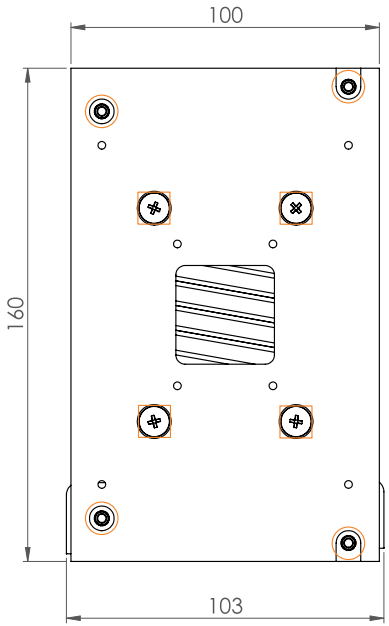




4.2 HSP Dimensions





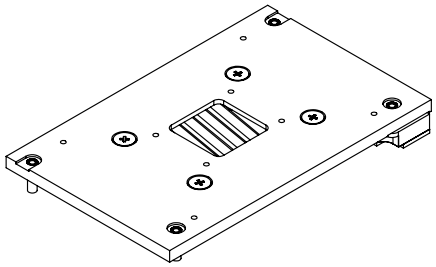


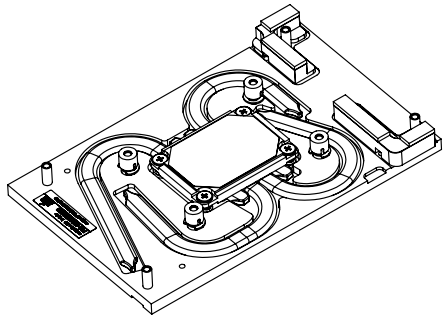
M2.5 threaded standoff
for threaded version
or
ø2.7 non-threaded standoff
for borehole version

Maximum torque is 0.5 N/m

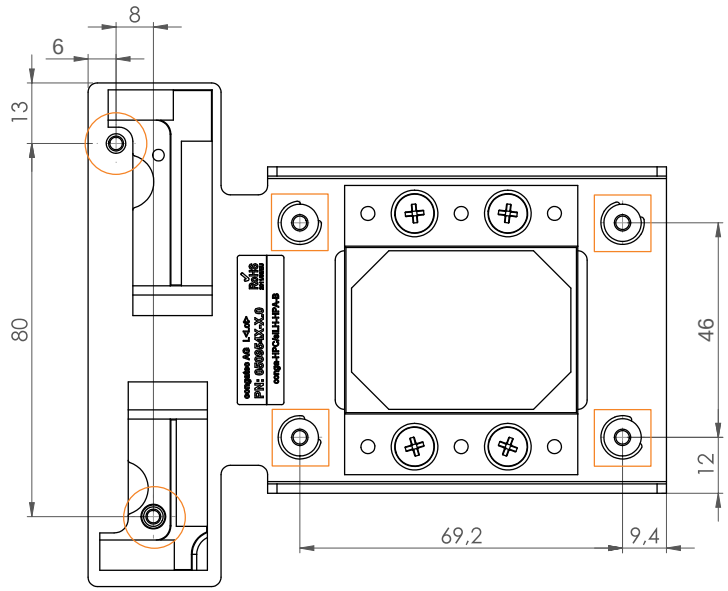
M3.5 screws for mounting the HSP and module to the retention frame

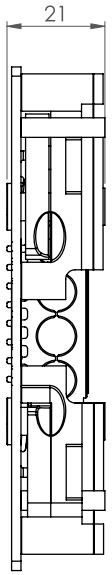
Maximum torque is 1.6 N/m

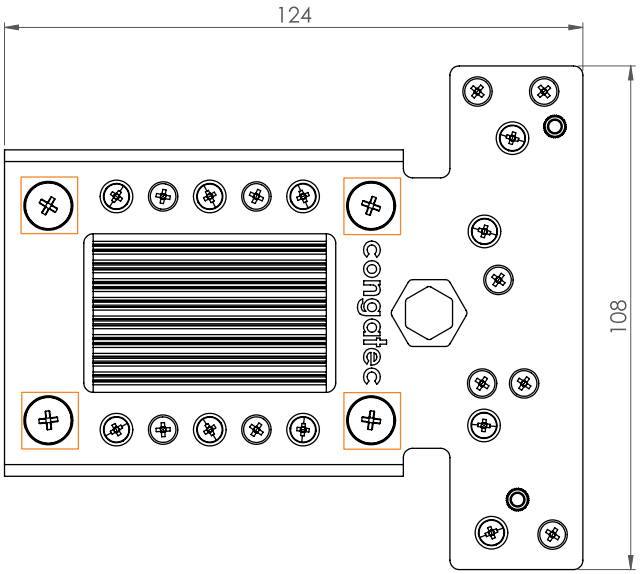


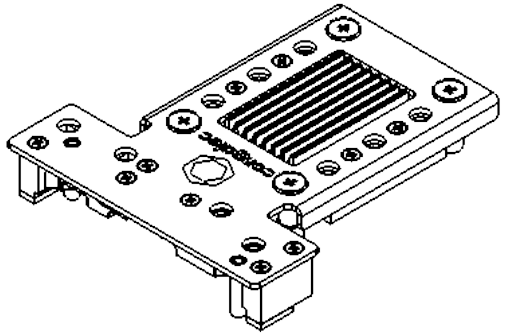


4.3 HPA Dimensions







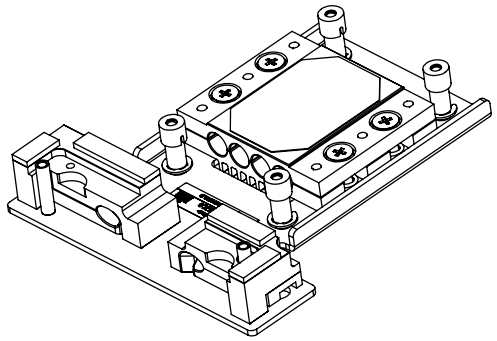


M2.5 threaded standoff
for threaded version
or
ø2.7 non-threaded standoff
for borehole version

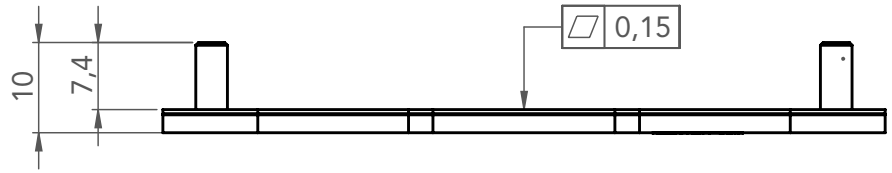
Maximum torque is 0.5 N/m

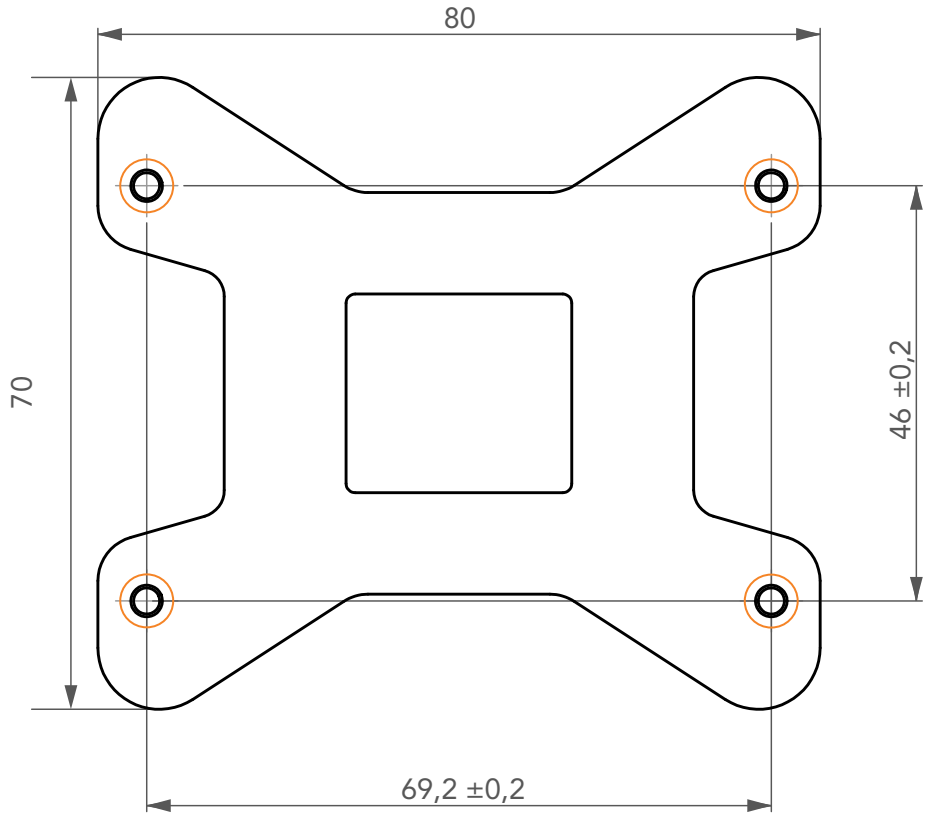
M3.5 screws for mounting the HSP and module to the retention frame

Maximum torque is 1.6 N/m



4.4 Retention Frame Dimensions





Stud for attaching
the CSA, CSP and HPA

5 Connector Rows

The conga-HPC/sILH is connected to the carrier board via two 400-pin connectors (COM-HPC server module pinout). These connectors are broken down into eight rows. The primary connector J1 consists of rows A, B, C, and D. The secondary connector J2 consists of rows E, F, G, and H. The following subsystems can be found on these connector rows.

5.1 PCI Express (PCIe)

The conga-HPC/sILH offers the following PCIe lanes:

- up to 16 PCIe Gen 3 lanes via the chipset
- up to 32 PCIe Gen 4 lanes via the SoC
- a PCIe lane for carrier BMC

5.1.1 PCIe Gen 3

The conga-HPC/sILH offers up to 16 PCIe 3.0 lanes via the chipset. The lanes support:

- PCI Express Specification 4.0a (data rate limited to 8 GT/s [1] (Gen 3))
- a 1 x8 + 2 x4 link configuration by default [2]
- a 16 x1, 8 x2, 4 x4 or 2 x8 link configurations with a custom BIOS (BOM option) [2]
- maximum of eight root ports
- lane reversal

Note

1. *Variants that support wider dynamic temperature range may limit rate to 5 GT/s.*
2. *The maximum combined HSIO bandwidth (PCIe 3.0 (PCH), USB and SATA) is 16 GB/s.*

5.1.2 PCIe Gen 4

The conga-HPC/sILH offers a 32-lane PCIe Gen 4.0 port (PEG port) via the SoC. The lanes support:

- PCI Express Specification 4.0, with up to 16 GT/s [1, 2]
- a 2 x16 link configuration by default
- a 4 x4, 2 x4 + 1 x8, 1 x8 + 2 x4, 2 x8 or 1 x16 link configuration (via the BIOS setup menu)
- maximum of eight root ports
- graphics or non-graphics PCIe devices
- lane reversal

Note

1. *Variants that support wider dynamic temperature range may limit rate to 8 GT/s.*
2. *Requires proper carrier board design considerations for PCIe Gen 4 operation. If the routing for the PCIe connectors is long or not optimized, the conga-HPC/sILH may not function as expected. For more information about Gen 4 design considerations, contact congatec technical support center.*

Note

1. *You can configure PCIe x16 port for multiple devices at narrower widths.*
2. *Linking Gen 4 lanes together with PCIe Gen 3 lanes is not allowed.*

5.1.3 BMC PCIe

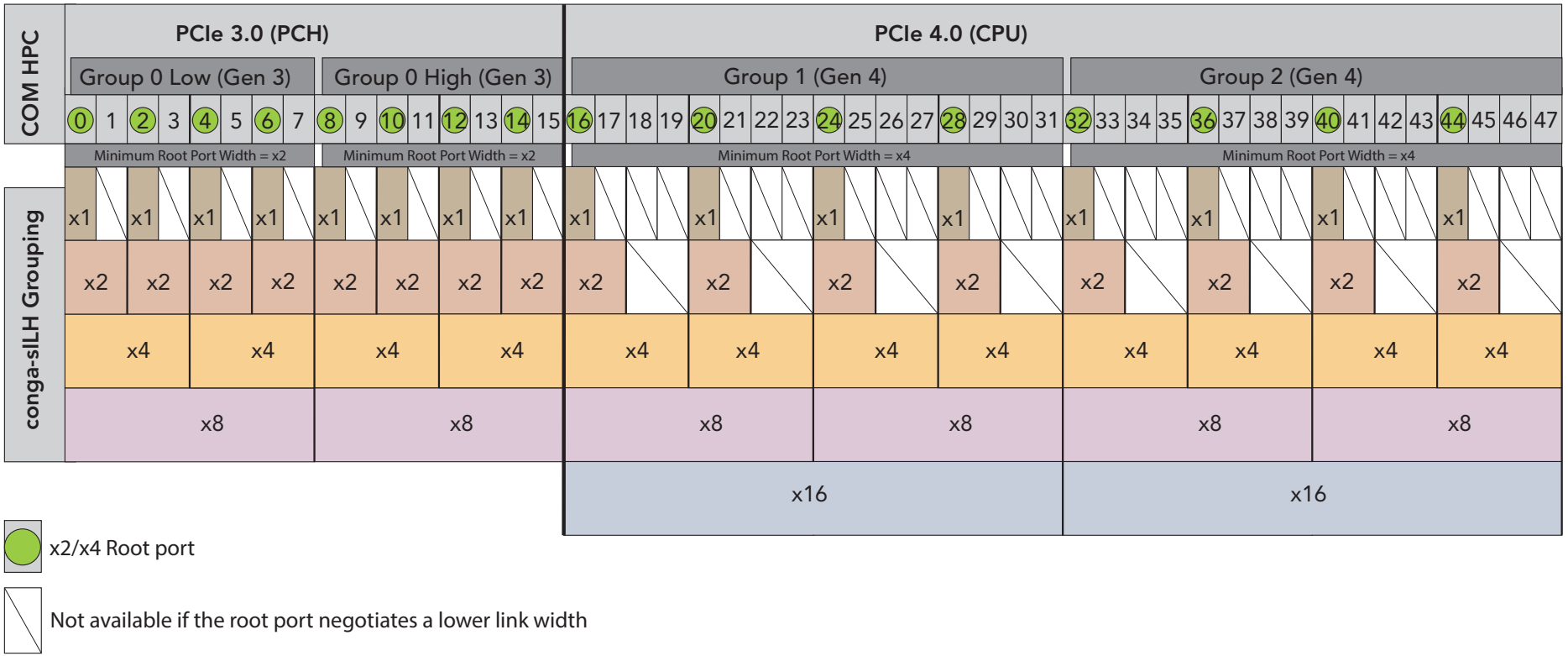
The conga-HPC/sILH offers a PCIe Gen 3 lane (PCIe_BMC_TX± and PCIe_BMC_RX±) for connecting a carrier board BMC or optionally as a PCIe x1 link.

5.1.4 PCIe Link Configuration

The possible link configurations are listed in the table below. 16 x1, 8 x2, 4 x4 or 2 x8

Table 10 PCIe Link

PCIe Lane	PCIe Generation	Link Configuration			COM-HPC Grouping	Source	Comment
		Default BIOS Setup Menu	Other BIOS Setup Menu	Custom BIOS (BOM)			
PCIe 00 - 07	Gen 3	1 x8	N.A	8 x1, 4 x2, 2 x4 or 1 x8	Group 0 Low	Chipset	
PCIe 08 - 15	Gen 3	2 x4	N.A	8 x1, 4 x2, 2 x4 or 1 x8	Group 0 High	Chipset	
PCIe 16 - 31	Gen 4	1 x16	4 x4, 2 x4 + 1 x8, 1 x8 + 2 x4, 2 x8 or 1 x16	N.A	Group 1	CPU	PEG port
PCIe 32 - 47	Gen 4	1 x16	4 x4, 2 x4 + 1 x8, 1 x8 + 2 x4, 2 x8 or 1 x16	N.A	Group 2	CPU	PEG port



5.2 NBASE-T Ethernet

The conga-HPC/sILH offers a 2.5 Gigabit Ethernet interface via an onboard Intel® i226-LM/IT controller. The interface supports:

- full-duplex operation at 10/100/1000/2500 Mbps
- half-duplex operation at 10/100 Mbps

The table below describes the LED signals of NBASE-T Ethernet interface.

Table 11 2.5 Gb Ethernet LED Description

Signals	Description
NBASET0_LINK_ACT#	Ethernet controller activity indicator
NBASET0_LINK_MAX#	Ethernet controller link indicator for 2500 Mbps (maximum link speed)
NBASET0_LINK_MID#	Ethernet controller link indicator for 1000 Mbps (lower link speed)

Note

The MAC address of the Intel i226 Ethernet controller is preprogrammed by default. The MAC address cannot be reprogrammed. If you require custom MAC address, contact your local sales representative.

5.3 Ethernet KR/KX and Related Standards

The conga-HPC/sILH Ethernet KR/KX interface supports the following features:

- 100GBASE-SR4/LR4, 100GBASE-CR4, 100GBASE-CAUI4-AOC/ACC for QSFP28 applications (default configuration) [1]
- 100GBASE-KR4, 50GBASE-KR2, 25GBASE-KR/KR1/KR-S, 10GBASE-KR, 25G-AUI-C2C, 10G-SFI-C2C for backplane applications
- 25GBASE-SR/LR, 25G-AUI-ACC/AOC, 25GBASE-CR/CR1/CR-S, 25G-AUI-C2C for SFP28 application [2]
- 10G-SFI-DA, 10GBASE-SR/LR or 10G-SFI-ACC/AOC for SFP+ application [2]
- 10GBASE-T, 1000BASE-SX/LX with Intel Coppervale X557-AT4 for SFP application

Note

1. *The Ethernet GbE PHY must be implemented on the carrier board.*
2. *For better signal integrity, we recommend to implement an external PHY or retimer on the carrier board (for example, the Intel Parkvale C827-AM/C827-IM for SFP application).*

5.3.1 Possible Ethernet Configurations (100 G SKUs)

The table below lists the KR/KX Ethernet configurations possible on the conga-HPC/sILH with standard NVM image.

Table 12 Supported Ethernet Configurations

Intel HW Config ID	Quad Config	Medium	Maximum Interface	Possible Link Modes	Rate Per Port (Quad 0/1)	100-G CPU Maximum Combinations	Comment
CFG 7.0 [1, 2, 3, 4] (default)	CEI/CEI (failover)	Parkvale C827-AM/IM	2 Ports	100GBASE-SR4/LR4	100 Gb/Failover	2x 100 G (1x 100 G as failover)	Full CEI support. **Note:** For 2 x100 G configuration, only one port is active at a time. The other port is used as a failover port. 100G requires the use use of four lanes.
				100GBASE-CR4			
				100G-CAUI4-AOC/ACC			
	CEI/Disabled		4 Ports	25GBASE-SR/LR	25 Gb/N.A	4x 25 G	
				25G-AUI-ACC/AOC (SR/LR)			
				25GBASE-CR/CR1/CR-S			
	CEI/CEI		8 Ports	10G-SFI-DA	10 Gb/10 Gb	8x 10 G	
				10GBASE-SR/LR			
				10G-SFI-ACC/AOC (SR/LR)			
	CEI/Disabled	Coppervale X557-AT4	4 Ports	10GBASE-T	10 Gb	4x 10 G	
	CEI/CEI		8 Ports			8x 10 G	
	CEI/Disabled	Marwell 88E1543	4 Ports	1000BASE-T	1 Gb	4x 1 G	
	CEI/CEI		8 Ports			8x 1 G	
CFG 7.1 [1, 2, 3, 4]	CEI/ Backplane	Parkvale C827-AM/IM and Backplane	8 Ports	10G-SFI-DA	10 Gb/10 Gb	8x 10 G	
				10GBASE-SR/LR			
				10G-SFI-ACC/AOC (SR/LR)			
				10GBASE-KR			
CFG 7.2 [1, 2, 3, 4]	CEI/4xSFP with IO Expander	Parkvale C827-AM/IM and Native SFI	8 Ports	10G-SFI-DA	10 Gb/10 Gb	8x 10 G	Combination of PHY and I/O expander. The IO expander leverages the CEI concept witohout a PHY.
				10GBASE-SR/LR			
				10G-SFI-ACC/AOC			
CFG 7.5 [1, 2, 3, 4]	4xSFP with IO Expander/ Disabled	Native SFI	4 Ports	10G-SFI-DA	10 Gb/N.A	4x 10G	With I/O expander (leveraging the CEI concept without a PHY on the carrier board).
				10GBASE-SR/LR			
				10G-SFI-ACC/AOC (SR/LR)			
	4xSFP with IO Expander/ CEI	Native SFI and Parkvale C827-AM/IM	8 Ports	10G-SFI-DA	10 Gb/10 Gb	8x 10G	
				10GBASE-SR/LR			
				10G-SFI-ACC/AOC			
CFG 7.6 [1, 2, 3, 4]	Backplane/ Disabled	Backplane	1 Port	100GBASE-KR4	100 Gb/N.A	1x 100 G	100G requires the use of four lanes. 50 G requires the use of two lanes.
	Backplane/ Backplane		2 Ports	100GBASE-KR4	100 Gb/Failover	2x 100 G (1x 100 G as failover)	
	Backplane/ Disabled		4 Ports	25GBASE-KR/KR1/KR-S	25 Gb/N.A	4x 25 G	

CFG 7.6 [1, 2, 3, 4]	Backplane/ Backplane	Backplane	6 Ports	25GBASE-KR/KR1/KR-S 10GBASE-KR	25 Gb/10 Gb	2x 25 G + 4x 10 G	100G requires the use of four lanes. 50 G requires the use of two lanes.
			8 Ports	10GBASE-KR	10 Gb/10 Gb	8x 10 G	
CFG 7.7 [1, 2, 3, 4]	4xSFP with IO Expander/ Disabled	Native SFI	4 Ports	25G-AUI-ACC/AOC (SR/LR) 25GBASE-SR/LR 25GBASE-CR/CR1/CR-S	25 Gb/N.A	4x 25 G	With I/O expander (leveraging the CEI concept without a PHY on the carrier board).
	2xSFP with IO Expander/ 4xSFP with IO Expander		6 Ports	25G-AUI-ACC/AOC (SR/LR) 25GBASE-SR/LR 25GBASE-CR/CR1/CR-S 10G-SFI-DA 10G-SFI-ACC/AOC (SR/LR) 10GBASE-SR/LR	25 Gb/10 Gb	2x 25 G + 4x 10 G	
	4xSFP with IO Expander/ 4xSFP with IO Expander		8 Port	10G-SFI-DA 10G-SFI-ACC/AOC (SR/LR) 10GBASE-SR/LR	10 Gb/10 Gb	8x 10 G	
CFG 7.9 [1, 2, 3, 4]	Backplane/ 4xSFP with IO Expander	Backplane/Native SFI	6 Ports	25GBASE-KR 10G-SFI-ACC/AOC(SR/LR) 10G-SFI-DA 10GBASE-SR/LR	25 Gb/10 Gb	2x 25 G + 4x 10 G	With I/O expander (leveraging the CEI concept without a PHY on the carrier board).
			8 Ports	10GBASE-KR 10GBASE-SR/LR 10G-SFI-ACC/AOC (SR/LR) 10G-SFI-DA	10 Gb/10 Gb	8x 10 G	
			2 Ports	50GBASE-KR2 10G-SFI-ACC/AOC (SR/LR) 10G-SFI-DA 10GBASE-SR/LR	50 Gb/10 Gb	1x 50 G + 1x 10 G	

Note

1. *Default config ID and port configuration in the BIOS is CFG 7.0 (4x 10G). To change the default config ID (CFG7.0) or the default port configuration (4x 10G), you need the deploy the corresponding LAN NVM image. For instructions on how to deploy LAN NVM and PHY NVM images, refer to congatec CTN 20230523 001 document in the restricted area of our website.*

2. *With a new BIOS flash, the config ID and port configuration is reset to this default configuration. If other config ID or port configuration is required, you need to deploy the corresponding LAN NVM image.*

3. *Highest supported speed shown per lane. A lower speed can be selected.*

4. *The 50 G LAN images can be used on 100 G SKUs to support 50 G configurations. The 100 G LAN images are however not supported on 50 G SKUs.*

5.3.2 Possible Ethernet Configurations (50 G SKUs)

The table below lists the KR/KX Ethernet configurations possible on the conga-HPC/sILH with standard NVM image.

Table 13 Supported Ethernet Configurations

Intel HW Config ID	Quad Config	Medium	Maximum Interface	Possible Link Modes	Rate Per Port (Quad 0/1)	50-G CPU Maximum Combinations	Comment
CFG 7.0 [1, 2, 3, 4] (default)	CEI/Disabled	Parkvale C827-AM/IM	2 Ports	25GBASE-SR/LR	25 Gb/N.A	2x 25 G	Full CEI support.
				25G-AUI-ACC/AOC (SR/LR)			
				25GBASE-CR/CR1/CR-S			
			4 Ports	10G-SFI-DA	10 Gb/N.A	4x 10 G	
				10GBASE-SR/LR			
				10G-SFI-ACC/AOC (SR/LR)			
	CEI/CEI		8 Ports	10G-SFI-DA	10 Gb/1 Gb	4x 10 G + 4x 1G	
				10GBASE-SR/LR			
				10G-SFI-ACC/AOC (SR/LR)			
				1000BASE-SX/LX			
CFG 7.1 [1, 2, 3, 4]	CEI/ Backplane	Parkvale C827-AM/IM and Backplane	8 Ports	10G-SFI-DA	10 Gb/2.5 Gb	4x 10 G + 4x 2.5 G	
				10GBASE-SR/LR			
				10G-SFI-ACC/AOC (SR/LR)			
				2500BASE-KX			
CFG 7.2 [1, 2, 3, 4]	CEI/4xSFP with IO Expander	Parkvale C827-AM/IM and Native SFI	8 Ports	10G-SFI-DA	10 Gb/1 Gb	4x 10 G + 4x 1G	Combination of PHY and I/O expander. The IO expander leverages the CEI concept witohout a PHY.
				10GBASE-SR/LR			
				10G-SFI-ACC/AOC (SR/LR)			
				1000BASE-SX/LX			
CFG 7.6 [1, 2, 3, 4]	Backplane/ Disabled	Backplane	1 Port	50GBASE-KR2	50 Gb/N.A	1x 50 G	50 G requires the use of two lanes.
			2 Ports	25GBASE-KR/KR1/KR-S	25 Gb/N.A	2x 25 G	
			4 Ports	10GBASE-KR	10 Gb/N.A	4x 10 G	
	Backplane/ Backplane		5 Ports	10GBASE-KR	10 Gb/10 Gb	5x 10 G	
			8 Ports	10GBASE-KR	10 Gb/2.5 Gb	4x 10 G + 4x 2.5 G	
				2500BASE-KX			
CFG 7.7 [1, 2, 3, 4]	4xSFP with IO Expander/ Disabled	Native SFI	2 Ports	25GBASE-SR/LR	25 Gb/N.A	2x 25 G	With I/O expander (leveraging the CEI concept without a PHY on the carrier board).
				25G-AUI-ACC/AOC (SR/LR)			
				25GBASE-CR/CR1/CR-S			
			4 Ports	10G-SFI-DA	10 Gb/N.A	4x 10 G	
				10G-SFI-ACC/AOC (SR/LR)			
				10GBASE-SR/LR			

CFG 7.7 [1, 2, 3, 4]	4xSFP with IO Expander/ 4xSFP with IO Expander	Native SFI	5 Ports	10G-SFI-DA 10G-SFI-ACC/AOC (SR/LR) 10GBASE-SR/LR	10 Gb/10 Gb	5x 10 G	With I/O expander (leveraging the CEI concept without a PHY on the carrier board).
			8 Ports		10 Gb/ 1 Gb	4x 10 G + 4x 1 G	
CFG 7.9 [1, 2, 3, 4]	Backplane/ 4xSFP with IO Expander	Backplane/Native SFI	8 Ports	10GBASE-KR 1000BASE-SX/LX	10 Gb/ 1 Gb	4x 10 G + 4x 1 G	With I/O expander (leveraging the CEI concept without a PHY on the carrier board).

Note

1. *Default config ID and port configuration in the BIOS is CFG 7.0 (4x 10G). To change the default config ID (CFG7.0) or the default port configuration (4x 10G), you need the deploy the corresponding LAN NVM image. For instructions on how to deploy LAN NVM and PHY NVM images, refer to congatec CTN 20230523 001 document in the restricted area of our website.*

2. *With a new BIOS flash, the config ID and port configuration is reset to this default configuration. If other config ID or port configuration is required, you need to deploy the corresponding LAN NVM image.*

3. *Lower link modes are supported.*

4. *The 50 G SKUs do not support the 100 G LAN images.*

5.3.3 IEEE 1588 and Time Synchronization

The ETH0-3_SDP pins are routed to the SoC, while the ETH4-7_SDP pins are routed to the optional DPLL. The Intel® Ice Lake SoC does not support PPS (IEEE 1588) or Synchronous Ethernet (SyncE) on the ETH0-3_SDP pins. As a result, the conga-HPC/sILH does not support PPS or SyncE unless a custom variant with a DPLL chip (assembly option) is used.

The custom variant (assembly option) enables the ETH4-7_SDP pins to support PPS or SyncE. On request, the ETH0-3_SDP pins can also be rerouted from the SoC to the DPLL to provide additional PPS or SyncE functionality.

Starting with revision A.x, the conga-HPC/sILH offers a custom variant (assembly option) to support PPS (IEE1588) without integrating a DPLL chip. In this configuration, the ETH5_SDP and ETH7_SDP pins are rerouted from the optional DPLL to the SoC. The ETH5_SDP pin supports PPS output (IEEE 1588) while the ETH7_SDP pin is configured supports PPS input.

Note

For PPS or SyncE support, you need a custom BIOS.

5.4 SATA

The conga-HPC/sILH offers two SATA interfaces (SATA 0-1) on J1 connector. The interfaces support:

- independent DMA operation
- SATA specification 3.2
- data transfer rates up to 6.0 Gb/s
- AHCI mode using memory space
- Hot-plug detect

Note

1. *The interfaces do not support legacy mode using I/O space. Therefore, you need an AHCI driver.*
2. *RAID is not supported.*
3. *The maximum combined HSIO bandwidth (PCIe 3.0 (PCH), USB and SATA) is 16 GB/s.*
4. *Variants that support wider dynamic temperature range may limit rate to 3 Gb/s*

5.5 USB

The conga-HPC/sILH offers four USB 2.0 interfaces and up to four SuperSpeed signals on J1 connector. You can combine each USB 2.0 port with corresponding USB SuperSpeed signals to create USB 3.1 Gen 1 port.

The xHCI host controller supports:

- USB 3.1 specification
- SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling
- data transfers [1] up to 5 Gbps for USB 3.1 Gen 1 port

Note

1. *The maximum combined HSIO bandwidth (PCIe 3.0 (PCH), USB and SATA) is 16 GB/s.*

5.6 UART

The conga-HPC/sILH offers two UART interfaces (UART0 and UART1) via the cBC by default. These interfaces comply with UART 16550 protocol and they support up to 115200 bps.

From the BIOS setup menu, you can select whether to route the UART0 signals from the cBC (default) or from the SoC. To route the UART1 signals from the SoC, you need a customized conga-HPC/sILH variant.

The SoC UART signals comply with UART 16550 and 16750 protocols.

5.7 GPIOs

The conga-HPC/sILH offers 12 General Purpose Input/Output signals via the congatec Board controller.

5.8 General Purpose SPI

The conga-HPC/sILH offers a general purpose SPI interface via the congatec Board Controller. The interface offers up to two chip select pins.

5.9 eSPI

The conga-HPC/sILH offers an eSPI interface for general purpose carrier board devices such as Super I/O, FPGAs, CPLDs and so on. The interface offers one chip select pin for carrier board device.

Unlike the LPC interface, the eSPI interface runs from a 1.8 V supply.

5.10 Boot SPI

The conga-HPC/sILH offers a Boot SPI interface for carrier-based SPI BIOS flash device. The congatec onboard flash device (Winbond W25Q512JVEIQ (512 Mb)) and TPM device are also connected to the Boot SPI interface.

The boot select configuration pins to select the carrier board flash device are described in section 5.11 "BIOS Flash Selection".

Note

1. *The power supply to the carrier board SPI (VCC_BOOT_SPI) is 3.3 V.*
2. *The onboard SPI flash is disabled when the carrier board SPI flash is enabled.*

5.11 BIOS Flash Selection

The boot select pins BSEL0-BSEL2 are configured to load the firmware BIOS from the conga-HPC/sILH by default. Optionally, you can configure these pins to load the boot firmware from the carrier board flash as described in the table below.

Table 14 BIOS Select Options

BSEL2	BSEL1	BSEL0	Boot Option
1	1	1	Boot from module SPI flash (default)
1	1	0	Boot from carrier board SPI flash

5.12 I²C

The conga-HPC/sILH offers two I²C interfaces (I2C0 and I2C1) via the congatec Board Controller. The I2C0 operates from a 3.3 V rail while the I2C1 operates from a 1.8 V rail.

The cBC provides a fast-mode multi-master I²C bus that has the maximum I²C bandwidth.

Table 15 Reserved I2C Address

8-bit Device Address	7-bit Device Address	Device	Description
0xA0	0x24	IPMI EEPROM	Reserved for IPMI
0x14, 0x16	0x0A, 0x0B	congatec Board Controller	Reserved for battery management
0x48	0x24	Carrier board IO expander	Reserved for carrier board IO Expander only if the conga-HPC/sILH module is attached to congatec conga-HPC/EVAL-Server carrier board
0xAE	0x57	Carrier board EEPROM	Reserved for carrier board EEPROM only if the conga-HPC/sILH module is attached to congatec conga-HPC/EVAL-Server carrier board

Note

1. *You need the congatec CGOS driver and API to access the I²C interface.*
2. *Onboard resources are not connected to the I²C bus.*

5.13 SMBus

The conga-HPC/sILH offers the System Management Bus (SMBus) via the congatec Board Controller by default. Optionally, you can route the SMBus signals from the SoC by configuring the routing in the BIOS setup menu.

Table 16 Reserved SMBus Address

8-bit Device Address	7-bit Device Address	Device	Description
0xD6, 0xD8, 0xDA	0x6B, 0x6C, 0x6D	Carrier board PCIe clock buffer	Reserved for PCIe clock buffer on the COM-HPC carrier board
0xD4	0x6A	PCIe clock generator	Reserved only if SMBus isolation is not active
0x2E	0x17	CPLD debug address	Reserved only if SMBus isolation is not active
0x14, 0x16	0x0A, 0x0B	congatec Board Controller	Reserved for battery management
0x10, 0x88	0x08, 0x44	Chipset	Reserved only if SMBus isolation is not active
0x70	0x38	DPLL	Reserved for DPLL variants only if SMBus isolation is not active

Note

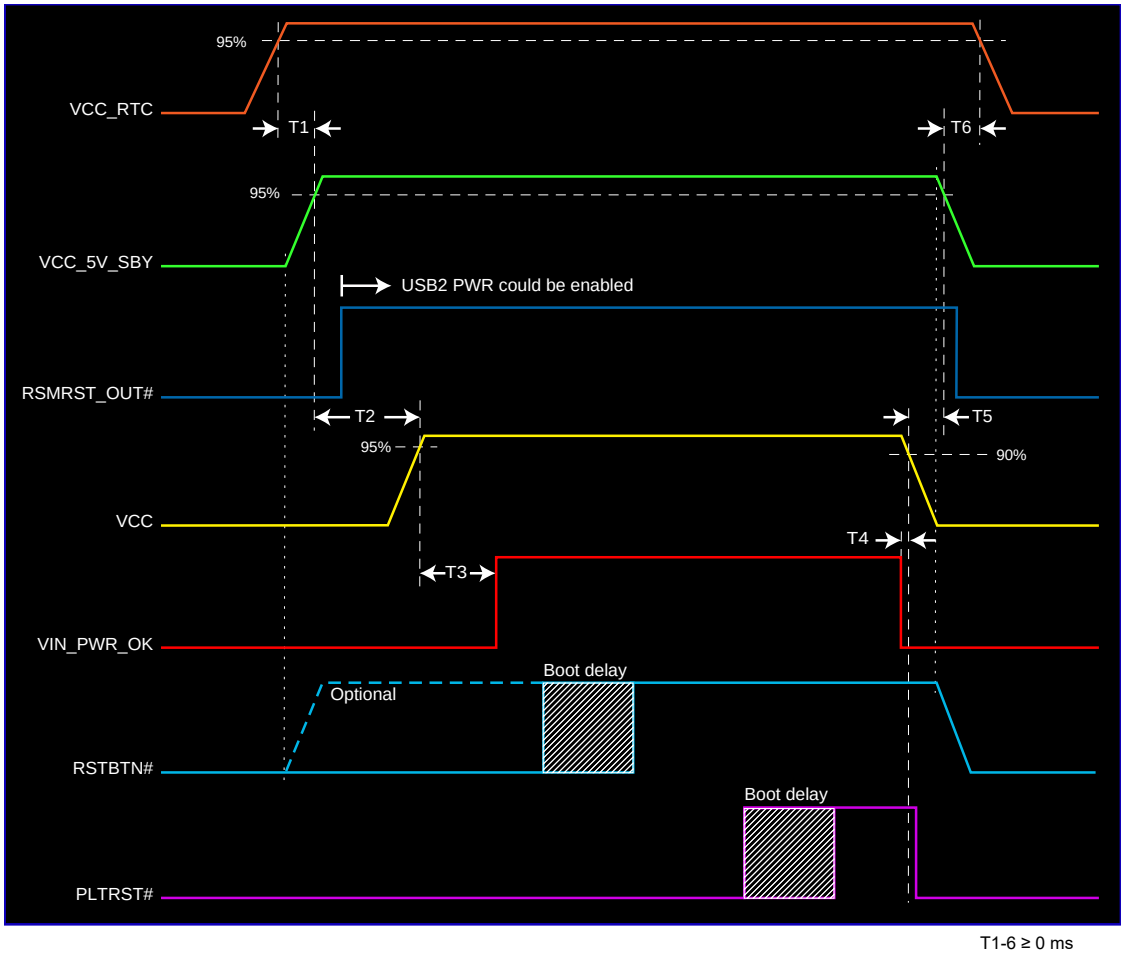
Make sure the address space of the carrier board SMBus devices does not overlap the address space of the module devices. For more information, refer to the COM-HPC Module Base Specification and Carrier Design Guide.

5.14 System Management Link (SML)

The conga-HPC/sILH offers two System Management Links (SML0 and SML1). The SML links can be used for the management of carrier board components such as ASICs or LAN controllers.

5.15 Power Control

The conga-HPC/sILH operates with 12 V input voltage range. Its power-up sequence is illustrated below:



The power control signals VIN_PWROK, RSTBTN#, SUS_S3#, and PWRBTN# are described below. For more information, refer to the COM-HPC Module Base Specification.

VIN_PWROK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. Carrier board hardware should not drive VIN_PWROK low after the input power is stable. Hold RSTBTN# low instead to keep the module in a reset condition if necessary.

Note

Due to the timing requirement of Intel Ice Lake-D SoC, VIN_PWROK signal must be active within 100 ms of SUS_S4_S5# deassertion.

SUS_S3#

The SUS_S3# signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. To accomplish this, invert the signal on the carrier board with an inverter or transistor that is supplied by standby voltage.

With SUS_S3#, the conga-HPC/sILH can control ATX-style power supplies.

Note

1. *If you do not use an ATX power supply, do not connect the conga-HPC/sILH pins SUS_S3#, VCC_5V_SBY and PWRBTN#.*

2. *The Intel SoC does not support the S3 sleep state.*

PWRBTN#

When using ATX-style power supplies, PWRBTN# is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 100 kΩ resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off.

The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

5.15.1 Inrush Current

The table below compares the inrush current and slew rate values of the conga-HPC/sILH at different voltage ramp durations.

Table 17 Inrush Current

Power Rail	Inrush Current [A]	Slew Rate [KV/s]	Voltage Ramp [ms]	Comment
VCC	57.60	15.71	0.61	Worst-case scenario
VCC_5V_SB	13.80	10.95	0.36	
VCC	30.40	9.52	1.01	Typical scenario
VCC_5V_SB	5.40	3.69	1.08	

Note

Ensure the power supply and decoupling capacitors on the carrier board are adequate for proper power sequencing.

5.15.2 Power Management

ACPI

The conga-HPC/sILH supports Advanced Configuration and Power Interface (ACPI) specification, revision 5.0a. For more information, see section 7.2 “ACPI Suspend Modes and Resume Events”.

6 Additional Features

6.1 congatec Board Controller (cBC)

The conga-HPC/sILH is equipped with Microchip MEC1706 microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. By isolating some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, the microcontroller provides higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The board controller supports the following features:

- Board information
- General Purpose Input/Output
- Watchdog
- I²C bus (see section 5.12 “I²C”)
- SMBus (see section 5.13 “SMBus”)
- UART (see section 5.6 “UART”)
- Port 80 debug information over USB power delivery pins
- Power loss control
- Fan control
- General Purpose SPI
- User EEPROM space

6.1.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.1.2 General Purpose Input/Output

The conga-HPC/sILH offers general purpose inputs and outputs for custom system design. These GPIOs are controlled by the cBC.

6.1.3 Watchdog

The conga-HPC/sILH is equipped with a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, see the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

Note

The conga-HPC/sILH module does not support watchdog NMI mode.

6.1.4 Port 80 Debug Information

The conga-HPC/sILH board controller offers BIOS Port 80h debug information over the USB Power Delivery I^2C bus (USB_PD_I2C_DAT and USB_PD_I2C_CLK). The debug information is serialized and must be deserialized on the carrer board.

For information on how to deserialize and display the debug information on carrier board 7-segment displays, refer to the COM-HPC Carrier Design Guide.

6.1.5 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The term "power loss" implies that all power sources, including the standby power are lost (G3 state). Once power loss (transition to G3) or shutdown (transition to S5) occurs, the board controller continuously monitors the standby power rail. If the standby voltage remains stable for 30 seconds, the cBC assumes the system was switched off properly. If the standby voltage is no longer detected within 30 seconds, the module considers this an AC power loss condition.

The power loss control feature has three different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to "ON".*
2. *The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.*
3. *The 30 seconds monitoring cycle applies only to the "Last State" power loss control mode.*

6.1.6 Fan Control

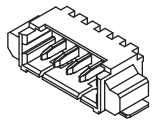
The conga-HPC/sILH offers a fan header X12 onboard. The header uses FAN_PWMOUT output signal and FAN_TACHOIN input signal for fan control, thereby improving system management. The FAN_PWMOUT signal controls the system fan with PWM (Pulse Width Modulation) while the FAN_TACHOIN signal provides the ability to monitor the system's fan RPMs (revolutions per minute).

The FAN_TACHOIN signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two-pulse per revolution fan or similar hardware solution is recommended.

Table 18 X12 Pinout Description

Pin	Signal
1	GND
2	+12 VDC
3	FAN_TACHOIN
4	FAN_PWMOUT

X12



Note

1. *A four wire fan must be used to generate the correct speed readout.*

2. *For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM-HPC Design Guide.*

Connector Type

X12: 1 x 4-pin, 1.25 pitch SMT header (Molex 53261-0471)
Possible Mating Connector: Molex 51021-0400

6.2 OEM BIOS Customization

The conga-HPC/sILH is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below.

6.2.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.2.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN11_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.2.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.2.4 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.3 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addition to the ACPI-Compliant Control Method Battery, the latest versions of the conga-HPC/sILH BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery-only solution (no charger). All three battery solutions are supported on the I^2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface, contact your local sales representative.

6.4 API Support (CGOS)

To benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux.

The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available on the congatec website.

6.5 Security Features

The conga-HPC/sILH offers offers a discrete SPI TPM 2.0 (Infineon SLB9672XU2/SLB9672VU2) by default.

6.6 Suspend to Ram/Disk

The Suspend to RAM and Suspend to Disk states are not supported on the conga-HPC/sILH.

7 conga Tech Notes

The Intel Ice Lake D-HCC SoC supports the following core features:

- Virtual and physical address space of 48 bits
- Intel 64 architecture with support for IA-32 instruction set
- Instruction Set Architecture (ISA) enhancements accelerating producer-consumer communication
- Intel Streaming SIMD Extensions 4.1 and 4.2 (SSE4.1 and SSE4.2)
- Intel Advanced Vector Extensions 512 (Intel AVX-512)
- AVX 512 Vector Byte Manipulation Instructions
- Vector Neural Network Instructions
- Intel Advanced Encryption Standard New Instructions (Intel AES-NI)
- Intel Secure Hash Algorithm New Instructions (SHA-NI)
- Intel Software Guard Extensions (Intel SGX)
- Intel Virtualization Technology (Intel VT-x) for Intel 64 and IA-32 Intel Architecture (Intel VT-x)
- Execute Disable Bit
- Package Power States (C-States)
- Intel Speed Select Technology (Intel SST)
- Intel Turbo Boost Technology
- Intel Hyper-Threading Technology (Intel HT Technology

7.1 Intel® Ice Lake D-HCC Technologies

This section describes some of the technological features the Intel Ice Lake D-HCC supports.

7.1.1 Adaptive Thermal Monitor and Catastrophic Thermal Protection

Intel® Xeon processors have a thermal monitor feature that helps to control the processor's temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu "CPU submenu".

The Adaptive Thermal Monitor controls the processor temperature using two methods:

- Adjusting the processor's operating frequency and core voltage (EIST transitions)
- Modulating (start or stop) the processor's internal clocks at a duty cycle of 25% on and 75% off

When activated, the TCC causes the processor core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated. Clock modulation is activated if frequency and voltage adjustments are insufficient. Additional hardware, software drivers, or operating system support is not required.

Note

1. *Use a properly designed thermal solution for adequate heat dissipation. This solution ensures the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum. The Intel® Xeon processor's respective datasheet can provide you with more information about this subject.*

2. *To enable THERMTRIP# to switch off the system automatically, use an ATX style power supply.*

7.1.2 Intel SpeedStep Technology (EIST)

Intel® processors on the conga-HPC/sILH run at different voltage/frequency states (performance states), referred to as Enhanced Intel® SpeedStep® Technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it is not being fully used.

The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime. The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that the power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

The 11th Generation Intel® Core™ processor family supports Intel Speed Shift, a new and energy efficient method for frequency control. This feature is also referred to as Hardware-controlled Performance States (HWP). It is a hardware implementation of the ACPI defined Collaborative Processor Performance Control (CPPC2) and is supported by newer operating systems (Win 8.1 or newer).

With this feature enabled, the processor autonomously selects performance states based on workload demand and thermal limits while also considering information provided by the Operating System (for example, the performance limits and workload history).

7.1.3 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits. Intel® Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state. The maximum frequency of Intel® Turbo Boost Technology is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost 2 Technology state depends on the workload and operating environment. Any of the following can set the upper limit of Intel® Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase by 100 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached.

For more information about Intel® Turbo Boost Technology, visit the Intel® website.

Note

1. *For real-time sensitive applications, disable EIST and Turbo Mode in the BIOS setup to ensure a more deterministic performance.*
2. *Disable Turbo mode for industrial use conditions.*
3. *Refer to section 2.5 "Power Consumption" for information about the maximum turbo frequency available for each conga-HPC/sILH variant.*

7.1.4 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel VT and is verified on all current congatec x86 hardware.

Note

congatec supports RTS Hypervisor.

7.2 ACPI Suspend Modes and Resume Events

The conga-HPC/sILH BIOS does not supports S3 and S4 states. The S5 state is however supported. The table below lists the events that wake the system from S5 state.

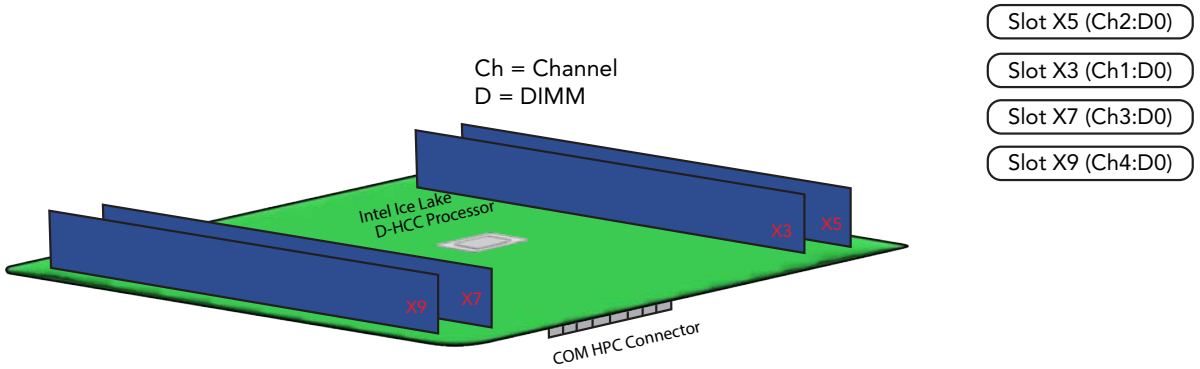
Table 19 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S5
Onboard LAN Event	Device driver must be configured for Wake On LAN support
SMB_ALERT#	Wakes unconditionally from S5
PCI Express WAKE#	Wakes unconditionally from S5
WAKE#	Wakes unconditionally from S5
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device or enable 'Resume On PME#' in the Power setup menu.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Wakes unconditionally from S5.
Watchdog Power Button Event	Wakes unconditionally from S5

7.3 Memory Population Rules

The Intel Ice Lake-D HCC SoC featured on the conga-HPC/sILH supports ECC and non-ECC DDR4 memory modules, up to 2933 MTps. The DDR4 memory modules have lower voltage requirements with higher data rate transfer speeds.

The diagram below shows the location of the memory slots on the conga-HPC/sILH.



The conga-HPC/sILH supports the following population rules:

- All DIMMs must be DDR4
- All DIMMs in a channel must have same width (x4, x8 or x16)
- The SoC does not support mixing of ECC and non-ECC memory modules
- Mixing DIMM type (UDIMM, RDIMM and so on) within and across the channels is not supported
- Mixing rank is allowed but may reduce the memory speed
- Mixing of DIMMs with different operational speeds is not validated by Intel
- Mixing memory densities (8 Gb vs 16 Gb) within a channel is allowed

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on the conga-HPC/sILH. The pinout of the module complies with COM-HPC size D server module.

The table below describes the terminology used in this section. The PU/PD column indicates if a COM-HPC module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The signal description tables do not list internal pull-ups or pull-downs implemented by the chip vendors. Only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 20 Terminology Descriptions

Term	Description
I	Input 1.8 V, 3.3 V or 5 V tolerant
O	Output 1.8 V, 3.3 V or 5 V tolerant
I/O	Bi-directional signal; 1.8 V, 3.3 V or 5 V tolerant
VSB	Voltage active in standby state
KR	Ethernet 25GBASE-KR or 10GBASE-KR compatible signal
LV_DIFF	Low voltage differential signals —may include DP, TMDS, DP_AUX, MIPI D-PHY
MDI	Media Dependent Interface, used for NBASE-T signaling
OD	Open drain output
P	Power Input/Output
PCIE	In compliance with PCI Express Base Specification
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the carrier board.
REF	Reference voltage output (minimum GND, maximum 3.3V). May be sourced from a module power plane
SATA	In compliance with SATA specification
USB	USB 2.0 compliant differential signals
USB_SS	USB Super Speed compliant signals (USB 3.0, USB 3.1, USB 3.2)
V_{OL}	Output low voltage
V_{OH}	Output high voltage

8.1 Connectors Signal Descriptions

Table 21 Primary Connector J1 Pinout

Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A01	VCC	B01	VCC	C01	VCC	D01	VCC
A02	VCC	B02	PWRBTN#	C02	RSTBTN#	D02	VCC
A03	VCC	B03	VCC	C03	VCC	D03	VCC
A04	VCC	B04	THERMTRIP#	C04	CARRIER_HOT#	D04	VCC
A05	VCC	B05	VCC	C05	VCC	D05	VCC
A06	VCC	B06	TAMPER#	C06	VIN_PWROK	D06	VCC
A07	VCC	B07	VCC	C07	VCC	D07	VCC
A08	VCC	B08	SUS_S3#	C08	SUS_S4_S5#	D08	VCC
A09	VCC	B09	VCC	C09	VCC	D09	VCC
A10	GND	B10	WD_STROBE#	C10	GND	D10	WAKE0#
A11	BATLOW#	B11	WD_OUT	C11	FAN_PWMOUT	D11	WAKE1#
A12	PLTRST#	B12	GND	C12	FAN_TACHIN	D12	GND
A13	GND	B13	USB5- [1]	C13	GND	D13	USB1-
A14	USB7- [1]	B14	USB5+ [1]	C14	USB3-	D14	USB1+
A15	USB7+ [1]	B15	GND	C15	USB3+	D15	GND
A16	GND	B16	USB4- [1]	C16	GND	D16	USB0-
A17	USB6- [1]	B17	USB4+ [1]	C17	USB2-	D17	USB0+
A18	USB6+ [1]	B18	GND	C18	USB2+	D18	GND
A19	GND	B19	RSVD [1]	C19	GND	D19	ETH0_RX-
A20	ETH4_RX-	B20	RSVD [1]	C20	ETH0_TX-	D20	ETH0_RX+
A21	ETH4_RX+	B21	RSVD [1]	C21	ETH0_TX+	D21	GND
A22	GND	B22	RSVD [1]	C22	GND	D22	ETH1_RX-
A23	ETH5_RX-	B23	RSVD [1]	C23	ETH1_TX-	D23	ETH1_RX+
A24	ETH5_RX+	B24	VCC_5V_SBY	C24	ETH1_TX+	D24	GND
A25	GND	B25	USB67_OC# [1]	C25	GND	D25	ETH2_RX-
A26	ETH6_RX-	B26	USB45_OC# [1]	C26	ETH2_TX-	D26	ETH2_RX+
A27	ETH6_RX+	B27	USB23_OC#	C27	ETH2_TX+	D27	GND
A28	GND	B28	USB01_OC#	C28	GND	D28	ETH3_RX-
A29	ETH7_RX-	B29	SML1_CLK	C29	ETH3_TX-	D29	ETH3_RX+
A30	ETH7_RX+	B30	SML1_DAT	C30	ETH3_TX+	D30	GND
A31	GND	B31	PMCALERT#	C31	GND	D31	USB3_SSTX-
A32	RSVD [1]	B32	SML0_CLK	C32	USB3_SSRX-	D32	USB3_SSTX+
A33	RSVD [1]	B33	SML0_DAT	C33	USB3_SSRX+	D33	GND
A34	GND	B34	USB_PD_ALERT#	C34	GND	D34	USB2_SSTX-
A35	ETH4_TX-	B35	USB_PD_I2C_CLK	C35	USB2_SSRX-	D35	USB2_SSTX+
A36	ETH4_TX+	B36	USB_PD_I2C_DAT	C36	USB2_SSRX+	D36	GND

A37	GND	B37	USB_RT_ENA [1]	C37	GND	D37	USB1_SSTX0-
A38	ETH5_TX-	B38	USB1_LSRX [1]	C38	USB1_SSRX0-	D38	USB1_SSTX0+
A39	ETH5_TX+	B39	USB1_LSTX [1]	C39	USB1_SSRX0+	D39	GND
A40	GND	B40	USB0_LSRX [1]	C40	GND	D40	USB1_SSTX1- [1]
A41	ETH6_TX-	B41	USB0_LSTX [1]	C41	USB1_SSRX1- [1]	D41	USB1_SSTX1+ [1]
A42	ETH6_TX+	B42	GND	C42	USB1_SSRX1+ [1]	D42	GND
A43	GND	B43	USB0_AUX- [1]	C43	GND	D43	USB0_SSTX0-
A44	ETH7_TX-	B44	USB0_AUX+ [1]	C44	USB0_SSRX0-	D44	USB0_SSTX0+
A45	ETH7_TX+	B45	RSVD [1]	C45	USB0_SSRX0+	D45	GND
A46	GND	B46	RSVD [1]	C46	GND	D46	USB0_SSTX1- [1]
A47	USB1_AUX- [1]	B47	VCC_BOOT_SPI	C47	USB0_SSRX1- [1]	D47	USB0_SSTX1+ [1]
A48	USB1_AUX+ [1]	B48	BOOT_SPI_CS#	C48	USB0_SSRX1+ [1]	D48	GND
A49	GND	B49	BSEL0	C49	GND	D49	SATA0_RX-
A50	eSPI_IO0	B50	BSEL1 [1]	C50	BOOT_SPI_IO0	D50	SATA0_RX+
A51	eSPI_IO1	B51	BSEL2 [1]	C51	BOOT_SPI_IO1	D51	GND
A52	eSPI_IO2	B52	eSPI_ALERT0#	C52	BOOT_SPI_IO2	D52	SATA0_TX-
A53	eSPI_IO3	B53	eSPI_ALERT1# [2]	C53	BOOT_SPI_IO3	D53	SATA0_TX+
A54	eSPI_CLK	B54	eSPI_CS0#	C54	BOOT_SPI_CLK	D54	GND
A55	GND	B55	eSPI_CS1#	C55	GND	D55	SATA1_RX-
A56	PCIe_CLKREQ0_LO#	B56	eSPI_RST#	C56	PCIe_REFCLK0_HI-	D56	SATA1_RX+
A57	PCIe_CLKREQ0_HI#	B57	GND	C57	PCIe_REFCLK0_HI+	D57	GND
A58	GND	B58	PCIe_BMC_RX-	C58	GND	D58	SATA1_TX-
A59	PCIe_BMC_TX-	B59	PCIe_BMC_RX+	C59	PCIe_REFCLK0_LO-	D59	SATA1_TX+
A60	PCIe_BMC_TX+	B60	GND	C60	PCIe_REFCLK0_LO+	D60	GND
A61	GND	B61	PCIe08_RX-	C61	GND	D61	PCIe00_TX-
A62	PCIe08_TX-	B62	PCIe08_RX+	C62	PCIe00_RX-	D62	PCIe00_TX+
A63	PCIe08_TX+	B63	GND	C63	PCIe00_RX+	D63	GND
A64	GND	B64	PCIe09_RX-	C64	GND	D64	PCIe01_TX-
A65	PCIe09_TX-	B65	PCIe09_RX+	C65	PCIe01_RX-	D65	PCIe01_TX+
A66	PCIe09_TX+	B66	GND	C66	PCIe01_RX+	D66	GND
A67	GND	B67	PCIe10_RX-	C67	GND	D67	PCIe02_TX-
A68	PCIe10_TX-	B68	PCIe10_RX+	C68	PCIe02_RX-	D68	PCIe02_TX+
A69	PCIe10_TX+	B69	GND	C69	PCIe02_RX+	D69	GND
A70	GND	B70	PCIe11_RX-	C70	GND	D70	PCIe03_TX-
A71	PCIe11_TX-	B71	PCIe11_RX+	C71	PCIe03_RX-	D71	PCIe03_TX+
A72	PCIe11_TX+	B72	GND	C72	PCIe03_RX+	D72	GND
A73	GND	B73	PCIe12_RX-	C73	GND	D73	PCIe04_TX-
A74	PCIe12_TX-	B74	PCIe12_RX+	C74	PCIe04_RX-	D74	PCIe04_TX+
A75	PCIe12_TX+	B75	GND	C75	PCIe04_RX+	D75	GND
A76	GND	B76	PCIe13_RX-	C76	GND	D76	PCIe05_TX-
A77	PCIe13_TX-	B77	PCIe13_RX+	C77	PCIe05_RX-	D77	PCIe05_TX+

A78	PCIe13_TX+	B78	GND	C78	PCIe05_RX+	D78	GND
A79	GND	B79	PCIe14_RX-	C79	GND	D79	PCIe06_TX-
A80	PCIe14_TX-	B80	PCIe14_RX+	C80	PCIe06_RX-	D80	PCIe06_TX+
A81	PCIe14_TX+	B81	GND	C81	PCIe06_RX+	D81	GND
A82	GND	B82	PCIe15_RX-	C82	GND	D82	PCIe07_TX-
A83	PCIe15_TX-	B83	PCIe15_RX+	C83	PCIe07_RX-	D83	PCIe07_TX+
A84	PCIe15_TX+	B84	GND	C84	PCIe07_RX+	D84	GND
A85	GND	B85	TEST#	C85	GND	D85	NBASET0_MDI0-
A86	VCC_RTC	B86	RSMRST_OUT#	C86	SMB_CLK	D86	NBASET0_MDI0+
A87	SUS_CLK	B87	UART1_TX	C87	SMB_DAT	D87	GND
A88	GPIO_00	B88	UART1_RX	C88	SMB_ALERT#	D88	NBASET0_MDI1-
A89	GPIO_01	B89	UART1_RTS#	C89	UART0_TX	D89	NBASET0_MDI1+
A90	GPIO_02	B90	UART1_CTS#	C90	UART0_RX	D90	GND
A91	GPIO_03	B91	IPMB_CLK	C91	UART0_RTS#	D91	NBASET0_MDI2-
A92	GPIO_04	B92	IPMB_DAT	C92	UART0_CTS#	D92	NBASET0_MDI2+
A93	GPIO_05	B93	GP_SPI_MOSI	C93	I2C0_CLK	D93	GND
A94	GPIO_06	B94	GP_SPI_MISO	C94	I2C0_DAT	D94	NBASET0_MDI3-
A95	GPIO_07	B95	GP_SPI_CS0#	C95	I2C0_ALERT#	D95	NBASET0_MDI3+
A96	GPIO_08	B96	GP_SPI_CS1#	C96	I2C1_CLK	D96	GND
A97	GPIO_09	B97	GP_SPI_CS2# [1]	C97	I2C1_DAT	D97	NBASET0_LINK_MAX#
A98	GPIO_10	B98	GP_SPI_CS3# [1]	C98	NBASET0_SDP	D98	NBASET0_LINK_MID#
A99	GPIO_11	B99	GP_SPI_CLK	C99	NBASET0_CTREF [1]	D99	NBASET0_LINK_ACT#
A100	TYPE0	B100	GP_SPI_ALERT#	C100	TYPE1	D100	TYPE2 [1]

Note

1. *Not connected*

2. *Not supported*

Table 22 Connector J2 Pinout

Pin	Row E	Pin	Row F	Pin	Row G	Pin	Row H
E1	RAPID_SHUTDOWN [2]	F1	ETH2_SDP [2, 3]	G1	VCC_5V_SBY	H1	RSVD
E2	GND	F2	ETH3_SDP [2, 3]	G2	FUSA_STATUS0 [1]	H2	RSVD
E3	RSVD	F3	ETH4_SDP [2]	G3	FUSA_STATUS1 [1]	H3	RSVD
E4	RSVD	F4	ETH5_SDP [2]	G4	FUSA_ALERT# [1]	H4	RSVD
E5	GND	F5	ETH6_SDP [2]	G5	FUSA_SPI_CS# [2]	H5	RSVD
E6	RSVD	F6	ETH7_SDP [2]	G6	FUSA_SPI_CLK [2]	H6	RSVD
E7	RSVD	F7	ETH4-7_I2C_CLK	G7	FUSA_SPI_MISO [1]	H7	RSVD
E8	GND	F8	ETH4-7_I2C_DAT	G8	FUSA_SPI_MOSI [2]	H8	RSVD
E9	RSVD	F9	ETH4-7_INT#	G9	FUSA_SPI_ALERT [1]	H9	RSVD
E10	RSVD	F10	ETH4-7_MDIO_CLK	G10	FUSA_VOLTAGE_ERR# [1]	H10	RSVD
E11	GND	F11	ETH4-7_MDIO_DAT	G11	PROCHOT#	H11	RSVD
E12	RSVD	F12	ETH4-7_PHY_INT# [2]	G12	CATERR#	H12	RSVD
E13	RSVD	F13	ETH4-7_PHY_RST#	G13	RSVD	H13	RSVD
E14	GND	F14	ETH4-7_PRSNT#	G14	GND	H14	RSVD
E15	RSVD	F15	RSVD	G15	RSVD	H15	RSVD
E16	RSVD	F16	RSVD	G16	RSVD	H16	RSVD
E17	GND	F17	RSVD	G17	RSVD	H17	RSVD
E18	RSVD	F18	RSVD	G18	RSVD	H18	RSVD
E19	RSVD	F19	GND	G19	RSVD [1]	H19	GND
E20	GND	F20	PCIe32_RX-	G20	GND	H20	PCIe40_TX-
E21	PCIe32_TX-	F21	PCIe32_RX+	G21	PCIe40_RX-	H21	PCIe40_TX+
E22	PCIe32_TX+	F22	GND	G22	PCIe40_RX+	H22	GND
E23	GND	F23	PCIe33_RX-	G23	GND	H23	PCIe41_TX-
E24	PCIe33_TX-	F24	PCIe33_RX+	G24	PCIe41_RX-	H24	PCIe41_TX+
E25	PCIe33_TX+	F25	GND	G25	PCIe41_RX+	H25	GND
E26	GND	F26	PCIe34_RX-	G26	GND	H26	PCIe42_TX-
E27	PCIe34_TX-	F27	PCIe34_RX+	G27	PCIe42_RX-	H27	PCIe42_TX+
E28	PCIe34_TX+	F28	GND	G28	PCIe42_RX+	H28	GND
E29	GND	F29	PCIe35_RX-	G29	GND	H29	PCIe43_TX-
E30	PCIe35_TX-	F30	PCIe35_RX+	G30	PCIe43_RX-	H30	PCIe43_TX+
E31	PCIe35_TX+	F31	GND	G31	PCIe43_RX+	H31	GND
E32	GND	F32	PCIe36_RX-	G32	GND	H32	PCIe44_TX-
E33	PCIe36_TX-	F33	PCIe36_RX+	G33	PCIe44_RX-	H33	PCIe44_TX+
E34	PCIe36_TX+	F34	GND	G34	PCIe44_RX+	H34	GND
E35	GND	F35	PCIe37_RX-	G35	GND	H35	PCIe45_TX-
E36	PCIe37_TX-	F36	PCIe37_RX+	G36	PCIe45_RX-	H36	PCIe45_TX+
E37	PCIe37_TX+	F37	GND	G37	PCIe45_RX+ [1]	H37	GND
E38	GND	F38	PCIe38_RX-	G38	GND	H38	PCIe46_TX-

E39	PCIe38_TX-	F39	PCIe38_RX+	G39	PCIe46_RX-	H39	PCIe46_TX+
E40	PCIe38_TX+	F40	GND	G40	PCIe46_RX+	H40	GND
E41	GND	F41	PCIe39_RX-	G41	GND	H41	PCIe47_TX-
E42	PCIe39_TX-	F42	PCIe39_RX+	G42	PCIe47_RX-	H42	PCIe47_TX+
E43	PCIe39_TX+	F43	GND	G43	PCIe47_RX+	H43	GND
E44	GND	F44	PCIe16_RX-	G44	GND	H44	PCIe24_TX-
E45	PCIe16_TX-	F45	PCIe16_RX+	G45	PCIe24_RX-	H45	PCIe24_TX+
E46	PCIe16_TX+	F46	GND	G46	PCIe24_RX+	H46	GND
E47	GND	F47	PCIe17_RX-	G47	GND	H47	PCIe25_TX-
E48	PCIe17_TX-	F48	PCIe17_RX+	G48	PCIe25_RX-	H48	PCIe25_TX+
E49	PCIe17_TX+	F49	GND	G49	PCIe25_RX+	H49	GND
E50	GND	F50	PCIe18_RX-	G50	GND	H50	PCIe26_TX-
E51	PCIe18_TX-	F51	PCIe18_RX+	G51	PCIe26_RX-	H51	PCIe26_TX+
E52	PCIe18_TX+	F52	GND	G52	PCIe26_RX+	H52	GND
E53	GND	F53	PCIe19_RX-	G53	GND	H53	PCIe27_TX-
E54	PCIe19_TX-	F54	PCIe19_RX+	G54	PCIe27_RX-	H54	PCIe27_TX+
E55	PCIe19_TX+	F55	GND	G55	PCIe27_RX+	H55	GND
E56	GND	F56	PCIe20_RX-	G56	GND	H56	PCIe28_TX-
E57	PCIe20_TX-	F57	PCIe20_RX+	G57	PCIe28_RX-	H57	PCIe28_TX+
E58	PCIe20_TX+	F58	GND	G58	PCIe28_RX+	H58	GND
E59	GND	F59	PCIe21_RX-	G59	GND	H59	PCIe29_TX-
E60	PCIe21_TX-	F60	PCIe21_RX+	G60	PCIe29_RX-	H60	PCIe29_TX+
E61	PCIe21_TX+	F61	GND	G61	PCIe29_RX+	H61	GND
E62	GND	F62	PCIe22_RX-	G62	GND	H62	PCIe30_TX-
E63	PCIe22_TX-	F63	PCIe22_RX+	G63	PCIe30_RX-	H63	PCIe30_TX+
E64	PCIe22_TX+	F64	GND	G64	PCIe30_RX+	H64	GND
E65	GND	F65	PCIe23_RX-	G65	GND	H65	PCIe31_TX-
E66	PCIe23_TX-	F66	PCIe23_RX+	G66	PCIe31_RX-	H66	PCIe31_TX+
E67	PCIe23_TX+	F67	GND	G67	PCIe31_RX+	H67	GND
E68	GND	F68	PCIe48_RX- [1]	G68	GND	H68	PCIe56_TX- [1]
E69	PCIe48_TX- [1]	F69	PCIe48_RX+ [1]	G69	PCIe56_RX- [1]	H69	PCIe56_TX+ [1]
E70	PCIe48_TX+ [1]	F70	GND	G70	PCIe56_RX+ [1]	H70	GND
E71	GND	F71	PCIe49_RX- [1]	G71	GND	H71	PCIe57_TX- [1]
E72	PCIe49_TX- [1]	F72	PCIe49_RX+ [1]	G72	PCIe57_RX- [1]	H72	PCIe57_TX+ [1]
E73	PCIe49_TX+ [1]	F73	GND	G73	PCIe57_RX+ [1]	H73	GND
E74	GND	F74	PCIe50_RX- [1]	G74	GND	H74	PCIe58_TX- [1]
E75	PCIe50_TX- [1]	F75	PCIe50_RX+ [1]	G75	PCIe58_RX- [1]	H75	PCIe58_TX+ [1]
E76	PCIe50_TX+ [1]	F76	GND	G76	PCIe58_RX+ [1]	H76	GND
E77	GND	F77	PCIe51_RX- [1]	G77	GND	H77	PCIe59_TX- [1]
E78	PCIe51_TX- [1]	F78	PCIe51_RX+ [1]	G78	PCIe59_RX- [1]	H78	PCIe59_TX+ [1]
E79	PCIe51_TX+ [1]	F79	GND	G79	PCIe59_RX+ [1]	H79	GND

E80	GND	F80	PCIe52_RX- [1]	G80	GND	H80	PCIe60_TX- [1]
E81	PCIe52_TX- [1]	F81	PCIe52_RX+ [1]	G81	PCIe60_RX- [1]	H81	PCIe60_TX+ [1]
E82	PCIe52_TX+ [1]	F82	GND	G82	PCIe60_RX+ [1]	H82	GND
E83	GND	F83	PCIe53_RX- [1]	G83	GND	H83	PCIe61_TX- [1]
E84	PCIe53_TX- [1]	F84	PCIe53_RX+ [1]	G84	PCIe61_RX- [1]	H84	PCIe61_TX+ [1]
E85	PCIe53_TX+ [1]	F85	GND	G85	PCIe61_RX+ [1]	H85	GND
E86	GND	F86	PCIe54_RX- [1]	G86	GND	H86	PCIe62_TX- [1]
E87	PCIe54_TX- [1]	F87	PCIe54_RX+ [1]	G87	PCIe62_RX- [1]	H87	PCIe62_TX+ [1]
E88	PCIe54_TX+ [1]	F88	GND	G88	PCIe62_RX+ [1]	H88	GND
E89	GND	F89	PCIe55_RX- [1]	G89	GND	H89	PCIe63_TX- [1]
E90	PCIe55_TX- [1]	F90	PCIe55_RX+ [1]	G90	PCIe63_RX- [1]	H90	PCIe63_TX+ [1]
E91	PCIe55_TX+ [1]	F91	GND	G91	PCIe63_RX+ [1]	H91	GND
E92	GND	F92	PCIe_REFCLK2-	G92	GND	H92	PCIe_REFCLKIN0- [1]
E93	PCIe_REFCLK1-	F93	PCIe_REFCLK2+	G93	PCIe_REFCLK3-	H93	PCIe_REFCLKIN0+ [1]
E94	PCIe_REFCLK1+	F94	GND	G94	PCIe_REFCLK3+	H94	GND
E95	GND	F95	PCIe_CLKREQ3#	G95	GND	H95	PCIe_REFCLKIN1- [1]
E96	PCIe_CLKREQ1#	F96	ETH0-3_PRSNT#	G96	ETH0-3_I2C_CLK	H96	PCIe_REFCLKIN1+ [1]
E97	PCIe_CLKREQ2#	F97	ETH0-3_PHY_RST#	G97	ETH0-3_I2C_DAT	H97	GND
E98	PCIe_CLKREQ_OUT0# [1]	F98 [2]	ETH0_SDP [2, 3]	G98	ETH0-3_PHY_INT# [2]	H98	ETH0-3_MDIO_CLK [3]
E99	PCIe_CLKREQ_OUT1# [1]	F99 [2]	ETH1_SDP [2, 3]	G99	ETH0-3_INT#	H99	ETH0-3_MDIO_DAT [3]
E100	PCIe_PERST_IN0# [1]	F100	PCIe_PERST_IN1# [1]	G100	PCIe_WAKE_OUT0# [1]	H100	PCIe_WAKE_OUT1# [1]

Note

1. *Not connected*
2. *Not supported*
3. *Boot strap signals*

Table 23 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIe00_TX+ PCIe00_TX-	D62 D61	PCI Express Transmit Output Differential Pairs 0	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIe00_RX+ PCIe00_RX-	C63 C62	PCI Express Receive Input Differential Pairs 0	I PCIE		
PCIe01_TX+ PCIe01_TX-	D65 D64	PCI Express Transmit Output Differential Pairs 1	O PCIE		
PCIe01_RX+ PCIe01_RX-	C66 C65	PCI Express Receive Input Differential Pairs 1	I PCIE		
PCIe02_TX+ PCIe02_TX-	D68 D67	PCI Express Transmit Output Differential Pairs 2	O PCIE		
PCIe02_RX+ PCIe02_RX-	C69 C68	PCI Express Receive Input Differential Pairs 2	I PCIE		
PCIe03_TX+ PCIe03_TX-	D71 D70	PCI Express Transmit Output Differential Pairs 3	O PCIE		
PCIe03_RX+ PCIe03_RX-	C72 C71	PCI Express Receive Input Differential Pairs 3	I PCIE		
PCIe04_TX+ PCIe04_TX-	D74 D73	PCI Express Transmit Output Differential Pairs 4	O PCIE		
PCIe04_RX+ PCIe04_RX-	C75 C74	PCI Express Receive Input Differential Pairs 4	I PCIE		
PCIe05_TX+ PCIe05_TX-	D77 D76	PCI Express Transmit Output Differential Pairs 5	O PCIE		
PCIe05_RX+ PCIe05_RX-	C78 C77	PCI Express Receive Input Differential Pairs 5	I PCIE		
PCIe06_TX+ PCIe06_TX-	D80 D79	PCI Express Transmit Output Differential Pairs 6	O PCIE		
PCIe06_RX+ PCIe06_RX-	C81 C80	PCI Express Receive Input Differential Pairs 6	I PCIE		
PCIe07_TX+ PCIe07_TX-	D83 D82	PCI Express Transmit Output Differential Pairs 7	O PCIE		
PCIe07_RX+ PCIe07_RX-	C84 C83	PCI Express Receive Input Differential Pairs 7	I PCIE		
PCIe08_TX+ PCIe08_TX-	A63 A62	PCI Express Transmit Output Differential Pairs 8	O PCIE		
PCIe08_RX+ PCIe08_RX-	B62 B61	PCI Express Receive Input Differential Pairs 8	I PCIE		
PCIe09_TX+ PCIe09_TX-	A66 A65	PCI Express Transmit Output Differential Pairs 9	O PCIE		
PCIe09_RX+ PCIe09_RX-	B65 B64	PCI Express Receive Input Differential Pairs 9	I PCIE		

PCIe10_TX+ PCIe10_TX-	A69 A68	PCI Express Transmit Output Differential Pairs 10	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE10_RX+ PCIE10_RX-	B68 B67	PCI Express Receive Input Differential Pairs 10	I PCIE		
PCIE11_TX+ PCIE11_TX-	A72 A71	PCI Express Transmit Output Differential Pairs 11	O PCIE		
PCIE11_RX+ PCIE11_RX-	B71 B70	PCI Express Receive Input Differential Pairs 11	I PCIE		
PCIE12_TX+ PCIE12_TX-	B75 A74	PCI Express Transmit Output Differential Pairs 12	O PCIE		
PCIE12_RX+ PCIE12_RX-	B74 B73	PCI Express Receive Input Differential Pairs 12	I PCIE		
PCIE13_TX+ PCIE13_TX-	A78 A77	PCI Express Transmit Output Differential Pairs 13	O PCIE		
PCIE13_RX+ PCIE13_RX-	B77 B76	PCI Express Receive Input Differential Pairs 13	I PCIE		
PCIE14_TX+ PCIE14_TX-	A81 A80	PCI Express Transmit Output Differential Pairs 14	O PCIE		
PCIE14_RX+ PCIE14_RX-	B80 B79	PCI Express Receive Input Differential Pairs 14	I PCIE		
PCIE15_TX+ PCIE15_TX-	A84 A83	PCI Express Transmit Output Differential Pairs 15	O PCIE		
PCIE15_RX+ PCIE15_RX-	B83 B82	PCI Express Receive Input Differential Pairs 15	I PCIE		
PCIE16_TX+ PCIE16_TX-	E46 E45	PCI Express Transmit Output Differential Pairs 16	O PCIE		Supports PCI Express Base Specification, Revision 4.0
PCIE16_RX+ PCIE16_RX-	F45 F44	PCI Express Receive Input Differential Pairs 16	I PCIE		
PCIE17_TX+ PCIE17_TX-	E49 E48	PCI Express Transmit Output Differential Pairs 17	O PCIE		
PCIE17_RX+ PCIE17_RX-	F48 F47	PCI Express Receive Input Differential Pairs 17	I PCIE		
PCIE18_TX+ PCIE18_TX-	E52 E51	PCI Express Transmit Output Differential Pairs 18	O PCIE		
PCIE18_RX+ PCIE18_RX-	F51 F50	PCI Express Receive Input Differential Pairs 18	I PCIE		
PCIE19_TX+ PCIE19_TX-	E55 E54	PCI Express Transmit Output Differential Pairs 19	O PCIE		
PCIE19_RX+ PCIE19_RX-	F54 F53	PCI Express Receive Input Differential Pairs 19	I PCIE		
PCIE20_TX+ PCIE20_TX-	E58 E57	PCI Express Transmit Output Differential Pairs 20	O PCIE		
PCIE20_RX+ PCIE20_RX-	F57 F56	PCI Express Receive Input Differential Pairs 20	I PCIE		

PCIE21_TX+ PCIE21_TX-	E61 E60	PCI Express Transmit Output Differential Pairs 21	O PCIE		Supports PCI Express Base Specification, Revision 4.0
PCIE21_RX+ PCIE21_RX-	F60 F59	PCI Express Receive Input Differential Pairs 21	I PCIE		
PCIE22_TX+ PCIE22_TX-	E64 E63	PCI Express Transmit Output Differential Pairs 22	O PCIE		
PCIE22_RX+ PCIE22_RX-	F63 F62	PCI Express Receive Input Differential Pairs 22	I PCIE		
PCIE23_TX+ PCIE23_TX-	E67 E66	PCI Express Transmit Output Differential Pairs 23	O PCIE		
PCIE23_RX+ PCIE23_RX-	F66 F65	PCI Express Receive Input Differential Pairs 23	I PCIE		
PCIE24_TX+ PCIE24_TX-	H45 H44	PCI Express Transmit Output Differential Pairs 24	O PCIE		
PCIE24_RX+ PCIE24_RX-	G46 G45	PCI Express Receive Input Differential Pairs 24	I PCIE		
PCIE25_TX+ PCIE25_TX-	H48 H47	PCI Express Transmit Output Differential Pairs 25	O PCIE		
PCIE25_RX+ PCIE25_RX-	G46 G45	PCI Express Receive Input Differential Pairs 25	I PCIE		
PCIE26_TX+ PCIE26_TX-	H51 H50	PCI Express Transmit Output Differential Pairs 26	O PCIE		
PCIE26_RX+ PCIE26_RX-	G52 G51	PCI Express Receive Input Differential Pairs 26	I PCIE		
PCIE27_TX+ PCIE27_TX-	H54 H53	PCI Express Transmit Output Differential Pairs 27	O PCIE		
PCIE27_RX+ PCIE27_RX-	G55 G54	PCI Express Receive Input Differential Pairs 27	I PCIE		
PCIE28_TX+ PCIE28_TX-	H57 H56	PCI Express Transmit Output Differential Pairs 28	O PCIE		
PCIE28_RX+ PCIE28_RX-	G58 G57	PCI Express Receive Input Differential Pairs 28	I PCIE		
PCIE29_TX+ PCIE29_TX-	H60 H59	PCI Express Transmit Output Differential Pairs 29	O PCIE		
PCIE29_RX+ PCIE29_RX-	G61 G60	PCI Express Receive Input Differential Pairs 29	I PCIE		
PCIE30_TX+ PCIE30_TX-	H63 H62	PCI Express Transmit Output Differential Pairs 30	O PCIE		
PCIE30_RX+ PCIE30_RX-	G64 G63	PCI Express Receive Input Differential Pairs 30	I PCIE		
PCIE31_TX+ PCIE31_TX-	H66 H65	PCI Express Transmit Output Differential Pairs 31	O PCIE		
PCIE31_RX+ PCIE31_RX-	G67 G66	PCI Express Receive Input Differential Pairs 31	I PCIE		

PCIE32_TX+ PCIE32_TX-	E22 E21	PCI Express Transmit Output Differential Pairs 32	O PCIE		Supports PCI Express Base Specification, Revision 4.0
PCIE32_RX+ PCIE32_RX-	F21 F20	PCI Express Receive Input Differential Pairs 32	I PCIE		
PCIE33_TX+ PCIE33_TX-	E25 E24	PCI Express Transmit Output Differential Pairs 33	O PCIE		
PCIE33_RX+ PCIE33_RX-	F24 F23	PCI Express Receive Input Differential Pairs 33	I PCIE		
PCIE34_TX+ PCIE34_TX-	E28 E27	PCI Express Transmit Output Differential Pairs 34	O PCIE		
PCIE34_RX+ PCIE34_RX-	F27 F26	PCI Express Receive Input Differential Pairs 34	I PCIE		
PCIE35_TX+ PCIE35_TX-	E31 E30	PCI Express Transmit Output Differential Pairs 35	O PCIE		
PCIE35_RX+ PCIE35_RX-	F30 F29	PCI Express Receive Input Differential Pairs 35	I PCIE		
PCIE36_TX+ PCIE36_TX-	E34 E33	PCI Express Transmit Output Differential Pairs 36	O PCIE		
PCIE36_RX+ PCIE36_RX-	F33 F32	PCI Express Receive Input Differential Pairs 36	I PCIE		
PCIE37_TX+ PCIE37_TX-	E37 E36	PCI Express Transmit Output Differential Pairs 37	O PCIE		
PCIE37_RX+ PCIE37_RX-	F36 F35	PCI Express Receive Input Differential Pairs 37	I PCIE		
PCIE38_TX+ PCIE38_TX-	E40 E39	PCI Express Transmit Output Differential Pairs 38	O PCIE		
PCIE38_RX+ PCIE38_RX-	F39 F38	PCI Express Receive Input Differential Pairs 38	I PCIE		
PCIE39_TX+ PCIE39_TX-	E43 E42	PCI Express Transmit Output Differential Pairs 39	O PCIE		
PCIE39_RX+ PCIE39_RX-	F42 F41	PCI Express Receive Input Differential Pairs 39	I PCIE		
PCIE40_TX+ PCIE40_TX-	H21 H20	PCI Express Transmit Output Differential Pairs 40	O PCIE		
PCIE40_RX+ PCIE40_RX-	G22 G21	PCI Express Receive Input Differential Pairs 40	I PCIE		
PCIE41_TX+ PCIE41_TX-	H24 H23	PCI Express Transmit Output Differential Pairs 41	O PCIE		
PCIE41_RX+ PCIE41_RX-	G25 G24	PCI Express Receive Input Differential Pairs 41	I PCIE		
PCIE42_TX+ PCIE42_TX-	H27 H26	PCI Express Transmit Output Differential Pairs 42	O PCIE		
PCIE42_RX+ PCIE42_RX-	G28 G27	PCI Express Receive Input Differential Pairs 42	I PCIE		

PCIE43_TX+ PCIE43_TX-	H30 H29	PCI Express Transmit Output Differential Pairs 43	O PCIE		Supports PCI Express Base Specification, Revision 4.0
PCIE43_RX+ PCIE43_RX-	G31 G30	PCI Express Receive Input Differential Pairs 43	I PCIE		
PCIE44_TX+ PCIE44_TX-	H33 H32	PCI Express Transmit Output Differential Pairs 44	O PCIE		
PCIE44_RX+ PCIE44_RX-	G34 G33	PCI Express Receive Input Differential Pairs 44	I PCIE		
PCIE45_TX+ PCIE45_TX-	H36 H35	PCI Express Transmit Output Differential Pairs 45	O PCIE		
PCIE45_RX+ PCIE45_RX-	G37 G36	PCI Express Receive Input Differential Pairs 45	I PCIE		
PCIE46_TX+ PCIE46_TX-	H39 H38	PCI Express Transmit Output Differential Pairs 46	O PCIE		
PCIE46_RX+ PCIE46_RX-	G40 G39	PCI Express Receive Input Differential Pairs 46	I PCIE		
PCIE47_TX+ PCIE47_TX-	H42 H41	PCI Express Transmit Output Differential Pairs 47	O PCIE		
PCIE47_RX+ PCIE47_RX-	G43 G42	PCI Express Receive Input Differential Pairs 47	I PCIE		
PCIE48_TX+ PCIE48_TX-	E70 E69	PCI Express Transmit Output Differential Pairs 48	O PCIE		Not connected
PCIE48_RX+ PCIE48_RX-	F69 F68	PCI Express Receive Input Differential Pairs 48	I PCIE		
PCIE49_TX+ PCIE49_TX-	E73 E72	PCI Express Transmit Output Differential Pairs 49	O PCIE		
PCIE49_RX+ PCIE49_RX-	F72 F71	PCI Express Receive Input Differential Pairs 49	I PCIE		
PCIE50_TX+ PCIE50_TX-	E76 E75	PCI Express Transmit Output Differential Pairs 50	O PCIE		
PCIE50_RX+ PCIE50_RX-	F75 F74	PCI Express Receive Input Differential Pairs 50	I PCIE		
PCIE51_TX+ PCIE51_TX-	E79 E78	PCI Express Transmit Output Differential Pairs 51	O PCIE		
PCIE51_RX+ PCIE51_RX-	F78 F77	PCI Express Receive Input Differential Pairs 51	I PCIE		
PCIE52_TX+ PCIE52_TX-	E82 E81	PCI Express Transmit Output Differential Pairs 52	O PCIE		
PCIE52_RX+ PCIE52_RX-	F81 F80	PCI Express Receive Input Differential Pairs 52	I PCIE		

PCIE53_TX+ PCIE53_TX-	E85 E84	PCI Express Transmit Output Differential Pairs 53	O PCIE		Not connected
PCIE53_RX+ PCIE53_RX-	F84 F83	PCI Express Receive Input Differential Pairs 53	I PCIE		
PCIE54_TX+ PCIE54_TX-	E88 E87	PCI Express Transmit Output Differential Pairs 54	O PCIE		
PCIE54_RX+ PCIE54_RX-	F87 F86	PCI Express Receive Input Differential Pairs 54	I PCIE		
PCIE55_TX+ PCIE55_TX-	E91 E90	PCI Express Transmit Output Differential Pairs 55	O PCIE		
PCIE55_RX+ PCIE55_RX-	F90 F89	PCI Express Receive Input Differential Pairs 55	I PCIE		
PCIE56_TX+ PCIE56_TX-	H69 H68	PCI Express Transmit Output Differential Pairs 56	O PCIE		
PCIE56_RX+ PCIE56_RX-	G70 G69	PCI Express Receive Input Differential Pairs 56	I PCIE		
PCIE57_TX+ PCIE57_TX-	H72 H71	PCI Express Transmit Output Differential Pairs 57	O PCIE		
PCIE57_RX+ PCIE57_RX-	G73 G72	PCI Express Receive Input Differential Pairs 57	I PCIE		
PCIE58_TX+ PCIE58_TX-	H75 H74	PCI Express Transmit Output Differential Pairs 58	O PCIE		
PCIE58_RX+ PCIE58_RX-	G76 G75	PCI Express Receive Input Differential Pairs 58	I PCIE		
PCIE59_TX+ PCIE59_TX-	H78 H77	PCI Express Transmit Output Differential Pairs 59	O PCIE		
PCIE59_RX+ PCIE59_RX-	G79 G78	PCI Express Receive Input Differential Pairs 59	I PCIE		
PCIE60_TX+ PCIE60_TX-	H81 H80	PCI Express Transmit Output Differential Pairs 60	O PCIE		
PCIE60_RX+ PCIE60_RX-	G82 G81	PCI Express Receive Input Differential Pairs 60	I PCIE		
PCIE61_TX+ PCIE61_TX-	H84 H83	PCI Express Transmit Output Differential Pairs 61	O PCIE		
PCIE61_RX+ PCIE61_RX-	G85 G84	PCI Express Receive Input Differential Pairs 61	I PCIE		
PCIE62_TX+ PCIE62_TX-	H87 H86	PCI Express Transmit Output Differential Pairs 62	O PCIE		
PCIE62_RX+ PCIE62_RX-	G88 G87	PCI Express Receive Input Differential Pairs 62	I PCIE		
PCIE63_TX+ PCIE63_TX-	H90 H89	PCI Express Transmit Output Differential Pairs 63	O PCIE		
PCIE63_RX+ PCIE63_RX-	G91 G90	PCI Express Receive Input Differential Pairs 63	I PCIE		

PCIE_BMC_TX+ PCIE_BMC_TX-	A60 A59	PCI Express Differential Transmit Pair for carrier BMC	O PCIE		Supports PCI Express Base Specification, Revision 3.0 for carrier BMC
PCIE_BMC_RX+ PCIE_BMC_RX-	B59 B58	PCI Express Differential Receive Pair for carrier BMC	I PCIE		
PCIe_REFCLK0_LO+ PCIe_REFCLK0_LO-	C60 C59	Reference clock pair for PCIe lanes [0:7], also referred to as PCIe Group 0 Low and for the PCIe_BMC link	O LV_DIFF		PCIe clock for PCIe Gen 3 devices and BMC (lanes 0 - 7)
PCIe_REFCLK0_HI+ PCIe_REFCLK0_HI-	C57 C56	Reference clock pair for PCIe lanes [8:15] also referred to as PCIe Group 0 High	O LV_DIFF		PCIe clock for PCIe Gen 3 devices (lanes 8 - 15)
PCIe_REFCLK1+ PCIe_REFCLK1-	E94 E93	Reference clock pair for PCIe lanes [16:31] also referred to as PCIe Group 1	O LV_DIFF		PCIe clock for PCIe Gen 4 devices (lanes 16 - 31)
PCIe_REFCLK2+ PCIe_REFCLK2-	F93 F92	Reference clock pair for PCIe lanes [32:47] also referred to as PCIe Group 2	O LV_DIFF		PCIe clock for PCIe Gen 4 devices (lanes 32 - 47)
PCIe_REFCLK3+ PCIe_REFCLK3-	G94 G93	Reference clock pair for PCIe lanes [48:63] also referred to as PCIe Group 3	O LV_DIFF		PCIe clock for PCIe Gen 3 devices
PCIe_CLKREQ0_LO#	A56	PCIe reference clock request signal from carrier devices for PCIe_REFCLK0_LO clock pair	Bi-Dir OD 3.3 V	PU 10 KΩ 3.3 V	Reference clock control for PCIe Gen 3 devices
PCIe_CLKREQ0_HI#	A57	PCIe reference clock request signal from carrier devices for PCIe_REFCLK0_HI clock pair	Bi-Dir OD 3.3 V	PU 10 KΩ 3.3 V	
PCIe_CLKREQ1#	E96	PCIe reference clock request signal from carrier devices for PCIe_REFCLK1 clock pair	Bi-Dir OD 3.3 V	PU 10 KΩ 3.3 V	Reference clock control for PCIe Gen 4 devices
PCIe_CLKREQ2#	E97	PCIe reference clock request signals from carrier devices for PCIe_REFCLK2 clock pair	Bi-Dir OD 3.3 V	PU 10 KΩ 3.3 V	
PCIe_CLKREQ3#	F95	PCIe reference clock request signal from carrier devices for PCIe_REFCLK3 pair	Bi-Dir OD 3.3 V	PU 10 KΩ 3.3 V	Reference clock control for PCIe Gen 3 devices
PCI Express Additional Signals to Support Module-based PCIe Targets					
PCIe_REFCLKIN0+ PCIe_REFCLKIN0-	H93 H92	Reference clock inputs allowing carrier based root to operate with module based PCIe targets. The module designer making use of these clocks should terminate them in a way appropriate to that design.	I LV_DIFF 3.3 V		Not connected
PCIe_REFCLKIN1+ PCIe_REFCLKIN1-	H96 H95	Reference clock inputs allowing carrier based root to operate with module based PCIe targets. The module designer making use of these clocks should terminate them in a way appropriate to that design.	I LV_DIFF 3.3 V		
PCIe_WAKE_OUT0#	G100	Wake request signal from module based PCIe target to an off-module PCIe Root complex	OD 3.3 V		
PCIe_WAKE_OUT1#	H100	Wake request signal from module based PCIe target to an off-module PCIe root complex	OD 3.3 V		
PCIe_PERST_IN0#	E100	Reset signals into module to reset module PCIe targets	I 3.3 V		
PCIe_PERST_IN1#	F100	Reset signals into module to reset module PCIe targets	I 3.3 V		

Table 24 NBASE-T Ethernet Signal Descriptions

<table>
<tr><th>Gigabit Ethernet</th><th>Pin #</th><th>Description</th><th>I/O</th><th>PU/PD</th><th>Comment</th></tr>
<tr><td>NBASET0_MDI0+
NBASET0_MDI0-
NBASET0_MDI1+
NBASET0_MDI1-
NBASET0_MDI2+
NBASET0_MDI2-
NBASET0_MDI3+
NBASET0_MDI3-</td><td>D86
D85
D89
D88
D92
D91
D95
D94</td><td>Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 10 Gbps, 1 Gbps, 100 Mbps and 10 Mbps modes.
Some pairs are unused in some modes, per the following:

<table><tr><td></td><td>10000BASE-T
1000BASE-T</td><td>100BASE-TX</td><td>10BASE-T</td></tr><tr><td>MDI[0]+/-</td><td>B1_DA+/-</td><td>TX+/-</td><td>TX+/-</td></tr><tr><td>MDI[1]+/-</td><td>B1_DB+/-</td><td>RX+/-</td><td>RX+/-</td></tr><tr><td>MDI[2]+/-</td><td>B1_DC+/-</td><td></td><td></td></tr><tr><td>MDI[3]+/-</td><td>B1_DD+/-</td><td></td><td></td></tr></table></td><td>I/O MDI
3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_ACT#</td><td>D99</td><td>NBASE-T Ethernet controller activity indicator, active low.
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_MAX#</td><td>D97</td><td>NBASE-T Ethernet controller maximum speed link indicator (active low). If active, the link is established at the maximum speed that the Ethernet controller is capable of (which may be 10G, 5G, 2.5G etc).
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_MID#</td><td>D98</td><td>NBASE-T Ethernet controller mid speed link indicator (active low). If active, the link is established but at a speed lower than what the maximum speed that the Ethernet controller is capable of.
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_CTREF</td><td>C99</td><td>Reference voltage for carrier board NBASET Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V.

If not needed, these pins may be left open on the carrier. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.</td><td>REF</td><td></td><td>Not connected</td></tr>
<tr><td>NBASET0_SDP</td><td>C98</td><td>NBASE-T Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.</td><td>I/O 3.3 VSB</td><td></td><td></td></tr>
</table>

Note

The MAC address of the Intel i226 Ethernet controller is preprogrammed by default. The MAC address cannot be reprogrammed. If you require custom MAC address, contact your local sales representative.

Table 25 Ethernet KR and KX Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
ETH0_TX+ ETH0_TX-	C21 C20	Ethernet KR ports, transmit output differential pairs.	O KR		
ETH0_RX+ ETH0_RX-	D20 D19	Ethernet KR ports, receive input differential pairs.	I KR		
ETH1_TX+ ETH1_TX-	C24 C23	Ethernet KR ports, transmit output differential pairs.	O KR		
ETH1_RX+ ETH1_RX-	D23 D22	Ethernet KR ports, receive input differential pairs.	I KR		
ETH2_TX+ ETH2_TX-	C27 C26	Ethernet KR ports, transmit output differential pairs.	O KR		
ETH2_RX+ ETH2_RX-	D26 D25	Ethernet KR ports, receive input differential pairs.	I KR		
ETH3_TX+ ETH3_TX-	C30 C29	Ethernet KR ports, transmit output differential pairs.	O KR		
ETH3_RX+ ETH3_RX-	D29 D28	Ethernet KR ports, receive input differential pairs.	I KR		
ETH4_TX+ ETH4_TX-	A36 A35	Ethernet KR ports, transmit output differential pairs.	O KR		
ETH4_RX+ ETH4_RX-	A21 A20	Ethernet KR ports, receive input differential pairs.	I KR		
ETH5_TX+ ETH5_TX-	A39 A38	Ethernet KR ports, transmit output differential pairs.	O KR		
ETH5_RX+ ETH5_RX-	A24 A23	Ethernet KR ports, receive input differential pairs.	I KR		
ETH6_TX+ ETH6_TX-	A42 A41	Ethernet KR ports, transmit output differential pairs.	O KR		
ETH6_RX+ ETH6_RX-	A27 A26	Ethernet KR ports, receive input differential pairs.	I KR		
ETH7_TX+ ETH7_TX-	A45 A44	Ethernet KR ports, transmit output differential pairs.	O KR		
ETH7_RX+ ETH7_RX-	A30 A29	Ethernet KR ports, receive input differential pairs.	I KR		
ETH0-3_MDIO_DAT [1]	H99	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 3	I/O 3.3 VSB	PU 952Ω 3.3 VSB	
ETH0-3_MDIO_CLK [1]	H98	Clock signal for Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 3	O 3.3 VSB	PU 952Ω 3.3 VSB	
ETH4-7_MDIO_DAT	F11	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 4 to 7	I/O 3.3 VSB	PU 952Ω 3.3 VSB	
ETH4-7_MDIO_CLK	F10	Clock signal for Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 4 to 7	O 3.3 VSB	PU 952Ω 3.3 VSB	
ETH0-3_INT#	G99	Active low interrupt signal from IO Port expanders for ETH ports 0 to 3	I 3.3 VSB	PU 10 KΩ 3.3 VSB	

ETH4-7_INT#	F9	Active low interrupt signal from IO Port expanders for ETH ports 4 to 7	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
ETH0-3_PHY_INT#	G98	Active low PHY interrupt signal from ETH ports 0 to 3	I 3.3 V	PU 10 KΩ 3.3 VSB	
ETH4-7_PHY_INT#	F12	Active low PHY interrupt signal from ETH ports 4 to 7	I 3.3 V	PU 10 KΩ 3.3 VSB	
ETH0-3_PHY_RST#	F97	Active low output PHY reset signal for ETH ports 0 to 3	O 3.3 V	PD 10 KΩ	
ETH4-7_PHY_RST#	F13	Active low output PHY reset signal for ETH ports 4 to 7	O 3.3 V	PD 10 KΩ	
ETH0-3_I2C_DAT	G97	I2C data signal of the 2-wire management interface used by the Ethernet KR controller to access the management registers of an external SFP module or to configure the carrier PHY for ETHx ports 0 to 3 and for serialized status information (e.g. LED states)	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
ETH0-3_I2C_CLK	G96	The I2C clock signals associated with ETH0-3 I2C data lines in the row above	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
ETH4-7_I2C_DAT	F8	I2C data signal of the 2-wire management interface used by the Ethernet KR controller to access the management registers of an external SFP module or to configure the carrier PHY for ETHx ports 4 to 7 and for serialized status information (e.g. LED states)	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
ETH4-7_I2C_CLK	F7	The I2C clock signals associated with ETH4-7 I2C data lines in the row above	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
ETH0_SDP [1]	F98	ETH0 Software-Definable Pin	I 3.3 VSB	PU 10 KΩ 3.3 VSB	Not supported by default. See section 5.3.3 "IEEE 1588 and Time Synchronization" for more information.
ETH1_SDP [1]	F99	ETH1 Software-Definable Pin	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
ETH2_SDP [1]	F1	ETH2 Software-Definable Pin	O 3.3 VSB	PU 10 KΩ 3.3 VSB	
ETH3_SDP [1]	F2	ETH3 Software-Definable Pin	O 3.3 VSB	PU 10 KΩ 3.3 VSB	
ETH4_SDP	F3	Software-Definable Pins. By default, ETH4_SDP and ETH6_SDP can be used for SyncE while ETH5_SDP and ETH7_SDP can be used for IEEE1588 (PPS).	O 3.3 VSB		Supported on variants with part numbers 050995 and 050996. Assembly option on other variants.
ETH5_SDP	F4		O 3.3 VSB		
ETH6_SDP	F5		I 3.3 VSB		
ETH7_SDP	F6		I 3.3 VSB		
ETH0-3_PRSNT#	F96	Carrier pulls this line to GND if there is carrier hardware present to support Ethernet KR signaling on ETH0 through ETH3. If the entire KR quad is not supported it should fill from ETH0 on up	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
ETH4-7_PRSNT#	F14	Carrier pulls this line to GND if there is carrier hardware present to support Ethernet KR signaling on ETH4 through ETH7. If the entire KR quad is not supported it should fill from ETH4 on up	I 3.3 VSB	PU 10 KΩ 3.3 VSB	

Note

1. *These signals have special function during the reset process. For more information, see section 8.2 "Boot Strap Signals".*

Table 26 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_TX+ SATA0_TX-	D53 D52	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports SATA specification 3.2
SATA0_RX+ SATA0_RX-	D50 D49	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports SATA specification 3.2
SATA1_TX+ SATA1_TX-	D59 D58	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports SATA specification 3.2
SATA1_RX+ SATA1_RX-	D56 D55	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports SATA specification 3.2

Table 27 USB Signal Descriptions

USB	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	D17 D16	USB 2.0 differential pairs, channels 0 through 3. USB0 may be configured as a USB client or as a host, or both at the module designer's discretion. All other USB ports, if implemented, shall be host ports If any SuperSpeed ports are implemented, then they must be supported by a USB 2.0 port, using one of the USB[0:3] ports from this pool.	I/O USB 3.3 V		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+ USB1-	D14 D13		I/O USB 3.3 V		
USB2+ USB2-	C18 C17		I/O USB 3.3 V		
USB3+ USB3-	C15 C14		I/O USB 3.3 V		
USB4+ USB4-	B17 B16	USB 2.0 differential pairs, channels 4 through 7.	I/O USB 3.3 V		Not connected
USB5+ USB5-	B14 B13		I/O USB 3.3 V		
USB6+ USB6-	A18 A17		I/O USB 3.3 V		
USB7+ USB7-	A15 A14		I/O USB 3.3 V		
USB0_SSTX0+ USB0_SSTX0-	D44 D43	USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB0 USB 2.0 differential pairs)	O USB SS		USB 3.1 Gen 1 compliant.
USB0_SSRX0+ USB0_SSRX0-	C45 C44		I USB SS		
USB0_SSTX1+ USB0_SSTX1-	D47 D46	Additional sets of SuperSpeed differential pairs used to realize one USB 3.2 Gen 2 port 0.	O USB SS		Not connected
USB0_SSRX1+ USB0_SSRX1-	C48 C47		I USB SS		

USB1_SSTX0+ USB1_SSTX0-	D38 D37	USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB1 USB 2.0 differential pairs)	O USB SS		USB 3.1 Gen 1 compliant.
USB1_SSRX0+ USB1_SSRX0-	C39 C38		I USB SS		
USB1_SSTX1+ USB1_SSTX1-	D41 D40	Additional sets of SuperSpeed differential pairs used to realize one USB 3.2 Gen 2 port 1.	O USB SS		Not connected
USB1_SSRX1+ USB1_SSRX1-	C42 C41		I USB SS		
USB2_SSTX+ USB2_SSTX-	D35 D34	Two sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 1 or Gen 2 implementation This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB2 USB 2.0 differential pairs)	O USB SS		USB 3.1 Gen 1 compliant.
USB2_SSRX+ USB2_SSRX-	C36 C35		I USB SS		
USB3_SSTX+ USB3_SSTX-	D32 D31	Two sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 1 or Gen 2 implementation. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB3 USB 2.0 differential pairs)	O USB SS		USB 3.1 Gen 1 compliant.
USB3_SSRX+ USB3_SSRX-	C33 C32		I USB SS		
USB01_OC#	B28	USB over-current sense, USB channels 0,1; channels 2,3; channels 4,5 and channels 6,7 respectively. A pull-up for each of these lines to the 3.3V Suspend rail shall be present on the module. The pull-up should be 10K. An open drain driver from USB current monitors on the carrier board may drive this line low. The carrier board shall not pull these lines up Note that the over-current limits for USB 2.0 and USB 3.0 are different; this is a carrier board implementation item.	I 3.3 V	PU 10 KΩ 3.3 VSB	
USB23_OC#	B27			PU 10 KΩ 3.3 VSB	
USB45_OC#	B26				Not connected
USB67_OC#	B25				Not connected
RSMRST_OUT#	B86	USB devices that are to be powered in the S5 Suspend states should not have their 5 V VBUS power enabled before RSMRST_OUT# transitions to the high state.	O 3.3 V	PD 10 KΩ	

Table 28 USB 4 Support Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0_AUX+ USB0_AUX-	B44 B43	DisplayPort Aux channel for USB4 DP modes High speed differential pair	LV_DIFF		Not connected
USB1_AUX+ USB1_AUX-	A48 A47	DisplayPort Aux channel for USB4 DP modes High speed differential pair	LV_DIFF		
USB0_LSTX	B41	Sideband TX interface for USB4 Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V		
USB0_LSRX	B40	Sideband RX interface for USB4 Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V		
USB1_LSTX	B39	Sideband TX interface for USB4 Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V		
USB1_LSRX	B38	Sideband RX interface for USB4 Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V		
SML0_DAT	B33	Data line for I2C data based System Management Links between chipset masters and carrier.	Bi-Dir OD 3.3 VSB	PU 499 Ω 3.3 VSB	
SML1_DAT	B30				
SML0_CLK	B32	Clock lines for System Management Links 0 and 1.	Bi-Dir OD 3.3 VSB	PU 499 Ω 3.3 VSB	
SML1_CLK	B29				
PMCALERT#	B31	Active low Alert signal associated with the SML1 System Management link	I 3.3 VSB	PU 2.2 KΩ 3.3 VSB	Not connected
USB_RT_ENA	B37	Power Enable signal	O 3.3 V	PD 10 KΩ	
USB_PD_I2C_DAT	B36	I2C data line	Bi-Dir OD 3.3 V	PU 2.2 KΩ 3.3 VSB	Used for port 80 redirection
USB_PD_I2C_CLK	B35	I2C clock line	Bi-Dir OD 3.3 V	PU 2.2 KΩ 3.3 VSB	Used for port 80 redirection
USB_PD_ALERT#	B34	Active low Alert signal f	I 3.3 V	PU 2.2 KΩ 3.3 VSB	
Additional Signals to Support USB4 Implementation					
PLTRST#	A12	Platform Reset: output from module to carrier board. Active low. Issued by module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software PLTRST# should remain asserted (low) while the RSTBTN# is low.	O 3.3 V	PD 10 KΩ	
SUS_S4_S5#	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output	O 3.3 V	PD 10 KΩ	The Intel SoC does not support Suspend to Disk (S4) state

Note

1. *The conga-HPC/sILH does not support USB 4.*

Table 29 eSPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eSPI_IO0	A50	eSPI Master Data Input / Outputs. These are bi-directional input/output pins used to transfer data between master and slaves	I/O 1.8 VSB	PU 10 KΩ 1.8 VSB	
eSPI_IO1	A51			PU 10 KΩ 1.8 VSB	
eSPI_IO2	A52			PU 10 KΩ 1.8 VSB	
eSPI_IO3	A53			PU 10 KΩ 1.8 VSB	
eSPI_CS0#	B54	eSPI Master Chip Select Outputs. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select pin. If an eSPI_CSx# pins is not in use, it shall be either pulled high or actively driven high	O 1.8 VSB	PU 10 KΩ 1.8 VSB	
eSPI_CS1#	B55			PU 10 KΩ 1.8 VSB	Not connected
eSPI_CLK	A54	eSPI Master Clock Output. This pin provides the reference timing for all the serial input and output operations	O 1.8 VSB	PD 10 KΩ	
eSPI_ALERT0#	B52	eSPI pins used by eSPI slave to request service from the eSPI master	I 1.8 VSB	PU 1 KΩ 1.8 VSB	
eSPI_ALERT1#	B53	eSPI pins used by eSPI slave to request service from the eSPI master	I 1.8 VSB	PU 10 KΩ 1.8 VSB	Not supported
eSPI_RST#	B56	eSPI Reset - resets the eSPI interface for both master and slaves. eSPI_RST# is typically driven from the eSPI master to eSPI slaves	O 1.8 VSB	PU 20 KΩ 1.8 VSB	

Table 30 Boot SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
BOOT_SPI_CS#	B48	Chip select for carrier board SPI If the BOOT_SPI_CS# pin is not in use, it shall be either pulled high or actively driven high.	O VCC_BOOT_SPI	PU 20 KΩ 3.3 VSB	
BOOT_SPI_IO0	C50	Bidirectional 4 bit data path out of and into a carrier SPI flash operating in Serial Quad Interface (SQI) mode. If the flash memory device is operating in traditional Serial Peripheral Interface (SPI) mode, then signal BOOT_SPI_IO0 is used for getting serial data into the flash device (referred to as SI or MOSI in SPI Flash data sheets) and signal BOOT_SPI_IO1 is used to get serial data from the flash device (referred to as SO or MISO in flash data sheets)	I/O VCC_BOOT_SPI	PU 20 KΩ 3.3 VSB	
BOOT_SPI_IO1	C51			PU 20 KΩ 3.3 VSB	
BOOT_SPI_IO2	C52			PU 20 KΩ 3.3 VSB	
BOOT_SPI_IO3	C53			PU 20 KΩ 3.3 VSB	
BOOT_SPI_CLK	C54	Clock from module chipset to carrier SPI	O VCC_BOOT_SPI	PU 20 KΩ 3.3 VSB	
VCC_BOOT_SPI	B47	Power supply for carrier board SPI – sourced from module – nominally either 1.8V or 3.3V. The module shall provide a minimum of 100mA on VCC_BOOT_SPI. Carriers shall use less than 100mA from this power source. VCC_BOOT_SPI shall only be used to power SPI devices on the carrier board. The module vendor may choose what power domains the BOOT_SPI is active in.	Power (Out from module)		3.3 VSB (active in suspend state)

Table 31 BIOS Select Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
BSEL2	B51	Boot Select pins. These pins distinguish between a SPI or eSPI BIOS boot and between an on—module or off-module BIOS. Pulled up on module to vendor specific power rail	I 3.3 VSB		Not connected
BSEL1	B50		I 3.3 VSB		Not connected
BSEL0	B49		I 3.3 VSB	PU 10 KΩ 3.3 VSB	Pulled up to 3.3 VSB (active in suspend state)

Table 32 Asynchronous Serial Port Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
UART0_TX	C89	Logic level asynchronous serial port transmit signal	O 3.3 V		
UART0_RX	C90	Logic level asynchronous serial port receive signal	I 3.3 V	PU 20 KΩ 3.3V	
UART0_RTS#	C91	Logic level asynchronous serial port Request to Send signal, active low	O 3.3 V		
UART0_CTS#	C92	Logic level asynchronous serial port Clear to Send input, active low	I 3.3 V	PU 20 KΩ 3.3V	
UART1_TX	B87	Logic level asynchronous serial port transmit signal	O 3.3 V		
UART1_RX	B88	Logic level asynchronous serial port receive signal	I 3.3 V	PU 20 KΩ 3.3V	
UART1_RTS#	B89	Logic level asynchronous serial port Request to Send signal, active low	O 3.3 V		
UART1_CTS#	B90	Logic level asynchronous serial port Clear to Send input, active low	I 3.3 V	PU 20 KΩ 3.3V	

Table 33 I²C Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C0_CLK	C93	Clock I/O line for the general purpose I2C0 port	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
I2C0_DAT	C94	Data I/O line for the general purpose I2C0 port	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
I2C0_ALERT#	C95	Alert input / interrupt for I2C0	I 3.3 V	PU 2.2 KΩ 3.3 VSB	
I2C1_CLK	C96	Clock I/O line for the general purpose I2C1 port	I/O OD 1.8 V	PU 2.2 KΩ 1.8 VSB	
I2C1_DAT	C97	Data I/O line for the general purpose I2C1 port	I/O OD 1.8 V	PU 2.2 KΩ 1.8 VSB	

Table 34 IPMB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
IPMB_CLK	B91	Clock I/O line for the multi-master IPMB port	I/O OD 3.3 VSB	PU 47 KΩ 3.3 VSB	
IPMB_DAT	B92	Data I/O line for the multi-master IPMB port	I/O OD 3.3 VSB	PU 47 KΩ 3.3 VSB	

Table 35 General Purpose SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GP_SPI_MISO	B94	Serial data into the COM-HPC module from the carrier GP_SPI device ("Master In Slave Out")	I 3.3 V	PU 10 KΩ 3.3 V	
GP_SPI_MOSI	B93	Serial data from the COM-HPC module to the carrier GP_SPI device ("Master Out Slave In")	O 3.3 V		
GP_SPI_CLK	B99	Clock from the module to carrier GP_SPI device	O 3.3 V		
GP_SPI_CS0#	B95	GP_SPI chip selects, active low	O 3.3 V	PU 10 KΩ 3.3 V	
GP_SPI_CS1#	B96			PU 10 KΩ 3.3 V	
GP_SPI_CS2#	B97	GP_SPI chip selects, active low		PU 10 KΩ 3.3 V	Not supported
GP_SPI_CS3#	B98				
GP_SPI_ALERT#	B100	Alert (interrupt) from a carrier GP_SPI device to the module	I 3.3 V	PU 10 KΩ 3.3 V	

Table 36 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B02	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as to power the system down (with a sustained low).	I 3.3 VSB		
RSTBTN#	C02	Reset button input. The RSTBTN# may be level sensitive (active low) or may be triggered by the falling edge of the signal. The module PLTRST# signal (below) should not be released (driven or pulled high) while the RSTBTN# is low. For situations when RSTBTN# is not able to reestablish control of the system, VIN_PWR_OK or a power cycle may be used.	I 3.3 VSB		
PLTRST#	A12	Platform Reset: Active low output from module to carrier board. Issued by module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.	O 3.3 VSB	PD 10 KΩ	
VIN_PWROK	C06	Power OK from main power supply. A high value indicates that the power is good.	I 3.3 VSB		
SUS_S3#	B08	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the carrier board should be used to enable the non-standby power on a typical ATX supply. Even in single input supply system implementations (AT mode, no standby input), the SUS_S3# module output should be used to disable any carrier voltage regulators when SUS_S3# is low, to prevent bleed leakage from carrier circuits into the module.	O 3.3 VSB	PD 10 KΩ	Suspend to RAM is not supported. Signals can be used for Sx state indicator
SUS_S4_S5#	C08	Active low output signal that indicates the system is in Suspend to Disk (S4) or Soft Off (S5) state.	O 3.3 VSB	PD 10 KΩ	Suspend to Disk is not supported. Signals can be used for Sx state indicator

SUS_CLK	A87	32.768 kHz +/- 100 ppm clock used by carrier peripherals such as M.2 cards in their low power modes.	O 3.3 VSB		
WAKE0#	D10	PCI Express wake up signal.	I/O 3.3 VSB	PU 10 KΩ 3.3 VSB	
WAKE1#	D11	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
BATLOW#	A11	Indicates that external battery is low. This port provides a battery-low signal to the module for orderly transitioning to power saving or power cut-off ACPI modes.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
TAMPER#	B06	Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a tamper event.	I 3.3 VSB	PU 1 MΩ 3.3 VSB	
RSMRST_OUT#	B86	This is a buffered copy of the internal module RSMRST# (resume reset, active low) signal. The internal module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable. USB devices on the carrier that are to be active in S5/S0 should not have their 5 V supply applied before RSMRST_OUT# goes high. RSMRST_OUT# shall be a 3.3 V CMOS module output, active in all power states.	O 3.3 V	PD 10 KΩ	

Table 37 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_ SHUTDOWN	E1	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs. Pull-down / disable on module if RAPID_ SHUTDOWN pin is not asserted.	I 5 V	PD 10 KΩ	Not supported by default

Table 38 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CARRIER_HOT#	C04	Input from off-module temp sensor indicating an over-temp situation.	I 3.3 V	PU 10 KΩ 3.3 V	
THERMTRIP#	B04	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3 V	PD 10 KΩ	

Table 39 SMBus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CLK	C86	System Management Bus bidirectional clock line.	I/O OD 3.3 VSB	PU 1 KΩ 3.3 VSB	
SMB_DAT	C87	System Management Bus bidirectional data line.	I/O OD 3.3 VSB	PU 1 KΩ 3.3 VSB	
SMB_ALERT#	C88	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3V	PU 1 KΩ 3.3 VSB	

Table 40 General Purpose Input Output Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPIO_00	A88	General purpose input / output pins. Upon a hardware reset, these pins should be configured as inputs. As inputs, these pins should be able to generate an interrupt to the module host.	I/O 3.3 VSB	PU 100 KΩ 3.3 VSB	
GPIO_01	A89				
GPIO_02	A90				
GPIO_03	A91				
GPIO_04	A92				
GPIO_05	A93				
GPIO_06	A94				
GPIO_07	A95				
GPIO_08	A96				
GPIO_09	A97				
GPIO_10	A98				
GPIO_11	A99				

Table 41 Module Type Definition Signal Description

<table>
<tr><th>Signal</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>TYPE0
TYPE1
TYPE2</td><td>A100
C100
D100</td><td>The TYPE pins indicate to the carrier board the pin-out type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). These pins shall be pulled up on the carrier, to carrier standby voltage rail of 5 V or less. Carrier hardware reads the level on these straps.
<table>
<tr><th></th><th colspan="3">Module Connections</th><th rowspan="2">Meaning</th></tr>
<tr><th>Ref</th><th>TYPE2</th><th>TYPE1</th><th>TYPE0</th></tr>
<tr><td>7</td><td>NC</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>6</td><td>NC</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>5</td><td>NC</td><td>GND</td><td>NC</td><td>Reserved</td></tr>
<tr><td>4</td><td>NC</td><td>GND</td><td>GND</td><td>Server module - Fixed 12 V input</td></tr>
<tr><td>3</td><td>GND</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>2</td><td>GND</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>1</td><td>GND</td><td>GND</td><td>NC</td><td>Client module - Wide range 8 V to 20 V input</td></tr>
<tr><td>0</td><td>GND</td><td>GND</td><td>GND</td><td>Client module - Fixed 12 V input</td></tr>
</table>
The module shall implement all three TYPE[x] pins per the table above.

The carrier board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX PS_ON# signal to an ATX power supply or otherwise deactivates VCC to the COM- HPC module) if an incompatible module pin-out type is detected. All three TYPE[x] pins should be monitored by the carrier. The carrier board logic may also implement a fault indicator such as an LED.</td><td>PDS</td><td></td></tr>
</table>

Table 42 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WD_OUT	B11	Output indicating that a watchdog time-out event has occurred	O 3.3 V	PD 100 KΩ	
WD_STROBE#	B10	Strobe input to watchdog timer. Periodic strobing prevents the watchdog, if enabled, from timing out.	I 3.3 V		
FAN_PWMOUT	C11	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3 V		
FAN_TACHIN	C12	Fan tachometer input for a fan with a two pulse output.	I OD 3.3 V	PU 47 KΩ 3.3 V	
TEST#	B85	Module input to allow vendor specific module test mode(s). Carrier designers should leave this pin open on the carrier. Designers involved in the design of specialty carriers for module test may pull this line to GND or possibly to a module specific analog voltage between GND and 3.3 V to select a test mode.	I OD 3.3 V		
RSVD	A32-A33 B19-B23 B45-B46 E3-E4 E6-E7 E9-E10 E12-E13 E15-E16 E18-E19 F15- F18 G13 G15-G19 H1-H18	Reserved pins. These may be assigned functions in future versions of this specification. Reserved pins shall not be connected to anything, and shall not be connected to each other.			

Table 43 Functional Safety (FuSa) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FUSA_SPI_MOSI	G8	Serial data from the carrier FuSa SPI master to the COM-HPC module SPI slave ("Master Out Slave In")	I 3.3V	PU 10 KΩ 3.3 V	Not supported
FUSA_SPI_MISO	G7	Serial data from the COM-HPC module SPI slave to the carrier FuSa SPI master ("Master In Slave Out")	O 3.3V		Not connected
FUSA_SPI_CS#	G5	Active low chip select from the carrier FuSa Safety controller SPI master to the COM-HPC module	I 3.3V	PU 10 KΩ 3.3 V	Not supported
FUSA_SPI_CLK	G6	Clock from the carrier FuSa Safety controller SPI master to the COM-HPC module	I 3.3V	PU 10 KΩ 3.3 V	
FUSA_SPI_ALERT	G9	Active high alert output from the COM-HPC module to alert the carrier FuSa Safety controller that module FuSa SPI data is available for transfer	O 3.3V		Not connected

THERMTRIP#	B04	Active low output indicating that the CPU has entered thermal shutdown	O 3.3V	PD 10 KΩ	
PROCHOT#	G11	Active low output indicating a temperature excursion event on the COM-HPC module	O 3.3V	PD 10 KΩ	
CATERR#	G12	Active low output indicating a catastrophic error on the COM-HPC CPU or SOC	O 3.3V	PD 10 KΩ	
FUSA_STATUS[1:0]	G3 G2	Two bit FuSa staus / error indication outputs to carrier based Safety Controller hardware (bit 1= NOK; bit 0 = OK) 00 - power off 01 - no error (OK state) 10 - error state (NOK state) 11 - reset state	O 3.3V		Not connected
FUSA_ALERT#	G4	Active low output from the COM-HPC module that signals the occurrence of a correctable error on the COM-HPC module; the carrier FuSa Safety Controller should query the status via the FuSa SPI interface	O 3.3V		
FUSA_VOLTAGE_ERR#	G10	Active low output indicating an over- or under voltage or over-current condition of the monitored voltage rails of the FuSa relevant module power supply	O 3.3V		

Note

The conga-HPC/sILH does not support FuSa.

Table 44 External Power Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	A01-A09, B01, B03, B05, B07, B09 C01, C03, C05, C07, C09 D01-D09	Primary power input: • fixed +12V on the Client Type 0; • wide range +8V to +20V on the Client Type 1; • fixed +12V on the Server. Refer to section 2.4.1 “Electrical Characteristics” for further details. All available VCC pins on the connector shall be used.			
VCC_5V_SBY	B24 G1	Standby power input: +5.0V nominal. Refer to section 2.4.1 “Electrical Characteristics” for further details. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.			
VCC_RTC	A86	Real-time clock circuit-power input. Nominally +3.0V. section 2.4.1 “Electrical Characteristics” for details.			

GND	A10, A13, A16, A19, A22, A25, A28, A31, A34, A37, A40, A43, A46, A49, A55, A58, A61, A64, A67, A70, A73, A76, A79, A82, A85 B12, B15, B18, B42, B57, B60, B63, B66, B69, B72, B75, B78, B81, B84 C10, C13, C16, C19, C22, C25, C28, C31, C34, C37, C40, C43, C46, C49, C55, C58, C61, C64, C67, C70, C73, C76, C79, C82, C85 D12, D15, D18, D21, D24, D27, D30, D33, D36, D39, D42, D45, D48, D51, D54, D57, D60, D63, D66, D69, D72, D75, D78, D81, D84, D87, D90, D93, D96 E2, E5, E8, E11, E14, E17, E20, E23, E26, E29, E32, E35, E38, E41, E44, E47, E50, E53, E56, E59, E62, E65, E68, E71, E74, E77, E80, E83, E86, E89, E92, E95 F19, F22, F25, F28, F31, F34, F37, F40, F43, F46, F49, F52, F55, F58, F61, F64, F67, F70, F73, F76, F79, F82, F85, F88, F91, F94 G14, G20, G23, G26, G29, G32, G35, G38, G41, G44, G47, G50, G53, G56, G59, G62, G65, G68, G71, G74, G77, G80, G83, G86, G89, G92, G95 H19, H22, H25, H28, H31, H34, H37, H40, H43, H46, H49, H52, H55, H58, H61, H64, H67, H70, H73, H76, H79, H82, H85, H88, H91, H94, H97	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane(s).			

8.2 Boot Strap Signals

Table 45 Boot Strap Signal Descriptions

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
ETH0_SDP	F98	Software-Definable Pins	I/O 3.3 VSB	PU 10 KΩ 3.3 VSB	
ETH1_SDP	F99				
ETH2_SDP	F1				
ETH3_SDP	F2				
ETH0-3_MDIO_DAT	H99	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 3	I/O 3.3 VSB	PU 952Ω 3.3 VSB	
ETH0-3_MDIO_CLK	H98	Clock signal for Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 3	O 3.3 VSB	PU 952Ω 3.3 VSB	

Note

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), the COM-HPC or chipset internally implemented resistors pull these signals to the correct state.

Caution

No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External circuitry may override the internal strap states and cause the COM-HPC module to malfunction or cause irreparable damage to the module.

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-HPC/sILH module is functionally identical with a standard PC/AT. The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards.

Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.2 PCI Configuration Space Map

Table 1 PCI Configuration Space Map

Bus Number (Hex)	Device Number (Hex)	Function Number (Hex)	Description and Device ID
00h [1]	00h	00h	Mesh2IIO MMAP/VT-D
00h [1]	00h	01h	Mesh2IIO PMON
00h [1]	00h	02h	Mesh2IIO RAS
00h [1]	00h	03h	Mesh2IIO DFX
00h [1]	00h	04h	Satellite IEH
00h	01h	00h	Intel QuickData Technology CH0
00h	01h	01h	Intel QuickData Technology CH1
00h	01h	02h	Intel QuickData Technology CH2
00h	01h	03h	Intel QuickData Technology CH3
00h	01h	04h	Intel QuickData Technology CH4
00h	01h	05h	Intel QuickData Technology CH5
00h	01h	06h	Intel QuickData Technology CH6
00h	01h	07h	Intel QuickData Technology CH7
00h	02h	00h	PECI Out-Of-Band Management Services Module (OOB-MSM)
00h	02h	01h	PECI OOB-MSM - Performance Monitoring Unit (PMU)
00h	02h	04h	CPU Intel Trace Hub
00h	09h	00h	PCH PCIe Cluster 0 Root Port 0 (downstream is COM Express PCIe 0–7)
00h	0Eh	00h	SATA Controller
00h	0Fh	00h	Host SMBus
00h [2]	10h	00h	PCH PCIe Cluster 1 Root Port 4 (downstream is COM Express PCIe 8–11)
00h [2]	12h	00h	PCH PCIe Cluster 1 Root Port 6 (downstream is COM Express PCIe 12–15)
00h [2]	14h	00h	PCH PCIe Cluster 2 Root Port 8 (downstream is Intel I226 Ethernet controller)
00h [2]	15h	00h	PCH PCIe Cluster 2 Root Port 9 (downstream is Aspeed AST2600)
00h [3]	18h	00h	Intel ME - HECI 1

00h [3]	18h	01h	Intel ME - HECI 2
00h [3]	18h	04h	Intel ME - HECI 3
00h	1Ah	00h	HSUART 0
00h	1Ah	01h	HSUART 1
00h	1Ah	02h	HSUART 2
00h	1Ah	03h	Reserved
00h	1Dh	00h	Satellite IEH
00h	1Eh	00h	USB Combo Controller
00h	1Eh	02h	Intel RAM
00h	1Fh	00h	LPC/eSPI Controller
00h	1Fh	04h	Legacy SMBus
00h	1Fh	05h	SPI Controller
00h	1Fh	07h	PCH Intel Trace Hub
01h [4]	00h	00h	PCIe Device inserted in PCI Express Port 0-7
02h [4]	00h	00h	PCIe Device inserted in PCI Express Port 8-11
03h [4]	00h	00h	PCIe Device inserted in PCI Express Port 12-15
04h [4]	00h	00h	Intel Ethernet I226
05h [4]	00h	00h	ASPEED2600
06h [4]	00h	00h	ASPEED2600 VGA
15h [1]	00h	00h	Mesh2IIO MMAP/VT-D
15h [1]	00h	01h	Mesh2IIO PMON
15h [1]	00h	02h	Mesh2IIO RAS
15h [1]	00h	03h	Mesh2IIO DFX
15h [1]	00h	04h	Satellite IEH
80h [1]	00h	00h	Mesh2IIO MMAP/VT-D
80h [1]	00h	01h	Mesh2IIO PMON
80h [1]	00h	02h	Mesh2IIO RAS
80h [1]	00h	03h	Mesh2IIO DFX
80h [1]	00h	04h	Satellite IEH
88h [1]	00h	00h	Mesh2IIO MMAP/VT-D
88h [1]	00h	01h	Mesh2IIO PMON
88h [1]	00h	02h	Mesh2IIO RAS
88h [1]	00h	03h	Mesh2IIO DFX
88h [1]	00h	04h	Satellite IEH
89h	00h	00h	25G Ethernet Controller
89h	00h	01h	25G Ethernet Controller
89h	00h	02h	25G Ethernet Controller
89h	00h	03h	25G Ethernet Controller
90h [1]	00h	00h	Mesh2IIO MMAP/VT-D
90h [1]	00h	01h	Mesh2IIO PMON
90h [1]	00h	02h	Mesh2IIO RAS

90h [1]	00h	03h	Mesh2IIO DFX
90h [1]	00h	04h	Satellite IEH
FEh	00h	00h	UBOX - Global Events
FEh	00h	01h	UBOX
FEh	00h	02h	UBOX -DEC
FEh	00h	03h	UBOX - Global IEH
FEh	00h	05h	MS2UBox
FEh	0Bh	00h	SPD0_SMBUS
FEh	0Bh	01h	SPD1_SMBUS
FEh	0Bh	02h	VPP_SMBUS
FEh	0Ch	00h	Mesh2IMC0
FEh	0Dh	00h	Mesh2IMC1
FEh	1Ah	00h	IMC0
FEh	1Bh	00h	IMC1
FFh	00h	00h	CHA0_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	01h	CHA1_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	02h	CHA2_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	03h	CHA3_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	04h	CHA4_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	05h	CHA5_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	06h	CHA6_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	07h	CHA7_GRP1 - UNICAST_GROUP1_CHA
FFh	01h	00h	CHA8_GRP1 - UNICAST_GROUP1_CHA
FFh	01h	01h	CHA9_GRP1 - UNICAST_GROUP1_CHA
FFh	01h	02h	CHA10_GRP1 - UNICAST_GROUP1_CHA
FFh	01h	03h	CHA11_GRP1 - UNICAST_GROUP1_CHA
FFh	0Ah	00h	CHA0_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	01h	CHA1_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	02h	CHA2_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	03h	CHA3_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	04h	CHA4_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	05h	CHA5_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	06h	CHA6_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	07h	CHA7_GRP0 - UNICAST_GROUP0_CHA
FFh	0Bh	00h	CHA8_GRP0 - UNICAST_GROUP0_CHA
FFh	0Bh	01h	CHA9_GRP0 - UNICAST_GROUP0_CHA
FFh	0Bh	02h	CHA10_GRP0 - UNICAST_GROUP0_CHA
FFh	0Bh	03h	CHA11_GRP0 - UNICAST_GROUP0_CHA
FFh	1Dh	00h	CHAALL0 - Multicast DRAM Rules
FFh	1Dh	01h	CHAALL1 - Multicast MMIO Rules
FFh	1Eh	00h	PCU

FFh	1Eh	01h	PCU
FFh	1Eh	02h	PCU
FFh	1Eh	03h	PCU
FFh	1Eh	04h	PCU
FFh	1Eh	05h	PCU
FFh	1Eh	06h	PCU
FFh	1Eh	07h	PCU

Note

1. *In the standard configuration, the Memory Map / Intel VT-d controller has 3 policy groups on Bus 0, Bus 14h, and Bus F3h.*
2. *The PCI Express Ports are visible only if a device is attached to the PCI Express Slot on the carrier board.*
3. *In the standard configuration, the Intel Management Engine (ME) related devices are partly present or not present at all.*
4. *The table represents a case when a single function PCI/PCIe device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

10 BIOS Setup Description

The BIOS setup description of the conga-HPC/sILH can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note “AN42 - BIOS Setup Description” available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST. The right frame displays the key legend.

Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-HPC/sILH is identified as HEIHR1xx, where:

- R is the identifier for a BIOS binary file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The conga-HPC/sILH BIOS binary size is 64 MB.

10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-HPC/sILH features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions— UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated.*

Caution

Use only the UEFI shell for critical updates. The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates.

10.3.1 Updating from External Flash

For instructions on how to update the BIOS from external flash, refer to the AN7_External_BIOS_Update.pdf application note on the congatec website at http://www.congatec.com.

10.4 Supported Flash Devices

The conga-HPC/sILH supports the following flash devices:

- Winbond W25Q512JVEIQ (DFN8x6 package) 64 MB
- Micron MT25QL512ABB1EW9-0SIT (DFN8x6 package) 64 MB
- Macronix MX25L51245GMI-08G (SOIC16 package) 64 MB

The flash devices listed above can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.