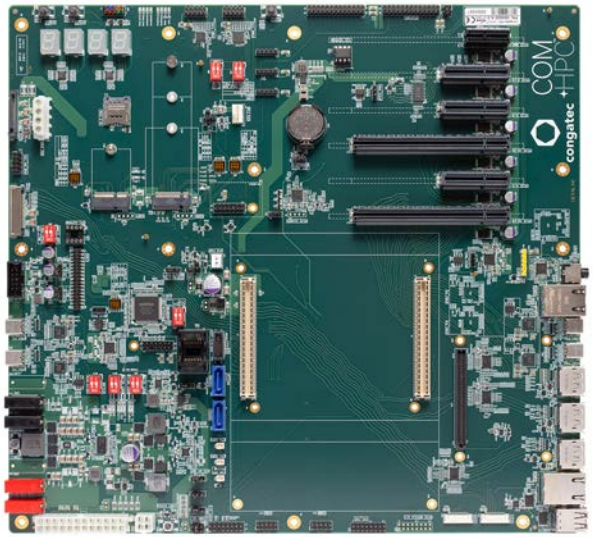

conga-HPC/EVAL-Client

Detailed description of the congatec COM-HPC® evaluation carrier board for client modules

User's Guide

Revision 1.01

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2021-03-15	BEU	• Preliminary release
0.2	2021-04-14	BEU	• Updated operating and storage temperature in section 3.1 “Feature List” and 3.3 “Environmental Specifications”
0.3	2021-07-26	BEU	• Added Software License Information to preface section • Updated section 3.1 “Feature List”
1.00	2023-08-01	BEU	• Updated RoHS Directive in preface section • Updated audio interfaces in Table 1 • Updated image and description in section 2 “Connector Layout” • Updated feature summary in Table 3 • Improved orientation and alignment of connector images throughout the document • Improved information design in section 4.3 “PCIe Connectors” • Removed bifurcation information from note in section 4.3.2 “PCIe x4 Slots” • Added note that LVDS is currently not supported to section 4.4.2 “eDP/LVDS” and 4.4.2.1 “LVDS” • Added PMCALERT# jumper descriptions to section 4.5.1 “USB4 Type-C Ports” • Improved caution in section 4.5.1 “Disk Drive Power Connector” • Merged ethernet connectors X36 and X38 into one image in section 4.7 “Ethernet Ports” • Corrected ETH0/1 to NBASET0/1 in section 4.7 “Ethernet Ports” • Added note about incorrect ETH0/1 writing on the silkscreen to section 4.7 “Ethernet Ports” • Added note about missing SoundWire codec to section 4.9.1 “Audio Jack (4-Pole)” • Added description for additional CPU fan header to section 4.15 “CPU Fan Header” • Updated connector in section 4.24 “CSI Port 0” and 4.25 “CSI Port 1” • Updated number of test points in section 5.2 “Ground Test Points” • Official release
1.01	2025-02-18	BEU	• Updated title page • Added WEEE Compliance Decleration • Updated section 1 “Introduction” • Updated connector layout picture in section 2 “Connector Layout” • Updated section 3.2 “Mechanical Dimensions” • Added note to section 3.3 “Environmental Specifications” • Updated connector pinout Table 4 and Table 5 • Added description of DIP switch 10.2 in section 4.1 “Power Supply Connectors” • Improved description of DIP SW15.1 in section 4.1.1 “ATX Power Connectors” • Added section 4.1.3 “Power Sense Connector” • Updated supported PCIe speed of lanes 16-31 to Gen 5 in table 18 • Updated default setting of JP12 in section 4.1.7 “Module Type Detection” • Added section 4.3.6 “PCIe Clock Request Signals” • Moved information about JP1 from section 4.3 “PCIe Connectors” to section 4.3.6 “PCIe Clock Request Signals” • Updated information about JP1 in section section 4.3.6 “PCIe Clock Request Signals” • Added information about JP16 to section 4.3.6 “PCIe Clock Request Signals” • Added HDA codec and DIP switch 18.1 to section 4.9.1 “Audio Jack (4-Pole)” • Updated section 4.9.2 “I²S/SoundWire” • Added section 4.24 “FuSa Header”

Preface

This user's guide provides information about the components, features, and connectors available on the conga-HPC/EVAL-Client evaluation carrier board.

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The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Connector Type

Describes the connector that must be used with the congatec evaluation carrier board, not the connector found on the congatec evaluation carrier board.

Link to connector layout diagram

This link icon is located in the top left corner of each page. It provides a direct link to the connector layout diagram on page 12 of this document.

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Terminology

Term	Description
PCIe	Peripheral Component Interface Express
SDIO	Secure Digital Input Output
USB	Universal Serial Bus
SATA	Serial AT Attachment
HDA	High Definition Audio
I²C Bus	Inter-Integrated Circuit Bus
SM Bus	System Management Bus
GbE	Gigabit Ethernet
LVDS	Low Voltage Differential Signaling
HBR3	High Bit Rate 3
DDC	Display Data Channel
GPIO	General Purpose Input/Output
eDP	Embedded DisplayPort
LVDS	Low Voltage Differential Signaling
NC	Not connected
NA	Not available
TBD	To be determined

Contents

List of Tables

1 Introduction

1.1 COM-HPC® Concept

COM-HPC® is an open standard defined specifically for high performance Computer-on-Modules (COMs) for embedded systems. The defined module types are client module with fixed input voltage, client module with variable input voltage and server module with fixed input voltage.

The COM-HPC® modules are available in the following form factors:

- Mini 95 mm x 70 mm
- Size A 95 mm x 120 mm
- Size B 120 mm x 120 mm
- Size C 160 mm x 120 mm
- Side D 160 mm x 160 mm
- Side E 200 mm x 160 mm

Table 1 COM-HPC® Interface Summary

Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
Ethernet	NBASE-T	1 / 2	1 / 2	1 / 1	
	KR/KX	N.A	0 / 2	2 / 8	
	SGMII	0 / 2	N.A	N.A	
Storage	SATA	0 / 2	0 / 2	0 / 2	Pin is shared with PCIe on mini module
PCIe	Lane 0-47	1 / 16	4 / 48	8 / 48	Two PCIe reference clock output pairs required on mini module
	Lane 48-63	N.A	N.A	0 / 16	
	BMC	N.A	0 / 1	1 / 1	
USB	USB 2.0 Ports 0-7	6 / 8	4 / 8	4 / 8	Ports 0-5 (mini module) or ports 0-3 (server/client module) are used for USB 3.2 and USB4 if implemented.
	USB 3.2 Gen 1 or Gen 2	0 / 5	0 / 4	0 / 4	Requires one SuperSpeed Tx pair and one Rx pair per port
	USB 3.2 Gen 2x2	0 / 4	0 / 4	0 / 2	Requires two SuperSpeed Tx pairs and two Rx pairs per port
	USB4	0 / 4	0 / 4	0 / 2	USB4 ports use USB 3.2 Gen 2x2 ports
SPI	eSPI	0 / 1	0 / 1	0 / 1	
	Boot SPI	1 / 1	1 / 1	1 / 1	
	General Purpose SPI	1 / 1	1 / 1	1 / 1	
BIOS Select	-	1 / 1	1 / 1	1/1	

Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
Display	DDI	0 / 2	1 / 3	N.A	Additional display outputs may be available on the USB4 interface. On mini module, DDI pins are shared with USB4.
	eDP	0 / 1	0 / 1	N.A	
MIPI	DSI	0 / 1	0 / 1	N.A	
	CSI	N.A [1]	0 / 2	N.A	[1] Optional FFC connectors for MIPI-CSI on the mini module.
Audio	Soundwire	0 / 2	0 / 2	N.A	I2S pins may be used for one HDA port or two additional SoundWire ports for a total of up to four SoundWire ports.
	I2S	0 / 1	0 / 1	N.A	
Other Serial Ports	I2C	2 / 3	2 / 2	2 / 2	I2C0 and I2C1 for client and server modules. The mini module supports a third I2C port (I2C2/MDIO for SGMII PHY setup).
	SMBus	1 / 1	1 / 1	1 / 1	
	IPMB	N.A	0 / 1	0 / 1	
	UART	0 / 2	0 / 2	1 / 2	
GPIO	-		12 / 12	12 / 12	
Miscellaneous	Watchdog Timer	0 / 1	0 / 1	0 / 1	
	Fan (PWM and tachometer)	1 / 1	1 / 1	1 / 1	
FuSa	FuSa set of signals	0 / 1	0 / 1	0 / 1	
Power Rails	VCC	12 / 12	28 / 28	28 / 28	
	VCC_5V-SBY	N.A	0 / 2	0 / 2	The mini module does not have 5V standby pins.
	VCC_RTC	1 / 1	1 / 1	1 / 1	
	GND	All	All	All	All available GND pins shall be used.
Connector	J1	1 / 1	1 / 1	1 / 1	
	J2	N.A	0 / 1	1 / 1	

1.2 conga-HPC/EVAL-Client

The conga-HPC/EVAL-Client carrier board is designed for COM-HPC® Client Module Sizes A, B, and C.

The conga-HPC/EVAL-Client provides most of the functional requirements for any embedded PC application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB4, and Gigabit Ethernet. To ensure stable data throughput, the carrier board is equipped with high performance connectors in accordance with the COM-HPC® specification.

By combining the scalability of COM-HPC® Client Modules, the conga-HPC/EVAL-Client carrier board provides manufacturers and developers with a platform to jump-start the development of systems and applications based on COM-HPC® specification. This helps to reduce product design cycle and encourages rapid innovation in system design, to meet the ever-changing needs of the market.

The various features and capabilities offered by the conga-HPC/EVAL-Client carrier board makes it ideal for the integration of Client Module Sizes A, B, and C.

1.3 Order Number

Table 2 Order Description

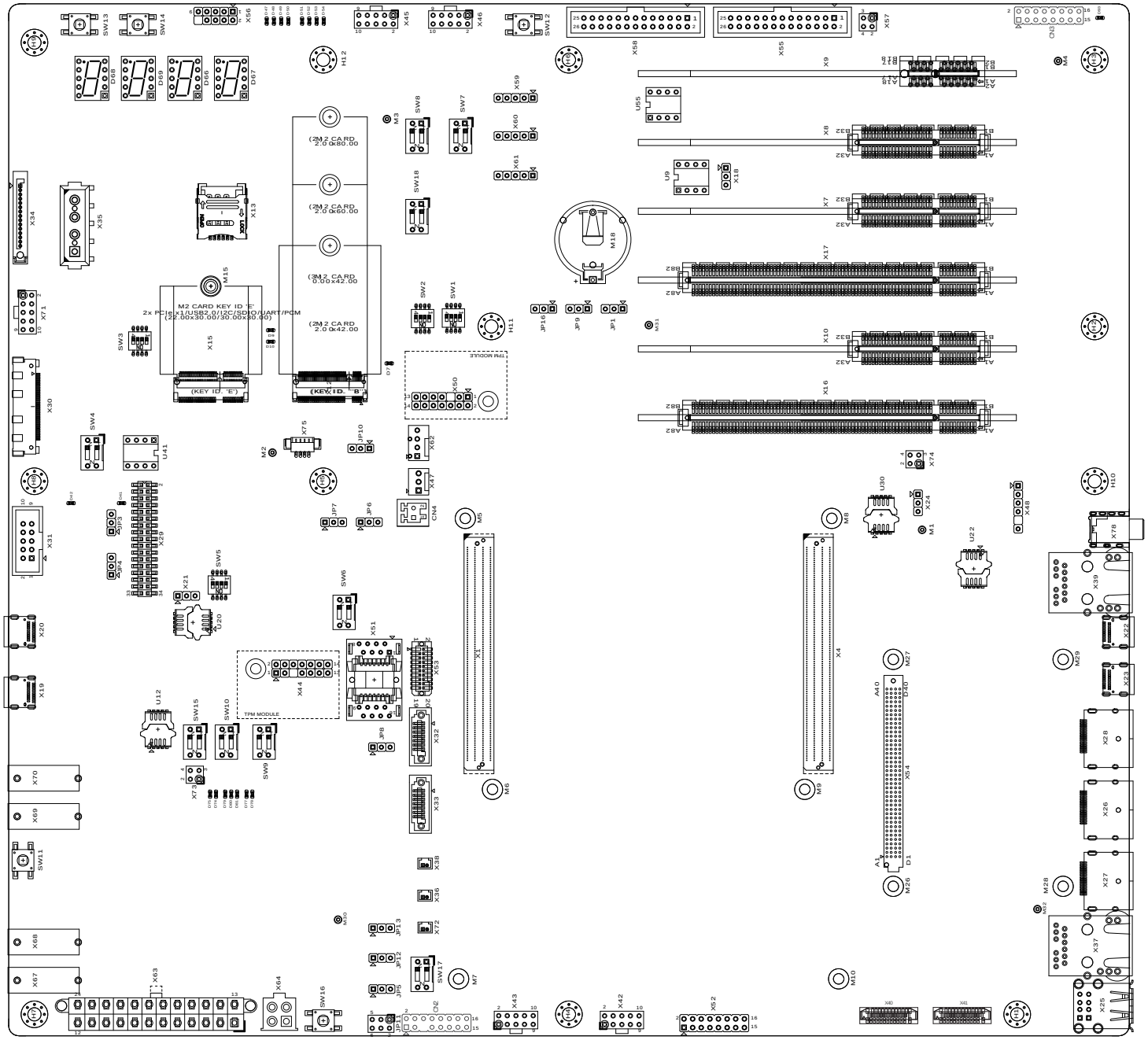
Part Number	Product Name	Description
065600	conga-HPC/EVAL-Client	Evaluation Carrier Board for COM-HPC® Client Size A, B, C Modules
065610	conga-HPC/EVAL-Client IO Shield	IO Shield Standard size for conga-HPC/EVAL-Client

2 Connector Layout

The connector layout picture shows each connector and its designator.

Hover over any component. When the mouse icon changes, click on the link to go to the area in the document where the component is described.

Use the mouse icon in the top left hand corner of the destination page to return to the connector layout picture.



3 Specifications

3.1 Feature List

Table 3 Feature Summary

Formfactor	Extended ATX	
Board Variant	Evaluation Carrier Board for COM-HPC® Client Type Modules (Sizes A, B, C)	
Internal Connectors and Features	1x PCIe Gen5 x16 1x PCIe Gen4 x16 3x PCIe Gen4 x4 BMC PCIe x1 2x USB4 M.2 Key B 2242 (USB2, 2x PCIe) M.2 Key E 2230 (USB2, 2x PCIe) two-lane KR connector to connect Mezzanine Cards for LAN options eDP DMIC header 2x MIPI CSI	2x SATA SATA Power Disk Drive Power 4x COM (2x via SIO) GPSPI header I2C header SMB header GPIO header Feature header System Fan CPU Fan
External Connectors	Dual USB 2 3x DP++ 2x 10GbE RJ45 2x USB4	
Postcode	4x 7-Segment Postcode LEDs connected to PD I2C	
Power Input	1x ATX standard power input 24pin 1x ATX12V power input 4pin 1x AT power input DC In 8-20Vmax (via 4x Banana jacks)	
Operating Temperature	Operating Temp.: 0°C … +60°C Storage Temp.: -20°C … +70°C	
Humidity	Operating Hum.: 10% … 90% r. H. non cond. Storage Hum.: 5% … 95% r. H. non cond.	
Size	304.8 x 330.2 mm (approx. 12 x 13 inches)	
Order Information	PN 065600 conga-HPC/EVAL-Client	

Note

The module must also support the features for them to function. Refer to the module's user's guide for information about supported features.

3.2 Mechanical Dimensions

- Size: 304.8 mm x 330.2 mm (approximately 12 x 13 inches)
- Height: approximately 43.0 mm (top side)

Note

3D models of congatec products are available at www.congatec.com/login. These models indicate the overall length, height and width of each product. If you need login access, contact your local sales representative.

3.3 Environmental Specifications

Temperature	Operation: 0°C to +60°C	Storage: -20°C to +70°C
Relative Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heat spreader, the maximum operating temperature refers to any measurable spot on the heat spreader's surface.

Humidity specifications are for non-condensing conditions.

4 Connectors and Features

Primary Carrier Connector P1 (X1)

Table 4 Connector P1 (X1) Pinout

Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A01	VCC	B01	VCC	C01	VCC	D01	VCC
A02	VCC	B02	PWRBTN#	C02	RSTBTN#	D02	VCC
A03	VCC	B03	VCC	C03	VCC	D03	VCC
A04	VCC	B04	THERMTRIP#	C04	CARRIER_HOT#	D04	VCC
A05	VCC	B05	VCC	C05	VCC	D05	VCC
A06	VCC	B06	TAMPER#	C06	VIN_PWR_OK	D06	VCC
A07	VCC	B07	VCC	C07	VCC	D07	VCC
A08	VCC	B08	SUS_S3#	C08	SUS_S4_S5#	D08	VCC
A09	VCC	B09	VCC	C09	VCC	D09	VCC
A10	GND	B10	WD_STROBE#	C10	GND	D10	WAKE0#
A11	BATLOW#	B11	WD_OUT	C11	FAN_PWMOUT	D11	WAKE1#
A12	PLTRST#	B12	GND	C12	FAN_TACHIN	D12	GND
A13	GND	B13	USB5-	C13	GND	D13	USB1-
A14	USB7-	B14	USB5+	C14	USB3-	D14	USB1+
A15	USB7+	B15	GND	C15	USB3+	D15	GND
A16	GND	B16	USB4-	C16	GND	D16	USB0-
A17	USB6-	B17	USB4+	C17	USB2-	D17	USB0+
A18	USB6+	B18	GND	C18	USB2+	D18	GND
A19	GND	B19	I2S_LRCLK/SNDW_CLK3/ HDA_SYNC	C19	GND	D19	DDI0_SDA_AUX-
A20	DDI1_SDA_AUX-	B20	I2S_DOUT/SNDW_DAT3/ HDA_SDO	C20	SNDW_DMIC_CLK1	D20	DDI0_SCL_AUX+
A21	DDI1_SCL_AUX+	B21	I2S_MCLK/HDA_RST#	C21	SNDW_DMIC_DAT1	D21	GND
A22	GND	B22	I2S_DIN/SNDW_DAT2/ HDA_SDI	C22	GND	D22	DDI0_PAIR0-
A23	DDI1_PAIR0-	B23	I2S_CLK/SNDW_CLK2/ HDA_BCLK	C23	SNDW_DMIC_CLK0	D23	DDI0_PAIR0+
A24	DDI1_PAIR0+	B24	VCC_5V_SBY	C24	SNDW_DMIC_DAT0	D24	GND
A25	GND	B25	USB67_OC#	C25	GND	D25	DDI0_PAIR1-
A26	DDI1_PAIR1-	B26	USB45_OC#	C26	DDI0_DDC_AUX_SEL	D26	DDI0_PAIR1+
A27	DDI1_PAIR1+	B27	USB23_OC#	C27	DDI1_DDC_AUX_SEL	D27	GND
A28	GND	B28	USB01_OC#	C28	DDI0_HPD	D28	DDI0_PAIR2-
A29	DDI1_PAIR2-	B29	SML1_CLK	C29	DDI1_HPD	D29	DDI0_PAIR2+
A30	DDI1_PAIR2+	B30	SML1_DAT	C30	eDP_HPD	D30	GND
A31	GND	B31	PMCALERT#	C31	eDP_VDD_EN	D31	DDI0_PAIR3-

A32	DDI1_PAIR3-	B32	SML0_CLK	C32	eDP_BKLT_EN	D32	DDI0_PAIR3+
A33	DDI1_PAIR3+	B33	SML0_DAT	C33	eDP_BKLTCTL	D33	GND
A34	GND	B34	USB_PD_ALERT#	C34	GND	D34	AC_PRESENT
A35	eDP_AUX-	B35	USB_PD_I2C_CLK	C35	USB1_AUX-	D35	RSVD
A36	eDP_AUX+	B36	USB_PD_I2C_DAT	C36	USB1_AUX+	D36	GND
A37	GND	B37	USB_RT_ENA	C37	GND	D37	USB1_SSTX0-
A38	eDP_TX0-	B38	USB1_LSRX	C38	USB1_SSRX0-	D38	USB1_SSTX0+
A39	eDP_TX0+	B39	USB1_LSTX	C39	USB1_SSRX0+	D39	GND
A40	GND	B40	USB0_LSRX	C40	GND	D40	USB1_SSTX1-
A41	eDP_TX1-	B41	USB0_LSTX	C41	USB1_SSRX1-	D41	USB1_SSTX1+
A42	eDP_TX1+	B42	GND	C42	USB1_SSRX1+	D42	GND
A43	GND	B43	USB0_AUX-	C43	GND	D43	USB0_SSTX0-
A44	eDP_TX2-	B44	USB0_AUX+	C44	USB0_SSRX0-	D44	USB0_SSTX0+
A45	eDP_TX2+	B45	LID#	C45	USB0_SSRX0+	D45	GND
A46	GND	B46	SLEEP#	C46	GND	D46	USB0_SSTX1-
A47	eDP_TX3-	B47	VCC_BOOT_SPI	C47	USB0_SSRX1-	D47	USB0_SSTX1+
A48	eDP_TX3+	B48	BOOT_SPI_CS#	C48	USB0_SSRX1+	D48	GND
A49	GND	B49	BSEL0	C49	GND	D49	SATA0_RX-
A50	eSPI_IO0	B50	BSEL1	C50	BOOT_SPI_IO0	D50	SATA0_RX+
A51	eSPI_IO1	B51	BSEL2	C51	BOOT_SPI_IO1	D51	GND
A52	eSPI_IO2	B52	eSPI_ALERT0#	C52	BOOT_SPI_IO2	D52	SATA0_TX-
A53	eSPI_IO3	B53	eSPI_ALERT1#	C53	BOOT_SPI_IO3	D53	SATA0_TX+
A54	eSPI_CLK	B54	eSPI_CS0#	C54	BOOT_SPI_CLK	D54	GND
A55	GND	B55	eSPI_CS1#	C55	GND	D55	SATA1_RX-
A56	PCIe_CLKREQ0_LO#	B56	eSPI_RST#	C56	PCIe_REFCLK0_HI-	D56	SATA1_RX+
A57	PCIe_CLKREQ0_HI#	B57	GND	C57	PCIe_REFCLK0_HI+	D57	GND
A58	GND	B58	PCIe_BMC_RX-	C58	GND	D58	SATA1_TX-
A59	PCIe_BMC_TX-	B59	PCIe_BMC_RX+	C59	PCIe_REFCLK0_LO-	D59	SATA1_TX+
A60	PCIe_BMC_TX+	B60	GND	C60	PCIe_REFCLK0_LO+	D60	GND
A61	GND	B61	PCIe08_RX-	C61	GND	D61	PCIe00_TX-
A62	PCIe08_TX-	B62	PCIe08_RX+	C62	PCIe00_RX-	D62	PCIe00_TX+
A63	PCIe08_TX+	B63	GND	C63	PCIe00_RX+	D63	GND
A64	GND	B64	PCIe09_RX-	C64	GND	D64	PCIe01_TX-
A65	PCIe09_TX-	B65	PCIe09_RX+	C65	PCIe01_RX-	D65	PCIe01_TX+
A66	PCIe09_TX+	B66	GND	C66	PCIe01_RX+	D66	GND
A67	GND	B67	PCIe10_RX-	C67	GND	D67	PCIe02_TX-
A68	PCIe10_TX-	B68	PCIe10_RX+	C68	PCIe02_RX-	D68	PCIe02_TX+
A69	PCIe10_TX+	B69	GND	C69	PCIe02_RX+	D69	GND
A70	GND	B70	PCIe11_RX-	C70	GND	D70	PCIe03_TX-

A71	PCIe11_TX-	B71	PCIe11_RX+	C71	PCIe03_RX-	D71	PCIe03_TX+
A72	PCIe11_TX+	B72	GND	C72	PCIe03_RX+	D72	GND
A73	GND	B73	PCIe12_RX-	C73	GND	D73	PCIe04_TX-
A74	PCIe12_TX-	B74	PCIe12_RX+	C74	PCIe04_RX-	D74	PCIe04_TX+
A75	PCIe12_TX+	B75	GND	C75	PCIe04_RX+	D75	GND
A76	GND	B76	PCIe13_RX-	C76	GND	D76	PCIe05_TX-
A77	PCIe13_TX-	B77	PCIe13_RX+	C77	PCIe05_RX-	D77	PCIe05_TX+
A78	PCIe13_TX+	B78	GND	C78	PCIe05_RX+	D78	GND
A79	GND	B79	PCIe14_RX-	C79	GND	D79	PCIe06_TX-
A80	PCIe14_TX-	B80	PCIe14_RX+	C80	PCIe06_RX-	D80	PCIe06_TX+
A81	PCIe14_TX+	B81	GND	C81	PCIe06_RX+	D81	GND
A82	GND	B82	PCIe15_RX-	C82	GND	D82	PCIe07_TX-
A83	PCIe15_TX-	B83	PCIe15_RX+	C83	PCIe07_RX-	D83	PCIe07_TX+
A84	PCIe15_TX+	B84	GND	C84	PCIe07_RX+	D84	GND
A85	GND	B85	TEST#	C85	GND	D85	NBASET0_MDI0-
A86	VCC_RTC	B86	RSMRST_OUT#	C86	SMB_CLK	D86	NBASET0_MDI0+
A87	SUS_CLK	B87	UART1_TX	C87	SMB_DAT	D87	GND
A88	GPIO_00	B88	UART1_RX	C88	SMB_ALERT#	D88	NBASET0_MDI1-
A89	GPIO_01	B89	UART1_RTS#	C89	UART0_TX	D89	NBASET0_MDI1+
A90	GPIO_02	B90	UART1_CTS#	C90	UART0_RX	D90	GND
A91	GPIO_03	B91	IPMB_CLK	C91	UART0_RTS#	D91	NBASET0_MDI2-
A92	GPIO_04	B92	IPMB_DAT	C92	UART0_CTS#	D92	NBASET0_MDI2+
A93	GPIO_05	B93	GP_SPI_MOSI	C93	I2C0_CLK	D93	GND
A94	GPIO_06	B94	GP_SPI_MISO	C94	I2C0_DAT	D94	NBASET0_MDI3-
A95	GPIO_07	B95	GP_SPI_CS0#	C95	I2C0_ALERT#	D95	NBASET0_MDI3+
A96	GPIO_08	B96	GP_SPI_CS1#	C96	I2C1_CLK	D96	GND
A97	GPIO_09	B97	GP_SPI_CS2#	C97	I2C1_DAT	D97	NBASET0_LINK_MAX#
A98	GPIO_10	B98	GP_SPI_CS3#	C98	NBASET0_SDP	D98	NBASET0_LINK_MID#
A99	GPIO_11	B99	GP_SPI_CLK	C99	NBASET0_CTREF	D99	NBASET0_LINK_ACT#
A100	TYPE0	B100	GP_SPI_ALERT#	C100	TYPE1	D100	TYPE2

Table 5 Connector P2 (X4) Pinout

Pin	Row E	Pin	Row F	Pin	Row G	Pin	Row H
E1	RAPID_SHUTDOWN	F1	FUSA_STATUS0	G1	VCC_5V_SBY	H1	GND
E2	GND	F2	FUSA_STATUS1	G2	GND	H2	USB2_SSTX0-
E3	DDI2_SDA_AUX-	F3	FUSA_ALERT#	G3	USB2_SSRX0-	H3	USB2_SSTX0+
E4	DDI2_SCL_AUX+	F4	FUSA_SPI_CS#	G4	USB2_SSRX0+	H4	GND
E5	GND	F5	FUSA_SPI_CLK	G5	GND	H5	USB2_SSTX1-
E6	DDI2_PAIR0-	F6	FUSA_SPI_MISO	G6	USB2_SSRX1-	H6	USB2_SSTX1+
E7	DDI2_PAIR0+	F7	FUSA_SPI_MOSI	G7	USB2_SSRX1+	H7	GND
E8	GND	F8	FUSA_SPI_ALERT	G8	GND	H8	USB3_SSTX0-
E9	DDI2_PAIR1-	F9	FUSA_VOLTAGE_ERR#	G9	USB3_SSRX0-	H9	USB3_SSTX0+
E10	DDI2_PAIR1+	F10	PROCHOT#	G10	USB3_SSRX0+	H10	GND
E11	GND	F11	CATERR#	G11	GND	H11	USB3_SSTX1-
E12	DDI2_PAIR2-	F12	RSVD	G12	USB3_SSRX1-	H12	USB3_SSTX1+
E13	DDI2_PAIR2+	F13	RSVD	G13	USB3_SSRX1+	H13	GND
E14	GND	F14	RSVD	G14	GND	H14	USB2_AUX-
E15	DDI2_PAIR3-	F15	RSVD	G15	USB3_LSRX	H15	USB2_AUX+
E16	DDI2_PAIR3+	F16	RSVD	G16	USB3_LSTX	H16	GND
E17	GND	F17	RSVD	G17	USB2_LSRX	H17	USB3_AUX-
E18	DDI2_DDC_AUX_SEL	F18	RSVD	G18	USB2_LSTX	H18	USB3_AUX+
E19	DDI2_HPD	F19	GND	G19	PEG_LANE_REV#	H19	GND
E20	GND	F20	PCIe32_RX-	G20	GND	H20	PCIe40_TX-
E21	PCIe32_TX-	F21	PCIe32_RX+	G21	PCIe40_RX-	H21	PCIe40_TX+
E22	PCIe32_TX+	F22	GND	G22	PCIe40_RX+	H22	GND
E23	GND	F23	PCIe33_RX-	G23	GND	H23	PCIe41_TX-
E24	PCIe33_TX-	F24	PCIe33_RX+	G24	PCIe41_RX-	H24	PCIe41_TX+
E25	PCIe33_TX+	F25	GND	G25	PCIe41_RX+	H25	GND
E26	GND	F26	PCIe34_RX-	G26	GND	H26	PCIe42_TX-
E27	PCIe34_TX-	F27	PCIe34_RX+	G27	PCIe42_RX-	H27	PCIe42_TX+
E28	PCIe34_TX+	F28	GND	G28	PCIe42_RX+	H28	GND
E29	GND	F29	PCIe35_RX-	G29	GND	H29	PCIe43_TX-
E30	PCIe35_TX-	F30	PCIe35_RX+	G30	PCIe43_RX-	H30	PCIe43_TX+
E31	PCIe35_TX+	F31	GND	G31	PCIe43_RX+	H31	GND
E32	GND	F32	PCIe36_RX-	G32	GND	H32	PCIe44_TX-
E33	PCIe36_TX-	F33	PCIe36_RX+	G33	PCIe44_RX-	H33	PCIe44_TX+
E34	PCIe36_TX+	F34	GND	G34	PCIe44_RX+	H34	GND
E35	GND	F35	PCIe37_RX-	G35	GND	H35	PCIe45_TX-
E36	PCIe37_TX-	F36	PCIe37_RX+	G36	PCIe45_RX-	H36	PCIe45_TX+
E37	PCIe37_TX+	F37	GND	G37	PCIe45_RX+	H37	GND

E38	GND	F38	PCIe38_RX-	G38	GND	H38	PCIe46_TX-
E39	PCIe38_TX-	F39	PCIe38_RX+	G39	PCIe46_RX-	H39	PCIe46_TX+
E40	PCIe38_TX+	F40	GND	G40	PCIe46_RX+	H40	GND
E41	GND	F41	PCIe39_RX-	G41	GND	H41	PCIe47_TX-
E42	PCIe39_TX-	F42	PCIe39_RX+	G42	PCIe47_RX-	H42	PCIe47_TX+
E43	PCIe39_TX+	F43	GND	G43	PCIe47_RX+	H43	GND
E44	GND	F44	PCIe16_RX-	G44	GND	H44	PCIe24_TX-
E45	PCIe16_TX-	F45	PCIe16_RX+	G45	PCIe24_RX-	H45	PCIe24_TX+
E46	PCIe16_TX+	F46	GND	G46	PCIe24_RX+	H46	GND
E47	GND	F47	PCIe17_RX-	G47	GND	H47	PCIe25_TX-
E48	PCIe17_TX-	F48	PCIe17_RX+	G48	PCIe25_RX-	H48	PCIe25_TX+
E49	PCIe17_TX+	F49	GND	G49	PCIe25_RX+	H49	GND
E50	GND	F50	PCIe18_RX-	G50	GND	H50	PCIe26_TX-
E51	PCIe18_TX-	F51	PCIe18_RX+	G51	PCIe26_RX-	H51	PCIe26_TX+
E52	PCIe18_TX+	F52	GND	G52	PCIe26_RX+	H52	GND
E53	GND	F53	PCIe19_RX-	G53	GND	H53	PCIe27_TX-
E54	PCIe19_TX-	F54	PCIe19_RX+	G54	PCIe27_RX-	H54	PCIe27_TX+
E55	PCIe19_TX+	F55	GND	G55	PCIe27_RX+	H55	GND
E56	GND	F56	PCIe20_RX-	G56	GND	H56	PCIe28_TX-
E57	PCIe20_TX-	F57	PCIe20_RX+	G57	PCIe28_RX-	H57	PCIe28_TX+
E58	PCIe20_TX+	F58	GND	G58	PCIe28_RX+	H58	GND
E59	GND	F59	PCIe21_RX-	G59	GND	H59	PCIe29_TX-
E60	PCIe21_TX-	F60	PCIe21_RX+	G60	PCIe29_RX-	H60	PCIe29_TX+
E61	PCIe21_TX+	F61	GND	G61	PCIe29_RX+	H61	GND
E62	GND	F62	PCIe22_RX-	G62	GND	H62	PCIe30_TX-
E63	PCIe22_TX-	F63	PCIe22_RX+	G63	PCIe30_RX-	H63	PCIe30_TX+
E64	PCIe22_TX+	F64	GND	G64	PCIe30_RX+	H64	GND
E65	GND	F65	PCIe23_RX-	G65	GND	H65	PCIe31_TX-
E66	PCIe23_TX-	F66	PCIe23_RX+	G66	PCIe31_RX-	H66	PCIe31_TX+
E67	PCIe23_TX+	F67	GND	G67	PCIe31_RX+	H67	GND
E68	GND	F68	RSVD	G68	GND	H68	RSVD
E69	RSVD	F69	RSVD	G69	RSVD	H69	RSVD
E70	RSVD	F70	GND	G70	RSVD	H70	GND
E71	RSVD	F71	NBASET1_MDI0-	G71	GND	H71	CSI1_RX0-
E72	RSVD	F72	NBASET1_MDI0+	G72	CSI0_RX0-	H72	CSI1_RX0+
E73	RSVD	F73	GND	G73	CSI0_RX0+	H73	GND
E74	RSVD	F74	NBASET1_MDI1-	G74	GND	H74	CSI1_RX1-
E75	RSVD	F75	NBASET1_MDI1+	G75	CSI0_RX1-	H75	CSI1_RX1+
E76	RSVD	F76	GND	G76	CSI0_RX1+	H76	GND
E77	RSVD	F77	NBASET1_MDI2-	G77	GND	H77	CSI1_RX2-
E78	NBASET1_CTREF	F78	NBASET1_MDI2+	G78	CSI0_RX2-	H78	CSI1_RX2+

E79	NBASET1_SDP	F79	GND	G79	CSI0_RX2+	H79	GND
E80	NBASET1_LINK_MID#	F80	NBASET1_MDI3-	G80	GND	H80	CSI1_RX3-
E81	NBASET1_LINK_ACT#	F81	NBASET1_MDI3+	G81	CSI0_RX3-	H81	CSI1_RX3+
E82	NBASET1_LINK_MAX#	F82	GND	G82	CSI0_RX3+	H82	GND
E83	GND	F83	RSVD	G83	GND	H83	CSI1_CLK-
E84	RSVD	F84	RSVD	G84	CSI0_CLK-	H84	CSI1_CLK+
E85	RSVD	F85	GND	G85	CSI0_CLK+	H85	GND
E86	GND	F86	ETH0_TX-	G86	GND	H86	CSI1_I2C_CLK
E87	ETH0_RX-	F87	ETH0_TX+	G87	CSI0_I2C_CLK	H87	CSI1_I2C_DAT
E88	ETH0_RX+	F88	GND	G88	CSI0_I2C_DAT	H88	CSI1_MCLK
E89	GND	F89	ETH1_TX-	G89	CSI0_MCLK	H89	CSI1_RST#
E90	ETH1_RX-	F90	ETH1_TX+	G90	CSI0_RST#	H90	CSI1_ENA
E91	ETH1_RX+	F91	GND	G91	CSI0_ENA	H91	GND
E92	GND	F92	PCIe_REFCLK2-	G92	GND	H92	PCIe_REFCLKIN0-
E93	PCIe_REFCLK1-	F93	PCIe_REFCLK2+	G93	RSVD	H93	PCIe_REFCLKIN0+
E94	PCIe_REFCLK1+	F94	GND	G94	RSVD	H94	GND
E95	GND	F95	RSVD	G95	GND	H95	PCIe_REFCLKIN1-
E96	PCIe_CLKREQ1#	F96	ETH0-1_PRSNT#	G96	ETH0-1_I2C_CLK	H96	PCIe_REFCLKIN1+
E97	PCIe_CLKREQ2#	F97	ETH0-1_PHY_RST#	G97	ETH0-1_I2C_DAT	H97	GND
E98	PCIe_CLKREQ_OUT0#	F98	ETH0_SDP	G98	ETH0-1_PHY_INT#	H98	ETH0-1_MDIO_CLK
E99	PCIe_CLKREQ_OUT1#	F99	ETH1_SDP	G99	ETH0-1_INT#	H99	ETH0-1_MDIO_DAT
E100	PCIe_PERST_IN0#	F100	PCIe_PERST_IN1#	G100	PCIe_WAKE_OUT0#	H100	PCIe_WAKE_OUT1#

4.1 Power Supply Connectors

The conga-HPC/EVAL-Client provides the following power supply connectors:

- standard 24-pin ATX power connector (X63)
- additional 4-pin ATX12V power connector (X64)
- 8-21 Vmax DC banana jacks (X67, X68, X69, and X70)

To enable the 5V standby power circuit when no module is connected, set DIP switch 10.2 to ON.

SW10

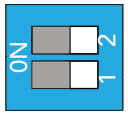


Table 6 SW10.2 - 5V Standby Without Module

Setting	Configuration
OFF	5V Standby Without Module Disabled (default)
ON	5V Standby Without Module Enabled

Note

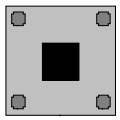
1. *Do not supply power via the DC banana jacks and the ATX connectors at the same time.*
2. *In ATX mode, power must be supplied to the 24-pin ATX (X63) and the 4-pin ATX12V (X64) power connectors.*
3. *In ATX mode, the 3.3 V, 5 V, and 12 V are derived from the ATX power supply. If power is supplied via the DC banana jacks, the onboard DC/DC regulators generate the 3.3 V, 5 V and 12 V. The onboard buck-boost converter generates the 12 V from 8-21 Vmax.*

4.1.1 ATX Power Connectors

The conga-HPC/EVAL-Client provides a standard 24-pin ATX power connector (X63) and 4-pin ATX12V power connector (X64) for an ATX power supply. Power must be supplied to both connectors.

With an ATX power supply, the COM-HPC® module starts after you press the power-on button SW11 (ATX mode).

SW11

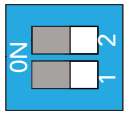


For AT mode, set DIP switch SW15.1 to ON. In this mode, the PS_ON# signal from the power supply is active. Therefore, the module starts immediately after power is connected to the system.

Table 7 SW15.1 - ATX/AT PSU Settings

Setting	Configuration
OFF	ATX mode (default)
ON	AT mode

SW15

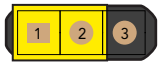


Jumper JP13 can be used to disconnect the 5 V standby voltage from the whole system.

Table 8 JP13 - ATX 5V Standby Settings

Pin	Description
1-2	5V standby connected (default)
2-3	5V standby disconnected

JP13



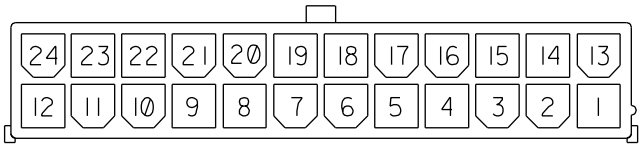
Connector Type

JP13: 2.54 mm, 2-pin jumper

Table 9 X63 - 24-Pin ATX Power Pinout

Pin	Signal	Description	Pin	Signal	Description
1	+3.3V	Power supply +3.3 VDC	13	+3.3V	Power supply +3.3 VDC
2	+3.3V	Power supply +3.3 VDC	14	-12V	Power supply -12 VDC
3	GND	Power ground	15	GND	Power ground
4	+5V	Power supply +5 VDC	16	PS_ON#	Power Supply On (active low). Short this pin to GND to switch power supply ON; disconnect from GND to switch OFF.
5	GND	Power ground	17	GND	Power ground
6	+5V	Power supply +5 VDC	18	GND	Power ground
7	GND	Power ground	19	GND	Power ground
8	VIN_ PWR_OK	Power Ok	20	N.C	
9	5V_SB	Standby power supply +5 VDC	21	+5V	Power supply +5 VDC
10	+12V	Power supply +12 VDC	22	+5V	Power supply +5 VDC
11	+12V	Power supply +12 VDC	23	+5V	Power supply +5 VDC
12	+3.3V	Power supply +3.3 VDC	24	GND	Power ground

X63



Connector Type

X63: Standard 24-pin ATX Power connector

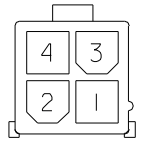
Note

The -12 V power output of the ATX power supply is not used.

Table 10 X64 - 4-Pin ATX12V Power Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Power ground	2	GND	Power ground
3	+12V	Power supply +12 VDC	4	+12V	Power supply +12 VDC

X64



Connector Type

X64: Standard 4-pin ATX12V Power connector

4.1.2 DC Banana Jacks

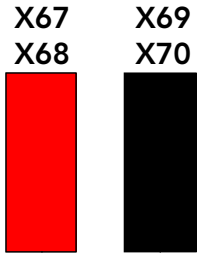
The conga-HPC/EVAL-Client provides four banana jacks (X67, X68, X69, X70) for a DC power supply to power both the module and the voltage regulators on the carrier board. The maximum power rating per banana jack is 16 A. Depending on the power requirements of the system, use one or two pairs of banana jacks to power the system. Although the carrier board is designed for the input voltage range of 8-21 Vmax, the input voltage range is defined by the module. For more information, see section 4.1.7 “Module Type Detection”.

Caution

Do not exceed the voltage rating of the COM-HPC® module. Doing so will damage the module.

Table 11 X67, X68, X69, X70 - DC Banana Jacks Pinout

Connector	Description
X67, X68	Input voltage for module and carrier board (usually +12 V)
X69, X70	Ground



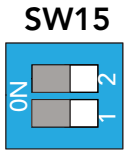
Connector Type

X67, X68, X69, X70: 4 mm diameter banana plug (max. 16 A)

The onboard buck-boost converter that generates 12 V from 8-21 Vmax in AT mode can be disabled via DIP switch SW15.2.

Table 12 SW15.2 - Buck-Boost Converter Settings

Setting	Description
OFF	Enabled (default)
ON	Disabled



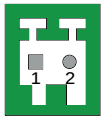
4.1.3 Power Sense Connector

The conga-HPC/EVAL-Client provides a power sense connector (CN4) to monitor the main input power rail (VCC) of the module.

Table 13 CN4 - Power Sense Connector

Pin	Description
1	VCC (Main power rail)
2	Ground

CN4



Connector Type

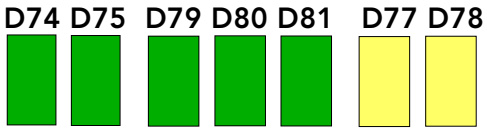
CN4: Phoenix Contact 1881558 with 2-positions; Possible mating connector Phoenix Contact 1881325

4.1.4 Power States LEDs

The LEDs D74-D75 and D77-D81 indicate the different power states of the conga-HPC/EVAL-Client as described in the table below.

Table 14 Power LEDs Status

LED	Status	Description
All	Off	No power applied.
All	On	ATX power supply is fully switched on, with stable 3.3 V, 5 V and 12 V. (D77 is off in AT mode)
D74	On	The green LED indicates the status of SUS_S4#
D75	On	The green LED indicates the status of SUS_S3#
D77	On	The yellow LED indicates that 5V standby power is applied to the conga-HPC/EVAL-Client. If only D77 lights, it indicates that the ATX power supply is mechanically switched on and only 5 V standby power is applied to the conga-HPC/EVAL-Client.
D78	On	The yellow LED indicates that the onboard 3.3 V standby power is present
D79	On	The green LED indicates that 12 V main power is present
D80	On	The green LED indicates that 5 V main power is present
D81	On	The green LED indicates that the onboard 3.3 V main power is present



4.1.5 VIN_PWR_OK Signal

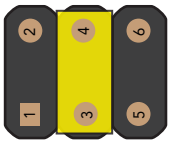
The VIN_PWR_OK signal is a high-active input from the main power supply to the module. It indicates whether the power is good.

Use jumper JP11 to configure the VIN_PWR_OK signal.

Table 15 JP11 - VIN_PWR_OK Signal Settings

Pin	Description
1 - 2	Add 3.3V pull-up to VIN_PWR_OK signal (for debug purposes)
3 - 4	Connect VIN_PWR_OK signal from ATX power supply (default)
5 - 6	Connect VIN_PWR_OK signal from onboard DC/DC regulator (only in single 12 V mode)

JP11



Connector Type

JP11: 2.54 mm, 2-pin jumper

4.1.6 Power-Up Control

The module's SUS_S3# signal controls the ATX power supply control signal (PS_ON#). When the system goes to Suspend to RAM (S3) or Soft Off (S5), the module's chipset asserts the SUS_S3# signal. Through the use of an inverter, the low active PS_ON# signal goes high and switches off the ATX power supply.

When the system is in a power-down system state, any system wake-up event invokes the chipset of the module to deassert the SUS_S3# signal. With the deassertion, the system transitions to Full-On state (S0).

4.1.7 Module Type Detection

The signals TYPE0, TYPE1, and TYPE2 indicate the pinout type of the module connected to the carrier board. These pins are either open (NC) or strapped to ground (GND) by the module as shown in the table below.

Table 16 Module Type Detection Pinout Description

TYPE2	TYPE1	TYPE0	Meaning
NC	NC	NC	Reserved
NC	NC	GND	Reserved
NC	GND	NC	Reserved
NC	GND	GND	Server Module - Fixed 12V Input
GND	NC	NC	Reserved
GND	NC	GND	Reserved
GND	GND	NC	Client Module - Wide Range 8V to 20V input
GND	GND	GND	Client Module - Fixed 12V input

Note

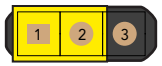
If the conga-HPC/EVAL-Client detects an incompatible module pinout, an onboard logic prevents the board from powering up the whole system by controlling the PS_ON# signal of the ATX power supply. Only works in ATX mode. AT mode does not support this feature.

Jumper JP12 can be used to manually set the TYPE0 signal to NC (Client Module 8-20V).

Table 17 JP12 - TYPE0 Signal Settings

Pin	Description
1-2	Check module TYPE0 signal
2-3	NC (Client Module 8-20V) (default)

JP12



Connector Type

JP12: 2.54 mm, 2-pin jumper

4.2 CMOS Battery Holder

The conga-HPC/EVAL-Client provides battery holder M18 for a CR2032 battery. The battery supplies power to the RTC and CMOS memory.

Warning

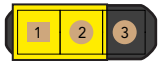
Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Jumper JP9 can be used to disconnect the battery.

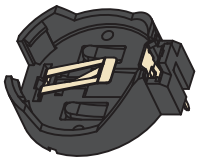
Table 18 JP9 - Battery Settings

Pin	Description
1 - 2	Connect battery (default)
2 - 3	Disconnect the battery

JP9



M18



Connector Type

JP9: 2.54 mm, 2-pin jumper

M18: CR2032 battery

4.3 PCIe Connectors

The conga-HPC/EVAL-Client provides the PCIe® connectors listed in the table below:

Table 19 Required Module PCIe® Link Configurations

Connector	PCIe x4 (X7)				PCIe x4 (X10)				PCIe x4 (X8)				M.2 B (X12)		M.2 E (X15)		PCIe x16 (X16)				PCIe x16 (X17)			
Lane	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	...	31	32	33	...	47
Link	x4				x4				x4				x2		x2		x16				x16			
Gen	4								4				3				5				4			

Note

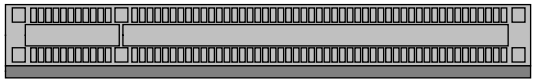
For each connector you require, check the user's guide of your module for the supported link configurations and configure the respective PCIe® lanes of your module as highlighted above.

4.3.1 PCIe x16 Slots

The conga-HPC/EVAL-Client provides two standard PCIe® x16 slots:

- PCIe® lanes [16:31] on connector X16 (PEG Port)
- PCIe® lanes [32:47] on connector X17

X16, X17



Connector Type

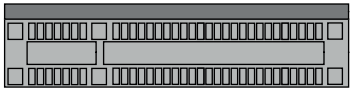
X16, X17: PCIe® x16 card

4.3.2 PCIe x4 Slots

The conga-HPC/EVAL-Client provides three standard PCIe® x4 slots:

- PCIe® lanes [0:3] on connector X7
- PCIe® lanes [4:7] on connector X10
- PCIe® lanes [8:11] on connector X8

X7, X8, X10



Note

The PCIe® lanes [8:11] on connector X8 are routed through a PCIe® Gen4 compatible retimer on the conga-HPC/EVAL-Client.

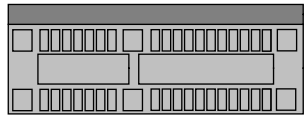
Connector Type

X7, X8, X10: PCIe® x4 card

4.3.3 PCIe BMC Slot

The conga-HPC/EVAL-Client provides a standard PCIe® x1 slot (X9) dedicated for a Board Management Controller (BMC) card.

X9



Connector Type

X9: PCIe® BMC Card

4.3.4 M.2 Key B + micro-SIM Card Slot

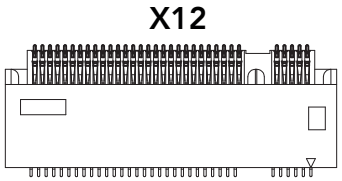
The conga-HPC/EVAL-Client provides a standard M.2 Key B socket X12. The socket is routed to the module's PCIe® lanes [12:13] and USB Port 6. LED D7 lights red when there is activity on this socket.

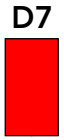
The UIM interface of the M.2 Key B socket is connected to micro-SIM card slot X13.

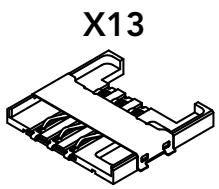
Connector Type

X12: M.2 Key B card size 3042, 2242, 2260, 2280

X13: micro-SIM card

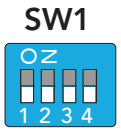






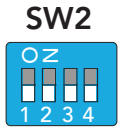
Use DIP SW1 and SW2 to configure the M.2 Key B settings as described in the two tables below.

Table 20 SW1 - M.2 Key B Settings



Switch	Configuration	Description
SW1.1	OFF	Disconnect M.2 SMB_ALERT# (default)
	ON	Connect M.2 SMB_ALERT#
SW1.2	OFF	Disconnect WOWWAN# (default)
	ON	Connect WOWWAN#
SW1.3	OFF	Connect M.2 SMB_DAT/CLK (default)
	ON	Disconnect M.2 SMB_DAT/CLK
SW1.4	OFF	Deactive M.2 full card power-off control
	ON	Activate M.2 full card power-off control

Table 21 SW2 - M.2 Key B Settings

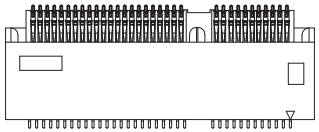


Switch	Configuration	Description
SW2.2	OFF	Deactivate M.2 reset control (default)
	ON	Activate M.2 reset control
SW2.3	OFF	Deactivate M.2 WDIS2# control - wireless 2 (default)
	ON	Activate M.2 WDIS2# control
SW2.4	OFF	Deactivate M.2 WDIS1# control - wireless 1 (default)
	ON	Activate M.2 WDIS1# control

4.3.5 M.2 Key E

The conga-HPC/EVAL-Client provides a standard M.2 Key E socket X15. The socket is routed to the module's PCIe® lanes [14:15], USB Port 7, and UART1 port. LED D9 is connected to the LED2# signal of the M.2 Key E socket. LED D10 is connected to the LED1# signal of the M.2 Key E socket.

X15



D9, D10

Connector Type

X15: M.2 Key E card size 2230

The clock request signal (PCIe_CLKREQ0_HI#) can be permanently enabled via jumper JP16 for:

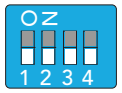
- PCIe® x4 slot (X8)
- M.2 Key B (X12)
- M.2 Key E (X15)

Use DIP SW3 to configure the M.2 Key E settings as described in the table below.

Table 22 SW3 - M.2 Key E Control

Switch	Configuration	Description
SW3.1	OFF	Deactivate M.2 WDIS1# control - wireless 1 (default)
	ON	Activate M.2 WDIS1# control
SW3.2	OFF	Deactivate M.2 WDIS2# control - wireless 2 (default)
	ON	Activate M.2 WDIS2# control
SW3.3	OFF	Deactivate UART (default)
	ON	Activate UART

SW3



Note

The UART signals are shared with the UART1 signals on connector X43 and X55. For more information, see section 4.14.2.4 "Module Serial Port 1" and section 4.17 "Feature Connector".

4.3.6 PCIe Clock Request Signals

The clock request signal (PCIe_CLKREQ0_LO#) can be permanently enabled via jumper JP1 for:

- PCIe® x4 slots (X7, X10)
- PCIe® BMC slot (X9)

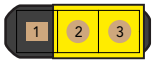
The clock request signal (PCIe_CLKREQ0_HI#) can be permanently enabled via jumper JP16 for:

- PCIe® x4 slot (X8)
- M.2 Key B (X12)
- M.2 Key E (X15)

Table 23 JP1, JP16 - PCIe® Clock Request Signal Settings

Pin	Description
1 - 2	Enable permanently
2 - 3	Enable (default)

JP1, JP16



Connector Type

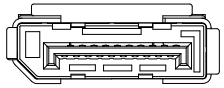
JP1, JP16: 2.54 mm, 2-pin jumper

4.4 Display Interfaces

4.4.1 DP++

The conga-HPC/EVAL-Client provides three DP++ ports (X26, X27, and X28). The three DP++ ports are routed through a DisplayPort re-driver to support HBR3 data rate (up to 12 Gbps).

X26, X27, X28



Connector Type

X26, X27, X28: Standard DP plug

4.4.2 eDP/LVDS

The conga-HPC/EVAL-Client connects the module's eDP/LVDS interface to:

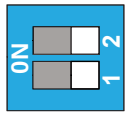
- eDP panel on connector X30
- LVDS panel on connector X29

Use DIP SW4.1 to select eDP or LVDS functionality.

Table 24 SW4.1 - eDP/LVDS Settings

Setting	Description
OFF	eDP (default)
ON	LVDS

SW4



Note

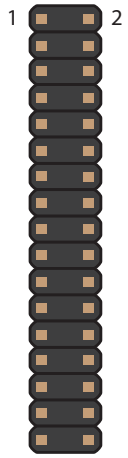
LVDS is currently not supported (hardware revision A.x).

4.4.2.1 LVDS

Table 25 X29 - LVDS Pinout

Pin	Signal	Pin	Signal
1	LVDS_DDC_DAT	2	LVDS_DDC_CLK
3	N.C	4	N.C
5	GND	6	LVDS0_D0-
7	LVDS0_D0+	8	LCD0_VDD_EN
9	LVDS0_D1-	10	LVDS0_D1+
11	LCD0_BKLTEN	12	LVDS0_D2+
13	LVDS0_D2-	14	NC
15	LVDS0_CLK-	16	LVDS0_CLK+
17	NC	18	LVDS0_D3+
19	LVDS0_D3-	20	GND
21	LVDS1_D0-	22	LVDS1_D0+
23	GND	24	LVDS1_D1-
25	LVDS1_D1+	26	GND
27	LVDS1_D2-	28	LVDS1_D2+
29	GND	30	LVDS1_CLK+
31	LVDS1_CLK	32	NC
33	LVDS1_D3+	34	LVDS1_D3-

X29



Connector Type

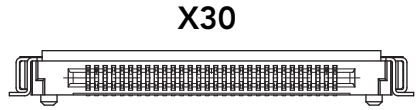
X29: 2 mm, 2x17 pin female connector

Note

LVDS is currently not supported (hardware revision A.x).

4.4.2.2 eDP

Table 26 X30 - eDP Pinout



Pin	Signal	Pin	Signal
1	N.C.	21	PANEL_PWR
2	GND	22	N.C.
3	eDP_TX3-	23	GND
4	eDP_TX3+	24	GND
5	GND	25	GND
6	eDP_TX2-	26	GND
7	eDP_TX2+	27	eDP_HPD
8	GND	28	GND
9	eDP_TX1-	29	GND
10	eDP_TX1+	30	GND
11	GND	31	GND
12	eDP_TX0-	32	eDP_LVDS_BKLT_EN
13	eDP_TX0+	33	eDP_LVDS_BKLT_CTRL
14	GND	34	N.C.
15	eDP]_AUX+	35	N.C.
16	eDP_AUX-	36	N.C
17	GND	37	BKLT_PWR
18	PANEL_PWR	38	BKLT_PWR
19	PANEL_PWR	39	BKLT_PWR
20	PANEL_PWR	40	N.C.

Connector Type

X30: 0.5 mm, 40 Pos. (ACES 50203-04001-001 or compatible)

Note

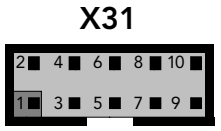
For eDP functionality, set DIP SW4.1 to OFF.

4.4.2.3 eDP Panel and Backlight Power Supply

The power supply for eDP panels and backlight inverter is available on connector X31. LED D41 lights red when power for the flat panel is on. LED D42 lights red when power for the backlight is on.

Table 27 X31 - eDP Power Pinout

Pin	Signal	Pin	Signal
1	VDD_LFP (Switched by EDP_VDD_EN)	2	VDD_BKLT (Switched by EDP_BLKT_EN)
3	+5V (2.0 A fuse)	4	+12V (1.5 A fuse)
5	EDP_VDD_EN	6	EDP_BKLT_EN
7	N.C	8	EDP_BKLT_CTRL_R
9	GND	10	GND



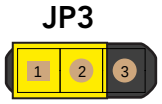
Connector Type

X31: 2.54 mm, 2x5 pin female connector

4.4.2.4 Flat Panel and Backlight Voltage Selection

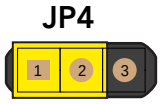
The conga-HPC/EVAL-Client supports different voltages for the panel and backlight. Follow the descriptions in the tables below to set the panel and backlight voltages.

Table 28 JP3 - Flat Panel Voltage Settings



Pin	Description
1-2	5 V panel power (default)
2-3	3.3 V panel power

Table 29 JP4 - Backlight Voltage Settings



Pin	Description
1-2	12 V backlight Power (default)
2-3	5 V backlight Power

Connector Type

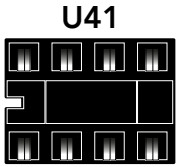
JP3, JP4: 2.54 mm grid jumper

4.4.2.5 Flat Panel Configuration Data

The LVDS panel configuration data can be stored in EEPROM U41.

Connector Type

U41: EEPROM in 8-pin DIL package



4.5 Universal Serial Bus (USB)

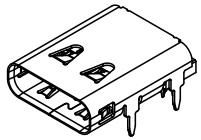
The conga-HPC/EVAL-Client provides the following USB connectors:

- four USB Type-C
  - port 0 on connector X19
  - port 1 on connector X20
  - port 2 on connector X22
  - port 3 on connector X23
- two USB 2.0 Type-A (dual-stacked)
  - ports 4 and 5 on connector X25
- USB 2.0 @ M.2 Key B
  - port 6 on connector X12
- USB 2.0 @ M.2 Key E
  - port 7 on connector X15

4.5.1 USB Type-C Ports

The conga-HPC/EVAL-Client provides four USB Type-C ports (X19, X20, X22, X23). Each port can support up to USB 40Gbps (depending on the module) and USB Power Delivery (PD) up to 5V @ 3A.

X19, X20, X22, X23



Each port is connected to one of four onboard Intel® JHL9040RIT Thunderbolt™ 4 re-timers. Each re-timer can be programmed via the SML0 pins of the COM-HPC® connector.

Each port is connected to one of two onboard USB PD controllers (TI TPS65994BH). The firmware of each USB PD controller is stored in a separate EEPROM (U20, U30). The socketed EEPROM can be programmed externally with an EEPROM programmer. Alternatively, each EEPROM can be programmed via one of two onboard I2C headers (X21, X24) or an onboard Aardvark connector (X71).

The table below provides an overview of the relevant USB Type-C devices, interfaces and addresses:

Table 30 USB Type-C Port Devices, Interfaces and Addresses

	Port 0	Port 1	Port 2	Port 3
USB Type-C Connector	X19	X20	X22	X23
USB PD Controller:				
- EEPROM Socket	U20		U30	
- Programming Header	X21		X24	
- SML1 Address	0x21	0x25	0x20	0x24
Thunderbolt Re-Timer:				
- SML0 Address (7-bit)	55	56	57	58

Connector Type

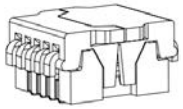
X19, X20, X22, X23: USB Type-C plug

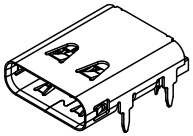
4.5.1.1 USB Type-C Ports 0/1

The USB Type-C and USB PD controller for ports 0/1 (X19, X20) can be programmer via header X21. The firmware is stored in EEPROM U20.

Table 31 X21 - Programming Header for USB PD Controller Ports 0/1

Pin	Description
1	I2C3m_SDA
2	GND
3	I2C3m_SCL

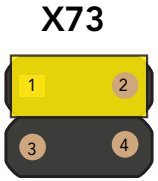




Use jumper X73 to disconnect PMCALERT# from the COM-HPC® connector for the USB Type-C and USB PD controller of ports 0/1.

Table 32 X73 - PMCALERT# USB PD X19/X20 Setting

Pin	Description
1-2	PMCALERT# connected to COM-HPC (default)
3-4	PMCALERT# disconnected



Connector Type

X21: 3-pin, 2.54 mm grid female header

U20: SOIC-8, 1.8 V to 5.5 V, 256K I2C Serial EEPROM

X73: 2.54 mm grid jumper

4.5.1.2 USB Type-C Ports 2/3

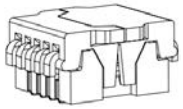
The USB Type-C and USB PD controller for ports 2/3 (X22, X23) can be programmer via header X21. The firmware is stored in EEPROM U20.

Table 33 X24 - Programming Header for USB PD Controller Ports 2/3

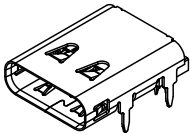
Pin	Description
1	I2C3m_SDA
2	GND
3	I2C3m_SCL

X24

U30



X22, X23

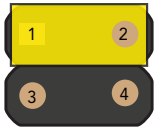


Use jumper X74 to disconnect PMCALERT# from the COM-HPC® connector for the USB Type-C and USB PD controller of ports 2/3.

Table 34 X74 - PMCALERT# USB PD Ports 2/3

Pin	Description
1-2	PMCALERT# connected to COM-HPC (default)
3-4	PMCALERT# disconnected

X74



Connector Type

X24: 3-pin, 2.54 mm grid female header

U30: SOIC-8, 1.8 V to 5.5 V, 256K I2C Serial EEPROM

X74: 2.54 mm grid jumper

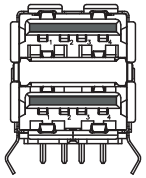
4.5.2 Dual Stacked USB 2.0 Type-A Ports

The conga-HPC/EVAL-Client provides two USB 2.0 ports via a dual-stacked USB Type-A connector (X25). Each port provides up to 1.7 A.

Connector Type

X25: USB Type-A plug

X25

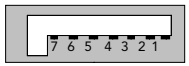


4.6 SATA

The conga-HPC/EVAL-Client provides two standard SATA connectors (X32, X33):

- SATA0 port on connector X32
- SATA1 port on connector X33

X32, X33



Connector Type

X32, X33: Standard SATA plug

4.6.1 Disk Drive Power Connector

The conga-HPC/EVAL-Client provides connector X35, a 4-pin connector for powering disk drives.

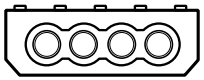
Caution

Do not connect more than one device to connector X35. Otherwise, the device may get damaged.

Table 35 X35 - Disk Drive Power Pinout

Pin	Description
1	12 V (1.5 A fuse; resettable; shared with X34)
2	GND
3	GND
4	5 V (2 A fuse; resettable; shared with X34)

X35



Connector Type

X35: Standard 4-pin disk drive power plug

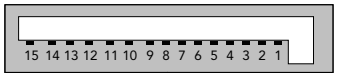
4.6.2 SATA Power

The conga-HPC/EVAL-Client provides a standard 15-pin SATA power connector (X34).

Table 36 X34 - SATA Power Pinout

Pin	Signal
1, 2, 3	3.3 V (2 A fuse; resettable)
4, 5, 6	GND
7, 8, 9	5 V (2 A fuse; resettable; shared with X35)
10, 11, 12	GND
13, 14, 15	12 V (1.5 A fuse; resettable; shared with X35)

X34



Connector Type

X34: Standard 15-pin SATA power connector

4.7 Ethernet Ports

The conga-HPC/EVAL-Client provides RJ45 ethernet ports X37 and X39. The NBASE-T Ethernet Controller [0:1] Software-Definable Pins (SDP) NBASET[0:1]_SDP are provided on pin headers X36 and X38:

- NBASET0 port on connector X37
  - NBASET0_SDP on connector X36
- NBASET1 port on connector X39
  - NBASET1_SDP on connector X38

The SDP pins can also be used for IEEE1588 support (e.g. 1PPS signal).

Table 37 X37, X39 - Ethernet Status LEDs Description

Color (LED)	Description
Green (right LED)	Link activity
Off (left bicolor LED)	100 Mbit
Green (left bicolor LED)	Half speed (Module specific)
Yellow (left bicolor LED)	Full speed (Module specific)

X37, X39

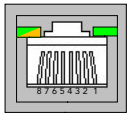


Table 38 X36 - NBASET0_SDP Header Pinout

Pin	Description
1	NBASET0_SDP signal
2	Ground

X36, X38

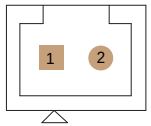


Table 39 X38 - NBASET1_SDP Header Pinout

Pin	Description
1	NBASET1_SDP signal
2	Ground

Connector Type

X37, X39: RJ45 plug

X36, X38: 1.25 mm, 2-pin female connector

Note

The silkscreen on the conga-HPC/EVAL-Client Rev. X.x and A.x incorrectly states ETH0/1 instead of NBASET0/1 for the ethernet ports.

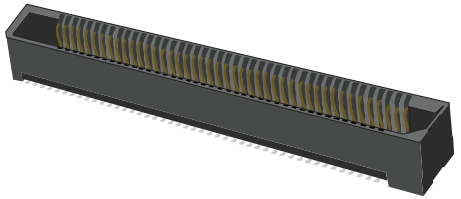
4.8 Ethernet Mezzanine Card Connector

The conga-HPC/EVAL-Client provides connector X54 for an Ethernet Mezzanine card.

Table 40 X54 - Ethernet Mezzanine Card Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	GND	B1	ETH0_RX0P	C1	GND	D1	GND
A2	GND	B2	ETH0_RX0N	C2	GND	D2	ETH0_SDP
A3	ETH0_TX0P	B3	GND	C3	NC	D3	GND
A4	ETH0_TX0N	B4	GND	C4	NC	D4	ETH0-1_INT
A5	GND	B5	ETH1_RX0P	C5	GND	D5	GND
A6	GND	B6	ETH1_RX0N	C6	GND	D6	ETH1_SDP
A7	ETH1_TX0P	B7	GND	C7	NC	D7	GND
A8	ETH1_TX0N	B8	GND	C8	NC	D8	ETH0-1_I2C_DAT
A9	GND	B9	NC	C9	GND	D9	ETH0-1_I2C_CLK
A10	GND	B10	NC	C10	GND	D10	NC

X54



A11	NC	B11	GND	C11	NC	D11	GND
A12	NC	B12	GND	C12	NC	D12	ETH0-1_MDIO_DAT
A13	GND	B13	NC	C13	GND	D13	ETH0-1_MDIO_CLK
A14	GND	B14	NC	C14	GND	D14	NC
A15	NC	B15	GND	C15	NC	D15	ETH0-1_PHY_INT#
A16	NC	B16	GND	C16	NC	D16	ETH0-1_PHY_RST#
A17	GND	B17	NC	C17	GND	D17	ETH0-1_PRSNT#
A18	GND	B18	NC	C18	GND	D18	NC
A19	NC	B19	GND	C19	NC	D19	GND
A20	NC	B20	GND	C20	NC	D20	NC
A21	GND	B21	NC	C21	GND	D21	GND
A22	GND	B22	NC	C22	GND	D22	NC
A23	NC	B23	GND	C23	NC	D23	GND
A24	NC	B24	GND	C24	NC	D24	NC
A25	GND	B25	NC	C25	GND	D25	NC
A26	GND	B26	NC	C26	GND	D26	NC
A27	NC	B27	GND	C27	NC	D27	GND
A28	NC	B28	GND	C28	NC	D28	NC
A29	GND	B29	NC	C29	GND	D29	NC
A30	GND	B30	NC	C30	GND	D30	NC
A31	NC	B31	GND	C31	NC	D31	NC
A32	NC	B32	GND	C32	NC	D32	NC
A33	GND	B33	NC	C33	NC	D33	GND
A34	GND	B34	NC	C34	NC	D34	NC
A35	GND	B35	GND	C35	GND	D35	GND
A36	GND	B36	GND	C36	GND	D36	GND
A37	GND	B37	GND	C37	GND	D37	GND
A38	+V12S	B38	+V12S	C38	+V12S	D38	+V12S
A39	+V12S	B39	+V12S	C39	+V12S	D39	+V12S
A40	+V12S	B40	+V12S	C40	+V12S	D40	+V12S

Connector Type

X54: Ethernet Mezzanine Card

4.9 Audio Interfaces

The conga-HPC/EVAL-Client features the following audio interfaces:

- Audio Jack (4-pole) on connector X78
- Connector X50 for an external I²S or SoundWire® codec
- DMIC signals on connector X48

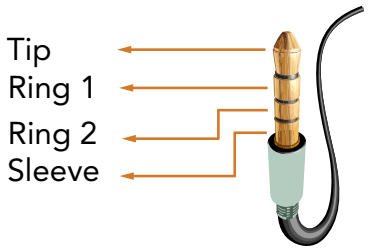
4.9.1 Audio Jack (4-Pole)

The conga-HPC/EVAL-Client features a 4-pole audio jack (X78) for a 3.5 mm CTIA standard plug. The audio signals are provided by an onboard TSI 92HD91B HDA codec. This codec can be disabled via DIP switch 18.1.

Table 41 X78 - Audio Jack Pinout

Pin	Jack	Signal	Description
1	Tip	LINE_L	Line-OUT - left channel
2	Ring 1	LINE_R	Line-OUT - right channel
3	Ring 2	A_GND	Analog ground
4	Sleeve	MIC	Microphone

Audio Jack Plug



Connector Type

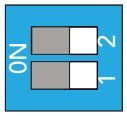
X78: 3.5 mm, 4-pole CTIA standard plug

The onboard codec can be disabled via DIP switch SW18.1.

Table 42 SW18.1 - Disable Onboard Audio Codec

Setting	Description
OFF	Enabled audio codec (default)
ON	Disabled audio codec

SW18



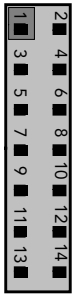
4.9.2 I²S/SoundWire

The conga-HPC/EVAL-Client features header X50 to connect a card with an external I²S or SoundWire® codec.

Table 43 X50 - I²S/SoundWire Header Pinout

Pin	Signal	Pin	Signal
1	GND	2	HDA_SYNC_HDR
3	CODECSET_HDR	4	HDA_BITCLK_HDR
5	NC	6	HDA_SDIN0_HDR
7	CB_RESET#	8	HDA_SDOUT_HDR
9	+V3.3 Standby (fused)	10	HDA_RST#_HDR
11	NC	12	SNDW_DAT0
13	NC	14	SNDW_CLK0

X50



Connector Type

X50: 2.54 mm, 2x7pin female connector

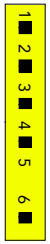
4.9.3 DMIC

The conga-HPC/EVAL-Client features DMIC signals on connector X48.

Table 44 X48 - DMIC Header Pinout

Pin	Signal
1	+V1.8 (0.75 A fused)
2	DMIC_DAT
3	GND
4	DMIC_CLK
5	Key
6	NC

X48



Connector Type

X48: 2.54 mm, 6-pin female connector

4.10 I²C Buses

The COM-HPC® Specification defines two general purpose I²C buses (I2C[0:1).

I2C0 Bus

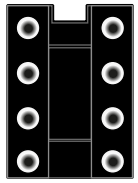
The conga-HPC/EVAL-Client provides the I2C0 signals on connector X52 and X59. For more information, see section 4.23 “I2C I/O Expander Pin Header” and section 4.19 “I2C0 Pin Header”.

The conga-HPC/EVAL-Client provides an EEPROM 24C32 on the 8-pin DIL socket U55 for test purposes during system development. This EEPROM is connected to the I2C0 bus and has the I²C address 0xAE. Use the I²C control commands implemented in the congatec CGOS API driver to access the EEPROM. For more information, refer to the CGOS manual and the user’s guide of the COM-HPC® module.

I2C1 Bus

The conga-HPC/EVAL-Client provides the I2C1 signals on connector X50 and X60. For more information, see section section 4.9.2 “I²S/ SoundWire” and section 4.20 “I2C1 Pin Header”.

U55



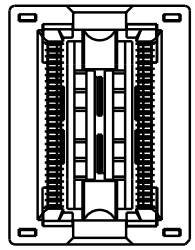
Connector Type

U55: 2-wire 3.3 V Serial EEPROMS in 8-pin DIL package

4.11 SPI Flash Socket

The conga-HPC/EVAL-Client provides a 16-pin SOIC16 socket (X51) for an SPI flash.

X51



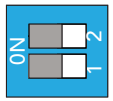
Connector Type

X51: SPI flash in 16-pin SOIC16 package

The boot select pins BSEL[2:0] are routed to DIP SW9 and SW10:

- BSEL0 to DIP SW9.1
- BSEL1 to DIP SW9.2
- BSEL2 to DIP SW10

SW9, SW10



For the BIOS select options via these DP switches, refer to the table below.

Table 45 BIOS Select Options

BSEL [2:0]	Chipset eSPI1_CS1# (If Available on chipset)	Chipset eSPI_CS2# (If Available on chipset)	Chipset SPI_CS0#	Chipset SPI_CS1#	Chipset eSPI0_CS0#	Boot Option	Use Case	Boot Option and CS# Routing Details
111	Carrier J1.B54 COM-HPC eSPI_CS0#	Carrier J1.B55 COM-HPC eSPI_CS1#	Module	Module	Module	MAFS on Module	Most Common Usage	CSME / DT on Chipset SPI0 device on Module BIOS on SPI0 or SPI1 on Module
						SAFS on Module	Module EC/MMC with SAFS BIOS on far side of EC/MMC	CSME / DT on Slave Attached Flash on Module BIOS on Module SAFS
110	Carrier J1.B54	Carrier J1.B55	Carrier J1.B48	Module	Module	MAFS on Carrier	Casino Gaming Removable BIOS option on Carrier	CSME / DT on Chipset SPI0 device on Carrier BIOS on SPI0 on Carrier or on SPI1 on Module
101	Carrier J1.B54	Carrier J1.B55	Module	Carrier J1.B48	Module	MAFS on Module	Casino Gaming Removable BIOS option on Carrier Alternate version	CSME / DT on Chipset SPIO device on Module BIOS on SPI0 on Module or on SP1 on Carrier
011	Module	Carrier J1.B55	Module	Module	Carrier J1.B54 COM-HPC eSPI_CS0#	MAFS on Module	Same as 111 except eSPI_CS routing	CSME / DT on Chipset SPI0 device on Module BIOS on SPI0 or SPI1 on Module
010	Module	Carrier J1.B55	Module	Module	Carrier J1.B54	SAFS on Carrier	BIOS totally under Carrier BMC control	CSME / DT on Carrier SAFS BIOS on Carrier SAFS
001	Module	Carrier J1.B55	Module	Module	Carrier J1.B54	MAFS on Module and SAFS on Carrier	BIOS mostly under Carrier BMC control	CSME / DT on Chipset SPI0 device on Module BIOS on Carrier SAFS

Note

For the conga-HPC/EVAL-Client, the most common BSEL[2:0] settings are 111 and 110. Use DIP SW9.1 to switch between these two options.

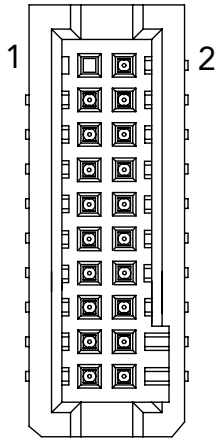
4.12 Intel ISP Adaptor-C2 Connector

The conga-HPC/EVAL-Client provides connector X53 for an Intel ISP Adaptor-C2.

Table 46 X53 - Intel ISP Adaptor-C2 Connector Pinout

Pin	Signal	Pin	Signal
1	Key	2	BOOT_SPI_CS0#
3	DEBUG_RST#	4	NC
5	GND	6	VCC_BOOT_SPI
7	SPI_CLK_ISP	8	SPI_IO2_ISP
9	SPI_IO3_ISP	10	SPI_IO1_ISP
11	NC	12	SPI_IO0_ISP
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	PLTRST#	20	NC

X53

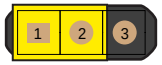


Use jumper JP8 to select the DEBUG_RST# trigger signal of the connector X53.

Table 47 JP8 - Debug Reset Trigger Signal Settings

Pin	Description
1-2	SYS_RST# (default)
2-3	VIN_PWR_OK#

JP8



Connector Type

X53: 1.27 mm, 2x10 pin female connector (For a matching connector, see www.dediprog.com/product/ISP-ADP-INTEL-C2)

JP8: 2.54 mm grid jumper

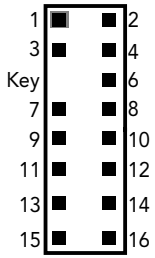
4.13 General Purpose SPI Port

The conga-HPC/EVAL-Client provides a general purpose SPI port (CN2).

Table 48 CN2 - General Purpose SPI Port Pinout

Pin	Signals	Pin	Signals
1	GND	2	GP_SPI_CS0#
3	GP_SPI_CLK	4	NC
5	KEY	6	NC
7	SPI_RST#	8	GP_SPI_MISO
9	+V3.3S	10	GP_SPI_MOSI
11	SPI_RST# (PLTRST#)	12	GP_SPI_CS1#
13	+V3.3A	14	GP_SPI_ALERT#
15	GP_SPI_CS2#	16	GP_SPI_CS3#

CN2



Connector Type

CN2: 2.54 mm, 2x8 pin female connector

4.14 eSPI

On the conga-HPC/EVAL-Client, the module's eSPI interface is routed to a Super I/O controller (Nuvoton NCT6122D).

The Super I/O controller provides the following interfaces:

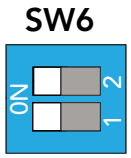
- One eSPI header (X44)
- Two serial ports (X45 and X46)
- One 3-pin system fan header (X47)

The Super I/O controller also provides eSPI based Port 80 information via eight LEDs. For more information, see section 5.4 "Debug LEDs".

DIP SW6.1 can be used to disable the Super I/O.

Table 49 SW6.1 - Super I/O Settings

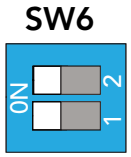
Setting	Description
ON	Enable Super I/O (default)
OFF	Disable Super I/O



Use DIP SW6.2 to select eSPI_CS0# or eSPI_CSI1# for the Super I/O.

Table 50 SW6.2 - ESPI_CSI[0:1]# Settings

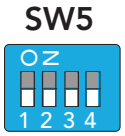
Setting	Description
ON	Selects eSPI_CS0# for Super I/O
OFF	Selects eSPI_CS1# for Super I/O (default)



Use DIP SW5 to configure the Super I/O.

Table 51 SW5 - Super I/O Settings

Switch	Configuration	Description
SW5.1	OFF	Configuration IO address 2Eh (default)
	ON	Configuration IO address 4Eh
SW5.2	OFF	Super IO key selection 87h (default)
	ON	Super IO key selection 88h
SW5.3	OFF	Disables Super IO Port 80 control (default)
	ON	Enables Super IO Port 80 control
SW5.4	OFF	Enable Port 80 to UART Serial Output (default)
	ON	Disable Port 80 to UART Serial Output

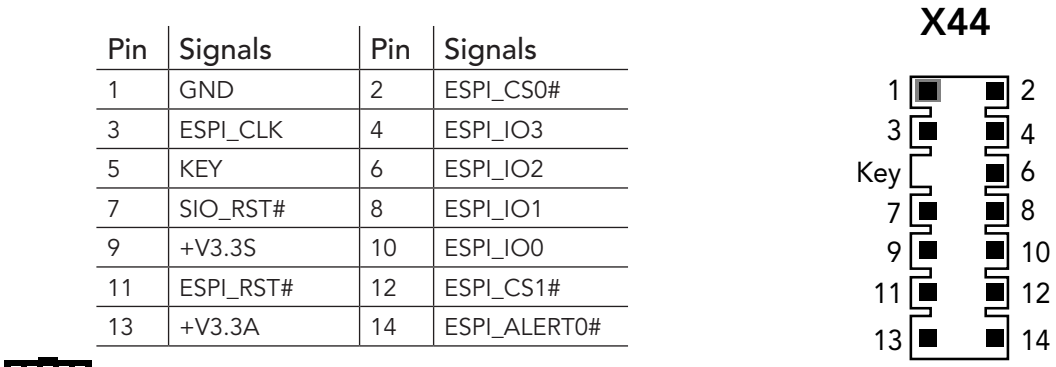


4.14.1 eSPI Header

The conga-HPC/EVAL-Client provides eSPI signals on header X44.

Table 52 X44 - eSPI Header Pinout

Pin	Signals	Pin	Signals
1	GND	2	ESPI_CS0#
3	ESPI_CLK	4	ESPI_IO3
5	KEY	6	ESPI_IO2
7	SIO_RST#	8	ESPI_IO1
9	+V3.3S	10	ESPI_IO0
11	ESPI_RST#	12	ESPI_CS1#
13	+V3.3A	14	ESPI_ALERT0#



Connector Type

X44: 2.54 mm, 2x7 pin female connector

4.14.2 Serial Ports

The conga-HPC/EVAL-Client supports up to four serial ports:

- Super I/O COM port 0 (RS-232/422/485) on connector X46
- Super I/O COM port 1 (RS-232) on connector X45
- Module UART0 on connector X42
- Module UART1 on connector X43

4.14.2.1 COM Port 0 Header

The conga-HPC/EVAL-Client provides COM port 0 on connector X46 via the onboard Super I/O. The port supports RS-232, RS-422 and RS-485 I/O voltage levels.

Use DIP SW7 and SW8 to configure the functionality of the COM port 0 transceiver.

Table 53 SW7 - COM Port 0 Transceiver Settings

SW 1	SW 2	Description
OFF	OFF	Loopback
ON	OFF	RS-232
OFF	ON	RS-485 half duplex
ON	ON	RS-485/RS-422 full duplex

SW7

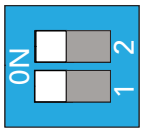


Table 54 SW8 - COM Port 0 Transceiver Settings

Switch	Configuration	Description
SW8.1	OFF	1 Mbps SLEW
	ON	250 kbps SLEW LIMITING (for EMI)
SW8.2	OFF	RS-485/422 Termination disabled
	ON	RS-485/422 Termination enabled

SW8

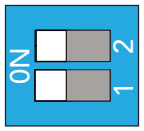
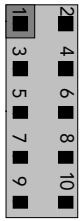


Table 55 X46 - COM 0 Pinout

Pin	Signals	Pin	Signals
1	DCD#	2	DSR
3	RX	4	RTS#
5	TX	6	CTS#
7	DTR#	8	RI#
9	GND	10	+5V (750mA fuse)

X46



Connector Type

X46: 2.54 mm, 2x5 pin female connector

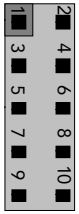
4.14.2.2 COM Port 1 Header

The conga-HPC/EVAL-Client provides COM port 1 on connector X45 via the onboard Super I/O.

Table 56 X45 - COM 1 Header Pinout

Pin	Signals	Pin	Signals
1	DCD#	2	DSR
3	RX	4	RTS#
5	TX	6	CTS#
7	DTR#	8	RI#
9	GND	10	+5V (750 mA fuse)

X45



Connector Type

X45: 2.54 mm, 2x5 pin female connector

Note

This port supports RS-232 I/O voltage levels only.

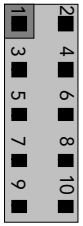
4.14.2.3 Module Serial Port 0

The conga-HPC/EVAL-Client provides the module's serial port 0 (UART0) on header X42. UART0 is also connected to pins 19 and 21 of the feature connector X55. For more information, see section 4.17 "Feature Connector".

Table 57 X42 - UART0 Pinout

Pin	Signals	Pin	Signals
1	NC	2	NC
3	RX	4	RTS#
5	TX	6	CTS#
7	NC	8	NC
9	GND	10	+5V (750 mA fuse)

X42

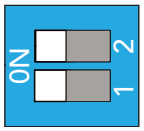


Use DIP SW17.1 to disable UART0.

Table 58 SW17.1 - Disable UART0

Setting	Description
ON	Disable UART0
OFF	Enable UART0 (default)

SW17

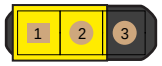


Use jumper JP5 to power the UART0 and UART1 RS-232 transmitter/receiver via +3.3 V runtime or standby power.

Table 59 JP5 - UART0 and UART1 Power Settings

Pin	Description
1-2	3.3 V runtime (default)
2-3	3.3 V standby

JP5



Connector Type

X42: 2.54 mm, 2x5 pin female connector

JP5: 2.54 mm grid jumper

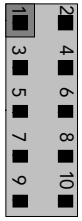
4.14.2.4 Module Serial Port 1

The conga-HPC/EVAL-Client provides the module's serial port 1 (UART1) on header X43. UART1 is also connected to the M.2 key E slot X15 and feature connector X55. For more information, see section 4.3.5 "M.2 Key E" and section 4.17 "Feature Connector".

Table 60 X43 - UART1 Pinout

Pin	Signals	Pin	Signals
1	NC	2	NC
3	RX	4	RTS#
5	TX	6	CTS#
7	NC	8	NC
9	GND	10	+5V (750 mA fuse)

X43

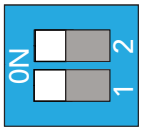


Use DIP SW17.2 to disable UART1.

Table 61 SW17.2 - Disable UART1

Setting	Description
ON	Disable UART1
OFF	Enable UART1 (default)

SW17

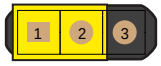


Use jumper JP5 to power the UART0 and UART1 RS-232 transmitter/receiver via +3.3 V runtime or standby power.

Table 62 JP5 - UART0 and UART1 Power Settings

Pin	Configuration
1-2	3.3 V runtime (default)
2-3	3.3 V standby

JP5



Connector Type

X43: 2.54 mm, 2x5 pin female connector

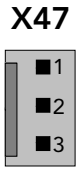
JP5: 2.54 mm grid jumper

4.14.3 System Fan Header

The conga-HPC/EVAL-Client provides a 3-pin fan connector X47 via the Super I/O controller.

Table 63 X47 - SYS Fan Pinout

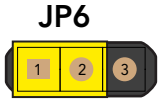
Pin	Signal
1	GND
2	+VDD (12V/5V)
3	Sense



Use jumper JP6 to set the fan's supply voltage level.

Table 64 JP6 - Fan Voltage Settings

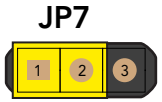
Pin	Description
1-2	12 V supply voltage for auxiliary fan (default)
2-3	5 V supply voltage for auxiliary fan



Use jumper JP7 to select the fan's control source.

Table 65 JP7 - Fan Speed Settings

Pin	Description
1-2	Fan speed control via Super I/O located on the conga-HPC/EVAL-Client (default)
2-3	Fan speed control via the COM-HPC® module
Open	Full fan speed if the pins are left open



Connector Type

X47: 2.54 mm, 3-pin fan plug

JP6, JP7: 2.54 mm grid jumper

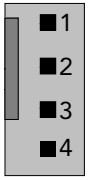
4.15 CPU Fan Header

The conga-HPC/EVAL-Client provides two different 4-pin fan connectors X62 and X75 that share the same signals.

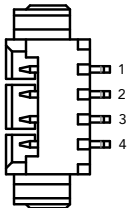
Table 66 X62 and X75 - CPU Fan Header Pinout

Pin	Signal
1	GND
2	+VDD (12V/5V)
3	Sense
4	Control

X62



X75

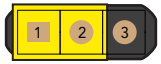


Use jumper JP10 to set the fan's supply voltage level.

Table 67 JP10 - CPU Fan Voltage Control

Pin	Configuration
1-2	12 V supply voltage (default)
2-3	5 V supply voltage

JP10



Connector Type

X62: 2.54 mm, standard 4-pin fan plug
X75: 1.25 mm, PicoBlade 4-pin fan plug (Molex 53261-0471); Possible Mating Connector: Molex 51021-0400
JP10: 2.54 mm grid jumper

4.16 Debug Header

The conga-HPC/EVAL-Client provides pin header X57 for measuring or debugging PCIE_WAKE# and PLTRST# signals.

Table 68 X57 - Debug Header Pinout

Pin	Signal	Pin	Signal
1	PLTRST#	2	GND
3	PCIE_WAKE#	4	GND

X57

Connector Type

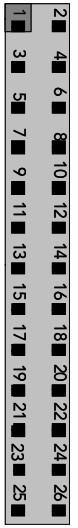
X57: 2.54 mm, 2x2 pin female connector

4.17 Feature Connector

Table 69 X55 - Feature Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	+V5S	5V main supply (0.75 A fuse)	2	+V5A	5V standby supply (0.75 A fuse)
3	SUS_CLK	32.768 kHz +/- 100 ppm clock used by Carrier peripherals such as M.2 cards in their low power modes.	4	RAPID_ SHUTDOWN	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs. Pull-down / disable on Module if RAPID_SHUTDOWN pin is not asserted.
5	TAMPER#	Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a Tamper event.	6	SUS_S4_S5#	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.
7	PS_ON#	Power supply on (active low).	8	CARRIER_HOT#	Input from off -Module temp sensor indicating an over-temp situation.
9	SUS_S3#	Suspend to RAM state. Active low output.	10	LID#	Module input signal, generation a LID close or open event.
11	THERMTRIP#	Active low output indicating that the CPU has entered thermal shutdown.	12	WAKE1#	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.
13	WD_OUT	Output indicating that a watchdog time-out event has occurred.	14	PEG_LANE_ REV#	PCI Express Graphics lane reversal input strap.
15	WDTRIG#	Watchdog Trigger	16	VIN_PWR_OK#	Power OK from main power supply. A high value indicates that the power is good.
17	BATLOW#	Indicates that external battery is low.	18	SLEEP#	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.
19	UART0_TX	COM module's serial port 0 transmit line	20	UART1_TX	COM module's serial port 1 transmit line
21	UART0_RX	COM module's serial port 0 receive line	22	UART1_RX	COM module's serial port 1 receive line
23	TEST#	Module input for vendor specific module test mode(s).	24	AC_PRESENT	Driven hard low on Carrier if system AC power is not present.
25	GND	Power ground	26	GND	Power ground

X55



Connector Type

X55: 2.54 mm, 2x13 pin female connector

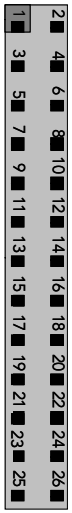
4.18 GPIO Pin Header

The conga-HPC/EVAL-Client provides 12 GPIO pins on header X58.

Table 70 X58 - GPIO Header Pinout

Pin	Signal	Pin	Signal
1	+V3.3 standby (0.75 A fuse)	2	+V3.3 main (0.75 A fuse)
3	GPIO_00	4	GND
5	GPIO_01	6	GND
7	GPIO_02	8	GND
9	GPIO_03	10	GND
11	GPIO_04	12	GND
13	GPIO_05	14	GND
15	GPIO_06	16	GND
17	GPIO_07	18	GND
19	GPIO_08	20	GND
21	GPIO_09	22	GND
23	GPIO_10	24	GND
25	GPIO_11	26	GND

X58



Connector Type

X58: 2.54 mm, 2x13 pin female connector

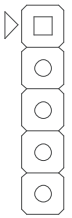
4.19 I2C0 Pin Header

The conga-HPC/EVAL-Client provides I2C0 pins on header X59. I2C0 is defined to operate with **3.3 V.**

Table 71 X59 - I2C0 Pin Header Pinout

Pin	Signal
1	+V3.3 standby (0.75 A fuse)
2	I2C0_DAT
3	I2C0_CLK
4	I2C0_ALERT#
5	GND

X59



Connector Type

X59: 2.54 mm, 5-pin female connector

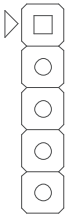
4.20 I2C1 Pin Header

The conga-HPC/EVAL-Client provides I2C1 pins on header X60. I2C1 is defined to operate with **1.8 V**.

Table 72 X60 - I2C1 Pin Header Pinout

Pin	Signal
1	+V1.8 standby (0.75 A fuse)
2	I2C1_DAT
3	I2C1_CLK
4	+V1.8 standby
5	GND

X60



Connector Type

X60: 2.54 mm, 5-pin female connector

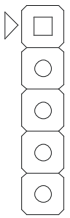
4.21 SMBus Pin Header

The conga-HPC/EVAL-Client provides SMBus pins on header X61.

Table 73 X61 - SMBus Header Pinout

Pin	Signal
1	+V3.3 standby (0.75 A fuse)
2	SMB_DAT
3	SMB_CLK
4	SMB_ALERT#
5	GND

X61



Connector Type

X61: 2.54 mm, 5-pin female connector

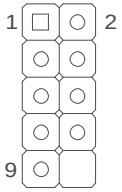
4.22 Front Panel Pin Header

The conga-HPC/EVAL-Client provides front panel pins on header X56.

Table 74 X56 - Front Panel Pin Header Pinout

Pin	Signal	Pin	Signal
1	NC	2	+V5
3	NC	4	GND
5	GND	6	PWRBTN#
7	RSTBTN#	8	GND
9	NC	10	No pin

X59



Connector Type

X56: 2.54 mm, 2x5 pin female connector

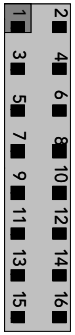
4.23 I2C I/O Expander Pin Header

The conga-HPC/EVAL-Client provides eight I²C pins on header X52 via an I/O expander (TI PCA9554). The I/O expander is connected to I2C0.

Table 75 X52 - I2C Header Pinout

Pin	Signal	Pin	Signal
1	I2C_IOE_B0	2	GND
3	I2C_IOE_B1	4	GND
5	I2C_IOE_B2	6	GND
7	I2C_IOE_B3	8	GND
9	I2C_IOE_B4	10	GND
11	I2C_IOE_B5	12	GND
13	I2C_IOE_B6	14	GND
15	I2C_IOE_B7	16	GND

X52



Connector Type

X52: 2.54 mm, 2x8 pin female connector

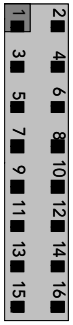
4.24 FuSa Header

The conga-HPC/EVAL-Client provides FuSa pins on header CN3. LED D7 is connected to CATERR#, indicating a catastrophic error occured.

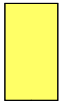
Table 76 CN3 - FuSa Header Pinout

Pin	Signal	Pin	Signal
1	+3.3V (Resettable Fuse)	2	FUSA_SPI_MISO
3	FUSA_STATUS0	4	FUSA_SPI_MOSI
5	FUSA_STATUS1	6	FUSA_SPI_ALERT
7	FUSA_ALERT#	8	FUSA_VOLTAGE_ERR#
9	FUSA_SPI_CS#	10	PROCHOT#
11	FUSA_SPI_CLK	12	CATERR#
13	NC	14	NC
15	GND	16	GND

CN3



D93



Connector Type

CN3: 2.54 mm, 2x8 pin female connector

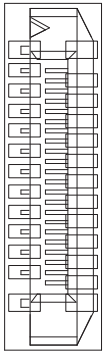
4.25 CSI Port 0

The conga-HPC/EVAL-Client provides Cameria Serial Interface (CSI) port 0 on connector X40.

Table 77 X40 - CSI Port 0 Pinout

Pin	Signal
1	+V3.3 Standby
2	+V3.3 Standby
3	CSI0_RX0P
4	CSI0_RX0N
5	GND
6	CSI0_RX1P
7	CSI0_RX1N
8	GND
9	CSI0_RX2P
10	CSI0_RX2N
11	CSI0_RST#
12	CSI0_RX3P
13	CSI0_RX3N
14	GND
15	CSI0_CLKP
16	CSI0_CLKN
17	GND
18	CSI0_I2C_CLK
19	CSI0_I2C_DAT
20	CSI0_ENA
21	CSI0_MCLK
22	NC

X40



Connector Type

X40: 22-pin flexible flat cable, 0.5 mm pitch

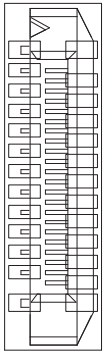
4.26 CSI Port 1

The conga-HPC/EVAL-Client provides Cameria Serial Interface (CSI) port 1 on connector X41.

Table 78 X41 - CSI Port 1 Pinout

Pin	Signal
1	+V3.3 Standby
2	+V3.3 Standby
3	CSI1_RX0P
4	CSI1_RX0N
5	GND
6	CSI1_RX1P
7	CSI1_RX1N
8	GND
9	CSI1_RX2P
10	CSI1_RX2N
11	CSI1_RST#
12	CSI1_RX3P
13	CSI1_RX3N
14	GND
15	CSI1_CLKP
16	CSI1_CLKN
17	GND
18	CSI1_I2C_CLK
19	CSI1_I2C_DAT
20	CSI1_ENA
21	CSI1_MCLK
22	NC

X41



Connector Type

X41: 22-pin flexible flat cable, 0.5 mm pitch

5 Additional Features

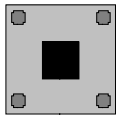
5.1 Buttons

The conga-HPC/EVAL-Client features power, reset, LID and sleep buttons.

5.1.1 Power

When you press the power button SW11, it triggers the module's PWRBTN# signal. The triggered event usually initiates a transition from one power state to another (for example, from S5 to S0). However, the system's behavior depends on the ACPI settings of the Operating System.

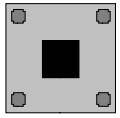
SW11



5.1.2 Reset

When you press the reset button SW12, it triggers the module's RSTBTN# signal. The triggered event usually invokes a system warm reset. This behavior however depends on the configuration of the module.

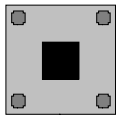
SW12



5.1.3 LID

When you press the lid button SW13, it triggers the module's LID# signal. The system's behavior depends on the ACPI settings of the Operating System.

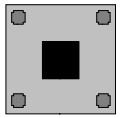
SW13



5.1.4 Sleep

When you press the sleep button SW14, it triggers the module's SLEEP# signal. The system's behavior depends on the ACPI settings of the Operating System.

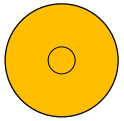
SW14



5.2 Ground Test Points

The conga-HPC/EVAL-Client provides 13 test points (M1-M10 and M30-M32). These test points are connected to ground and they make it easier to connect oscilloscope probes or multimeter lines or both to ground during measurements.

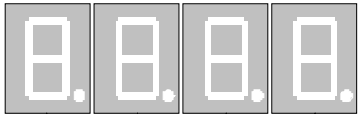
M1-M10
M30-M32



5.3 Debug Display

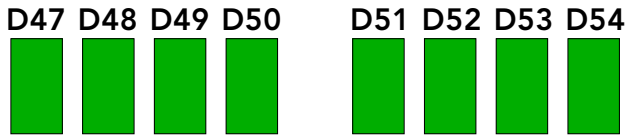
The conga-HPC/EVAL-Client provides four 14-segment displays (D66-D69) for post code or debug information. A list of the BIOS POST codes and associated POST test and initialization routines for congatec COM-HPC® modules is available at www.congatec.com.

D66 D67 D68 D69



5.4 Debug LEDs

The conga-HPC/EVAL-Client provides eight LEDs (D47-D54) for post code or debug information in binary format. A list of the BIOS POST codes and associated POST test and initialization routines for congatec COM-HPC® modules is available at www.congatec.com.



6 Mechanical Drawing