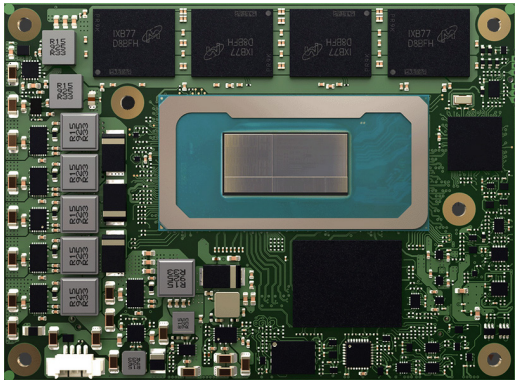

conga-HPC/mPTL

COM-HPC® 1.30 Mini Module with Intel® Core™ Ultra Series 3 Processors

User's Guide

Revision 0.01 (Preliminary)

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.01	2026-08-28	HSU	• Preliminary release

Preface

This user's guide provides information about the components, features, connectors and system resources available on the conga-HPC/mPTL. It is one of three documents that should be referred to when designing a COM-HPC® application. The other reference documents that should be used include the following:

COM-HPC® Module Base Specification
COM-HPC® Carrier Design Guide

These documents can be found on the PICMG® website at www.picmg.org.

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Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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Terminology

Term	Description
cBC	congatec Board Controller
CSI	Camera Serial Interface
CSM	Compatibility Suppport Module
COM	Computer-on-Module
DDI	Digital Display Interface
DP++	DisplayPort Dual-Mode
DPoC	DisplayPort over Type-C
DTR	Dynamic Temperature Range
E-cores	Efficient-cores
eDP	Embedded DisplayPort
EUs	Execution Units
HDA	High Definition Audio
N.A	Not available
N.C	Not connected
PCH	Platform Controller Hub
PCIe	PCI Express
P-cores	Performance-cores
PEG	PCI Express Graphics
TBD	To be determined
TDP	Thermal Design Power
TPM	Trusted Platform Module
TSN	Time-Sensitive Networking

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List of Tables

1 Introduction

1.1 COM-HPC® Concept

COM-HPC® is an open standard defined specifically for high performance Computer-on-Modules (COMs) for embedded systems. The defined module types are client module with fixed input voltage, client module with variable input voltage and server module with fixed input voltage.

The COM-HPC® modules are available in the following form factors:

- Mini 95 mm x 70 mm
- Size A 95 mm x 120 mm
- Size B 120 mm x 120 mm
- Size C 160 mm x 120 mm
- Side D 160 mm x 160 mm
- Side E 200 mm x 160 mm

Table 1 COM-HPC® Interface Summary

Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
Ethernet	NBASE-T	1 / 2	1 / 2	1 / 1	
	KR/KX	N.A	0 / 2	2 / 8	
	SGMII	0 / 2	N.A	N.A	
Storage	SATA	0 / 2	0 / 2	0 / 2	Pin is shared with PCIe on mini module
PCIe	Lane 0-47	1 / 16	4 / 48	8 / 48	Two PCIe reference clock output pairs required on mini module
	Lane 48-63	N.A	N.A	0 / 16	
	BMC	N.A	0 / 1	1 / 1	
USB	USB 2.0 Ports 0-7	6 / 8	4 / 8	4 / 8	Ports 0-5 (mini module) or ports 0-3 (server/client module) are used for USB 3.2 and USB4 if implemented.
	USB 3.2 Gen 1 or Gen 2	0 / 5	0 / 4	0 / 4	Requires one SuperSpeed Tx pair and one Rx pair per port
	USB 3.2 Gen 2x2	0 / 4	0 / 4	0 / 2	Requires two SuperSpeed Tx pairs and two Rx pairs per port
	USB4	0 / 4	0 / 4	0 / 2	USB4 ports use USB 3.2 Gen 2x2 ports
SPI	eSPI	0 / 1	0 / 1	0 / 1	
	Boot SPI	1 / 1	1 / 1	1 / 1	
	General Purpose SPI	1 / 1	1 / 1	1 / 1	

Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
BIOS Select	-	1 / 1	1 / 1	1/1	
Display	DDI	0 / 2	1 / 3	N.A	Additional display outputs may be available on the USB4 interface. On mini module, DDI pins are shared with USB4.
	eDP	0 / 1	0 / 1	N.A	
MIPI	DSI	0 / 1	0 / 1	N.A	
	CSI	N.A [1]	0 / 2	N.A	[1] Optional FFC connectors for MIPI-CSI on the mini module.
Audio	Soundwire	0 / 2	0 / 2	N.A	I2S pins may be used for one HDA port or two additional SoundWire ports for a total of up to four SoundWire ports.
	I2S	0 / 1	0 / 1	N.A	
Other Serial Ports	I2C	2 / 3	2 / 2	2 / 2	I2C0 and I2C1 for client and server modules. The mini module supports a third I2C port (I2C2/MDIO for SGMII PHY setup).
	SMBus	1 / 1	1 / 1	1 / 1	
	IPMB	N.A	0 / 1	0 / 1	
	UART	0 / 2	0 / 2	1 / 2	
GPIO	-		12 / 12	12 / 12	
Miscellaneous	Watchdog Timer	0 / 1	0 / 1	0 / 1	
	Fan (PWM and tachometer)	1 / 1	1 / 1	1 / 1	
FuSa	FuSa set of signals	0 / 1	0 / 1	0 / 1	
Power Rails	VCC	12 / 12	28 / 28	28 / 28	
	VCC_5V-SBY	N.A	0 / 2	0 / 2	The mini module does not have 5V standby pins.
	VCC_RTC	1 / 1	1 / 1	1 / 1	
	GND	All	All	All	All available GND pins shall be used.
Connector	J1	1 / 1	1 / 1	1 / 1	
	J2	N.A	0 / 1	1 / 1	

1.2 The conga-HPC/mPTL

The conga-HPC/mPTL is a COM-HPC® Mini module with Intel® Core™ Ultra Series 3 processors. The conga-HPC/mPTL is equipped with one high performance connector that ensure stable data throughput. It provides all the core functional requirements for any embedded application when mounted onto an application-specific carrier board.

1.3 Options Information

The conga-HPC/mPTL is currently available in six commercial and four industrial variants. The tables below show the different variants:

Table 2 Commercial Variants

Part-No.			045800	045801	045802	045803
Processor			Intel® Core™ Ultra 9 386H 16 Core™	Intel® Core™ Ultra X7 368H 16 Core™	Intel® Core™ Ultra 7 366H 16 Core™	Intel® Core™ Ultra 7 356H 16 Core™
# of Cores	P-Cores		4	4	4	4
	E-Cores	Normal	8	8	8	8
		Low Power	4	4	4	4
Entire Threads			16	16	16	16
Basic Clock Frequency	P-Cores		2.1 GHz	2 GHz	2 GHz	1.9 GHz
	E-Cores	Normal	1.6 GHz	1.6 GHz	1.6 GHz	1.5 GHz
		Low Power	1.6 GHz	1.6 GHz	1.6 GHz	1.5 GHz
Intel® Smart Cache			18 MB	18 MB	18 MB	18 MB
Assured Power (cTDP)	Processor Base Power		25 W	25 W	25 W	25 W
	Min. Assured Power		15 W	15 W	15 W	15 W
	Max. Assured Power		65 W	65 W	65 W	65 W
Max. Turbo Clock Frequency [1]	P-Cores		TBD	TBD	TBD	TBD
	E-Cores	Normal	TBD	TBD	TBD	TBD
		Low Power	TBD	TBD	TBD	TBD
Processor Graphics			Intel® Graphics (4 Xe Cores)	Intel® Arc™ B390 GPU (12 Xe Cores)	Intel® Graphics (4 Xe Cores)	Intel® Graphics (4 Xᵉ Cores)
Max Dynamic Frequency			2.5 GHz	2.5 GHz	2.5 GHz	2.45 GHz
Memory Specifications	Memory Type and Speed		LPDDR5X 8533 MT/s	LPDDR5X 8533 MT/s	LPDDR5X 8533 MT/s	LPDDR5X 8533 MT/s
	Size		32 GB	32 GB	16 GB	16 GB
	ECC Support		InBand ECC supported	InBand ECC supported	InBand ECC supported	InBand ECC supported
Storage Size			128 GB	128 GB	128 GB	128 GB
PCIe® Lanes	Total Supported		20	12	20	20
	Used (NVMe and Ethernet)		4	4	4	4
	Available Gen 4		4	4	4	4
	Available Gen 5		12	4	12	12
Ethernet Controller			Intel® I226-LM	Intel® I226-LM	Intel® I226-LM	Intel® I226-V
CPU Tjunction	Min.		0 °C	0 °C	0 °C	0 °C
	Max.		100 °C	100 °C	100 °C	100 °C
Compatible Carrier Board			conga-HPC/EVAL-Mini or conga-HPC/3.5-Mini			

Part-No.			045804	045805
Processor			Intel® Core™ Ultra 5 336H 12 Core™	Intel® Core™ Ultra 5 325 8 Core™
# of Cores	P-Cores		4	4
	E-Cores	Normal	4	0
		Low Power	4	4
Entire Threads			12	8
Basic Clock Frequency	P-Cores		1.9 GHz	2.1 GHz
	E-Cores	Normal	1.5 GHz	1.6 GHz
		Low Power	1.5 GHz	1.6 GHz
Intel® Smart Cache			18 MB	12 MB
Assured Power (cTDP)	Processor Base Power		25 W	25 W
	Min. Assured Power		15 W	12 W
	Max. Assured Power		65 W	55 W
Max. Turbo Clock Frequency [1]	P-Cores		TBD	TBD
	E-Cores	Normal	TBD	TBD
		Low Power	TBD	TBD
Processor Graphics			Intel® Graphics (4 Xe Cores)	Intel® Graphics (4 Xe Cores)
Max Dynamic Frequency			2.3 GHz	2.45 GHz
Memory Specifications	Memory Type and Speed		LPDDR5X 8533 MT/s	LPDDR5X 7467 MT/s
	Size		16 GB	16 GB
	ECC Support		InBand ECC supported	InBand ECC supported
Storage Size			128 GB	128 GB
PCIe® Lanes	Total Supported		20	12
	Used (NVMe and Ethernet)		4	4
	Available Gen 4		4	4
	Available Gen 5		12	4
Ethernet Controller			Intel® I226-LM	Intel® I226-V
CPU Tjunction	Min.		0 °C	0°C
	Max.		100 °C	100 °C
Compatible Carrier Board			conga-HPC/EVAL-Mini or conga-HPC/3.5-Mini	

Note

1. *The core frequencies and types vary by workload, power consumption and other factors.*

Table 3 Industrial Variants

Part-No.			045810	045811	045812	045813
Processor			Intel® Core™ Ultra 7 366HRE 16 Core™	Intel® Core™ Ultra 7 365RE 8 Core™	Intel® Core™ Ultra 5 336HRE 12 Core™	Intel® Core™ Ultra 5 335RE 8 Core™
# of Cores	P-Cores		4	4	4	4
	E-Cores	Normal	8	0	4	0
		Low Power	4	4	4	4
Entire Threads			16	8	12	8
Basic Clock Frequency	P-Cores		TBD	TBD	TBD	TBD
	E-Cores	Normal	TBD	TBD	TBD	TBD
		Low Power	TBD	TBD	TBD	TBD
Intel® Smart Cache			18 MB	12 MB	18 MB	12 MB
Assured Power (cTDP)	Processor Base Power		TBD	TBD	TBD	TBD
	Min. Assured Power		TBD	TBD	TBD	TBD
	Max. Assured Power		65 W	55 W	65 W	65 W
Max. Turbo Clock Frequency [1]	P-Cores		TBD	TBD	TBD	TBD
	E-Cores	Normal	TBD	TBD	TBD	TBD
		Low Power	TBD	TBD	TBD	TBD
Processor Graphics			Intel® Graphics (4 Xᵉ Cores)	Intel® Graphics (4 Xᵉ Cores)	Intel® Graphics (4 Xᵉ Cores)	Intel® Graphics (4 Xᵉ Cores)
Max Dynamic Frequency			TBD	TBD	TBD	TBD
Memory Specifications	Memory Type and Speed		LPDDR5X 8533 MT/s	LPDDR5X 7467 MT/s	LPDDR5X 8533 MT/s	LPDDR5X 8533 MT/s
	Size		32 GB	16 GB	32 GB	16 GB
	ECC Support		InBand ECC supported	InBand ECC supported	InBand ECC supported	InBand ECC supported
Storage Size			128 GB	128 GB	128 GB	128 GB
PCIe® Lanes	Total Supported		20	20	20	20
	Used (NVMe and Ethernet)		4	4	4	4
	Available Gen 4		4	4	4	4
	Available Gen 5		12	12	12	12
Ethernet Controller			Intel® I226-IT	Intel® I226-IT	Intel® I226-IT	Intel® I226-IT
CPU Tjunction	Min.		0 °C	0 °C	0 °C	0 °C
	Max.		100 °C	100 °C	100 °C	100 °C
Compatible Carrier Board			conga-HPC/EVAL-Mini or conga-HPC/3.5-Mini			

Note

1. *The core frequencies and types vary by workload, power consumption and other factors.*

2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	COM-HPC® Mini		
CPUs	Intel® Core™ Ultra Processors (Series 3) Panther Lake-H		
DRAM	Up to 32 GB LPDDR5x soldered down (optional up to 96 GB) with max. 8533 MT/s ; dual channel ; in-band ECC support on selected SKUs		
Graphics	Intel® Arc Graphics with up to 12 Xe cores or Intel® Graphics with up to 4 Xe cores ; Intel® Xe Matrix Extensions		
AI Acceleration	Integrated NPU accelerator with up to 50 TOPS		
Display	DP/DP++ (adding second DP/DP++ would require separate BIOS which disables USB4) ; eDP		
Ethernet	2x 2.5 GbE with TSN support via Intel® i226 Ethernet controller series (TSN only on selected PNs)		
I/O Interfaces	4x x1 PCIe Gen4 ; 1x x4 PCIe Gen5 ; 2x x4 PCIe Gen5 on selected SKUs ; USB4 (USB4 would be disabled if second DP/DP++ was enabled by separate BIOS) ; up to 4x USB 3.2 Gen2x1 ; up to 8x USB 2.0 ; 2x UART ; GP_SPI ; eSPI ; SM Bus ; FAN Control ; 12x GPIO		
Audio	HDA		
Storage	NVMe SSD with 128GB (optional up to 1 TB capacity)		
congatec Board controller	Next Gen 6 congatec Board Controller ; Multi-stage Watchdog ; non-volatile User Data Storage ; Manufacturing and Board Information Board Statistics ; I²C bus (fast mode, 400 kHz, multi-master) ; Power Loss Control Hardware Health Monitoring ; POST Code redirection		
Embedded BIOS Feature	AMI Aptio® UEFI firmware ; 64 Mbyte serial SPI with congatec Embedded BIOS feature ; OEM Logo OEM CMOS Defaults ; LCD Control ; Display Auto Detection ; Backlight Control ; Flash Update		
Security	Trusted Platform Module (TPM 2.0)		
Power Management	ACPI 6.0 with battery support		
Operating Systems	Microsoft® Windows 11 ; Microsoft® Windows 11 IoT Enterprise ; Linux ; Yocto		
Hypervisor	conga-zones hypervisor (previously known as RTS Hypervisor)		
Temperature Range	Commercial variants Industrial variants	Operation: 0°C to +60°C Operation: -40°C to +85°C	Storage: -20 to +80°C Storage: -40 to +85°C
Humidity	Operation: Storage:	10 to 85% r. H. non cond. 5 to 85% r. H. non cond.	
Size	95 x 70 mm²		

2.2 Supported Operating Systems

The conga-HPC/mPTL supports the following operating systems:

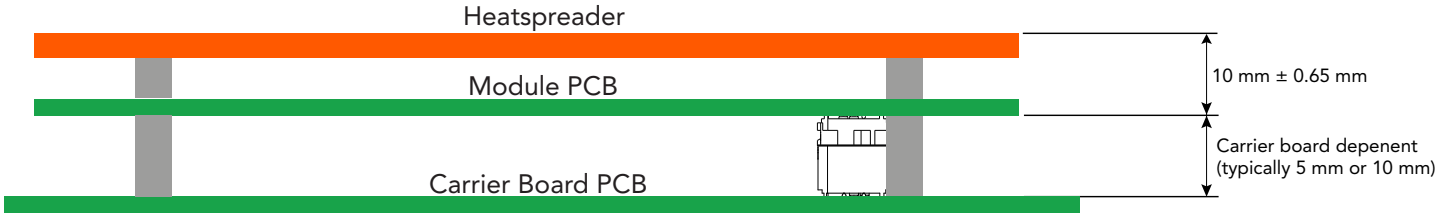
- Microsoft® Windows 11 (64-bit)
- Microsoft® Windows 11 IoT Enterprise (64-bit)
- Linux (64-bit)
- Yocto
- conga-zones hypervisor (previously known as RTS Hypervisor)

2.3 Mechanical Dimensions

The conga-HPC/mPTL has the following dimensions:

- length of 70 mm
- width of 95 mm
- PCB thickness of 2 mm +/- 10%

The overall height of an assembly is shown below:



Note

3D models of congatec products are available at www.congatec.com/login. These models indicate the overall length, height and width of each product. If you need login access, contact your local sales representative.

2.4 Supply Voltage Standard Power

The conga-HPC/mPTL requires 8 - 20 V DC input power.

2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for the conga-HPC/mPTL.

Table 5 Input Power - Wide Range Vin

Power Rail	Module VCC Pin Current Capability 20% derated (Amps)	Input Range (Volts)	Minimum Input (Volts)	Max Module Input Power (at minimum input voltage) (Watts)	Assumed Conversion Efficiency	Max Module Load Power at minimum input voltage (Watts)
VCC	12 * 1.12 = 13.4	8 - 20	8.0	107	85%	91
VCC_RTC	1.12	2.3 - 3.3	2.3			

2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal within a timeframe of 0.1 ms to 20 ms. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-HPC/mPTL
- modified congatec carrier board
- conga-HPC/mPTL cooling solution
- Microsoft® Windows® TBD

Note

The CPU was stressed to its maximum workload with the Intel® Power and Thermal Analysis Tool.

The power consumption values were recorded during the following system states:

Table 6 Measurement Description

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	Suspend to RAM state	Power for all power states, including full on, suspend and standby, are provided through the 12 VCC pins.
S5	Soft-Off state	
S5e	Enhanced Soft-Off state (congatec proprietary)	

Note

1. *The fan was powered externally.*
2. *All other peripherals except a DP monitor were disconnected before measurement.*

The table below provides the TDP Base power current values for the conga-HPC/mPTL at various system states:

Table 7 Power Consumption Values

Part No.	Memory Size	H.W Rev.	BIOS Rev.	CPU	Current (A) @ 12V					
					S0: Min	S0: Max	S0: Peak	S3	S5	S5e
045800	TBD	A.0	TBD	Intel® Core™ Ultra 9 386H 16 Core™	TBD	TBD	TBD	TBD	TBD	TBD
045801	TBD	A.0	TBD	Intel® Core™ Ultra X7 368H 16 Core™	TBD	TBD	TBD	TBD	TBD	TBD
045802	TBD	A.0	TBD	Intel® Core™ Ultra 7 366H 16 Core™	TBD	TBD	TBD	TBD	TBD	TBD
045803	TBD	A.0	TBD	Intel® Core™ Ultra 7 356H 16 Core™	TBD	TBD	TBD	TBD	TBD	TBD
045804	TBD	A.0	TBD	Intel® Core™ Ultra 5 336H 12 Core™	TBD	TBD	TBD	TBD	TBD	TBD
045805	TBD	A.0	TBD	Intel® Core™ Ultra 5 325 8 Core™	TBD	TBD	TBD	TBD	TBD	TBD
045810	TBD	A.0	TBD	Intel® Core™ Ultra 7 366HRE 16 Core™	TBD	TBD	TBD	TBD	TBD	TBD
045811	TBD	A.0	TBD	Intel® Core™ Ultra 7 365RE 8 Core™	TBD	TBD	TBD	TBD	TBD	TBD
045812	TBD	A.0	TBD	Intel® Core™ Ultra 5 336HRE 12 Core™	TBD	TBD	TBD	TBD	TBD	TBD
045813	TBD	A.0	TBD	Intel® Core™ Ultra 5 335RE 8 Core™	TBD	TBD	TBD	TBD	TBD	TBD

2.6 Supply Voltage Battery Power

Table 8 CMOS Battery Power Consumption

Module	RTC @	Voltage	Current
Commercial Variants	-10°C	3V DC	TBD µA
	20°C	3V DC	TBD µA
	70°C	3V DC	TBD µA
Industrial Variants	-50°C	3V DC	TBD µA
	20°C	3V DC	TBD µA
	95°C	3V DC	TBD µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to https://wiki.congatec.com/wiki/RTC_Battery_Lifetime_(AN09).*
4. *We recommend to always have a CMOS battery present when operating the conga-HPC/mPTL.*

2.7 Environmental Specifications

Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to 80°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to 85°C
Relative Humidity	Operation: 10% to 85%	Storage: 5% to 85%

Caution

The product is designed to operate in the above operating temperature range. It is the system integrator's responsibility to ensure that all components used on or with the product are operated within their individually specified temperature limits. For detailed information regarding the temperature specifications of individual components used on the product, refer to the respective thermal documentation (e.g., Hotspots CTNs) available in the customer login area at www.congatec.com and/or the customer knowledge base wiki.congatec.com. Appropriate cooling measures must be implemented in the final application to ensure proper heat dissipation.

Humidity specifications are for non-condensing conditions.

2.8 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

2.8.1 Module

For long-term storage of the conga-HPC/mPTL (more than six months), keep the conga-HPC/mPTL in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

Note

We do not recommend storing the conga-HPC/mPTL for more than five years under these conditions.

2.8.2 Cooling Solution

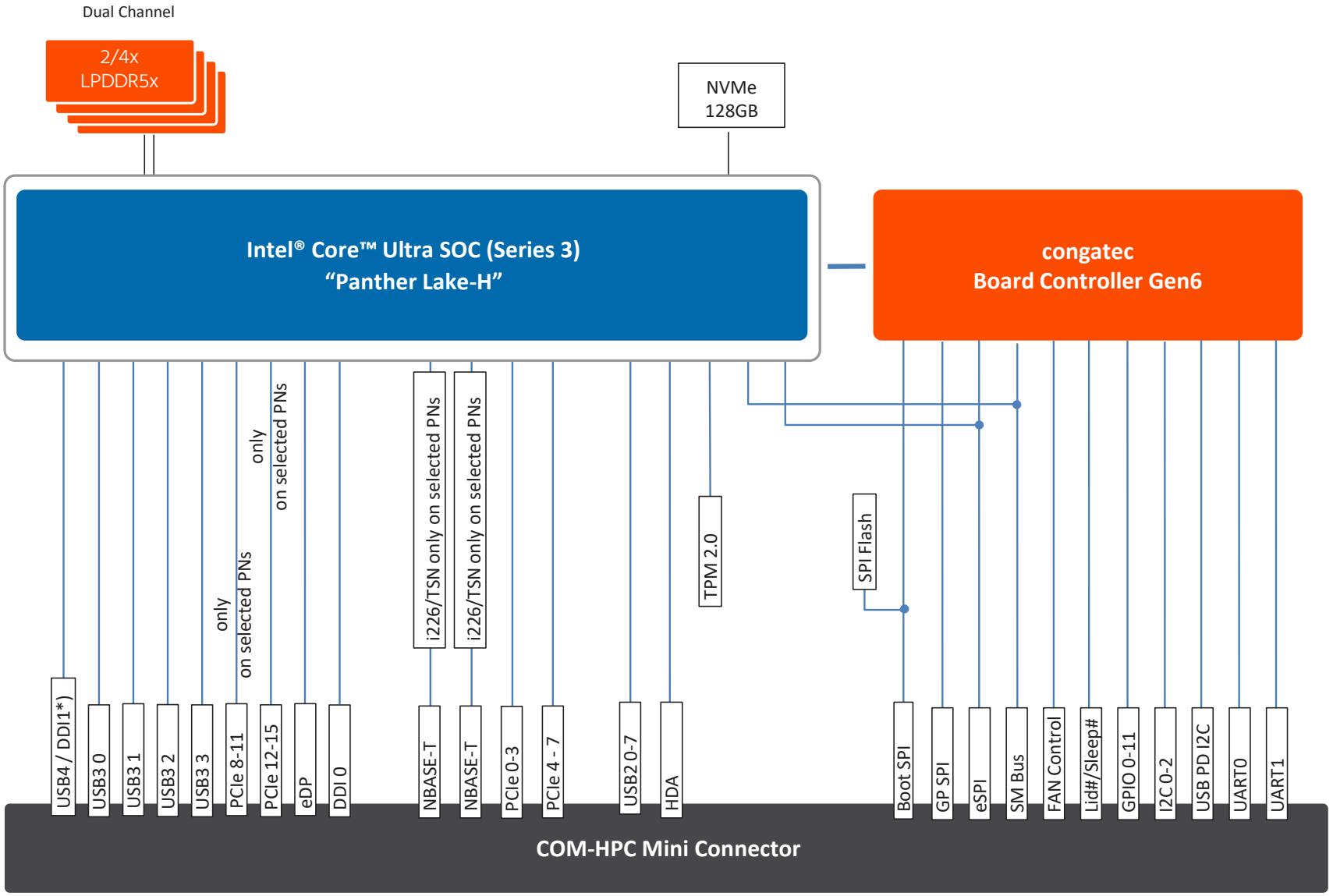
The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. For optimal cooling performance, do not store the heatspreaders/cooling solutions at temperatures below -20°C.

Caution

1. *For temperatures between -10°C and -20°C, preheat the heatpipes before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your local sales representative.*

2. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

3 Block Diagram



*) adding second DP/DP++ would require separate BIOS which disables USB4

4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-HPC/mPTL. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

Cooling Solution	Part No	Description
CSA	045850	Active cooling solution with 24.8 mm overall heat sink height, integrated 12 V fan and 2.7 mm bore-hole standoffs.
	045851	Active cooling solution with 24.8 mm overall heat sink height, integrated 12 V fan and M2.5 threaded standoffs
CSP	045852	Passive cooling solution with 24 mm overall heat sink height and 2.7 mm bore-hole standoffs
	045853	Passive cooling solution with 24 mm overall heat sink heightand M2.5 threaded standoffs
HSP	045854	Heatspreader with 2.7 mm bore-hole standoffs
	045855	Heatspreader with M2.5 threaded standoffs

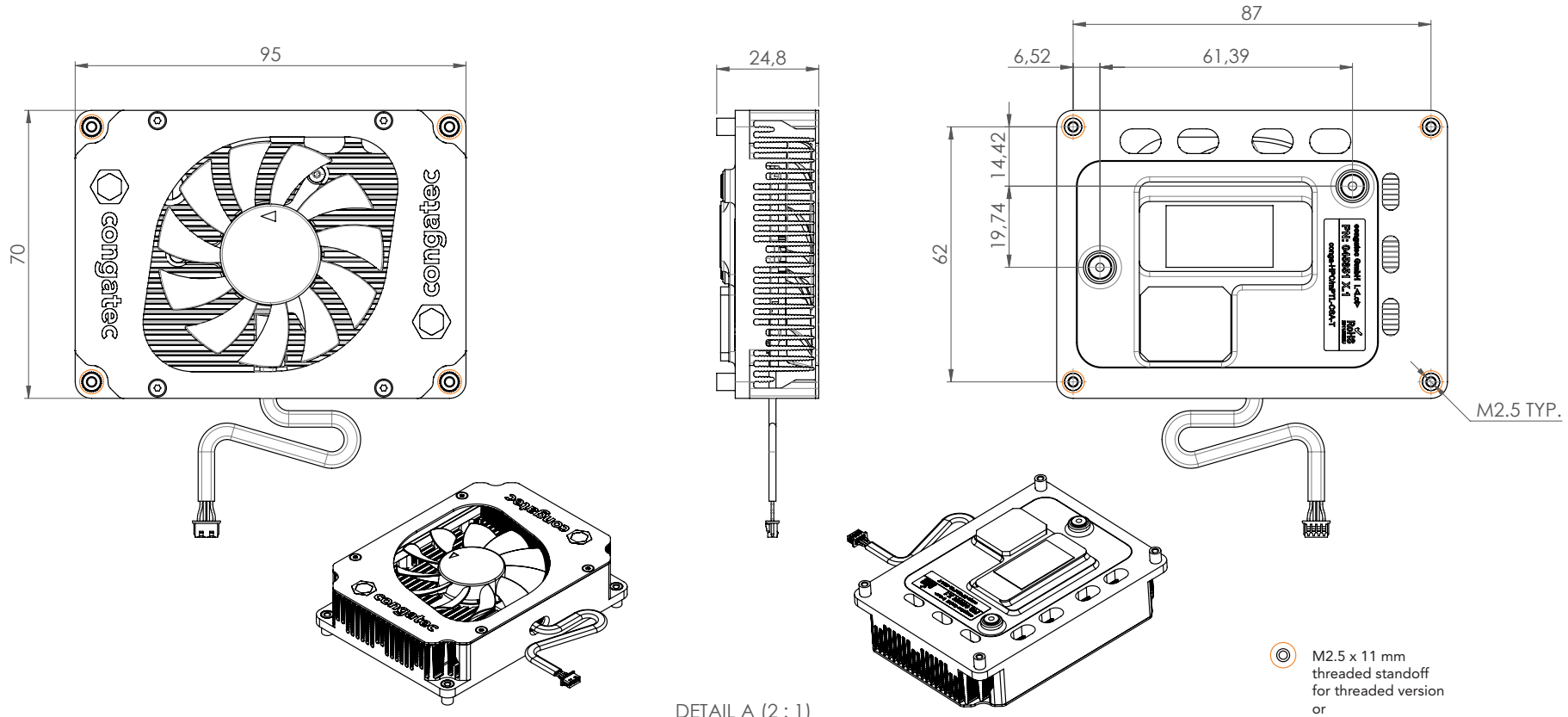
Caution

1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heat spreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. To ensure optimal cooling performance, they should not be stored at temperatures below -20°C. If the storage temperature drops below -10°C, the heatpipes should be pre-heated before operation. Optionally, the heatpipes can be filled with acetone instead.*
3. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
4. *For applications that require a vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
5. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

Note

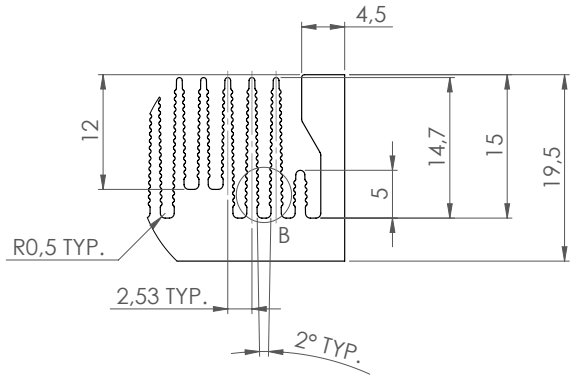
1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*
2. *The gap pad material used on congatec heat spreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*
3. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

4.1 CSA Dimensions

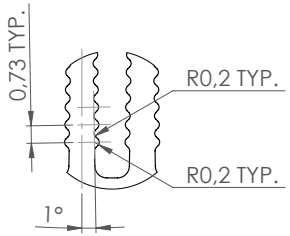


M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version

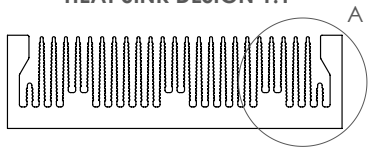
DETAIL A (2 : 1)



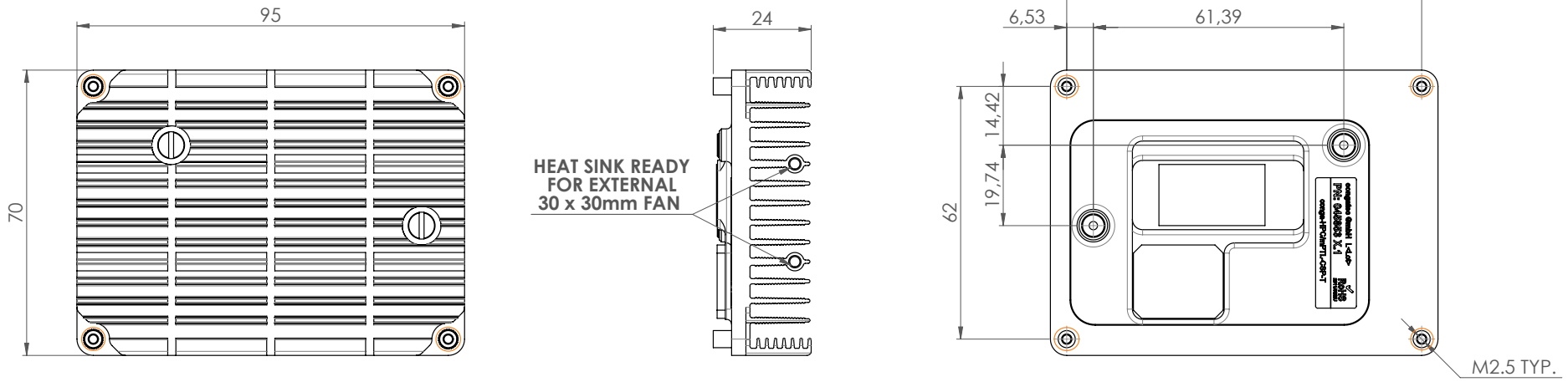
DETAIL B (5 : 1)

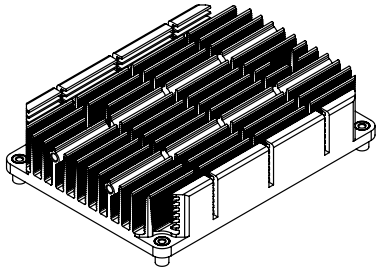


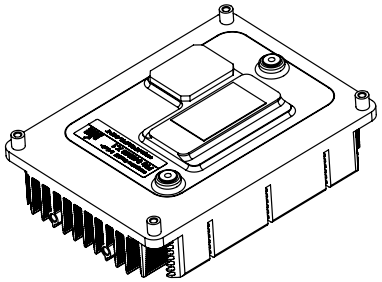
HEAT SINK DESIGN 1:1



4.2 CSP Dimensions

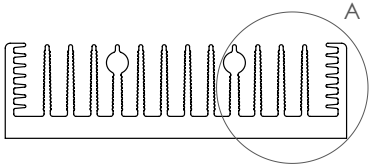




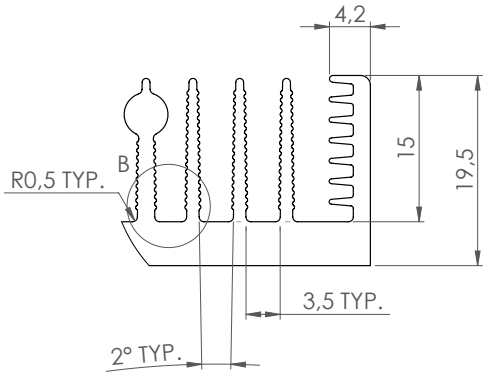


M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version

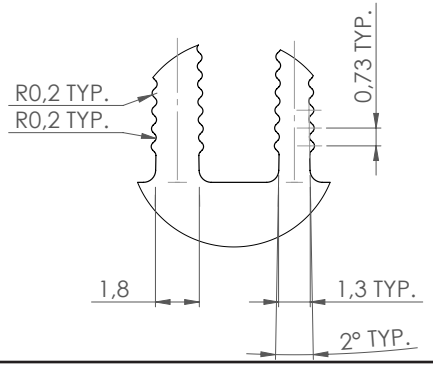
HEAT SINK DESIGN 1:1



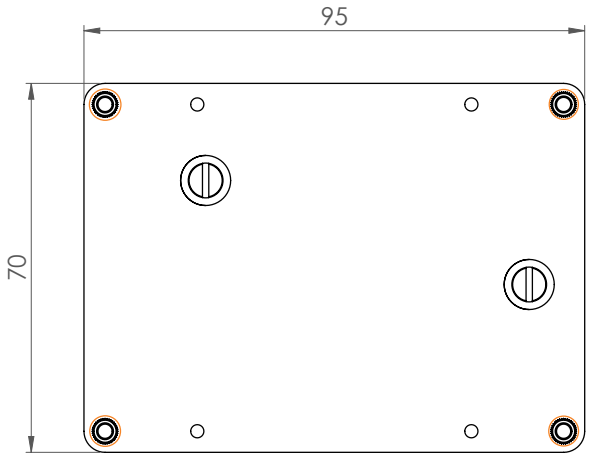
DETAIL A (2 : 1)

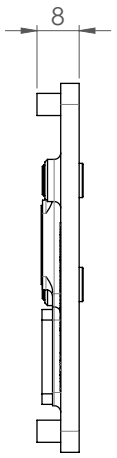


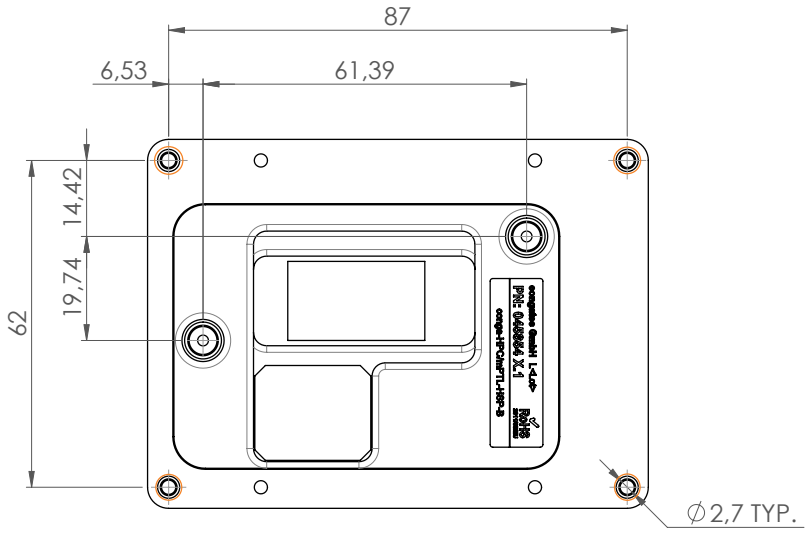
DETAIL B (5 : 1)



4.3 HSP Dimensions







M2.5 x 11 mm
threaded standoff
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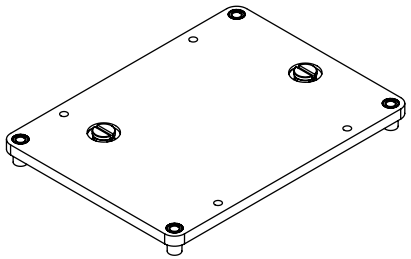
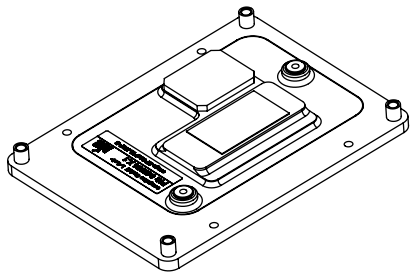
non-threaded standoff
for borehole version

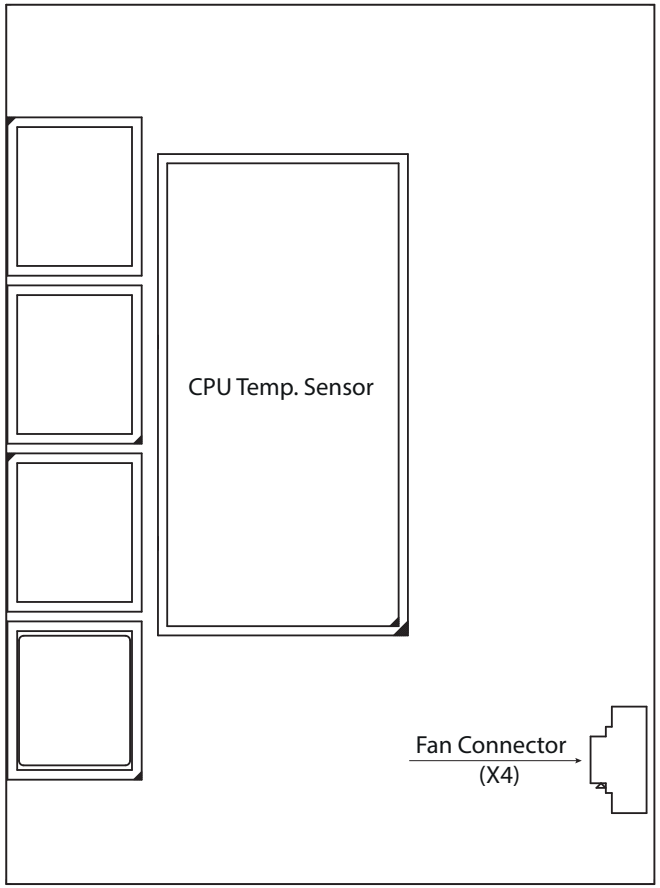




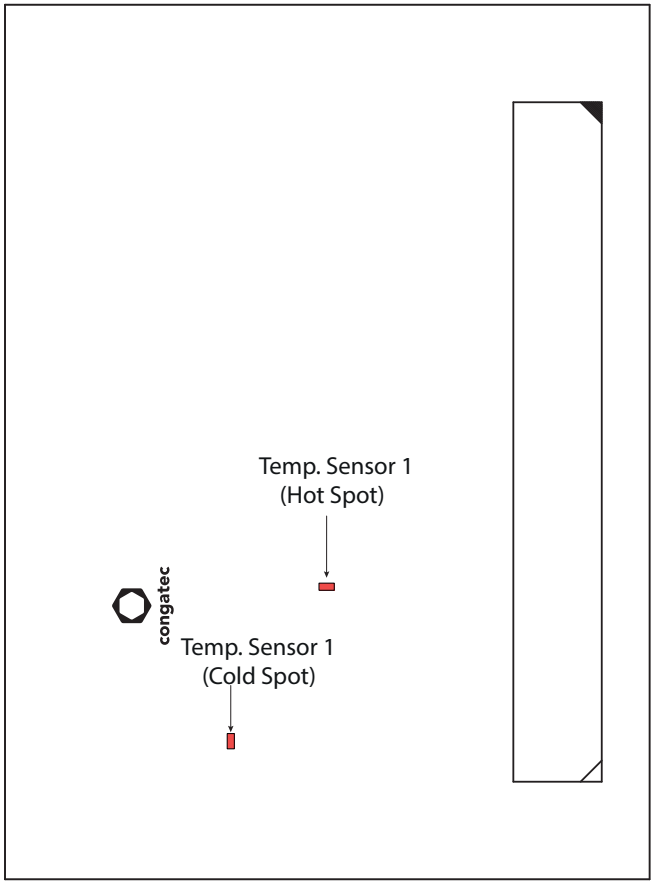
5 Onboard Temperature Sensors

The conga-HPC/mPTL features temperature sensor on the top-side in the processor CPU and two temperature sensors on the bottom-side. The location of each sensor and the fan connector (X4) is indicated in the drawings below:

Top-Side



Bottom-Side



6 Connector Rows

The conga-HPC/mPTL is connected to the carrier board via one 400-pin connector (COM-HPC® Mini pinout). This connector (J1) is broken down into four rows: A, B, C, and D. The following subsystems can be found on these connector rows.

6.1 NBASE-T Ethernet

The conga-HPC/mPTL offers two 2.5 Gigabit Ethernet interfaces (NBASET[0:1]) via two onboard Intel® i226-LM/V/IT controllers by default.

The 2.5 Gigabit Ethernet interfaces support:

- full-duplex operation at 10/100/1000/2500 Mbps
- half-duplex operation at 10/100 Mbps
- Intel® Active Management Technology (AMT) accesible via NBASET0 [1]
- Time-Sensitive Networking (TSN) for Intel® i226-LM and Intel® i226-IT controllers [1,2]
- one Software Defined Pin (SDP) per interface according to IEEE 1588

The table below explains the NBASET[0:1] link indicators:

Table 10 NBASET[0:1] Link Indicators

	When Active (Low)
NBASET[0:1]_LINK_MAX#	2.5 Gbit/s link
NBASET[0:1]_LINK_MID#	1 Gbit/s link
NBASET[0:1]_LINK_ACT#	Link and toggles for activity (either receive or transmit)

Note

1. *Not supported by commercial conga-HPC/mPTL variants with Intel® i226-V controllers (see section 1.3 "Options Information").*
2. *Not supported in Windows® Operating Systems.*
3. *The MAC address of the Intel® i226 Ethernet controller is preprogrammed by default. The MAC address cannot be reprogrammed. If you require custom MAC address, contact your local sales representative.*

6.2 PCI Express (PCIe)

The conga-HPC/mPTL can support the PCIe® link configurations listed in the table below:

Table 11 Supported PCIe Link Configurations

Lane	Bifurcation			Gen	Supported SKUs	TX AC-Coupling Capacitors	RX AC-Coupling Capacitors
15	—	—	x4	5	Only on variants supporting total 20 PCIe lanes	On Module	Off Module
14							
13		x2					
12	x1						
11	—	—	x4				
10							
09		x2					
08	x1						
07	—	x2	x4		All Variants	Off Module	Off Module
06							
05		x2					
04	x1						
03	x1	x2	x4	4			
02	x1						
01	x1	x2					
00	x1						

Note

1. *PCIe lanes 08 to 15 are not supported on the 045801 and 045805 variants, which provide a total of 12 PCIe lanes. These lanes are only supported on selected variants providing up to 20 PCIe lanes. Refer to Chapter 1.3 "Options Information" for an overview of variants providing 20 and 12 PCIe lanes.*

2. *Default link width highlighted in green. Optional link configurations require a customized BIOS.*

6.3 USB4 / DDI / USB 3.2 / USB 2.0 Interfaces

The conga-HPC/mPTL supports eight USB 2.0 ports and eight Super Speed lanes that may be used for USB4®, DDI or USB 3.2 interfaces according to the "Configuration 1" and "Configuration 2" defined in the COM-HPC® Module Base Specification.

The conga-HPC/mPTL supports "Configuration 2" by default. Optionally, it can support "Configuration 1" instead (Optional BIOS). The interfaces supported by each configuration are listed in the table below:

Table 12 Supported Super Speed Lane Configurations

Configuration 1 (Optional BIOS)	Configuration 2 (Default BIOS)
DDI #0	DDI #0
DDI #1	**USB4 #0**
USB3 #3	USB3 #3
USB3 #2	USB3 #2
USB3 #1	USB3 #1
USB3 #0	USB3 #0

Note

For information about implementing USB4®, DDI, USB 3.2 and USB 2.0 interfaces, refer to the COM-HPC® Module Base Specification Revision 1.30 and COM-HPC® Carrier Design Guide.

The USB interfaces support the functions listed in the table below:

Table 13 USB4, USB 3.2 and USB 2.0 Ports

Function	USB4 #0 [1]	USB 3.2 #0	USB 3.2 #1	USB 3.2 #2	USB 3.2 #3	USB 2.0 #0	USB 2.0 #1	USB 2.0 #2
USB 1.0	x	x	x	x	x	x	x	x
USB 1.1	x	x	x	x	x	x	x	x
USB 2.0	x	x	x	x	x	x	x	x
USB 3.2 Gen 1x1	x	x	x	x	x			
USB 3.2 Gen 2x1	x	x	x	x	x			
USB 3.2 Gen 2x2	x							
USB4 Gen 2x2	x							
USB4 Gen 3x2	x							
DisplayPort over Type-C	x							

Note

1. *Either USB4® (default BIOS) or DD1 (optional BIOS) can be supported.*
2. *The numbering of the ports (indicated by #x) does not correspond to the pin names of the COM-HPC® connector.*

The USB 2.0 and Super Speed pairs assigned to each USB interface are listed in the table below:

Table 14 USB 2.0 and SS Pair Assignments

	USB4 #0 [1]	USB 3.2 #0	USB 3.2 #1	USB 3.2 #2	USB 3.2 #3	USB 2.0 #0	USB 2.0 #1	USB 2.0 #2
Required USB 2.0 Pair	USB0	USB5	USB3	USB4	USB1	USB2	USB6	USB7
Required SS-Pair	2/3	7	6	5	4	-	-	-

Note

1. *Either USB4® (default BIOS) or DD1 (optional BIOS) can be supported.*
2. *The numbering of the ports (indicated by #x) does not correspond to the pin names of the COM-HPC® connector.*
3. *For information about implementing USB4®, DDI, USB 3.2 and USB 2.0 interfaces, refer to the COM-HPC® Module Base Specification Revision 1.30 and COM-HPC® Carrier Design Guide.*
4. *USB4® ports (also the corresponding USB 2.0 ports) requires a PD controller and retimer to function with the default BIOS. These ports may optionally be used as USB 3.2 Gen 2x1 ports (or lower) without a PD controller and retimer (Custom BIOS Option).*

USB PD controllers and retimers implemented on the carrier board must use the SMLink addresses listed in the table below:

Table 15 USB PD Controller and Retimer Addresses

USB4 Port	0
USB PD Controller:	
- SML1 Address (7-bit)	0x48
- USB_PD_I2C Address(7-bit)	0x22
Thunderbolt Retimer:	
- SML0 Address (7-bit)	0x55

6.4 Display Interfaces

The conga-HPC/mPTL can offer up to three display interfaces as listed in the table below:

Table 16 Display Combinations and Resolutions

DDI0		DDI1 [1]		eDP	
Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution
DP++	Up to 6K at 60 Hz	DP++	Up to 6K at 60 Hz	eDP	up to 4K at 120Hz HDR
	Up to 8K at 60 Hz compressed		Up to 8K at 60 Hz compressed		
	Up to 5K at 120 Hz compressed		Up to 5K at 120 Hz compressed		

Note

1. *Either DD1 (default) or USB4® (optional BIOS) can be supported.*

6.4.1 DisplayPort Dual-Mode (DP++)

The conga-HPC/mPTL offers up to two DP++ interfaces (DDI[0:1])[1,2] with support for:

- VESA® DisplayPort™ Standard 2.1
- Upto UHBR20 (20 Gbit/s per lane)
- Various audio formats

Note

1. *Either USB4® (default BIOS) or DD1 (optional BIOS) can be supported.*

2. *For information about implementing USB4®, DDI, USB 3.2 and USB 2.0 interfaces, refer to the COM-HPC® Module Base Specification Revision 1.30 and COM-HPC® Carrier Design Guide.*

6.4.2 Embedded DisplayPort (eDP)

The conga-HPC/mPTL offers one eDP™ interface with support for:

- VESA® Embedded DisplayPort™ Standard 1.4b/1.5
- Up to HBR3 (8.1 Gbit/s per lane)
- Spread-Spectrum Clocking
- eDP™ display authentication

6.5 eSPI Interface

The conga-HPC/mPTL offers an eSPI interface for general purpose carrier board devices such as Super I/O, FPGAs, CPLDs and so on. The interface offers two chip select pins (eSPI_CS0# and eSPI_CS1#) for carrier board devices.

6.6 Boot SPI Interface

The conga-HPC/mPTL offers a Boot SPI interface for a carrier-based SPI BIOS flash device. The congatec onboard flash device is connected to this Boot SPI interface.

The pins to select the carrier-based SPI BIOS flash device are described in the section 6.8 "BIOS Boot Selection" below.

Note

1. *The power supply to the carrier board SPI (VCC_BOOT_SPI) is 1.8 V.*

2. *The onboard SPI flash is disabled when the carrier board SPI flash is enabled.*

6.7 BIOS Boot Selection

The boot select pins BSEL0-BSEL2 are configured to load the BIOS firmware from the conga-HPC/mPTL by default. Optionally, you can configure these pins to load the BIOS firmware from the carrier board SPI flash as described in the table below:

Table 17 BIOS Select Options

BSEL2	BSEL1	BSEL0	Boot Option
N.C	N.C	N.C	Boot from module SPI flash (default)
N.C	N.C	GND	Boot from carrier board SPI flash

6.8 Audio Interfaces

The conga-HPC/mPTL offers the following audio interfaces by default:

- one Intel® High Definition Audio (HDA) interface
- two MIPI SoundWire® interfaces

Optionally, the conga-HPC/mPTL can offer two additional MIPI SoundWire® interfaces or one I²S interface instead of HDA (assembly option).

Note

The I2S interface is not verified because the relevant drivers are currently not available. For a verified audio interface, we recommend to use HDA.

6.9 Asynchronous Serial Port Interfaces

The conga-HPC/mPTL offers two 16C550 compatible UART interfaces (UART[0:1]) via the congatec Board Controller by default. The interfaces support hardware handshake, flow control, and up to 115200 baud rate.

6.10 I2C Ports

The conga-HPC/mPTL offers three I2C ports (I2C[0:2]) via the congatec Board Controller with support for 400 kHz operation and multi-master mode. I2C0 also supports interrupts via the I2C0_ALERT# signal.

Note

1. *You need the congatec CGOS driver and API to access the I2C interface.*
2. *Onboard resources are not connected to the I2C bus.*

6.11 Port 80 Support on USB_PD I2C Bus

The conga-HPC/mPTL offers BIOS Port 80h debug information over the USB Power Delivery I²C Bus (USB_PD_I2C_DAT and USB_PD_I2C_CLK). The debug information is serialized and must be deserialized on the carrier board. For information on how to deserialize and display the debug information on carrier board 7-segment displays, refer to the COM-HPC® Carrier Design Guide.

6.12 General Purpose SPI Port

The conga-HPC/mPTL offers a general purpose SPI port and two chip selects (GP_SPI_CS[0:1]#) via the congatec Board Controller by default.

Optionally, the general purpose SPI port can be provided via the Intel® chipset instead with support for GP_SPI_CS0# only (assembly option).

6.13 SMBus

The conga-HPC/mPTL offers a System Management Bus (SMBus) via the Intel® chipset. The SMBus can be either always connected or isolated via a switch (BIOS Setup option).

The table below lists addresses reserved for onboard devices on the conga-HPC/mPTL:

Table 18 Reserved SMBus Addresses on the conga-HPC/mPTL

7-bit Address	Onboard SMBus Device
0x6F	Voltage regulator for primary fan

Note

Make sure the address space of the carrier board SMBus devices does not overlap the address space of the module devices. For more information, refer to the COM-HPC® Module Base Specification and COM-HPC® Carrier Design Guide.

6.14 General Purpose Input Outputs (GPIOs)

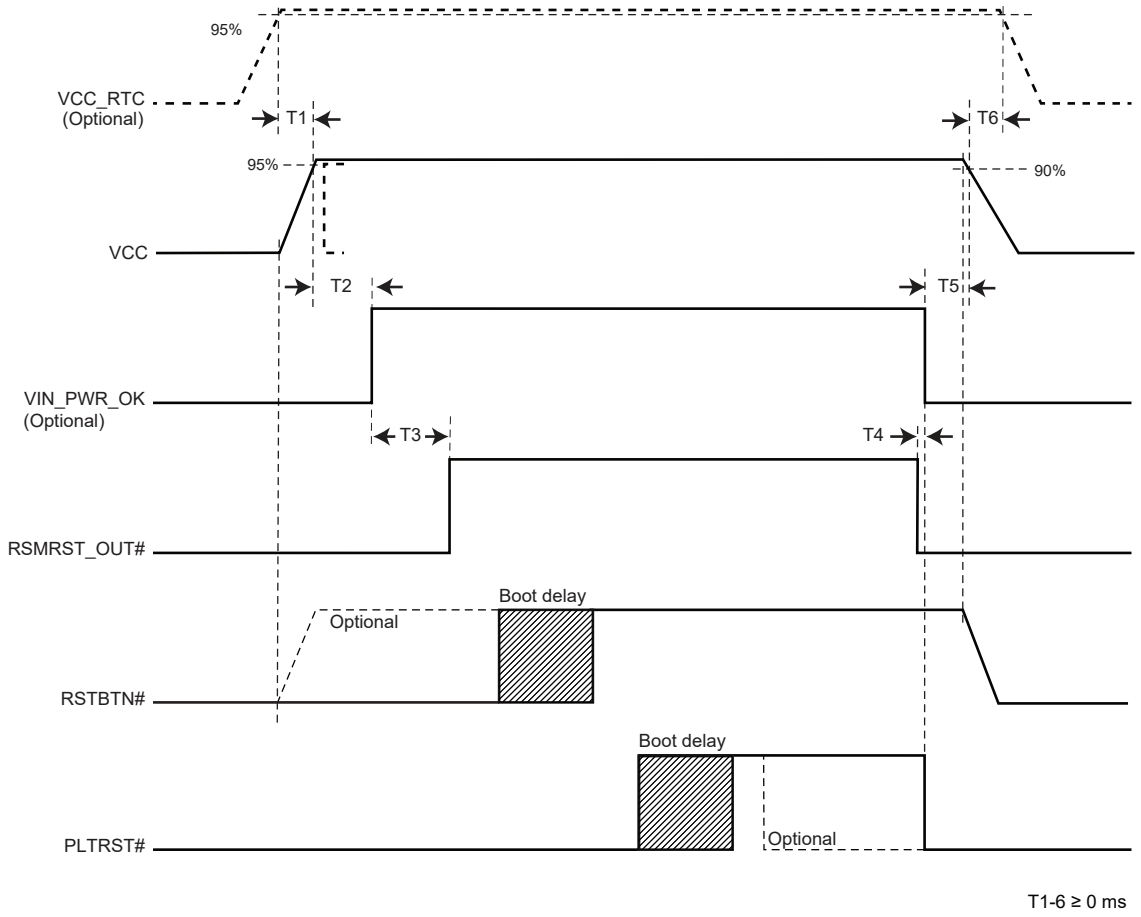
The conga-HPC/mPTL offers 12 general purpose inputs and outputs (GPIO_[00:11]) via the congatec Board Controller.

Note

M.2-specific signal overlays on GPIO_[03:11] are not supported.

6.15 Power Control

The conga-HPC/mPTL operates over a range of 8 V to 20 V input power. Its power-up sequence is illustrated below:



Note

For more information about the power sequencing requirements, refer to the COM-HPC® Module Base Specification 1.30.

6.16 Power Management

ACPI

The conga-HPC/mPTL supports Advanced Configuration and Power Interface (ACPI) specification, revision 6.0. For more information, see section 8.5 "ACPI Suspend Modes and Resume Events".

S5e Power State

The conga-HPC/mPTL features a congatec proprietary Enhanced Soft-Off power state, described in section 7.2.4 "Enhanced Soft-Off State".

6.17 Inrush and Maximum Current Peaks

The table below compares the inrush current and slew rate values of the conga-HPC/mPTL at different voltage ramp durations.

Table 19 Inrush Current

Power Rail	Inrush Current [A]	Slew Rate [kV/s]	Voltage Ramp [ms]	Comment
VCC	TBD	TBD	TBD	Worst-case scenario
VCC	TBD	TBD	TBD	Typical scenario

Note

Ensure the power supply and decoupling capacitors on the carrier board are adequate for proper power sequencing.

7 Additional Features

7.1 conga-zones hypervisor

The conga-zones hypervisor (formerly known as RTS Hypervisor) is integrated into the congatec firmware on the conga-HPC/mPTL by default. With the conga-zones hypervisor, you can consolidate functionality that previously required multiple dedicated systems on a single x86 hardware platform.

The integrated conga-zones hypervisor offers a 30-day free evaluation license. The 30-day evaluation starts when the customer receives the x86-based modules. To access the full package, contact congatec Sales team via the online "Request Quote" button for your particular product at https://www.congatec.com/en/products/hypervisor-products/.

To activate the conga-zones hypervisor, change the “Boot Device” in the BIOS setup menu to “Integrated RTS Hypervisor”.

1. Press F2 or DEL during POST to enter the BIOS setup menu.
2. Go to the Boot tab to enter the Boot setup screen.
3. Select “Integrated RTS Hypervisor" as “1st Boot Device”.
4. Go to the Save & Exit tab and select “Save Changes and Exit”.

For more information about the integrated Hypervisor, refer to https://wiki.congatec.com/wiki/Hypervisor_on_Module_(AN56).

Note

1. *The configuration steps and the BIOS setup menu above are valid for "Type Based Boot Priority". For "UEFI Boot Priority", the BIOS setup menu may differ.*
2. *The Real-Time Operating System images, driver packages for the General-Purpose Operating System and the installation procedures for the Operating Systems are available for download under the "Technical information" section, in the restricted area of congatec website at www.congatec.com/login. If you require login access, contact your local sales representative.*

7.2 congatec Board Controller (cBC)

The conga-HPC/mPTL is equipped with a Microchip microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The congatec Board Controller (cBC) supports the following features:

- Board information (See section 7.2.1)
- Watchdog (See section 7.2.2)
- Asynchronous Serial Port Interfaces (See section 6.10)
- I²C Ports (See section 6.11)
- Port 80 Support on USB_PD I2C Bus (See section 6.12)
- General Purpose SPI Port (See section 6.13)
- SMBus (See section 6.14)
- General Purpose Input Outputs (GPIOs) (See section 6.15)
- Fan Control (See section 7.2.3)
- Enhanced Soft-Off State (section 7.2.4)
- Power Loss Control (See section 7.2.5)

7.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

7.2.2 Watchdog

The cBC provides a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, refer to https://wiki.congatec.com/wiki/Watchdog_(AN03).

7.2.3 Fan Control

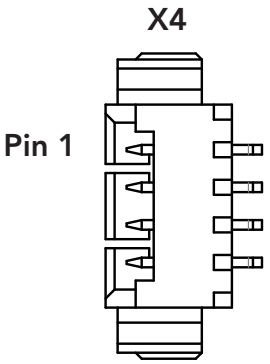
The cBC provides signals for a primary and secondary fan. Signals for the primary fan are routed to onboard connector X4. Signals for the secondary fan are routed to the COM-HPC® connector.

For the location of the onboard connector and information about the temperature sensors, see section 5 "Onboard Temperature Sensors".

The pinout of the primary fan connector (X4) is described in the table below:

Table 20 Primary Fan Connector (X4) Pinout

Pin	Signal
1	GND
2	+12V_FAN (max. 700mA)
3	CPU_FAN_TACHIN
4	CPU_FAN_PWMOUT



Connector Type

X4: 4x1 pins, 1.25mm pitch (Molex 53261-0471); Possible Mating Connector: Molex 51021-0400

Note

A four wire fan must be used to generate the correct speed readout.

7.2.4 Enhanced Soft-Off State

The cBC provides an enhanced Soft-Off state (S5e)—a congatec proprietary low-power Soft-Off state. In this state, the CPU module switches off almost all the onboard logic to reduce the power consumption to absolute minimum.

The S5e supports power button, sleep button and SMBALERT# wake events. For detailed description of the S5e state, refer to https://wiki.congatec.com/wiki/S5e_Implementation_(AN36).

7.2.5 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after a power loss occurs. The power loss control feature has three different modes that define how the system responds when power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to "ON".*
2. *The 30 seconds monitoring cycle applies only to the "Last State" power loss control mode.*

7.3 OEM BIOS Customization

The conga-HPC/mPTL is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide: https://wiki.congatec.com/wiki/Congatec_System_Utility_-_CGUTIL or contact technical support. The supported customization features are described in the following sub-sections.

7.3.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. For more information on how to add OEM default settings to the congatec Embedded BIOS, refer to https://wiki.congatec.com/wiki/Create_OEM_Default_Map_(AN08).

7.3.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. For instructions on how to add OEM boot logo to the congatec Embedded BIOS, refer to https://wiki.congatec.com/wiki/Create_and_add_a_Boot_Logo_(AN11).

7.3.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

7.3.4 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

7.4 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-HPC/mPTL BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system. For more information about the supported Battery Management Interface, contact your local sales representative.

7.5 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available at www.congatec.com.

7.6 Security Features

The conga-HPC/mPTL is equipped with an onboard SPI TPM 2.0 (Infineon SLB 9672VU2.0 FW15 for commercial variants and SLB 9672XU2.0 FW15 for industrial variants).

7.7 NVMe

The conga-HPC/mPTL offers an onboard BGA NVMe (Micron 4100AT) with 128 GB by default. The NVMe is connected via a x2 PCIe Gen 4 link.

Optionally, the NVMe can be offered in the following storage capacities (assembly option):

- 256 GB
- 512 GB
- 1 TB

8 conga Tech Notes

The Intel® Panther Lake (PTL) processor is a 64-bit, multi-core processor built on Intel® 18A process, N6 and N3E technology. Some of the important features supported by the processor are:

- Intel® Image Processing Unit 7.5 (Intel® IPU 7.5)
- Intel® Neural Processing Unit (Intel® NPU)
- Intel® VT-x and VT-d
- Intel® Turbo Boost Technology 2.0
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)
- Intel® Thread Director
- Intel® Boot Guard
- Intel® SpeedStep Technology
- Intel® Active Management Technology (Intel® AMT)
- Intel® Platform Trust Technology (Intel® PTT)
- Intel® Dynamic Tuning Technology (Intel® DTT)
- Intel® Total Memory Encryption (Intel® TME)
- Intel® Volume Management Device (Intel® VMD)
- Intel® High Definition Audio (HD Audio)
- Intel® Smart Sound Technology (SST)
- Intel® Active Management Technology (AMT)

8.1 Processor Performance Control

8.1.1 Enhanced Intel SpeedStep Technology (EIST)

Intel® processors found on the conga-HPC/mPTL run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® Technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states to efficiently operate the processor when it is not being fully used. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that the power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

The Intel® Core™ Ultra Series 3 processor family supports Intel® Speed Shift, a new and energy efficient method for frequency control. This feature is also referred to as Hardware-controlled Performance States (HWP). The feature is a hardware implementation of the ACPI defined Collaborative Processor Performance Control (CPPC2) and is supported by newer operating systems (Win 8.1 or newer).

With this feature enabled, the processor autonomously selects performance states based on workload demand and thermal limits while also considering information provided by the OS e.g., the performance limits and workload history.

8.1.2 Intel Speed Shift Technology

Intel® Speed Shift Technology is an energy-saving approach to frequency control that relies on hardware rather than operating system control. The operating system is informed of the hardware P-states that are available and can either request a specific P-state or allow the hardware to determine the P-state.

The request made by the operating system is based on the workload requirements and knowledge of the processor's capabilities. Meanwhile, the processor's decision is influenced by various system constraints, such as workload demand, thermal limits, and the minimum and maximum levels of performance requested by the operating system, while taking into account the activity window.

8.1.3 Intel Turbo Boost Technology 2.0

The IA core/processor graphics core of the processor can automatically run faster than its base frequency, using the Intel® Turbo Boost Technology 2.0. This feature operates within power, temperature, and current limits and optimizes performance for both single-threaded and multi-threaded workloads.

With Intel® Turbo Boost Technology 2.0, the application power is directed more towards Thermal Design Power (TDP). The processor can

exceed the TDP by going as high as PL2 for short durations. However, if the cooling solution is not designed accordingly, the system may face performance and thermal issues as more applications will run at the maximum power limit for extended periods. For more information about Intel® Turbo Boost 2.0 Technology visit the Intel® website.

8.2 Intel® Neural Processing Unit (Intel® NPU)

The Intel® Neural Processing Unit (NPU) is a dedicated hardware accelerator integrated into Intel® Panther Lake processors. It enables high-performance processing for AI applications while maintaining optimized power consumption, making it suitable for embedded, edge, and client platforms. The NPU offloads AI-related tasks from the CPU and GPU, improving overall system efficiency and responsiveness. It consists of a host control subsystem and a deep learning accelerator, which together manage task scheduling and execution. The deep learning accelerator is based on multiple Neural Compute Engine (NCE) tiles that provide scalable parallel processing capabilities. These tiles integrate specialized compute units and local memory to efficiently process neural network operations.

8.3 Adaptive Thermal Monitor and Catastrophic Thermal Protection

Intel® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu “CPU submenu”.

The Adaptive Thermal Monitor controls the processor temperature using two methods:

- Adjusting the processor’s operating frequency and core voltage (EIST transitions)
- Modulating (start/stop) the processor’s internal clocks at a duty cycle of 25% on and 75% off

When activated, the TCC causes both processor core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated. Clock modulation is activated if frequency and voltage adjustments are insufficient. Additional hardware, software driver, or operating system support is not required.

Intel® processors use the THERMTRIP# signal to shut down the system if the processor’s silicon reaches a temperature of approximately 125°C. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

Note

To ensure that the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Panther Lake (PTL) processor’s respective datasheet can provide you with more information about this subject.

8.4 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel® architecture microprocessors and chipsets. Intel® Virtualization Technology for Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

conga-zones hypervisor supports Intel® VT and is verified on all current congatec x86 hardware.

Note

congatec supports conga-zones hypervisor.

8.5 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to implement cooling decisions according to the demands of the application.

The conga-HPC/mPTL offers hardware-based support for passive and active cooling. Passive cooling is implemented in the Intel® CPU via the Thermal Control Circuit (TCC) Activation Offset setting in the CPU configuration setup sub-menu. The TCC in the processor is activated at 100°C by default but can be lowered by the Activation Offset—for example, an activation offset of "10" will activate TCC at 90°C. ACPI OS support is not required. See section 8.3 "Adaptive Thermal Monitor and Catastrophic Thermal Protection" for more information.

The congatec Board Controller (cBC) supports active cooling solution. The cBC controls the fan's speed based on the temperature readings of the CPU. This feature does not require ACPI OS support. The only software-controlled thermal trip point on conga-HPC/mPTL is the Critical Trip Point. The active or passive cooling policy should ensure that the CPU temperature does not reach this trip point. However, if the critical trip point is reached, the OS will shut down properly in order to prevent damage to the system. Use the "critical trip point" setup node in the BIOS setup menu to determine the temperature threshold at which the system shuts down.

Note

The Automatic Critical Trip Point BIOS setting shuts down the system at 5°C above the maximum specified temperature of the processor.

8.6 ACPI Suspend Modes and Resume Events

The conga-HPC/mPTL BIOS supports S3 (Suspend to RAM), S4 (Suspend to Disk), S5 (Soft-Off) and S5e (congatec proprietary low-power Soft-Off). The table below lists the events that wake the system.

Table 21 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5; S5e
Onboard LAN Event	Device driver must be configured for Wake On LAN support
SMBALERT#	Wakes unconditionally from S3-S5; S5e
PCI Express WAKE#	Wakes unconditionally from S3-S5
WAKE#	Wakes unconditionally from S3
PME#	Activate the wake up capabilities of a PCI device using Windows device manager configuration options for this device or set "Resume On PME#" to "Enabled" in the power setup menu
USB Mouse/Keyboard Event	When "Standby mode" is set to S3, USB hardware must be powered by standby power source. Set "USB Device Wakeup" from S3/S4 to "Enabled" in the ACPI setup menu (if setup node is available in BIOS setup program). In device manager, look for the keyboard/mouse devices. Go to the power management tab and check "Allow this device to bring the computer out of standby".
RTC Alarm	Activate and configure "Resume On RTC Alarm" in the power setup menu (only available in S5)
Watchdog Power Button Event	Wakes unconditionally from S3-S5

9 Signal Descriptions and Pinout Tables

This section describes the signals found on the conga-HPC/mPTL. The pinout complies with PICMG® COM-HPC®, revision 1.30. The table below describes the terminology used in this section. The PU/PD column indicates if a pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors. Only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 22 Signal Description Terminology

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 1.8 V	Bi-directional signal 1.8V tolerant
I/O 3.3 V	Bi-directional signal 3.3V tolerant
I/O 5 V	Bi-directional signal 5V tolerant
I 1.8 V	Input 1.8V tolerant
I 3.3 V	Input 3.3V tolerant
I 5 V	Input 5V tolerant
I/O 1.8 VSB	Bi-directional signal 1.8V tolerant active in standby state
I/O 3.3 VSB	Bi-directional signal 3.3V tolerant active in standby state
O 1.8 V	Output 1.8V signal level
O 3.3 V	Output 3.3V signal level
O 5 V	Output 5V signal level
OD	Open drain output
V_{OL}	Output low voltage
V_{OH}	Output high voltage
P	Power Input/Output
DDC	Display Data Channel
PCIE	PCI Express®
SATA	Serial ATA
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

9.1 Connector Signal Descriptions

Table 23 Primary Connector (J1) Pinout

Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A01	VCC	B01	VCC	C01	VCC	D01	VCC
A02	VCC	B02	PWRBTN#	C02	RSTBTN#	D02	VCC
A03	VCC	B03	VCC	C03	VCC	D03	VCC
A04	VCC	B04	THERMTRIP#	C04	CARRIER_HOT#	D04	VCC
A05	RAPID_SHUTDOWN	B05	CAN_TX [1]	C05	CAN_RX [1]	D05	PLTRST#
A06	FUSA_SPI_ALERT [1]	B06	TAMPER#	C06	VIN_PWR_OK	D06	FUSA_SPI_CS# [1]
A07	FUSA_STATUS0 [1]	B07	PROCHOT#	C07	CATERR#	D07	FUSA_SPI_CLK [1]
A08	FUSA_STATUS1 [1]	B08	SUS_S3#	C08	SUS_S4_S5#	D08	FUSA_SPI_MISO [1]
A09	PCIe_PERST_IN0#	B09	FUSA_VOLTAGE_ERR# [1]	C09	FUSA_ALERT# [1]	D09	FUSA_SPI_MOSI [1]
A10	GND	B10	WD_STROBE#	C10	BATLOW#	D10	WAKE0#
A11	PCIe_REFCLKIN0-/ PCIe_REFCLK1-	B11	WD_OUT	C11	FAN_PWMOUT	D11	WAKE1#
A12	PCIe_REFCLKIN0+/PCIe_REFCLK1+	B12	GND	C12	FAN_TACHIN	D12	GND
A13	GND	B13	USB5-	C13	GND	D13	USB1-
A14	USB7-	B14	USB5+	C14	USB3-	D14	USB1+
A15	USB7+	B15	GND	C15	USB3+	D15	GND
A16	GND	B16	USB4-	C16	GND	D16	USB0-
A17	USB6-	B17	USB4+	C17	USB2-	D17	USB0+
A18	USB6+	B18	GND	C18	USB2+	D18	GND
A19	GND	B19	I2S0_LRCLK/SNDW_CLK3/HDA_SYNC	C19	GND	D19	SS01_SDA_AUX-
A20	SS23_SDA_AUX-	B20	I2S0_DOUT/SNDW_DAT3/HDA_SDO	C20	I2S1_CLK/SNDW_DMIC_CLK1	D20	SS01_SCL_AUX+
A21	SS23_SCL_AUX+	B21	I2S_MCLK/HDA_RST#	C21	I2S1_DOUT/ SNDW_DMIC_DAT1	D21	GND
A22	GND	B22	I2S0_DIN/SNDW_DAT2/HDA_SDI	C22	GND	D22	SS0_TX-
A23	SS2_TX-	B23	I2S0_CLK/SNDW_CLK2/HDA_BCLK	C23	I2S1_LRCLK/ SNDW_DMIC_CLK0	D23	SS0_TX+
A24	SS2_TX+	B24	RSVD	C24	I2S1_DIN/ SNDW_DMIC_DAT0	D24	GND
A25	GND	B25	USB67_OC#	C25	GND	D25	SS0_RX-
A26	SS2_RX-	B26	USB45_OC#	C26	USB0_LSRX/DDI1_DDC_AUX_SEL	D26	SS0_RX+
A27	SS2_RX+	B27	USB23_OC#	C27	USB1_LSRX	D27	GND
A28	GND	B28	USB01_OC#	C28	USB0_LSTX/DDI1_HPD	D28	SS1_TX-
A29	SS3_TX-	B29	SML1_CLK	C29	USB1_LSTX	D29	SS1_TX+
A30	SS3_TX+	B30	SML1_DAT	C30	eDP_HPD	D30	GND
A31	GND	B31	PMCALERT#	C31	eDP_VDD_EN	D31	SS1_RX-
A32	SS3_RX-	B32	SML0_CLK	C32	eDP_BKLT_EN	D32	SS1_RX+
A33	SS3_RX+	B33	SML0_DAT	C33	eDP_BKLTCTL	D33	GND

Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A34	GND	B34	USB_PD_ALERT#	C34	GND	D34	ACPRESENT
A35	eDP_AUX-	B35	USB_PD_I2C_CLK	C35	USB3_AUX- [1]	D35	NBASET1_SDP
A36	eDP_AUX+	B36	USB_PD_I2C_DAT	C36	USB3_AUX+ [1]	D36	GND
A37	GND	B37	USB_RT_ENA	C37	GND	D37	SS6_TX-
A38	eDP_TX0-	B38	USB3_LSRX	C38	SS6_RX-	D38	SS6_TX+
A39	eDP_TX0+	B39	USB3_LSTX	C39	SS6_RX+	D39	GND
A40	GND	B40	USB2_LSRX / DDI0_DDC_AUX_SEL	C40	GND	D40	SS7_TX-
A41	eDP_TX1-	B41	USB2_LSTX / DDI0_HPD	C41	SS7_RX-	D41	SS7_TX+
A42	eDP_TX1+	B42	GND	C42	SS7_RX+	D42	GND
A43	GND	B43	USB1_AUX- [1]	C43	GND	D43	SS4_TX-
A44	eDP_TX2-	B44	USB1_AUX+ [1]	C44	SS4_RX-	D44	SS4_TX+
A45	eDP_TX2+	B45	LID#	C45	SS4_RX+	D45	GND
A46	GND	B46	SLEEP#	C46	GND	D46	SS5_TX-
A47	eDP_TX3-	B47	VCC_BOOT_SPI	C47	SS5_RX-	D47	SS5_TX+
A48	eDP_TX3+	B48	BOOT_SPI_CS#	C48	SS5_RX+	D48	GND
A49	GND	B49	BSEL0	C49	GND	D49	NBASET1_MDI0-
A50	eSPI_IO0	B50	BSEL1	C50	BOOT_SPI_IO0	D50	NBASET1_MDI0+
A51	eSPI_IO1	B51	BSEL2	C51	BOOT_SPI_IO1	D51	GND
A52	eSPI_IO2	B52	eSPI_ALERT0#	C52	BOOT_SPI_IO2	D52	NBASET1_MDI1-
A53	eSPI_IO3	B53	eSPI_ALERT1#	C53	BOOT_SPI_IO3	D53	NBASET1_MDI1+
A54	eSPI_CLK	B54	ESPI_CS0#	C54	BOOT_SPI_CLK	D54	GND
A55	GND	B55	eSPI_CS1#	C55	GND	D55	NBASET1_MDI2-
A56	PCIe_CLKREQ0_LO#	B56	eSPI_RST#	C56	PCIe_REFCLK0_HI-	D56	NBASET1_MDI2+
A57	PCIe_CLKREQ0_HI#	B57	PCIe_WAKE_OUT0# [1]	C57	PCIe_REFCLK0_HI+	D57	GND
A58	PCIe_CLKREQ_OUT0#/PCIe_CLKREQ1#	B58	NBASET1_LINK_MID#	C58	GND	D58	NBASET1_MDI3-
A59	NBASET1_LINK_MAX#	B59	NBASET1LINK_ACT#	C59	PCIe_REFCLK0_LO-	D59	NBASET1_MDI3+
A60	NBASET1_CTREF [1]	B60	GND	C60	PCIe_REFCLK0_LO+	D60	GND
A61	GND	B61	PCIe08_RX-	C61	GND	D61	PCIe00_TX-
A62	PCIe08_TX-	B62	PCIe08_RX+	C62	PCIe00_RX-	D62	PCIe00_TX+
A63	PCIe08_TX+	B63	GND	C63	PCIe00_RX+	D63	GND
A64	GND	B64	PCIe09_RX-	C64	GND	D64	PCIe01_TX-
A65	PCIe09_TX-	B65	PCIe09_RX+	C65	PCIe01_RX-	D65	PCIe01_TX+
A66	PCIe09_TX+	B66	GND	C66	PCIe01_RX+	D66	GND
A67	GND	B67	PCIe10_RX-	C67	GND	D67	PCIe02_TX-/(SGMII1_TX-) [3]
A68	PCIe10_TX-	B68	PCIe10_RX+	C68	PCIe02_RX-/(SGMII1_RX-) [3]	D68	PCIe02_TX+/(SGMII1_TX+)[3]
A69	PCIe10_TX+	B69	GND	C69	PCIe02_RX+/(SGMII1_RX+) [3]	D69	GND

Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A70	GND	B70	PCIe11_RX-	C70	GND	D70	PCIe03_TX-/(SGMII0_TX-) [3]
A71	PCIe11_TX-	B71	PCIe11_RX+	C71	PCIe03_RX-/(SGMII0_RX-) [3]	D71	PCIe03_TX+/(SGMII0_TX+) [3]
A72	PCIe11_TX+	B72	GND	C72	PCIe03_RX+/(SGMII0_RX+) [3]	D72	GND
A73	GND	B73	PCIe12_RX-	C73	GND	D73	PCIe04_TX-
A74	PCIe12_TX-	B74	PCIe12_RX+	C74	PCIe04_RX-	D74	PCIe04_TX+
A75	PCIe12_TX+	B75	GND	C75	PCIe04_RX+	D75	GND
A76	GND	B76	PCIe13_RX-	C76	GND	D76	PCIe05_TX-
A77	PCIe13_TX-	B77	PCIe13_RX+	C77	PCIe05_RX-	D77	PCIe05_TX+
A78	PCIe13_TX+	B78	GND	C78	PCIe05_RX+	D78	GND
A79	GND	B79	PCIe14_RX-	C79	GND	D79	PCIe06_TX-/SATA1_TX- [2]
A80	PCIe14_TX-	B80	PCIe14_RX+	C80	PCIe06_RX-/SATA1_RX- [2]	D80	PCIe06_TX+/SATA1_TX+ [2]
A81	PCIe14_TX+	B81	GND	C81	PCIe06_RX+/SATA1_RX+ [2]	D81	GND
A82	GND	B82	PCIe15_RX-	C82	GND	D82	PCIe07_TX-/SATA0_TX- [2]
A83	PCIe15_TX-	B83	PCIe15_RX+	C83	PCIe07_RX-/SATA0_RX- [2]	D83	PCIe07_TX+/SATA0_TX+ [2]
A84	PCIe15_TX+	B84	GND	C84	PCIe07_RX+/SATA0_RX+ [2]	D84	GND
A85	GND	B85	TEST#	C85	GND	D85	NBASET0_MDI0-
A86	VCC_RTC	B86	RSMRST_OUT#	C86	SMB_CLK / I2C3_CLK	D86	NBASET0_MDI0+
A87	SUS_CLK	B87	UART1_TX	C87	SMB_DAT / I2C3_DAT	D87	GND
A88	GPIO_00	B88	UART1_RX	C88	SMB_ALERT# / I2C3_ALERT#	D88	NBASET0_MDI1-
A89	GPIO_01	B89	UART1_RTS#	C89	UART0_TX	D89	NBASET0_MDI1+
A90	GPIO_02	B90	UART1_CTS#	C90	UART0_RX	D90	GND
A91	GPIO_03 / WLAN_MGMT_CLK	B91	I2C2_CLK/ETH_MDIO_CLK	C91	UART0_RTS#	D91	NBASET0_MDI2-
A92	GPIO_04 / WLAN_MGT_DAT	B92	I2C2_DAT/ETH_MDIO_DAT	C92	UART0_CTS#	D92	NBASET0_MDI2+
A93	GPIO_05 / WLAN_MGMT_INT_RST#	B93	GP_SPI_MOSI	C93	I2C0_CLK	D93	GND
A94	GPIO_06 / WIRELESS_DISABLE1#	B94	GP_SPI_MISO	C94	I2C0_DAT	D94	NBASET0_MDI3-
A95	GPIO_07 / WIRELESS_DISABLE2#	B95	GP_SPI_CS0#	C95	I2C0_ALERT#	D95	NBASET0_MDI3+
A96	GPIO_08 / WWAN_DISABLE#	B96	GP_SPI_CS1#	C96	I2C1_CLK	D96	GND
A97	GPIO_09 / WWAN_FCP_OFF#	B97	GP_SPI_CS2#	C97	I2C1_DAT	D97	NBASET0_LINK_MAX#
A98	GPIO_10 / WWAN_RST#	B98	GP_SPI_CS3#	C98	NBASET0_SDP	D98	NBASET0_LINK_MID#
A99	GPIO_11 / WWAN_PERST#	B99	GP_SPI_CLK	C99	NBASET0_CTREF [1]	D99	NBASET0_LINK_ACT#
A100	PINOUT_TYPE0 [1]	B100	GP_SPI_ALERT#	C100	PINOUT_TYPE1 [1]	D100	PINOUT_TYPE2 [1]

Note

1. *Not connected*
2. *SATA interface is not supported*
3. *SGMII is not supported*

Table 24 NBASE-T Ethernet Signal Descriptions

<table>
<tr><th>Gigabit Ethernet</th><th>Pin #</th><th>Description</th><th>I/O</th><th>PU/PD</th><th>Comment</th></tr>
<tr><td>NBASET0_MDI0+
NBASET0_MDI0-
NBASET0_MDI1+
NBASET0_MDI1-
NBASET0_MDI2+
NBASET0_MDI2-
NBASET0_MDI3+
NBASET0_MDI3-</td><td>D86
D85
D89
D88
D92
D91
D95
D94</td><td>Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 2.5 Gbps, 1 Gbps, 100 Mbps and 10 Mbps modes.
Some pairs are unused in some modes, per the following:

<table><tr><th></th><th>2.5GBASE-T
1GBASE-T</th><th>100BASE-TX</th><th>10BASE-T</th></tr><tr><td>MDI[0]+/-</td><td>B1_DA+/-</td><td>TX+/-</td><td>TX+/-</td></tr><tr><td>MDI[1]+/-</td><td>B1_DB+/-</td><td>RX+/-</td><td>RX+/-</td></tr><tr><td>MDI[2]+/-</td><td>B1_DC+/-</td><td></td><td></td></tr><tr><td>MDI[3]+/-</td><td>B1_DD+/-</td><td></td><td></td></tr></table></td><td>I/O MDI
3.3 VSB</td><td></td><td>The conga-HPC/mPTL supports up to 2.5 Gbps.</td></tr>
<tr><td>NBASET1_MDI0+
NBASET1_MDI0-
NBASET1_MDI1+
NBASET1_MDI1-
NBASET1_MDI2+
NBASET1_MDI2-
NBASET1_MDI3+
NBASET1_MDI3-</td><td>D50
D49
D53
D52
D56
D55
D59
D58</td><td>Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in modes up to 2.5Gbps. Some pairs are unused in some modes, per the following:</td><td>I/O MDI
3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_ACT#
NBASET1LINK_ACT#</td><td>D99
B59</td><td>NBASE-T Ethernet Controller activity indicator, active low.
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_MAX#
NBASET1_LINK_MAX#</td><td>D97
A59</td><td>NBASE-T Ethernet Controller MAX Speed Link indicator, active low. If active, the link is established at the maximum speed that the Ethernet controller is capable of (which may be 10G, 5G, 2.5G etc).
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_MID#
NBASET1_LINK_MID#</td><td>D98
B58</td><td>NBASE-T Ethernet Controller MID Speed Link indicator, active low. If active, the link is established but at a speed lower than what the maximum speed that the Ethernet controller is capable of.
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_CTREF
NBASET1_CTREF</td><td>C99
A60</td><td>Reference voltage for Carrier Board NBASET Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V.

If not needed, these pins may be left open on the Carrier. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.</td><td>REF</td><td></td><td>Not Connected</td></tr>
<tr><td>NBASET0_SDP
NBASET1_SDP</td><td>C98
D35</td><td>NBASE-T Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.</td><td>I/O 3.3 VSB</td><td></td><td></td></tr>
</table>

Table 25 PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIe00_TX+ PCIe00_TX-	D62 D61	PCI Express Transmit Output Differential Pairs 0	O PCIE		PCIe Gen 4
PCIe00_RX+ PCIe00_RX-	C63 C62	PCI Express Receive Input Differential Pairs 0	I PCIE		
PCIe01_TX+ PCIe01_TX-	D65 D64	PCI Express Transmit Output Differential Pairs 1	O PCIE		PCIe Gen 4
PCIe01_RX+ PCIe01_RX-	C66 C65	PCI Express Receive Input Differential Pairs 1	I PCIE		
PCIe02_TX+/SGMII1_TX+ PCIe02_TX-/SGMII1_TX	D68 D67	PCI Express Transmit Output Differential Pairs 2	O PCIE		PCIe Gen 4 SGMII is not supported
PCIe02_RX+/SGMII1_RX+ PCIe02_RX-/SGMII1_RX	C69 C68	PCI Express Receive Input Differential Pairs 2	I PCIE		
PCIe03_TX+/SGMII0_TX+ PCIe03_TX-/SGMII0_TX-	D71 D70	PCI Express Transmit Output Differential Pairs 3	O PCIE		PCIe Gen 4 SGMII is not supported
PCIe03_RX+/SGMII0_RX+ PCIe03_RX-/SGMII0_RX	C72 C71	PCI Express Receive Input Differential Pairs 3	I PCIE		
PCIe04_TX+ PCIe04_TX-	D74 D73	PCI Express Transmit Output Differential Pairs 4	O PCIE		PCIe Gen 5
PCIe04_RX+ PCIe04_RX-	C75 C74	PCI Express Receive Input Differential Pairs 4	I PCIE		
PCIe05_TX+ PCIe05_TX-	D77 D76	PCI Express Transmit Output Differential Pairs 5	O PCIE		PCIe Gen 5
PCIe05_RX+ PCIe05_RX-	C78 C77	PCI Express Receive Input Differential Pairs 5	I PCIE		
PCIe06_TX+/SATA1_TX+ PCIe06_TX-/SATA1_TX-	D80 D79	PCI Express Transmit Output Differential Pairs 6 Serial ATA channel 1, Transmit Output differential pair	O PCIE/SATA		PCIe Gen 5
PCIe06_RX+/SATA1_RX+ PCIe06_RX-/SATA1_RX-	C81 C80	PCI Express Receive Input Differential Pairs 6 Serial ATA channel 1, Receive Input differential pair	I PCIE/SATA		
PCIe07_TX+/SATA0_TX+ PCIe07_TX-/SATA0_TX-	D83 D82	PCI Express Transmit Output Differential Pairs 7 Serial ATA channel 0, Transmit Output differential pair	O PCIE/SATA		PCIe Gen 5
PCIe07_RX+/SATA0_RX+ PCIe07_RX-/SATA0_RX-	C84 C83	PCI Express Receive Input Differential Pairs 7 Serial ATA channel 0, Receive Input differential pair	I PCIE/SATA		
PCIe08_TX+ PCIe08_TX-	A63 A62	PCI Express Transmit Output Differential Pairs 8	O PCIE		PCIe Gen 5
PCIe08_RX+ PCIe08_RX-	B62 B61	PCI Express Receive Input Differential Pairs 8	I PCIE		
PCIe09_TX+ PCIe09_TX-	A66 A65	PCI Express Transmit Output Differential Pairs 9	O PCIE		
PCIe09_RX+ PCIe09_RX-	B65 B64	PCI Express Receive Input Differential Pairs 9	I PCIE		

PCIe10_TX+ PCIe10_TX-	A69 A68	PCI Express Transmit Output Differential Pairs 10	O PCIE		PCIe Gen 5
PCIE10_RX+ PCIE10_RX-	B68 B67	PCI Express Receive Input Differential Pairs 10	I PCIE		
PCIE11_TX+ PCIE11_TX-	A72 A71	PCI Express Transmit Output Differential Pairs 11	O PCIE		
PCIE11_RX+ PCIE11_RX-	B71 B70	PCI Express Receive Input Differential Pairs 11	I PCIE		
PCIE12_TX+ PCIE12_TX-	B75 A74	PCI Express Transmit Output Differential Pairs 12	O PCIE		
PCIE12_RX+ PCIE12_RX-	B74 B73	PCI Express Receive Input Differential Pairs 12	I PCIE		
PCIE13_TX+ PCIE13_TX-	A78 A77	PCI Express Transmit Output Differential Pairs 13	O PCIE		
PCIE13_RX+ PCIE13_RX-	B77 B76	PCI Express Receive Input Differential Pairs 13	I PCIE		
PCIE14_TX+ PCIE14_TX-	A81 A80	PCI Express Transmit Output Differential Pairs 14	O PCIE		
PCIE14_RX+ PCIE14_RX-	B80 B79	PCI Express Receive Input Differential Pairs 14	I PCIE		
PCIE15_TX+ PCIE15_TX-	A84 A83	PCI Express Transmit Output Differential Pairs 15	O PCIE		
PCIE15_RX+ PCIE15_RX-	B83 B82	PCI Express Receive Input Differential Pairs 15	I PCIE		
PCIe_REFCLK0_LO+ PCIe_REFCLK0_LO-	C60 C59	Reference clock pair for PCIe lanes [0:7], also referred to as PCIe Group 0 Low	O LV_DIFF		
PCIe_REFCLK0_HI+ PCIe_REFCLK0_HI-	C57 C56	Reference clock pair for PCIe lanes [8:15] also referred to as PCIe Group 0 High	O LV_DIFF		
PCIe_CLKREQ0_LO#	A56	PCIe reference clock request signal from Carrier devices for PCIe_REFCLK0_LO clock pair	Bi-Dir OD 1.8V	PU 10 KΩ 1.8 V	
PCIe_CLKREQ0_HI#	A57	PCIe reference clock request signal from Carrier devices for PCIe_REFCLK0_HI clock pair	Bi-Dir OD 1.8V	PU 10 KΩ 1.8 V	
PCI Express Additional Signals to Support Module-based PCIe Targets					
PCIe_REFCLKIN0+ / PCIe_REFCLK1+	A12	Reference clock inputs allowing Carrier based root to operate with Module based PCIe targets. The Module designer making use of these clocks should terminate them in a way appropriate to that design. Alternate Use: Output reference clock 1.	I LV_DIFF		PCIe Target not supported. Used as PCIe REFCLK1+/- according to the COM-HPC® rev. 1.30.
PCIe_REFCLKIN0-/ PCIe_REFCLK1-	A11				
PCIe_WAKE_OUT0#	B57	Wake request signal from Module based PCIe Target to an off-Module PCIe Root complex.	OD 1.8VSB		Not Connected
PCIe_PERST_IN0#	A09	Reset signals into Module to reset Module PCIe Targets.	I 1.8V	PD 100 KΩ	PCIe Target not supported
PCIe_CLKREQ_OUT0# / PCIe_CLKREQ1#	A58	PCIe reference clock request signal from Module target PCIe device to an off-Module PCIe root device. Alternate Use: PCIe reference clock request signal from Carrier target devices for PCIe_REFCLK1 clock pair.	Bi-Dir OD 1.8 V	PU 10 KΩ 1.8 V	PCIe Target not supported. Used as PCIe CLKREQ1# according to the COM-HPC® rev. 1.30.

Note

1. *conga-HPC mPTL does not support 4 individual x1 links on COM-HPC® PCIe4-PCIe7.*
2. *Default link configurations for PCIe0 - PCIe3 are individual x1 links.*
3. *PCIe4- PCIe7, PCIe8 - PCIe11, PCIe12 - PCIe15 are individual x4 links by default.*
4. *Customized link configurations may require a customized BIOS.*

Table 26 USB Signal Descriptions

USB	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	D17 D16	USB 2.0 differential pairs, channels 0 through 7. USB0 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports.	I/O USB 2.0		
USB1+ USB1-	D14 D13		I/O USB 2.0		
USB2+ USB2-	C18 C17		I/O USB 2.0		
USB3+ USB3-	C15 C14		I/O USB 2.0		
USB4+ USB4-	B17 B16		I/O USB 2.0		
USB5+ USB5-	B14 B13		I/O USB 2.0		
USB6+ USB6-	A18 A17		I/O USB 2.0		
USB7+ USB7-	A15 A14		I/O USB 2.0		
SS0_TX+ SS0_TX-	D23 D22	Signals configured for DDI0. USB4 is not supported.	O USB SS		DC coupled on Module Shall be AC coupled on Carrier or off Module
SS0_RX+ SS0_RX-	D26 D25		I USB SS		
SS1_TX+ SS1_TX-	D29 D28		O USB SS		
SS1_RX+ SS1_RX-	D32 D31		I USB SS		

SS2_TX+ SS2_TX-	A24 A23	Signals configured for USB4_0 by default. With an optional BIOS, DDI1 can be supported instead.	O USB SS		DC coupled on Module Shall be AC coupled on Carrier or off Module
SS2_RX+ SS2_RX-	A27 A26		I USB SS		
SS3_TX+ SS3_TX-	A30 A29		O USB SS		
SS3_RX+ SS3_RX-	A33 A32		I USB SS		
SS4_TX+ SS4_TX-	D44 D43	Signals configured for USB3.2 Gen 2x1 ports	O USB SS		
SS4_RX+ SS4_RX-	C45 C44		I USB SS		
SS5_TX+ SS5_TX-	D47 D46	Signals configured for USB3.2 Gen 2x1 ports	O USB SS		
SS5_RX+ SS5_RX-	C48 C47		I USB SS		
SS6_TX+ SS6_TX-	D38 D37	Signals configured for USB3.2 Gen 2x1 ports	O USB SS		
SS6_RX+ SS6_RX-	C39 C38		I USB SS		
SS7_TX+ SS7_TX-	D41 D40	Signals configured for USB3.2 Gen 2x1 ports	O USB SS		
SS7_RX+ SS7_RX-	C42 C41		I USB SS		
USB01_OC#	B28	USB over-current sense, USB 2.0 channels 0,1; channels 2,3; channels 4,5 and channels 6,7 respectively. A pull-up for each of these lines to the 1.8V Suspend rail shall be present on the Mini Module. The pull-up should be 10 KΩ. An open drain driver from USB current monitors on the Carrier Board may drive this line low. The Carrier Board shall not pull these lines up. Note that the over-current limits for USB 2.0 and USB 3.0 are different; this is a Carrier board implementation item.	I 1.8 VSB	PU 10 KΩ 1.8 VSB	
USB23_OC#	B27		I 1.8 VSB	PU 10 KΩ 1.8 VSB	
USB45_OC#	B26		I 1.8 VSB	PU 10 KΩ 1.8 VSB	
USB67_OC#	B25		I 1.8 VSB	PU 10 KΩ 1.8 VSB	
RSMRST_OUT#	B86	USB devices that are to be powered in the S5 / S4 / S3 Suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the hi state.	O 1.8 VSB	PD 100 KΩ	

Note

For information about implementing USB4®, DDI, USB 3.2 and USB 2.0 interfaces, refer to the COM-HPC® Module Base Specification Revision 1.30 and COM-HPC® Carrier Design Guide.

Table 27 USB4 Sideband Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SS01_SDA_AUX- SS01_SCL_AUX+	D19 D20	DisplayPort Aux channel USB4 Aux channel Display Data Channel (DDC)	LV_DIFF I/O OD 1.8 V		
USB1_AUX- USB1_AUX+	B43 B44	USB4 Aux channel	LV_DIFF		Not connected
SS23_SDA_AUX- SS23_SCL_AUX+	A20 A21	DisplayPort Aux channel USB4 Aux channel Display Data Channel (DDC)	LV_DIFF I/O OD 1.8 V		
USB3_AUX- USB3_AUX+	C35 C36	USB4 Aux channel	LV_DIFF		Not connected
USB0_LSTX	C28	Sideband TX interfaces for USB4 Alternate modes "Low Speed" asynchronous serial TX lines	O 1.8 V	PD 1 MΩ	
USB1_LSTX	C29		O 1.8 V	PD 1 MΩ	Not supported
USB2_LSTX	B41		O 1.8 V		Not supported
USB3_LSTX	B39		O 1.8 V	PD 1 MΩ	Not supported
USB0_LSRX	C26	Sideband RX interfaces for USB4 Alternate modes "Low Speed" asynchronous serial RX lines	I 1.8 V	PD 1 MΩ	
USB1_LSRX	C27		I 1.8 V	PD 1 MΩ	Not supported
USB2_LSRX	B40		I 1.8 V		Not supported
USB3_LSRX	B38		I 1.8 V	PD 1 MΩ	Not supported

Note

For information about implementing USB4®, DDI, USB 3.2 and USB 2.0 interfaces, refer to the COM-HPC® Module Base Specification Revision 1.30 and COM-HPC® Carrier Design Guide.

Table 28 USB4 Configuration Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SML0_DAT	B33	Data line for I2C data based System Management Links between chipset masters and Carrier. SML0 is used to control the Carrier based USB re-timers. SML1 controls the Carrier based USB Power Delivery Controller.	Bi-Dir OD 1.8 VSB	PU 1 KΩ 1.8 VSB	
SML1_DAT	B30		Bi-Dir OD 1.8 VSB	PU 1 KΩ 1.8 VSB	
SML0_CLK	B32	Clock lines for System Management Links 0 and 1. SML0 is used to support Carrier USB4 re-timers SML1 is used to support Carrier USB Power Delivery (PD) Controller.	Bi-Dir OD 1.8 VSB	PU 1 KΩ 1.8 VSB	
SML1_CLK	B29		Bi-Dir OD 1.8 VSB	PU 1 KΩ 1.8	
PMCALERT#	B31	Active low Alert signal associated with the SML1 System Management link, from the Carrier based USB Power Delivery Controller.	I 1.8 V	PU 10 KΩ 1.8 VSB	
USB_RT_ENA	B37	Power Enable for Carrier based USB Retimers. Sourced from chipset GPO. "USB Re-Timer Enable".	O 1.8 V	PD 100 KΩ	
USB_PD_I2C_DAT	B36	I2C data line between Module based Embedded Controller master and Carrier based USB Power Delivery Controller slave.	Bi-Dir OD 1.8 VSB	PU 1 KΩ 1.8 VSB	
USB_PD_I2C_CLK	B35	I2C clock line between Module based Embedded Controller master and Carrier based USB Power Delivery Controller slave.	Bi-Dir OD 1.8 VSB	PU 1 KΩ 1.8 VSB	
USB_PD_ALERT#	B34	Active low Alert signal from USB Power Delivery Controller to the Module Embedded Controller.	I 1.8 VSB	PU 10 KΩ 1.8 VSB	
Additional Signals to Support USB4® Implementation					
PLTRST#	D05	Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.	O 1.8 VSB	PD 100 KΩ	
SUS_S4_S5#	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 1.8 VSB	PD 100 KΩ	

Note

For information about implementing USB4®, DDI, USB 3.2 and USB 2.0 interfaces, refer to the COM-HPC® Module Base Specification Revision 1.30 and COM-HPC® Carrier Design Guide.

Table 29 eSPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eSPI_IO0 eSPI_IO1 eSPI_IO2 eSPI_IO3	A50 A51 A52 A53	eSPI Master Data Input / Outputs. These are bi-directional input/output pins used to transfer data between master and slaves.	I/O 1.8 VSB		
eSPI_CS0#	B54	eSPI Master Chip Select Outputs. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select pin. If an eSPI_CSx# pins is not in use, it shall be either pulled high or actively driven high.	O 1.8 VSB		
eSPI_CS1#	B55		O 1.8 VSB		
eSPI_CLK	A54	eSPI Master Clock Output. This pin provides the reference timing for all the serial input and output operations.	O 1.8 VSB		
eSPI_ALERT0#	B52	eSPI pins used by eSPI slave to request service from the eSPI master.	I 1.8 VSB	PU 10 KΩ 1.8 VSB	
eSPI_ALERT1#	B53		I 1.8 VSB	PU 10 KΩ 1.8 VSB	
eSPI_RST#	B56	eSPI Reset - resets the eSPI interface for both master and slaves. eSPI_RST# is typically driven from the eSPI master to eSPI slaves.	O 1.8 VSB		

Table 30 Boot SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
BOOT_SPI_CS#	B48	Chip select for Carrier Board SPI If the BOOT_SPI_CS# pin is not in use, it shall be either pulled high or actively driven high.	O VCC_BOOT_SPI	PU 3.22 KΩ 1.8 VSB	
BOOT_SPI_IO0	C50	Bidirectional 4 bit data path out of and into a Carrier SPI flash operating in Serial Quad Interface (SQI) mode. If the flash memory device is operating in traditional Serial Peripheral Interface (SPI) mode, then signal BOOT_SPI_IO0 is used for getting serial data into the flash device (referred to as SI or MOSI in SPI Flash data sheets) and signal BOOT_SPI_IO1 is used to get serial data from the flash device (referred to as SO or MISO in flash data sheets)	I/O VCC_BOOT_SPI		
BOOT_SPI_IO1	C51				
BOOT_SPI_IO2	C52			PU 10 KΩ 1.8 VSB	
BOOT_SPI_IO3	C53			PU 10 KΩ 1.8 VSB	
BOOT_SPI_CLK	C54	Clock from Module chipset to Carrier SPI	O VCC_BOOT_SPI		
VCC_BOOT_SPI	B47	Power supply for Carrier Board SPI – sourced from Module – nominally 1.8 V or 3.3 V. The Module shall provide a minimum of 100 mA on VCC_BOOT_SPI. Carriers shall use less than 100 mA from this power source. VCC_BOOT_SPI shall only be used to power SPI devices on the Carrier Board. The Module vendor may choose what power domains the BOOT_SPI is active in.	Power (Out from Module)		1.8 VSB (active in suspend state)

Table 31 BIOS Select Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
BSEL2	B51	Boot Select pins. These pins distinguish between an SPI or eSPI BIOS boot and between an on-Module or off-Module BIOS. Pulled up on Module to vendor specific power rail.	I 1.8 VSB	PU 10 KΩ 1.8 VSB	Pulled up to 1.8 VSB (active in suspend state)
BSEL1	B50		I 1.8 VSB	PU 10 KΩ 1.8 VSB	
BSEL0	B49		I 1.8 VSB	PU 10 KΩ 1.8 VSB	

Table 32 DDI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI0_PAIR0+ DDI0_PAIR0-	D23 D22	Digital Display Interface 0 differential pair 0	O LV_DIFF		
DDI0_PAIR1+ DDI0_PAIR1-	D26 D25	Digital Display Interface 0 differential pair 1	O LV_DIFF		
DDI0_PAIR2+ DDI0_PAIR2-	D29 D28	Digital Display Interface 0 differential pair 2	O LV_DIFF		
DDI0_PAIR3+ DDI0_PAIR3-	D32 D31	Digital Display Interface 0 differential pair 3	O LV_DIFF		
DDI1_PAIR0+ DDI1_PAIR0-	A24 A23	Digital Display Interface 1 differential pair 0	O LV_DIFF		
DDI1_PAIR1+ DDI1_PAIR1-	A27 S26	Digital Display Interface 1 differential pair 1	O LV_DIFF		
DDI1_PAIR2+ DDI1_PAIR2-	A30 A29	Digital Display Interface 1 differential pair 2	O LV_DIFF		
DDI1_PAIR3+ DDI1_PAIR3-	A33 A32	Digital Display Interface 1 differential pair 3	O LV_DIFF		
DDI0_DDC_AUX_SEL DDI1_DDC_AUX_SEL	B40 C26	Selects the function of DDI[0:1]_SCL_AUX+ and DDI[0:1]_SDA_AUX-. If this input is unconnected on the Carrier, the AUX pair is used for the DP AUX+/- signals. If pulled or driven high on the Carrier, the AUX pair contains the SCL and SDA Display Data Channel (DDC) signals	I 1.8 V	PD 1 MΩ	
DDI0_SCL_AUX+ DDI1_SCL_AUX+	D20 A21	DP AUX+ function if DDI[0:1]_DDC_AUX_SEL is a no connect or driven to GND on the Carrier.	I/O LV_DIFF		
		SCL Display Data Channel (DDC) if DDI[0:1]_DDC_AUX_SEL is pulled or driven high on the Carrier.	I/O OD 1.8 V		PU 2k15 in case of SCL
DDI0_SDA_AUX- DDI1_SDA_AUX-	D19 A20	DP AUX- function if DDI[0:1]_DDC_AUX_SEL is no connect.	I/O LV_DIFF		
		SDA Display Data Channel (DDC) if DDI[0:1]_DDC_AUX_SEL is pulled high.	I/O OD 1.8 V		PU 2k15 in case of SDA
DDI0_HPD DDI1_HPD	B41 C28	DDI Hot-Plug Detect	I 1.8 V	PD 100 KΩ	

Note

1. *For information about implementing USB4®, DDI, USB 3.2 and USB 2.0 interfaces, refer to the COM-HPC® Module Base Specification Revision 1.30 and COM-HPC® Carrier Design Guide.*

2. *Super Speed (SS) lanes 0 and 1 are utilized by DDI0. SS lanes 2 and 3 may be utilized by DDI1 depending on the SS lane configuration.*

3. *DDI1 is only available if the SS lanes 2 and 3 supports DD1 as per the SS lane configuration.*

Table 33 eDP Embedded DisplayPort / MIPI DSI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eDP_TX0+ eDP_TX0-	A39 A38	eDP / DSI differential data pairs Multiplexed with DSI_TX1+ and DSI_TX1-	O LV_DIFF		
eDP_TX1+ eDP_TX1-	A42 A41	eDP / DSI differential data pairs Multiplexed with DSI_TX2+ and DSI_TX2-	O LV_DIFF		
eDP_TX2+ eDP_TX2-	A45 A44	eDP differential data pair DSI differential clock pair Multiplexed with DSI_CLK+ and DSI_CLK-	O LV_DIFF		
eDP_TX3+ eDP_TX3-	A48 A47	eDP / DSI differential data pairs Multiplexed with DSI_TX3+ and DSI_TX3-	O LV_DIFF		
eDP_AUX+ eDP_AUX-	A36 A35	eDP AUX channel differential pair DSI differential data pair Multiplexed with DSI_TX0+ and DSI_TX0-	I/O LV_DIFF		
eDP_VDD_EN	C31	eDP / DSI power enable Multiplexed with DSI_VDD_EN	O 1.8 V	PD 100 KΩ	
eDP_BKLT_EN	C32	eDP / DSI backlight enable Multiplexed with DSI_BKLT_EN	O 1.8 V	PD 100 KΩ	
eDP_BKLT_CTRL	C33	EDP / DSI backlight brightness control Multiplexed with DSI_BKLT_CTRL	O 1.8 V	PD 100 KΩ	
eDP_HPD	C30	eDP: Detection of Hot Plug / Unplug and notification of the link layer Multiplexed with DSI_TE DSI: Tearing Effect Input: this is an optional signal from the DSI display (that has it's own display controller and frame buffer) coordinating with the host display controller.	I 1.8 V	PD 100 KΩ	

Note

1. *MIPI DSI is not supported.*

2. *Supports up to eDP 1.4b / 1.5 (HBR3) and maximum resolution up to 4K120Hz HDR.*

Table 34 Soundwire Audio Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SNDW_DMIC_DAT0	C24	Bi-directional PCM audio data	I/O 1.8 VSB		
SNDW_DMIC_DAT1	C21	Bi-directional PCM audio data	I/O 1.8 VSB		
SNDW_DMIC_CLK0	C23	Clock for Soundwire transactions	O 1.8 VSB		
SNDW_DMIC_CLK1	C20	Clock for Soundwire transactions	O 1.8 VSB		

Table 35 I2S / Soundwire / HDA Audio Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2S0_CLK/ SNDW_CLK2/ HDA_BITCLK	B23	I2S0 Clock Alternative use as Soundwire 2 clock or Serial data clock generated by the external HDA codec	O 1.8 V		
I2S0_DIN/ SNDW_DAT2/ HDA_SDIN	B22	I2S0 Data In. This pin is an input in I2S mode. Alternative use as bi-directional Soundwire 2 data lane or Serial TDM data input	I/O 1.8 V		
I2S0_DOUT/ SNDW_DAT3/ HDA_SDO	B20	I2S0 Data Out. This pin is an input in I2S mode Alternative use as bi-directional Soundwire 2 data lane or Serial TDM data output to the codec	I/O 1.8 V	PD 100 KΩ	PD is only relevant if HDA or I2S is being used
I2S0_LRCLK/ SNDW_CLK3/ HDA_SYNC	B19	I2S0 L/R Clock Alternative use as Soundwire 3 clock or Sample-synchronization signal to the codec	O 1.8 V		
I2S_MCLK/ HDA_RST#	B21	I2S Master Clock Alternative use as Reset output to codec; active low	O 1.8 V		

Note

The I2S interface is not verified because the relevant drivers are currently not available. For a verified audio interface, we recommend to use HDA.

Table 36 Asynchronous Serial Port Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
UART0_TX	C89	Logic level asynchronous serial port transmit signal	O 1.8 VSB		
UART0_RX	C90	Logic level asynchronous serial port receive signal	I 1.8 VSB	PU 47.5 KΩ 1.8 VSB	
UART0_RTS#	C91	Logic level asynchronous serial port Request to Send signal, active low	O 1.8 VSB		
UART0_CTS#	C92	Logic level asynchronous serial port Clear to Send input, active low	I 1.8 VSB	PU 47.5 KΩ 1.8 VSB	
UART1_TX	B87	Logic level asynchronous serial port transmit signal	O 1.8 VSB		
UART1_RX	B88	Logic level asynchronous serial port receive signal	I 1.8 VSB	PU 47.5 KΩ 1.8 VSB	
UART1_RTS#	B89	Logic level asynchronous serial port Request to Send signal, active low	O 1.8 VSB		
UART1_CTS#	B90	Logic level asynchronous serial port Clear to Send input, active low	I 1.8 VSB	PU 47.5 KΩ 1.8 VSB	

Table 37 I2C Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C0_CLK	C93	Clock I/O line for the general purpose I2C0 port	I/O OD 1.8 VSB	PU 1 KΩ 1.8 VSB	
I2C0_DAT	C94	Data I/O line for the general purpose I2C0 port	I/O OD 1.8 VSB	PU 1 KΩ 1.8 VSB	
I2C0_ALERT#	C95	Alert input / interrupt for I2C0	I 1.8 VSB	PU 2.15 KΩ 1.8 VSB	
I2C1_CLK	C96	Clock I/O line for the general purpose I2C1 port	I/O OD 1.8 VSB	PU 1 KΩ 1.8 VSB	
I2C1_DAT	C97	Data I/O line for the general purpose I2C1 port	I/O OD 1.8 VSB	PU 1 KΩ 1.8 VSB	
I2C2_CLK/ ETH_MDIO_CLK	B91	Clock I/O line for the general purpose I2C2 port or for MDIO clock to support Mini Module SGMII0 and SGMII1 operation	I/O OD 1.8 VSB	PU 1 KΩ 1.8 VSB	
I2C2_DAT/ ETH_MDIO_DAT	B92	Data I/O line for the general purpose I2C2 port or for MDIO data to support Mini Module SGMII0 and SGMII1 operation	I/O OD 1.8 VSB	PU 1 KΩ 1.8 VSB	

Table 38 General Purpose SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GP_SPI_MISO	B94	Serial data into the COM-HPC® Module from the Carrier GP_SPI device ("Master In Slave Out")	I 1.8 V	PU 100 KΩ 1.8 V	
GP_SPI_MOSI	B93	Serial data from the COM-HPC® Module to the Carrier GP_SPI device ("Master Out Slave In")	O 1.8 V		
GP_SPI_CLK	B99	Clock from the Module to Carrier GP_SPI device	O 1.8 V		
GP_SPI_CS0#	B95	GP_SPI chip selects, active low	O 1.8 V		
GP_SPI_CS1#	B96				
GP_SPI_CS2#	B97			PU 100 KΩ 1.8 V	Not supported
GP_SPI_CS3#	B98			PU 100 KΩ 1.8 V	Not supported
GP_SPI_ALERT#	B100	Alert (interrupt) from a Carrier GP_SPI device to the Module	I 1.8 V	PU 10 KΩ 1.8 V	

Table 39 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B02	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down (with a sustained low).	I 1.8 VSB	PU 100 KΩ 1.8 VSB	
RSTBTN#	C02	Reset button input. The RSTBTN# may be level sensitive (active low) or may be triggered by the falling edge of the signal. The Module PLTRST# signal (below) should not be released (driven or pulled high) while the RSTBTN# is low. For situations when RSTBTN# is not able to reestablish control of the system, VIN_PWR_OK or a power cycle may be used.	I 1.8 VSB	PU 10 KΩ 1.8 VSB	
PLTRST#	D05	Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.	O 1.8 VSB	PD 100 KΩ	
VIN_PWR_OK	C06	Power OK from main power supply. A high value indicates that the power is good.	I 1.8 VSB	PU 100 KΩ 1.8 VSB	
SUS_S3#	B08	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board should be used to enable the non-standby power on a typical ATX supply. Even in single input supply system implementations (AT mode, no standby input), the SUS_S3# Module output should be used to disable any Carrier voltage regulators when SUS_S3# is low, to prevent bleed leakage from Carrier circuits into the Module.	O 1.8 VSB	PD 100 KΩ	
SUS_S4_S5#	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 1.8 VSB	PD 100 KΩ	
SUS_CLK	A87	32.768 kHz +/- 100 ppm clock used by Carrier peripherals such as M.2 cards in their low power modes.	O 1.8 VSB		
WAKE0#	D10	PCI Express wake up signal.	I/O 1.8 VSB	PU 1 KΩ 1.8 VSB	
WAKE1#	D11	General purpose wake up signal. May be used to implement wake- up on PS2 keyboard or mouse activity.	I 1.8 VSB	PU 10 KΩ 1.8 VSB	
BATLOW#	C10	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	I 1.8 VSB	PU 5 KΩ 1.8 VSB	
LID#	B45	LID switch. Low active signal used by the ACPI operating system for a LID switch.	I 1.8 VSB	PU 10 KΩ 1.8 VSB	
SLEEP#	B46	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I 1.8 VSB	PU 100 KΩ 1.8 VSB	

TAMPER#	B06	Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a Tamper event.	I 3.3 VCC_RTC	PU 1 MΩ 3.3 VCC_RTC	
ACPRESENT	D34	Driven hard low on Carrier if system AC power is not present	I 1.8 VSB	PU 10 KΩ 1.8 VSB	
RSMRST_OUT#	B86	This is a buffered copy of the internal Module RSMRST# (Resume Reset, active low) signal. The internal Module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable. USB devices on the Carrier that are to be active in S5 / S3 / S0 should not have their 5V supply applied before RSMRST_OUT# goes high. RSMRST_ OUT# shall be a 3.3V CMOS Module output, active in all power states.	O 1.8 VSB	PD 100 KΩ	

Table 40 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_SHUTDOWN	A05	Trigger for Rapid Shutdown. Must be driven to 5 V though a <= 50 Ω source impedance for ≥ 20 µs. Pull-down / disable on Module if RAPID_SHUTDOWN pin is not asserted.	I 5 VSB	PD 100 KΩ	Not supported

Table 41 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CARRIER_HOT#	C04	Input from off-Module temp sensor indicating an over-temp situation.	I 1.8 V	PU 10 KΩ 1.8 V	
THERMTRIP#	B04	Active low output indicating that the CPU has entered thermal shutdown.	O 1.8 V	PD 100 KΩ	

Table 42 SMBus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CLK	C86	System Management Bus bidirectional clock line.	I/O OD 1.8 VSB	PU 3.2 KΩ 1.8 VSB	
SMB_DAT	C87	System Management Bus bidirectional data line.	I/O OD 1.8 VSB	PU 3.2 KΩ 1.8 VSB	
SMB_ALERT# [1]	C88	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 1.8 VSB	PU 2.15 KΩ 1.8 VSB	

Note

1. *This signal may have a special functionality during the reset process. It may strap some basic important function of the module. For moreinformation refer to section 9.2 "Boot Strap Signals".*

Table 43 General Purpose Input Output Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPIO_00	A88	General purpose input / output pins. Upon a hardware reset, these pins should be configured as inputs. As inputs, these pins should be able to generate an interrupt to the Module host.	I/O 1.8 VSB	PU 100 KΩ 1.8 VSB	
GPIO_01	A89				
GPIO_02	A90				
GPIO_03	A91				
GPIO_04	A92				
GPIO_05	A93				
GPIO_06	A94				
GPIO_07	A95				
GPIO_08	A96				
GPIO_09	A97				
GPIO_10	A98				
GPIO_11	A99				

Table 44 Module Type Definition Signal Description

<table>
<tr><th>Signal</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>TYPE0
TYPE1
TYPE2</td><td>A100
C100
D100</td><td>The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). These pins shall be pulled up on the Carrier, to Carrier standby voltage rail of 5 V or less. Carrier hardware reads the level on these straps.
<table>
<tr><th></th><th colspan="3">Module Connections</th><th rowspan="2">Meaning</th></tr>
<tr><th>Ref</th><th>TYPE2</th><th>TYPE1</th><th>TYPE0</th></tr>
<tr><td>7</td><td>NC</td><td>NC</td><td>NC</td><td>Mini Module – Wide Range 8V to 20V input</td></tr>
<tr><td>6</td><td>NC</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>5</td><td>NC</td><td>GND</td><td>NC</td><td>Reserved</td></tr>
<tr><td>4</td><td>NC</td><td>GND</td><td>GND</td><td>Server module - Fixed 12 V input</td></tr>
<tr><td>3</td><td>GND</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>2</td><td>GND</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>1</td><td>GND</td><td>GND</td><td>NC</td><td>Client module - Wide range 8 V to 20 V input</td></tr>
<tr><td>0</td><td>GND</td><td>GND</td><td>GND</td><td>Client module - Fixed 12 V input</td></tr>
</table>
The module shall implement all three TYPE[x] pins per the table above.
The carrier board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX PS_ON# signal to an ATX power supply or otherwise deactivates VCC to the COM-HPC® Module) if an incompatible Module pin-out type is detected. All three TYPE[x] pins should be monitored by the Carrier. The Carrier Board logic may also implement a fault indicator such as an LED.</td><td>PDS</td><td>The conga-HPC/mPTL is a Ref 7 Type module (Mini Module – Wide Range 8V to 20V input).

Therefore, the TYPE2, TYPE1, and TYPE0 pins are not connected.</td></tr>
</table>

Table 45 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WD_OUT	B11	Output indicating that a watchdog time-out event has occurred. Refer to the COM-HPC® Module Base Specification for details.	O 1.8 V	PD 100 KΩ	
WD_STROBE#	B10	Strobe input to watchdog timer. Periodic strobing prevents the watchdog, if enabled, from timing out.	I 1.8 V	PU 10 KΩ 1.8 V	
FAN_PWMOUT	C11	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O 1.8 V		
FAN_TACHIN	C12	Fan tachometer input for a fan with a two pulse output.	I OD 1.8 V	PU 10 KΩ 1.8 V	
TEST#	B85	Module input to allow vendor specific Module test mode(s). Carrier designers should leave this pin open on the Carrier. Designers involved in the design of specialty Carriers for Module test may pull this line to GND or possibly to a Module specific analog voltage between GND and 1.8 V to select a test mode.	I OD 1.8 VSB	PU 10 KΩ 1.8 VSB	
RSVD	B24	Reserved pin. This pin may be assigned functions in future versions of this specification. Reserved pin shall not be connected to anything.			

Table 46 External Power Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	A01-A04	Primary power input: fixed +12 V on the Client Type 0; wide range +8 V to +20 V on the Client Type 1; fixed +12 V on the Server. All available VCC pins on the connector shall be used. Refer to COM-HPC® Module Base Specification for details.			
	B01, B03,				
	C01, C03				
	D01-D04				
VCC_RTC	A86	Real-time clock circuit-power input. Nominally +3.0 V. Refer to COM-HPC® Module Base Specification for details.			

Table 47 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN_TX	B05	CAN bus 1.8V logic level transmit signal. A Carrier based CAN transceiver is required to connect to a physical CAN bus.	O CMOS 1.8 V		Not connected
CAN_RX	C05	CAN bus 1.8V logic level receive signal. A Carrier based CAN transceiver is required to connect to a physical CAN bus.	I CMOS 1.8 V		Not connected

Table 48 Functional Safety (FuSa) Support Signal Descriptions

FUSA is not supported on conga-HPC/mPTL

9.2 Boot Strap Signals

Table 49 Boot Strap Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_ALERT#	C88	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 1.8 VSB	PU 2.15 KΩ 1.8 VSB	

Note

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), the COM-HPC® or chipset internally implemented resistors pull these signals to the correct state.

Caution

No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM-HPC® module to malfunction and/or cause irreparable damage to the module.

10 System Resources

TBD

11 BIOS Setup Description

The BIOS setup description of the conga-HPC/mPTL can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, refer to https://wiki.congatec.com/wiki/BIOS_Setup_Description_(AN42).

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

11.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST. The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

11.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-HPC/mPTL is identified as FPTLR0xx, where:

- R is the identifier for a BIOS ROM file,
- 0 is the so called feature number and
- xx is the major and minor revision number.

The binary size is 64 MB.

11.3 Updating the BIOS

BIOS updates are recommeded to correct platform issues or enhance the feature set of the module. The conga-HPC/mPTL features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility: https://wiki.congatec.com/wiki/Congatec_System_Utility_-_CGUTIL.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

11.3.1 Update from External Flash

For instructions on how to update the BIOS from external flash, refer to https://wiki.congatec.com/wiki/External_BIOS_Update_(AN07).

11.4 Supported Flash Devices

The conga-HPC/mPTL supports the following flash devices:

- GigaDevice GD25LB512MFYIGR (64 MB, 1.8 V)
- Winbond W25Q512NWEIM (64 MB, 1.8 V)

The flash device can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to https://wiki.congatec.com/wiki/External_BIOS_Update_(AN07).

Note

For the latest supported flash devices, refer to https://wiki.congatec.com/wiki/Supported_SPI_Flash_Devices_for_BIOS.