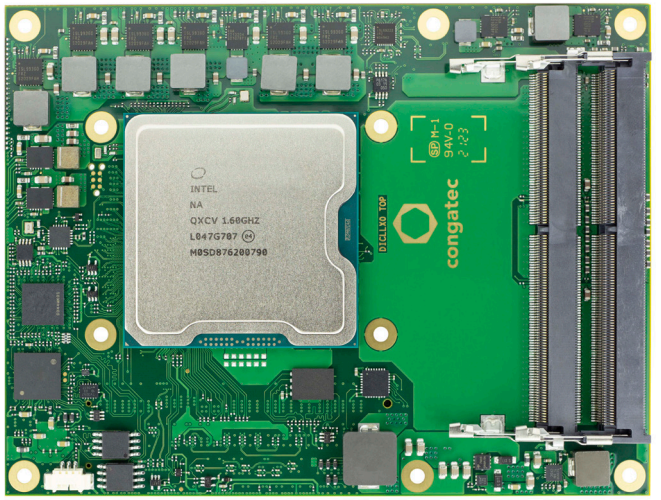

conga-B7XI

COM Express® 3.0/3.1 Type 7 Basic Module with Intel® Ice Lake-D LCC Processors

User's Guide

Revision 1.02

congatec

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.01	2022-12-16	AEM	• Preliminary release
0.02	2023-02-08	AEM	• Updated section 1.2 "Options Information" and added Intel DTR/DTS to table 2 "Commercial Variants" and table 3 "Industrial Variants" • Added notes to sections 4.1 "PCIe 3.0 (PCH), 4.4 "SATA" and 4.5 "USB" • Corrected the supported data rates in section 1.4 "Feature List" and section 6.3 "Memory Population Rules" • Updated the note in section 4.10 "SPI Bus" • Updated section 5.1.5 "Power Loss Control" • Updated section 6 "conga Tech Notes" • Updated table 20 "PCI Express Signal Descriptions (General Purpose)"
0.03	2023-07-26	AEM	• Updated the RoHS directive • Corrected the value of SUS_S3# pull-down resistor in table 27 "Power and System Management Signal Descriptions" • Updated note in section 4.1.4 "Power Control" • Updated the title page
1.00	2024-03-06	AEM	• Added the operating temperature of the variants to section 1.2 "Options Information" • Updated section 1.8 "Power Consumption" • Added note about the long term storage of the module to section 1.10 "Environmental Specifications" • Added section 1.11 "Storage Specifications" • Updated section 2 "Block Diagram" • Corrected the maximum torque for the mounting screws of the module in section 3 "Cooling Solutions" • Added note about the long term storage of congatec cooling solutions to section 3 "Cooling Solutions" • Updated section 4.12 "General Purpose Serial Interface" • Added section 4.15 "Inrush and Maximum Current Peaks" • Updated section 5.1 "congatec Board Controller" • Updated section 5.1.5 "Power Loss Control" • Official release
1.01	2025-01-27	AEM	• Added WEEE directive to the preface section • Added a new variant with PN: 050221 (COM 3.1 variant) to table 3 "Industrial Variants" • Added a note to section 1.10 "Environmental Specifications" • Updated the cooling diagrams in sections 3.1 "CSA Dimensions", 3.2 "CSP Dimensions" and 3.3 "HSP Dimensions" • Corrected the statement that 2 x8, 4 x4 or 8 x1 link configuration is possible via the BIOS setup menu in section 4.1 "PCIe 3.0 (PCH) • Corrected the name of congatec interposer card in section 4.7 "10 Gigabit Ethernet" • Added note about MAC address programming to section 4.6 "2.5 Gigabit Ethernet" and table 19 "Gigabit Ethernet Signal Descriptions" • Changed CFG 7.7 to CFG 5.1 in section 4.7.1 and section • Added note about industrial use conditions in section 6.1.3 "Intel Turbo Boost Technology" • Updated table 21 "10 Ggabit Ethernet Pinout Description (COM Rev. 3.0)" to indicate that 10G_SDP[0:3] signals are not supported

Revision	Date (yyyy-mm-dd)	Author	Changes
1.02	2025-03-06	RVI	• Added a note to disable Turbo mode for industrial variants in table 3 “Industrial Variants” • Added a note to the section 1.6 “Mechanical Dimensions” • Corrected a typographic error in section 1.11.1 “Module” • Added a caution to the section 3 “Cooling Solutions” • Corrected the description of medium in Table 12 CFG 2.2 to Marvell 88E1543 • Removed 100BASE-TX support in CFG 2.1 and CFG 7.0 Coppervale section in Table 12 and Table 38

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-B7XI. It is one of the documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

- COM Express® Module Base Specification
- COM Express® Carrier Design Guide

These documents are available on the PICMG website at **www.picmg.org**. Additionally, check the restricted area of the congatec website at **www.congatec.com** and the website of the respective silicon vendor for relevant documents (Erratum, PCN, Sighting Reports and others).

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Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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Terminology

Term	Description
CEI	Common Electrical Interface
CSA	Active Cooling Solution
CSP	Passive Cooling Solution
DTR	Dynamic Temperature Range
GB	Gigabyte
GHz	Gigahertz
HSP	Heatspreader
kB	Kilobyte
MB	Megabyte
Mbit	Megabit
Gbps	Gigabit per second
Mbps	Megabit per second
MTps	Megatransfer per second
kHz	Kilohertz
MHz	Megahertz
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
PCH	Platform Controller Hub
SM	System Management
SFI	SerDes Frame Interface
SFP+	Enhanced Small Form-factor Pluggable
SoDIMM	Small Outline Dual In-line Memory Modules
BMC	Baseboard Management Controller
N.C	Not connected
N.A	Not available
TBD	To be determined

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1 Introduction

1.1 COM Express Concept

COM Express is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express modules are available in following form factors:

- Mini 84 mm x 55 mm
- Compact 95 mm x 95 mm
- Basic 125 mm x 95 mm
- Extended 155 mm x110 mm

Table 1 COM Express 3.0 Pinout Types

Types	Connector Rows	PCIe Lanes	PEG	SATA Ports	LAN ports	USB 2.0/ SuperSpeed USB	Display Interfaces
Type 6	A-B C-D	Up to 24	1	Up to 4	1	Up to 8 / 4 [1]	VGA,LVDS/eDP, PEG, 3x DDI
Type 7	A-B C-D	Up to 32	-	Up to 2	5 (1x 1 Gb, 4x 10 Gb)	Up to 4 / 4	
Type 10	A-B	Up to 4	-	Up to 2	1	Up to 8 / 2 [1]	LVDS/eDP, 1xDDI

1. *The SuperSpeed USB ports (USB 3.0) are not in addition to the USB 2.0 ports. Up to 4 of the USB 2.0 ports can support SuperSpeed USB.*

The conga-B7XI modules use the Type 7 pinout definition and comply with COM Express 3.0 or 3.1 specification depending on the variant used. The conga-B7XI modules are equipped with two high performance connectors that ensure stable data throughput, and support high bandwidth networking.

The COM (computer on module) integrates all the core components of a common PC and is mounted onto an application-specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any embedded PC application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 3.0/2.0, and 10 Gigabit Ethernet. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

Most importantly, COM Express modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

1.2 Options Information

The conga-B7XI is currently available in six variants (two commercial and four industrial). The table below shows the different configurations available.

Table 2 Commercial Variants

Part-No.		050210	050211
Processor		Intel® Xeon® D-1735TR 2.20 GHz 8 Cores	Intel® Xeon® D-1712TR 2.0 GHz 4 Cores
Intel® Smart Cache		15 MB	10 MB
Max. Turbo Frequency		3.40 GHz	3.10 GHz
Processor Graphics		N.A	N.A
DDR4 Memory (ECC or Non-ECC)		2933 MTps dual channel (up to 128 GB) [1]	2400 MTps dual channel (up to 128 GB) [1]
Gigabit Ethernet		4x 10GBASE-KR/SFI/CEI [2] 1x 2500BASE-T	4x 10GBASE-KR/SFI/CEI [2] 1x 2500BASE-T
PCIe Lanes	Gen 3/Gen 4	16 lanes [3]	16 lanes [3]
	Gen 3	16 lanes	16 lanes
USB Ports		4x USB 3.1 Gen 1	4x USB 3.1 Gen 1
SATA (6 Gbps)		2	2
Processor TDP		59 W	40 W
Operating Temperature		0°C – 60°C	0°C – 60°C
CPU Use Condition [4]		Industrial	Industrial
CPU Tcase	Min.	0°C	0°C
	Max.	82°C	84°C
CPU DTSmax		100°C	100°C
CPU DTR [4]		90°C or 145°C depending on the combined supported high speed ports	
Compatible Carrier Board		conga-X7EVAL Evaluation Carrier Board	

Note

1. *The conga-B7XI features three memory sockets and supports up to 96 GB memory by default. For 128 GB memory, you need a customized module wiith four memory socket and the height of the carrier board's connectors and standoffs must be 8 mm.*
2. *Default configuration is 10GBASE-KR (COM 3.0 variant). 10GBASE-SFI/CEI requires a customized conga-B7XI (COM 3.1 variant).*
3. *PCIe Gen. 3 by default. For PCIe Gen. 4, you need a customized conga-B7XI.*
4. *Intel SoC use conditions. See Intel documentation for more information.*
5. *DTR is 90°C if CPU PCIe 4.0, PCH PCIe 3.0 and SATA 3 ports are supported. DTR is 145°C if CPU PCIe 3.0, PCIe 2.0 and SATA 2 ports are supported (no CPU PCIe 4.0, PCH PCIe 3.0 or SATA 3 support).*

Table 3 Industrial Variants

Part-No.		050200	050201	050202	050220 (4x DDR4 Sockets)	050221 (COM 3.1)
Processor		Intel® Xeon® D-1746TER 2.0 GHz 10 Cores	Intel® Xeon® D-1732TE 1.9 GHz 8 Cores	Intel® Xeon® D-1715TER 2.4 GHz 4 Cores	Intel® Xeon® D-1746TER 2.2 GHz 10 Cores	Intel® Xeon® D-1848TER 2.0 GHz 10 Cores
Intel® Smart Cache		15 MB	15 MB	10 MB	15 MB	15 MB
Max. Turbo Frequency [1]		3.10 GHz	3.0 GHz	3.5 GHz	3.10 GHz	3.10 GHz
Processor Graphics		N.A	N.A	N.A	N.A	N.A
DDR4 Memory (ECC or Non-ECC)		2666 MTps dual channel (up to 128 GB) [2]	2666 MTps dual channel (up to 128 GB) [2]	2666 MTps dual channel (up to 128 GB) [2]	2666 MTps dual channel (up to 128 GB) [2]	2666 MTps dual channel (up to 128 GB) [2]
Gigabit Ethernet		4x 10GBASE-KR/SFI/CEI [3] 1x 2500BASE-T	4x 10GBASE-KR/SFI/CEI [3] 1x 2500BASE-T	4x 10GBASE-KR/SFI/CEI [3] 1x 2500BASE-T	4x 10GBASE-KR/SFI/CEI [3] 1x 2500BASE-T	4x 10GBASE-KR/SFI/CEI [3] 1x 2500BASE-T
PCIe Lanes	Gen 3/Gen 4	16 lanes [4]	16 lanes [4]	16 lanes [4]	16 lanes [4]	16 lanes
	Gen 3	16 lanes	16 lanes	16 lanes	16 lanes	16 lanes
USB Ports		4x USB 3.1 Gen 1	4x USB 3.1 Gen 1	4x USB 3.1 Gen 1	4x USB 3.1 Gen 1	4x USB 3.1 Gen 1
SATA (6 Gbps)		2	2	2	2	2
Processor TDP		67 W	52 W	50 W	67 W	57 W
Operating Temperature		-40°C – 85°C	-40°C – 85°C	-40°C – 78°C	-40°C – 85°C	-40°C – 85°C
CPU Use Condition [5]		Industrial	Industrial	Industrial	Industrial	Industrial
CPU Tcase	Min.	-40°C	-40°C	-40°C	-40°C	-40°C
	Max.	85°C	90°C	78°C	85°C	87°C
CPU DTSmax		102°C	105°C	100°C	102°C	101°C
CPU DTR [6]		90°C or 145°C depending on the combined supported high speed ports				
Compatible Carrier Board		conga-X7EVAL Evaluation Carrier Board				

Note

1. *Disable Turbo mode for industrial use conditions.*
2. *The conga-B7XI features three memory sockets and supports up to 96 GB memory by default. For 128 GB memory, you need a customized module wiith four memory socket and the height of the carrier board's connectors and standoffs must be 8 mm.*
3. *Default configuration is 10GBASE-KR (COM 3.0 variant). 10GBASE-SFI/CEI requires a customized conga-B7XI or variant with PN: 050221.*
4. *PCIe Gen. 3 by default. For PCIe Gen. 4, you need a customized conga-B7XI or variant with PN: 050221.*
5. *Intel SoC use conditions. See Intel documentation for more information.*
6. *DTR is 90°C if CPU PCIe 4.0, PCH PCIe 3.0 and SATA 3 ports are supported. DTR is 145°C if CPU PCIe 3.0, PCIe 2.0 and SATA 2 ports are supported (no CPU PCIe 4.0, PCH PCIe 3.0 or SATA 3 support).*

1.3 COM Express Compliancy

The conga-B7XI complies with COM Express Specification 3.0 or 3.1, depending on the variant used. For a COM Express 3.1 variant with a different configuration, a customized conga-B7XI module can be created through a BOM option to meet specifice requirements. For more information about the COM Express Specification 3.1 signals the conga-B7XI supports, see section 8 “COM 3.1 Variants”.

1.4 Feature List

Table 4 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 7, revision 3.0 [1] (Basic size 125 x 95 mm)	
Processor	Intel® Xeon processor D-1700	
Memory [1]	Up to four memory sockets [2,3] (two on the top side and up to two on the bottom side). Supports: - DDR4 ECC and non-ECC SODIMM modules - dual channel (channel 0, DIMM 0 (top side, lower slot), channel 0, DIMM 1 (bottom side, lower slot), channel 1, DIMM 0 (top side, upper slot) and channel 1, DIMM 1 via assembly option (bottom side, upper slot)) - data rates up to 2933 MTps - up to 128 GB capacity (up to 4 x 32 GB each) [2]	
congatec Board Controller	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, hardware monitoring, fan control, I²C bus, Power loss control	
Chipset	Integrated in the SoC	
Ethernet	Gigabit Ethernet. Supports: - 4x 10GBASE-KR/SFI/CEI [4] - 1x 2500GBASE-T	
Audio	N.A	
Graphics	N.A	
Peripheral Interfaces	8x USB 2.0 (Up to 4x USB 3.1 Gen 1) 2x SATA® 6 Gbps 16x PCI Express® Gen. 3 lanes 16x PCI Express® Gen. 3/Gen 4 lanes [5] 1x Optional onboard NVMe SSD (PCIe x4 Gen 4 2x UART (16C550 compatible)	GPIOs LPC (no DMA) I²C (fast mode, 400 KHz, multi-master) SMBus SPI
BIOS	AMI Aptio® V UEFI 2.x firmware; 64 MB SPI with congatec Embedded BIOS features	
Onboard Storage	N.A	
Power Management	Supports: - ACPI 5.0a compliant with battery support. - Hardware power management - System Sleep State Control - Wake events from the Intel Management Engine	
Security	Discrete Trusted Platform Module (Infineon SLM9670_AQ2.0); new AES Instructions for faster and better encryption.	

Note

1. *For COM Express 3.1 compliant module, you need a customized conga-B7XI (BOM option) or the variant with PN: 050221.*
2. *The conga-B7XI features three memory sockets and supports up to 96 GB memory by default. For 128 GB memory, you need a customized module wiith four memory socket and the height of the carrier board's connectors and standoffs must be 8 mm.*
3. *See section 6.3 "Memory Population Rules".*
4. *10GBASE-KR by default (COM 3.0 variant). 10GBASE-SFI/CEI requires a customized conga-B7XI (COM 3.1 variant) or the variant with PN: 050221.*
5. *PCIe Gen 3 by default. For PCIe Gen. 4, you need a customized conga-B7XI or the variant with PN: 050221.*

Caution

The conga-B7XI will not boot if the top, upper slot is not populated in a dual memory configuration. See section 6.3 "Memory Population Rules" for more information.

1.5 Supported Operating Systems

The conga-B7XI supports the following operating systems.

- Microsoft® Windows® 10
- Microsoft® Windows® 10 IoT Enterprise
- Linux
- Yocto Project
- Real Time Systems Hypervisior

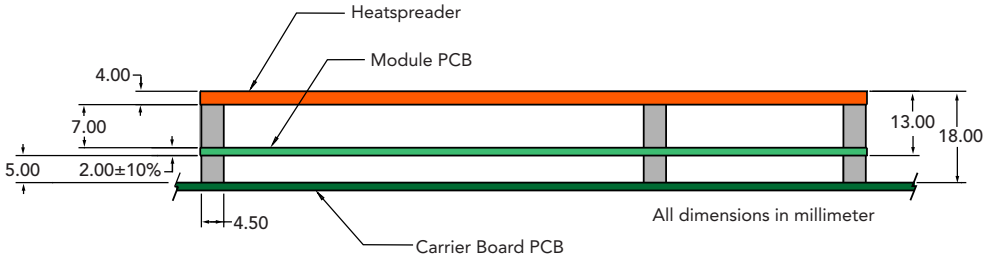
Note

For better system performance, use only 64-bit Operating Systems.

1.6 Mechanical Dimensions

- Length of 125 mm
- Width of 95 mm

The overall height (module, heatspreader and stack) is shown below:



Note

3D models of congatec products are available at www.congatec.com/login. *These models indicate the overall length, height and width of each product. If you need login access, contact your local sales representative.*

1.7 Supply Voltage Standard Power

- 12 V DC ± 5 %

1.7.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 7 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Ampere)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4 - 12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75 - 5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.5 - 3.3		+/- 20			

1.7.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

1.8 Power Consumption

The power consumption values were measured with the following setup:

- input voltage +12 V
- conga-B7XI COM
- modified congatec carrier board
- conga-B7XI cooling solution
- Microsoft Windows 10 (64 bit)

Note

The CPU was stressed to its maximum workload.

Table 5 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S5	COM is powered by VCC_5V_SBY	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Table 6 Power Consumption Values

The table below provides additional information about the conga-B7XI power consumption. The values are recorded at various operating mode.

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (A)				
					Variant	Cores	Freq. /Max. Turbo	S0: Min	S0: Max	S0: Peak	S3	S5
050210	3 x 4 GB	B.1	DICLR018	Windows 10	Intel® Xeon® D-1735TR	8	2.2 / 3.4 GHz	2.13	5.78	7.33	N.A	1.35
050211	3 x 4 GB	B.2	DICLR018	Windows 10	Intel® Xeon® D-1712TR	4	2.0 / 3.1 GHz	2.04	3.63	4.12	N.A	1.34
050200	3 x 4 GB	B.1	DICLR018	Windows 10	Intel® Xeon® D-1746TER	10	2.0 / 3.1 GHz	2.06	6.40	7.16	N.A	1.47
050201	3 x 4 GB	B.1	DICLR013	Windows 10	Intel® Xeon® D-1732TE	8	1.9 / 3.0 GHz	2.17	5.00	5.66	N.A	1.58
050202 (4x DDR4 Socket)	3 x 4 GB	B.2	DICLR016	Windows 10	Intel® Xeon® D-1715TER	4	2.4 / 3.5 GHz	2.23	5.19	5.75	N.A	1.55
050220	3 x 4 GB	B.2	DICLR016	Windows 10	Intel® Xeon® D-1746TER	10	2.0 / 3.1 GHz	2.11	6.44	7.90	N.A	1.47

1.9 Supply Voltage Battery Power

Table 7 CMOS Battery Power Consumption (Commericial Variants)

RTC @	Voltage	Current
-10°C	3V DC	1.96 µA
20°C	3V DC	2.65 µA
70°C	3V DC	3.06 µA

Table 8 CMOS Battery Power Consumption (Industrial Variants)

RTC @	Voltage	Current
-50°C	3V DC	1.30 µA
20°C	3V DC	2.03 µA
95°C	3V DC	3.46 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*

3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*

4. *We recommend to always have a CMOS battery present when operating the conga-TC570.*

1.10 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to 80°C (commercial variants)
Temperature	Operation: -40° to 85°C [1]	Storage: -40° to 85°C [1] (industrial variants)
Relative Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Note

1. *Depends on the CPU variant (see table 3 "Industrial Variants" for more information)*

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

1.11 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

1.11.1 Module

For long term storage of the conga-B7XI (more than six months), keep the conga-B7XI in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

Note

We do not recommend storing the conga-B7XI for more than five years under these conditions.

1.11.2 Cooling Solutions

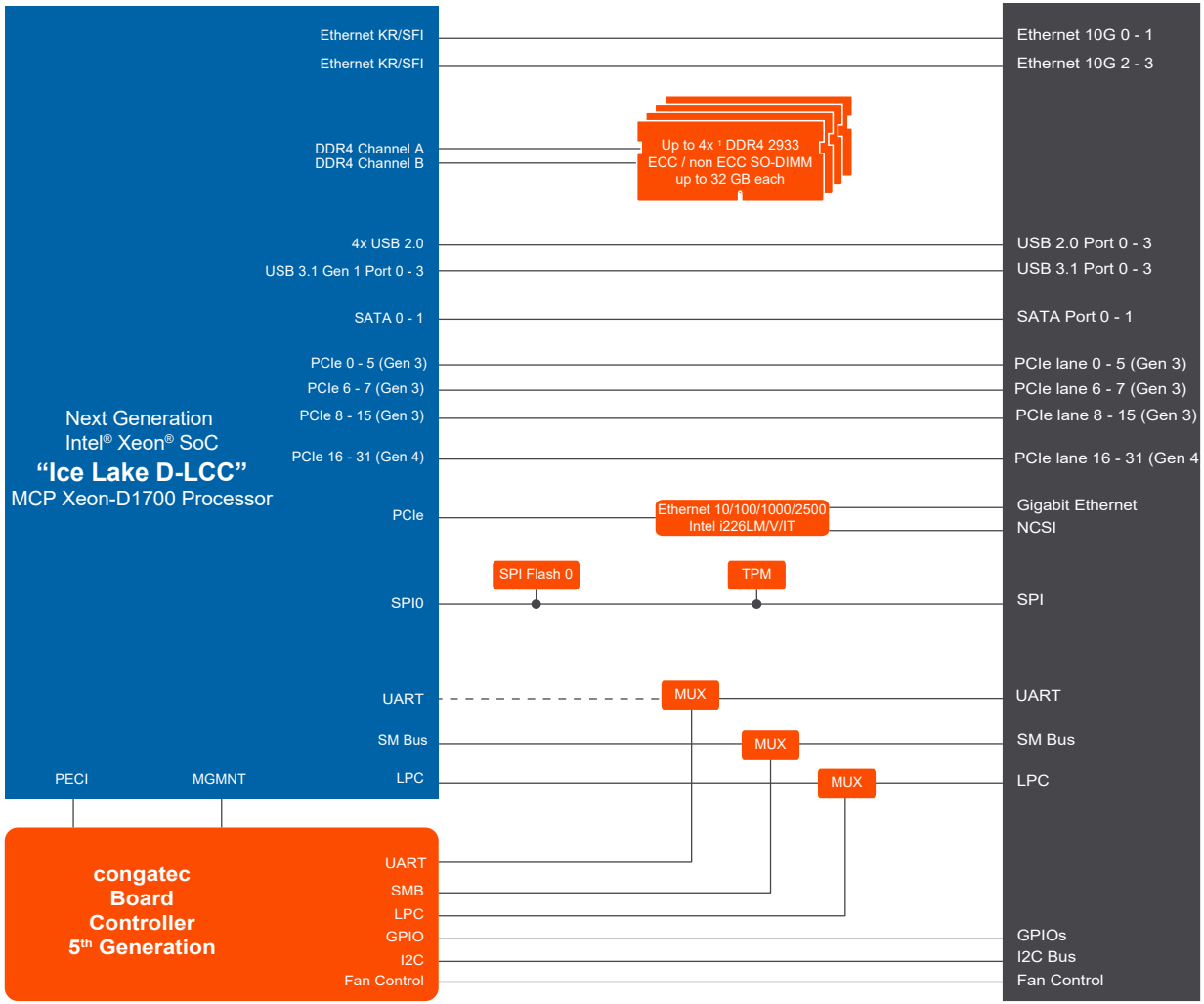
The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. For optimal cooling performance, do not store the heatspreaders/cooling solutions at temperatures below -20°C.

Note

1. *For temperatures between -10°C and -20°C, preheat the heatpipes before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your local sales representative.*

2. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

2 Block Diagram



[1] 3x DDR4 (96 GB) available by default. The fourth SO-DIMM slot (up to 128 GB) is by assembly option

– – – – Not available by default

3 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-B7XI. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

	Cooling Solution	Part No	Description
1	CSA-HP	050250	Active cooling solution with integrated heat pipes, 39.5 mm overall cooling height and integrated 12 V fan
3	CSP-HP	050252	Passive cooling solution with integrated heat pipes, 23.3 mm overall cooling height
4	HSP-B	050254	Heatspreader with integrated heat pipes, 11 mm overal cooling height and 2.7 mm bore-hole standoffs
		050255	Heatspreader with integrated heat pipes, 11 mm overal cooling height and M2.5 mm threaded standoffs
6	HPA	050256	Heatpipe adapter with metal bracket base, spring screws and accessory kit suitable for standard 8 mm heat pipes for optimal heat distribution

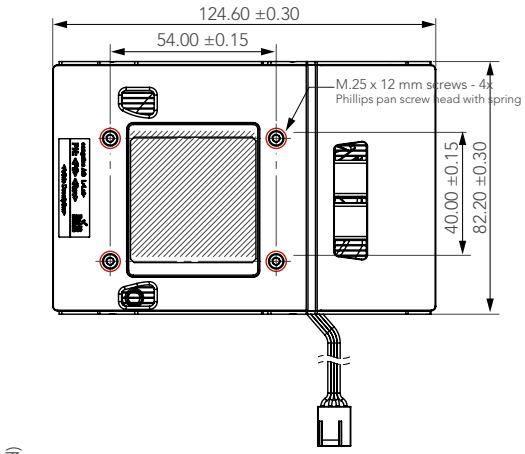
Caution

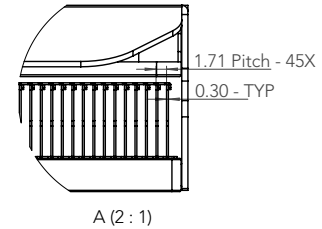
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. To ensure optimal cooling performance, they should not be stored at temperatures below -20°C. If the storage temperature drops below -10°C, the heatpipes should be pre-heated before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your local sales representative.*
3. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
4. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
5. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.245 Nm for module mounting screws.*
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*
3. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

3.1 CSA Dimensions





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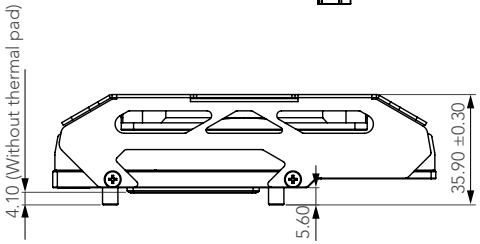
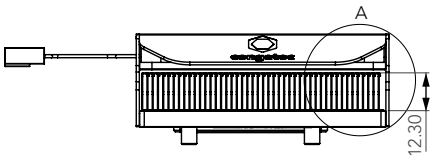
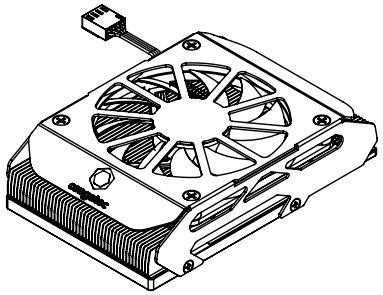
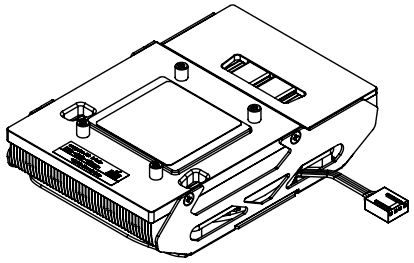
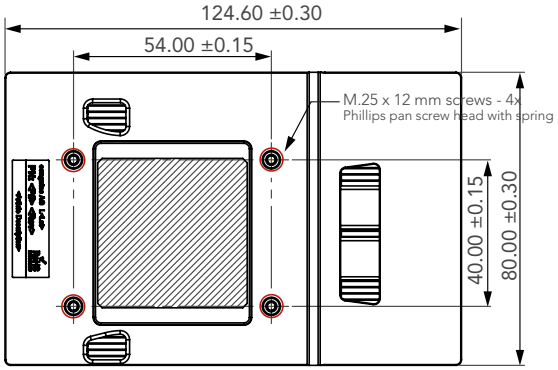


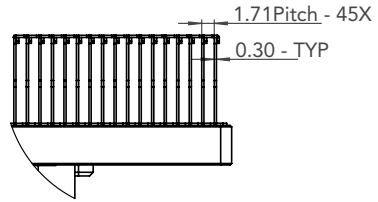






3.2 CSP Dimensions





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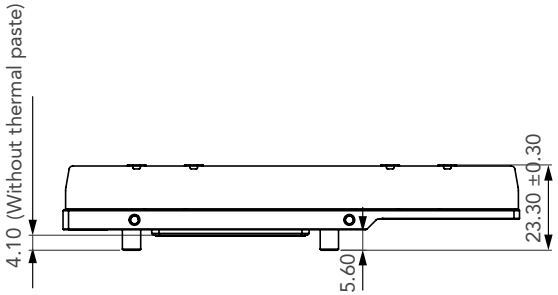
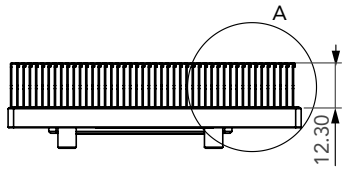
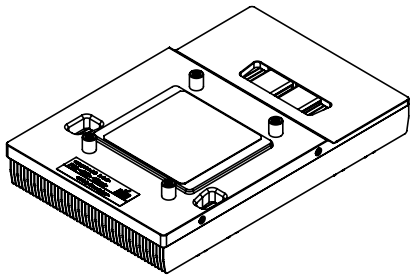
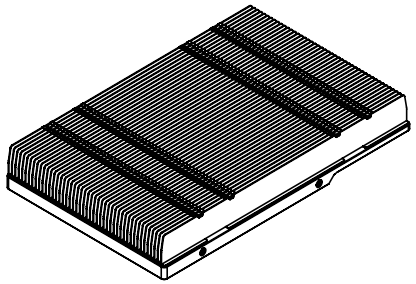
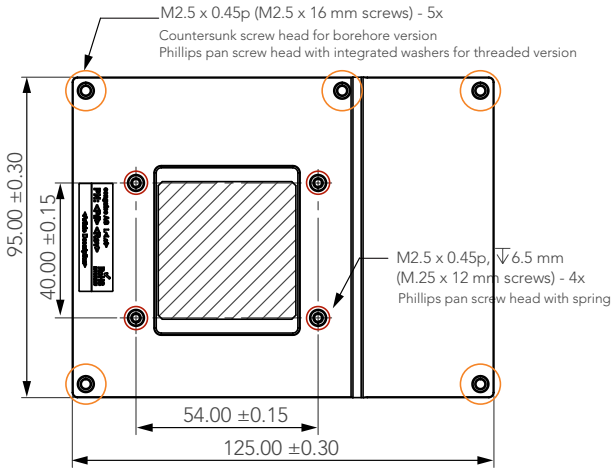


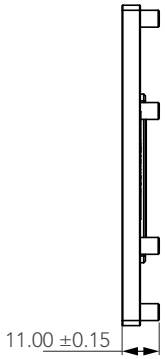


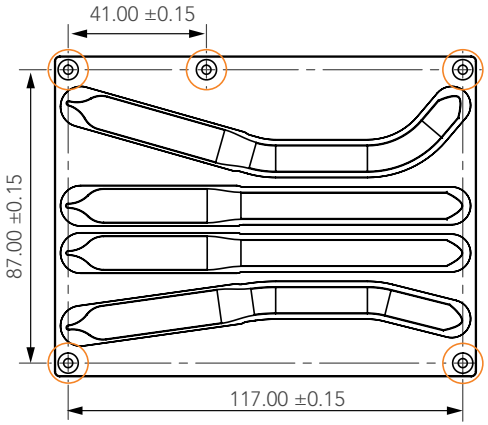


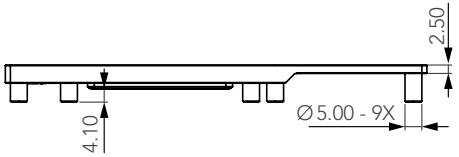


3.3 HSP Dimensions

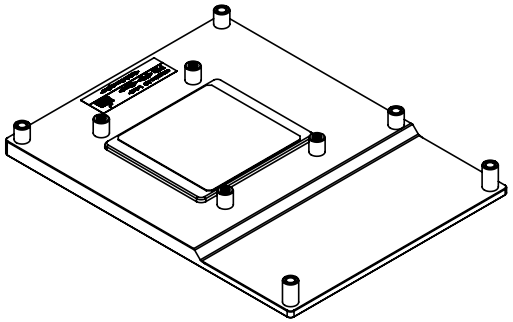


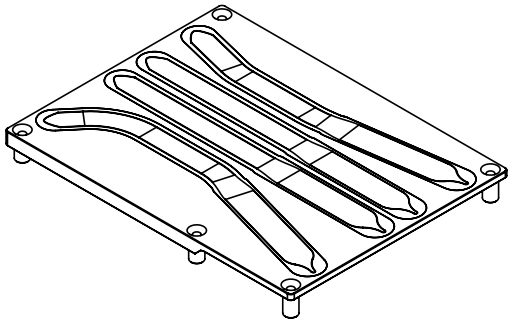




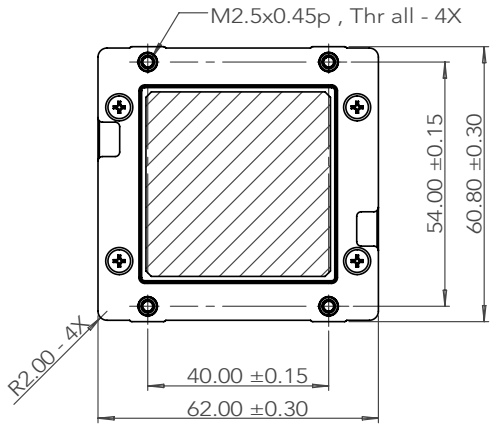


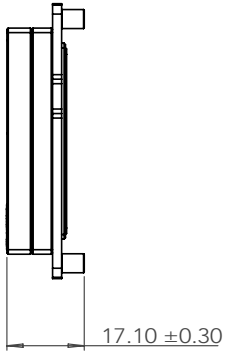
M2.5
threaded standoff
for threaded version
or
ø2.7
non-threaded standoff
for borehole version

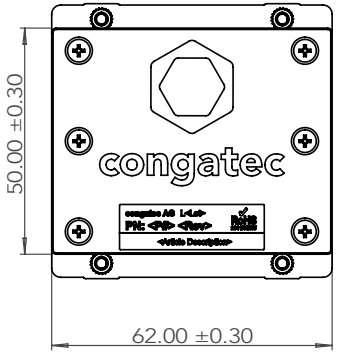


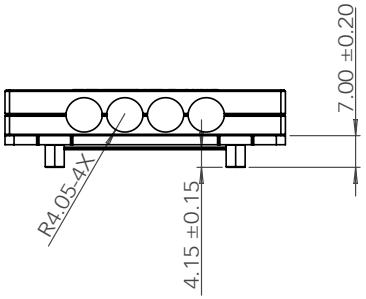


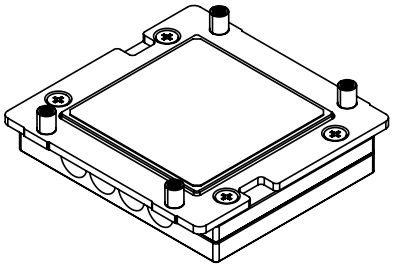
3.4 HPA Dimensions

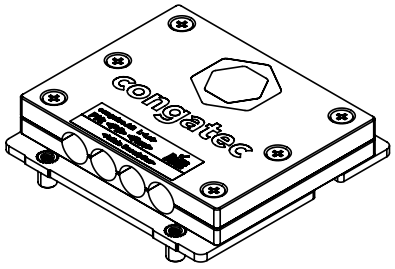












4 Connector Rows

The conga-B7XI is connected to the carrier board via two 220-pin connectors (COM Express Type 7 pinout). These connectors are broken down into four rows. The primary connector consists of rows A - B while the secondary connector consists of rows C - D.

The following subsystems can be found on the primary (A - B) and secondary (C - D) connector rows.

Table 10 Supported Interfaces on Rows A-B and C-D

Interfaces	Rows A-B	Rows C-D
SATA	2	-
USB 2.0	4	-
USB 3.1 Gen 1 SuperSpeed	-	4
NBASE-T	2.5 Gbps	-
10GBASE-KR/SFI/CEI	-	4
PCIe Gen 3	14 lanes	2 lanes
PCIe Gen 3/4 [1]	-	16 lanes
UART	2	-
Others	SPI, LPC, SMBus	-

Note

1. *For PCIe Gen 4 support, you need a customized conga-B7XI or the variant with PN:050221.*

4.1 PCIe 3.0 (PCH)

The conga-B7XI offers up to 16 PCIe 3.0 lanes from the Intel PCH—up to 14 lanes on the A–B connector and up to two lanes on the C–D connector. The conga-B7XI supports the following PCIe features:

- Up to 8 GT/s data rate [1]
- 1 x4, 2 x2 and 1 x8 link configuration by default
- 2 x8 or 4 x4 or 8 x1 link configuration with custom BIOS [2]
- Maximum of eight root ports
- Lane polarity inversion

Note

1. *The maximum combined HSIO bandwidth (PCIe 3.0 (PCH), USB and SATA) is 16 GB/s.*
2. *For 8 x1 PCIe configuration in Bucket 1, you need a customized conga-B7XI.*

4.2 PCIe 3.0/4.0 (CPU)

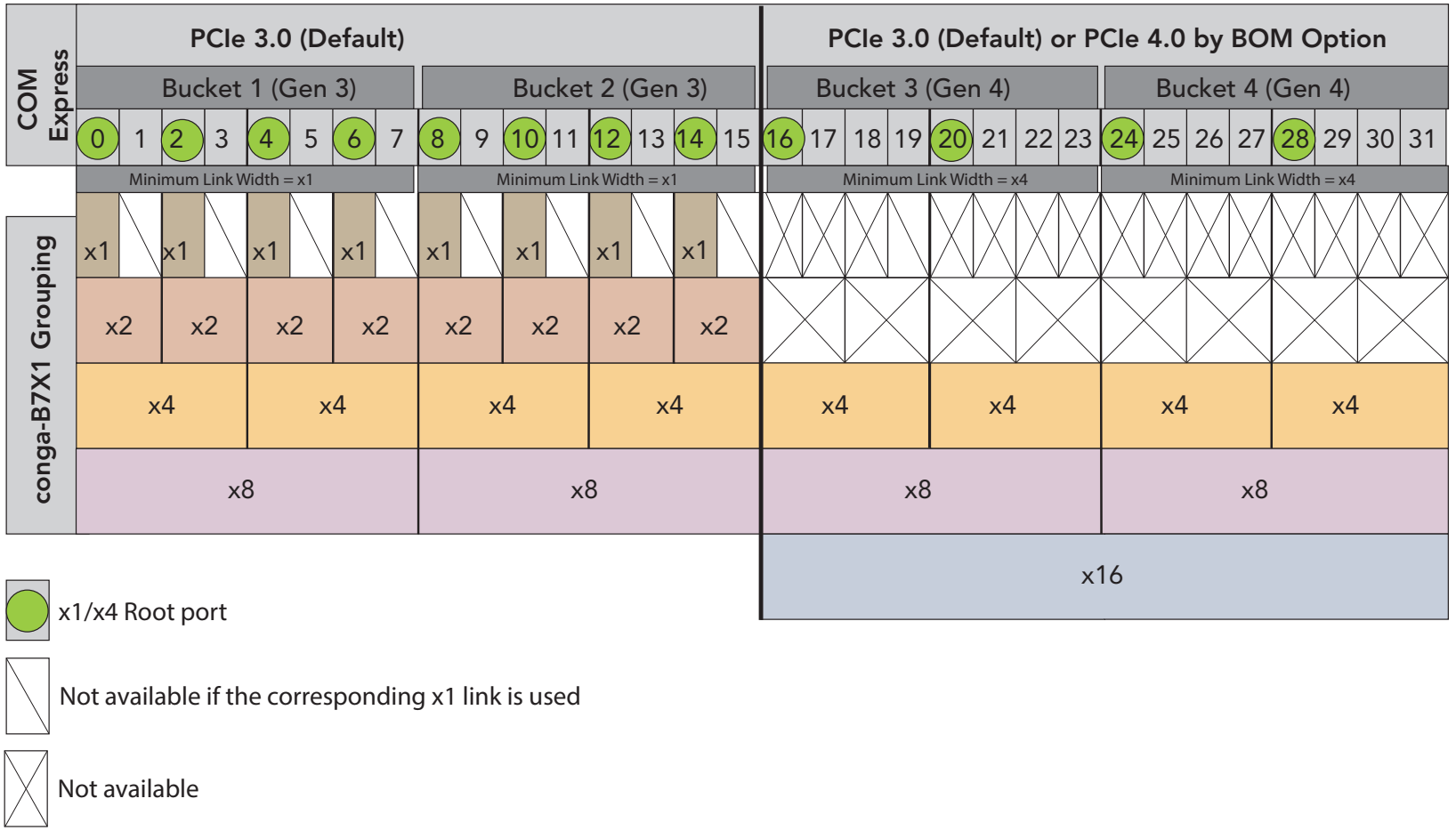
The conga-B7XI offers up to 16 PCIe 3.0/4.0 lanes from the Intel CPU. The lanes support PCIe 3.0 by default and PCIe 4.0 [1] lanes via a customized conga-B7XI. The conga-B7XI supports the following PCIe features:

- Up to 16 GT/s data rate
- 4 x4, 2 x4 + 1 x8, 1 x8 + 2 x4, 2 x8 or 1 x16 link configuration via the BIOS setup menu
- Maximum of four root ports
- Lane polarity inversion
- Lane reversal

Note

1. *PCIe Gen 3 by default. For PCIe Gen. 4, you need a customized conga-B7XI or the variant with PN: 050221 and a COM Express 3.1 compliant carrier board.*
2. *For COM Express 3.1 pin comparison, see section 8 "COM 3.1 Variants"*

4.3 PCI Express Routing/Configuration



Note

The minimum width link for buckets 3 and 4 is x4 link. If you use a x1 or a x2 link in these buckets, the remaining lanes that make up the x4 link will not be available.

4.4 SATA

The conga-B7XI offers two SATA ports on the A-B connector. The SATA interfaces support:

- Data transfer rates up to 6.0 Gb/s
- SATA Specification, rev 3.2
- AHCI mode using memory space
- Independent DMA operation
- Hot-plug detect

Note

1. *The interfaces do not support legacy mode using I/O space.*
2. *RAID is not supported.*
3. *The maximum combined HSIO bandwidth (PCIe 3.0 (PCH), USB and SATA) is 16 GB/s.*

4.5 USB

The conga-B7XI offers four USB 2.0 ports on the A-B connector and four SuperSpeed signals on the C-D connector. You can combine each USB 2.0 port with corresponding USB SuperSpeed signals to create USB 3.1 Gen 1 port.

The xHCI host controller supports:

- USB 3.1 specification
- SuperSpeedPlus, SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling
- Data transfers [1] up to 5 Gbps for USB 3.1 Gen 1 port

Note

1. *The maximum combined HSIO bandwidth (PCIe 3.0 (PCH), USB and SATA) is 16 GB/s.*

4.6 2.5 Gigabit Ethernet

The conga-B7XI offers a 2.5 Gigabit Ethernet interface via an onboard Intel® i226 controller. The interface supports:

- Full-duplex operation at 10/100/1000/2500 Mbps
- Half-duplex operation at 10/100 Mbps

The table below describes the LED operation.

Table 11 2.5 Gb Ethernet LED Description

LED Left Side	LED Right Side	Description
Off	Off	No link
Off	Green (blinking)	10 Mpbs or 100 Mbps link established
Green	Green (blinking)	1 Gbps link established
Yellow	Green (blinking)	2.5 Gbps link established

Note

The MAC address of the Intel i226 Ethernet controller is preprogrammed by default. The MAC address cannot be reprogrammed. If you require custom MAC address, contact your local sales representative.

4.7 10 Gigabit Ethernet

The conga-B7XI offers four 10 gigabit Ethernet interfaces The interface supports:

- 10GBASE-KR for backplane applications (default configuration) [1]
- 10G-SFI-DA, 10GBASE-SR/LR or 10G-SFI-ACC/AOC for SFP application [2]
- 10GBASE-T with Intel Coppervale X557-AT4
- NC-SI protocol

Note

1. *The 10 GbE PHY must be implemented on the carrier board.*
2. *For better signal integrity, we recommend to implement an external PHY or retimer on the carrier board (for example, the Intel Parkvale C827-AM/C827-IM for SFP application).*

Note

The Intel® Ice Lake SoC on the conga-B7XI does not support the INPHY CS4227 PHY used on the conga-X7EVAL. For 10 Gb SFI connection when using the conga-B7XI in combination with the conga-X7EVAL, you need the congatec DSFI interposer card for native SFI connection. For more information, contact your sales representative.

4.7.1 Possible Ethernet Configurations

The table below lists the 10 gigabit Ethernet configurations the conga-B7XI COM 3.1 supports.

Table 12 Supported Ethernet Configurations

Intel HW Config ID	Medium	Interface	Possible Link Modes	Rate	Carrier Board	Comment
CFG 1.0 [3]	Native SFI	4x SFP+	10G-SFI-DA	10 Gb	COM 3.0	Available on request with customized conga-B7XI COM 3.0 variant. This option does not support CEI. **Note:** 1 *We do not recommend this configuration.* 2 *SFP+ RS and RX_LOS signals are not supported.* 3 *Speed/link indicator is not supported..*
			10GBASE-SR/LR			
			10G-SFI-ACC/AOC			
			1000BASE-SX/LX	1 Gb		
CFG 2.0	Parkvale C827-AM/XL827-AM	4x SFP+	10G-SFI-DA	10 Gb	COM 3.0	Available on request with customized conga-B7XI COM 3.0 variant.This option does not support CEI. **Note:** 1 *We do not recommend this configuration.* 2 *SFP+ RS and RX_LOS signals are not supported.* 3 *Speed/link indicator is not supported..*
			10GBASE-SR/LR			
			10G-SFI-ACC/AOC			
			1000BASE-SX/LX	1 Gb		
CFG 2.1	Coppervale X557-AT4	4x 10GBASE-T	10GBASE-T	10 Gb	COM 3.0	Available on request with customized conga-B7XI COM 3.0 variant. This option does not support CEI. **Note:** Speed/link indicator is not supported.
			1000BASE-T	1 Gb		
CFG 2.2	Marwell 88E1543	4x 1000BASE-T	1000BASE-T	1 Gb	COM 3.0	Available on request with customized conga-B7XI COM 3.0 variant. This option does not support CEI. **Note:** Speed/link indicator is not supported.
			100BASE-TX	100 Mb		
CFG 7.0 [1, 2]	Parkvale C827-AM/XL827-AM	4x SFP+	10G-SFI-DA	10 Gb	COM 3.1	Full CEI support. **Note:** Requires customized conga-B7XI COM 3.1 variant or the variant with PN: 050221, BIOS update and corresponding NVM image.
			10GBASE-SR/LR			
			10G-SFI-ACC/AOC			
			1000BASE-SX/LX	1 Gb		

CFG 7.0 [1, 2]	Coppervale X557-AT4	4x 10GBASE-T	10GBASE-T	10 Gb	COM 3.1	Full CEI support. **Note:** Requires customized conga-B7XI COM 3.1 variant or the variant with PN: 050221, BIOS update and corresponding NVM image.
			1000BASE-T	1 Gb		
	Marwell 88E1543	4x 1000BASE-T	1000BASE-T	1 Gb		
			100BASE-TX	100 Mb		
CFG 7.6 [3, 4] (default)	Backplane	10GBASE-KR	10GBASE-KR	10 Gb	COM 3.0 and COM 3.1	
			2500BASE-X	2.5 Gb		
			1000BASE-KX	1 Gb		
CFG 5.1 [3]	Native SFI	4x SFP+	10G-SFI-DA	10 Gb	COM 3.1	With I/O expander (leveraging the CEI concept without a PHY on the carrier board). **Note:** Requires customized conga-B7XI COM 3.1 variant or the variant with PN: 050221, BIOS update and corresponding NVM image.
			10GBASE-SR/LR			
			10G-SFI-ACC/AOC			
			1000BASE-SX/LX	1 Gb		

Note

1. *The conga-B7XI COM 3.0 modules do not support CEI. For CEI support, you need a customized variant (BOM option). See section 8 "COM 3.1 Variants" for CEI-related pins and the pinout differences between COM 3.0 and COM 3.1 variants".*

2. *Appropriate NVM image must be used. For instructions on how to deploy 10 GbE LAN NVM and PHY NVM images, refer to congatec CTN 20180726 001 document in the restricted area of our website.*

3. *The Intel® Ice Lake SoC on the conga-B7XI does not support the INPHY CS4227 PHY featured on the conga-X7EVAL. If you use the conga-B7XI in combination with the conga-X7EVAL and you require 10 Gb SFI connection, use the congatec DFSI interposer card for native SFI connection. For more information, contact your sales representative.*

4. *To change from the default configuration CFG 7.6 to CFG 7.0 or CFG 5.1, you need a customized conga-B7XI, BIOS update and a corresponding NVM image. For more information, contact your sales representative.*

4.8 LPC Bus

The conga-B7XI offers the LPC (Low Pin Count) bus through the integrated PCH. The congatec cBC is connected to the LPC bus.

Note

The LPC bus does not support DMA devices.

4.9 I²C Bus

The I²C bus is implemented through the congatec Board Controller (cBC)and accessed with the congatec CGOS driver and API. The controller provides a fast-mode multi-master I²C bus that has the maximum I²C bandwidth.

Table 13 Reserved I²C Addresses

8-bit Device Address	7-bit Device Address	Device	Description
0xA0, 0xA2, 0xA4, 0xA6, 0xA8, 0xAA, 0xAC, 0XAE	0x50, 0x51, 0x52, 0x53, 0x54, 0x55, 0x56, 0x57	Optional Carrier board EEPROM	For COM Express carrier board EEPROM. Reserved only if the conga-B7XI is used in combination with the congatec conga-X7EVAL carrier board.
0x14	0x0A	congatec Board Controller	Reserved for battery management
0x16	0x0B	congatec Board Controller	Reserved for battery management
0xE2	0x71	POST Code Display	Reserved for COM Express carrier board port 80

Note

1. *You need the congatec CGOS driver and API to access the I²C interface.*

2. *Onboard resources are not connected to the I²C bus.*

4.10 SPI Bus

The conga-B7XI offers the SPI bus through the integrated PCH. The bus supports SPI-compatible flash devices. You can boot the conga-B7XI from the carrier board if you integrate an off-module flash device (BIOS) on the carrier board. This implementation is especially useful when evaluating a customized BIOS.

The conga-B7XI discrete SPI TPM (Infineon SLB9670_VQ2.0) and the congatec BIOS flash are connected to the SPI interface.

Note

This SPI bus is for external BIOS flash only.

4.11 SMBus

The conga-B7XI offers the SMBus for communicating and managing system devices such as thermal sensors, PCIe devices, RAM's serial presence detect.

The SMBus is implemented through the cBC and accessed with the congatec CGOS driver and API.

Table 14 Reserved I²C Addresses

8-bit Device Address	7-bit Device Address	Device	Description
0xA0, 0xA2, 0xA4, 0xA6	0x50, 0x51, 0x52, 0x53	Memory SPD EEPROM	Reserved for SPD EEPROM only if SMBus isolation is not active
0x30, 0x32, 0x34, 0x36	0x18, 0x19, 0x1A, 0x1B	Memory temperature sensors	Reserved for temperature sensors only if SMBus isolation is not active
0x14 0x16	0x0A 0x0B	congatec Board Controller	Reserved for battery management
0x2E	0x60	CPLD debug address	Reserved for CPLD only if SMBus isolation is not active
0xD4	0x6A	PCIe Gen4 clock generator	Reserved for PCIe Gen4 clock generator only if SMBus isolation is not active.
0xDC	0x6E	PCIe clock buffer	
0x10, 0x6C, 0x6E,0x88	0x08, 0x36, 0x37, 0x44	Chipset	Reserved for Intel IceLake-D internal devices only if SMBus isolation is not active.

Note

Make sure the address space of the carrier board SMBus devices does not overlap with the address space of the module devices. For more information, see the COM Express Specification.

4.12 General Purpose Serial Interface

The conga-B7XI offers two UART interfaces (SER0 and SER1) via the congatec Board Controller by default. These interfaces comply with UART 16550 and 16750 protocol. They support up to 115200 bps and can operate in low-speed, full-speed and high-speed modes.

Optionally, the SER0 port can be connected to the Intel Ice Lake-D LCC SoC (configurable via the BIOS setup menu). To connect the SER1 port to the SoC, you need a customized conga-B7X1 (BOM option).

Note

Hardware handshake and flow control are not supported.

4.13 GPIOs

The conga-B7XI offers four General Purpose Outputs and four General Purpose Inputs on the A-B connector. The GPIOs are sourced from the congatec Board Controller.

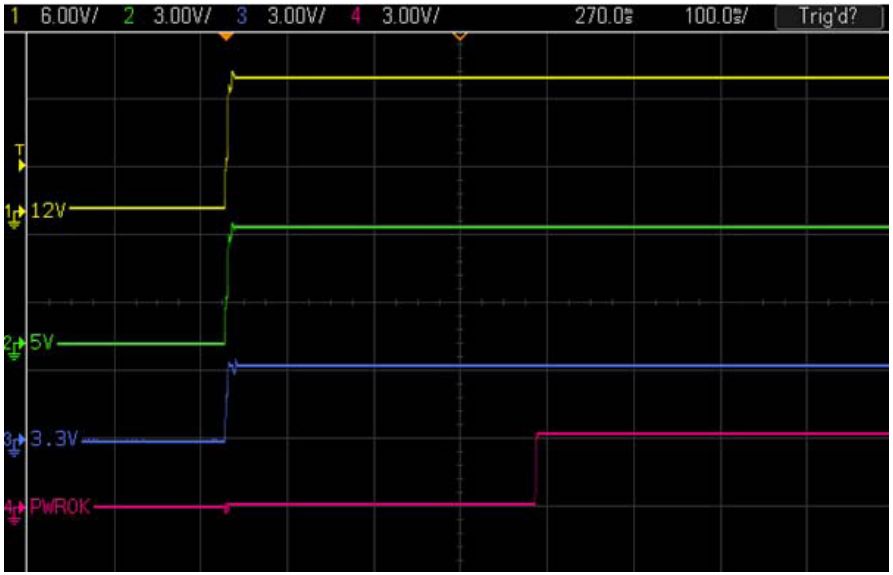
4.14 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system.

A sample screenshot is shown below:



Note

1. *The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.*
2. *Due to the timing requirement of Intel Ice Lake-D SoC, the PWR_OK signal must be active within 100 ms of SUS_S5#/SUS_S4# deassertion.*

Although the PWR_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board

hardware drives the signal low until it is safe to let the module boot-up.

Actively driving PWR_OK high is compliant with the COM Express specification but this can cause back driving. Therefore, congatec recommends driving the PWR_OK low to keep the module in reset and tri-state PWR_OK when the carrier board hardware is ready to boot.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the "power good" signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, make sure that before the 3.3 V goes up, all carrier board hardware is fully powered and all clocks are stable.

The conga-B7XI supports the controlling of ATX-style power supplies. If you do not use an ATX power supply, do not connect the conga-B7XI pins SUS_S3, 5V_SB, and PWRBTN# on the conga-B7XI.

SUS_S3#

The SUS_S3# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. To accomplish this, the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

Note

Intel® Ice Lake SoC does not support the S3 sleep mode.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

The 12 V input power is the sole operational power source for the conga-B7XI. Other required voltages are generated internally on the module using onboard voltage regulators.

Note

When designing a power supply for a conga-B7XI application, be aware that the system may malfunction when a 12V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.

The cause of this problem is that some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.

To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope, during the power supply qualication phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

4.15 Inrush and Maximum Current Peaks

The inrush current on the conga-B7XI can rise as high as 33.60 A on the VCC_12V power rail with a slew rate of 24.85 V/ms and as high as 6.48 A on the VCC_5V_SBY power rail with a slew rate of 34.19 V/ms. Therefore, ensure the power supply and decoupling capacitors on the carrier board are adequate for proper power sequencing.

4.16 Power Management

ACPI

The conga-B7XI supports Advanced Configuration and Power Interface (ACPI) specification, revision 5.0a. For more information, see section 6.2 "ACPI Suspend Modes and Resume Events".

5 Additional Features

5.1 congatec Board Controller (cBC)

The conga-B7XI is equipped with Texas Instruments microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The board controller supports the following features:

- Board information
- Watchdog
- General Purpose Input/Output (see section 4.13 “GPIOs”)
- I²C bus (see section 4.9 “I²C Bus”)
- SMBus (see section 4.11 “SMBus”)
- UART (see section 4.12 “General Purpose Serial Interface”)
- Power loss control
- Fan control

5.1.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

5.1.2 Watchdog

The conga-B7XI is equipped with a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, see the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

Note

The conga-B7XI module does not support watchdog NMI mode.

5.1.3 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The term "power loss" implies that all power sources, including the standby power are lost (G3 state). Once power loss (transition to G3) or shutdown (transition to S5) occurs, the board controller continuously monitors the standby power rail. If the standby voltage remains stable for 30 seconds, the cBC assumes the system was switched off properly. If the standby voltage is no longer detected within 30 seconds, the module considers this an AC power loss condition.

The power loss control feature has three different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to "ON".*
2. *The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.*
3. *The 30 seconds monitoring cycle applies only to the "Last State" power loss control mode.*

5.1.4 Fan Control

The conga-B7XI has additional signals and functions to further improve system management. One of these signals is FAN_PWMOUT, an output signal that allows system fan control using a PWM (Pulse Width Modulation) output. The other signal is the FAN_TACHOIN, an input signal that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

1. *A four wire fan must be used to generate the correct speed readout.*
2. *For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express Design Guide.*

5.2 OEM BIOS Customization

The conga-B7XI is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below.

5.2.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

5.2.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN11_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

5.2.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

5.2.4 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

5.3 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addition to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-B7XI BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery-only solution (no charger). All three battery solutions are supported on the I^2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface, contact your local congatec sales representative.

5.4 API Support (CGOS)

To benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available on the congatec website.

5.5 Security Features

The conga-B7XI offers a discrete SPI TPM 2.0 (Infineon SLB9670VQ2.0) by default.

5.6 Suspend to Ram

The Suspend to RAM feature is not supported on the conga-B7XI.

6 conga Tech Notes

The Intel Ice Lake D-LCC SoC supports the following core features:

- Virtual and physical address space of 48 bits
- Intel 64 architecture with support for IA-32 instruction set
- Instruction Set Architecture (ISA) enhancements accelerating producer-consumer communication
- Intel Streaming SIMD Extensions 4.1 and 4.2 (SSE4.1 and SSE4.2)
- Intel Advanced Vector Extensions 512 (Intel AVX-512)
- AVX 512 Vector Byte Manipulation Instructions
- Vector Neural Network Instructions
- Intel Advanced Encryption Standard New Instructions (Intel AES-NI)
- Intel Secure Hash Algorithm New Instructions (SHA-NI)
- Intel Software Guard Extensions (Intel SGX)
- Intel Virtualization Technology (Intel VT-x) for Intel 64 and IA-32 Intel Architecture (Intel VT-x)
- Execute Disable Bit
- Package Power States (C-States)
- Intel Speed Select Technology (Intel SST)
- Intel Turbo Boost Technology
- Intel Hyper-Threading Technology (Intel HT Technology

6.1 Intel® Ice Lake D-LCC Technologies

This section describes some of the technological features the Intel Ice Lake D-LCC supports.

6.1.1 Adaptive Thermal Monitor and Catastrophic Thermal Protection

Intel® Xeon processors have a thermal monitor feature that helps to control the processor's temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu "CPU submenu".

The Adaptive Thermal Monitor controls the processor temperature using two methods:

- Adjusting the processor's operating frequency and core voltage (EIST transitions)
- Modulating (start or stop) the processor's internal clocks at a duty cycle of 25% on and 75% off

When activated, the TCC causes the processor core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated. Clock modulation is activated if frequency and voltage adjustments are insufficient. Additional hardware, software drivers, or operating system support is not required.

Note

1. *Use a properly designed thermal solution for adequate heat dissipation. This solution ensures the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum. The Intel® Xeon processor's respective datasheet can provide you with more information about this subject.*

2. *To enable THERMTRIP# to switch off the system automatically, use an ATX style power supply.*

6.1.2 Intel SpeedStep Technology (EIST)

Intel® processors on the conga-B7XI run at different voltage/frequency states (performance states), referred to as Enhanced Intel® SpeedStep® Technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it is not being fully used.

The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime. The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that the power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

The Next Generation Intel® Core™ processor family supports Intel Speed Shift, a new and energy efficient method for frequency control. This feature is also referred to as Hardware-controlled Performance States (HWP). It is a hardware implementation of the ACPI defined Collaborative Processor Performance Control (CPPC2) and is supported by newer operating systems (Win 8.1 or newer).

With this feature enabled, the processor autonomously selects performance states based on workload demand and thermal limits while also considering information provided by the Operating System (for example, the performance limits and workload history).

6.1.3 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits. Intel® Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state. The maximum frequency of Intel® Turbo Boost Technology is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost 2 Technology state depends on the workload and operating environment. Any of the following can set the upper limit of Intel® Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase by 100 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached. For more information about Intel® Turbo Boost 2 Technology visit the Intel® website.

Note

1. *Refer to section 1.8 "Power Consumption" for information about the maximum turbo frequency available for each conga-B7XI variant.*
2. *For real-time sensitive applications, disable EIST and Turbo Mode in the BIOS setup to ensure a more deterministic performance.*
3. *Disable Turbo mode for industrial use conditions.*

6.1.4 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel VT and is verified on all current congatec x86 hardware.

Note

congatec supports RTS Hypervisor.

6.2 ACPI Suspend Modes and Resume Events

The conga-B7XI BIOS does not support S3 (Suspend to RAM) and S4 (Suspend to Disk). S5 is however supported. The table below lists the events that wake the system from S5.

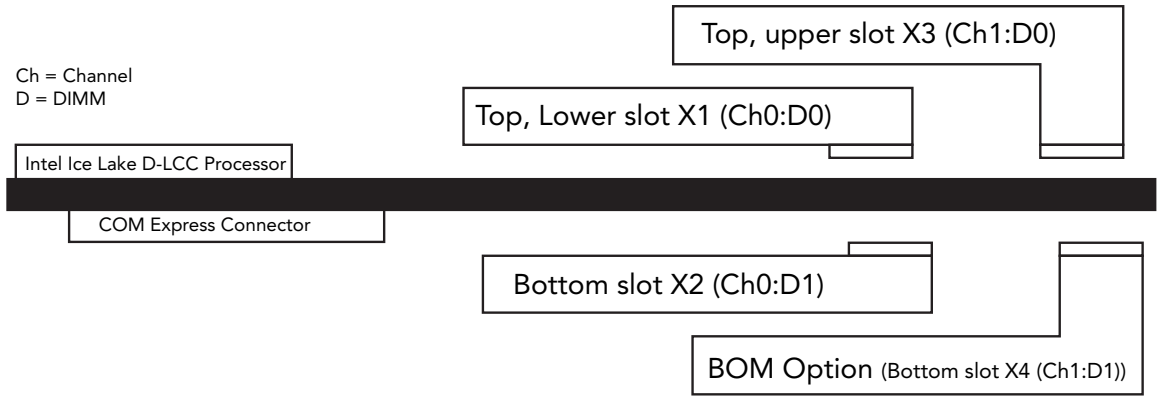
Table 15 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device or enable 'Resume On PME#' in the Power setup menu.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Wakes unconditionally from S5.
Watchdog Power Button Event	Wakes unconditionally from S5

6.3 Memory Population Rules

The Intel Ice Lake-D LCC SoC featured on the conga-B7XI supports ECC and non-ECC DDR4 memory modules, up to 2933 MTps. The DDR4 memory modules have lower voltage requirements with higher data rate transfer speeds.

The diagram below shows the location of the memory slots on the conga-B7XI.



The following population rules must be observed:

- All DIMMs in a channel must have same width (x4, x8 or x16)
- Do not mix ECC and non-ECC memory modules.
- Mixing single and dual rank DIMMs is allowed but may reduce the memory speed
- Mixing memory densities (8 Gb vs 16 Gb) within a channel is allowed
- Either channel 0 or channel 1, or both can be populated.

7 Signal Descriptions and Pinout Tables

The following section describes the signals found on the conga-B7XI. The pinout of the module complies with COM Express Type 7, rev. 3.0.

The table below describes the terminology used in this section. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors; only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 16 Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
T	Higher voltage tolerance
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0
REF	Reference voltage output. May be sourced from a module's power plane.
KR	10GBASE-KR compatible signal
PDS	Pull-down strap. A module output pin that is either tied to GND or left unconnected. It is used to indicate the module's capabilities (pinout type) to the carrier board.

7.1 Connectors Signal Descriptions

Table 17 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100# [3]	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000# [3]	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND(FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF [1]	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3# [2]	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	PCIE_TX8+	B71	PCIE_RX8+
A17	SATA0_TX-	B17	SATA1_TX-	A72	PCIE_TX8-	B72	PCIE_RX8-
A18	SUS_S4#	B18	SUS_STAT# [4]	A73	GND	B73	GND
A19	SATA0_RX+	B19	SATA1_RX+	A74	PCIE_TX9+	B74	PCIE_RX9+
A20	SATA0_RX-	B20	SATA1_RX-	A75	PCIE_TX9-	B75	PCIE_RX9-
A21	GND (FIXED)	B21	GND (FIXED)	A76	GND	B76	GND
A22	PCIE_TX15+	B22	PCIE_RX15+	A77	PCIE_TX10+	B77	PCIE_RX10+
A23	PCIE_TX15-	B23	PCIE_RX15-	A78	PCIE_TX10-	B78	PCIE_RX10-
A24	SUS_S5#	B24	PWR_OK	A79	GND	B79	GND
A25	PCIE_TX14+	B25	PCIE_RX14+	A80	GND (FIXED)	B80	GND (FIXED)
A26	PCIE_TX14-	B26	PCIE_RX14-	A81	PCIE_TX11+	B81	PCIE_RX11+
A27	BATLOW#	B27	WDT	A82	PCIE_TX11-	B82	PCIE_RX11-
A28	(S)ATA_ACT#	B28	RSVD [1]	A83	GND	B83	GND
A29	RSVD [1]	B29	RSVD [1, 3]	A84	NCSI_TX_EN	B84	VCC_5V_SBY
A30	RSVD [1]	B30	RSVD [1, 3]	A85	GPI3	B85	VCC_5V_SBY

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD [1]	B86	VCC_5V_SBY
A32	RSVD [1, 3]	B32	SPKR	A87	RSVD [1, 3]	B87	VCC_5V_SBY
A33	RSVD [1, 3]	B33	I2C_CK	A88	PCIE_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE_CK_REF-	B89	NCSI_RX_ER
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	PCIE_TX13+	B36	PCIE_RX13+	A91	SPI_POWER	B91	NCSI_CLK_IN
A37	PCIE_TX13-	B37	PCIE_RX13-	A92	SPI_MISO	B92	NCSI_RXD1
A38	GND	B38	GND	A93	GPO0	B93	NCSI_RXD0
A39	PCIE_TX12+	B39	PCIE_RX12+	A94	SPI_CLK	B94	NCSI_CRS_DV
A40	PCIE_TX12-	B40	PCIE_RX12-	A95	SPI_MOSI	B95	NCSI_TXD1
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	NCSI_TXD0
A42	USB2-	B42	USB3-	A97	TYPE10# [1]	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	NCSI_ARB_IN
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	NCSI_ARB_OUT [4]
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI_EN# [1]	A102	SER1_RX	B102	FAN_TACHIN
A48	RSVD [1]	B48	USB0_HOST_PRSNT [1]	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

1. *Not connected*
2. *Not supported*
3. *See section 8 “COM 3.1 Variants”*
4. *Boot strap signal*

Table 18 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PCIE_RX17-	D56	PCIE_TX17-
C2	GND	D2	GND	C57	TYPE1# [1]	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PCIE_RX18+	D58	PCIE_TX18+
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PCIE_RX18-	D59	PCIE_TX18-
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PCIE_RX19+	D61	PCIE_TX19+
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PCIE_RX19-	D62	PCIE_TX19-
C8	GND	D8	GND	C63	RSVD [3]	D63	RSVD [3]
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	RSVD [3]	D64	RSVD [3]
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	PCIE_RX20+	D65	PCIE_TX20+
C11	GND(FIXED)	D11	GND (FIXED)	C66	PCIE_RX20-	D66	PCIE_TX20-
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RAPID_SHUTDOWN	D67	GND
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	PCIE_RX21+	D68	PCIE_TX21+
C14	GND	D14	GND	C69	PCIE_RX21-	D69	PCIE_TX21-
C15	10G_PHY_MDC_SCL3 [3, 4]	D15	10G_PHY_MDIO_SDA3 [3, 4]	C70	GND (FIXED)	D70	GND (FIXED)
C16	10G_PHY_MDC_SCL2 [3, 4]	D16	10G_PHY_MDIO_SDA2 [3, 4]	C71	PCIE_RX22+	D71	PCIE_TX22+
C17	10G_SDP2 [2, 4]	D17	10G_SDP3 [2, 4]	C72	PCIE_RX22-	D72	PCIE_TX22-
C18	GND	D18	GND	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	PCIE_RX23+	D74	PCIE_TX23+
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	PCIE_RX23-	D75	PCIE_TX23-
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+	D22	PCIE_TX7+	C77	RSVD [3]	D77	RSVD [3]
C23	PCIE_RX7-	D23	PCIE_TX7-	C78	PCIE_RX24+	D78	PCIE_TX24+
C24	10G_INT2 [3]	D24	10G_INT3 [3]	C79	PCIE_RX24-	D79	PCIE_TX24-
C25	GND	D25	GND	C80	GND (FIXED)	D80	GND (FIXED)
C26	10G_KR_RX3+	D26	10G_KR_TX3+	C81	PCIE_RX25+	D81	PCIE_TX25+
C27	10G_KR_RX3-	D27	10G_KR_TX3-	C82	PCIE_RX25-	D82	PCIE_TX25-
C28	GND	D28	GND	C83	RSVD [3]	D83	RSVD [3]
C29	10G_KR_RX2+	D29	10G_KR_TX2+	C84	GND	D84	GND
C30	10G_KR_RX2-	D30	10G_KR_TX2-	C85	PCIE_RX26+	D85	PCIE_TX26+
C31	GND (FIXED)	D31	GND (FIXED)	C86	PCIE_RX26-	D86	PCIE_TX26-
C32	10G_SFP_SDA3 [3]	D32	10G_SFP_SCL3 [3]	C87	GND	D87	GND

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C33	10G_SFP_SDA2 [3]	D33	10G_SFP_SCL2 [3]	C88	PCIE_RX27+	D88	PCIE_TX27+
C34	10G_PHY_RST_23 [3]	D34	10G_PHY_CAP_23 [1, 3]	C89	PCIE_RX27-	D89	PCIE_TX27-
C35	10G_PHY_RST_01 [3]	D35	10G_PHY_CAP_01 [3]	C90	GND (FIXED)	D90	GND (FIXED)
C36	10G_LED_SDA [3]	D36	RSVD [1]	C91	PCIE_RX28+	D91	PCIE_TX28+
C37	10G_LED_SCL [3]	D37	RSVD [1]	C92	PCIE_RX28-	D92	PCIE_TX28-
C38	10G_SFP_SDA1 [3]	D38	10G_SFP_SCL1 [3]	C93	GND	D93	GND
C39	10G_SFP_SDA0 [3]	D39	10G_SFP_SCL0 [3]	C94	PCIE_RX29+	D94	PCIE_TX29+
C40	10G_SDP0 [2, 4]	D40	10G_SDP1 [2, 4]	C95	PCIE_RX29-	D95	PCIE_TX29-
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	10G_KR_RX1+	D42	10G_KR_TX1+	C97	RSVD [3]	D97	RSVD [3]
C43	10G_KR_RX1-	D43	10G_KR_TX1-	C98	PCIE_RX30+	D98	PCIE_TX30+
C44	GND	D44	GND	C99	PCIE_RX30-	D99	PCIE_TX30-
C45	10G_PHY_MDC_SCL1 [3, 4]	D45	10G_PHY_MDIO_SDA1 [3, 4]	C100	GND (FIXED)	D100	GND (FIXED)
C46	10G_PHY_MDC_SCL0 [3, 4]	D46	10G_PHY_MDIO_SDA0 [3, 4]	C101	PCIE_RX31+	D101	PCIE_TX31+
C47	10G_INT0 [3]	D47	10G_INT1 [3]	C102	PCIE_RX31-	D102	PCIE_TX31-
C48	GND	D48	GND	C103	GND	D103	GND
C49	10G_KR_RX0+	D49	10G_KR_TX0+	C104	VCC_12V	D104	VCC_12V
C50	10G_KR_RX0-	D50	10G_KR_TX0-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND(FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PCIE_RX16+	D52	PCIE_TX16+	C107	VCC_12V	D107	VCC_12V
C53	PCIE_RX16-	D53	PCIE_TX16-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	RSVD [1]	C109	VCC_12V	D109	VCC_12V
C55	PCIE_RX17+	D55	PCIE_TX17+	C110	GND (FIXED)	D110	GND (FIXED)

Note

1. *Not connected*
2. *Not supported*
3. *See section 8 “COM 3.1 Variants”*
4. *Boot strap signal*

Table 19 Gigabit Ethernet [1] Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10 Mbps modes. Some pairs are unused in some modes according to the following:				I/O Analog		
			1000BASE-T	100BASE-TX	10BASE-T			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				OD 3.3 V		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.				OD 3.3 V		
GBE0_LINK100# [2]	A4	Gigabit Ethernet Controller 0 100 Mbps link indicator, active low.				OD 3.3 V		
GBE0_LINK1000# [2]	A5	Gigabit Ethernet Controller 0 1000 Mbps link indicator, active low.				OD 3.3 V		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0 V and as high as 3.3 V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.				REF		Not connected
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1 pps signal.				I/O		

Note

1. *The MAC address of the Intel i226 Ethernet controller is preprogrammed by default. The MAC address cannot be reprogrammed. If you require custom MAC address, contact your local sales representative.*

2. *See section 8 "COM 3.1 Variants" for more information.*

Table 20 NC-SI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
NCSI_CLK_IN	B91	NC-SI Clock reference for receive, transmit, and control interface.	I 3.3 VSB	PD 10K	
NCSI_RXD0 NCSI_RXD1	B93 B92	NC-SI Receive Data (from NC to BMC)	O 3.3 VSB		
NCSI_TXD0 NCSI_TXD1	B96 B95	NC-SI Transmit Data (from BMC to NC).	I 3.3VSB	PD 10K	
NCSI_CRS_DV	B94	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.	O 3.3VSB		

Signal	Pin #	Description	I/O	PU/PD	Comment
NCSI_TX_EN	A84	NC-SI Transmit enable.	I 3.3VSB	PD 10K	
NCSI_RX_ER	B89	NC-SI Receive error.	O 3.3VSB		
NCSI_ARB_IN	B98	NC-SI hardware arbitration input.	I 3.3VSB	PD 10K	
NCSI_ARB_OUT	B99	NC-SI hardware arbitration output.	O 3.3VSB	PU 10K 3.3VSB	Boot strap signal

Table 21 10 Gigabit Ethernet Signal Descriptions (COM Rev. 3.0)

Signal	Pin #	Description	I/O	PU/PD	Comment
10G_KR_TX0+ 10G_KR_TX0-	D49 D50	10GBASE-KR ports, transmit output differential pairs 0	O KR		
10G_KR_RX0+ 10G_KR_RX0-	C49 C50	10GBASE-KR ports, receive input differential pairs 0	I KR		
10G_KR_TX1+ 10G_KR_TX1-	D42 D43	10GBASE-KR ports, transmit output differential pairs 1	O KR		
10G_KR_RX1+ 10G_KR_RX1-	C42 C43	10GBASE-KR ports, receive input differential pairs 1	I KR		
10G_KR_TX2+ 10G_KR_TX2-	D29 D30	10GBASE-KR ports, transmit output differential pairs 2	O KR		
10G_KR_RX2+ 10G_KR_RX2-	C29 C30	10GBASE-KR ports, receive input differential pairs 2	I KR		
10G_KR_TX3+ 10G_KR_TX3-	D26 D27	10GBASE-KR ports, transmit output differential pairs 3	O KR		
10G_KR_RX3+ 10G_KR_RX3-	C26 C27	10GBASE-KR ports, receive input differential pairs 3	I KR		
10G_PHY_MDIO_SDA[0:3] [1]	D46 D45 D16 D15	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O 3.3VSB		Boot strap signals
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD 3.3VSB	PU 1K 3.3VSB	
10G_PHY_MDC_SCL[0:3] [1]	C46 C45 C16 C15	MDIO Mode: Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY.	O 3.3VSB		Boot strap signals
		I2C Mode: I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD 3.3VSB	PU 1K 3.3VSB	

10G_PHY_CAP_01	D35	PHY mode capability pin: Indicates if the PHY for 10G lanes 0 and 1 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configuration capability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module. Based on this input, the actual protocol used is indicated over the dedicated I²C interface.	I 3.3VSB		Not connected
10G_PHY_CAP_23	D34	Phy mode capability pin: Indicates if the PHY for 10G lanes 2 and 3 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configuration capability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module. Based on this input, the actual protocol used is indicated over the dedicated I²C interface.	I 3.3VSB		Not connected
10G_SFP_SDA[0:3]	C39 C38 C33 C32	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP module.	I/O OD 3.3VSB	PU 10K 3.3VSB	
10G_SFP_SCL[0:3]	D39 D38 D33 D32	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP module.	I/O OD 3.3VSB	PU 10K 3.3VSB	
10G_LED_SDA	C36	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs.	I/O OD 3.3VSB	PU 2K2 3.3VSB	
10G_LED_SCL	C37	I2C Clock of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs.	I/O OD 3.3VSB	PU 2K2 3.3VSB	
10G_INT[0:3]	C47 D47 C24 D24	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.	I 3.3VSB	PU 2K2 3.3VSB	Boot strap signals
10G_SDP[0:3] [1, 2]	C40 D40 C17 D17	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.	I/O 3.3VSB	PU 10K 3.3VSB	Not supported
10G_PHY_RST_01	C35	Output signal that resets an optical PHY on port 0 and port1 (with copper PHY this signal is not used).	O 3.3VSB	PU 10K 3.3VSB	
10G_PHY_RST_23	C34	Output signal that resets an Optical PHY on port 2 and port 3 (with copper PHY this signal is not used).	O 3.3VSB		Not connected

Note

1. *This signal has special function during the reset process. For more information, see section 7.2 "Boot Strap Signals"".*
2. *The conga-B7XI does not support 10G_SDP[0:3].*

Table 22 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	I/O 3.3V		

Table 23 PCI Express Signal Descriptions (General Purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express Transmit Output Differential Pairs 0	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express Receive Input Differential Pairs 0	I PCIE		
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express Transmit Output Differential Pairs 1	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express Receive Input Differential Pairs 1	I PCIE		
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express Transmit Output Differential Pairs 2	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express Receive Input Differential Pairs 2	I PCIE		
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express Transmit Output Differential Pairs 3	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express Receive Input Differential Pairs 3	I PCIE		
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express Transmit Output Differential Pairs 4	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express Receive Input Differential Pairs 4	I PCIE		
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express Transmit Output Differential Pairs 5	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express Receive Input Differential Pairs 5	I PCIE		

PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express Transmit Output Differential Pairs 6	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express Receive Input Differential Pairs 6	I PCIE		
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express Transmit Output Differential Pairs 7	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express Receive Input Differential Pairs 7	I PCIE		
PCIE_TX8+ PCIE_TX8-	A71 A72	PCI Express Transmit Output Differential Pairs 8	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX8+ PCIE_RX8-	B71 B72	PCI Express Receive Input Differential Pairs 8	I PCIE		
PCIE_TX9+ PCIE_TX9-	A74 A75	PCI Express Transmit Output Differential Pairs 9	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX9+ PCIE_RX9-	B74 B75	PCI Express Receive Input Differential Pairs 9	I PCIE		
PCIE_TX10+ PCIE_TX10-	A77 A78	PCI Express Transmit Output Differential Pairs 10	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX10+ PCIE_RX10-	B77 B78	PCI Express Receive Input Differential Pairs 10	I PCIE		
PCIE_TX11+ PCIE_TX11-	A81 A82	PCI Express Transmit Output Differential Pairs 11	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX11+ PCIE_RX11-	B81 B82	PCI Express Receive Input Differential Pairs 11	I PCIE		
PCIE_TX12+ PCIE_TX12-	A39 A40	PCI Express Transmit Output Differential Pairs 12	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX12+ PCIE_RX12-	B39 B40	PCI Express Receive Input Differential Pairs 12	I PCIE		
PCIE_TX13+ PCIE_TX13-	A36 A37	PCI Express Transmit Output Differential Pairs 13	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX13+ PCIE_RX13-	B36 B37	PCI Express Receive Input Differential Pairs 13	I PCIE		
PCIE_TX14+ PCIE_TX14-	A25 A26	PCI Express Transmit Output Differential Pairs 14	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX14+ PCIE_RX14-	B25 B26	PCI Express Receive Input Differential Pairs 14	I PCIE		
PCIE_TX15+ PCIE_TX15-	A22 A23	PCI Express Transmit Output Differential Pairs 15	O PCIE		Supports PCI Express Base Specification, Revision 3.0.
PCIE_RX15+ PCIE_RX15-	B22 B23	PCI Express Receive Input Differential Pairs 15	I PCIE		
PCIE_TX16+ PCIE_TX16-	D52 D53	PCI Express Transmit Output Differential Pairs 16	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX16+ PCIE_RX16-	C52 C53	PCI Express Receive Input Differential Pairs 16	I PCIE		

PCIE_TX17+ PCIE_TX17-	D55 D56	PCI Express Transmit Output Differential Pairs 17	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX17+ PCIE_RX17-	C55 C56	PCI Express Receive Input Differential Pairs 17	I PCIE		
PCIE_TX18+ PCIE_TX18-	D58 D59	PCI Express Transmit Output Differential Pairs 18	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX18+ PCIE_RX18-	C58 C59	PCI Express Receive Input Differential Pairs 18	I PCIE		
PCIE_TX19+ PCIE_TX19-	D61 D62	PCI Express Transmit Output Differential Pairs 19	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX19+ PCIE_RX19-	C61 C62	PCI Express Receive Input Differential Pairs 19	I PCIE		
PCIE_TX20+ PCIE_TX20-	D65 D66	PCI Express Transmit Output Differential Pairs 20	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX20+ PCIE_RX20-	C65 C66	PCI Express Receive Input Differential Pairs 20	I PCIE		
PCIE_TX21+ PCIE_TX21-	D68 D69	PCI Express Transmit Output Differential Pairs 21	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX21+ PCIE_RX21-	C68 C69	PCI Express Receive Input Differential Pairs 21	I PCIE		
PCIE_TX22+ PCIE_TX22-	D71 D72	PCI Express Transmit Output Differential Pairs 22	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX22+ PCIE_RX22-	C71 C72	PCI Express Receive Input Differential Pairs 22	I PCIE		
PCIE_TX23+ PCIE_TX23-	D74 D75	PCI Express Transmit Output Differential Pairs 23	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX23+ PCIE_RX23-	C74 C75	PCI Express Receive Input Differential Pairs 23	I PCIE		
PCIE_TX24+ PCIE_TX24-	D78 D79	PCI Express Transmit Output Differential Pairs 24	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX24+ PCIE_RX24-	C78 C79	PCI Express Receive Input Differential Pairs 24	I PCIE		
PCIE_TX25+ PCIE_TX25-	D81 D82	PCI Express Transmit Output Differential Pairs 25	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX25+ PCIE_RX25-	C81 C82	PCI Express Receive Input Differential Pairs 25	I PCIE		
PCIE_TX26+ PCIE_TX26-	D85 D86	PCI Express Transmit Output Differential Pairs 26	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX26+ PCIE_RX26-	C85 C86	PCI Express Receive Input Differential Pairs 26	I PCIE		

PCIE_TX27+ PCIE_TX27-	D88 D89	PCI Express Transmit Output Differential Pairs 27	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX27+ PCIE_RX27-	C88 C89	PCI Express Receive Input Differential Pairs 27	I PCIE		
PCIE_TX28+ PCIE_TX28-	D91 D92	PCI Express Transmit Output Differential Pairs 28	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX28+ PCIE_RX28-	C91 C92	PCI Express Receive Input Differential Pairs 28	I PCIE		
PCIE_TX29+ PCIE_TX29-	D94 D95	PCI Express Transmit Output Differential Pairs 29	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX29+ PCIE_RX29-	C94 C95	PCI Express Receive Input Differential Pairs 29	I PCIE		
PCIE_TX30+ PCIE_TX30-	D98 D99	PCI Express Transmit Output Differential Pairs 30	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX30+ PCIE_RX30-	C98 C99	PCI Express Receive Input Differential Pairs 30	I PCIE		
PCIE_TX31+ PCIE_TX31-	D101 D102	PCI Express Transmit Output Differential Pairs 31	O PCIE		Supports PCI Express Base Specification, Revision 3.0. PCIe Gen 4 support with customized conga-B7XI.
PCIE_RX31+ PCIE_RX31-	C101 C102	PCI Express Receive Input Differential Pairs 31	I PCIE		
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if the design involves more than one PCI Express device.

Table 24 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB Port 0, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+ USB1-	B46 B45	USB Port 1, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+ USB2-	A43 A42	USB Port 2, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+ USB3-	B43 B42	USB Port 3, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10K 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10K 3.3VSB	Do not pull this line high on the carrier board.

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0_HOST_PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present	I 3.3VSB		Not connected
USB_SSRX0+ USB_SSRX0-	C4 C3	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX0+ USB_SSTX0-	D4 D3	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSRX1+ USB_SSRX1-	C7 C6	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX1+ USB_SSTX1-	D7 D6	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSRX2+ USB_SSRX2-	C10 C9	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX2+ USB_SSTX2-	D10 D9	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSRX3+ USB_SSRX3-	C13 C12	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX3+ USB_SSTX3-	D13 D12	Additional transmit signal differential pairs for the Superspeed USB data path	O		

Table 25 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V	PU 10K 3.3V	
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V	PU 10K 3.3V	
LPC_CLK	B10	LPC clock output - 24 MHz nominal	O 3.3V	PD 10K	
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V	PU 10K 3.3V	
LPC_SERIRQ	A50	LPC serial interrupt	I/O OD 3.3V	PU 10K 3.3V	
SUS_STAT# [1]	B18	In LPC mode, SUS_STAT# indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state.	O 3.3VSB	PD 10K	Boot strap signal
ESPI_EN#	B47	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The Carrier should only float this line or pull it low.	I 1.8V		Not connected
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device	I 3.3VSB		Not supported
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device	I 3.3VSB	PU 10K 3.3VSB	

Note

1. *This signal has special function during the reset process. For more information, see section 7.2 "Boot Strap Signals".*

Table 26 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS flash	O 3.3VSB		Carrier shall pull to SPI_POWER when external SPI is provided but not used.
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash	I 3.3VSB	PU 10K 3.3VSB	
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flas	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	O 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device	I 3.3VSB		Not supported
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device	I 3.3VSB	PU 10K 3.3VSB	

Table 27 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX [1, 2]	A98	General purpose serial port transmitter	O 3.3V-T		
SER0_RX [1]	A99	General purpose serial port receiver	I 3.3V-T	PU 47K 3.3V	
SER1_TX [1, 2]	A101	General purpose serial port transmitter	O 3.3V-T		
SER1_RX [1]	A102	General purpose serial port receiver	I 3.3V-T	PU 47K 3.3V	

Note

1. *Pins are protected on the module by a series schottky diode.*
2. *Requires pull-down resistor on the carrier board for proper logic level.*

Table 28 I²C Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output	I/O 3.3VSB	PU 2K21 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O 3.3VSB	PU 2K21 3.3VSB	

Table 29 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V	PD 10K	Not supported
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PD 100K	
FAN_PWMOUT [1,2]	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V		
FAN_TACHIN [1]	B102	Fan tachometer input.	I OD 3.3V	PU 47K 3.3V	Requires a fan with a two pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 1K	

Note

1. *Pins are protected on the module by a series schottky diode.*
2. *Requires pull-down resistor on the carrier board for proper logic level.*

Table 30 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V	PD 10K	
PWR_OK [1]	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to delay the startup of the of module to enable the programming of FPGAs or other configurable devices on the carrier board.	I 3.3V		Set by resistor divider to accept 3.3V.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices. Not used in eSPI implementations.	O 3.3VSB	PD 10K	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB	PD 1K	Suspend to RAM is not supported. Signals can be used for Sx state indicator.
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		Suspend to Disk is not supported. Signals can be used for Sx state indicator.
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB	PD 1K	

Signal	Pin #	Description	I/O	PU/PD	Comment
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10K 3.3VSB	
BATLOW#	A27	Runtime event of the battery sub-system.	I 3.3VSB	PU 10K 3.3VSB	Unlike in mobile platforms, the signal does not influence the power-up behavior of the module.
LID# [1]	A103	Lid button. Used by the ACPI operating system for a LID switch. Note: For proper detection, assert a pulse width of at least 16 ms.	I OD 3.3V	PU 47K 3.3VSB	
SLEEP# [1]	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again. Note: For proper detection, assert a pulse width of at least 16 ms.	I OD 3.3V	PU 100K 3.3VSB	

Note

1. *Pins are protected on the module by a series schottky diode.*

Table 31 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_SHUTDOWN	C67	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs.	I 3.3VSB		Not supported (for internal debugging only)

Table 32 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 10K 3.3V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10K 3.3V	

Table 33 SMBus Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line.	I/O 3.3VSB	PU 100K 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line.	I/O OD 3.3VSB	PU 100K 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3VSB	PU 100K 3.3VSB	

Table 34 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins	O 3.3V		
GPO1	B54	General purpose output pins	O 3.3V		
GPO2	B57	General purpose output pins	O 3.3V		
GPO3	B63	General purpose output pins	O 3.3V		
GPI0	A54	General purpose input pins. Pulled high internally on the module	I 3.3V	PU 100K 3.3V	
GPI1	A63	General purpose input pins. Pulled high internally on the module	I 3.3V	PU 100K 3.3V	
GPI2	A67	General purpose input pins. Pulled high internally on the module	I 3.3V	PU 100K 3.3V	
GPI3	A85	General purpose input pins. Pulled high internally on the module	I 3.3V	PU 100K 3.3V	

Note

The conga-B7XI does not support SDIO.

Table 35 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109 C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A38, A41, A51, A57, A60, A66, A70, A73, A76, A79, A80, A83, A90, A100, A110, B1, B11, B21, B31, B38, B41, B51, B60, B70, B73, B76, B79, B80, B83, B90, B100, B110, C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

Table 36 Module Type Definition Signal Description

<table>
<tr><th>Signal</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>TYPE0#
TYPE1#
TYPE2#</td><td>C54
C57
D57</td><td>The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1 and Type 10, these pins are don’t care (X).
<table>
<tr><th>TYPE2#</th><th>TYPE1#</th><th>TYPE0#</th><th></th></tr>
<tr><td>X
NC
NC
NC
NC
GND
GND
X</td><td>X
NC
NC
GND
GND
NC
NC
X</td><td>X
NC
GND
NC
GND
NC
GND
X</td><td>Pinout Type 1 (deprecated)
Pinout Type 2 (deprecated)
Pinout Type 3 (deprecated)
Pinout Type 4 (deprecated)
Pinout Type 5 (deprecated)
Pinout Type 6
Pinout Type 7
Pinout Type 10</td></tr>
</table>
The carrier board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The carrier board logic may also implement a fault indicator such as an LED.</td><td>PDS</td><td>TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard.
The conga-B7XI is based on the COM Express Type 7 pinout, therefore pins C54 and D57 are connected to GND and pin C57 is not connected.</td></tr>
<tr><td>TYPE10#</td><td>A97</td><td>Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed.
<table>
<tr><th>TYPE10#</th><th></th></tr>
<tr><td>NC
PD
12V</td><td>Pinout R2.0
Pinout Type 10 pull down to ground with 4.7K resistor
Pinout R1.0</td></tr>
</table>
This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. R3.0 module types 6 and 7 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7K resistor.</td><td>PDS</td><td>Not connected to indicate “Pinout R2.0”.</td></tr>
</table>

7.2 Boot Strap Signals

Table 37 Boot Strap Signal Descriptions

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
10G_SDP0	C40	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.	I/O 3.3 VSB	PU 10K VSB	
10G_SDP1	D40			PD 1K	
10G_SDP3	D17			PU 10K VSB	
10G_SDP2	C17			PU 10K VSB	
10G_PHY_MDIO_SDA0	D46	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O 3.3 VSB	PU 1K VSB	
10G_PHY_MDIO_SDA1	D45			PU 1K VSB	
10G_PHY_MDIO_SDA2	D16			PU 1K VSB	
10G_PHY_MDIO_SDA3	D15			PU 1K VSB	
10G_PHY_MDC_SCL0	C46	Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY	O 3.3 VSB	PU 1K VSB	
10G_PHY_MDC_SCL1	C45			PU 1K VSB	
10G_PHY_MDC_SCL2	C16			PU 1K VSB	
10G_PHY_MDC_SCL3	C15			PU 1K VSB	
NCSI_ARB_OUT	B99	NC-SI hardware arbitration output	O 3.3 VSB	PU 10K VSB	
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3 VSB	PD 10K	

Note

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), the COM Express or chipset internally implemented resistors pull these signals to the correct state.

Caution

No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM Express module to malfunction or cause irreparable damage to the module.

8 COM 3.1 Variants

The conga-B7XI supports the COM Express Specification 3.1 by default with PN: 050221 or through a customized conga-B7XI. This section outlines the supported Ethernet configurations and compares the pinout differences between COM Express Specification 3.0 and COM Express Specification 3.1.

8.1 Possible Ethernet Configurations

Table 38 Supported Ethernet Configurations

Intel HW Config ID	Medium	Interface	Possible Link Modes	Rate	Carrier Board	Comment
CFG 7.0 [1, 2]	Parkvale C827-AM/XL827-AM	4x SFP+	10G-SFI-DA	10 Gb	COM 3.1	Full CEI support. Requires a customized variant (COM 3.1) or the variant with PN: 050221, BIOS update and corresponding NVM image
			10GBASE-SR/LR			
			10G-SFI-ACC/AOC			
			1000BASE-SX/LX	1 Gb		
	Coppervale X557-AT4	4x 10GBASE-T	10GBASE-T	10 Gb		
			1000BASE-T	1 Gb		
	Marwell 88E1543	4x 1000BASE-T	1000BASE-T	1 Gb		
			100BASE-TX	100 Mb		
CFG 7.6 [3, 4]	Backplane	10GBASE-KR	10GBASE-KR	10 Gb	COM 3.0 and COM 3.1	
			2500BASE-X	2.5 Gb		
			1000BASE-KX	1 Gb		
CFG 5.1 (default) [3]	Native SFI	4x SFP+	10G-SFI-DA	10 Gb	COM 3.1	With I/O expander (leveraging the CEI concept without a PHY on the carrier board) **Note:** Requires a customized conga-B7XI COM 3.1 variant or the variant with PN: 050221, BIOS update and corresponding NVM image.
			10GBASE-SR/LR			
			10G-SFI-ACC/AOC			
			1000BASE-SX/LX	1 Gb		

Note

1. *The conga-B7XI COM 3.0 modules do not support CEI. For CEI support, you need a customized variant (BOM option).*
2. *Appropriate NVM image must be used. For instructions on how to deploy 10 GbE LAN NVM and PHY NVM images, refer to congatec CTN 20180726 001 document in the restricted area of our website.*
3. *The Intel Ice Lake SoC on the conga-B7XI does not support the INPHY CS4227 PHY featured on the conga-X7EVAL. If you use the conga-B7XI in combination with the conga-X7EVAL and you require 10 Gb SFI connection, use the congatec DFSI interposer card for native SFI connection. For more information, contact your sales representative.*
4. *To change from configuration CFG 7.6 to CFG 7.0 or CFG 5.1, you need a customized conga-B7XI and a modified NVM image.*

8.2 COM 3.1 CEI Signals

The conga-B7XI COM 3.1 variants support the following CEI signals:

COM 3.0	COM 3.1 CEI Implementation					
	CFG 7.0				CFG 5.1 (native SFI without PHY)	CFG 7.6
	4x SFP+ with Parkville	4x 10GBASE-T with Coppervale	4x 1000BASE-T with Marvell	1x or 2x QSFP with Parkville	4x SFP+ with Expander	Backplane
10G_PHY_MDIO_SDA0	CEI_MDIO					
10G_PHY_MDC_SCL	CEI_MDC					
10G_SFP_SDA0	CEI_SDA					
10G_SFP_SCL0	CEI_SCL					
10G_PHY_RST_01	CEI_ResetN					
10G_INT0	CEI_IntN					
10G_PHY_CAP_01	CEI_PresentN					

8.3 Pinout Comparison

The tables in this section compare the pinout differences between COM Express Specification 3.0 and COM Express Specification 3.1. The signals for COM Express Specification 3.1 are highlighted in bold.

Table 39 Comparison Between COM Rev 3.0 and COM Rev 3.1

COM Rev 3.0				COM Rev 3.1			
Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A4	GBE0_LINK100#	B4	LPC_AD0	A4	**GBE0_LINK_MID#** [3]	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1	A5	**GBE0_LINK_MAX#** [3]	B5	LPC_AD1
A28	(S)ATA_ACT#	B28	RSVD [1]	A28	(S)ATA_ACT#	B28	**GND** [3]
A29	RSVD [1]	B29	RSVD [1]	A29	RSVD [1]	B29	**PCIE1_CK_REF+** [3]
A30	RSVD [1]	B30	RSVD [1]	A30	RSVD [1]	B30	**PCIE1_CK_REF-** [3]
A32	RSVD [1]	B32	SPKR	A32	**IPMB_CLK** [3]	B32	SPKR
A33	RSVD [1]	B33	I2C_CK	A33	**IPMB_DAT** [3]	B33	I2C_CK
A48	RSVD [1]	B48	USB0_HOST_PRSNT [1]	A48	**RSMRST_OUT#** [1, 3]	B48	USB0_HOST_PRSNT [1]
A87	RSVD [1]	B87	VCC_5V_SBY	A87	**GND** [1, 3]	B87	VCC_5V_SBY

COM Rev 3.0				COM Rev 3.1			
Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C15	10G_PHY_MDC_SCL3	D15	10G_PHY_MDIO_SDA3 [1]	C15	**RSVD10G** [3]	D15	**RSVD10G** [3]
C16	10G_PHY_MDC_SCL2	D16	10G_PHY_MDIO_SDA2 [1]	C16	**RSVD10G** [3]	D16	**RSVD10G** [3]
C24	10G_INT2	D24	10G_INT3	C24	**RSVD10G** [2, 3]	D24	**RSVD10G** [2, 3]
C32	10G_SFP_SDA3	D32	10G_SFP_SCL3 [1]	C32	**RSVD10G** [3]	D32	**RSVD10G** [3]
C33	10G_SFP_SDA2	D33	10G_SFP_SCL2 [1]	C33	**RSVD10G** [3]	D33	**RSVD10G** [3]
C34	10G_PHY_RST_23	D34	10G_PHY_CAP_23 [1]	C34	**RSVD10G** [3]	D34	**RSVD10G** [3]
C35	10G_PHY_RST_01	D35	10G_PHY_CAP_01	C35	**CEI_RST#** [3]	D35	**CEI_PRSNT#** [3]
C36	10G_LED_SDA	D36	RSVD [1]	C36	**RSVD10G** [3]	D36	RSVD [1]
C37	10G_LED_SCL	D37	RSVD [1]	C37	**RSVD10G** [3]	D37	RSVD [1]
C38	10G_SFP_SDA1	D38	10G_SFP_SCL1	C38	**RSVD10G** [3]	D38	**RSVD10G** [3]
C39	10G_SFP_SDA0	D39	10G_SFP_SCL0	C39	**CEI_SDA** [3]	D39	**CEI_SCL** [3]
C45	10G_PHY_MDC_SCL1	D45	10G_PHY_MDIO_SDA1	C45	**RSVD10G** [3]	D45	**RSVD10G** [3]
C46	10G_PHY_MDC_SCL0	D46	10G_PHY_MDIO_SDA0	C46	**CEI_MDC** [3]	D46	**CEI_MDIO** [3]
C47	10G_INT0	D47	10G_INT1	C47	**CEI_INT#** [3]	D47	**ETH_PHY_INT#** [2, 3]
C54	TYPE0#	D54	RSVD [1]	C54	TYPE0#	D54	**GND** [3]
C63	RSVD	D63	RSVD	C63	**GND** [3]	D63	**GND** [3]
C64	RSVD	D64	RSVD	C64	**GND** [3]	D64	**GND** [3]
C77	RSVD	D77	RSVD	C77	**GND** [3]	D77	**GND** [3]
C83	RSVD	D83	RSVD	C83	**GND** [3]	D83	**GND** [3]
C97	RSVD	D97	RSVD	C97	**GND** [3]	D97	**GND** [3]

Note

1. *Not connected*
2. *Not supported by default*
3. *Supported on conga-B7XI COM 3.1 variant*

Table 40 NBASE-T (Gigabit) Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10 Mbps modes. Some pairs are unused in some modes according to the following:				I/O Analog		
			1000BASE-T 2.5GBASE-T 5.0GBASE-T 10GBASE-T	100BASE-TX	10BASE-T			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				OD 3.3VSB	PU 10K	
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.				OD 3.3VSB	PU 10K	
GBE0_LINK_MID#	A4	Gigabit Ethernet Controller MID Speed Link indicator, active low (GBE0_LINK100# in COM Express Rev. 3.0). If active, the link is established but at a speed lower than the maximum speed supported by the Ethernet controller. Based on capabilities of the Ethernet controller used, this signal might not be active for all possible lower link speeds.				OD 3.3VSB	PU 10K	**With a customized COM 3.1 variant or the variant with PN: 050221**
GBE0_LINK_MAX#	A5	Gigabit Ethernet Controller MAX Speed Link Indicator, active low (GBE0_LINK1000# in COM Express Rev 3.0). If active, the link is established at the maximum link speed supported by the controller				OD 3.3VSB	PU 10K	**With a customized COM 3.1 variant or the variant with PN: 050221**
GBE0_CTREF	A14	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0 V and as high as 3.3 V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.				REF		Not connected
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1 pps signal.				I/O		

Table 41 PCI Express Signal Descriptions (General Purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express Transmit Output Differential Pairs 0	O PCIE		Supports PCI Express Base Specification, revision 3.0 on conga-B7XI COM 3.0 variants.
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express Receive Input Differential Pairs 0	I PCIE		
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express Transmit Output Differential Pairs 1	O PCIE		
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express Receive Input Differential Pairs 1	I PCIE		
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express Transmit Output Differential Pairs 2	O PCIE		
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express Receive Input Differential Pairs 2	I PCIE		
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express Transmit Output Differential Pairs 3	O PCIE		
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express Receive Input Differential Pairs 3	I PCIE		
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express Transmit Output Differential Pairs 4	O PCIE		
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express Receive Input Differential Pairs 4	I PCIE		
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express Transmit Output Differential Pairs 5	O PCIE		
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express Receive Input Differential Pairs 5	I PCIE		
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express Transmit Output Differential Pairs 6	O PCIE		
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express Receive Input Differential Pairs 6	I PCIE		
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express Transmit Output Differential Pairs 7	O PCIE		
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express Receive Input Differential Pairs 7	I PCIE		
PCIE_TX8+ PCIE_TX8-	A71 A72	PCI Express Transmit Output Differential Pairs 8	O PCIE		
PCIE_RX8+ PCIE_RX8-	B71 B72	PCI Express Receive Input Differential Pairs 8	I PCIE		
PCIE_TX9+ PCIE_TX9-	A74 A75	PCI Express Transmit Output Differential Pairs 9	O PCIE		
PCIE_RX9+ PCIE_RX9-	B74 B75	PCI Express Receive Input Differential Pairs 9	I PCIE		

PCIE_TX10+ PCIE_TX10-	A77 A78	PCI Express Transmit Output Differential Pairs 10	O PCIE		Supports PCI Express Base Specification, revision 3.0 on conga-B7XI COM 3.0 variants.
PCIE_RX10+ PCIE_RX10-	B77 B78	PCI Express Receive Input Differential Pairs 10	I PCIE		
PCIE_TX11+ PCIE_TX11-	A81 A82	PCI Express Transmit Output Differential Pairs 11	O PCIE		
PCIE_RX11+ PCIE_RX11-	B81 B82	PCI Express Receive Input Differential Pairs 11	I PCIE		
PCIE_TX12+ PCIE_TX12-	A39 A40	PCI Express Transmit Output Differential Pairs 12	O PCIE		
PCIE_RX12+ PCIE_RX12-	B39 B40	PCI Express Receive Input Differential Pairs 12	I PCIE		
PCIE_TX13+ PCIE_TX13-	A36 A37	PCI Express Transmit Output Differential Pairs 13	O PCIE		
PCIE_RX13+ PCIE_RX13-	B36 B37	PCI Express Receive Input Differential Pairs 13	I PCIE		
PCIE_TX14+ PCIE_TX14-	A25 A26	PCI Express Transmit Output Differential Pairs 14	O PCIE		
PCIE_RX14+ PCIE_RX14-	B25 B26	PCI Express Receive Input Differential Pairs 14	I PCIE		
PCIE_TX15+ PCIE_TX15-	A22 A23	PCI Express Transmit Output Differential Pairs 15	O PCIE		
PCIE_RX15+ PCIE_RX15-	B22 B23	PCI Express Receive Input Differential Pairs 15	I PCIE		
PCIE_TX16+ PCIE_TX16-	D52 D53	PCI Express Transmit Output Differential Pairs 16	O PCIE		Supports PCI Express Base Specification, revision 3.0 on conga-B7XI COM 3.0 variants. **Supports PCIe Gen 4 on a customized COM 3.1 variant or the variant with PN: 050221.**
PCIE_RX16+ PCIE_RX16-	C52 C53	PCI Express Receive Input Differential Pairs 16	I PCIE		
PCIE_TX17+ PCIE_TX17-	D55 D56	PCI Express Transmit Output Differential Pairs 17	O PCIE		
PCIE_RX17+ PCIE_RX17-	C55 C56	PCI Express Receive Input Differential Pairs 17	I PCIE		
PCIE_TX18+ PCIE_TX18-	D58 D59	PCI Express Transmit Output Differential Pairs 18	O PCIE		
PCIE_RX18+ PCIE_RX18-	C58 C59	PCI Express Receive Input Differential Pairs 18	I PCIE		
PCIE_TX19+ PCIE_TX19-	D61 D62	PCI Express Transmit Output Differential Pairs 19	O PCIE		
PCIE_RX19+ PCIE_RX19-	C61 C62	PCI Express Receive Input Differential Pairs 19	I PCIE		
PCIE_TX20+ PCIE_TX20-	D65 D66	PCI Express Transmit Output Differential Pairs 20	O PCIE		
PCIE_RX20+ PCIE_RX20-	C65 C66	PCI Express Receive Input Differential Pairs 20	I PCIE		

PCIE_TX21+ PCIE_TX21-	D68 D69	PCI Express Transmit Output Differential Pairs 21	O PCIE		Supports PCI Express Base Specification, revision 3.0 on conga-B7XI COM 3.0 variants. **Supports PCIe Gen 4 on a customized COM 3.1 variant or the variant with PN: 050221.**
PCIE_RX21+ PCIE_RX21-	C68 C69	PCI Express Receive Input Differential Pairs 21	I PCIE		
PCIE_TX22+ PCIE_TX22-	D71 D72	PCI Express Transmit Output Differential Pairs 22	O PCIE		
PCIE_RX22+ PCIE_RX22-	C71 C72	PCI Express Receive Input Differential Pairs 22	I PCIE		
PCIE_TX23+ PCIE_TX23-	D74 D75	PCI Express Transmit Output Differential Pairs 23	O PCIE		
PCIE_RX23+ PCIE_RX23-	C74 C75	PCI Express Receive Input Differential Pairs 23	I PCIE		
PCIE_TX24+ PCIE_TX24-	D78 D79	PCI Express Transmit Output Differential Pairs 24	O PCIE		
PCIE_RX24+ PCIE_RX24-	C78 C79	PCI Express Receive Input Differential Pairs 24	I PCIE		
PCIE_TX25+ PCIE_TX25-	D81 D82	PCI Express Transmit Output Differential Pairs 25	O PCIE		
PCIE_RX25+ PCIE_RX25-	C81 C82	PCI Express Receive Input Differential Pairs 25	I PCIE		
PCIE_TX26+ PCIE_TX26-	D85 D86	PCI Express Transmit Output Differential Pairs 26	O PCIE		
PCIE_RX26+ PCIE_RX26-	C85 C86	PCI Express Receive Input Differential Pairs 26	I PCIE		
PCIE_TX27+ PCIE_TX27-	D88 D89	PCI Express Transmit Output Differential Pairs 27	O PCIE		
PCIE_RX27+ PCIE_RX27-	C88 C89	PCI Express Receive Input Differential Pairs 27	I PCIE		
PCIE_TX28+ PCIE_TX28-	D91 D92	PCI Express Transmit Output Differential Pairs 28	O PCIE		
PCIE_RX28+ PCIE_RX28-	C91 C92	PCI Express Receive Input Differential Pairs 28	I PCIE		
PCIE_TX29+ PCIE_TX29-	D94 D95	PCI Express Transmit Output Differential Pairs 29	O PCIE		
PCIE_RX29+ PCIE_RX29-	C94 C95	PCI Express Receive Input Differential Pairs 29	I PCIE		
PCIE_TX30+ PCIE_TX30-	D98 D99	PCI Express Transmit Output Differential Pairs 30	O PCIE		
PCIE_RX30+ PCIE_RX30-	C98 C99	PCI Express Receive Input Differential Pairs 30	I PCIE		
PCIE_TX31+ PCIE_TX31-	D101 D102	PCI Express Transmit Output Differential Pairs 31	O PCIE		
PCIE_RX31+ PCIE_RX31-	C101 C102	PCI Express Receive Input Differential Pairs 31	I PCIE		

PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if the design involves more than one PCI Express device.
PCIE1_CK_REF+ **PCIE1_CK_REF-**	B29 B30	Second PCIe Reference Clock output for higher speed PCIe Express implementation on Lanes 16–3.	O PCIE		**Supports PCIe Gen 4 compliant clock buffer chip with a customized COM 3.1 variant or the variant with PN: 050221**

Table 42 NC-SI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
NCSI_CLK_IN	B91	NC-SI Clock reference for receive, transmit, and control interface.	I 3.3 VSB	PD 10K	
NCSI_RXD0 NCSI_RXD1	B93 B92	NC-SI Receive Data (from NC to BMC)	O 3.3 VSB		
NCSI_TXD0 NCSI_TXD1	B96 B95	NC-SI Transmit Data (from BMC to NC).	I 3.3VSB	PD 10K	
NCSI_CRS_DV	B94	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.	O 3.3VSB		
NCSI_TX_EN	A84	NC-SI Transmit enable.	I 3.3VSB	PD 10K	
NCSI_RX_ER	B89	NC-SI Receive error.	O 3.3VSB		
NCSI_ARB_IN	B98	NC-SI hardware arbitration input.	I 3.3VSB	PD 10K	
NCSI_ARB_OUT	B99	NC-SI hardware arbitration output.	O 3.3VSB	PU 10K 3.3VSB	
IPMB_CLK	A32	Clock I/O line for the multi-master IPMB port. If the IPMB interface is used, an additional lower value pull-up is located on the carrier.	I/O OD 3.3VSB	PU 47K	**With a customized COM 3.1 variant or the variant with PN: 050221**
IPMB_DAT	A33	Data I/O line for the multi-master IPMB port. If the IPMB interface is used, an additional lower value pull-up is located on the carrier.	I/O OD 3.3VSB	PU 47K	**With a customized COM 3.1 variant or the variant with PN: 050221**

Table 43 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB Port 0, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+ USB1-	B46 B45	USB Port 1, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+ USB2-	A43 A42	USB Port 2, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1

Signal	Pin #	Description	I/O	PU/PD	Comment
USB3+ USB3-	B43 B42	USB Port 3, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10K 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10K 3.3VSB	Do not pull this line high on the carrier board.
USB0_HOST_ PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present	I 3.3VSB		Not connected
USB_SSRX0+ USB_SSRX0-	C4 C3	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX0+ USB_SSTX0-	D4 D3	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSRX1+ USB_SSRX1-	C7 C6	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX1+ USB_SSTX1-	D7 D6	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSRX2+ USB_SSRX2-	C10 C9	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX2+ USB_SSTX2-	D10 D9	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSRX3+ USB_SSRX3-	C13 C12	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX3+ USB_SSTX3-	D13 D12	Additional transmit signal differential pairs for the Superspeed USB data path	O		
RSMRST_OUT#	A48	USB devices that are to be powered in the S5 / S4 / S3 suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the high stae	O 3.3VSB		**Not connected**

Table 44 10 Gigabit Ethernet Signal Descriptions (COM Rev. 3.1)

Signal	Pin #	Description	I/O	PU/PD	Comment
10G_KR_TX0+ 10G_KR_TX0-	D49 D50	10GBASE-KR ports, transmit output differential pairs 0	O KR		
10G_KR_RX0+ 10G_KR_RX0-	C49 C50	10GBASE-KR ports, receive input differential pairs 0	I KR		
10G_KR_TX1+ 10G_KR_TX1-	D42 D43	10GBASE-KR ports, transmit output differential pairs 1	O KR		

10G_KR_RX1+ 10G_KR_RX1-	C42 C43	10GBASE-KR ports, receive input differential pairs 1	I KR		
10G_KR_TX2+ 10G_KR_TX2-	D29 D30	10GBASE-KR ports, transmit output differential pairs 2	O KR		
10G_KR_RX2+ 10G_KR_RX2-	C29 C30	10GBASE-KR ports, receive input differential pairs 2	I KR		
10G_KR_TX3+ 10G_KR_TX3-	D26 D27	10GBASE-KR ports, transmit output differential pairs 3	O KR		
10G_KR_RX3+ 10G_KR_RX3-	C26 C27	10GBASE-KR ports, receive input differential pairs 3	I KR		
CEI_MDIO [1]	D46	MDIO data for PHY setup.	I/O 3.3VSB	PU 1K 3.3VSB	10G_PHY_MDIO_SDA0 for COM Rev. 3.0
CEI_MDC [1]	C46	MDIO clock for PHY setup	O 3.3VSB	PU 1K 3.3VSB	10G_PHY_MDC_SCL0 for COM Rev. 3.0
CEI_SDA [1]	C39	I2C data for SFP setup, serialized status, LEDs and miscellaneous serialized signals	I/O OD 3.3VSB	PU 10K 3.3VSB	10G_SFP_SDA0 for COM Rev. 3.0
CEI_SCL [1]	D39	I2C clock for CEI I2C port	I/O OD 3.3VSB	PU 10K 3.3VSB	10G_SFP_SCL0 for COM Rev. 3.0
CEI_INT# [1]	C47	Active low interrupt input to Module from carrier based I2C I/O expander	I 3.3VSB	PU 10K 3.3VSB	10G_INT0 for COM Rev. 3.0
ETH_PHY_INT# [2]	D47	Second active low interrupt input to module from carrier based I2C I/O expander	I 3.3VSB	PU 1K 3.3VSB	10G_INT1 for COM Rev. 3.0
CEI_RST# [1]	C35	Active low reset output from Module to Carrier based I/O expander	O 3.3VSB	PD 10K	10G_PHY_RST_01 for COM Rev. 3.0
CEI_PRSNT# [1]	D35	Input signal from Carrier indicating presence of CEI compliant hardware on the carrier	I 3.3VSB	PU 10K 3.3VSB	10G_PHY_CAP_01 for COM Rev. 3.0
10G_SDP[0:3] [3]	C40 D40 C17 D17	Software-Definable Pins, can also be used for IEEE1588 support such as a 1pps signal	I/O 3.3V		10G_SDP[0:3]

Note

1. *For CEI support, you need a customized conga-B7XI COM 3.1 variant (BOM option) or the variant with PN: 050221.*
2. *Not supported by default*
3. *The conga-B7XI does not support 10G_SDP[0:3].*

Table 45 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109 C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A38, A41, A51, A57, A60, A66, A70, A73, A76, A79, A80, A83, A90, A100, A110, B1, B11, B21, B31, B38, B41, B51, B60, B70, B73, B76, B79, B80, B83, B90, B100, B110, C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		
	A87 [1] B28 C63, C64, C77, C83, C97				**With a customized COM 3.1 variant or the variant with PN: 050221**

Note

1. *Not connected*

9 System Resources

9.1 I/O Address Assignment

The fixed address ranges below are either positively decoded in the system agent or subtractively routed to the Primary to Sideband Bridge (P2SB). The P2SB claims many of the fixed I/O accesses and forwards the transactions to their functional target via sideband fabric.

Table 46 I/O Address Assignment

Device	IO Address
Interrupt Controller	20h-3Dh, A0h-BDh, 4D0h-4D1h
8254 Timers	40h-43h, 50h-53h
NMI Controller (CPU I/F)	61h, 63h, 65h, 67h
Reset Generator (CPU I/F)	92h
RTC	70h-77h
Reset Generator (CPU)	CF9h
PMC	B2h-B3h
LPC	2Eh-2Fh, 4Eh-4Fh, 62h, 66h, 80h, 84h-86h, 88h, 8Ch-8Eh, 90h, 94h-96h, 98h, 9Ch-9Eh, 200h-207F, 208h-20Fh, 220h-227h, 228h-22Fh, 238h-23Fh, 278h-27Fh, 2E8h-2EFh, 2F8h-2FFh, 338h-33Fh, 370h-375h, 377h, 378h-37Fh, 3BCh-3BEh, 3E8h-3EFh, 3F0h-3F5h, 3F7h, 3F8h-3FFh, 678h-67Fh, 778h-77Fh, 7BCh-7BEh

Note

Address ranges that are not listed, marked as reserved nor assigned to one of the variable ranges are not positively decoded by the PCH, and will be internally terminated by the PCH.

9.2 PCI Configuration Space Map

Table 47 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Device ID	Description and Device ID
00h	00h	00h	0x09A2	Mesh2IIO MMAP/VT-D
00h	00h	01h	0x09A4	Mesh2IIO PMON
00h	00h	02h	0x09A3	Mesh2IIO RAS
00h	00h	03h	0x09A5	Mesh2IIO DFX
00h	00h	04h	0x0998	Host Bridge
00h	01h	00h	0x0B00	Intel QuickData Technology CH0
00h	01h	01h	0x0B00	Intel QuickData Technology CH1
00h	01h	02h	0x0B00	Intel QuickData Technology CH2
00h	01h	03h	0x0B00	Intel QuickData Technology CH3
00h	01h	04h	0x0B00	Intel QuickData Technology CH4
00h	01h	05h	0x0B00	Intel QuickData Technology CH5
00h	01h	06h	0x0B00	Intel QuickData Technology CH6
00h	01h	07h	0x0B00	Intel QuickData Technology CH7
00h	02h	00h	0x09A6	PECI Out-Of-Band Management Services Module (OOB-MSM)
00h	02h	01h	0x09A7	PECI OOB-MSM - Performance Monitoring Unit (PMU)
00h	02h	04h	0x3456	CPU Intel Trace Hub
00h	0Eh	00h	0x18F2	SATA Controller
00h	0Fh	00h	0x18A3	Host SMBus
00h	10h	00h	0x18A8	PCH PCIe Cluster 1 Root Port 4
00h	14h	00h	0x18AD	PCH PCIe Cluster 2 Root Port 8
00h	18h	00h	0x18D3	Intel ME - HECI 1
00h	18h	01h	0x18D4	Intel ME - HECI 2
00h	18h	04h	0x18D6	Intel ME - HECI 3
00h	1Ah	00h	0x18D8	HSUART 0
00h	1Ah	01h	0x18D8	HSUART 1
00h	1Ah	02h	0x18D8	HSUART 2
00h	1Ah	03h	0x18D9	Reserved
00h	1Dh	00h	0x0998	Satellite IEH
00h	1Eh	00h	0x18D0	USB Combo Controller

00h	1Fh	00h	0x18DC	LPC/eSPI Controller
00h	1Fh	04h	0x18DF	Legacy SMBus
00h	1Fh	05h	0x18E0	SPI Controller
00h	1Fh	07h	0x18E1	PCH Intel Trace Hub

Note

1. *The PCI Express ports are visible only if a device is attached to the PCI Express slot on the carrier board and the PCI Express ports are set to "Enabled" or "Auto" in the BIOS setup menu.*

2. *The internal PCI devices that are not connected to the conga-B7XI are not listed.*

9.3 congatec System Sensors

The conga-B7XI offers the following sensors and monitor:

- Two temperature sensors (CPU temperature and board temperature sensor located on the board controller)
- Two voltage sensors (standard 5 V and 5 V standby voltage sensors)
- One current sensor
- One fan monitor

The sensors and monitor are accessible through CGOS interface or via the health monitor submenu in the BIOS setup menu.

10 Additional BIOS Information

The BIOS setup description of the conga-B7XI can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-B7XI is identified as DICLR1xx, where:

- R is the identifier for a BIOS binary file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The conga-B7XI BIOS binary size is 64 MB.

10.2 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-B7XI features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions— UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

Note

1. *Deprecated.*

10.2.1 Updating from External Flash

For instructions on how to update the BIOS from external flash, refer to the AN7_External_BIOS_Update.pdf application note on the congatec website at http://www.congatec.com.

10.3 Supported Flash Devices

The conga-B7XI supports the following flash devices:

- Winbond W25Q512JVEIQ (64 MB)
- Micron MTQL512ABB1EW9-0SIT (64 MB)

The flash devices listed above can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.