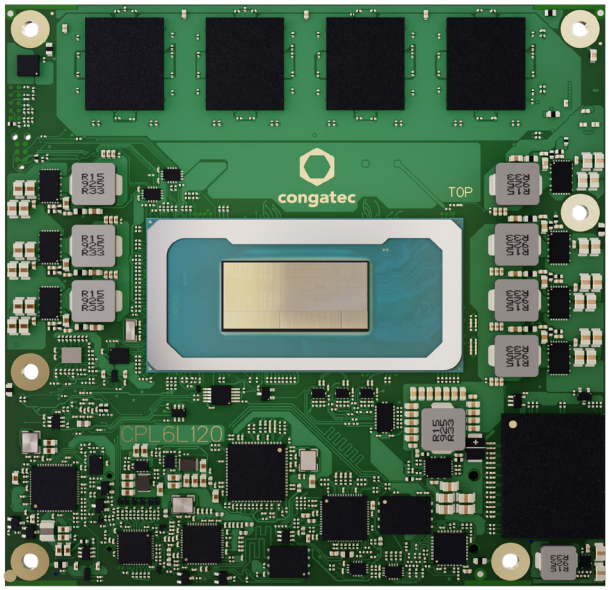

conga-TC1000r

COM Express® 3.1 Type 6 Compact Module with Intel® Core™ Ultra Series 3 Processors

User's Guide

Revision 0.01

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Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.01	2026-11-23	RVI	• Preliminary release

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Preface

This user's guide provides information about the components, features, connectors and system resources available on the conga-TC1000r. It is one of three documents that should be referred to when designing a COM Express® application. The other reference documents that should be used include the following:

- COM Express® Module Base Specification
- COM Express® Carrier Design Guide

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Terminology

Term	Description
CSA	Active Cooling Solution
CSP	Passive Cooling Solution
DSC	Display Stream Compression
DTR	Dynamic Temperature Range
eDP	Embedded DisplayPort
EU	Execution Unit
DDI	Digital Display Interface
GB	Gigabyte
GHz	Gigahertz
HDA	High Definition Audio
HBR	High Bit Rate
HSP	Heatspreader
kB	Kilobyte
kHz	Kilohertz
MB	Megabyte
Mbit	Megabit
MHz	Megahertz
N.A	Not available
N.C	Not connected
OEM	Original Equipment Manufacturer
PCIe	PCI Express
PCH	Platform Controller Hub
PEG	PCI Express Graphics
SATA	Serial ATA
TBD	To be determined
TCC	Time Coordinated Computing
TDP	Thermal Design Power
TSN	Time Sensitive Networking
UHBR	Ultra High Bit Rate

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Contents

1 Introduction 11
1.1 COM Express® Concept 11
1.2 Options Information 12
2 Specifications 15
2.1 Feature List 15
2.2 Supported Operating Systems 16
2.3 Mechanical Dimensions 16
2.4 Supply Voltage Standard Power 17
2.4.1 Electrical Characteristics 17
2.4.2 Rise Time 17
2.5 Power Consumption 17
2.6 Supply Voltage Battery Power 19
2.7 Environmental Specifications 20
2.8 Storage Specifications 20
2.8.1 Module 20
2.8.2 Cooling Solutions 21
3 Block Diagram 22
4 Cooling Solutions 23
4.1 HSP Dimensions (H484 Versions) 24
4.2 HSP Dimensions (H404 Versions) 25
5 Connector Rows 26
5.1 PCI Express 26
5.2 PCI Express Graphics (PEG) 27
5.3 Display Interfaces 28
5.3.1 DP++ 28
5.3.2 LVDS/eDP 28
5.4 SATA 29
5.5 Optional SSD 29
5.6 USB 29
5.6.1 USB 2.0 30
5.6.2 USB 3.2 30
5.6.3 USB4 31
5.7 NBASE-T Ethernet 32
5.8 High Definition Audio 32
5.9 General Purpose SPI 32
5.10 SPI 33
5.10.1 BIOS Flash Selection 33
5.11 UART/CAN 33
5.12 LPC Bus 33
5.13 I²C Bus 34
5.14 GPIOs 34
5.15 SMBus 35
5.16 Power Control 35
5.16.1 Power Management 37
5.16.2 Inrush Current 37
6 Additional Features 38
6.1 KSC 2.0 38
6.1.1 Board Information 38
6.1.2 Watchdog 38
6.1.3 Power Loss Control 39
6.1.4 Fan Control 39
6.2 OEM BIOS Customization 39
6.2.1 OEM Default Settings 40
6.2.2 OEM BIOS Code/Data 40
6.2.3 OEM DXE Driver 40
6.3 congatec Battery Management Interface 40
6.4 Suspend to Ram 40
7 conga Tech Notes 41
7.1 Processor Performance Control 41
7.1.1 Intel® SpeedStep® Technology (EIST) 41
7.1.2 Intel® Turbo Boost Technology 42
7.2 Intel® Neural Processing Unit (Intel® NPU) 43
7.3 Adaptive Thermal Monitor and Catastrophic Thermal Protection 43

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7.4 Intel® Virtualization Technology 44
7.5 Thermal Management 44
7.6 ACPI Suspend Modes and Resume Events 44

8 Signal Descriptions and Pinout Tables 46

8.1 Connector Signal Descriptions 47

9 System Resources 70

10 BIOS Setup Description 71

10.1 Navigating the BIOS Setup Menu 71
10.2 BIOS Versions 71
10.3 Updating the BIOS 72
10.4 Supported Flash Devices 72

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List of Tables

Table 1 COM Express® 3.1 Pinout Types 11
Table 2 Commercial Variants 12
Table 3 Industrial Variants 13
Table 4 Feature Summary 15
Table 5 Overview of Type 6 Limitations 17
Table 6 Measurement Description 18
Table 7 Power Consumption Values 18
Table 8 CMOS Battery Power Consumption (Commercial Variants) 19
Table 9 Cooling Solution Variants 23
Table 10 PCIe Link Configuration (with SATA Controller and Ethernet Controller Enabled) 26
Table 11 PCIe Link Configuration (with the Disabled SATA Controller and no Ethernet Controller) - Customized Configurations 27
Table 12 PEG Interface Configuration Options 27
Table 13 NBASE-T Ethernet LED Description 32
Table 14 BIOS Select Options 33
Table 15 Reserved I²C Addresses 34
Table 16 Inrush Current 37
Table 17 Wake Events 45
Table 18 Signal Tables Terminology Descriptions 46
Table 19 Connector A–B Pinout 47
Table 20 Connector C–D Pinout 49
Table 21 PCI Express Signal Descriptions (General Purpose) 51
Table 22 PCI Express Signal Descriptions (x16 Graphics) 52
Table 23 DDI Signal Description 54
Table 24 Embedded DisplayPort Signal Descriptions 56
Table 25 LVDS Signal Descriptions 56
Table 26 VGA Signal Descriptions 57
Table 27 SATA Signal Descriptions 58
Table 28 USB 2.0 and 3.2 Signal Descriptions 58
Table 29 USB4 Support Signal Descriptions 60
Table 30 NBASE-T Ethernet Signal Descriptions 62
Table 31 High Definition Audio Signals Descriptions 63
Table 32 LPC/eSPI Signal Descriptions 63
Table 33 SPI BIOS Flash Interface Signal Descriptions 64
Table 34 Miscellaneous Signal Descriptions 65
Table 35 General Purpose I/O Signal Descriptions 65
Table 36 Power and System Management Signal Descriptions 66
Table 37 Rapid Shutdown Signal Descriptions 66
Table 38 Thermal Protection Signal Descriptions 67
Table 39 SMBus Signal Description 67
Table 40 General Purpose Serial Interface Signal Descriptions 67
Table 41 General Purpose SPI Signal Descriptions 67
Table 42 Module Type Definition Signal Description 68
Table 43 Power and GND Signal Descriptions 69

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1 Introduction

1.1 COM Express® Concept

COM Express® is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express® modules are available in following form factors:

- Mini 84 mm x 55 mm
- Compact 95 mm x 95 mm
- Basic 125 mm x 95 mm
- Extended 155 mm x 110 mm

Table 1 COM Express® 3.1 Pinout Types

Types	Connector Rows	PCIe Lanes	PEG	SATA Ports	LAN ports	USB 2.0/ SuperSpeed USB	USB4	Display Interfaces
Type 6	A–B C–D	Up to 24	1	Up to 4	1 x NBASE-T	Up to 8 / 4 [1]	2	VGA,LVDS/eDP, PEG, 3x DDI
Type 7	A–B C–D	Up to 32	-	Up to 2	1x NBASE-T, 4x 10GBASE-KR	Up to 4 / 4 [1]	-	
Type 10	A–B	Up to 4	-	Up to 2	1x NBASE-T	Up to 8 / 2 [1]	-	LVDS/eDP, 1x DDI

1. *The SuperSpeed USB ports (USB 3.0) are not in addition to the USB 2.0 ports. Up to 4 of the USB 2.0 ports can support SuperSpeed USB.*

The conga-TC1000r modules use the Type 6 pinout definition and comply with COM Express® 3.1 specification. They are equipped with two high performance connectors that ensure stable data throughput.

The COM integrates all the core components and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

Most importantly, COM Express® modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

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1.2 Options Information

The conga-TC1000r is currently available in seven variants. The table below shows the different configurations available.

Table 2 Commercial Variants

Part-No.			052100	052102	052104
Processor			Intel® Core™ Ultra X9 388H 16 Core™	Intel® Core™ Ultra 5 336H 12 Core™	Intel® Core™ Ultra X7 358H 16 Core™
Total Core	P-Cores		4 Cores	4 Cores	4 Cores
	E-Cores	Normal	8 Cores	4 Cores	8 Cores
		Low Power	4 Cores	4 Cores	4 Cores
No of Threads			16	12	16
Core Base Frequency	P-Cores		2.1 GHz	1.9 GHz	1.9 GHz
	E-Cores	Normal	1.6 GHz	1.5 GHz	1.5 GHz
		Low Power	1.6 GHz	1.5 GHz	1.5 GHz
Intel® Smart Cache			18 MB	18 MB	18 MB
Assured Power (cTDP)	Processor Base Power		25 W	25 W	25 W
	Min. Assured Power		15 W	15 W	15 W
	Max. Assured Power		80 W	65 W	80 W
Maximum Turbo Freq. [1]	P-Cores		5.1 GHz	4.6 GHz	4.8 GHz
	E-Cores	Normal	3.8 GHz	3.4 GHz	3.5 GHz
		Low Power	3.7 GHz	3.2 GHz	3.3 GHz
Processor Graphics			Intel® Arc™ B390 GPU (12 Xᵉ Cores)	Intel® Graphics (4 Xᵉ Cores)	Intel® Arc™ B390 GPU (12 Xᵉ Cores)
GFX Max. Dynamic Freq.			2.5 GHz	2.3 GHz	2.5 GHz
DDR5 Memory[2]			Up to 8533 MT/s Dual channel Up to16 GB	Up to 8533 MT/s Dual channel Up to 16 GB	Up to 9600 MT/s Dual channel Up to 32 GB
PCIe Lanes	Max.		12	20	12
	PEG (Default) [3]		Up to 4 lanes	Up to 12 lanes	Up to 4 lanes
	NVMe Gen 4 (Assembly Option) [3]		1 x4 NVMe (Assembly option)	1 x4 NVMe (Assembly option)	1 x4 NVMe (Assembly option)
	PCIe Gen. 4		Up to 8 lanes	Up to 8 lanes	Up to 8 lanes
Ethernet Controller			Intel® I226-LM	Intel® I226-LM	Intel® I226-LM
CPU Use Condition [4]			Embedded	Embedded	Embedded
CPU Tjunction Max.			100°C	100°C	100°C
Compatible Carrier Board			conga-Eval Carrier2 T6 evaluation carrier board for COM Express® Type 6 modules		

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Table 3 Industrial Variants

Part-No.			052110 [5]	052111 [5]	052112 [5]	052113 [5]
Processor			Intel® Core™ Ultra 7 366HRE, 16 Cores™	Intel® Core™ Ultra 7 365RE, 16 Cores™	Intel® Core ™ Ultra 5 336HRE, 12 Cores™	Intel® Core ™ Ultra 5 335RE, 12 Cores™
Total Core	P-Cores		4 Cores	4 Cores	4 Cores	4 Cores
	E-Cores	Normal	8 Cores	0 Cores	4 Cores	0 Cores
		Low Power	4 Cores	4 Cores	4 Cores	4 Cores
No of Threads			16	8	12	8
Core Base Frequency	P-Cores		TBD	TBD	TBD	TBD
	E-Cores	Normal	TBD	TBD	TBD	TBD
		Low Power	TBD	TBD	TBD	TBD
Intel® Smart Cache			18 MB	18 MB	18 MB	18 MB
Assured Power (cTDP)	Processor Base Power		TBD	TBD	TBD	TBD
	Min. Assured Power		TBD	TBD	TBD	TBD
	Max. Assured Power		TBD	TBD	TBD	TBD
Maximum Turbo Freq. [1]	P-Cores		TBD	TBD	TBD	TBD
	E-Cores	Normal	TBD	TBD	TBD	TBD
		Low Power	TBD	TBD	TBD	TBD
Processor Graphics			Intel® Graphics (4 Xᵉ Cores)	Intel® Graphics (4 Xᵉ Cores)	Intel® Graphics (4 Xᵉ Cores)	Intel® Graphics (4 Xᵉ Cores)
GFX Max. Dynamic Freq.			TBD	TBD	TBD	TBD
DDR5 Memory[2]			Up to 8533 MT/s Dual channel Up to 32 GB	Up to 6800 MT/s Dual channel Up to 16 GB	Up to 8533 MT/s Dual channel Up to 16 GB	Up to 8533 MT/s Dual channel Up to 16 GB
PCIe Lanes	Max.		TBD	TBD	TBD	TBD
	PEG (Default) [3]		TBD	TBD	TBD	TBD
	NVMe Gen 4 (Assembly Option) [3]		1 x4 NVMe (Assembly option)	1 x4 NVMe (Assembly option)	1 x4 NVMe (Assembly option)	1 x4 NVMe (Assembly option)
	PCIe Gen. 4		TBD	TBD	TBD	TBD
Ethernet Controller			Intel® I226-IT	Intel® I226-IT	Intel® I226-IT	Intel® I226-IT
CPU Use Condition [4]			Embedded	Embedded	Embedded	Embedded
CPU Tjunction Max.			TBD	TBD	TBD	TBD
Compatible Carrier Board			conga-Eval Carrier2 T6 evaluation carrier board for COM Express® Type 6 modules			

Note

1. *The core frequencies and types vary by workload, power consumption and other factors.*
2. *Memory speed may vary depending on processor SKU and memory configuration.*
3. *The H484/H444 variants provide up to 20 PCIe lanes, while the H404 variant provides up to 12 PCIe lanes (Hxyz: x – number of performance*

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cores, y – number of efficient cores, z – number of low-power efficient cores). The PCIe lanes assigned to the PEG interface (x4, Gen 4) can alternatively be configured for NVMe support as an assembly option.

4. *Intel SoC use conditions. For more information, see Intel documentation.*

5. *Intel has not yet publicly released the information that are marked as TBD.*

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2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	COM Express® Compact ; Type 6 connector pinout	
Processor	Intel® Core™ Ultra Series 3 Panther Lake-H series	
DRAM	Up to 32 GB LPDDR5x soldered down (optional up to 64 GB) with max. 8.533 MT/s ; dual channel ; in-band ECC support on selected SKUs	
Mass Storage	NVMe x 4 SSD (optional) up to 1 TB capacity	
Graphics	Intel® Arc Graphics with up to 12 Xᵉ cores or Intel Graphics with up to 4 Xᵉ cores ; Intel® Xᵉ Matrix Extensions	
AI Acceleration	Integrated NPU accelerator up to 50 TOPS ; Up to 180 TOPS platform total	
Display	Up to 3x DDI (2x shared with USB4) ; LVDS or eDP ; 4x independent displays up to 8k	
Ethernet	2.5 GbE via Intel® i226 Ethernet controller series ; Supporting TSN - Time Sensitive Networking (only on selected product variants) ; Software Definable Pin (SDP) to be used for IEEE 1588	
Audio	Integrated High Definition Audio (HDA) interface ; Soundwire (optional)	
I/O Interfaces	Up to 12x PCIe Gen4 PEG (H484) or up to 4x PCIe Gen4 PEG (H12Xe, H404) Up to 8x PCIe Gen4 Up to 2x USB4 3x USB 3.2 Gen2 8x USB 2.0 2x SATA	2x UART (RX/TX only) GPIOs GP SPI LPC SM Bus I²C
Module Management Controller	Module Management Controller Multi Stage Watchdog Board Information Board Statistics	I²C bus (fast mode) Power Loss Control Hardware Health Monitoring POST Code Redirection
Security	Trusted Platform Module (TPM 2.0) through Infineon SLB9672	
Embedded BIOS Feature	AMI Aptio ® UEFI firmware ; OEM Logo ; OEM CMOS default settings ; LCD Control ; Display Auto Detection ; Backlight Control	
Power Management	ACPI 6.0 ; wide range power supply 8.5V – 20V ; single supply power	
Operating Systems	Microsoft® Windows® 11 IoT Enterprise ; Microsoft® Windows® 11 ; Linux	
Hypervisor	RTS Real-Time Hypervisor	
Temperature	Commercial Temp.: Operating 0 °C to 60 °C Industrial Temp.: Operating -40 °C to 85 °C	Storage : -20 °C to 80 °C Storage : -40 °C to 85 °C
Humidity	Operating : 10% to 85% r. H. non cond.	Storage : 5% to 85% r. H. non cond.
Size	95 x 95 mm	

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2.2 Supported Operating Systems

The conga-TC1000r supports the following operating systems.

- Microsoft® Windows® 11, Version 25H2
- Microsoft® Windows® 11 IoT Enterprise, Version 25H2
- Linux Ubuntu 24.04
- Yocto 5.3

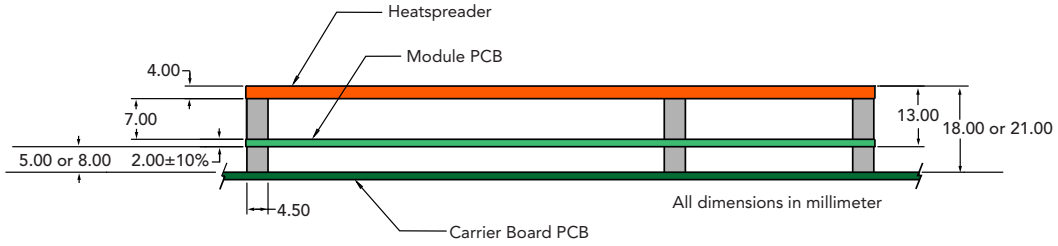
Note

1. *The processor supports only 64-bit operating systems.*
2. *The conga-TC1000r supports only native UEFI Operating Systems. Legacy Operating Systems which require CSM (Compatibility Suppport Module) as part of the UEFI firmware are not supported anymore.*
3. *To support Intel® i226 Ethernet controller in Linux by default, you need kernel 5.15 or higher.*

2.3 Mechanical Dimensions

- Length of 95 mm
- Width of 95 mm

The overall height (module, heatspreader and stack) is shown below:



Caution

The conga-TC1000r has a 4 mm-high memory socket on the bottom side, which exceeds the COM Express® specification limit of 3.8 mm. Ensure sufficient clearance on the carrier board to prevent possible short circuits or mechanical damage.

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Note

The 3D models of congatec products are available at www.congatec.com/login. *These models indicate the overall length, height and width of each product. If you need login access, contact your local sales representative.*

2.4 Supply Voltage Standard Power

The conga-TC1000r supports 8 V – 20 V DC input voltage.

2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Table 5 Overview of Type 6 Limitations

Power Rail	Module Pin Current Capability (Ampere)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.5-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values for conga-TC1000r have not been determined at the time of this document's release and will be provided with the final release of this user guide.

The power consumption values were measured with the following setup:

- Input voltage 12 V
- conga-TC1000r

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- Modified congatec carrier board
- conga-TC1000r cooling solution
- Microsoft Windows 11 (64 bit)

Note

The CPU was stressed to its maximum workload with the Intel® Power and Thermal Analysis Tool.

The power consumption values were recorded during the following system states:

Table 6 Measurement Description

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	COM is powered by VCC_5V_SBY	
S5	COM is powered by VCC_5V_SBY	
S5e	COM is powered by VCC_5V_SBY	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement*

The tables below provide additional information about the conga-TC1000r power consumption. The values were recorded at various operating modes.

Table 7 Power Consumption Values

Processor Base Power (15/28/45 W TDP)

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU				Current (Ampere)					
					Variant	P / E /LP-E Core	Core Freq. P / E / LP-E (GHz)	Turbo Freq. P / E / LP-E (GHz)	S0: Min (12V)	S0: Max (12V)	S0: Peak (12V)	S3 (5V)	S5 (5V)	S5e (5V)
052100	16 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra X9 388H	4 / 8 / 4	2.1 / 1.6 /1.6	5.1 / 3.8 / 3.7	TBD	TBD	TBD	TBD	TBD	TBD
052102	16 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra 5 336H	4 / 4 / 4	1.9 / 1.5 / 1.5	4.6 / 3.4 / 3.2	TBD	TBD	TBD	TBD	TBD	TBD
052104	32 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra X7 358H	4 / 8 / 4	1.9 / 1.5 / 1.5	4.8 / 3.5 / 3.5	TBD	TBD	TBD	TBD	TBD	TBD
052110	32 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra 7 366HRE	4 / 8 / 4	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

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052111	16 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra 7 365RE	4 / 0 / 4	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
052112	16 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra 5 336HRE	4 / 4 / 4	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
052113	16 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra 5 335RE	4 / 0 / 4	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Maximum Assured Power (28/65 W TDP)

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU				Current (Ampere)					
					Variant	P / E /LP-E Core	Core Freq. P / E / LP-E (GHz)	Turbo Freq. P / E / LP-E (GHz)	S0: Min (12V)	S0: Max (12V)	S0: Peak (12V)	S3 (5V)	S5 (5V)	S5e (5V)
052100	16 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra X9 388H	4 / 8 / 4	2.1 / 1.6 /1.6	5.1 / 3.8 / 3.7	TBD	TBD	TBD	TBD	TBD	TBD
052102	16 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra 5 336H	4 / 4 / 4	1.9 / 1.5 / 1.5	4.6 / 3.4 / 3.2	TBD	TBD	TBD	TBD	TBD	TBD
052104	32 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra X7 358H	4 / 8 / 4	1.9 / 1.5 / 1.5	4.8 / 3.5 / 3.5	TBD	TBD	TBD	TBD	TBD	TBD
052110	32 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra 7 366HRE	4 / 8 / 4	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
052111	16 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra 7 365RE	4 / 0 / 4	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
052112	16 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra 5 336HRE	4 / 4 / 4	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
052113	16 GB	C.1	TBD	Windows 11	Intel® Core™ Ultra 5 335RE	4 / 0 / 4	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

2.6 Supply Voltage Battery Power

Table 8 CMOS Battery Power Consumption (Commercial Variants)

RTC @	Voltage	Current
-10°C	3V DC	TBD µA
20°C	3V DC	TBD µA
70°C	3V DC	TBD µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to* https://wiki.congatec.com/wiki/RTC_Battery_Lifetime_(AN09).
4. *We recommend to always have a CMOS battery present when operating the conga-TC1000r.*

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2.7 Environmental Specifications

Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to 80°C
Relative Humidity	Operation: 10% to 85%	Storage: 5% to 85%



Caution

The product is designed to operate in the above operating temperature range. It is the system integrator's responsibility to ensure that all components used on or with the product are operated within their individually specified temperature limits. For detailed information regarding the temperature specifications of individual components used on the product, refer to the respective thermal documentation (e.g., Hotspots CTNs) available in the customer login area at www.congatec.com and/or the customer knowledge base wiki.congatec.com. Appropriate cooling measures must be implemented in the final application to ensure proper heat dissipation.

Humidity specifications are for non-condensing conditions.

2.8 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

2.8.1 Module

For long term storage of the conga-TC1000r (more than six months), keep the conga-TC1000r in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.



Note

We do not recommend storing the conga-TC1000r for more than five years under these conditions.

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2.8.2 Cooling Solutions

The heat pipes of congatec heatspreaders/cooling solutions are filled with water by default. For optimal cooling performance, do not store the heatspreaders/cooling solutions at temperatures below -20°C.



Caution

1. *For temperatures between -10°C and -20°C, preheat the heat pipes before operation. Optionally, the heat pipes can be filled with acetone instead. For more information, contact your local sales representative.*
2. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

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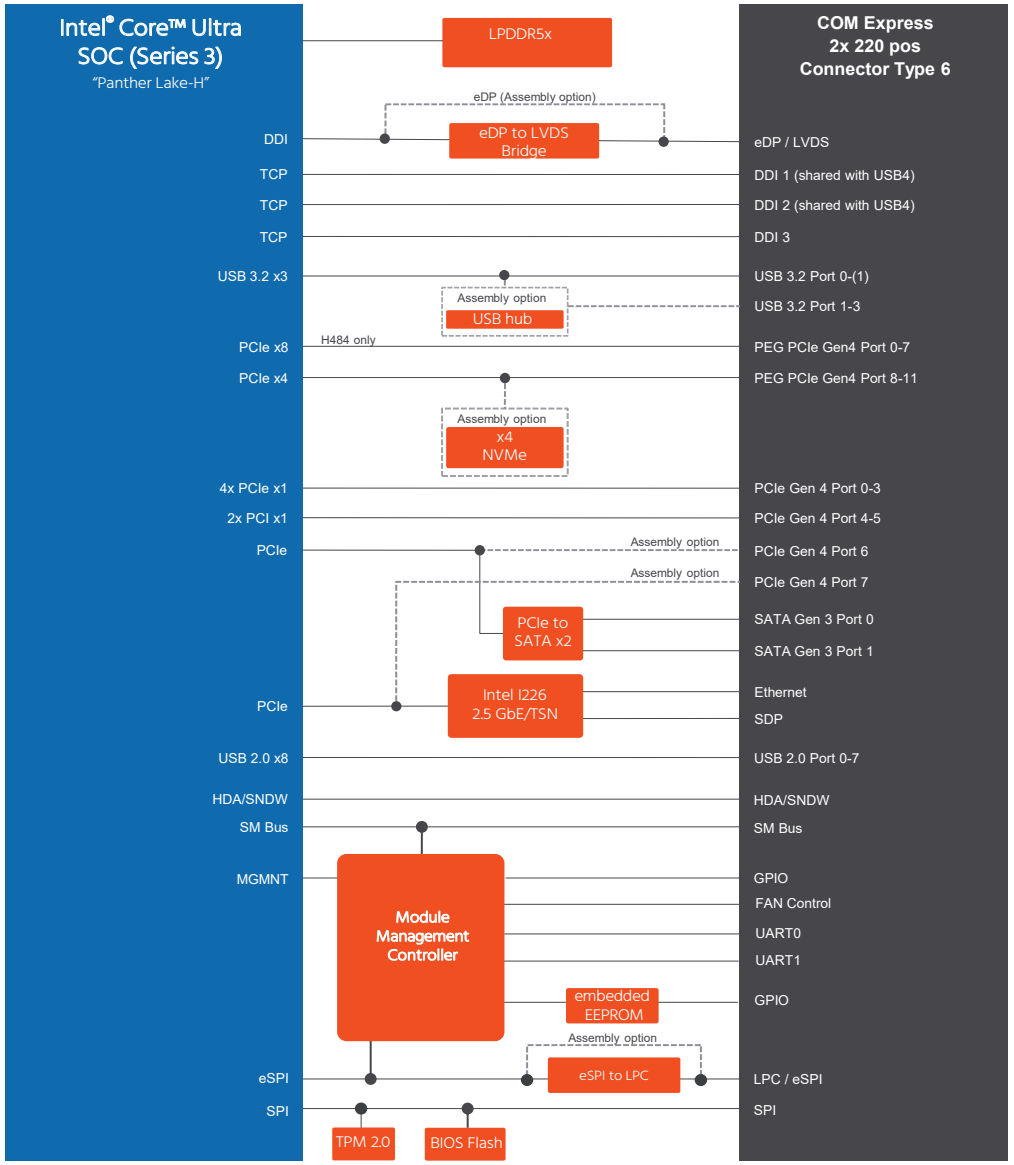
3 Block Diagram



NOTES

Assembly option
Only available on request

4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-TC1000r. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

Cooling Solution	Part-No.	Description
HSP	052154	Standard heatspreader for high performance COM Express module conga-TC1000r with H484. All standoffs are with 2.7mm bore hole.
	052155	Standard heatspreader for high performance COM Express module conga-TC1000r with H484. All standoffs are M2.5mm threaded.
	052156	Standard heatspreader for high performance COM Express module conga-TC1000r with H404. All standoffs are with 2.7mm bore hole.
	052157	Standard heatspreader for high performance COM Express module conga-TC1000r with H404. All standoffs are M2.5mm threaded.

Caution

1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. If your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*

2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

3. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

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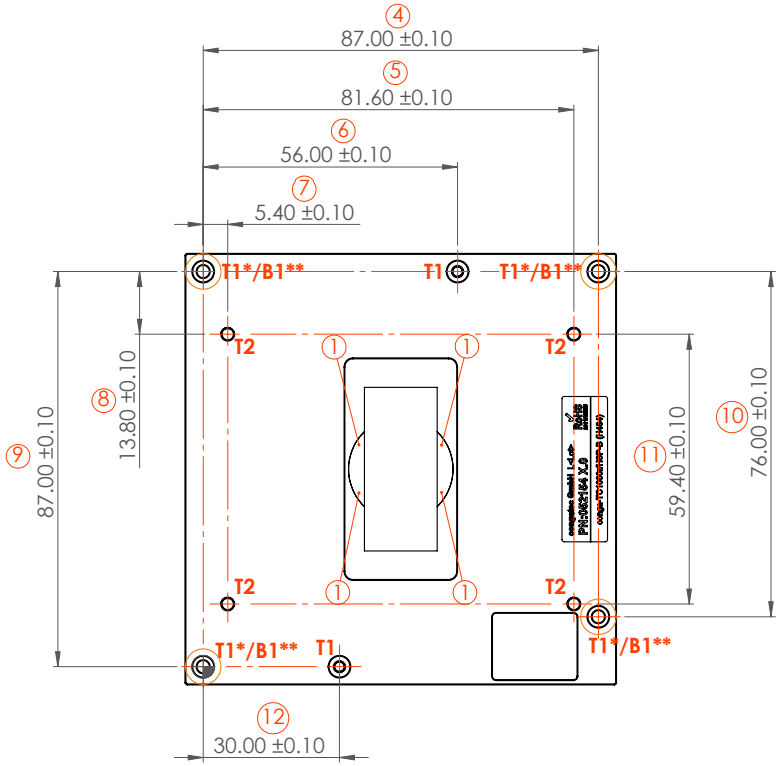
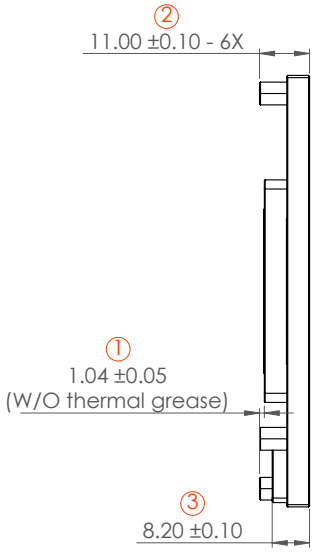
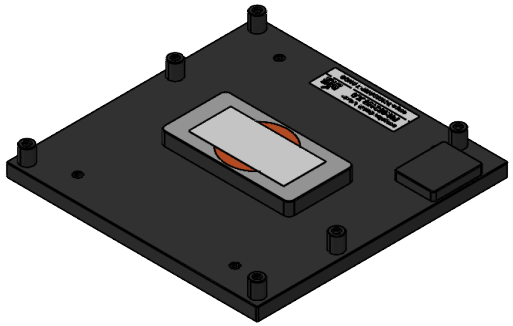
4.1 HSP Dimensions (H484 Versions)



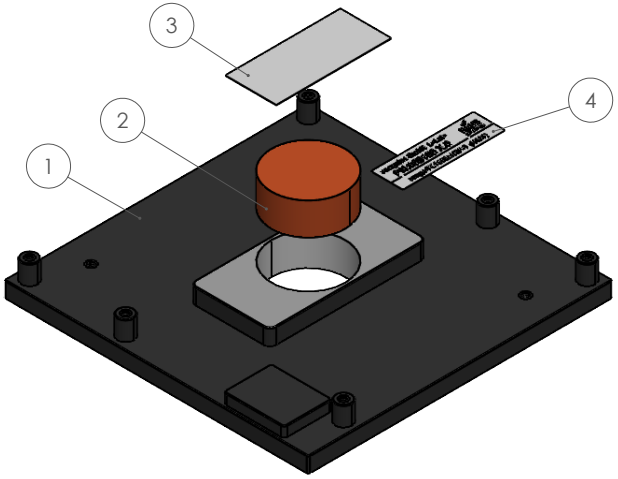




T1: M2.5 x 0.45 mm - 6H, threaded standoff for threaded version
B1: ø2.7 x 0.45 mm - 6H, non-threaded standoff for borehole version

T2: M3.5 x 0.5 mm - 6H, threaded standoff

* For threaded version
** For borehole version



Components:

1. H484 Cooling Profile HSP-T/HSP-B
2. H484 Heat Stack
3. Thermal Paste TC-5026, Size 36x16x0.12mm
4. ML0003, Label HSPCS 32x10mm, Polyester, White *

* The label reads:
PN:052154 / HSP-B for borehole version
PN:052155 / HSP-T for threaded version

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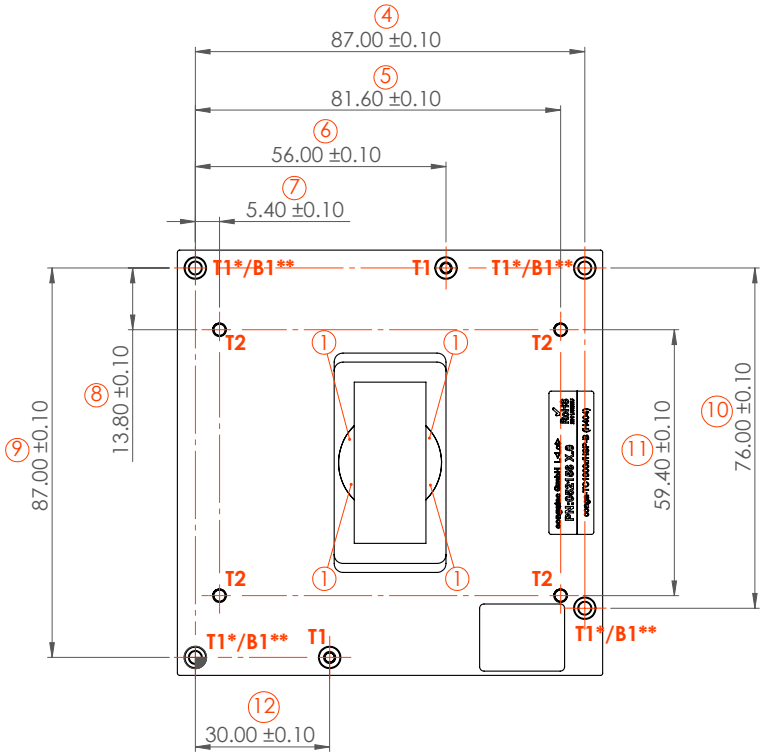
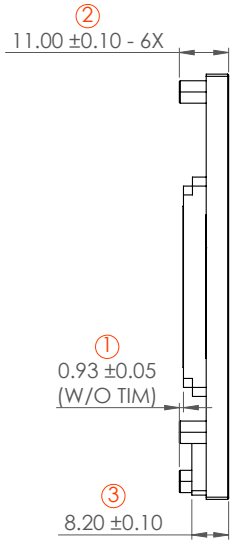
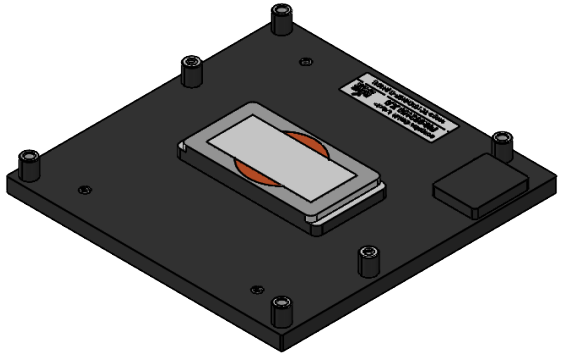
4.2 HSP Dimensions (H404 Versions)



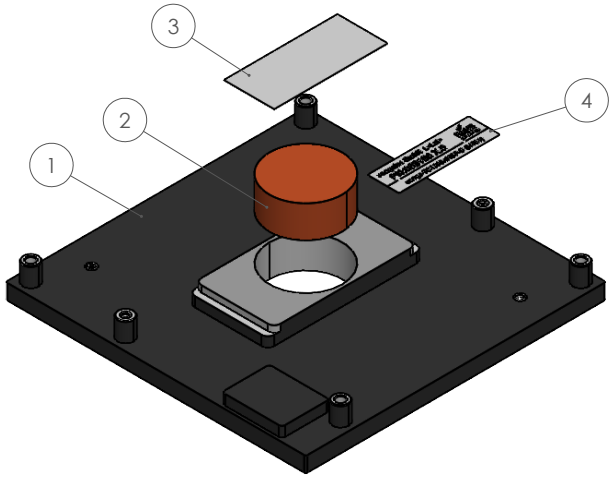




T1: M2.5 x 0.45 mm - 6H, threaded standoff for threaded version
B1: ø2.7 x 0.45 mm - 6H, non-threaded standoff for borehole version

T2: M3.5 x 0.5 mm - 6H, threaded standoff

* For threaded version
** For borehole version



Components:

1. H484 Cooling Profile HSP-T/HSP-B
2. H484 Heat Stack
3. Thermal Paste TC-5026, Size 36x16x0.12mm
4. ML0003, Label HSPCS 32x10mm, Polyester, White *

* The label reads:
PN:052154 / HSP-B for borehole version
PN:052155 / HSP-T for threaded version

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5 Connector Rows

The conga-TC1000r is connected to the carrier board via two 220-pin connectors (COM Express® Type 6 pinout). These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

5.1 PCI Express

The conga-TC1000r offers up to eight PCIe lanes, up to six lanes on the A–B connector and up to two lanes on the C–D connector. The conga-TC1000r supports the following:

- up to 16 GTps (Gen 4) speed
- a 6x1 link configuration by default (SATA controller and Ethernet controller are enabled by default) [1, 2, 3]
- lane polarity inversion

Note

1. *The SATA controller is multiplexed with PCIe6 by default.*
2. *The PCIe7 interface is used for the onboard Ethernet controller (Intel® i226) and is therefore not available for external use on variants where the controller is populated. On custom variants not featuring the Ethernet Controller on PCIe7, the PCIe7 interface may be provided as a standard PCI Express lane on the COM connector. For more information, contact your local congatec sales representative.*
3. *Ethernet Controller can also be multiplexed on PCIe5 as an optionl configuration.*

Table 10 PCIe Link Configuration (with SATA Controller and Ethernet Controller Enabled)

Lanes	PCIe 0	PCIe 1	PCIe 2	PCIe 3	PCIe 4	PCIe 5	PCIe 6	PCIe 7
Link Configuration	x1	x1	x1	x1	x1	x1	N.A	N.A
	x2		x2		x2		N.A	
	x4				N.A			

Note

1. *A maximum of six devices can be enabled in 6x1 link configuration, which is also the default configuration.*
2. *Other bifurication options require customized BIOS.*

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Table 11 PCIe Link Configuration (with the Disabled SATA Controller and no Ethernet Controller) - Customized Configurations

Lanes	PCIe 0	PCIe 1	PCIe 2	PCIe 3	PCIe 4	PCIe 5	PCIe 6	PCIe 7
Link Configuration	x1	x1	x1	x1	x1	x1	x1	x1
	x2		x2		x2		x2	
	x4				x4			

Note

Maximum of eight devices can be enabled.

5.2 PCI Express Graphics (PEG)

The conga-TC1000r supports the following PEG interface configurations on the COM Express Type 6 (C–D) connector.

Table 12 PEG Interface Configuration Options

Total PCIe lanes	PEG Configuration + NVMe Support	COM Express PEG Lanes	External PEG Interfaces
20[1]	x8 + x4 (no NVMe)	0-7, 8-11	1 x8 + 1 x4
12[2]	x4 (no NVMe)	8-11	1 x4
Optional Configurations			
20[3]	x8 + NVMe	0-7	1 x8
20[3]	x4+ x4 + x4 (no NVMe)	0-3, 8-11, 12-15	3 x4
20[3]	x4+ x4 + NVMe	0-3, 12-15	2 x4
12[3]	NVMe	N.A	N.A

Note

1. *The default PEG configuration across all variants featuring a total of 20 PCIe lanes. Refer to section 1.2 "Options Information" for an overview of variants providing 20 and 12 PCIe lanes.*
2. *The default PEG configuration across all variants featuring a total of 12 PCIe lanes. Refer to section 1.2 "Options Information" for an overview of variants providing 20 and 12 PCIe lanes.*
3. *These configurations are only available on custom variants. For more information, contact your local congatec sales representative.*

Note

The PEG lanes can not be linked together with the PCI Express lanes in section 5.1 "PCI Express".

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5.3 Display Interfaces

The conga-TC1000r offers up to five independent display interfaces:

- three DP++
- one dual-channel LVDS
- Optional VGA interface (assembly option) [1]

Note

1. *VGA signals are facilitated through a DP to VGA bridge connected to TCP3 port of the SoC. This is an assembly option requiring BOM modification.*

Note

Supported resolution depends on memory bandwidth.

5.3.1 DP++

The conga-TC1000r offers three independent DP++ interfaces. The interfaces support:

- VESA DisplayPort Standard 2.1
- Supports data-rates up to UHBR20
- VESA DSC 1.2b

5.3.2 LVDS/eDP

The conga-TC1000r offers an LVDS/eDP interface. This interface is configured in the BIOS to support LVDS by default.

The LVDS interface supports:

- single or dual channel LVDS (color depths of 18 bpp or 24 bpp)
- integrated flat panel interface with clock frequency up to 112 MHz
- VESA and JEIDA LVDS color mappings
- automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3
- resolution up to 1920x1200 in dual LVDS channel mode

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conga-TC1000r supports eDP as an assembly option (BOM change required). The eDP interface supports:

- eDP 1.4b specification
- VESA DSC 1.2a
- Spread-Spectrum Clocking

Note

The LVDS/eDP interface does not support both LVDS and eDP signals at the same time.

5.4 SATA

The conga-TC1000r supports two SATA interfaces by default and two port SATA controller (JMICRON - JMB582) is integrated to realize SATA Port 0 and SATA Port 1. The interfaces support:

- SATA specification revision 3.2
- data transfer rates up to 6.0 Gb/s
- Hot-plug detect

Note

1. *The SATA controller is multiplexed with PCIe6. SATA ports are enabled by default.*
2. *Switching between SATA and PCIe support is available as an assembly option and requires BOM modification.*
3. *The interface does not support legacy mode using I/O space.*

5.5 Optional SSD

The conga-TC1000r offers a x4 PCIe Gen 5 port for an optional onboard NVMe SSD (Gen3/4) storage. This option is only available on custom variants. For more information, contact your local congatec sales representative.

5.6 USB

The conga-TC1000r offers the following USB interfaces:

- up to eight USB 2.0 ports

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- up to four USB 3.2 Gen 2
- up to two USB4 ports

Note

To support all four super speed ports on the COM Express connector, a USB hub (TUSB8041A) is included in the default configuration, providing two additional ports (USB2/USB_SS[T/R]X2 and USB3/USB_SS[T/R]X3). The hub can be removed as an assembly option if the two ports directly connected to the SoC are sufficient.

5.6.1 USB 2.0

The conga-TC1000r offers up to eight USB 2.0 interfaces on the A–B connector. The interfaces support:

- USB 2.0 specification
- High-Speed, Full-Speed and Low-Speed USB signaling
- data transfers of up to 480 Mbps

Note

The number of USB 2.0 ports reduces if USB 3.2 or USB4 is implemented.

5.6.2 USB 3.2

The conga-TC1000r offers SuperSpeed signals for up to four USB 3.2 ports, each supporting up to USB 3.2 Gen 2x1 (10 Gbps). The configurations featuring the onboard USB hub (including the default configuration) [1] facilitates two additional USB 3.2 ports in addition to the two directly connected USB 3.2 ports.

The xHCI host controller supports:

- USB 3.2 specification
- SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling
- data transfers of up to 10 Gbps for USB 3.2 Gen 2x1 port
- data transfers of up to 5 Gbps for USB 3.2 Gen 1x1 port
- supports USB debug port on all USB 3.2 capable ports

Note

1. *The USB hub can be removed in custom variants with BOM modification. In configurations not featuring the USB hub, only two USB 3.2*

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ports are available. For more information, contact your local congatec sales representative.

Note

1. *Ensure the carrier board is designed for USB 3.2 Gen 2 operation (with onboard USB redriver). For USB 3.2 Gen 2 design considerations, contact congatec technical support center.*

2. *Each USB 3.2 port requires one USB 2.0 port and corresponding USB 3.2 SuperSpeed signals.*

5.6.3 USB4

conga-TC1000r does not support USB4 in the default configuration. As an assembly option, conga-TC1000r offers up to two USB4 ports. These ports support:

- DisplayPort 2.1 specification
- USB-C specification
- Data rate of up to 40 Gbps (requires two differential signals and USB-C connector)
- Power saving when USB-C is disconnected
- Wake capability
- USB dual role

Note

At the time of the release of this user guide, USB4 support has not been tested by congatec. Please consult product documentation in conga-wiki and contact congatec Support for more information.

Note

1. *USB4 port 1 is shared with DDI1 while USB port 2 is shared with DDI2. USB4 support is provided as an assembly option requiring BOM modification.*

2. *Each USB4 port requires one USB 2.0 port with corresponding USB4 SuperSpeed signals. For the first USB4 port, use USB 2.0 port 4. For the second USB4 port, use USB 2.0 port 5.*

3. *USB4 ports (also the corresponding USB 2.0 ports) require a PD controller and retimer to function with the default BIOS. These ports may optionally be used as USB 3.2 Gen 2x1 ports (or lower) without a PD controller and retimer (Custom BIOS Option).*

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5.7 NBASE-T Ethernet

The conga-TC1000r offers a 2.5 Gigabit Ethernet interface via an onboard Intel® i226-LM/IT controller. The interface supports:

- full-duplex operation at 10/100/1000/2500 Mbps [1,2]
- half-duplex operation at 10/100 Mbps [1,2]
- Time Sensitive Networking [3]
- Wake on LAN

The table below describes the LED signals of NBASE-T Ethernet interface.

Table 13 NBASE-T Ethernet LED Description

Signals	Description
GBE0_ACT#	Ethernet controller activity indicator
GBE0_LINK# [1, 2]	Ethernet controller link indicator
GBE0_LINK_MID# [2]	Ethernet controller link indicator for 1000 Mbps (lower link speed)
GBE0_LINK_MAX# [2]	Ethernet controller link indicator for 2500 Mbps (maximum link speed)

Note

1. *The GBE0_LINK# output is not active during a 10 Mb and 100 Mb connection. It is only active during a 1 Gb or 2.5 Gb connection. This is a limitation of Ethernet controller since it has only three LED outputs.*
2. *The GBE0_LINK# signal is a logic AND of the GBE0_LINK_MID# and GBE0_LINK_MAX# signals on the conga-TC1000r module.*
3. *Not supported in Windows Operating Systems.*

The Intel® i226-LM/IT controller is connected on the PCIe7 and as an optional configuration, the controller can be moved to PCIe5, making the the PCIe7 available on the COM connector.

5.8 High Definition Audio

The conga-TC1000r provides an HD audio interface on the A–B connector. Optionally, SoundWire interface can be connected instead of the HDA interface. For more information, contact your local sales representative.

5.9 General Purpose SPI

The conga-TC1000r offers a General Purpose SPI interface via the KSC 2.0 by default and from the PTL-SOC as an assembly option.

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5.10 SPI

The conga-TC1000r offers an onboard Winbond® W25Q256JWPIQ SPI flash.

You can boot the conga-TC1000r from the carrier board if you integrate an off-module flash device (BIOS) on the carrier board. This implementation is especially useful when evaluating a customized BIOS.

conga-TC1000r offers an optional configuration with discrete SPI TPM (Infineon SLB9672) connected to the SPI bus of the SoC.

5.10.1 BIOS Flash Selection

The boot select pins BIOS_DIS0# and BIOS_DIS1# are configured to load the firmware BIOS from the conga-TC1000r by default. Optionally, you can configure these pins to load the boot firmware from the carrier board flash as described in the table below.

Table 14 BIOS Select Options

BIOS_DIS1#	BIOS_DIS0#	Boot Option
N.C	N.C	Boot from module SPI flash (default)
GND	N.C	Boot from carrier board SPI flash

5.11 UART/CAN

conga-TC1000r offers two standard UART interfaces (UART0 and UART1) via embedded board controller KSC 2.0 by default [1]. These interfaces comply with UART 16550 protocol and they support up to 115200 bps. The UART interfaces do not support hardware handshake and flow control.

conga-TC1000r does not support CAN interface.

Note

1. *UART0 and UART1 ports of COM Connector can be directly connected to the SoC instead of the KSC 2.0 as an optional configuration requiring BOM modification.*

5.12 LPC Bus

The conga-TC1000r offers the LPC bus through an eSPI to LPC bridge. The nominal clock frequency of the bridge is 24 MHz. For information about the decoded LPC addresses, see section 9 “System Resources”.

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The LPC interface is connected to the Enhanced Serial Peripheral Interface (eSPI) controller of the SoC via a Microchip ECE1200 eSPI to LPC bridge by default. Optionally, the conga-TC1000r can offer eSPI instead of LPC (assembly option).

Based on the configuration used (LPC or eSPI enabled), the ESPI_EN# signal has to routed properly. ESPI_EN# signals to the module whether LPC or eSPI is used. If ESPI_EN# is unconnected on the carrier, LPC operation is expected. On contrary for eSPI operation, ESPI_EN# has to be connected to GND on the carrier. To be able to detect the correct mode of operation, the module will implement a pull-up resistor on this signal. The module refuses to boot up if the module and carrier configurations do not match.

Note

The LPC clock frequency is 24 MHz. The LPC_DRQ# signal is not supported.

5.13 I²C Bus

The I²C bus is implemented through the KSC 2.0. The KSC 2.0 provides a fast-mode, multi-master I²C bus with maximum I²C bandwidth.

Table 15 Reserved I²C Addresses

8-bit Device Address	Device	Description
0xA0	Module EEPROM [1]	Module Embedded EEPROM (JIDA EEPROM)
0xAE	Carrier board EEPROM [1, 2]	Reserved for COM Express® carrier board EEPROM
0x64	external RTC [1, 2]	
0xC0	DP-to-LVDS bridge	Internal I2C devices
0x40	DP-to-VGA bridge	
0xA0	external LVDS EEPROM	
0x20	IMVP9.3 voltage regulator	

Note

1. *External user-accessible I2C - available at COMe pins I2C_CK, I2C_DAT*
2. *Optional*

5.14 GPIOs

conga-TC1000r offers eight General Purpose Input/Output signals on the A–B connector for custom designs. The GPIOs are controlled by the embedded controller KSC 2.0.

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5.15 SMBus

On conga-TC1000r, the System Management Bus is provided by the SoC and can be accessed at the COM express pinout. It is an I²C bus variant for system management functions. SM Bus is routed on the module to the NVMe, COMe Connector, and to the KSC 2.0.

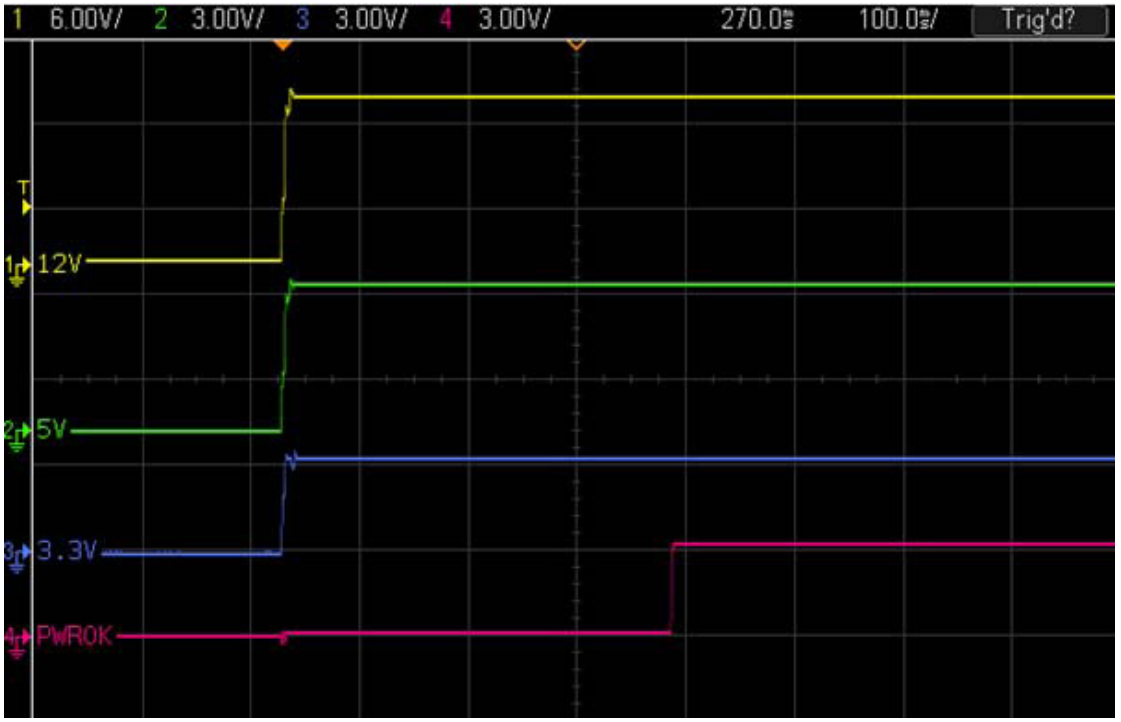
5.16 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system.

A sample screenshot is shown below:



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Note

The module remains in power-off state as long as the PWR_OK is driven by carrier board hardware.

The conga-TC1000r supports the controlling of ATX-style power supplies. If you do not use an ATX power supply, do not connect the conga-TC1000r pins SUS_S3, 5V_SB, and PWRBTN#.

SUS_S3#

The SUS_S3# (pin A15 on the A–B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. To accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies, PWRBTN# (pin B12 on the A–B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_VSB using a 100 kΩ resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

The 12 V input power is the sole operational power source for the conga-TC1000r. The other voltages required are generated internally on the module using onboard voltage regulators.

Note

When designing a power supply for a conga-TC1000r application, be aware that the system may malfunction when a 12 V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.

This problem occurs because some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.

To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope, during the power supply qualification phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

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5.16.1 Power Management

ACPI

The conga-TC1000r supports Advanced Configuration and Power Interface (ACPI) specification, revision 6.0a. It also supports Suspend to RAM and Suspend to Disk. For more information, see section 7.6 “ACPI Suspend Modes and Resume Events”.

5.16.2 Inrush Current

The inrush current of the conga-TC1000r is listed below.

Table 16 Inrush Current

Power Rail	Current [A]	Slew Rate [kV/s]	Voltage Ramp [ms]	Comment
VCC_12V	TBD	TBD	TBD	Typical scenario
VCC_5V_SBY	TBD	TBD	TBD	
VCC_12V	TBD	TBD	TBD	Worst-case scenario
VCC_5V_SBY	TBD	TBD	TBD	

Note

Ensure the power supply and decoupling capacitors on the carrier board are adequate for proper power sequencing.

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6 Additional Features

The following additional features are available on the conga-TC1000r.

6.1 KSC 2.0

The conga-TC1000r is equipped with Microchip MEC1521 microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or I²C bus from the x86 core architecture, resulting in higher performance and reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The KSC 2.0 supports the following features:

- Board information
- Watchdog
- Power loss control
- Fan control
- General Purpose SPI (see section 5.9 “General Purpose SPI”)
- UART (see section 5.11 “UART/CAN”)
- I2C bus (see section 5.13 “I²C Bus”)
- General Purpose Input/Output (see section 5.14 “GPIOs”)
- SMBus (see section 5.15 “SMBus”)
- User EEPROM space

6.1.1 Board Information

The KSC 2.0 provides access to manufacturing and board information stored in COMe defined EEPROM storage, including serial number, hardware revision of the module, production date etc. It also provides information about the firmware and its components running on the controller.

6.1.2 Watchdog

The conga-TC1000r is equipped with a multi stage watchdog solution that is triggered by software.

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Note

conga-TC1000r module does not support the watchdog NMI mode.

6.1.3 Power Loss Control

The CPU provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The power loss control feature has two different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition

Note

The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.

6.1.4 Fan Control

The conga-TC1000r offers signals for fan control, thereby improving system management. The FAN_PWMOUT signal controls the system fan with PWM (Pulse Width Modulation) while the FAN_TACHIN signal provides the ability to monitor the system's fan RPMs (revolutions per minute).

Note

1. *Only a 3-wire fan is supported on the module.*
2. *For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express® Design Guide.*

6.2 OEM BIOS Customization

The conga-TC1000r is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS.

The customization features supported are described below:

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6.2.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary through AMI SCE Tool. This tool is not supported on the standard BIOS release, thus it requires customized BIOS to enable support for this tool. Contact congatec technical support for more information regarding AMI SCE Tool.

6.2.2 OEM BIOS Code/Data

With the congatec embedded BIOS, it used to be possible for system designers to add their own code to the BIOS POST process. This feature is no longer supported with the new UEFI based firmware.

6.2.3 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.3 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec has defined an interface for the exchange of data between a x86 CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The latest BIOS offers a proprietary interface to the KSC which allows the servicing of the battery related ACPI functions in an OS ACPI engine. It uses either LTC1760 battery manager or LTC4100 single battery charger, which can be connected via SMBus to the system.

For more information about the supported Battery Management Interface contact your local congatec sales representative.

6.4 Suspend to Ram

The Suspend to RAM feature is available on the conga-TC1000r.

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7 conga Tech Notes

The Intel Panther Lake (PTL) processor is a 64-bit, multi-core processor built on Intel 18A process, N6 and N3E technology. Some of the important features supported by the processor are:

- Intel® Image Processing Unit 7.5 (Intel® IPU 7.5)
- Intel® Neural Processing Unit (Intel® NPU)
- Intel® VT-x and VT-d
- Intel® Turbo Boost Technology 2.0
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)
- Intel® Thread Director
- Intel® Boot Guard
- Intel® SpeedStep Technology
- Intel® Active Management Technology (Intel® AMT)
- Intel® Platform Trust Technology (Intel® PTT)
- Intel® Dynamic Tuning Technology (Intel® DTT)
- Intel® Total Memory Encryption (Intel® TME)
- Intel® Volume Management Device (Intel® VMD)
- Intel® High Definition Audio (HD Audio)
- Intel® Smart Sound Technology (SST)
- Intel® Active Management Technology (AMT)

7.1 Processor Performance Control

7.1.1 Intel® SpeedStep® Technology (EIST)

Intel® processors found on the conga-TC1000r run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® Technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states to efficiently operate the processor when it is not being fully used. The operating system will determine the

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necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that the power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

The Intel® Core™ Ultra Series 3 processor family supports Intel® Speed Shift, a new and energy efficient method for frequency control. This feature is also referred to as Hardware-controlled Performance States (HWP). The feature is a hardware implementation of the ACPI defined Collaborative Processor Performance Control (CPPC2) and is supported by newer operating systems (Win 8.1 or newer).

With this feature enabled, the processor autonomously selects performance states based on workload demand and thermal limits while also considering information provided by the OS e.g., the performance limits and workload history.

7.1.2 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology allows processor cores to run faster than the base operating frequency if it is operating below power, current, and temperature specification limits. Intel® Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state. The maximum frequency of Intel® Turbo Boost Technology depends on the number of active cores. The amount of time the processor spends in the Intel® Turbo Boost Technology state depends on the workload and operating environment.

Any of the following can set the upper limit of Intel® Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating within its defined power and thermal limits and the workload demands additional performance, the processor frequency dynamically increases above the base frequency until the upper limit is reached or the maximum achievable frequency for the number of active cores is attained.

For more information about Intel® Turbo Boost Technology, visit the Intel® website.

Note

1. *For real-time sensitive applications, disable EIST and Turbo Mode in the BIOS setup to ensure a more deterministic performance.*
2. *Disable Turbo mode for industrial use condition.*

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7.2 Intel® Neural Processing Unit (Intel® NPU)

The Intel® Neural Processing Unit (NPU) is a dedicated hardware accelerator integrated into Intel® Panther Lake processors. It enables high-performance processing for AI applications while maintaining optimized power consumption, making it suitable for embedded, edge, and client platforms. The NPU offloads AI-related tasks from the CPU and GPU, improving overall system efficiency and responsiveness. It consists of a host control subsystem and a deep learning accelerator, which together manage task scheduling and execution. The deep learning accelerator is based on multiple Neural Compute Engine (NCE) tiles that provide scalable parallel processing capabilities. These tiles integrate specialized compute units and local memory to efficiently process neural network operations.

7.3 Adaptive Thermal Monitor and Catastrophic Thermal Protection

Intel® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu “CPU submenu”.

The Adaptive Thermal Monitor controls the processor temperature using two methods:

- Adjusting the processor’s operating frequency and core voltage (EIST transitions)
- Modulating (start/stop) the processor’s internal clocks at a duty cycle of 25% on and 75% off

When activated, the TCC causes both processor core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated. Clock modulation is activated if frequency and voltage adjustments are insufficient. Additional hardware, software driver, or operating system support is not required.

Intel processors use the THERMTRIP# signal to shut down the system if the processor’s silicon reaches a temperature of approximately 125°C. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

Note

To ensure the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® processor’s respective datasheet can provide you with more information about this subject.

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7.4 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets.

Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) have hardware support in the processor to improve the virtualization performance and robustness.

7.5 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to implement cooling decisions according to the demands of the application.

The conga-TC1000r offers hardware-based support for passive and active cooling. Passive cooling is implemented in the Intel CPU via the Thermal Control Circuit (TCC) Activation Offset setting in the CPU configuration setup sub-menu. The TCC in the processor is activated at 100°C by default but can be lowered by the Activation Offset—for example, an activation offset of "10" will activate TCC at 90°C. ACPI OS support is not required. See section 7.3 "**Adaptive Thermal Monitor and Catastrophic Thermal Protection**" for more information

The congatec board controller supports active cooling solution. The board controller controls the fan's speed based on the temperature readings of the CPU. This feature does not require ACPI OS support. The only software-controlled thermal trip point on conga-TC1000r is the Critical Trip Point.

The active or passive cooling policy should ensure that the CPU temperature does not reach this trip point. However, if the critical trip point is reached, the OS will shut down properly in order to prevent damage to the system.

Use the "critical trip point" setup node in the BIOS setup menu to determine the temperature threshold at which the system shuts down.

Note

The Automatic Critical Trip Point BIOS setting shuts down the system at 5°C above the maximum specified temperature of the processor

7.6 ACPI Suspend Modes and Resume Events

The conga-TC1000r BIOS supports S3 (Suspend to RAM), S4 (Suspend to Disk) and S5 (Soft-Off).

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Table 17 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5
Onboard LAN Event	Device driver must be configured to support Wake On LAN.
SMBALERT#	Wakes unconditionally from S3-S5
PCI Express WAKE#	Wakes unconditionally from S3-S5
WAKE#	Wakes unconditionally from S4
PME#	Activate the wake-up capabilities of a PCI device using Windows Device Manager configuration options or set Resume On PME# to "Enabled" in the BIOS setup menu.
USB Mouse/Keyboard Event	When standby mode is set to S4, USB hardware must be powered by standby power source. Set "USB Device Wakeup" from "S4" to "Enabled" in the ACPI section of the BIOS setup menu (if setup node is available in BIOS setup program). In Device Manager, look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.

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8 Signal Descriptions and Pinout Tables

The following section describes the signals on the conga-TC1000r COM Express® Type 6 connectors. The pinout of the modules complies with COM Express® Type 6, rev. 3.1.

The table below describes the terminology used in this section. The PU/PD column indicates if a pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Table 18 Signal Tables Terminology Descriptions

Term	Description
DDC	Display Data Channel
I/O 3.3V	Bi-directional signal 3.3 V tolerant
I/O 5V	Bi-directional signal 5 V tolerant
I 3.3V	Input 3.3 V tolerant
I 5V	Input 5 V tolerant
I/O 3.3VSB	Input or output 3.3 V tolerant active in standby state
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
O 3.3V	Output 3.3 V signal level
O 5V	Output 5 V signal level
OD	Open drain output
P	Power Input/Output
PCIE	PCI Express compatible differential signal. In compliance with PCI Express Specification.
PD	Implemented pull-down resistor
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the carrier board.
PEG	PCI Express Graphics
PU	Implemented pull-up resistor
REF	Reference voltage output. May be sourced from a module power plane.
SATA	In compliance with Serial ATA specification revision 2.6 and 3.0.
USB_SS	USB Super Speed compliant signals. This includes USB 3.0, USB 3.1, USB 3.2 and USB4.

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8.1 Connector Signal Descriptions

Table 19 Connector A–B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#/(ESPI_CS0# [3])	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK_MID#	B4	LPC_AD0/(ESPI_IO_0 [3])	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK_MAX#	B5	LPC_AD1/(ESPI_IO_1 [3])	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2/(ESPI_IO_2 [3])	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3/(ESPI_IO_3 [3])	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0# /(ESPI_ALERT0# [3])	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# [1] /(ESPI_ALERT1#)	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK/(ESPI_CK [3])	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+ [3]	B16	SATA1_TX+ [3]	A71	eDP_TX2+/LVDS_A0+ [3]	B71	LVDS_B0+
A17	SATA0_TX- [3]	B17	SATA1_TX- [3]	A72	eDP_TX2-/LVDS_A0- [3]	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#/(ESPI_RESET# [3])	A73	eDP_TX1+/LVDS_A1+ [3]	B73	LVDS_B1+
A19	SATA0_RX+ [3]	B19	SATA1_RX+ [3]	A74	eDP_TX1-/LVDS_A1- [3]	B74	LVDS_B1-
A20	SATA0_RX- [3]	B20	SATA1_RX- [3]	A75	eDP_TX0+/LVDS_A2+ [3]	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	eDP_TX0-/LVDS_A2- [3]	B76	LVDS_B2-
A22	SATA2_TX+ [1, 3]	B22	SATA3_TX+ [1, 3]	A77	eDP_VDD_EN/LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX- [1, 3]	B23	SATA3_TX- [1, 3]	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP_BKLT_EN/LVDS_BKLT_EN [3]
A25	SATA2_RX+ [1, 3]	B25	SATA3_RX+ [1, 3]	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX- [1, 3]	B26	SATA3_RX- [1, 3]	A81	eDP_TX3+/LVDS_A_CK+ [3]	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	eDP_TX3-/LVDS_A_CK- [3]	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	(HDA_SDIN2 [1])/(SNDW0_CLK [3])	A83	eDP_AUX+/LVDS_I2C_CK [3]	B83	eDP_BKLT_CTRL/LVDS_BKLT_CTRL [3]
A29	HDA_SYNC	B29	(HDA_SDIN1 [1])/(SNDW0_DAT [3])	A84	eDP_AUX-/LVDS_I2C_DAT [3]	B84	VCC_5V_SBY
A30	HDA_RST#	B30	HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY

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Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A31	GND (FIXED)	B31	GND (FIXED)	A86	GP_SPI_MOSI	B86	VCC_5V_SBY
A32	HDA_BITCLK	B32	SPKR [2]	A87	eDP_HPD	B87	VCC_5V_SBY
A33	HDA_SDOUT	B33	I2C_CK	A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE_CLK_REF-	B89	VGA_RED [3]
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN [3]
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU [3]
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC [3]
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC [3]
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK [3]
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP [3]	B96	VGA_I2C_DAT [3]
A42	USB2-	B42	USB3-	A97	TYPE10# [1]	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	GP_SPI_MISO
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	GP_SPI_CK
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI_EN#	A102	SER1_RX	B102	FAN_TACHIN
A48	RSMRST_OUT#	B48	USB0_HOST_PRSNT [1]	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ/(ESPI_CS1#[2])	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+ [3]	B52	PCIE_RX5+ [3]	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5- [3]	B53	PCIE_RX5- [3]	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

1. *Not connected*
2. *Not supported in the default configuration.*
3. *Assembly option associated. See section 5 "Connector Rows" and respective signal description tables below for more information.*

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Table 20 Connector C–D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1- [6]	D56	PEG_TX1- [6]
C2	GND	D2	GND	C57	TYPE1# [1]	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+ [6]	D58	PEG_TX2+ [6]
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2- [6]	D59	PEG_TX2- [6]
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PEG_RX3+ [6]	D61	PEG_TX3+ [6]
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PEG_RX3- [6]	D62	PEG_TX3- [6]
C8	GND	D8	GND	C63	GND	D63	GND
C9	USB_SSRX2- [4]	D9	USB_SSTX2- [4]	C64	GND	D64	GND
C10	USB_SSRX2+ [4]	D10	USB_SSTX2+ [4]	C65	PEG_RX4+ [6]	D65	PEG_TX4+ [6]
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4- [6]	D66	PEG_TX4- [6]
C12	USB_SSRX3- [4]	D12	USB_SSTX3-[4]	C67	RAPID_SHUTDOWN [1, 2]	D67	GND
C13	USB_SSRX3+ [4]	D13	USB_SSTX3+ [4]	C68	PEG_RX5+ [6]	D68	PEG_TX5+ [6]
C14	GND	D14	GND	C69	PEG_RX5- [6]	D69	PEG_TX5- [6]
C15	USB4_1_LSTX	D15	DDI1_CTRLCLK_AUX+/USB4_1_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	USB4_1_LSRX	D16	DDI1_CTRLDATA_AUX-/USB4_1_AUX-	C71	PEG_RX6+ [6]	D71	PEG_TX6+ [6]
C17	USB4_RT_ENA	D17	USB4_PD_I2C_ALERT#	C72	PEG_RX6- [6]	D72	PEG_TX6- [6]
C18	GND	D18	PMCALERT#	C73	GND	D73	GND
C19	PCIE_RX6+ [2,3]	D19	PCIE_TX6+ [2,3]	C74	PEG_RX7+ [6]	D74	PEG_TX7+ [6]
C20	PCIE_RX6- [2, 3]	D20	PCIE_TX6- [2,3]	C75	PEG_RX7- [6]	D75	PEG_TX7- [6]
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+ [2, 3]	D22	PCIE_TX7+ [2,3]	C77	GND	D77	GND
C23	PCIE_RX7- [2, 3]	D23	PCIE_TX7- [2,3]	C78	PEG_RX8+ [7]	D78	PEG_TX8+ [7]
C24	DDI1_HPD	D24	GND	C79	PEG_RX8- [7]	D79	PEG_TX8- [7]
C25	SML0_CLK	D25	GND	C80	GND (FIXED)	D80	GND (FIXED)
C26	SML0_DAT	D26	DDI1_PAIR0+/USB4_1_SSTX0+ [2, 5]	C81	PEG_RX9+ [6, 7]	D81	PEG_TX9+ [7]
C27	SML1_CLK	D27	DDI1_PAIR0-/USB4_1_SSTX0- [2, 5]	C82	PEG_RX9- [6, 7]	D82	PEG_TX9- [7]
C28	SML1_DAT	D28	GND	C83	GND	D83	GND
C29	USB4_PD_I2C_CLK	D29	DDI1_PAIR1+/USB4_1_SSRX0+ [2, 5]	C84	GND	D84	GND
C30	USB4_PD_I2C_DAT	D30	DDI1_PAIR1-/USB4_1_SSRX0- [2, 5]	C85	PEG_RX10+ [7]	D85	PEG_TX10+ [7]
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- [7]	D86	PEG_TX10- [7]
C32	DDI2_CTRLCLK_AUX+/USB4_2_AUX+ [5]	D32	DDI1_PAIR2+/USB4_1_SSTX1+ [2, 5]	C87	GND	D87	GND
C33	DDI2_CTRLDATA_AUX-/USB4_2_AUX- [2, 5]	D33	DDI1_PAIR2-/USB4_1_SSTX1- [2, 5]	C88	PEG_RX11+ [7]	D88	PEG_TX11+ [7]

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Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11- [7]	D89	PEG_TX11- [7]
C35	USB4_2_LSTX [2]	D35	USB4_2_LSRX [2]	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+/USB4_1_SSRX1+ [2, 5]	C91	PEG_RX12+ [1]	D91	PEG_TX12+ [1]
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-/USB4_1_SSRX1- [2, 5]	C92	PEG_RX12- [1]	D92	PEG_TX12- [1]
C38	DDI3_DDC_AUX_SEL	D38	GND	C93	GND	D93	GND
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+/USB4_2_SSTX0+ [2, 5]	C94	PEG_RX13+ [1]	D94	PEG_TX13+ [1]
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-/USB4_2_SSTX0- [2, 5]	C95	PEG_RX13- [1]	D95	PEG_TX13- [1]
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+/USB4_2_SSRX0+ [2, 5]	C97	GND	D97	GND
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-/USB4_2_SSRX0- [2, 5]	C98	PEG_RX14+ [1]	D98	PEG_TX14+ [1]
C44	DDI3_HPD	D44	DDI2_HPD	C99	PEG_RX14- [1]	D99	PEG_TX14- [1]
C45	GP_SPI_CS#	D45	GND	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+/USB4_2_SSTX1+ [2, 5]	C101	PEG_RX15+ [1]	D101	PEG_TX15+ [1]
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-/USB4_2_SSTX1- [2, 5]	C102	PEG_RX15- [1]	D102	PEG_TX15- [1]
C48	RSVD [1]	D48	GND	C103	GND	D103	GND
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+/USB4_2_SSRX1+ [2, 5]	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-/USB4_2_SSRX1- [2, 5]	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+ [6]	D52	PEG_TX0+ [6]	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0- [6]	D53	PEG_TX0- [6]	C108	VCC_12V	D108	VCC_12V
C54	TYPE0# [1]	D54	PEG_LANE_RV# [2]	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+ [6]	D55	PEG_TX1+ [6]	C110	GND (FIXED)	D110	GND (FIXED)

Note

1. *Not connected*
2. *Not supported in the default configuration.*
3. *Assembly option associated. See section 5 "Connector Rows" and respective signal description tables below for more information.*
4. *Not supported on optional configurations having no USB hub.*
5. *USB4 is not supported on conga-TC1000r.*
6. *Not connected on variants with H404 and H12Xe SKUs.*
7. *PEG ports 8 to 11 available only on variants without optional on-module NVMe.*

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Table 21 PCI Express Signal Descriptions (General Purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair	I PCIE		
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair	O PCIE		
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair	I PCIE		
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair	O PCIE		
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair	I PCIE		
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair	O PCIE		
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair	I PCIE		
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair	O PCIE		
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair	I PCIE		
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair	O PCIE		
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair	I PCIE		
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair	O PCIE		
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair	I PCIE		Not supported in default configuration SATA Ports 0 and 1 (default) PCIe Port 6 (available as an assembly option with no SATA support)
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair	O PCIE		
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair	I PCIE		Assembly option. Not connected by default. PCIe Port 7 can be connected to the COM connector instead of the Ethernet interface as an assembly option.
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair	O PCIE		
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes	O PCIE		100 MHz

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Table 22 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+ PEG_RX0-	C52 C53	PCI Express Graphics differential pairs 0 *Note: Can also be used as PCI Express differential pairs 16*	I PCIE		PEG 0-7 are directly connected to the SOC PORT D on selected CPU SKUs
PEG_TX0+ PEG_TX0-	D52 D53		O PCIE		
PEG_RX1+ PEG_RX1-	C55 C56	PCI Express Graphics differential pairs 1 *Note: Can also be used as PCI Express differential pairs 17*	I PCIE		
PEG_TX1+ PEG_TX1-	D55 D56		O PCIE		
PEG_RX2+ PEG_RX2-	C58 C59	PCI Express Graphics differential pairs 2 *Note: Can also be used as PCI Express differential pairs 18*	I PCIE		
PEG_TX2+ PEG_TX2-	D58 D59		O PCIE		
PEG_RX3+ PEG_RX3-	C61 C62	PCI Express Graphics differential pairs 3 *Note: Can also be used as PCI Express differential pairs 19*	I PCIE		
PEG_TX3+ PEG_TX3-	D61 D62		O PCIE		
PEG_RX4+ PEG_RX4-	C65 C66	PCI Express Graphics differential pairs 4 *Note: Can also be used as PCI Express differential pairs 20*	I PCIE		
PEG_TX4+ PEG_TX4-	D65 D66		O PCIE		
PEG_RX5+ PEG_RX5-	C68 C69	PCI Express Graphics differential pairs 5 *Note: Can also be used as PCI Express differential pairs 21*	I PCIE		
PEG_TX5+ PEG_TX5-	D68 D69		O PCIE		
PEG_RX6+ PEG_RX6-	C71 C72	PCI Express Graphics differential pairs 6 *Note: Can also be used as PCI Express differential pairs 22*	I PCIE		
PEG_TX6+ PEG_TX6-	D71 D72		O PCIE		
PEG_RX7+ PEG_RX7-	C74 C75	PCI Express Graphics differential pairs 7 *Note: Can also be used as PCI Express differential pairs 23*	I PCIE		
PEG_TX7+ PEG_TX7-	D74 D75		O PCIE		

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Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX8+ PEG_RX8-	C78 C79	PCI Express Graphics differential pairs 8 *Note: Can also be used as PCI Express differential pairs 24*	I PCIE		Optionally, an on-module NVMe (assembly option) can be connected instead of PEG Ports 8 to 11 (default). [1, 2, 3]
PEG_TX8+ PEG_TX8-	D78 D79		O PCIE		
PEG_RX9+ PEG_RX9-	C81 C82	PCI Express Graphics differential pairs 9 *Note: Can also be used as PCI Express differential pairs 25*	I PCIE		
PEG_TX9+ PEG_TX9-	D81 D82		O PCIE		
PEG_RX10+ PEG_RX10-	C85 C86	PCI Express Graphics differential pairs 10 *Note: Can also be used as PCI Express differential pairs 26*	I PCIE		
PEG_TX10+ PEG_TX10-	D85 D86		O PCIE		
PEG_RX11+ PEG_RX11-	C88 C89	PCI Express Graphics differential pairs 11 *Note: Can also be used as PCI Express differential pairs 27*	I PCIE		
PEG_TX11+ PEG_TX11-	D88 D89		O PCIE		
PEG_RX12+ PEG_RX12-	C91 C92	PCI Express Graphics differential pairs 12 *Note: Can also be used as PCI Express differential pairs 28*	I PCIE		Not connected on conga-TC1000r
PEG_TX12+ PEG_TX12-	D91 D92		O PCIE		
PEG_RX13+ PEG_RX13-	C94 C95	PCI Express Graphics differential pairs 13 *Note: Can also be used as PCI Express differential pairs 29*	I PCIE		
PEG_TX13+ PEG_TX13-	D94 D95		O PCIE		
PEG_RX14+ PEG_RX14-	C98 C99	PCI Express Graphics differential pairs 14 *Note: Can also be used as PCI Express differential pairs 30*	I PCIE		
PEG_TX14+ PEG_TX14-	D98 D99		O PCIE		
PEG_RX15+ PEG_RX15-	C101 C102	PCI Express Graphics differential pairs 15 *Note: Can also be used as PCI Express differential pairs 31*	I PCIE		
PEG_TX15+ PEG_TX15-	D101 D102		O PCIE		
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I 3.3 V	PU 100 kΩ 3.3 V	

Note

1. *Only PEG ports 8 to 11 are available on module variants with H404 and H12Xe SKUs.*
2. *Optionally, all module variants can offer an on-module NVMe instead of PEG ports 8 to 11 (assembly option).*
3. *An x16 card in a carrier-board x16 slot with all lanes connected directly to the COMe PEG port may experience functional issues. This configuration has not been tested, and therefore, further action such as disabling the upper port in BIOS may be required. Contact congatec support should you require more information.*

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Table 23 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with DP1_LANE0+, TMDS1_DATA2+ and USB4_1_SSTX0+ Multiplexed with DP1_LANE0-, TMDS1_DATA2- and USB4_1_SSTX0- DDI1 differential pair 0	O LV_DIFF		
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with DP1_LANE1+, TMDS1_DATA1+ and USB4_1_SSRX0+ Multiplexed with DP1_LANE1-, TMDS1_DATA1- and USB4_1_SSRX0- DDI1 differential pair 1	O LV_DIFF		
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with DP1_LANE2+, TMDS1_DATA0+ and USB4_1_SSTX1+ Multiplexed with DP1_LANE2-, TMDS1_DATA0- and USB4_1_SSTX1- DDI1 differential pair 2	O LV_DIFF		
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with DP1_LANE3+, TMDS1_CLK+ and USB4_1_SSRX1+ Multiplexed with DP1_LANE3-, TMDS1_CLK- and USB4_1_SSRX1- DDI1 differential pair 3	O LV_DIFF		
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD DDI1 Hot plug detect	I 3.3 V	PD 100 kΩ	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with DP1_AUX+, HDMI1_CTRLCLK and USB4_1_AUX+ DisplayPort AUX+ or USB4 AUX+ function if DDI1_DDC_AUX_SEL is no connect or TMDS I²C control clock if DDI1_DDC_AUX_SEL is pulled high.	I/O LV_DIFF or I/O OD 3.3 V	PD 100 kΩ (DP mode)	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with DP1_AUX-, HDMI1_CTRLDATA and USB4_1_AUX- DisplayPort AUX- or USB4 AUX- function if DDI1_DDC_AUX_SEL is no connect or TMDS I²C control data if DDI1_DDC_AUX_SEL is pulled high.	I/O LV_DIFF or I/O OD 3.3 V	PU 100 kΩ (DP mode)	
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX- This pin shall have a 1 MΩ pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled- high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3 V	PD 1 MΩ	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+, TMDS2_DATA2+ and USB4_2_SSTX0+ Multiplexed with DP2_LANE0-, TMDS2_DATA2- and USB4_2_SSTX0- DDI2 differential pair 0	O LV_DIFF		
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+, TMDS2_DATA1+ and USB4_2_SSRX0+ Multiplexed with DP2_LANE1-, TMDS2_DATA1- and USB4_2_SSRX0- DDI2 differential pair 1	O LV_DIFF		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+, TMDS2_DATA0+ and USB4_2_SSTX1+ Multiplexed with DP2_LANE2-, TMDS2_DATA0- and USB4_2_SSTX1- DDI2 differential pair 2	O LV_DIFF		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+, TMDS2_CLK+ and USB4_2_SSRX1+ Multiplexed with DP2_LANE3-, TMDS2_CLK- and USB4_2_SSRX0- DDI2 differential pair 3	O LV_DIFF		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD DDI2 hot plug detect	I 3.3 V	PD 100 kΩ	
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+, HDMI2_CTRLCLK and USB4_2_AUX+ DisplayPort AUX+ or USB4 AUX+ function if DDI2_DDC_AUX_SEL is no connect or TMDS I²C control clock if DDI2_DDC_AUX_SEL is pulled high.	I/O LV_DIFF or I/O OD 3.3 V	PD 100 kΩ (DP mode)	

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Signal	Pin #	Description	I/O	PU/PD	Comment
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX-, HDMI2_CTRLDATA and USB4_2_AUX- DisplayPort AUX- or USB4 AUX- function if DDI2_DDC_AUX_SEL is no connect or TMDS I²C control data if DDI2_DDC_AUX_SEL is pulled high.	I/O LV_DIFF or I/O OD 3.3 V	PU 100 kΩ (DP mode)	
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1 M pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the TMDS CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1 MΩ	
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+ Multiplexed with DP3_LANE0- and TMDS3_DATA2- DDI3 differential pair 0	O LV_DIFF		
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+ Multiplexed with DP3_LANE1- and TMDS3_DATA1- DDI3 differential pair 1	O LV_DIFF		
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+ Multiplexed with DP3_LANE2- and TMDS3_DATA0- DDI3 differential pair 2	O LV_DIFF		
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+ Multiplexed with DP3_LANE3- and TMDS3_CLK- DDI3 differential pair 3	O LV_DIFF		
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD DDI3 hot plug detect	I 3.3 V	PD 100 kΩ	
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK DisplayPort AUX+ function if DDI3_DDC_AUX_SEL is no connect or TMDS I²C control clock if DDI3_DDC_AUX_SEL is pulled high.	I/O LV_DIFF or I/O OD 3.3 V	PD 100 kΩ (DP mode)	
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA DisplayPort AUX- function if DDI3_DDC_AUX_SEL is no connect or TMDS I²C control data if DDI3_DDC_AUX_SEL is pulled high.	I/O LV_DIFF or I/O OD 3.3 V	PU 100 kΩ 3.3 V (DP mode)	
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1 MΩ pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled- high, the AUX pair contains the TMDS CTRLCLK and CTRLDATA signals.	I 3.3 V	PD 1 MΩ	

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Table 24 Embedded DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eDP_TX3+ eDP_TX3- eDP_TX2+ eDP_TX2- eDP_TX1+ eDP_TX1- eDP_TX0+ eDP_TX0-	A81 A82 A71 A72 A73 A74 A75 A76	eDP differential pairs	O LV_DIFF AC coupled off module		
eDP_VDD_EN	A77	eDP power enable	O 3.3 V	PD 100 kΩ	
eDP_BKLT_EN	B79	eDP backlight enable	O 3.3 V	PD 100 kΩ	
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3 V		
eDP_AUX+	A83	eDP AUX+	I/O LV_DIFF AC coupled off module		
eDP_AUX-	A84	eDP AUX-	I/O LV_DIFF AC coupled off module		
eDP_HPD	A87	Detection of hot plug / unplug and notification of the link layer	I 3.3 V	PD 100 kΩ	

Note

1. *The eDP interface is multiplexed with LVDS interface.*
2. *LVDS is supported in the default configuration. eDP support is an assmbly option requiring BOM modification.*
3. *The LVDS/eDP interface does not support both LVDS and eDP signals at the same time.*

Table 25 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		

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Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3 V	PD 100 kΩ	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3 V	PD 100 kΩ	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3 V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control	I/O 3.3 V	PU 1.4 kΩ 3.3 V	PU for LVDS support (default)
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control	I/O 3.3 V	PU 1.4 kΩ 3.3 V	PU for LVDS support (default)

Note

1. *The LVDS interface is multiplexed with eDP interface.*
2. *The BIOS supports LVDS by default.*
3. *The LVDS/eDP interface does not support both LVDS and eDP signals at the same time.*

Table 26 VGA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	CRT_RED / Analog Video RGB-RED	O VGA	PD 150 Ω	Only offered as an assembly option
VGA_GRN	B91	Analog Video RGB-GREEN	O VGA	PD 150 Ω	
VGA_BLU	B92	Analog Video RGB-BLUE	O VGA	PD 150 Ω	
VGA_HSYNC	B93	Analog Video H-Sync	O 3.3 V		
VGA_VSYNC	B94	Analog Video V-Sync	O 3.3 V		
VGA_I2C_CK	B95	Display Data Channel Clock	I 3.3 V	PU 2.2 kΩ	
VGA_I2C_DAT	B96	Display Data Channel Data	I 3.3 V	PU 2.2 kΩ	

Note

VGA support is an assembly option offered by installing a DP to VGA bridge that supports industrial temperatures.

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Table 27 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	SATA channel 0, receive input differential pair	I SATA		Either SATA Ports 0 and 1 are supported by default. PCIe Port 6 can be connected as an assembly option replacing SATA support.
SATA0_TX+ SATA0_TX-	A16 A17	SATA channel 0, transmit output differential pair	O SATA		
SATA1_RX+ SATA1_RX-	B19 B20	SATA channel 1, receive input differential pair	I SATA		
SATA1_TX+ SATA1_TX-	B16 B17	SATA channel 1, transmit output differential pair	O SATA		
SATA2_RX+ SATA2_RX-	A25 A26	SATA channel 2, receive input differential pair	I SATA		Not connected by default Can be connected instead of SATA0 as an assembly option
SATA2_TX+ SATA2_TX-	A22 A23	SATA channel 2, transmit output differential pair	O SATA		
SATA3_RX+ SATA3_RX-	B25 B26	SATA channel 3, receive input differential pair	I SATA		Not connected by default Can be connected instead of SATA1 as an assembly option
SATA3_TX+ SATA3_TX-	B22 B23	SATA channel 3, transmit output differential pair	O SATA		
S_ATA_ACT#	A28	SATA activity indicator, active low	O 3.3 V	PU 10 kΩ	

Note

Optionally, PCIe Port 6 (assembly option) can be connected to the COM connector replacing SATA support.

Table 28 USB 2.0 and 3.2 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O USB		
USB0-	A45	USB Port 0, data - or D-			
USB1+	B46	USB Port 1, data + or D+	I/O USB		
USB1-	B45	USB Port 1, data - or D-			
USB2+	A43	USB Port 2, data + or D+	I/O USB		
USB2-	A42	USB Port 2, data - or D-			
USB3+	B43	USB Port 3, data + or D+	I/O USB		
USB3-	B42	USB Port 3, data - or D-			
USB4+	A40	USB Port 4, data + or D+	I/O USB		
USB4-	A39	USB Port 4, data - or D-			
USB5+	B40	USB Port 5, data + or D+	I/O USB		
USB5-	B39	USB Port 5, data - or D-			

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Signal	Pin #	Description	I/O	PU/PD	Comment
USB6+	A37	USB Port 6, data + or D+	I/O USB		
USB6-	A36	USB Port 6, data - or D-			
USB7+	B37	USB Port 7, data + or D+	I/O USB		
USB7-	B36	USB Port 7, data - or D-			
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I USB_SS		
USB_SSRX0-	C3				
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O USB_SS		
USB_SSTX0-	D3				
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I USB_SS		
USB_SSRX1-	C6				
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O USB_SS		
USB_SSTX1-	D6				
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I USB_SS		Supported by installing a USB hub on USB_ SS[T/R]X1 path. Supported in the deafult configuration. Not supported in optional configurations that do not feature the USB hub.
USB_SSRX2-	C9				
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O USB_SS		
USB_SSTX2-	D9				
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I USB_SS		
USB_SSRX3-	C12				
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O USB_SS		
USB_SSTX3-	D12				
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line is on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
USB0_HOST_ PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high values indicates that a host is present.	I 3.3 VSB	PD 47 kΩ	Not Connected
RSMRST_OUT#	A48	USB devices that are to be powered in the S5 / S4 / S0i3 suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the high state.	O 3.3 VSB	PD 10 kΩ	

Note

Signals USB_SS[T/R]X[2:3] are not supported in optional configurations that do not contain a USB hub, limiting the no. of supported USB ports.

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Table 29 USB4 Support Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB4_1_SSTX0+	D26	High speed USB4 port 1, data transmit pairs 0 The pins are shared with DDI1_PAIR0+ and DDI1_PAIR0-	USB_SS		
USB4_1_SSTX0-	D27				
USB4_1_SSRX0+	D29	High speed USB4 port 1, data receive pairs 0 The pins are shared with DDI1_PAIR1+ and DDI1_PAIR1- For 4-lane DP Alternate Mode, these RX lines are repurposed as DP TX lines per the USB4 specification	USB_SS		
USB4_1_SSRX0-	D30				
USB4_1_SSTX1+	D32	High speed USB4 port 1, data transmit pairs 1 The pins are shared with DDI1_PAIR2+ and DDI1_PAIR2-	USB_SS		
USB4_1_SSTX1-	D33				
USB4_1_SSRX1+	D36	High speed USB4 port 1 data receive pairs 1 The pins are shared with DDI1_PAIR3+ and DDI1_PAIR3- For 4-lane DP Alternate Mode, these RX lines are repurposed as DP TX lines per the USB4 specification	USB_SS		
USB4_1_SSRX1-	D37				
USB4_1_LSTX	C15	Sideband TX interface for USB4 port 1 alternate mode "Low Speed" asynchronous serial TX line	O 3.3 V		
USB4_1_LSRX	C16	Sideband RX interface for USB4 port 1 alternate mode "Low Speed" asynchronous serial RX line	I 3.3 V		
USB4_1_AUX+	D15	DisplayPort Aux channel for USB4 port 1 DP mode Pins are shared with DDI_ CTRLCLK_AUX+ and DDI_CTRLDATA_AUX-	Bi-Dir LV_DIFF	PD 100 kΩ	
USB4_1_AUX-	D16			PU 100 kΩ 3.3VSB	
USB4_2_SSTX0+	D39	High speed USB4 port 2, data transmit pairs 0. The pins are shared with DDI2_PAIR0+ and DDI2_PAIR0-.	USB_SS		
USB4_2_SSTX0-	D40				
USB4_2_SSRX0+	D42	High speed USB4 port 2, data receive pairs 0. The pins are shared with DDI2_PAIR1+ and DDI2_PAIR1-. For 4-lane DP Alternate Mode, these RX lines are repurposed as DP TX lines per the USB4 specification.	USB_SS		
USB4_2_SSRX0-	D43				
USB4_2_SSTX1+	D46	High speed USB4 port 2, data transmit pairs 1. The pins are shared with DDI2_PAIR2+ and DDI2_PAIR2-.	USB_SS		
USB4_2_SSTX1-	D47				
USB4_2_SSRX1+	D49	High speed USB4 port 2, data receive pairs 1. The pins are shared with DDI2_PAIR3+ and DDI2_PAIR3-.	USB_SS		
USB4_2_SSRX1-	D50				
USB4_2_LSTX	C35	Sideband TX interface for USB4 port 2 alternate mode "Low Speed" asynchronous serial TX line	O 3.3 V		
USB4_2_LSRX	D35	Sideband RX interface for USB4 port 2 alternate mode "Low Speed" asynchronous serial RX line	I 3.3 V		

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USB4_2_AUX+	C32	DisplayPort Aux channel for USB4 port 2 DP mode. The pins are shared with DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-.	Bi-Dir LV_DIFF		
USB4_2_AUX-	C33				
SML0_CLK	C25	Clock lines for System Management Links 0. The pin is shared with DDI1_PAIR4+. SML0 is used to support carrier USB4 re-timers	Bi-Dir OD 3.3 VSB	PU 768 Ω 3.3 VSB	
SML0_DAT	C26	Data line for I²C data based System Management Links between chipset masters and carrier. The pin is shared with DDI1_PAIR4-. SML0 is used to control the carrier based USB re-timers.	Bi-Dir OD 3.3 VSB	PU 768 Ω 3.3 VSB	
SML1_CLK	C27	Clock lines for System Management Links 1. SML1 is used to support carrier USB Power Delivery (PD) controller	Bi-Dir OD 3.3 VSB	PU 768 Ω 3.3 VSB	
SML1_DAT	C28	Data line for I²C data based System Management Links between chipset masters and carrier. SML1 controls the carrier based USB Power Delivery controller.	Bi-Dir OD 3.3 VSB	PU 768 Ω 3.3 VSB	
USB4_PD_I2C_CLK	C29	I²C clock line between module based Embedded Controller master and carrier based USB Power Delivery Controller slave. The pin is shared with DDI1_PAIR5+.	Bi-Dir OD 3.3 V	PU 2.2 kΩ 3.3 VSB	
USB4_PD_I2C_DAT	C30	I²C data line between module based Embedded Controller master and carrier based USB Power Delivery Controller slave. The pin is shared with DDI1_PAIR5-.	Bi-Dir OD 3.3 VSB	PU 2.2 kΩ 3.3 VSB	
USB4_RT_ENA	C17	Power Enable for carrier based USB Retimers. Sourced from chipset GPO "USB Re-Timer Enable"	O 3.3 V		
USB4_PD_I2C_ ALERT#	D17	Active low alert signal from USB Power Delivery controller to the module Embedded Controller	I 3.3 VSB		
PMCALERT#	D18	Active low alert signal associated with the SML1 System Management link, from the carrier based USB Power Delivery controller	I 3.3 VSB	PU 100 kΩ 3.3 VSB	Pulling low can prevent startup

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Table 30 NBASE-T Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10 Mb/s modes or in 2.5 Gbps modes. Some pairs are unused in some modes according to the following:	I/O Analog		

	1000BASE-T 2.5GBASE-T	100BASE-TX	10BASE-T
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
MDI[2]+/-	B1_DC+/-		
MDI[3]+/-	B1_DD+/-		

GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low	OD 3.3 VSB		
GBE0_LINK# [1, 2]	A8	Gigabit Ethernet Controller 0 link indicator, active low	OD 3.3 VSB		
GBE0_LINK_MID#	A4	Gigabit Ethernet Controller MID Speed Link indicator, active low (GBE0_LINK100# in COM Express Rev. 3.0). If active, the link is established but at a speed lower than the maximum speed supported by the Ethernet controller. Based on capabilities of the Ethernet controller used, this signal might not be active for all possible lower link speeds.	OD 3.3 VSB		
GBE0_LINK_MAX#	A5	Gigabit Ethernet Controller MAX Speed Link Indicator, active low (GBE0_LINK1000# in COM Express Rev 3.0). If active, the link is established at the maximum link speed supported by the controller	OD 3.3 VSB		
GBE0_CTREF	A14	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0 V and as high as 3.3 V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.	REF		
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1 pps signal.	I/O 3.3 VSB	PD 10 kΩ	Signal is provided by the Intel i226 controller

Note

1. *The GBE0_LINK# output is not active during a 10 Mb and 100 Mb connection. It is only active during a 1 Gb or 2.5 Gb connection. This is a limitation of Ethernet controller since it has only three LED outputs.*
2. *The GBE0_LINK# signal is a logic AND of the GBE0_LINK_MID# and GBE0_LINK_MAX# signals on the conga-TC1000r module.*
3. *Optionally, PCIe Port 7 (assembly option) can be connected to the COM connectior instead of the NBASE-T Ethernet interface.*
4. *Optionally, the Ethernet controller can be connected to the PCIe Port 5, making PCIe 7 available on the COM connector (assembly option).*

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Table 31 High Definition Audio Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST#	A30	Reset output to codec; active low	O 3.3 V		
HDA_SYNC	A29	Sample-synchronization signal to the codec(s)	O 3.3 V		
HDA_BITCLK	A32	Serial data clock generated by the external codec(s)	O 3.3 V		
HDA_SDOUT	A33	Serial TDM data output to the codec	O 3.3 V		
HDA_SDIN0	B30	Serial TDM data input from codec 0	I/O 3.3 V		
HDA_SDIN1/ SNDW0_DAT [1]	B29	Serial TDM data input from codec 1	I/O 3.3 V		Default
		Alternative use as Soundwire bi-directional data line	I/O 1.8 V		Not connected
HDA_SDIN2/ SNDW0_CLK [1]	B28	Serial TDM data input from codec 2	I/O 3.3 V		Not connected
		Alternative use as Soundwire bi-directional clock line	I/O 1.8 V		Assembly option

Note

1. *Optionally, SoundWire (assembly option) can be connected instead of the HDA interface (default).*

Table 32 LPC/eSPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD0/ ESPI_IO_0	B4	LPC Mode: LPC multiplexed address, command and data bus ESPI Mode: eSPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves. Multiplexed with LPC_AD[0:3]	I/O 3.3 V / I/O 1.8 V	PU 20 kΩ 3.3 V	No PUs in eSPI mode
LPC_AD1/ ESPI_IO_1	B5			PU 20 kΩ 3.3 V	
LPC_AD2/ ESPI_IO_2	B6			PU 20 kΩ 3.3 V	
LPC_AD3// ESPI_IO_3	B7			PU 20 kΩ 3.3 V	
LPC_FRAME#/ ESPI_CS0#	B3	LPC Mode: LPC Frame indicates the start of a LPC cycle ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select0#. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin.	O 3.3 V / O 1.8 VSB		
LPC_CLK/ ESPI_CK	B10	LPC Mode: LPC clock output ESPI Mode: eSPI Master Clock Output This pin provides the reference timing for all the serial input and output operations.	O 3.3 V / O 1.8 VSB		24MHz
LPC_DRQ0#/ ESPI_ALERT0#	B8	LPC Mode: LPC serial DMA request ESPI Mode: eSPI pins used by eSPI slave to request service from the eSPI master.	I 3.3 V / O 1.8 VSB	PU 100 kΩ 3.3 V / PU 10 kΩ 1.8 VSB for ESPI	LPC option: 10k PU to 3.3V but are not connected/functional eSPI option: 10k PU to 1.8VSB
LPC_DRQ1#/ ESPI_ALERT1#	B9				

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Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_SERIRQ/ ESPI_CS1#	A50	LPC Mode: LPC serial interrupt ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select# A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin.	I/O 3.3 V / 1.8 VSB	PU 8.2 kΩ 3.3 V / No PU/PD	No PU/PD for eSPI mode
SUS_STAT#/ ESPI_RESET#	B18	LPC Mode: Indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state. ESPI Mode: eSPI Reset Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves.	O 3.3 V / O 1.8 V	PD 10 kΩ	
ESPI_EN#	B47	This signal is used by the carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The carrier should only float this line or pull it low.	I		

Note

1. *The conga-TC1000r does not support LPC_DRQ.*

2. *eSPI is not connected by default. Optionally, eSPI can be connected instead of LPC (Assembly option).*

Table 33 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for carrier board SPI BIOS flash	O 1.8 VSB	PU 10 kΩ 1.8 VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash	I 1.8 VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash	O 1.8 VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash	O 1.8 VSB	PU 4.7 kΩ 1.8 VSB	
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	O 1.8 VSB	PD 100 kΩ	Maximum 100 mA
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. Refer to table 4.15 of the COM Express Module Base Specification 3.1 for strapping options of BIOS disable signals.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	

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Table 34 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C Bus bidirectional clock line.	I/O OD 3.3 VSB	PU 2.2 kΩ 3.3 VSB	
I2C_DAT	B34	General purpose I²C Bus bidirectional data line.	I/O 3.3 V	PU 2.2 kΩ 3.3 VSB	
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3 V	PD 10 kΩ	
WDT	B27	Output indicating that a watchdog time-out event has occurred	O 3.3 V	PD 10 kΩ	
FAN_PWMOUT [1,2]	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O 3.3 V		
FAN_TACHIN [1]	B102	Fan tachometer input	I OD	PU 47.5 kΩ 3.3 V	Requires a fan with a two pulse output Pulse can be set in BIOS
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3 V	PD 10 kΩ	Not connected

Note

1. *Pins are protected on the module by a series schotty diode.*
2. *Pull-down resistor is required on the carrier board for proper logic level.*

Table 35 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins	O 3.3 V	PD 100 kΩ	
GPO1	B54		O 3.3 V	PD 100 kΩ	
GPO2	B57		O 3.3 V	PD 100 kΩ	
GPO3	B63		O 3.3 V	PD 100 kΩ	
GPI0	A54	General purpose input pins (bidirectional signal). Pulled high internally on the module.	I 3.3 V	PU 100 kΩ 3.3 V	
GPI1	A63		I 3.3 V	PU 100 kΩ 3.3 V	
GPI2	A67		I 3.3 V	PU 100 kΩ 3.3 V	
GPI3	A85		I 3.3 V	PU 100 kΩ 3.3 V	

Note

The conga-TC1000r does not support SDIO.

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Table 36 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge Note: For proper detection, assert a pulse width of at least 16 ms	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3 VSB	PD 10 kΩ	
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices	O 3.3 VSB	PD 10 kΩ	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3 VSB	PD 100 kΩ	
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output	O 3.3 VSB	PD 100 kΩ	
SUS_S5#	A24	Indicates system is in Soft Off state	O 3.3 VSB	PD 100 kΩ	
WAKE0#	B66	PCI Express wake up signal	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Assertion will prevent wake from S3-S5 state
LID# [1]	A103	Lid switch. Used by the ACPI operating system for a LID switch. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3 VSB	PU 47 kΩ 3.3 VSB	
SLEEP# [1]	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3 VSB	PU 47 kΩ 3.3 VSB	

Note

1. *Pins are protected on the module by a series schotty diode.*

Table 37 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_ SHUTDOWN	C67	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs.	I 3.3 V or 5 V	PD 100 kΩ	Not connected

Note

The conga-TC1000r does not support Rapid Shutdown.

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Table 38 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation	I 3.3 V	PU 10 kΩ 3.3 V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown	O 3.3 V	PU 10 kΩ 3.3 V	

Table 39 SMBus Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line.	I/O OD 3.3 VSB	PU 3.9 kΩ 3.3 VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line.	I/O OD 3.3 VSB	PU 3.9 kΩ 3.3 VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	

Table 40 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX [1, 2]	A98	General purpose serial port transmitter	O 3.3 V		
SER1_TX [1, 2]	A101	General purpose serial port transmitter	O 3.3 V		
SER0_RX [1]	A99	General purpose serial port receiver	I 3.3 V	PU 10 kΩ 3.3 V	
SER1_RX [1]	A102	General purpose serial port receiver	I 3.3 V	PU 10 kΩ 3.3 V	

Note

1. *Pins are protected on the module by a clamping circuit.*
2. *Pull-down resistor is required on the carrier board for proper logic level.*

Table 41 General Purpose SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GP_SPI_CS#	C45	Chip select from module's SPI master to carrier's SPI slave	O 3.3 VSB		
GP_SPI_MISO	B98	Serial data into module SPI master from the carrier SPI slave ("Master In Slave Out")	I 3.3 VSB		
GP_SPI_MOSI	A86	Serial data from the module SPI master to the carrier SPI slave ("Master Out Slave In")	O 3.3 VSB		
GP_SPI_CK	B99	Clock from the module SPI master to carrier SPI slave	O 3.3 VSB		

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Table 42 Module Type Definition Signal Description

<table>
<tr><th>Signal</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>TYPE0#
TYPE1#
TYPE2#</td><td>C54
C57
D57</td><td>The TYPE pins indicate to the carrier board the pinout type that is implemented on the module.

The pins are tied on the module to either ground (GND) or are no-connects (NC). For pinout Type 1, these pins are don’t care (X).

<table>
<tr><th>TYPE2#</th><th>TYPE1#</th><th>TYPE0#</th><th></th></tr>
<tr><td>X
NC
NC
NC
NC
GND</td><td>X
NC
NC
GND
GND
NC</td><td>X
NC
GND
NC
GND
NC</td><td>Pinout Type 1
Pinout Type 2
Pinout Type 3 (no IDE)
Pinout Type 4 (no PCI)
Pinout Type 5 (no IDE, no PCI)
Pinout Type 6 (no IDE, no PCI)</td></tr>
</table>
The carrier board should implement combinatorial logic that monitors the module ‘TYPE’ pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected.

The carrier board logic may also implement a fault indicator such as an LED.</td><td>PDS</td><td>TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard.

The conga-TC1000r is based on the COM Express Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.</td></tr>
<tr><td>TYPE10#</td><td>A97</td><td>Dual use pin.
Indicates to the carrier board that a Type 10 module is installed.
Indicates to the carrier that a Rev. 1.0/2.0 module is installed.

<table>
<tr><th>TYPE10#</th><th></th></tr>
<tr><td>NC
PD
12V</td><td>Pinout R2.0
Pinout Type 10 pull down to ground with 4.7k resistor
Pinout R1.0</td></tr>
</table>
This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins.

In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12 V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7 kΩ resistor.</td><td>PDS</td><td>Not connected to indicate “Pinout R2.0”.</td></tr>
</table>

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Table 43 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109 C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110 C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground: DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

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9 System Resources

Information regarding the system resources of conga-TC1000r will be published with the final release of this user guide.

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10 BIOS Setup Description

The BIOS setup description of the conga-TC1000r can be viewed without having access to the module. A BIOS user guide will be provided in the HMTL format, along with the BIOS release package.

The BIOS user guide contains the BIOS setup description of a particular BIOS revision including default settings. The BIOS user guide is in HTML format and can be viewed using any internet browser. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-TC1000r is identified as CPL6R110, where:

- CPL6 is the project name
- R is the identifier for a BIOS ROM file
- 1 is the feature number
- 10 is the major and minor revision number ('10' for the initial version).

The binary size of conga-TC1000r BIOS is 32 MByte.

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10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-TC1000r features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. The utility has three versions—UEFI shell, Win32 command line, and Linux version. The UEFI shell and Windows tools, along with calling instructions, are included in the conga-TC1000r FlashPackage. For the Linux version, contact your local congatec sales representative.

10.4 Supported Flash Devices

The conga-TC1000r supports the following flash device:

- Winbond W25Q256JWPIQ (32MB)

The flash devices listed above can be used on the carrier board for external BIOS support.

Note

For the latest supported flash devices, refer to https://wiki.congatec.com/wiki/Supported_SPI_Flash_Devices_for_BIOS.

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