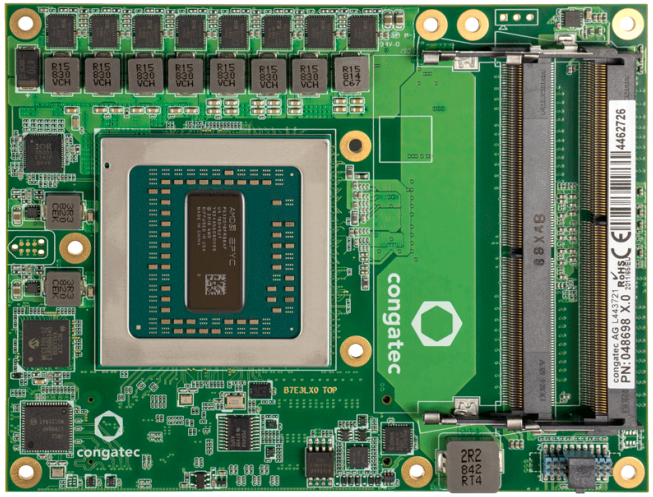


conga-B7E3

COM Express 3.0 Type 7 Basic Module with Next Generation AMD EPYC™ Embedded 3000 Processors

User's Guide

Revision 1.8

congatec

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2020-08-11	AEM	• Preliminary release
1.0	2020-12-08	AEM	• Added power consumption values to tables 6 "Power Consumption Values" and 7 "CMOS Battery Power Consumption" • Added new cooling variants and adapter to section 4 "Cooling Solutions" • Added sections 4.5 "SP4 HSP Dimensions" and 4.6 "SP4 HPA Dimensions" • Indicated in several sections that 10 GbE is not supported in Windows Operating System • Updated section 5.1.3 "Gigabit Ethernet" • Removed Windows 7 and Windows 8 references from section 6.3.4 "OEM BIOS Code/Data" • Added sections 9.3 "I^2C Bus and 9.4 "SM Bus" • Official release
1.1	2021-01-12	AEM	• Deleted the CSA's for the SP4 variant in table 8 "Cooling Solution Variants" • Deleted section 4.4 "SP4 CSA Dimensions"
1.2	2021-08-02	AEM	• Added Software License Information • Changed congatec AG to congatec GmbH • Updated the Power Supply Implementation Guidelines in section 5.1.11 "Power Control" • Updated section 6.4 "congatec Battery Management interface" • Updated section 10.5 "Supported Flash Devices"
1.3	2021-09-23	AEM	• Changed the NVMe feature on SP4 variants to assembly option • Updated the 10 Gb port 2-3 routing for SP4r2 variants in section 3 "Block Diagram"
1.4	2022-03-16	AEM	• Updated section 4 "Block Diagram"
1.5	2022-07-11	AEM	• Added section 1.3 "Supported 10 GbE Configurations"
1.6	2023-11-30	AEM	• Renamed the title of the document • Updated the RoHS statement • Added a note about optimal storage conditions to section 2.7 "Environmental Specifications" • Added note about the storage of congatec cooling solutions to section 4 "Cooling Solutions" • Deleted the defeatured CSAs (PN 048650 and 048651) from table 9 "Cooling Solution Variants" and also deleted section 4.1 "SP4r2 HSP Dimensions" • Reformated section 6 "Additional Features" • Updated section 6.2.3 "Power Loss Control"
1.7	2024-11-08	AEM	• Updated the section "Preface" • Updated the section "Terminology" • Changed humidity to relative humidity in section 2.7 "Environmental Specifications" • Added section 2.8 "Storage Specifications" • Updated section 4.2 "SP4r2 HPA Dimensions" • Added a caution to table 19 "Connector C-D Pinout"
1.8	2025-03-06	RVI	• Added WEEE directive to the preface section • Added a note to the section 2.3 "Mechanical Dimensions" • Added a caution to section 4 "Cooling Solutions"

Preface

This user's guide provides information about the components, features, connectors and system resources available on the conga-B7E3. It is one of three documents that should be referred to when designing a COM Express® application. The other reference documents that should be used include the following:

- COM Express® Module Base Specification
- COM Express® Carrier Design Guide

These documents are available on the PICMG website at **www.picmg.org**. Additionally, check the restricted area of the congatec website at **www.congatec.com** and the website of the respective silicon vendor for relevant documents (Erratum, PCN, Sighting Reports and others).

Software Licenses

Notice Regarding Open Source Software

The congatec products contain Open Source software that has been released by programmers under specific licensing requirements such as the "General Public License" (GPL) Version 2 or 3, the "Lesser General Public License" (LGPL), the "ApacheLicense" or similar licenses.

You can find the specific details at https://www.congatec.com/en/licenses/. Search for the revision of the BIOS/UEFI or Board Controller Software (as shown in the POST screen or BIOS setup) to get the complete product related license information. To the extent that any accompanying material such as instruction manuals, handbooks etc. contain copyright notices, conditions of use or licensing requirements that contradict any applicable Open Source license, these conditions are inapplicable.

The use and distribution of any Open Source software contained in the product is exclusively governed by the respective Open Source license. The Open Source software is provided by its programmers without ANY WARRANTY, whether implied or expressed, of any fitness for a particular purpose, and the programmers DECLINE ALL LIABILITY for damages, direct or indirect, that result from the use of this software.

OEM/ CGUTL BIOS

BIOS/UEFI modified by customer via the congatec System Utility (CGUTL) is subject to the same license as the BIOS/UEFI it is based on. You can find the specific details at https://www.congatec.com/en/licenses/.

Disclaimer

The information contained within this user's guide, including but not limited to any product specification, is subject to change without notice.

congatec GmbH provides no warranty with regard to this user's guide or any other information contained herein and hereby expressly disclaims any implied warranties of merchantability or fitness for any particular purpose with regard to any of the foregoing. congatec GmbH assumes no liability for any damages incurred directly or indirectly from any technical or typographical errors or omissions contained herein or for discrepancies between the product and the user's guide. In no event shall congatec GmbH be liable for any incidental, consequential, special, or exemplary damages, whether based on tort, contract or otherwise, arising out of or in connection with this user's guide or any other information contained herein or the use thereof.

Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

WEEE Directive

To comply with Directive 2012/19/EU on Waste Electrical and Electronic Equipment (WEEE), ensure that this product is disposed of correctly at the end of its lifecycle. Customers are required to take electrical and electronic equipment to designated collection facilities separate from unsorted municipal waste, following applicable regional laws.

Proper disposal through designated collection points allows for the recycling, recovery, and reuse of valuable materials, supporting a more efficient use of resources and reducing environmental impact.

Note

Standalone congatec components, such as modules, carrier boards, and cooling solutions are designed to function only within other products. WEEE registration for the complete product must be completed by the entity placing the final product on the market.

Electrostatic Sensitive Device

All congatec GmbH products are electrostatic sensitive devices. They are enclosed in static shielding bags, and shipped enclosed in secondary packaging (protective packaging). The secondary packaging does not provide electrostatic protection.

Do not remove the device from the static shielding bag or handle it, except at an electrostatic-free workstation. Also, do not ship or store electronic devices near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original packaging. Be aware that failure to comply with these guidelines will void the congatec GmbH Limited Warranty.

RoHS Directive

All congatec GmbH designs comply with EU RoHS Directive 2011/65/EU and Delegated Directive 2015/863.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Copyright Notice

congatec GmbH has made every attempt to ensure that the information in this document is accurate yet the information contained within is supplied "as-is".

Trademarks

Product names, logos, brands, and other trademarks featured or referred to within this user's guide, or the congatec website, are the property of their respective trademark holders. These trademark holders are not affiliated with congatec GmbH, our products, or our website.

Warranty

congatec GmbH makes no representation, warranty or guaranty, express or implied regarding the products except its standard form of limited warranty ("Limited Warranty") per the terms and conditions of the congatec entity, which the product is delivered from. These terms and conditions can be downloaded from www.congatec.com. congatec GmbH may in its sole discretion modify its Limited Warranty at any time and from time to time.

The products may include software. Use of the software is subject to the terms and conditions set out in the respective owner's license agreements, which are available at www.congatec.com and/or upon request.

Beginning on the date of shipment to its direct customer and continuing for the published warranty period, congatec GmbH represents that the products are new and warrants that each product failing to function properly under normal use, due to a defect in materials or workmanship or due to non conformance to the agreed upon specifications, will be repaired or exchanged, at congatec's option and expense.

Customer will obtain a Return Material Authorization ("RMA") number from congatec GmbH prior to returning the non conforming product freight prepaid. congatec GmbH will pay for transporting the repaired or exchanged product to the customer.

Repaired, replaced or exchanged product will be warranted for the repair warranty period in effect as of the date the repaired, exchanged or replaced product is shipped by congatec, or the remainder of the original warranty, whichever is longer. This Limited Warranty extends to congatec's direct customer only and is not assignable or transferable.

Except as set forth in writing in the Limited Warranty, congatec makes no performance representations, warranties, or guarantees, either express or implied, oral or written, with respect to the products, including without limitation any implied warranty (a) of merchantability, (b) of fitness for a particular purpose, or (c) arising from course of performance, course of dealing, or usage of trade.

congatec GmbH shall in no event be liable to the end user for collateral or consequential damages of any kind. congatec shall not otherwise be liable for loss, damage or expense directly or indirectly arising from the use of the product or from any other cause. The sole and exclusive remedy against congatec, whether a claim sound in contract, warranty, tort or any other legal theory, shall be repair or replacement of the product only.

Certification

congatec GmbH is certified to DIN EN ISO 9001 standard.

Technical Support

congatec GmbH technicians and engineers are committed to providing the best possible technical support for our customers so that our products can be easily used and implemented. We request that you first visit our website at www.congatec.com for the latest documentation, utilities and drivers, which have been made available to assist you. If you still require assistance after visiting our website then contact our technical support department by email at support@congatec.com

Terminology

Term	Description
CSA	Active Cooling Solution
CSP	Passive Cooling Solution
10GBASE	10 Gbit Ethernet
2500BASE	2.5 Gbit Ethernet
BMC	Baseboard Management Controller
GB	Gigabyte
GHz	Gigahertz
Gbps	Gigabit per second
HSP	Heatspreader
kB	Kilobyte
KR	GBASE-KR Ethernet Interface
KX	GBASE-KX Ethernet Interface
MB	Megabyte
Mbit	Megabit
Mbps	Megabit per second
MHz	Megahertz
MT/s	Megatransfer per second
N.C	Not connected
N.A	Not available
PEG	PCI Express Graphics
PCH	Platform Controller Hub
PCIe	PCI Express
SATA	Serial ATA
SM	System Management
TBD	To be determined
TDP	Thermal Design Power

Contents

List of Tables

1 Introduction

1.1 COM Express Concept

COM Express is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express modules are available in following form factors:

- Mini 84mm x 55mm
- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x 110mm

Table 1 COM Express 3.0 Pinout Types

Types	Connector Rows	PCIe Lanes	PCI	IDE	SATA Ports	LAN ports	USB 2.0/ USB 3.0	Display Interfaces
Type 1	A-B	Up to 6		-	4	1	8 / 0	VGA, LVDS
Type 2	A-B C-D	Up to 22	32 bit	1	4	1	8 / 0	VGA, LVDS, PEG/SDVO
Type 3	A-B C-D	Up to 22	32 bit	-	4	3	8 / 0	VGA,LVDS, PEG/SDVO
Type 4	A-B C-D	Up to 32		1	4	1	8 / 0	VGA,LVDS, PEG/SDVO
Type 5	A-B C-D	Up to 32		-	4	3	8 / 0	VGA,LVDS, PEG/SDVO
Type 6	A-B C-D	Up to 24		-	4	1	8 / 4 [1]	VGA,LVDS/eDP, PEG, 3x DDI
Type 7	A-B C-D	Up to 32		-	2	5 (1x 1 GbE, 4x 10 GbE)	4/ 4 [1]	-
Type 10	A-B	Up to 4		-	2	1	8 / 2	LVDS/eDP, 1xDDI

[1] *The SuperSpeed USB ports (USB 3.0) are not in addition to the USB 2.0 ports. Up to 4 of the USB 2.0 ports can support SuperSpeed USB.*

The conga-B7E3 modules use the Type 7 pinout definition and comply with COM Express 3.0 specification. They are equipped with two high performance connectors that ensure stable data throughput, and support high bandwidth networking.

The COM (computer on module) integrates all the core components of a common PC and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any embedded PC application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 3.0/2.0, and 10 Gigabit Ethernet.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

1.2 Options Information

The conga-B7E3 is currently available in seven variants (six commercial and one industrial). The table below shows the different configurations available.

Table 2 Commercial Variants

Part No.		048600	048602	048605	048606	048607	048608
Processor		AMD EPYC 3451 2.15 GHz 16 Cores	AMD EPYC 3351 1.9 GHz 12 Cores	AMD EPYC 3251 2.5 GHz 8 Cores	AMD EPYC 3201 1.5 GHz 8 Cores	AMD EPYC 3151 2.7 GHz 4 Cores	AMD EPYC 3101 2.1 GHz 4 Cores
BGA Socket		SP4	SP4	SP4r2	SP4r2	SP4r2	SP4r2
Package		Multi-die	Multi-die	Single-die	Single-die	Single-die	Single-die
Boost Frequency	Maximum [1]	3.0 GHz	3.0 GHz	3.1 GHz	3.1 GHz	2.9 GHz	2.9 GHz
	All Cores	2.45 GHz	2.75 GHz				
L3 Cache		32 MB	32 MB	16 MB	16 MB	16 MB	8 MB
Processor Graphics		None	None	None	None	None	None
DDR4 Memory (ECC or Non-ECC)		2666 MT/s triple channel (up to 96 GB)	2666 MT/s triple channel (up to 96 GB)	2666 MT/s dual channel (up to 64 GB)	2133 MT/s dual channel (up to 64 GB)	2666 MT/s dual channel (up to 64 GB)	2666 MT/s dual channel (up to 64 GB)
Gigabit Ethernet	10GBASE-KR [2]	4	4	4	4	4	4
	1 GbE	1	1	1	1	1	1
PCIe Lanes [3,4,5] (Gen 3)		32 lanes	32 lanes	24 lanes	24 lanes	24 lanes	24 lanes
Storage	SATA (6 Gbps)	2	2	2	2	2	2
	Onboard NVMe	Optional (BOM)	Optional (BOM)	N.A	N.A	N.A	N.A
USB Ports		4 ports (4 x USB 3.0)	4 ports (4 x USB 3.0)	4 ports (4 x USB 3.0)	4 ports (4 x USB 3.0)	4 ports (4 x USB 3.0)	4 ports (4 x USB 3.0)
TPM 2.0		Discrete	Discrete	Discrete	Discrete	Discrete	Discrete
Processor TDP (cTDP)		100 W (80 W)	80 W (60 W)	55 W	30 W	45 W	35 W

Note

1. *Maximum frequency by any single core under normal operating conditions*
2. *Not supported in Windows Operating System*
3. *COM Express PCIe lane 4 is shared with the BMC on congatec carrier board.*
4. *Each x16 lane supports a maximum of eight devices.*
5. *Different lane configurations with assembly option (see section 5.1.1 "PCI Express™").*

Table 3 Industrial Variants

Part-No.		048604
Processor		AMD EPYC 3255 2.5 GHz 8 Cores
BGA Socket		SP4r2
Package		Single-die
Boost Frequency	Maximum	3.1 GHz
	All Cores	
L3 Cache		16 MB
Processor Graphics		None
DDR4 Memory (ECC or Non-ECC)		2666 MT/s dual channel (up to 64 GB)
Gigabit Ethernet	10GBASE-KR [1]	4
	1 GbE	1
PCIe Lanes [2,3,4] (Gen 3)		24 lanes
Storage	SATA (6 Gbps)	2
	Onboard NVMe	N.A
USB Ports		4 ports (4 x USB 3.0)
TPM 2.0		Discrete
Processor TDP		55 W (25W)

Note

1. *Not supported in Windows Operating System.*
2. *COM Express PCIe lane 4 is shared with the BMC on congatec carrier board.*
3. *Each x16 lane supports a maximum of eight devices.*
4. *Different lane configurations with assembly option (see section 5.1.1 "PCI Express™").*

1.3 Supported 10 GbE Configurations

The table below lists the 10 GbE configurations the conga-B7E3 supports.

Table 4 Supported 10 GbE configurations

Configurations	conga-B7E3
10GBASE-KR	Supported [1, 2]
Native SFI	Supported [1, 2]
Inphi CS4227 - SFI	Supported [1, 4, 5]
Intel X557 - 10G-BASE-T	Not supported
Marvell 88X3310P - 10G-BASE-T	Supported [1, 2, 3]
Marvell 88E6190 2500BASE-KX	Not supported

Note

1. *Appropriate configuration must be enabled in BIOS setup menu*
2. *Not validated by congatec*
3. *No reference design available*
4. *Validated SFP+ transceiver is the Intel FTLX8571D3BCV-IT-10Gb*
5. *Validated SFP+ DAC cable is the "All best Electronics R-CS-PBB7PBB-DI-1000-G (1m)"*

2 Specifications

2.1 Feature List

Table 5 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 7, rev. 3.0 (basic size 125 x 95 mm)	
Processor	AMD® EPYC™ Embedded 3000 product family	
Memory	Three memory sockets [1] (two stacked on the top side and one on the bottom side). Supports - DDR4 ECC and non-ECC SODIMM modules - Triple channel (channel A, DIMM 0 and channel D, DIMM 2 on the top side; channel B, DIMM 1 on the bottom side) - Data rates up to 2666 MT/s - Maximum 96 GB capacity (32 GB per slot)	
congatec Board Controller	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, hardware monitoring, fan control, I²C bus, power loss control	
Chipset	Integrated in the SoC	
Ethernet	Gigabit Ethernet. Supports up to: - 4 x 10GBASE-KR [2] - 1 x 1 GbE (standard interface)	
Audio	N.A	
Graphics	N.A	
Peripheral Interfaces	4x USB 3.0 ports (supports also USB 2.0) 2x SATA® (6 Gb/s) Up to 32 PCIe Gen. 3 lanes 2x UART GPIOs	LPC (no DMA) I²C (fast mode, 400 KHz, multi-master) SMBus SPI
BIOS	AMI Aptio® V UEFI 2.6 firmware 16 MB serial SPI flash with congatec Embedded BIOS features	
Onboard Storage	Optional NVMe SSD, up to 1 TB capacity (available on only SP4 variants)	
Power Management	Supports: - ACPI Specification Version 5.0 (Errata A) - Hardware power management - System Sleep State Control - S5 Wake events from the AMD Management Engine	
Security	Discrete SPI TPM 2.0 (Infineon SLB9670_VQ2.0) New AES Instructions for faster and better encryption	

Note

1. *For DIMM configuration, see section 7.3 "DIMM Configuration"*
2. *Some designs may require a 10 GbE PHY on the carrier board*

2.2 Supported Operating Systems

The conga-B7E3 supports the following operating systems.

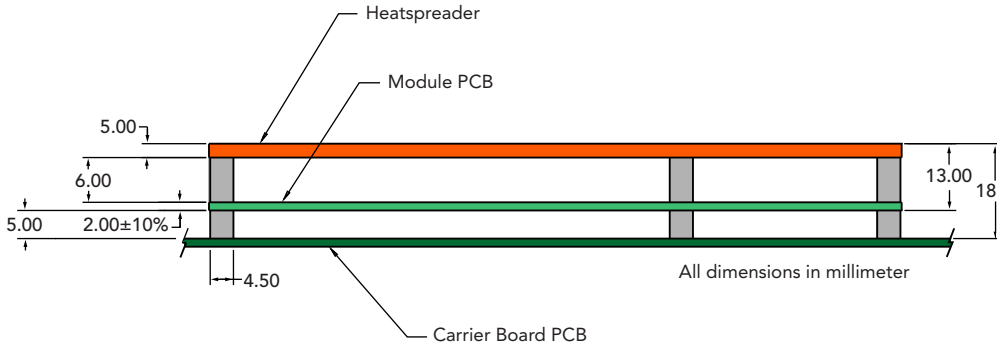
- Microsoft® Windows® 10
- Microsoft® Windows® Server 2019
- Ubuntu
- Yocto Project
- Real Time Systems Hypervisior

Note

For better system performance, use only 64-bit Operating Systems.

2.3 Mechanical Dimensions

- 95.0 mm x 125.0 mm
- Height approximately 18 or 21 mm (including heatspreader) depending on the carrier board connector that is used. If the 5 mm (height) carrier board connector is used, then approximate overall height is 18 mm. If the 8 mm (height) carrier board connector is used, then approximate overall height is 21 mm



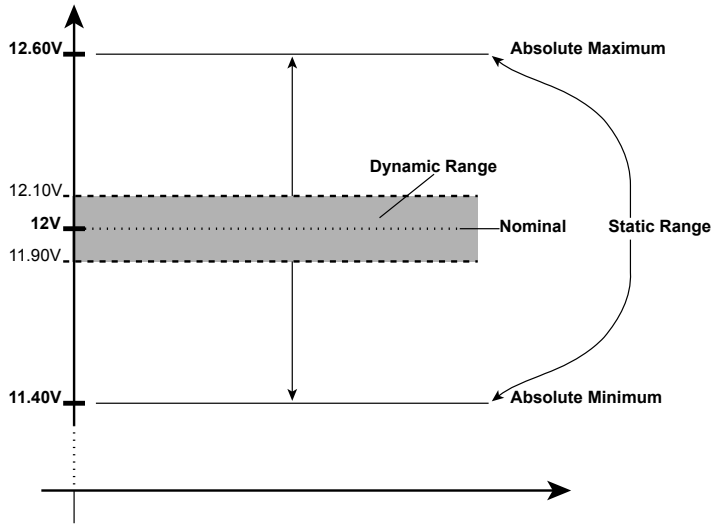
Note

3D models of congatec products are available at www.congatec.com/login. These models indicate the overall length, height and width of each product. If you need login access, contact your local sales representative.

2.4 Supply Voltage Standard Power

- 12 V DC ± 5 %

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 7 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4 - 12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75 - 5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.5 - 3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- Input voltage +12 V
- conga-B7E3 COM
- modified congatec carrier board
- conga-B7E3 cooling solution
- Microsoft Windows Server 2019 (64 bit)

Note

The CPU was stressed to its maximum workload.

Table 6 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S5	COM is powered by VCC_5V_SBY	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Table 7 Power Consumption Values

The table below provides additional information about the conga-B7E3 power consumption. The values are recorded at various operating mode.

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (A)			
					Variant	Cores	Freq. /Boost (GHz)	S0: Min	S0: Max	S0: Peak	S5
048600	3 x 4 GB	Y.2	B7E3R013	Windows 10	AMD® EPYC® C3451	16	2.1 / 3.0	1.46	8.27	8.63	0.15
048602	3 x 4 GB	Y.2	B7E3R013	Windows 10	AMD® EPYC® C3351	12	1.9 / 3.0	1.14	5.93	6.52	0.15
048604	2 x 4 GB	A.1	B7E3R013	Windows 10	AMD® EPYC® C3255	8	2.5 / 3.1	0.92	4.51	4.88	0.15
048605	2 x 4 GB	A.1	B7E3R013	Windows 10	AMD® EPYC® C3251	8	2.5 / 3.1	0.96	4.46	4.59	0.15
048606	2 x 4 GB	A.1	B7E3R013	Windows 10	AMD® EPYC® C3201	8	1.5 / 3.1	0.83	2.62	2.78	0.15
048607	2 x 4 GB	A.1	B7E3R013	Windows 10	AMD® EPYC® C3151	8	2.7 / 2.9	0.93	3.94	4.13	0.15
048608	2 x 4 GB	A.1	B7E3R013	Windows 10	AMD® EPYC® C3101	4	2.1 / 2.9	0.92	2.63	2.69	0.15

2.6 Supply Voltage Battery Power

Table 8 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	2.00 µA
20°C	3V DC	2.11 µA
70°C	3V DC	2.34 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-B7E3.*

2.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to 80°C (commercial variants)
Temperature	Operation: -40° to 85°C	Storage: -40° to 85°C (industrial variants)
Relative Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

1. *The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.*
2. *Humidity specifications are for non-condensing conditions.*

2.8 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

2.8.1 Module

For long-term storage of the conga-B7E3 (more than six months), keep the conga-B7E3 in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

Note

We do not recommend storing the conga-B7E3 for more than five years under these conditions.

2.8.2 Cooling Solution

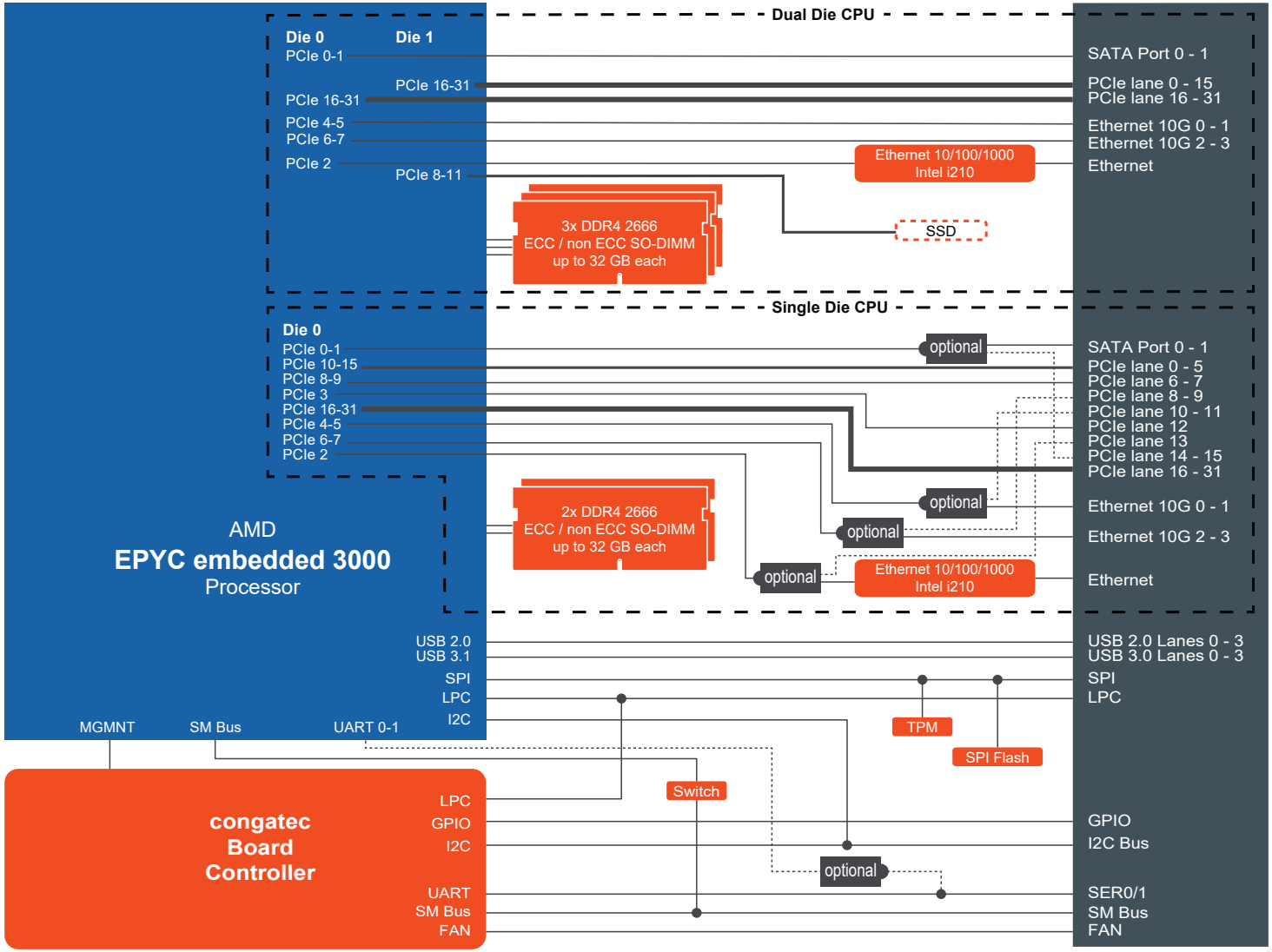
The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. For optimal cooling performance, do not store the heatspreaders/cooling solutions at temperatures below -20°C.

Caution

1. *For temperatures between -10°C and -20°C, preheat the heatpipes before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your sales representative.*
2. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

3 Block Diagram

conga-B7E3 COM Express Rev. 3.0, Basic Size, Type 7 Pinout



4 Cooling Solutions

The conga-B7E3 supports the cooling solutions/adapter listed in the table below. The dimensions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

	Cooling Solution/Adapter	Part No.	SoC Variant	Description
1	HSP	048652	SP4r2	Heatspreader with integrated heat pipes and 2.7 mm bore-hole standoffs
		048653		Heatspreader with integrated heat pipes and M2.5 mm threaded standoffs
2	HPA	048660		Heatpipe adapter with metal bracket base, spring screws and accessory kit
3	HSP	048656	SP4	Heatspreader with integrated heat pipes and 2.7 mm bore-hole standoffs
		048657		Heatspreader with integrated heat pipes and M2.5 mm threaded standoffs
4	HPA	048662		Heatpipe adapter with metal bracket base, spring screws and accessory kit

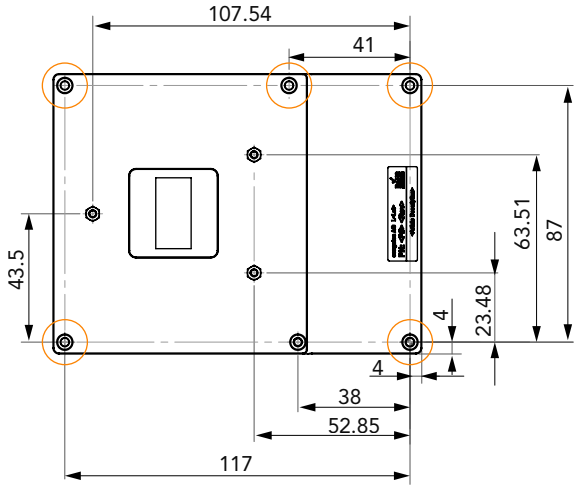
Note

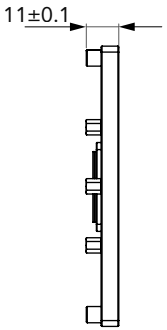
1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

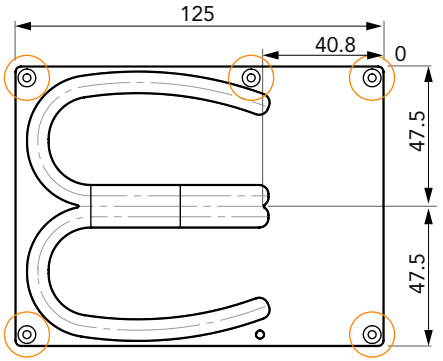
Caution

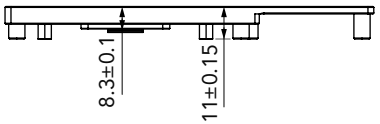
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. If your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. To ensure optimal cooling performance, they should not be stored at temperatures below -20°C. If the storage temperature drops below -10°C, the heatpipes should be pre-heated before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your local sales representative.*
3. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
4. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
5. *Do not exceed the maximum torque specified for the screws. Doing so may damage the module or/and the carrier board.*

4.1 SP4r2 HSP Dimensions

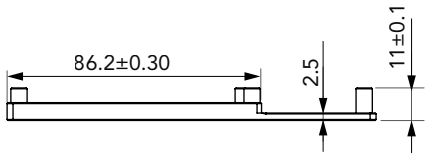


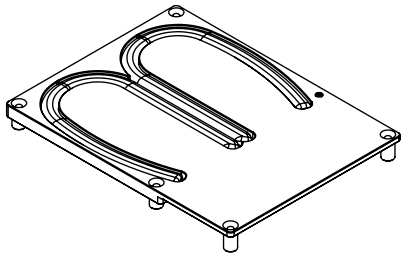


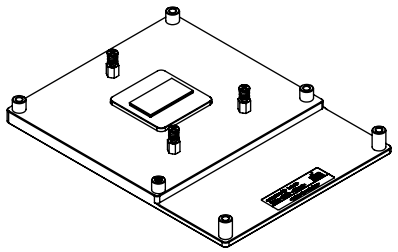




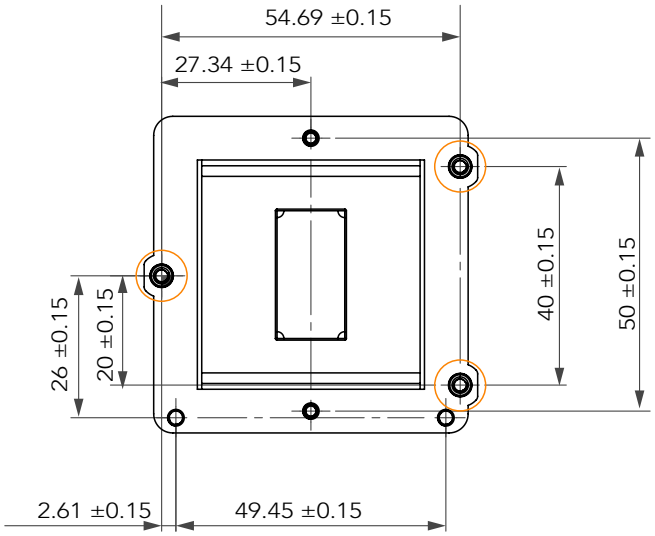
M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version

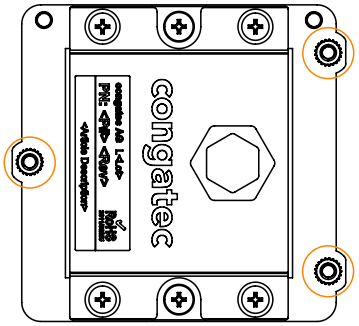


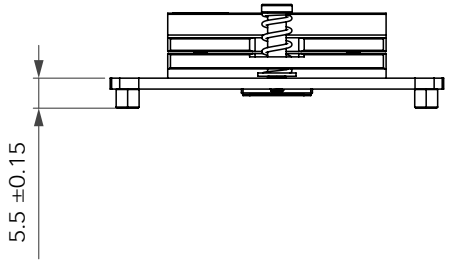




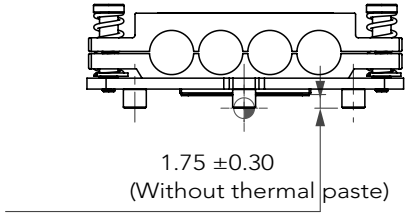
4.2 SP4r2 HPA Dimensions

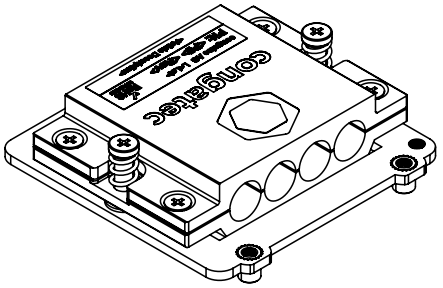


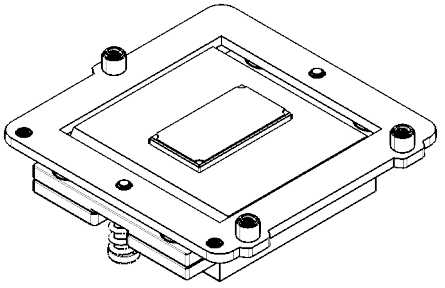




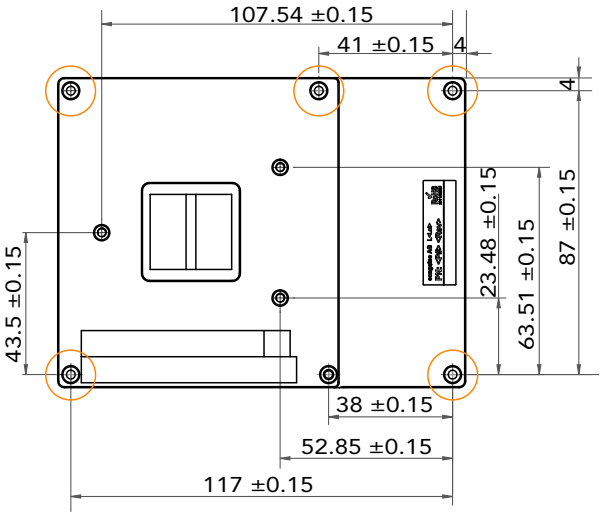
M2.5 x 5.5 mm
threaded standoff

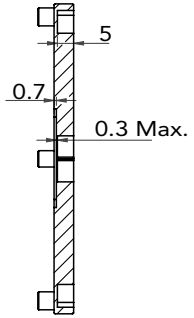


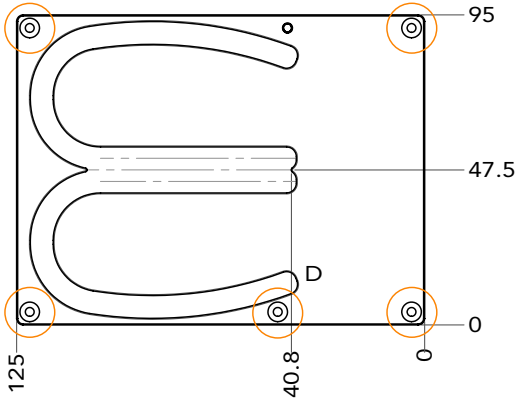


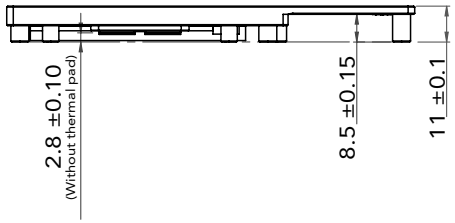


4.3 SP4 HSP Dimensions

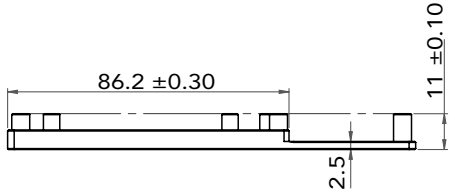


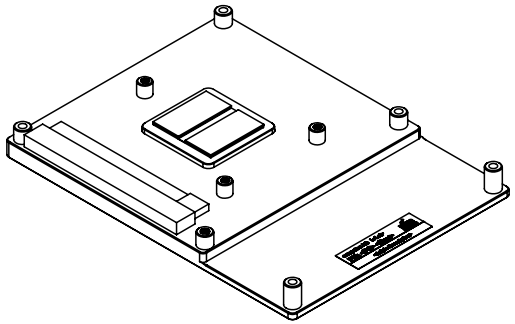


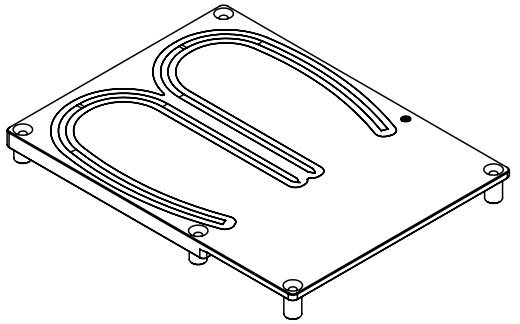




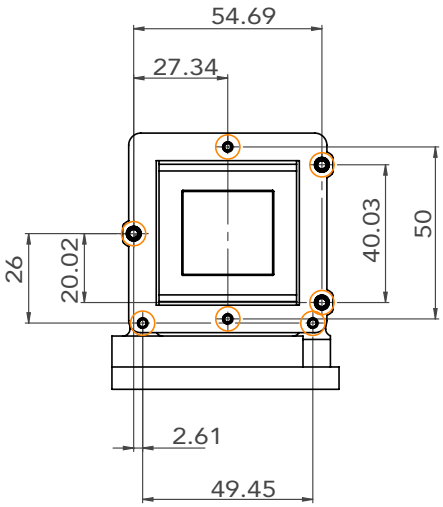
M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version

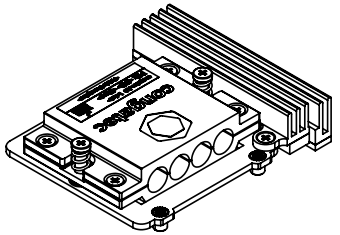


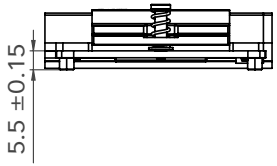




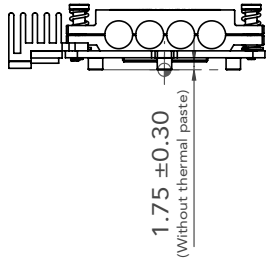
4.4 SP4 HPA Dimensions

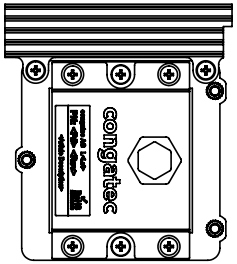


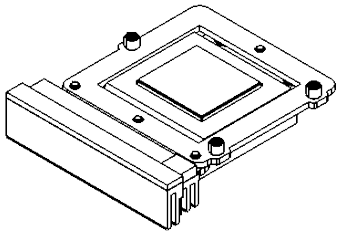




M2.5 threaded screws







5 Connector Rows

The conga-B7E3 is connected to the carrier board via two 220-pin connectors (COM Express Type 7 pinout). These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

5.1 Primary and Secondary Connector Rows

The following subsystems can be found on the primary and secondary connector rows.

Table 10 Supported Interfaces on Rows A-B and C-D

Interfaces	Rows A–B	Rows C–D
SATA	2	-
USB 2.0	4	-
USB 3.0	-	4 [1]
Gigabit Ethernet	1x 1 Gbps	Up to 4 x 10GBASE-KR [2]
PCIe Gen 3	14 lanes [2]	18 lanes [2]
Buses	SPI, LPC, SMB, I²C	-
congatec System Mgmt.	GPIOs, fan control, 2x UARTs	-

Note

1. *Superspeed signals*
2. *Some variants have different configurations. See section 1.2 "Options Information" for more information.*

5.1.1 PCI Express™

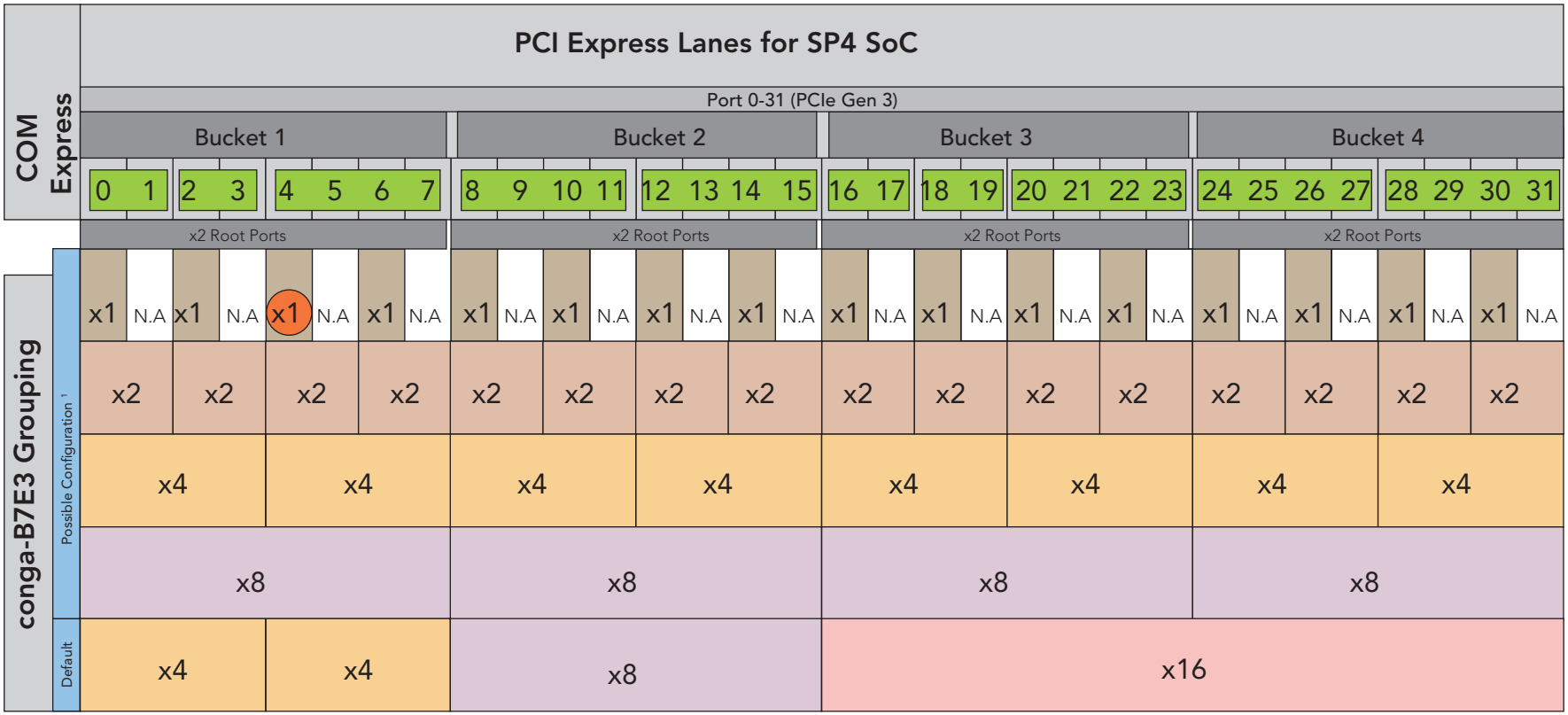
Table 11 PCI Express Features

Rows A–B	Rows C–D
14 PCIe lanes: - PCIe Gen. 3 lanes with up to 8 GTps - x2 root ports - various lane configurations possible [1]	Up to 18 PCIe lanes: - PCIe Gen. 3 lanes with up to 8 GTps - x2 root ports - various lane configurations possible [1]

Note

For the PCIe mapping, see sections 5.1.1.1 "SP4 PCIe Routing" and 5.1.1.2 "SP4r2 PCIe Routing".

5.1.1.1 SP4 PCIe Routing



PHY lane grouping

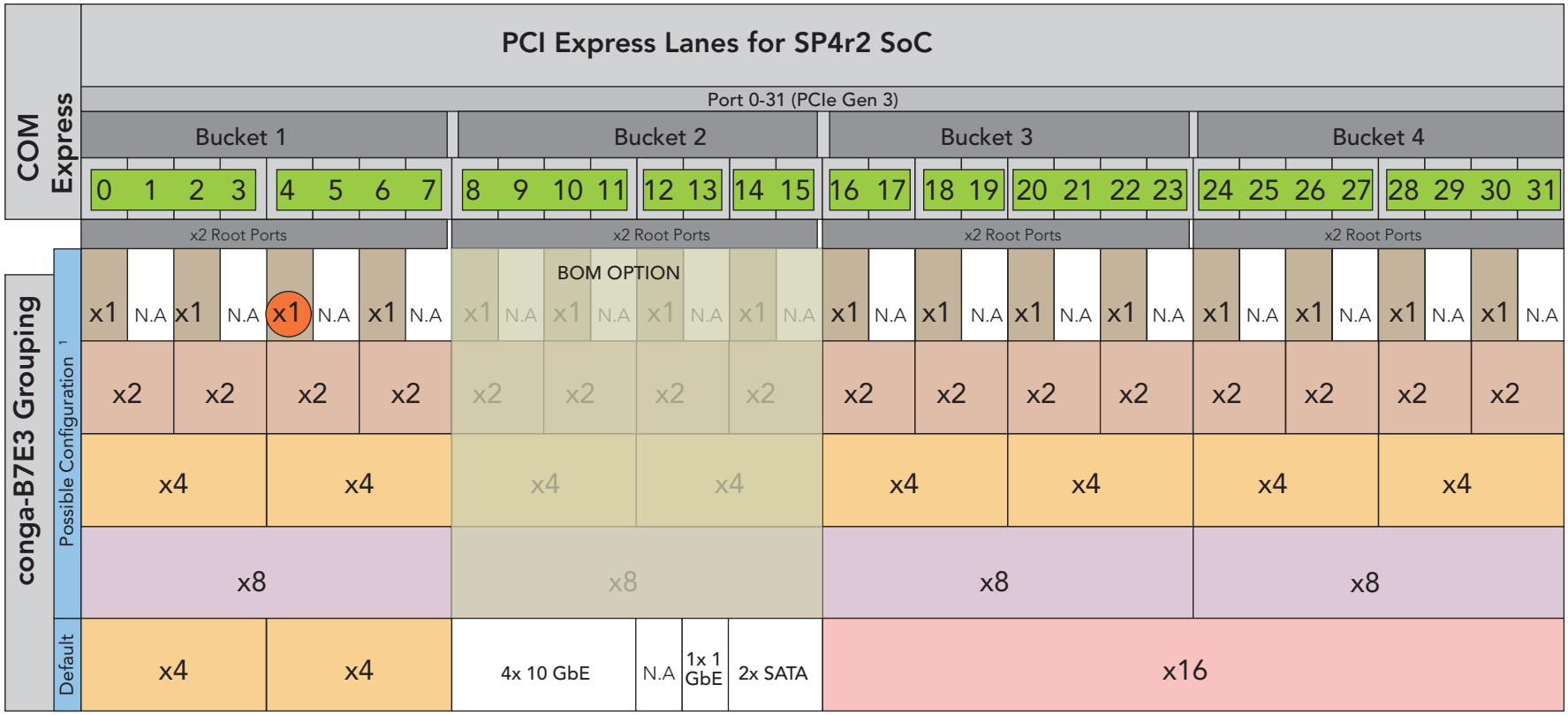
N.A — Not available if the corresponding x1 link is used

congatec carrier board uses lane 4 for BMC VGA

[1] MAPPING INSTRUCTIONS:

- All PHY lane grouping supports only PCIe protocol
- Any grouping of 16 lanes supports maximum of eight separate links
- Any eight lane subset of 16-lane grouping supports maximum of seven links
- All PCIe links subset of 16-lane grouping must be alligned in their natural bit boundaries (Lanes 0-7 and 8-15 for x8 links; lanes 0-3, 4-7, 8-11, 12-15 for x4 links and so on)

5.1.1.2 SP4r2 PCIe Routing



PHY lane grouping

N.A — Not available if the corresponding x1 link is used

congatec carrier board uses lane 4 for BMC VGA

[1] MAPPING INSTRUCTIONS:

- All PHY lane groupings except groupings in bucket 2 support only PCIe protocol
- Any grouping of 16 lanes supports maximum of eight separate links
- Any eight lane subset of 16-lane grouping supports maximum of seven links
- All PCIe links subset of 16-lane grouping must be alligned in their natural bit boundaries (Lanes 0-7 and 8-15 for x8 links; lanes 0-3, 4-7, 8-11, 12-15 for x4 links and so on)

5.1.2 SATA

Table 12 SATA Features

Rows A–B	Rows C–D
Two SATA interfaces with support for - SATA Gen 3 specification with up to 6.0 Gbps transfer rate - independent DMA operation - AHCI mode only	None

5.1.3 Gigabit Ethernet

Table 13 Gigabit Ethernet Features

Rows A–B	Rows C–D
One 1 GbE [1] interface. Supports: - MDI interface - full-duplex operation at 10/100/1000 Mbps - half-duplex operation at 10/100 Mbps - IEEE 802.3x flow control specification - wake on LAN	four 10 GbE [2,3] LAN controllers . Supports: - 10GBASE-KR backplane interfaces - full-duplex operation at all supported speeds

Note

1. *On SP4r2 variants, COM Express PCIe lane 13 is routed to 1 gigabit Ethernet controller by default. PCIe lanes 12 and 13 are not available (requires assembly option) if 1 GbE is supported.*

2. *On SP4r2 variants, COM Express PCIe lanes 8-11 are routed to four 10 GbE controllers by default. PCIe lanes lanes 8-11 are not available (requires assembly option) if four 10 GbE are supported.*

3. *Not supported in Windows Operating System*

5.1.4 USB Interface

Table 14 USB Features

Rows A–B	Rows C–D
Four USB 2.0 ports: - ports 0-3 can be combined with USB SuperSpeed signals to create USB 3.0 ports - supports data transfers up to 480 Mbps - supports USB 1.x and USB 2.0 compliant devices	Four USB 3.0 SuperSpeed Tx/Rx differential signals: - each port requires corresponding USB 2.0 differential pairs - supports data transfers up to 5 Gbps

5.1.5 General Purpose Serial Interface (UART)

Table 15 UART Features

Rows A–B	Rows C–D
Two UART interfaces. Supports: - low, full and high speed modes - programmable baud rates from 2400 bps up to 115200 bps - legacy mode	None

Note

Hardware handshake and flow control are not supported.

5.1.6 LPC Bus

The conga-B7E3 offers the LPC bus through the SoC. The congatec Board Controller is connected to the LPC bus.

Note

The LPC bus supports one DMA device.

5.1.7 I²C

The I²C bus is implemented through the congatec Board Controller, and accessed through the congatec CGOS driver and API. The controller provides a fast-mode multi-master I²C bus that has the maximum bandwidth.

5.1.8 SPI

The conga-B7E3 offers the SPI bus for SPI-compatible flash devices. By integrating an off-module flash device (BIOS) on the carrier board, you can boot the conga-B7E3 from the carrier board. This is especially useful when evaluating a customized BIOS.

The Infineon SLB9670_VQ2.0 TPM 2.0 is also connected to the SPI bus.

5.1.9 SMBus

The conga-B7E3 offers the SMBus for communicating and managing system devices such as thermal sensors, PCIe devices, RAM's serial presence detect.

Note

Make sure the address space of the carrier board SMBus devices does not overlap with the address space of the module devices. For more information, see the COM Express Specification.

5.1.10 GPIOs

The conga-B7E3 offers four General Purpose Input signals and four General Purpose Output signals on the A–B connector for custom system design. These GPIOs are controlled by the cBC

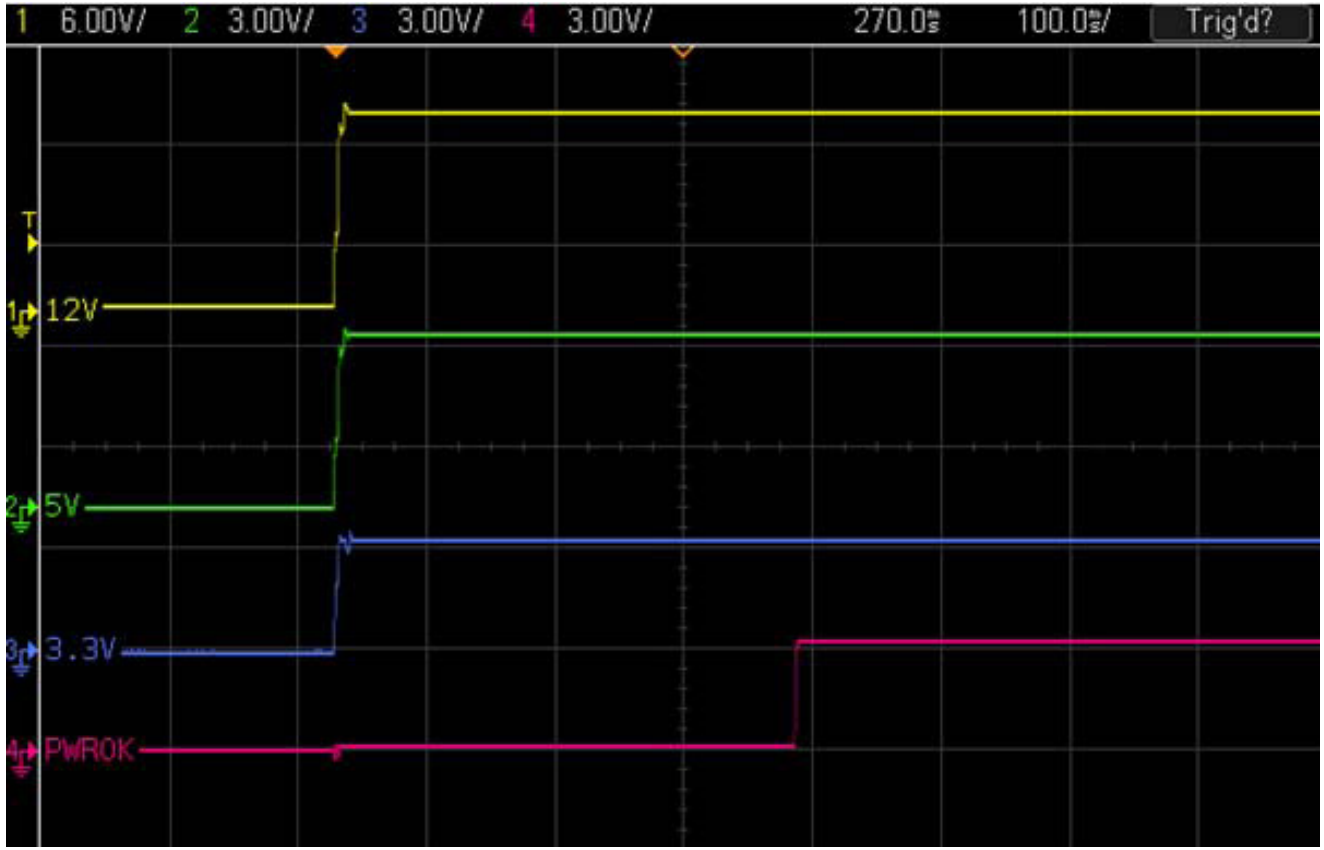
5.1.11 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system.

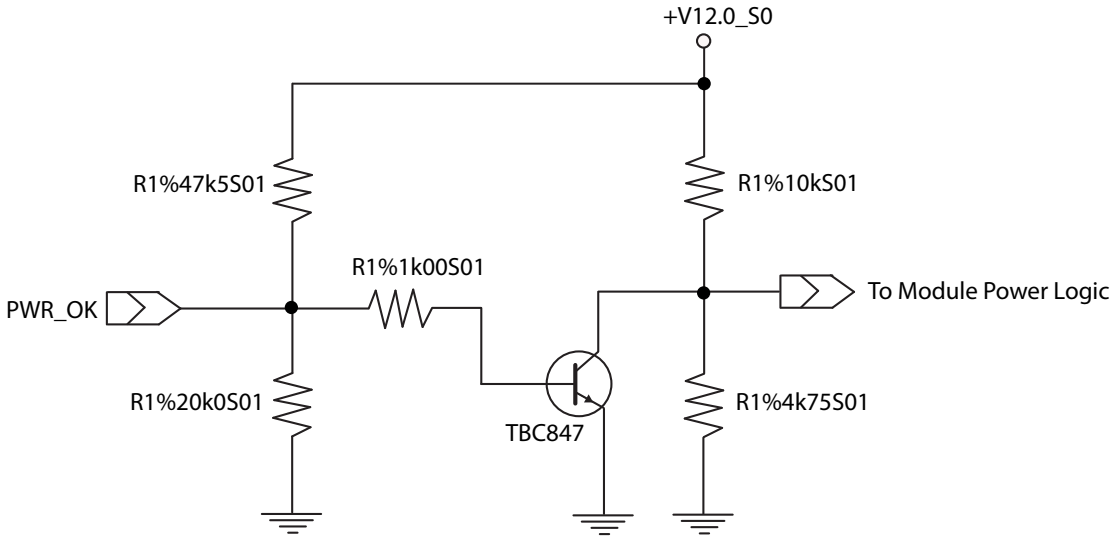
A sample screenshot is shown below:



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The conga-B7E3 PWR_OK input circuitry is implemented as shown below:



The voltage divider ensures the input complies with 3.3 V CMOS characteristic. It also makes it possible to use the module on carrier board designs that do not use the PWR_OK signal. Although the PWR_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

When considering the above shown voltage divider circuitry and the transistor stage, the voltage measured at the PWR_OK input pin may be only around 0.8 V when the 12 V is applied to the module. Actively driving PWR_OK high is compliant to the COM Express specification but this can cause back driving. Therefore, congatec recommends driving the PWR_OK low to keep the module in reset and tri-state PWR_OK when the carrier board hardware is ready to boot.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the "power good" signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1 k resistor to the carrier board 3.3 V power rail.

Note

1. *With this solution, make sure that before the 3.3 V goes up, all carrier board hardware is fully powered and all clocks are stable.*

2. *The conga-B7E3 supports the controlling of ATX-style power supplies. If you do not use an ATX power supply, do not connect the conga-B7E3 pins SUS_S3/PS_ON, 5V_SB and PWRBTN# on the conga-B7E3.*

SUS_S3#

The conga-B7E3 does not support S3 and S4 power states.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

12 V input power is the sole operational power source for the conga-B7E3. Other required voltages are generated internally on the module using onboard voltage regulators.

Note

When designing a power supply for a conga-B7E3 application, be aware that the system may malfunction when a 12 V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.

This problem occurs because some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.

To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope, during the power supply qualication phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com

5.1.12 Power Management

ACPI

The conga-B7E3 supports Advanced Configuration and Power Interface (ACPI) specification, revision 5.0 (Errata A). For more information, see section 7.2 "ACPI Suspend Modes and Resume Events".

6 Additional Features

The following features are available on the conga-B7E3.

6.1 TPM 2.0

The conga-B7E3 offers a discrete SPI TPM 2.0 (Infineon SLB9670VQ2.0) by default. To use the discrete TPM, ensure that the firmware-based TPM is disabled in the BIOS setup menu via the Advanced -> Platform Trust Technology -> fTPM. Save the changes and exit to complete the system configuration changes.

6.2 congatec Board Controller (cBC)

The conga-B7E3 is equipped with Texas Instruments Tiva™ microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features.

Some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture are fully isolated. This isolation results in higher performance and reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The board controller supports the following features:

- Board information
- General Purpose Input/Output (see section 5.1.10 “GPIOs”)
- Watchdog
- I²C bus (see section 5.1.7 “I²C”)
- SMBus (see section 5.1.9 “SMBus”)
- UART (see section 5.1.5 “General Purpose Serial Interface (UART)”)
- Power loss control
- Fan control

6.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.2.2 Watchdog

The conga-B7E3 is equipped with a multi stage watchdog solution that is triggered by software. For more information about the watchdog feature, see the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

Note

The conga-B7E3 module does not support watchdog NMI mode.

6.2.3 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The term "power loss" implies that all power sources, including the standby power are lost (G3 state). Once power loss (transition to G3) or shutdown (transition to S5) occurs, the board controller continuously monitors the standby power rail. If the standby voltage remains stable for 30 seconds, the cBC assumes the system was switched off properly. If the standby voltage is no longer detected within 30 seconds, the module considers this an AC power loss condition.

The power loss control feature has three different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to "ON".*
2. *The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.*
3. *The 30 seconds monitoring cycle applies only to the "Last State" power loss control mode.*

6.2.4 Fan Control

The conga-B7E3 has additional signals and functions to further improve system management. One of these signals is FAN_PWMOUT, an output signal that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, the input signal FAN_TACHOIN provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

1. *A four wire fan must be used to generate the correct speed readout.*

2. *For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express Design Guide.*

6.3 OEM BIOS Customization

The conga-B7E3 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

6.3.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.3.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.3.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.3.4 OEM BIOS Code/Data

With the congatec embedded BIOS, system designers can add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support Windows 10 OEM activation (OA3.0), verb tables for HDA codecs, PCI/PCIe OpROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is called only when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.3.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.4 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addition to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-B7E3 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I^2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface, contact your local congatec sales representative.

6.5 API Support (CGOS)

To benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win64, Linux.

The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available on the congatec website.

6.6 Suspend to Ram

The conga-B7E3 does not support Suspend to RAM feature.

7 conga Tech Notes

The conga-B7E3 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

7.1 AMD®64 Architecture

The AMD64 architecture is a set of x86 architecture extensions that allows the CPU to run 64-bit software required for higher performance applications, while supporting legacy 16-bit and 32-bit applications and operating systems without modification and recompilation. The architecture includes the following features:

- eight additional general-purpose registers (GPRs)
- all GPRs are 64-bit wide
- eight additional YMM/XMM registers
- uniform byte-register addressing for all GPRs
- an instruction prefix accesses the extended registers
- up to 64-bit virtual address
- 64-bit intruction pointer
- instruction pointer relative data-addressing mode
- flat address space

Platforms with AMD® 64 can be run in two ways:

1. **Legacy Mode:** This mode supports 32-bit operating system and 32-bit applications. In this mode no software changes are required, however the benefits of AMD® 64 are not utilized. The legacy mode consists of three submodes—protected mode, virtual-8086 mode and real mode.

2. **Long Mode:** The long mode requires a 64-bit Operating System. It consists of 64-bit mode and compatibility mode (for 32-bit applications).

   – The 64-bit mode provides full support for 64-bit system software and applications. It also requires the recompilation of existing application binaries to 64-bit mode.

   – The compatibility mode allows 64-bit operating systems to run existing 16-bit or 32-bit x86 applications without recompilation.

7.1.1 AMD® Virtualization Technology

AMD® Virtualization Technology (AMD® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system.

Note

congatec supports only RTS Hypervisor. For more information, contact congatec technical support.

7.2 ACPI Suspend Modes and Resume Events

The table below lists the events that wake the system from S5.

Table 16 Wake Events

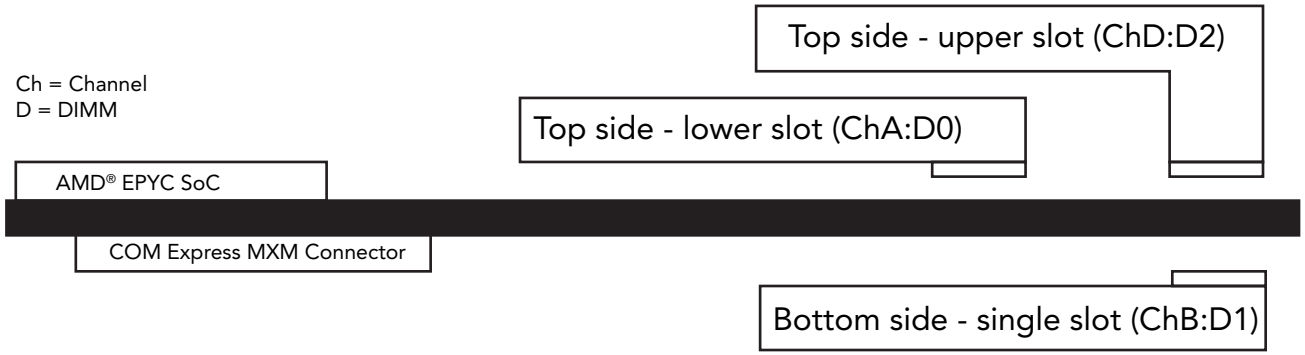
Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S5
Onboard LAN Event	Device driver must be configured for Wake On LAN support
PCI Express WAKE#	Wakes unconditionally from S5
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device or enable 'Resume On PME#' in the Power setup menu
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Wakes unconditionally from S5
Watchdog Power Button Event	Wakes unconditionally from S5

Note

The conga-B7E3 does not support S3 and S4.

7.3 DIMM Configuration

The SoC featured on the conga-B7E3 supports ECC and non-ECC DDR4 memory modules, up to 2666 MT/s. The diagram below shows the location of the memory slots on the conga-B7E3.



8 Signal Descriptions and Pinout Tables

The following section describes the signals found on the conga-B7E3. The pinout of the module complies with COM Express Type 7, rev. 3.0.

The table below describes the terminology used in this section. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors; only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 17 Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
T	Higher voltage tolerance
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant; active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0 and 3.0
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
KR	10GBASE-KR compatible signal
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

8.1 Connector Signal Descriptions

Table 18 Connector A–B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# [1]	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND(FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1# [2]
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF [1]	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	PCIE_TX8+	B71	PCIE_RX8+
A17	SATA0_TX-	B17	SATA1_TX-	A72	PCIE_TX8-	B72	PCIE_RX8-
A18	SUS_S4#	B18	SUS_STAT#	A73	GND	B73	GND
A19	SATA0_RX+	B19	SATA1_RX+	A74	PCIE_TX9+	B74	PCIE_RX9+
A20	SATA0_RX-	B20	SATA1_RX-	A75	PCIE_TX9-	B75	PCIE_RX9-
A21	GND (FIXED)	B21	GND (FIXED)	A76	GND	B76	GND
A22	PCIE_TX15+	B22	PCIE_RX15+	A77	PCIE_TX10+	B77	PCIE_RX10+
A23	PCIE_TX15-	B23	PCIE_RX15-	A78	PCIE_TX10-	B78	PCIE_RX10-
A24	SUS_S5#	B24	PWR_OK	A79	GND	B79	GND
A25	PCIE_TX14+	B25	PCIE_RX14+	A80	GND (FIXED)	B80	GND (FIXED)
A26	PCIE_TX14-	B26	PCIE_RX14-	A81	PCIE_TX11+	B81	PCIE_RX11+
A27	BATLOW#	B27	WDT	A82	PCIE_TX11-	B82	PCIE_RX11-
A28	(S)ATA_ACT#	B28	RSVD [1]	A83	GND	B83	GND
A29	RSVD [1]	B29	RSVD [1]	A84	NCSI_TX_EN	B84	VCC_5V_SBY
A30	RSVD [1]	B30	RSVD [1]	A85	GPI3	B85	VCC_5V_SBY

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD [1]	B86	VCC_5V_SBY
A32	RSVD [1]	B32	SPKR [2]	A87	RSVD [1]	B87	VCC_5V_SBY
A33	RSVD [1]	B33	I2C_CK	A88	PCIE_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0# [2]	B34	I2C_DAT	A89	PCIE_CK_REF-	B89	NCSI_RX_ER [2]
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	PCIE_TX13+	B36	PCIE_RX13+	A91	SPI_POWER	B91	NCSI_CLK_IN
A37	PCIE_TX13-	B37	PCIE_RX13-	A92	SPI_MISO	B92	NCSI_RXD1
A38	GND	B38	GND	A93	GPO0	B93	NCSI_RXD0
A39	PCIE_TX12+	B39	PCIE_RX12+	A94	SPI_CLK	B94	NCSI_CRS_DV
A40	PCIE_TX12-	B40	PCIE_RX12-	A95	SPI_MOSI	B95	NCSI_TXD1
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	NCSI_TXD0
A42	USB2-	B42	USB3-	A97	TYPE10# [1]	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	NCSI_ARB_IN
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	NCSI_ARB_OUT
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI_EN# [1]	A102	SER1_RX	B102	FAN_TACHIN
A48	RSVD [1]	B48	USB0_HOST_PRSNT [2]	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

1. *Not connected*
2. *Not supported*

Table 19 Connector C–D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PCIE_RX17-	D56	PCIE_TX17-
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PCIE_RX18+	D58	PCIE_TX18+
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PCIE_RX18-	D59	PCIE_TX18-
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PCIE_RX19+	D61	PCIE_TX19+
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PCIE_RX19-	D62	PCIE_TX19-
C8	GND	D8	GND	C63	RSVD	D63	RSVD [1]
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	RSVD (see caution below)	D64	RSVD [1]
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	PCIE_RX20+	D65	PCIE_TX20+
C11	GND(FIXED)	D11	GND (FIXED)	C66	PCIE_RX20-	D66	PCIE_TX20-
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RAPID_SHUTDOWN [2]	D67	GND
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	PCIE_RX21+	D68	PCIE_TX21+
C14	GND	D14	GND	C69	PCIE_RX21-	D69	PCIE_TX21-
C15	10G_PHY_MDC_SCL3 [2]	D15	10G_PHY_MDIO_SDA3 [2]	C70	GND (FIXED)	D70	GND (FIXED)
C16	10G_PHY_MDC_SCL2	D16	10G_PHY_MDIO_SDA2	C71	PCIE_RX22+	D71	PCIE_TX22+
C17	10G_SDP2 [2]	D17	10G_SDP3 [2]	C72	PCIE_RX22-	D72	PCIE_TX22-
C18	GND	D18	GND	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	PCIE_RX23+	D74	PCIE_TX23+
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	PCIE_RX23-	D75	PCIE_TX23-
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+	D22	PCIE_TX7+	C77	RSVD	D77	RSVD [1]
C23	PCIE_RX7-	D23	PCIE_TX7-	C78	PCIE_RX24+	D78	PCIE_TX24+
C24	10G_INT2	D24	10G_INT3	C79	PCIE_RX24-	D79	PCIE_TX24-
C25	GND	D25	GND	C80	GND (FIXED)	D80	GND (FIXED)
C26	10G_KR_RX3+	D26	10G_KR_TX3+	C81	PCIE_RX25+	D81	PCIE_TX25+
C27	10G_KR_RX3-	D27	10G_KR_TX3-	C82	PCIE_RX25-	D82	PCIE_TX25-
C28	GND	D28	GND	C83	RSVD	D83	RSVD [1]
C29	10G_KR_RX2+	D29	10G_KR_TX2+	C84	GND	D84	GND
C30	10G_KR_RX2-	D30	10G_KR_TX2-	C85	PCIE_RX26+	D85	PCIE_TX26+
C31	GND (FIXED)	D31	GND (FIXED)	C86	PCIE_RX26-	D86	PCIE_TX26-
C32	10G_SFP_SDA3	D32	10G_SFP_SCL3	C87	GND	D87	GND

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C33	10G_SFP_SDA2	D33	10G_SFP_SCL2	C88	PCIE_RX27+	D88	PCIE_TX27+
C34	10G_PHY_RST_23	D34	10G_PHY_CAP_23 [2]	C89	PCIE_RX27-	D89	PCIE_TX27-
C35	10G_PHY_RST_01	D35	10G_PHY_CAP_01 [2]	C90	GND (FIXED)	D90	GND (FIXED)
C36	10G_LED_SDA [2]	D36	RSVD [1]	C91	PCIE_RX28+	D91	PCIE_TX28+
C37	10G_LED_SCL [2]	D37	RSVD [1]	C92	PCIE_RX28-	D92	PCIE_TX28-
C38	10G_SFP_SDA1	D38	10G_SFP_SCL1	C93	GND	D93	GND
C39	10G_SFP_SDA0	D39	10G_SFP_SCL0	C94	PCIE_RX29+	D94	PCIE_TX29+
C40	10G_SDP0 [2]	D40	10G_SDP1 [2]	C95	PCIE_RX29-	D95	PCIE_TX29-
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	10G_KR_RX1+	D42	10G_KR_TX1+	C97	RSVD	D97	RSVD [1]
C43	10G_KR_RX1-	D43	10G_KR_TX1-	C98	PCIE_RX30+	D98	PCIE_TX30+
C44	GND	D44	GND	C99	PCIE_RX30-	D99	PCIE_TX30-
C45	10G_PHY_MDC_SCL1 [2]	D45	10G_PHY_MDIO_SDA1 [2]	C100	GND (FIXED)	D100	GND (FIXED)
C46	10G_PHY_MDC_SCL0	D46	10G_PHY_MDIO_SDA0	C101	PCIE_RX31+	D101	PCIE_TX31+
C47	10G_INT0	D47	10G_INT1	C102	PCIE_RX31-	D102	PCIE_TX31-
C48	GND	D48	GND	C103	GND	D103	GND
C49	10G_KR_RX0+	D49	10G_KR_TX0+	C104	VCC_12V	D104	VCC_12V
C50	10G_KR_RX0-	D50	10G_KR_TX0-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND(FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PCIE_RX16+	D52	PCIE_TX16+	C107	VCC_12V	D107	VCC_12V
C53	PCIE_RX16-	D53	PCIE_TX16-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	RSVD [1]	C109	VCC_12V	D109	VCC_12V
C55	PCIE_RX17+	D55	PCIE_TX17+	C110	GND (FIXED)	D110	GND (FIXED)

Note

1. *Not connected*
2. *Not supported*

Caution

Using the conga-B7E3 on a COM Express 3.1 carrier board may cause functionality issues. Pin C64 (defined as RSVD in COM Express 3.0) is used for cBC diagnostic output. This pin is defined as GND in COM Express 3.1 specification.

Table 20 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express Transmit Output Differential Pairs 0	O PCIE		
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express Receive Input Differential Pairs 0	I PCIE		
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express Transmit Output Differential Pairs 1	O PCIE		
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express Receive Input Differential Pairs 1	I PCIE		
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express Transmit Output Differential Pairs 2	O PCIE		
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express Receive Input Differential Pairs 2	I PCIE		
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express Transmit Output Differential Pairs 3	O PCIE		
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express Receive Input Differential Pairs 3	I PCIE		
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express Transmit Output Differential Pairs 4	O PCIE		Shared with BMC on congatec carrier board (not available if congatec carrier board BMC is enabled)
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express Receive Input Differential Pairs 4	I PCIE		
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express Transmit Output Differential Pairs 5	O PCIE		Not available if congatec carrier board BMC is enabled
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express Receive Input Differential Pairs 5	I PCIE		
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express Transmit Output Differential Pairs 6	O PCIE		
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express Receive Input Differential Pairs 6	I PCIE		
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express Transmit Output Differential Pairs 7	O PCIE		
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express Receive Input Differential Pairs 7	I PCIE		
PCIE_TX8+ PCIE_TX8-	A71 A72	PCI Express Transmit Output Differential Pairs 8	O PCIE		Supported on SP4 variants by default (BOM option on SP4r2 variants)
PCIE_RX8+ PCIE_RX8-	B71 B72	PCI Express Receive Input Differential Pairs 8	I PCIE		
PCIE_TX9+ PCIE_TX9-	A74 A75	PCI Express Transmit Output Differential Pairs 9	O PCIE		Supported on SP4 variants by default (BOM option on SP4r2 variants)
PCIE_RX9+ PCIE_RX9-	B74 B75	PCI Express Receive Input Differential Pairs 9	I PCIE		

PCIE_TX10+ PCIE_TX10-	A77 A78	PCI Express Transmit Output Differential Pairs 10	O PCIE		Supported on SP4 variants by default (BOM option on SP4r2 variants)
PCIE_RX10+ PCIE_RX10-	B77 B78	PCI Express Receive Input Differential Pairs 10	I PCIE		
PCIE_TX11+ PCIE_TX11-	A81 A82	PCI Express Transmit Output Differential Pairs 11	O PCIE		Supported on SP4 variants by default (BOM option on SP4r2 variants)
PCIE_RX11+ PCIE_RX11-	B81 B82	PCI Express Receive Input Differential Pairs 11	I PCIE		
PCIE_TX12+ PCIE_TX12-	A39 A40	PCI Express Transmit Output Differential Pairs 12	O PCIE		Supported on SP4 variants by default (BOM option on SP4r2 variants)
PCIE_RX12+ PCIE_RX12-	B39 B40	PCI Express Receive Input Differential Pairs 12	I PCIE		
PCIE_TX13+ PCIE_TX13-	A36 A37	PCI Express Transmit Output Differential Pairs 13	O PCIE		Supported on SP4 variants by default (BOM option on SP4r2 variants)
PCIE_RX13+ PCIE_RX13-	B36 B37	PCI Express Receive Input Differential Pairs 13	I PCIE		
PCIE_TX14+ PCIE_TX14-	A25 A26	PCI Express Transmit Output Differential Pairs 14	O PCIE		Supported on SP4 variants by default (BOM option on SP4r2 variants)
PCIE_RX14+ PCIE_RX14-	B25 B26	PCI Express Receive Input Differential Pairs 14	I PCIE		
PCIE_TX15+ PCIE_TX15-	A22 A23	PCI Express Transmit Output Differential Pairs 15	O PCIE		Supported on SP4 variants by default (BOM option on SP4r2 variants)
PCIE_RX15+ PCIE_RX15-	B22 B23	PCI Express Receive Input Differential Pairs 15	I PCIE		
PCIE_TX16+ PCIE_TX16-	D52 D53	PCI Express Transmit Output Differential Pairs 16	O PCIE		
PCIE_RX16+ PCIE_RX16-	C52 C53	PCI Express Receive Input Differential Pairs 16	I PCIE		
PCIE_TX17+ PCIE_TX17-	D55 D56	PCI Express Transmit Output Differential Pairs 17	O PCIE		
PCIE_RX17+ PCIE_RX17-	C55 C56	PCI Express Receive Input Differential Pairs 17	I PCIE		
PCIE_TX18+ PCIE_TX18-	D58 D59	PCI Express Transmit Output Differential Pairs 18	O PCIE		
PCIE_RX18+ PCIE_RX18-	C58 C59	PCI Express Receive Input Differential Pairs 18	I PCIE		
PCIE_TX19+ PCIE_TX19-	D61 D62	PCI Express Transmit Output Differential Pairs 19	O PCIE		
PCIE_RX19+ PCIE_RX19-	C61 C62	PCI Express Receive Input Differential Pairs 19	I PCIE		
PCIE_TX20+ PCIE_TX20-	D65 D66	PCI Express Transmit Output Differential Pairs 20	O PCIE		
PCIE_RX20+ PCIE_RX20-	C65 C66	PCI Express Receive Input Differential Pairs 20	I PCIE		

PCIE_TX21+ PCIE_TX21-	D68 D69	PCI Express Transmit Output Differential Pairs 21	O PCIE		
PCIE_RX21+ PCIE_RX21-	C68 C69	PCI Express Receive Input Differential Pairs 21	I PCIE		
PCIE_TX22+ PCIE_TX22-	D71 D72	PCI Express Transmit Output Differential Pairs 22	O PCIE		
PCIE_RX22+ PCIE_RX22-	C71 C72	PCI Express Receive Input Differential Pairs 22	I PCIE		
PCIE_TX23+ PCIE_TX23-	D74 D75	PCI Express Transmit Output Differential Pairs 23	O PCIE		
PCIE_RX23+ PCIE_RX23-	C74 C75	PCI Express Receive Input Differential Pairs 23	I PCIE		
PCIE_TX24+ PCIE_TX24-	D78 D79	PCI Express Transmit Output Differential Pairs 24	O PCIE		
PCIE_RX24+ PCIE_RX24-	C78 C79	PCI Express Receive Input Differential Pairs 24	I PCIE		
PCIE_TX25+ PCIE_TX25-	D81 D82	PCI Express Transmit Output Differential Pairs 25	O PCIE		
PCIE_RX25+ PCIE_RX25-	C81 C82	PCI Express Receive Input Differential Pairs 25	I PCIE		
PCIE_TX26+ PCIE_TX26-	D85 D86	PCI Express Transmit Output Differential Pairs 26	O PCIE		
PCIE_RX26+ PCIE_RX26-	C85 C86	PCI Express Receive Input Differential Pairs 26	I PCIE		
PCIE_TX27+ PCIE_TX27-	D88 D89	PCI Express Transmit Output Differential Pairs 27	O PCIE		
PCIE_RX27+ PCIE_RX27-	C88 C89	PCI Express Receive Input Differential Pairs 27	I PCIE		
PCIE_TX28+ PCIE_TX28-	D91 D92	PCI Express Transmit Output Differential Pairs 28	O PCIE		
PCIE_RX28+ PCIE_RX28-	C91 C92	PCI Express Receive Input Differential Pairs 28	I PCIE		
PCIE_TX29+ PCIE_TX29-	D94 D95	PCI Express Transmit Output Differential Pairs 29	O PCIE		
PCIE_RX29+ PCIE_RX29-	C94 C95	PCI Express Receive Input Differential Pairs 29	I PCIE		
PCIE_TX30+ PCIE_TX30-	D98 D99	PCI Express Transmit Output Differential Pairs 30	O PCIE		
PCIE_RX30+ PCIE_RX30-	C98 C99	PCI Express Receive Input Differential Pairs 30	I PCIE		
PCIE_TX31+ PCIE_TX31-	D101 D102	PCI Express Transmit Output Differential Pairs 31	O PCIE		
PCIE_RX31+ PCIE_RX31-	C101 C102	PCI Express Receive Input Differential Pairs 31	I PCIE		

PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express Lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if the design involves more than one PCI Express device.

Table 21 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair	I SATA		Supports Serial ATA specification, Revision 3.0
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair	O SATA		Supports Serial ATA specification, Revision 3.0
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair	I SATA		Supports Serial ATA specification, Revision 3.0
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair	O SATA		Supports Serial ATA specification, Revision 3.0
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low	I/O 3.3V	PU 10K	Indicates NVMe activity on variants with SP4 BGA socket. **Note:** Not supported on variants with SP4r2 BGA socket

Table 22 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		
			1000BASE-T	100BASE-TX	10BASE-T			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low				OD 3.3V		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low				OD 3.3V		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low				OD 3.3V		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low				OD 3.3V		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less				REF		Not connected
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1 pps signal				I/O 3.3VSB	PU 10K	

Table 23 NC-SI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
NCSI_CLK_IN	B91	NC-SI Clock reference for receive, transmit, and control interface	I 3.3V	PD 10K	
NCSI_RXD0 NCSI_RXD1	B93 B92	NC-SI Receive Data (from NC to BMC)	O 3.3V	PU 10K	
NCSI_TXD0 NCSI_TXD1	B96 B95	NC-SI Transmit Data (from BMC to NC)	I 3.3V	PU 10K	
NCSI_CRS_DV	B94	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid	O 3.3V	PD 10K	
NCSI_TX_EN	A84	NC-SI Transmit enable	I 3.3V	PD 10K	
NCSI_RX_ER	B89	NC-SI Receive error	O 3.3V		Not supported
NCSI_ARB_IN	B98	NC-SI hardware arbitration input	I 3.3V	PU 10K	
NCSI_ARB_OUT	B99	NC-SI hardware arbitration output	O 3.3V		

Table 24 10 Gigabit Ethernet Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
10G_KR_TX0+ 10G_KR_TX0-	D49 D50	10GBASE-KR ports, transmit output differential pairs 0	O KR		
10G_KR_RX0+ 10G_KR_RX0-	C49 C50	10GBASE-KR ports, receive input differential pairs 0	I KR		
10G_KR_TX1+ 10G_KR_TX1-	D42 D43	10GBASE-KR ports, transmit output differential pairs 1	O KR		
10G_KR_RX1+ 10G_KR_RX1-	C42 C43	10GBASE-KR ports, receive input differential pairs 1	I KR		
10G_KR_TX2+ 10G_KR_TX2-	D29 D30	10GBASE-KR ports, transmit output differential pairs 2	O KR		
10G_KR_RX2+ 10G_KR_RX2-	C29 C30	10GBASE-KR ports, receive input differential pairs 2	I KR		
10G_KR_TX3+ 10G_KR_TX3-	D26 D27	10GBASE-KR ports, transmit output differential pairs 3	O KR		
10G_KR_RX3+ 10G_KR_RX3-	C26 C27	10GBASE-KR ports, receive input differential pairs 3	I KR		
10G_PHY_MDIO_SDA[0:3]	D46 D45 D16 D15	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY	O 3.3V	PU 2.2K	10G_PHY_MDIO_SDA1 and 10G_PHY_MDIO_SDA3 are not supported
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY	I/O OD 3.3V	PU 2.2K	

10G_PHY_MDC_SCL[0:3]	C46 C45 C16 C15	MDIO Mode: Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY	O 3.3V	PU 2.2K	10G_PHY_MDC_SCL1 and 10G_PHY_MDC_SCL3 are not supported
		I2C Mode: I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY	I/O OD 3.3V	PU 2.2K	
10G_PHY_CAP_01	D35	PHY mode capability pin: Indicates if the PHY for 10G lanes 0 and 1 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configuration capability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module. Based on this input, the actual protocol used is indicated over the dedicated I²C interface	I 3.3V		Not connected
10G_PHY_CAP_23	D34	Phy mode capability pin: Indicates if the PHY for 10G lanes 2 and 3 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configuration capability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module. Based on this input, the actual protocol used is indicated over the dedicated I²C interface	I 3.3V		Not connected
10G_SFP_SDA[0:3]	C39 C38 C33 C32	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP module	I/O OD 3.3V	PU 2.2K	
10G_SFP_SCL[0:3]	D39 D38 D33 D32	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP module	I/O OD 3.3V	PU 2.2K	
10G_LED_SDA	C36	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs	I/O OD 3.3V		Not connected
10G_LED_SCL	C37	I2C Clock of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs	I/O OD 3.3V		Not connected
10G_INT[0:3]	C47 D47 C24 D24	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I CMOS	PU 2.2K	
10G_SDP[0:3]	C40 D40 C17 D17	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O 3.3V		Not connected
10G_PHY_RST_01	C35	Output signal that resets an optical PHY on port 0 and port1 (with copper PHY this signal is not used)	O 3.3V		
10G_PHY_RST_23	C34	Output signal that resets an Optical PHY on port 2 and port 3 (with copper PHY this signal is not used)	O 3.3V		

Table 25 USB 2. 0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB Port 0, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+ USB1-	B46 B45	USB Port 1, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+ USB2-	A43 A42	USB Port 2, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+ USB3-	B43 B42	USB Port 3, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low	I 3.3VSB	PU 10K	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low	I 3.3VSB	PU 10K	Do not pull this line high on the carrier board.
USB0_HOST_ PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high values indicates that a host is present	I 3.3VSB		Not connected

Table 26 USB 3.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+ USB_SSRX0-	C4 C3	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX0+ USB_SSTX0-	D4 D3	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSRX1+ USB_SSRX1-	C7 C6	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX1+ USB_SSTX1-	D7 D6	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSRX2+ USB_SSRX2-	C10 C9	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX2+ USB_SSTX2-	D10 D9	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSRX3+ USB_SSRX3-	C13 C12	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX3+ USB_SSTX3-	D13 D12	Additional transmit signal differential pairs for the Superspeed USB data path	O		

Table 27 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V	PU 4.7K	
LPC_CLK	B10	LPC clock output - 24 MHz nominal	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V		LPC_DRQ1# is not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3V	PU 10K	
SUS_STAT#	B18	In LPC mode, SUS_STAT# indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state	O 3.3V		
ESPI_EN#	B47	This signal is used by the carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The carrier should only float this line or pull it low	I 3.3V		Not connected

Table 28 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for carrier board SPI BIOS flash	O 3.3VSB		Carrier shall pull to SPI_POWER when external SPI is provided but not used.
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flas	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	O 3.3V		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device	I 3.3VSB		Not supported
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device	I 3.3VSB	PU 10K 3.3 VSB	

Table 29 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O 3.3V-T		
SER0_RX	A99	General purpose serial port receiver	I 3.3V-T	PU 47.5K 3.3V	
SER1_TX	A101	General purpose serial port transmitter	O 3.3V-T		
SER1_RX	A102	General purpose serial port receiver	I 3.3V-T	PU 47.5K 3.3V	

Table 30 I²C Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output	I/O OD 3.3VSB	PU 2.2K	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O OD 3.3VSB	PU 2.2K	

Table 31 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		Not supported
WDT	B27	Output indicating that a watchdog time-out event has occurred	O 3.3V	PD 100K	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM	O OD 3.3V-T		
FAN_TACHIN	B102	Fan tachometer input.	I OD 3.3V-T	PU 47.5K 3.3V	Requires a fan with a two pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM	I 3.3V	PD 100K	

Table 32 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered System will not be held in hardware reset while this input is kept low	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to delay the startup of the of module to enable the programming of FPGAs or other configurable devices on the carrier board	I 3.3V		Set by resistor divider to accept 3.3V.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices. Not used in eSPI implementations	O 3.3VSB		

Signal	Pin #	Description	I/O	PU/PD	Comment
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board may be used to enable the non-standby power on a typical ATX power supply	O 3.3VSB	PD 4.7K	Signal may be used to enable ATX power supply but does not initiate a "Suspend-to-RAM" state.
SUS_S4#	A18	SUS_S4# pin is tied to SUS_S5# pin. When asserted, it indicates that system is in Soft Off state	O 3.3VSB	PD 4.7K	
SUS_S5#	A24		O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity	I 3.3VSB		Not supported
BATLOW#	A27	Can be used as a power-fail indication	I 3.3VSB	PU 10K 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch	I OD 3.3VSB-T	PU 47.5K 3.3VSB	
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again	I OD 3.3VSB-T	PU 10K 3.3VSB	

Table 33 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_ SHUTDOWN	C67	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs	I 3.3V		Not supported

Table 34 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation	I 3.3V	PU 10K 3.3V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown	O 3.3V	PU 4.75K 3.3V	

Table 35 SMBus Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line	I/O 3.3VSB	PU 2.2K	
SMB_DAT#	B14	System Management Bus bidirectional data line	I/O OD 3.3VSB	PU 2.2K	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system	I 3.3VSB	PU 10K 3.3VSB	

Table 36 SDIO / General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins	O 3.3V		
GPO1	B54	General purpose output pins	O 3.3V		
GPO2	B57	General purpose output pins	O 3.3V		
GPO3	B63	General purpose output pins	O 3.3V		
GPI0	A54	General purpose input pins; pulled high internally on the module	I 3.3V	PU 10K 3.3V	
GPI1	A63	General purpose input pins; pulled high internally on the module	I 3.3V	PU 10K 3.3V	
GPI2	A67	General purpose input pins; pulled high internally on the module	I 3.3V	PU 10K 3.3V	
GPI3	A85	General purpose input pins; pulled high internally on the module	I 3.3V	PU 10K 3.3V	

Note

The conga-B7E3 does not support SDIO.

Table 37 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109 C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V	P		

Signal	Pin #	Description	I/O	PU/PD	Comment
GND	A1, A11, A21, A31, A38, A41, A51, A57, A60, A66, A70, A73, A76, A79, A80, A83, A90, A100, A110 B1, B11, B21, B31, B38, B41, B51, B60, B70, B73, B76, B79, B80, B83, B90, B100, B110 C1, C2, C5, C8, C11, C14, C18, C21, C25, C28, C31, C41, C44, C48, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110 D1, D2, D5, D8, D11, D14, D18, D21, D25, D28, D31, D41, D44, D48, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

Table 38 Module Type Definition Signal Description

Signal	Pin #	Description				I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1 and Type 10, these pins are don't care (X)				PDS	TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard. The conga-B7E3 is based on the COM Express Type 7 pinout, therefore pins C54 and D57 are connected to GND and pin C57 is not connected.
		TYPE2#	TYPE1#	TYPE0#			
		X NC NC NC NC GND GND X	X NC NC GND GND NC NC X	X NC GND NC GND NC GND X	Pinout Type 1 (deprecated) Pinout Type 2 (deprecated) Pinout Type 3 (deprecated) Pinout Type 4 (deprecated) Pinout Type 5 (deprecated) Pinout Type 6 Pinout Type 7 Pinout Type 10		
		The carrier board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The carrier board logic may also implement a fault indicator such as an LED					

Signal	Pin #	Description		I/O	Comment
TYPE10#	A97	Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed		PDS	Not connected to indicate "Pinout R2.0".
		TYPE10#			
		NC PD 12V	Pinout R2.0 Pinout Type 10 pull down to ground with 4.7K resistor Pinout R1.0		
		This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. R3.0 module types 6 and 7 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7K resistor			

8.2 Boot Strap Signals

Table 39 Boot Strap Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_FRAME#	B3	Boot interface selection	O 3.3V	PU 4.7K	

Note

1. *The signal listed in the table above is used as chipset configuration strap during system reset. During reset, the COM Express or chipset internal resistors pull this signal to the correct state.*

2. *Do not drive this signal until 1 microsecond after CB_RESET# de-asserts.*

Caution

No external DC loads or external pull-up or pull-down resistors should change the configuration of the signal listed in the above table during the power-up sequence. The COM Express module may malfunction or be damaged if external resistors override the internal strap state.

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-B7E3 module is functionally identical with a standard PC/AT. The table below shows the most important addresses and the addresses that differ from the standard PC/AT configuration.

Table 40 I/O Resources

Address	Device
A00h - A3Fh	ASPEED BMC software wake control
A40h - A4Fh	ASPEED BMC mailbox
CA0h - CAFh	ASPEED BMC keyboard controller style interface
E00h - EFFh	congatec Board Controller

9.2 PCI Configuration Space Map

Table 41 PCI Device Mapping

Bus	Device (hex)	Function (hex)	Vendor ID (hex)	Device ID (hex)	Description
00h / 40h [1]	00h	00h	1022h	1450h	Root Complex
00h / 40h [1]	00h	02h	1022h	1451h	IOMMU
00h / 40h [1]	01h	00h	1022h	1452h	PCIe Dummy Host Bridge
00h / 40h [1]	01h	01h	1022h	1453h	PCIe GPP Bridge 0
00h / 40h [1]	01h	02h	1022h	1453h	PCIe GPP Bridge 1
00h / 40h [1]	01h	03h	1022h	1453h	PCIe GPP Bridge 2
00h / 40h [1]	01h	04h	1022h	1453h	PCIe GPP Bridge 3
00h / 40h [1]	01h	05h	1022h	1453h	PCIe GPP Bridge 4
00h / 40h [1]	01h	06h	1022h	1453h	PCIe GPP Bridge 5
00h / 40h [1]	01h	07h	1022h	1453h	PCIe GPP Bridge 6
00h / 40h [1]	02h	00h	1022h	1452h	PCIe Dummy Host Bridge
00h / 40h [1]	02h	01h	1022h	1453h	PCIe GPP Bridge 7
00h / 40h [1]	03h	00h	1022h	1452h	PCIe Dummy Host Bridge
00h / 40h [1]	03h	01h	1022h	1453h	PCIe GPP Bridge 0
00h / 40h [1]	03h	02h	1022h	1453h	PCIe GPP Bridge 1
00h / 40h [1]	03h	03h	1022h	1453h	PCIe GPP Bridge 2

Bus	Device (hex)	Function (hex)	Vendor ID (hex)	Device ID (hex)	Description
00h / 40h [1]	03h	04h	1022h	1453h	PCIe GPP Bridge 3
00h / 40h [1]	03h	05h	1022h	1453h	PCIe GPP Bridge 4
00h / 40h [1]	03h	06h	1022h	1453h	PCIe GPP Bridge 5
00h / 40h [1]	03h	07h	1022h	1453h	PCIe GPP Bridge 6
00h / 40h [1]	04h	00h	1022h	1452h	PCIe Dummy Host Bridge
00h / 40h [1]	04h	01h	1022h	1453h	PCIe GPP Bridge 7
00h / 40h [1]	07h	00h	1022h	1452h	PCIe Dummy Host Bridge
00h / 40h [1]	07h	01h	1022h	1454h	Internal PCIe GPP Bridge 0 to Bus B / D
00h / 40h [1]	08h	00h	1022h	1452h	PCIe Dummy Host Bridge
00h / 40h [1]	08h	01h	1022h	1454h	Internal PCIe GPP Bridge 0 to Bus C / E
00h	14h	00h	1022h	790Bh	SMBus Controller
00h	14h	03h	1022h	790Eh	LPC Bridge
00h	18h	00h	1022h	1460h	Data Fabric
00h	18h	01h	1022h	1461h	Data Fabric
00h	18h	02h	1022h	1462h	Data Fabric
00h	18h	03h	1022h	1463h	Data Fabric
00h	18h	04h	1022h	1464h	Data Fabric
00h	18h	05h	1022h	1465h	Data Fabric
00h	18h	06h	1022h	1466h	Data Fabric
00h	18h	07h	1022h	1467h	Data Fabric
00h	19h	00h	1022h	1460h	Data Fabric [4]
00h	19h	01h	1022h	1461h	Data Fabric [4]
00h	19h	02h	1022h	1462h	Data Fabric [4]
00h	19h	03h	1022h	1463h	Data Fabric [4]
00h	19h	04h	1022h	1464h	Data Fabric [4]
00h	19h	05h	1022h	1465h	Data Fabric [4]
00h	19h	06h	1022h	1466h	Data Fabric [4]
00h	19h	07h	1022h	1467h	Data Fabric [4]
Bus B / D [2]	00h	00h	1022h	145Ah	PCIe Dummy Function
Bus B / D [2]	00h	02h	1022h	1456h	Cryptographic Coprocessor PSPCCP
Bus B / D [2]	00h	03h	1022h	145Fh	USB3 XHC
Bus C / E [2]	00h	00h	1022h	1455h	PCIe Dummy Function
Bus C / E [2]	00h	01h	1022h	1468h	Cryptographic Coprocessor NTBCCP
Bus C	00h	02h	1022h	7901h	SATA AHCI Mode
Bus C	00h	03h	1022h	1457h	HD Audio Controller
Bus C	00h	04h	1022h	1458h	10 Gb Ethernet Controller (XGbE) Port 0
Bus C	00h	05h	1022h	1458h	10 Gb Ethernet Controller (XGbE) Port 1
Bus C	00h	06h	1022h	1459h	10 Gb Ethernet Controller (XGbE) Port 2
Bus C	00h	07h	1022h	1459h	10 Gb Ethernet Controller (XGbE) Port 3

Bus	Device (hex)	Function (hex)	Vendor ID (hex)	Device ID (hex)	Description
Bus E	00h	04h	1022h	1458h	10 Gb Ethernet Controller (XGbE) Port 2 [4]
Bus E	00h	05h	1022h	1458h	10 Gb Ethernet Controller (XGbE) Port 3 [4]
Bus I [3]	00h	00h	8086h	1533h	Intel Ethernet Controller (i210 GbE)
Bus J [3]	00h	00h	126Fh	2263h	Onboard NVMe SSD [4]
Bus K [3]	00h	00h	1A03h	1150h	ASPEED 2500 BMC [5]
Bus L [3]	00h	00h	1A03h	2000h	ASPEED 2500 BMC VGA [5]

Note

1. *The boot die in a multi-die processor assigns bus to 00h. For SP4 processor, bus 40h is assigned to die 1.*
2. *Programmable bus numbers are labeled B, C, D and E. Buses with different labels cannot be assigned the same bus number. Bus B and C are associated with the boot die, and Bus D and E are associated with die 1 for SP4 processor.*
3. *The bus numbers represented with I, J, K and L will vary depending on the system configuration (lane width), the connected PCIe devices (switches or bridges) and where PCIe devices are connected.*
4. *Applies only to conga-B7E3 variants with SP4 processor.*
5. *These devices are not available if the BMC is not implemented on the carrier board.*

9.3 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.4 SMBus

The SMBus signals are connected to the AMD SoC. The SMBus is not intended to be used by off-board non-system management devices. For more information about this subject, contact congatec technical support.

10 BIOS Setup Description

The BIOS setup description of the conga-B7E3 can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note “AN42 - BIOS Setup Description” available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-B7E3 is identified as B7E3R1xx, where:

- R is the identifier for a BIOS binary file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The conga-B7E3 BIOS binary size is 16 MB.

10.3 Updating the BIOS

BIOS updates are recommeded to correct platform issues or enhance the feature set of the module. The conga-B7E3 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated.*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

10.4 Recovering from External Flash

The following congatec documents describe how to recover a congatec module from external flash. You can find these documents on the congatec website:

- AN1_BIOS_Update.pdf
- AN5_BIOS_Update_And_Write_Protection.pdf
- AN7_External_BIOS_Update.pdf

10.5 Supported Flash Devices

The conga-B7E3 supports the following flash devices:

- Winbond W25Q128JVSIQ
- Macronix MX25L12833FM2I-10G
- Macronix MX25L12835FM2I-10G

The flash devices listed above can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.