congatec Application Note

Affected Products	All Products
Subject	USB 3.2 Gen 2 Carrier Board Design Considerations
Confidential/Public	Public
Author	SDA

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
1.0	2020-04-27	SDA	Initial Release
1.1	2021-02-11	SDA	Added section 2.2.1 AC Coupling Capacitors

Preface

This application note provides routing rules, reference schematic and design notes for USB 3.2 Gen 2 carrier board designs.

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Symbols

The following are symbols used in this application note.

Note

Notes call attention to important information that should be observed.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

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Terminology

Term	Description
CMC	Common Mode Choke
Tx	Transmit Differential Pair
Rx	Receive Differential Pair
ESD	Electrostatic Discharge
EOS	Electrical Overstress
COM	Computer-On-Module
EMI	Electromagnetic Interference
SMD	Surface Mount Device
THT	Through Hole Technology

1 Introduction

Industrial applications become increasingly powerful and demand a higher performance connection between the embedded computer and sophisticated external peripherals.

In order to meet this requirement, the USB 3.2 Specification released in September 2017, specified the following transfer rates:

- USB 3.2 Gen 1 (SuperSpeed USB 5 Gbps)
- USB 3.2 Gen 2 (SuperSpeed USB 10 Gbps)
- USB 3.2 Gen 2x2 (SuperSpeed USB 20 Gbps)

USB 3.2 Gen 1 (previously known as USB 3.0 or USB SuperSpeed) provides a maximum transfer rate of 5 Gbps through one lane. USB 3.2 Gen 2 increased the maximum transfer rate to 10 Gbps and reduced line encoding overhead to just 3% by changing the encoding scheme to 128b/132b. USB 3.2 specification additionally defined USB-C connector for multi-lane operation between new USB 3.2 hosts and devices. This allows to use two USB 3.2 Gen 2 lanes to reach a transfer rate of 20 Gbps.

This application note shows design considerations for USB 3.2 Gen 2 (SuperSpeed USB 10 Gbps).

2 USB 3.2 Gen 2 Design Guidelines

2.1 Routing Rules

Parameter	Trace Routing
Transfer Rate	10 Gbps
Maximum trace length allowance for the COM Express carrier board	3.0 Inches The maximum trace length strongly depends on the dielectric loss tangent of the used PCB material. The maximum trace length is defined for FR-4 (Dk≤3.9, Df≤0.02) PCB material
Length matching ("within layer" and "total length")	Max. 5 mils
Differential Impedance	85 Ω +/-10%
Microstrip/Stripline	Microstrip preferred
Via Usage	2
Via stub length	< 10 mils
Via anti-pad	Single oval anti-pad size of 40mils for each differential pair Via optimization to match impedance and reduce loss is recommended
Reference plane	Continuous Ground
Common Mode Choke (CMC)	Not required for Rx lane
Recommended ESD Protection Diodes	Max. capacitance: 0.2pF ON Semiconductor ESD7008 (Optional: Nexperia PUSB3AB4)

Recommended Connector	USB-C (SMD)
Recommended COM Express connector	ept Colibri Plug 401-55103-51
Routing Insertion Loss Diagram	Max 3.5dB @ 5GHz (PCB trace routing only, no components attached) 

2.2 Design Notes

2.2.1 AC Coupling Capacitors

USB_TX

The required AC coupling capacitors for USB_TX signals are featured on the Computer-On-Module (COM) and should not be placed on the carrier board.

USB_RX

The AC coupling capacitors for USB_RX signals are typically featured in the USB device and should not be placed on the carrier board.

However, optional AC coupling capacitors can help to protect against electrostatic discharge (ESD), electrical overstress (EOS), and reduce bias level. We recommend 330nF capacitors in order to meet the minimum capacitance requirement (75nF to 265nF) for RX detection. A 0Ω resistor per signal trace can be used to replace the optional AC coupling capacitors.

Note

conga-TR4 and conga-B7E3 feature AC coupling capacitors for USB_RX signals.

2.2.2 Common Mode Choke (CMC)

USB designs should include common mode chokes in Tx and Rx differential pairs to improve EMI behavior. These components suppress common mode noise introduced by intra-pair skew or power noise coupling. However, they distort the signal quality of USB SuperSpeed signaling.

Single 0 Ω resistors per signal trace can be used to replace the CMC components if it is proven that there is no EMI risk. Layout implementation should be carried out with a common footprint for CMC component and resistors. CMC components for USB Rx differential pairs are not required because of a lower risk for introducing electromagnetic disturbance. For USB-C alternate mode, which uses DisplayPort instead of USB SuperSpeed, it is required to use CMC components in all differential pairs.

2.2.3 USB Connector

Proper connector choice is critical to ensure adequate USB signal quality. To improve the signal integrity, use an SMD USB Type-C connector.

For USB Type-A, use the SMD based connector instead of the THT connector. When using the THT USB Type-A connector, the USB SuperSpeed signals should be routed to the bottom side of the through-hole connector in order to minimize stub effects. Additionally, note that stacked USB connectors may also cause signal degradation.

2.2.4 COM connector

The COM board-to-board connector introduces additional signal losses. High-speed capable COM standards like COM-HPC® meets the high-speed signaling requirements. Recommended COM connector for COM Express designs is EPT Colibri Plug (401-55103-51).

2.2.5 ESD Protection

In order to ensure adequate ESD robustness, place ESD protection diodes for each USB data line. However, ESD diodes introduce parasitic capacitance and additional signal losses. ESD protection diodes for high-speed interfaces should offer a very low line capacitance. We recommend ON Semiconductor ESD7008 protection diodes with a typical line capacitance of 0.12pF.

2.2.6 Routing Impedance

This document recommends a differential impedance of 85Ω. However, lower routing impedance can improve the signal if the PCB stackup allows it. A differential impedance of 80Ω shows fewer copper losses and fits better to capacitive vias. Additionally, we recommend controlled impedance manufacturing.

2.2.7 Via Design

Transitional vias should use oval anti-pads on all plane layers to reduce via capacitance. We recommend to design-in independent anti-pads for each differential pair in order to

avoid coupling effects. The vias must also have a symmetrical trace entry.

Additionally, it is required to use current return vias for each signal via. Figure 1 shows an example of an appropriate via design with four current return vias. The minimum requirement is to use two current return via.

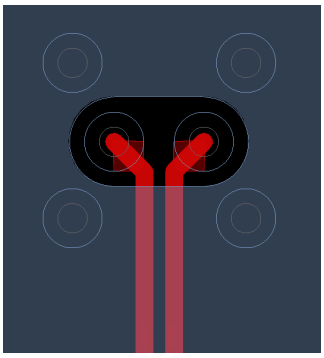

Figure 1: Via Design

2.2.8 GND cutouts

GND cutouts underneath SMD components like AC coupling capacitors, CMCs or ESD diodes should be used in order to avoid parasitic capacitance.

3 USB 3.2 Gen 2 Re-Driver Guidelines

This section provides guidelines for carrier board designers who intend to use re-driver for USB 3.2 Gen 2 implementations.

Re-drivers are active components that may provide receiver equalization, transmitter de-emphasis or signal amplification. Re-drivers do not perform retiming. These components change the analog behavior of the incoming signal only. They do not use any interface protocol or clock source.

Re-timers are protocol-aware components. Re-timers perform re-sampling of the incoming signal and re-transmit the recovered signal.

3.1 USB 3.2 Gen 2 Re-Driver Reference Schematic

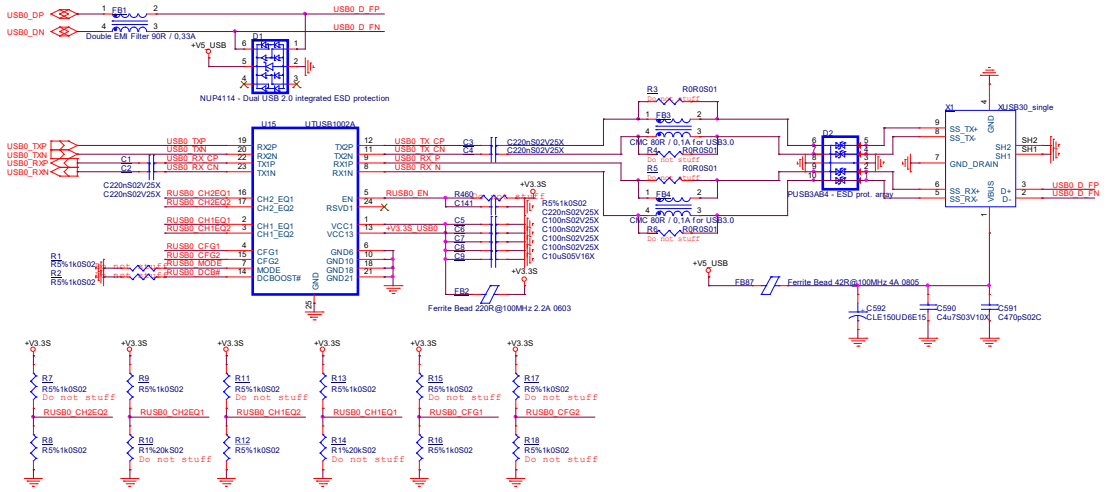

Figure 2: USB 3.2 Gen2 Re-Driver Reference Schematic

The reference schematic shows the implementation of Texas Instruments TUSB1002A USB 3.2 10 Gbps re-driver with a standard USB Type-A connector.

Each USB lane must have AC coupling capacitors between the transmitter and the receiver. The AC coupling capacitors for the Tx lines (USB0_TXP, USB0_TXN) are implemented on the COM. The AC coupling capacitors (C1, C2) for Rx signal lines (USB0_RXP, USB0_RXN) must be implemented on the carrier board. In this example, 220nF capacitors are used.

Additionally, on the carrier board, AC coupling capacitors (C3, C4) must be added to the re-driver's Tx signal lines (USB0_TX_CP, USB0_TX_CN). Note that AC coupling capacitors are not required for the re-driver's Rx signal lines (USB0_RX_P, USB0_RX_N) because the USB device is typically equipped with AC coupling capacitors. Refer to section 2.2.1 "AC Coupling Capacitors" for more information.

The TUSB1002A provides configuration pins CFG1, CFG2, CH1_EQ1, CH1_EQ2, CH2_EQ1, and CH2_EQ2. The configuration pins are used to control the equalization gain and the output voltage swing. The equalization settings and the output voltage swing must be adjusted for different implementations and routing length. The reference design above shows the adjusted settings for conga-TEVAL/COMe 3.0.