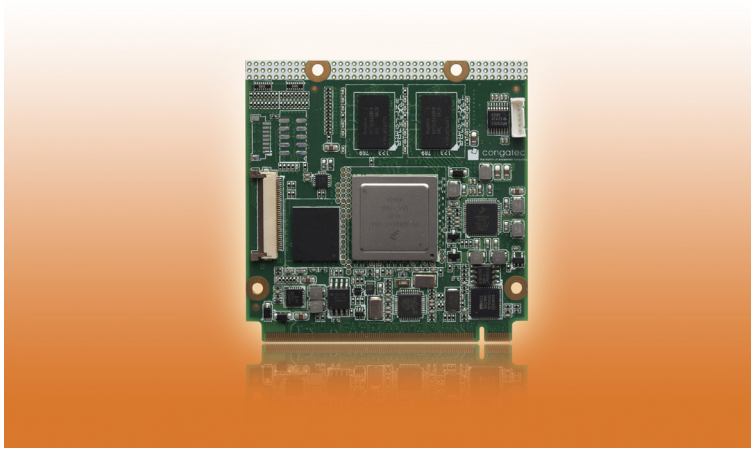

Qseven® conga-QMX6

Freescale® i.MX6 ARM® Cortex A9 processor with Ultra Low Power Consumption

User's Guide

Revision 0.3 (Preliminary)

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2013.03.28	AEM	• Preliminary release
0.2	2013.11.05	AEM	• Corrected the LVDS data rates/resolutions supported in sections 2.1 “Feature List“ and 5.8 “LVDS”. • Added information about the Atheros Quadcomm Ethernet PHY for conga-QMX6 revision B.0 in sections 2.1 “Feature List” and 5.3 “Gigabit Ethernet”. • Updated section 4 “Heatspreader”. Added additional heatspreader variants. • Updated section 5.2 “UART”. Updated section 5.13 “Manufacturing/Jtag Interface”. • Added pin descriptions for the onboard UART connector and the RS-232 adapter cable in section 10.1 “UART/RS-232 Debug Port”. • Added section 10.3 “JTAG Interface”.
0.3	2014.02.28	AEM	• Added the new Ethernet PHY (Qualcomm Atheros) for conga-QMX6 revision B.x to relevant sections. • Changed the eMMC value of industrial variants from 2G to 4G • Deleted the row “RSVD” from table 23 “ Manufacturing Signal Description”. • Edited section 5.2 “UART” and added caution statement. • Updated the whole document.

Preface

This user's guide provides information about the components, features, connectors and signals available on the conga-QMX6. It is one of four documents that you should refer to when designing an i.MX6 based Qseven® application. The other reference documents that should be used include the following:

Qseven® Design Guide

Qseven® Specification

i.MX6 Applications Processor Reference Manual (available at www.freescale.com)

The links to these documents can be found on the congatec AG website at www.congatec.com

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Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
PCI Express (PCIe)	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
ARM	Advanced RISC Machine
JTAG	Joint Test Action Group
eCSPI	Enhanced Configurable Serial Peripheral Interface
MIPI	Mobile Industry CPU Interface
GPIO	General Purpose Input Output
RGMII	Reduced Gigabit Media Independent Interface
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for transmitting and two differential lines for Receiving. Clocking information is embedded into the data stream.
x1, x2, x4, x8, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4, x8, or x16 link.
PCI Express Mini Card	PCI Express Mini Card add-in card is a small size unique form factor optimized for mobile computing platforms.
eMMC	Embedded Multi Media Card is a non-volatile memory system, which frees the processor from low level flash memory management.
SDIO card	SDIO (Secure Digital Input Output) is a non-volatile memory card format developed for use in portable devices.
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial-interface standard for hard disks
HDA	High Definition Audio
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
I²C Bus	Inter-Integrated Circuit Bus: is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system.
SM Bus	System Management Bus: is a popular derivative of the I²C-bus.
SPI Bus	Serial Peripheral Interface is a synchronous serial data link standard named by Motorola that operates in full duplex mode.
CAN Bus	Controller-area network is a vehicle bus standard designed to allow microcontrollers and devices to communicate with each other within a vehicle without a host computer.
AMBA	Advanced Microcontroller Bus Architecture
IOMUX	Input Output Multiplexer
GbE	Gigabit Ethernet
LVDS	Low-Voltage Differential Signaling
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

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Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device

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1 INTRODUCTION

Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector. The pinout remains the same regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The Qseven® evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose what are suitable for their application. Qseven® applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another; no need to redesign the carrier board.

This document describes the features available on the Qseven® evaluation carrier board. Additionally, the schematics for the Qseven® evaluation carrier board can be found on the congatec website.

Note

The conga-QMX6 design is based on the Qseven specification 2.0 and in revision B.0 design, we took into consideration the Qseven Specification 2.0 Errata.

conga-QMX6 Options Information

The conga-QMX6 is currently available in nine variants (five commercial and four industrial). This user's guide describes the features these variants offer. Below you will find an order table showing the base configuration modules that are currently offered by congatec AG. For more information about additional conga-QMX6 variants offered by congatec, contact your local congatec sales representative or visit the congatec website at www.congatec.com.

Table 1 Commercial variants

Part-No.	016100	016101	016102	016103	016104
Processor	Freescale® i.MX6 Cortex A9 1.0 GHz Single Core	Freescale® i.MX6 Cortex A9 1.0 GHz Dual Lite	Freescale® i.MX6 Cortex A9 1.0 GHz Dual Core	Freescale® i.MX6 Cortex A9 1.0 GHz Quad Core	Freescale® i.MX6 Cortex A9 1.0 GHz Quad Core
L2 Cache	512 kB	512 kB	1 MB	1 MB	1 MB
Onboard Memory	1GB DDR3	1GB DDR3	1GB DDR3	1GB DDR3	2GB DDR3
eMMC up to 8GB	4GB	4GB	4GB	4GB	4GB
PCI Express Lane	Yes	Yes	Yes	Yes	Yes
CAN Bus	Yes	Yes	Yes	Yes	Yes
Gigabit Ethernet	Yes	Yes	Yes	Yes	Yes
SATA	No	No	Yes	Yes	Yes

Table 2 Industrial Variants

Part-No.	016110	016111	016112	016113
Processor	Freescale® i.MX6 Cortex A9 800 MHz Single Core	Freescale® i.MX6 Cortex A9 800 MHz Dual Lite	Freescale® i.MX6 Cortex A9 800 MHz Dual Core	Freescale® i.MX6 Cortex A9 800 MHz Quad Core
L2 Cache	512 kB	512 kB	1 MB	1 MB
Onboard Memory	1GB DDR3	1GB DDR3	1GB DDR3	1GB DDR3
eMMC up to 8GB	4GB	4GB	4GB	4GB
PCI Express Lane	Yes	Yes	Yes	Yes
CAN Bus	Yes	Yes	Yes	Yes
Gigabit Ethernet	Yes	Yes	Yes	Yes
SATA	No	No	Yes	Yes

Caution

Do not alter the conga-QMX6 boot fuse settings. These fuse settings are already programmed during production process and are not protected against alteration. Changing the boot fuse settings will void the congatec AG warranty.

2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	Based on Qseven® form factor specification revision 2.0	
Processor	Freescale® i.MX6 Cortex A9	
Memory	up to 2 GB onboard DDR3 memory	
Audio	I2S format supported	
Ethernet	Gigabit Ethernet (Qualcomm Atheros PHY) on conga-QMX6 rev B.x. Earlier conga-QMX6 variants are equipped with Micrel KSZ9031 PHY.	
Graphics Options	Integrated video graphic subsystem consisting of Video Processing Unit (VPU), Graphic Processing Unit (3D GPU, 2D GPU, Open VG), Image Processing Unit, Display interface bridges (LVDS, HDMI, MIPI/DSI).	

	• 1x HDMI 1.4.
	• Two LVDS channels driven by the LVDS display bridge. Support:
	  • Single channel LVDS interface : 1 x 18 bpp or 1 x 24 bpp (up to 85 MHz per interface e.g 1366x768 @ 60Hz + 35% blanking)
	  • Dual channel LVDS interface: 2 x 18 bpp OR 2 x 24 bpp (up to 170 MHz pixel clock e.g 1600x1200 @ 60 Hz + 35% blanking).
	NOTE:
	Supports three independent displays (must be 2x single channel LVDS and 1x HDMI)
		• Video Decode Acceleration:
		MPEG2 MP, HP
		MPEG4 SP
		H.264
		VC-1
		DivX

Peripheral Interfaces	• 1x Serial ATA® Gen 2 (3GB/s) • 1x SDIO • x1 PCI Express Lane Gen 2.0 offering up to 5 GB/s • 5x USB 2.0 ports (4x USB 2.0 hosts and 1x USB 2.0 OTG) • I2S Bus • SPI • CAN	• 8x GPIOs • 3x I²C fast mode, multi-master (two shared I²C buses and one unshared bus) • 1x UART (fully featured UART with control signals, supported on the MXM connector) • 2x RS-232 interfaces supported onboard the conga-QMX6 via RS232 transceiver.
Onboard Interfaces and Devices	• Android Buttons • JTAG • RS-232 Debug Port • SPI Flash (contains the bootloader)	• DDR3 SDRAM memory (up to 2 GB) • Micro-SD Socket • eMMC module (4GB onboard)
Bootloader	Pre-installed open-source bootloader (U-boot)	
Power Management	Yes.	

Note

Some of the features mentioned in the above feature summary are optional. Check the article number of your module and compare it to the conga-QMX6 options information list on page 12 of this user's guide to determine what options are available on your particular module.

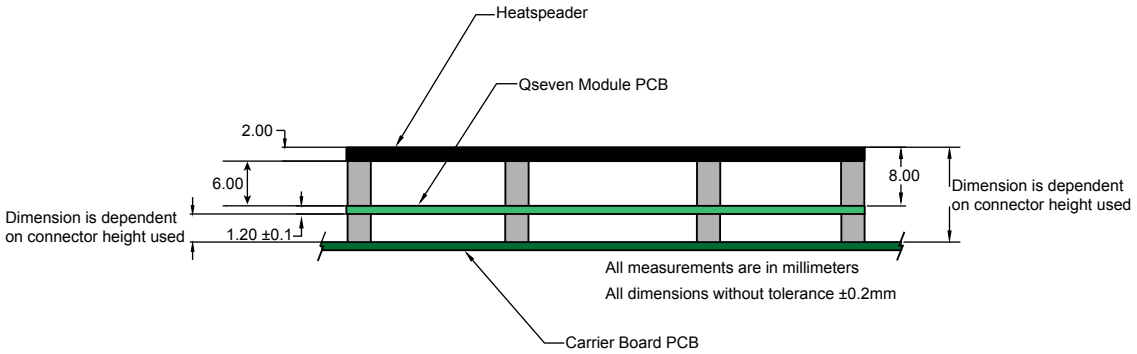
2.2 Supported Operating Systems

The conga-QMX6 supports the following operating systems.

- Microsoft® Windows® Embedded Compact 7
- Android
- Linux

2.3 Mechanical Dimensions

- 70.0 mm x 70.0 mm @ (2 ¾" x 2 ¾")
- The Qseven™ module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.

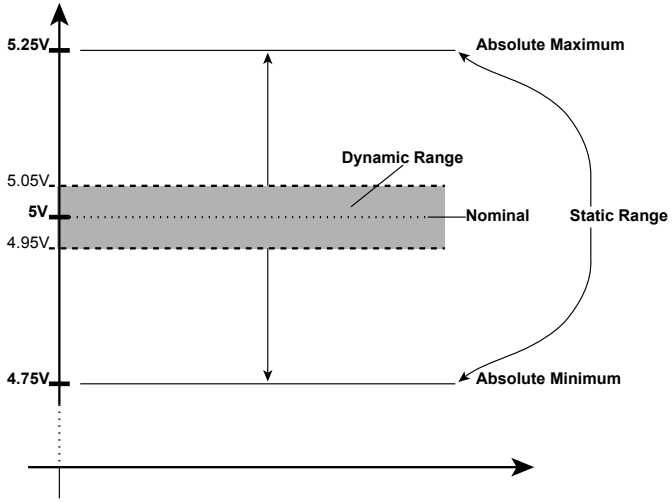


Rear View of Qseven Module

2.4 Supply Voltage Standard Power

- 5V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Characteristics			Min.	Typ.	Max.	Units	Comment
5V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV_{PP}	0-20MHz
	Current						
5V_SB	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple				± 50	mV_{PP}	

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

Note

For information about the input power sequencing of the Qseven® module, refer to the Qseven® specification.

2.5 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used for testing includes a conga-QMX6 module, carrier board for Qseven ARM, TFT monitor, micro-SD card and USB keyboard. The carrier board was powered externally by a power supply unit so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. All recorded values were averaged over a 30 second time period. The modules were cooled by the heatspreader specific to the module variants

Each module was measured while running 32 bit Linaro Ubuntu 11.10. To measure the worst case power consumption, the cooling solution was removed and the CPU core temperature was allowed to run between 95° and 100°C at 100% workload. The peak current value was then recorded. This value should be taken into consideration when designing the system's power supply to ensure that the power supply is sufficient during worst case scenarios.

Power consumption values were recorded during the following stages:

Linaro Ubuntu 11.10 (32 bit)

- Desktop Idle
- 100% CPU workload
- 100% CPU workload at approximately 100°C peak power consumption

Note

With the linux stress tool, we stressed the CPU to maximum frequency.

Processor Information

The tables below provide additional information about the different variants offered by the conga-QMX6.

2.5.1 Freescale® i.MX6 Cortex A9 1.0 GHz Single Core 512kB L2 cache

With 4GB onboard eMMC

conga-QMX6 Art. No. 016100	Freescale® i.MX6 Cortex A9 1.0 GHz 512kB L2 cache 40nm Layout Rev. QMX6LB1 /Bootloader Rev. QMX6Rx07		
Memory Size	1GB onboard		
Operating System	Ubuntu		
Power State	Desktop Idle	100% workload	Max. Power Consumption
Power consumption (measured in Amperes/Watts)	0.22 A/ 1.1 W	0.34 A/ 1.7 W	0.46 A/2.3 W

2.5.2 Freescale® i.MX6 Cortex A9 1.0 GHz Dual Lite 512kB L2 cache

With 4GB onboard eMMC

conga-QMX6 Art. No. 016101	Freescale® i.MX6 Cortex A9 1.0 GHz 512kB L2 cache 40nm Layout Rev. QMX6LB1 /Bootloader Rev. QMX6Rx07		
Memory Size	1GB onboard		
Operating System	Ubuntu		
Power State	Desktop Idle	100% workload	Max. Power Consumption
Power consumption (measured in Amperes/Watts)	0.26 A/ 1.3 W	0.44 A/ 2.2 W	0.66 A/ 3.3 W

2.5.3 Freescale® i.MX6 Cortex A9 1.0 GHz Dual Core 1MB L2 cache

With 4GB onboard eMMC

conga-QMX6 Art. No. 016102	Freescale® i.MX6 Cortex A9 1.0 GHz 1MB L2 cache 40nm Layout Rev. QMX6LB1 /Bootloader Rev. QMX6Rx07		
Memory Size	1GB onboard		
Operating System	Ubuntu		
Power State	Desktop Idle	100% workload	Max. Power Consumption
Power consumption (measured in Amperes/Watts)	0.28 A/ 1.4 W	0.5 A/ 2.5 W	0.7 A/ 3.2 W

2.5.4 Freescale® i.MX6 Cortex A9 1.0 GHz Quad Core 1MB L2 cache

With 4GB onboard eMMC

conga-QMX6 Art. No. 016103	Freescale® i.MX6 Cortex A9 1.0 GHz 1MB L2 cache 40nm Layout Rev. QMX6LB1 /Bootloader Rev. QMX6Rx07		
Memory Size	1GB onboard		
Operating System	Ubuntu		
Power State	Desktop Idle	100% workload	Max. Power Consumption
Power consumption (measured in Amperes/Watts)	0.3 A/ 1.5 W	0.72 A/ 3.6 W	0.92 A/ 4.6 W

2.5.5 Freescale® i.MX6 Cortex A9 1.0 GHz Quad Core 1MB L2 cache

With 4GB onboard eMMC

conga-QMX6 Art. No. 016104	Freescale® i.MX6 Cortex A9 1.0 GHz 1MB L2 cache 40nm Layout Rev. QMX6LB1 /Bootloader Rev. QMX6Rx07		
Memory Size	2GB onboard		
Operating System	Ubuntu		
Power State	Desktop Idle	100% workload	Max. Power Consumption
Power consumption (measured in Amperes/Watts)	0.3 A/ 1.5 W	0.74 A/ 3.7 W	0.94 A/ 4.7 W

2.5.6 Freescale® i.MX6 Cortex A9 800 MHz Single Core 512kB L2 cache (2GB eMMC)

With 2GB onboard eMMC

conga-QMX6 Art. No. 016110	Freescale® i.MX6 Cortex A9 800 MHz 512kB L2 cache 40nm Layout Rev. QMX6LB1 /Bootloader Rev. QMX6Rx07		
Memory Size	1GB onboard		
Operating System	Ubuntu		
Power State	Desktop Idle	100% workload	Max. Power Consumption
Power consumption (measured in Amperes/Watts)	0.24 A/ 1.2 W	0.30 A/ 1.5 W	0.48 A/ 2.1 W

2.5.7 Freescale® i.MX6 Cortex A9 800 MHz Dual Lite 512kB L2 cache (2GB eMMC)

With 2GB onboard eMMC

conga-QMX6 Art. No. 016111	Freescale® i.MX6 Cortex A9 800 MHz 512kB L2 cache 40nm Layout Rev. QMX6LB1 /Bootloader Rev. QMX6Rx07		
Memory Size	1GB onboard		
Operating System	Ubuntu		
Power State	Desktop Idle	100% workload	Max. Power Consumption
Power consumption (measured in Amperes/Watts)	TBD A/ W	TBD A/ W	TBD A/ W

2.5.8 Freescale® i.MX6 Cortex A9 800 MHz Dual Core 1MB L2 cache (2GB eMMC)

With 2GB onboard eMMC

conga-QMX6 Art. No. 016112	Freescale® i.MX6 Cortex A9 800 MHz 1MB L2 cache 40nm Layout Rev. QMX6LB1 /Bootloader Rev. QMX6Rx07		
Memory Size	1GB onboard		
Operating System	Ubuntu		
Power State	Desktop Idle	100% workload	Max. Power Consumption
Power consumption (measured in Amperes/Watts)	0.30 A/ 1.5W	0.42 A/ 2.1 W	0.60 A/ 3.0 W

2.5.9 Freescale® i.MX6 Cortex A9 800 MHz Quad Core 1MB L2 cache (2GB eMMC)

With 2GB onboard eMMC

conga-QMX6 Art. No. 016113	Freescale® i.MX6 Cortex A9 800 MHz 1MB L2 cache 40nm Layout Rev. QMX6LB1 /Bootloader Rev. QMX6Rx07		
Memory Size	1GB onboard		
Operating System	Ubuntu		
Power State	Desktop Idle	100% workload	Max. Power Consumption
Power consumption (measured in Amperes/Watts)	0.30 A/ 1.5 W	0.54 A/ 2.7 W	0.72 A/ 3.6 W

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

2.6 Supply Voltage Battery Power

- 2.0V-3.6V DC
- Typical 3V DC

2.6.1 CMOS Battery Power Consumption

RTC @ 20°C	Voltage	Current
RTC onboard the conga-QMX6 module	3V DC	1.45 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

Note

To improve the lifetime of the CMOS battery, congatec implemented an external real time clock onboard the conga-QMX6 module.

2.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C *(commercial grade variants of conga-QMX6)*
Temperature	Operation: -40° to 85°C	Storage: -40° to +85°C *(industrial grade variants of conga-QMX6)*
Humidity	Operation: 10% to 90%	Storage: 5% to 95% *(humidity specifications are for non-condensing conditions)*

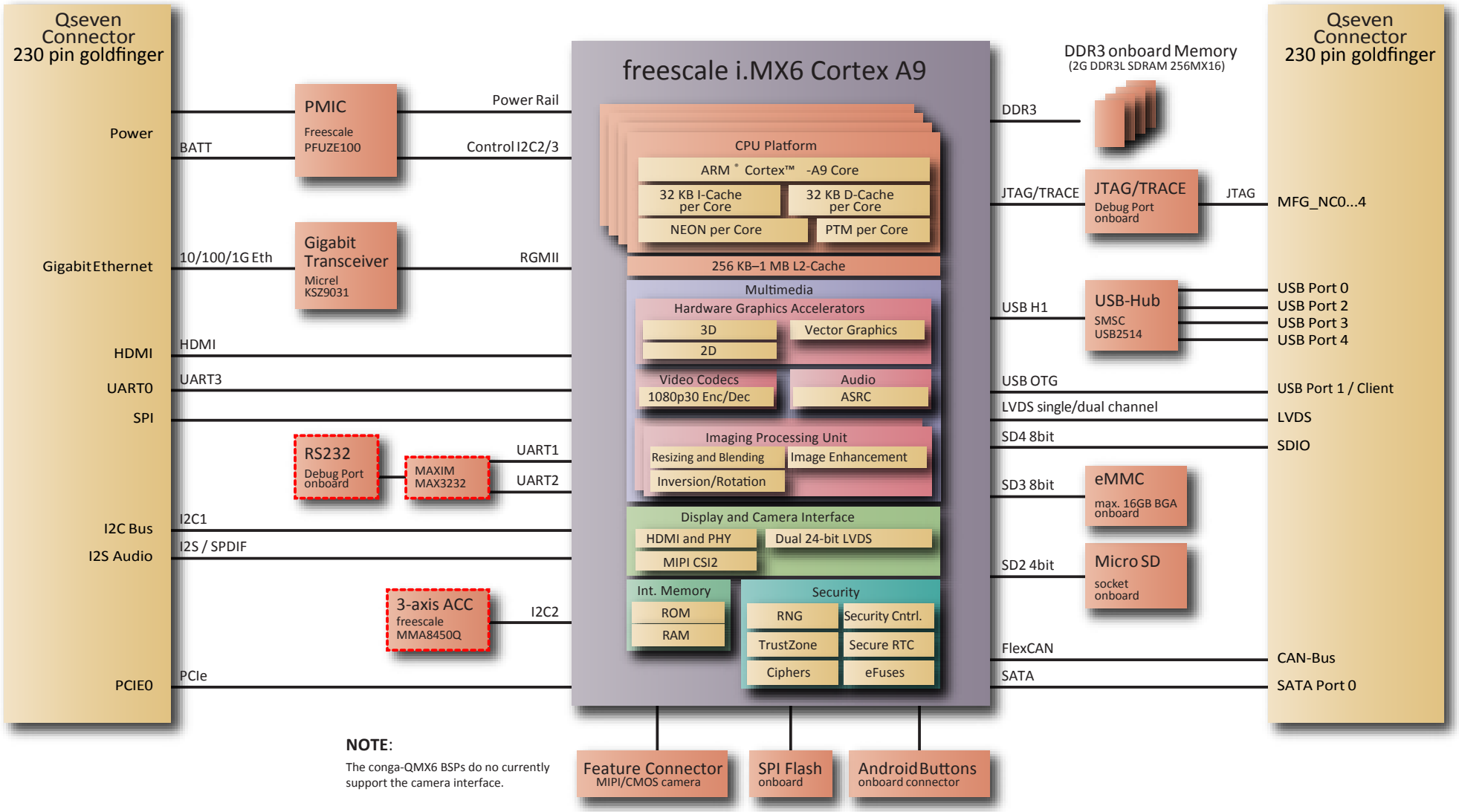
Caution

The above operating temperatures must be strictly adhered to at all times. The congatec heatspreader is only suitable for use within commercial temperature ranges (0° to 60°C), it is not designed to be used within industrial temperature ranges (-40° to 85°C). When using a heatspreader with conga-QMX6 commercial grade variants, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution when used in a commercial temperature range.

If it is not possible to use the appropriate congatec module heatspreader for conga-QMX6 commercial grade variants, or an industrial grade variant of conga-QMX6 is being used within industrial temperature ranges, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

3 Block Diagram



4 Heatspreader

Thermal design is an important factor for systems. This factor is critical when the power dissipation level increases in certain high performance use cases. To ensure the performance and reliability of the system, adequate thermal management technique such as the heatspreader is necessary.

The heatspreader acts as a thermal coupling device to the module. It is thermally coupled to the CPU via a thermal gap filler and on some modules, it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers. Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed as a thermal interface between the module and the application specific thermal solution.

The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis thereby using the whole chassis as a heat dissipater.

congatec AG offers three heatspreader variants for the conga-QMX6. Each heatspreader variant is intended for specific conga-QMX6 modules as shown in the table below:

Heatspreader Variants	Heatspreader Part No. (PN)	Compatible conga-QMX6 Variants (PN)	Comment
conga-QMX6/HSP1-B	016160	016112, 016113	For modules equipped with lidded FC-PBGA CPU (1mm Gap Pad)
conga-QMX6/HSP2-B	016161	016100, 016101, 016110, 016111	For modules equipped with MA-PBGA CPU (2mm Gap Pad)
conga-QMX6/HSP3-B	016162	016102, 016103, 016104	For modules equipped with non-lidded FC-PBGA CPU (heatstack solution)

Note

Currently, only a few Freescale® iMX6 on-chip devices are enabled by default in the bootloader. With this default configuration, the conga-QMX6 power consumption is low. However, power consumption may increase significantly depending on the application and the workload of the CPU.

Caution

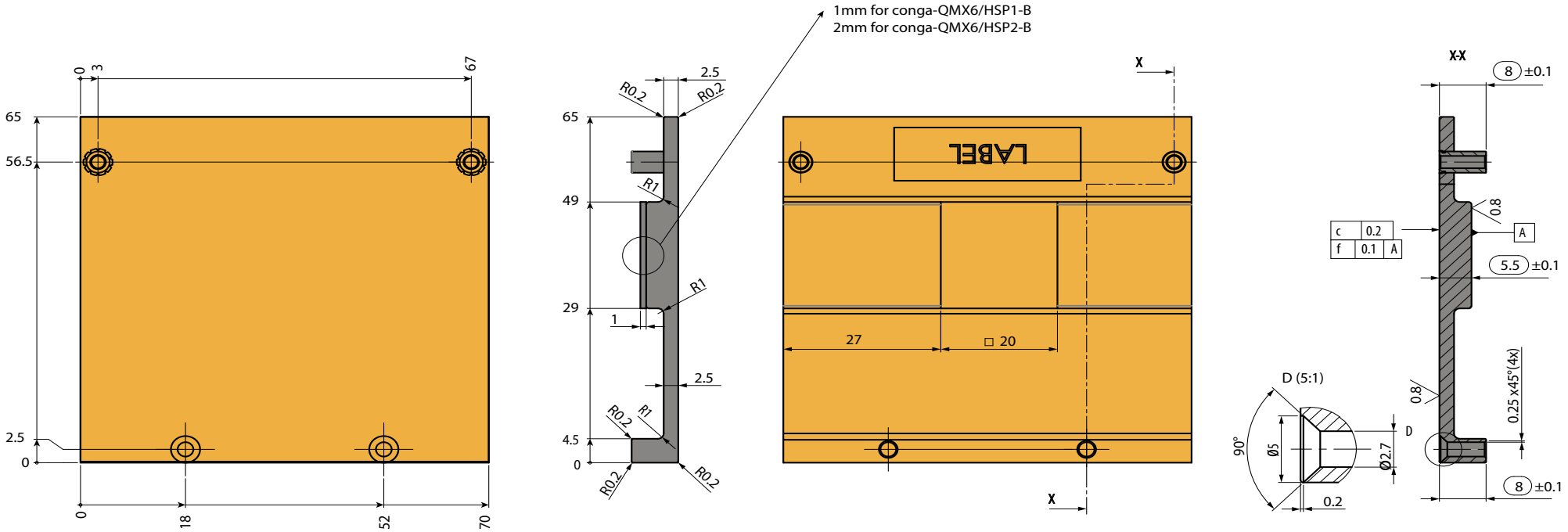
congatec Qseven® heaspreaders have been specifically designed for use within commercial temperature ranges (0° to 60°C) only. When using industrial temperature variants of the conga-QMX6 in industrial temperature ranges (-40° to 85°C), use of the conga-QMX6 heatspreaders is not recommended by congatec; furthermore, its use is at the risk of the end user. It is the responsibility of the end user to design an optimized thermal solution that meets the needs of their application within the industrial environmental conditions it operates in.

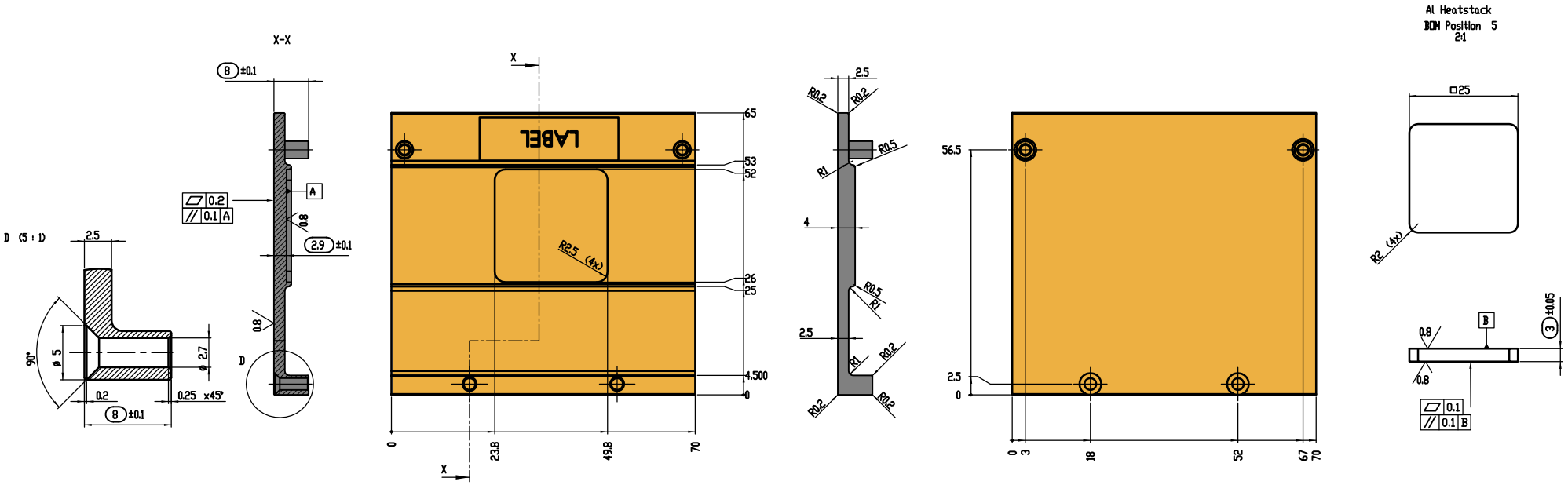
There are mounting holes on the heatspreader designed to attach the heatspreader to the module. These mounting holes must be used to ensure that all components that are required to make contact with heatspreader do so. Failure to utilize these mounting holes will result in improper contact between these components and heatspreader thereby reducing heat dissipation efficiency.

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

4.1 Heatspreader Dimensions

conga-QMX6/HSP1-B and HSP2-B





Note

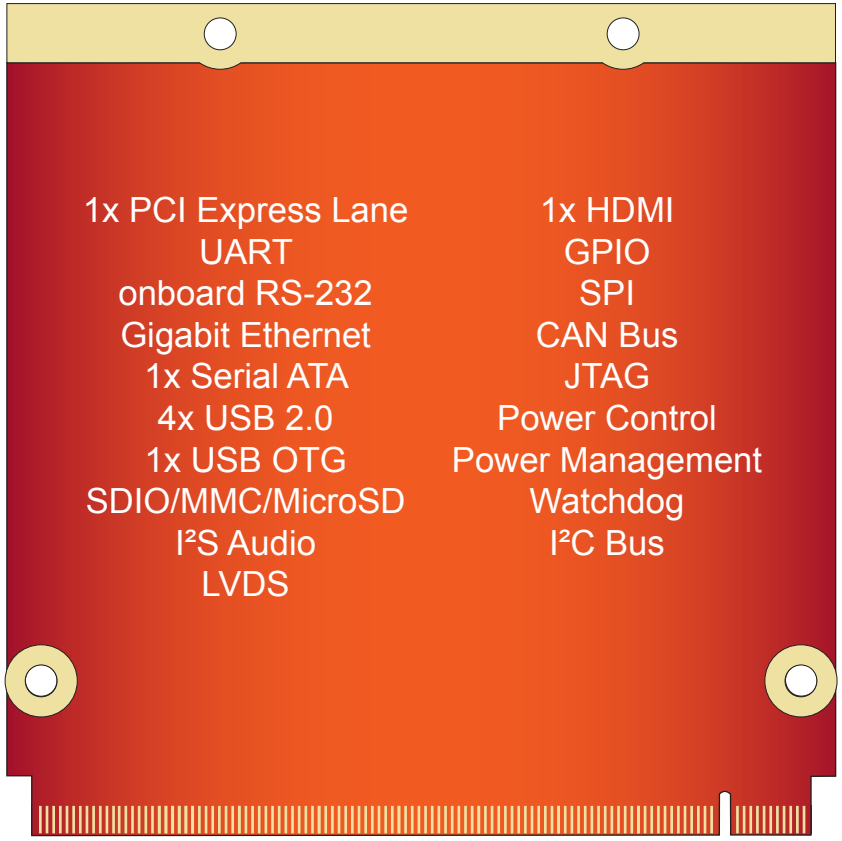
All measurements are in millimeters. Torque specification for heatspreader screws is 0.3 Nm. Mechanical system assembly mounting shall follow the valid DIN/IS0 specifications.

Caution

When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.

5 Connector Subsystems

The conga-QMX6 is based on the Qseven® standard and therefore has 115 edge fingers on the top and bottom side of the module that mate with the 230-pin card-edge MXM connector located on the carrier board. This connector provides the ability to interface the available signals of the conga-QMX6 with the carrier board peripherals.



5.1 PCI Express™

The conga-QMX6 offers one PCI Express lane. The PCIe signals are routed from the Freescale® i.MX6 processor to the PCI Express port 0 of the conga-QMX6 edge finger. These signals support PCI Express Gen. 2.0 interfaces at 5 Gb/s and are backward compatible to Gen. 1.1 interfaces at 2.5 Gb/s. Only x1 PCI Express link configuration is possible.

For more information about the PCI Express interface on the edge finger, refer to the conga-QMX6 pinout table in section 9 “Interface - Signal Descriptions and Pinout Tables.”

5.2 UART/RS-232

The conga-QMX6 offers one UART interface on the MXM connector and two RS-232 interfaces onboard. The UART offered on the MXM connector is fully featured with control signals (4 pin UART) and is connected directly to UART3 port of the Freescale® i.MX6 Cortex A9 processor.

The conga-QMX6 offers the two onboard RS-232 interfaces via a 6-pin Molex connector. This connector is provided by routing the UART2 and UART5 pins of the Freescale® i.MX6 processor to the MAXIM-3232 transceiver. The transceiver converts the Qseven® UART CMOS level (3.3V) to RS-232 voltage levels (5v) and is guaranteed to run at data rates of 250 kbps in the normal operating mode, while maintaining RS-232 output levels. With the Molex connector, you can output data to the console by using the appropriate RS-232 adapter cable.

The UART interfaces support speeds up to 4.0 Mbps and Non-Return-To-Zero encording format, RS-485 compatible 9 bit data format and IrDA compatible infrared slow data rate format.

Note

You can realize a second UART interface on the MFG interface. This implementation however requires a customized conga-QMX6 variant. Contact congatec support for more information.

To display the u-boot output to console, you need the RS232 adapter cable (PN: 48000023). See section 10.1 “UART/RS-232 Debug Port” for more information about the RS232 adapter cable and the UART pin description.

Caution

The MFG_NC4 pin is high active on the conga-QMX6 module. This means that the MFG interface on the edge connector functions as JTAG interface by default. Therefore, do not use the MFG interface for UART purposes or externally pull the MFG_NC4 pin to ground. Failure to adhere to this warning may result to back-driving which can damage the module.

If you need the UART function on the MFG interface, then you require a customized conga-QMX6. For more information, contact congatec support.

5.3 Gigabit Ethernet

The conga-QMX6 rev B.x offers Gigabit Ethernet with the integration of Qualcomm Atheros Gigabit Transceiver. This transceiver is implemented via the RGMII interface of the i.MX6 processor. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MDI0± to GBE0_MDI3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

Earlier conga-QMX6 revisions offer Gigabit Ethernet with the integration of Micrel KSZ 9031 Ethernet PHY.

Note

The theoretical maximum performance of 1 Gbps Ethernet is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For more information, consult Freescale's Errata ERR004512.

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information, refer to section 9.21 of this user's guide.

5.4 SATA

The Freescale® i.MX6 Cortex A9 processor on the conga-QMX6 supports one SATA port only. The supported signals are coupled with 10nF capacitors and then routed to conga-QMX6 edge finger. The conga-QMX6 offers this SATA port on the MXM connector. This port supports SATA I (1.5Gbps) and SATA II (3Gbps) and is compliant with SATA specification 3.0, AHCI specification 1.3 and Advanced Microcontroller Bus Architecture (AMBA) specification 2.0.

Note

SATA interface is only supported on conga-QMX6 quad and dual core variants. Solo core and dual lite variants do not support SATA.

5.5 USB 2.0

The conga-QMX6 offers five USB ports via USB 2.0 host controllers provided by the Freescale® i.MX6 Cortex A9 processor. These controllers provide high performance USB functionality that complies with USB 2.0 specification and with OTG supplement.

The offered ports comprise of one USB OTG port and four USB hosts. These four USB hosts are derived through the integration of an SMSC USB hub, and are implemented by routing the USB H1 port of the processor to the SMSC Hub. The USB OTG port (OTG client) is connected directly to the USB_OTG port of the i.MX6 processor.

The OTG client port can drop the hosting role and act as a normal USB device when conga-QMX6 is attached to another host. The direction

of OTG port depends on the USB control signal (USB_ID). If asserted high, the OTG is set to client and if low, the OTG port is set to host. All ports are capable of supporting USB 1.1 and 2.0 compliant devices.

5.6 SD/SDIO/MMC

SDIO stands for Secure Digital Input Output. Devices that support SDIO can use small devices such as SD-Card or MMC-Card flash memories. The SD/SDIO/MMC cards communicate with the host system via the Ultra Secured Digital Host Controller (uSDHC). This controller acts as a bridge by sending commands and accessing data to and from the cards. The Freescale® i.MX6 processor on the conga-QMX6 provides SD/SDIO/MMC controllers (SD1-SD4) for communicating with different SD, SDIO and MMC devices.

The conga-QMX6 offers one SDIO interface on the MXM connector via the Freescale® i.MX6 SD4 port. Two other SDIO ports provided by the Freescale® i.MX6 processor are supported onboard the conga-QMX6. These ports (SD2 and SD3) connect the onboard 4 bit micro SD and the onboard 8 bit eMMC respectively

The SDIO ports support SDIO Revision 1.1, SD Memory Card Specification Revision 3.0 and MMC Revision 4.4.

5.7 HDA/I2S/AC'97

The conga-QMX6 uses the I2S format for audio signals. These signals are derived from the Synchronous Serial Interface (SSI) of the Freescale® i.MX6 processor. The SSI is a full duplex serial port that allows communication with external devices using a variety of serial protocols. The I2S protocol is part of the protocols supported by the Freescale® i.MX6 Cortex A9 processor. The SSI supports up to 1.4 Mbps.

Note

The conga-QMX6 currently supports only I2S format.

5.8 LVDS

The LVDS Display Bridge (LDB) from the Freescale® i.MX6 Cortex A9 processor found on the conga-QMX6 offers two LVDS channels, with up to 170 Mhz pixel clock. Each channel consists of one clock pair and four data pairs. The LDB supports the flow of synchronous RGB data from the Image Processing Unit (IPU) to external display devices through LVDS interface.

The LVDS interface supports 18 bit and 24 bit dual channel. The LVDS interface also supports various resolutions but with stipulated maximum data rates. The data rates supported are as follows:

For single channel output: Up to 85 MHz per interface (e.g 1366x768 @ 60 Hz + 35 % blanking).

For dual channel output: Up to 170 MHz pixel clock (e.g 1600x1200 @ 60Hz + 35 % blanking)

The LVDS ports support the following configurations:

- One single channel output
- One dual channel output: single input split to two output channels
- Two identical outputs: single input sent to both output channels
- Two independent outputs: two inputs sent, each to a different output channel

Note

The LVDS interface can be used either as a single channel or as a dual channel. It is also possible to use the LVDS interface as two independent single LVDS channels. To do this, it is recommended to configure the LVDS display in the bootloader.

Three independent displays are possible when connected as two single LVDS channel and one HDMI interface.

5.9 HDMI

High-Definition Multimedia Interface (HDMI) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video.

The conga-QMX6 provides HDMI connection directly from the Freescale® i.MX6 processor. Video data is provided through three differential TMDS data pairs (TMDS_LANE0± to TMDS_LANE2±) and one differential clock pair (TMDS_CLK±). In addition, the conga-QMX6 includes one standard I2C interface (I2C2_SDA and I2C2_SCL) for configuring and testing the HDMI 3D Tx PHY and a pin (DP_HDMI_HPD) for HDMI hot plug detection support.

5.10 LPC/GPIO

The conga-QMX6 does not support the Low Pin Count (LPC) signals, instead eight GPIO pins shared with the LPC pins according to Qseven specification 2.0 are supported.

The General Purpose Input/Output pins can be configured as inputs or outputs. When configured as output, it is possible to write to an internal register to control the state driven on the output pin. When configured as input, the input state can be detected by reading the status of an internal register. To select the GPIO mode, configure the IOMUX.

5.11 SPI

The Freescale® i.MX6 processor provides Enhanced Configurable Serial Peripheral Interfaces (ECSPIs) capable of up to 66 Mbps write speed and 31 Mbps read speed. The ECSPI interfaces offer full-duplex, synchronous serial interface with maximum operation frequency up to the reference clock frequency. It can be configured to support Master/Slave modes and four chip selects to support multiple peripherals.

The conga-QMX6 offers one SPI interface on the edge finger connector. Another SPI interface from the Freescale® i.MX6 processor is connected to the 32 Mbit SPI Flash memory onboard the conga-QMX6. The Freescale® i.MX6 processor is programmed to boot from the bootloader contained in the SPI flash memory.

5.12 CAN Bus

The conga-QMX6 supports CAN bus. The CAN controller performs communication in accordance with the CAN Protocol Version 2.0B Active1 (standard format and extended format). The bit rate can be programmed to a maximum of 1 Mbit/s, based on the technology used. To connect the CAN controller module to the CAN bus, it is necessary to add transceiver hardware. A complete description of the CAN controller registers and functionality is beyond the scope of this user's guide. Consult Freescale's i.MX6 processor reference manual for additional information about this interface.

5.13 Manufacturing/JTAG Interface

The manufacturing signals defined in Qseven Specification 2.0 are reserved for either manufacturing or debugging purposes. The conga-QMX6 offers this interface as a 10-pin JTAG interface, for debugging purposes. This interface is connected to the JTAG controller of the Freescale® i.MX6 processor. The JTAG control fuses are used to allow or disallow JTAG access to secured resources.

Note

For compatible JTAG adapters, contact the congatec support team or order the Nit6X_JTAG from Boundary Devices.

5.14 Power Control

PWGIN (pin 26) can be connected to an external power good circuit or it may also be utilized as a manual reset input. To use PWGIN as a manual reset input, the pin must be grounded through the use of a momentary-contact push-button switch. When external circuitry asserts this signal, it is necessary that an open-drain driver drives this signal causing it to be held low for a minimum of 15ms to initiate a reset. Using this input is optional.

For more information, see the note below.

SUS_S3#

The SUS_S3# (pin 18) signal shuts off power to all runtime system components that are not maintained during suspend mode. This signal is an output signal and is connected to the Power Management Integrated Circuit (PMIC). See section 9.16 “Power Management” for more information.

PWRBTN#

When using ATX-style power supplies, PWRBTN# (pin 20) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off.

Note

The conga-QMX6 boots up immediately power is applied to the module’s +5v input rail. To shutdown the system, use the the linux command “poweroff”. Depending on the operating system, the shutdown can also be performed by pressing the power button. If the system is in shutdown or standby state, pressing the power button restores the system back to full-on state. When the chip main power supply is Off, a button press greater in duration than 750 ms asserts an output signal to request power from a power IC to power up the SoC.

If it’s desired to keep the system switched off even when the +5V input power rail is initially powered on (ATX-style), an external logic has to be used that prevents the system from booting by means of the power good signal (PWGIN). It is the responsibility of the external logic to release the PWGIN signal, when the desired event (e.g. pressing the power button) occurs.

Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-QMX6. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. When designing a power supply for a conga-QMX6 application, a carrier board designer should be aware of the important information below:

- It has been noticed that on some occasions, problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn’t arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document “ATX12V Power Supply Design Guide V2.2”.

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush-current on the conga-QMX6 VCC_5V_SB power rail can go up as high as 2.3A for a maximum of 100µS. Sufficient decoupling capacitance must be implemented to ensure proper power-up sequencing.

The maximum peak-current on the conga-QMX6 VCC (5V) power rail can be as high as 3.0A. This requires that the power supply be properly dimensioned.

Note

For more information about power control event signals refer to the Qseven® specification.

5.15 Power Management

Onboard the conga-QMX6 is a 14 channel configurable Power Management Integrated Circuit (PMIC). The PMIC provides a cost effective programmable power management solution for a wide range of applications. This high efficiency, configurable power management IC is designed to work seamlessly with Freescale® processors. The Freescale® i.MX6 cortex A9 processor uses advanced integration Power Management Unit (PMU) to reduce supply connections. The PMIC complements the processor's internal regulators in providing a complete and simple way to supply voltage domain with different voltages when needed.

The PMIC features four bulk regulators (up to six independent outputs), one boost regulator, six general purpose LDOs, one switch/LDO combination and a DDR voltage reference to supply voltages for the application processor and peripheral devices.

With integrated memory power, RTC supply and additional bulk and linear regulators to power system peripherals, multiple point of power supply across the PCB is drastically reduced.

5.16 Watchdog

The watchdog timer (WDOG) protects against system failures by providing a method of escaping from unexpected events or programming errors. The software must periodically service the watchdog timer once the WDOG is activated. Without the servicing, the timer times out.

The Freescale® i.MX6 processor on the conga-QMX6 offers two watchdog timers - a watchdog timer integrated within the ARM Cortex A9 platform and a TrustZone watchdog timer.

5.17 I2C Bus

The I2C bus is suitable for applications requiring occasional communications over a short distance between many devices. The I2C interfaces offered by the Freescale® i.MX6 processor support up to 400 kbps, depending on pin loading and timing characteristics

The conga-QMX6 offers three I2C interfaces (I2C1, I2C2 and I2C3) on the Qseven edge connector. The I2C2 and I2C3 buses on the edge connector are shared with some onboard devices - I2C3 is shared with LVDS and RTC while I2C2 is shared with camera interface and HDMI. The I2C1 bus is routed directly without sharing on the edge connector.

Note

On the conga-QMX6 revision B.x and later, we implemented a multiplexer on the I2C2 interface. The multiplexer separates the PMIC functions from other devices (camera, HDMI) that share the bus. Due to this implementation, the user needs to download the latest kernel from git.congatec.com/public or at least ensure the congatec I2C multiplexer patches (CGT000031, CGT000032) are applied to the desired kernel, to achieve proper behaviour.

The I2C3 is also available on the SMB Bus signals (pin 60 and 62) of the Qseven edge connector.

6 Additional Features

6.1 High Assurance Boot (HAB)

The High Assurance Boot is a software library executed in internal ROM on the Freescale® processor at boot time, which among other things, authenticates software in external memory by verifying digital signatures. The HAB enables the ROM to authenticate software which executes immediately after ROM, by using digital signatures. This software is usually a bootloader. The High Assurance Boot component of the ROM protects against the potential threat of attackers modifying areas of code or data in programmable memory to make it behave in an incorrect manner.

6.2 Dedicated Hardware Accelerators

The Freescale® i.MX6 processor uses dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption while having the CPU core relatively free for performing other tasks. The hardware accelerators available in the processor are VPU, IPUv3H, 3D GPU, 2D GPU, OpenVG 1.1 GPU and Asynchronous Sample Rate Converter (ASRC).

6.3 Power Management

The Freescale® i.MX6 processor integrates power management functions to simplify system power management requirements. The processor provides power management units for offering power to various Soc domains. Temperature sensor for monitoring the die temperature is also provided.

Dynamic Voltage and Frequency Scaling techniques, software state retention, power gating and various levels of system power mode are supported. The use of simple and low-cost power regulators in place of complicated external power management ICs reduces system design cost.

6.4 Dynamic Voltage and Frequency Scaling

Dynamic Voltage and Frequency Scaling is a power management technique used in changing the clock frequency and/or the operating voltage of a processor based on system performance requirements at any point in time. This scaling is normally carried out during less demanding periods of nominal run speed. In General, it helps in balancing the performance demands of processor with the high amount of power needed to satisfy those demands.

6.5 Smart Speed Technology

The Freescale's Smart Speed Technology with enhanced Cycles Per Instruction (eCPI) determines the speed of the processor by the set of tasks to be performed instead of the clock speed. The set of tasks determines the execution units needed to make sure the system work more efficiently. This ensures that the system provides enough performance without wasting resources.

With the Smart Speed Technology, several execution units work in parallel, thereby providing higher processor speed at lower power consumption. System parallelism is accomplished via the Smart Speed crossbar switch that nearly eliminates wait states. This results in improved processor performance without power consumption penalty associated with higher operating frequencies.

By employing Smart Speed Technology, portable devices can run longer, retain smaller form factors and support more innovative applications without substantially increasing the battery power.

6.6 Suspend Mode

The Suspend Mode feature is available on the conga-QMX6.

7 ARM Technologies

7.1 Media Processing Engine (MPE-NEON)

The Media Processing Engine (MPE-NEON) is a single instruction multiple data (SIMD) instruction set that provides flexible and powerful acceleration for media and signal processing applications. Support for a wide range of multimedia codecs with fewer cycles helps in enhancing user experience. NEON is used for multimedia data processing.

7.2 Jazelle DBX

The Jazelle is an instruction set that introduces technological infrastructure for running java codes faster than the software based java virtual machine. The Jazelle DBX (Direct Bytecode eXecution) enabled cores execute the majority of Java bytecodes in hardware. No modification is required in the application code to take advantage of this technology. To configure and turn on the Jazelle DBX, the software support code needs to be integrated into a Java Virtual Machine (JVM). Contact ARM for further information on how to obtain the software support code.

7.3 TrustZone

The ARM TrustZone technology is a security extension that provides additional dedicated security to a System on Chip (SoC). This technology aims to provide a framework that enables a device to counter many of the specific threats that it will experience. The security of the system is achieved by partitioning all of the SoC's hardware and software resources so that they exist in one of two worlds - the secure world (more trusted) and the normal world (less trusted). The memory and peripherals are then made aware of the operating world of the core and may use this to provide access control to secrets and code in the device.

7.4 Floating Point Unit

The Floating Point Unit (FPU) provides significant acceleration for both single and double precision scalar Floating-Point operations. It provides industry leading image processing, graphics and scientific computation capabilities. The FPU provides an optimized solution in performance, power and area for embedded applications and high performance for general purpose applications.

8 conga Tech Notes

The conga-QMX6 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

8.1 Freescale® i.MX6 Processor Features

8.1.1 Temperature Monitor (TEMPMON)

The Freescale® i.MX6 Cortex A9 processors have a temperature sensor module that implements a temperature sensor/conversion function based on a temperature-dependent voltage to time conversion.

The module features an alarm function that can raise an interrupt signal if the temperature is above a specified threshold. A self repeating mode can also be programmed which executes a temperature sensing operation based on a programmed delay.

Software can use this module to monitor the on-die temperature and take appropriate actions such as throttling back the core frequency when a temperature interrupt is set.

During normal system operation, software can use the temperature sensor counter output in conjunction with the fused temperature calibration data to determine the on-die operational temperature or to set an over-temperature interrupt alarm to within a couple of degree centigrade.

8.2 Thermal Management

To meet low power design requirement while maintaining a high performance operation, the Freescale® iMX6 incorporated several low power design techniques. Even with these techniques, it is vital to manage the heat dissipation of the module in accordance with internal and external conditions.

The conga-QMX6 employs basically two types of thermal management strategies:

Active Cooling

During this cooling policy, the operating system turns the fan on/off. Though the active thermal management technique provides better heat dissipation and lower thermal resistances, the cooling solutions are however expensive and have large form factors.

Passive Cooling

The passive cooling policy employs the technique of enhancing conduction and natural convection. This passive thermal management procedure provides cost effective cooling solutions up to certain power levels without introducing reliability concerns. Some of these techniques typically used are thermal gap fillers, heatspreaders and heat shields.

8.3 Audio Mux

Audio Mux (AUDMUX) is one of the modules found in the audio subsystem of the Freescale® i.MX6 processor. It provides flexible programmable routing of the on-chip serial interfaces to and from off-chip devices. The AUDMUX includes internal port that connect to the processor serial interfaces and external ports that connect to off-chip audio devices. Connection is established by configuring the appropriate host and peripheral ports. Though controlled by ARM, the AUDMUX can route data even when the ARM is in a low-power mode.

8.4 LVDS Bridge

The LVDS Bridge (LDB) supports the flow of synchronous RGB data from the Image Processing Unit to external devices through LVDS interface. This support includes synchronization and control capabilities, connectivitity to relevant devices as well as proper data arrangement as required by the external display receiver and by LVDS display standards.

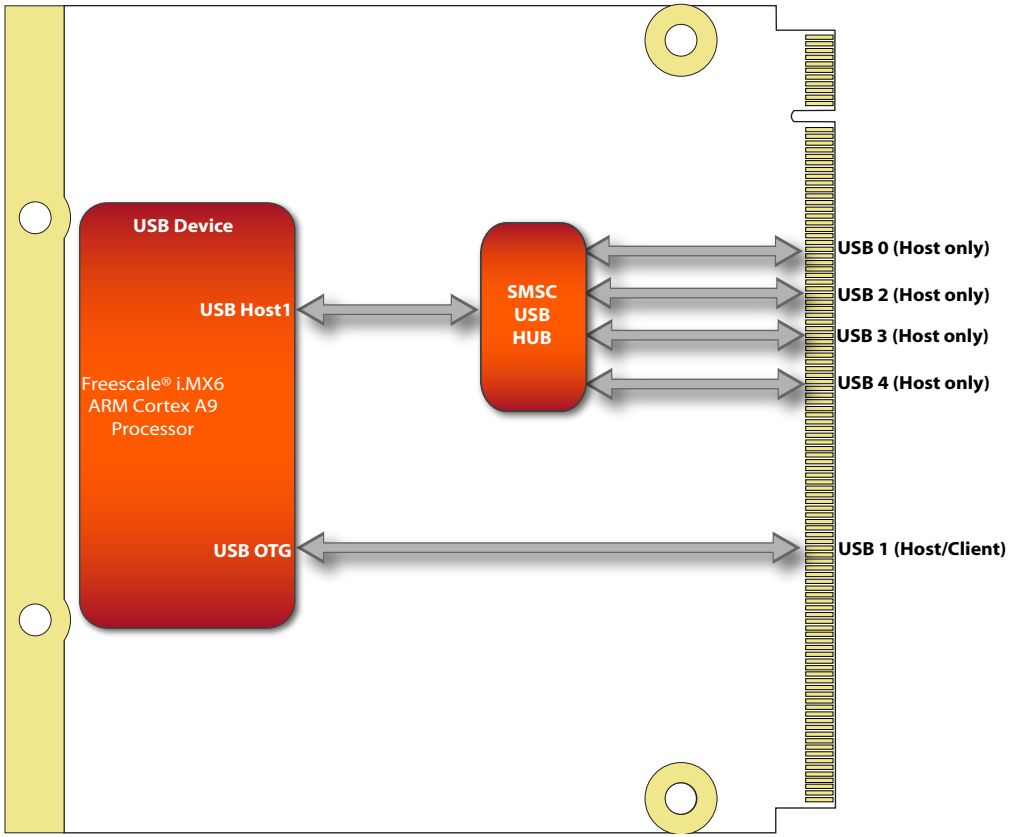
8.5 USB Port Connections

The conga-QMX6 offers a total of 5 USB ports (one USB OTG port and four Host-only ports). The four Host-only ports found on the conga-QMX6 are implemented by routing one Host-only port (USB H1) from the Freescale® i.MX6 processor to the conga-QMX6 edge finger via a SMSC USB Hub.

The USB_OTG port (OTG client) of the conga-QMX6 is routed directly to the USB_OTG port of the i.MX6 processor. This port can drop the hosting role and act as a normal USB device when conga-QMX6 is attached to another host. It is also used as a downstream and upstream port while the Host-only cores are used as downstream ports.

For more information refer to the conga-QMX6 USB routing diagram shown below:

conga-QMX6 USB Routing Diagram



9 Interface - Signal Descriptions and Pinout Tables

The following section describes the signals found on Qseven® module's edge fingers and the interfaces implemented on the conga-QMX6.

Table 3 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a Qseven® module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Not all the signals described in this section are available on all conga-QMX6 variants. Use the article number of the module and refer to the options table on page 8 to determine the options available on the module.

Table 4 Signal Tables Terminology Descriptions

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PP	Push Pull
I/O	Bi-directional Input/Output Pin
3.3VSB	3.3V tolerant active in standby state
P	Power Input
NA	Not applicable
NC	Not Connected
PCIE	PCI Express differential pair signals. In compliance with the PCI Express Base Specification 1.0a.
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet Specification.
USB	Universal Serial Bus differential pair signals. In compliance with the Universal Serial Bus Specification 2.0
SATA	Serial Advanced Technology Attachment differential pair signals. In compliance with the Serial ATA High Speed Serialized AT Attachment Specification 1.0a.
SPI	Serial Peripheral Interface bus is a synchronous serial data link that operates in full duplex mode.
CAN	Controller Area Network bus is a vehicle bus standard that allows microcontrollers and devices to communicate with each other within a vehicle without a host computer.
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

Table 5 Edge Finger Pinout

Pin	Signal	Pin	Signal
1	GND	2	GND
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	GBE_LINK#	14	GBE_ACT#
15	GBE_CTREF (*)	16	SUS_S5#
17	WAKE#	18	SUS_S3#
19	SUS_STAT#*	20	PWRBTN#
21	SLP_BTN#	22	LID_BTN#
23	GND	24	GND
25	GND	26	PWGIN
27	BATLOW#	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+(*)
31	SATA0_TX-	32	SATA1_TX- (*)
33	SATA_ACT#	34	GND
35	SATA0_RX+	36	SATA1_RX+ (*)
37	SATA0_RX-	38	SATA1_RX- (*)
39	GND	40	GND
41	BIOS_DISABLE# / BOOT_ALT#	42	SDIO_CLK
43	SDIO_CD#	44	SDIO_LED
45	SDIO_CMD	46	SDIO_WP
47	SDIO_PWR#	48	SDIO_DAT1
49	SDIO_DAT0	50	SDIO_DAT3
51	SDIO_DAT2	52	SDIO_DAT5
53	SDIO_DAT4	54	SDIO_DAT7
55	SDIO_DAT6	56	RESERVED
57	GND	58	GND
59	HDA_SYNC / I2S_WS	60	SMB_CLK / GP1_I2C_CLK
61	HDA_RST# / I2S_RST#	62	SMB_DAT / GP1_I2C_DAT
63	HDA_BITCLK / I2S_CLK	64	SMB_ALERT#
65	HDA_SDI / I2S_SDI	66	GP0_I2C_CLK
67	HDA_SDO / I2S_SDO	68	GP0_I2C_DAT
69	THRM#	70	WDTRIG#
71	THRMTRIP#	72	WDOUT
73	GND	74	GND
75	USB_P7- / USB_SSTX0-	76	USB_P6- / USB_SSRX0-
77	USB_P7+ / USB_SSTX0+	78	USB_P6+ / USB_SSRX0+

Pin	Signal	Pin	Signal
79	USB_6_7_OC#	80	USB_4_5_OC#
81	USB_P5- / USB_SSTX1-	82	USB_P4- / USB_SSRX1-
83	USB_P5+ / USB_SSTX1+	84	USB_P4+ / USB_SSRX1+
85	USB_2_3_OC#	86	USB_0_1_OC#
87	USB_P3-	88	USB_P2-
89	USB_P3+	90	USB_P2+
91	USB_CC	92	USB_ID
93	USB_P1-	94	USB_P0-
95	USB_P1+	96	USB_P0+
97	GND	98	GND
99	eDP0_TX0+ / LVDS_A0+	100	eDP1_TX0+ / LVDS_B0+
101	eDP0_TX0- / LVDS_A0-	102	eDP1_TX0- / LVDS_B0-
103	eDP0_TX1+ / LVDS_A1+	104	eDP1_TX1+ / LVDS_B1+
105	eDP0_TX1- / LVDS_A1-	106	eDP1_TX1- / LVDS_B1-
107	eDP0_TX2+ / LVDS_A2+	108	eDP1_TX2+ / LVDS_B2+
109	eDP0_TX2- / LVDS_A2-	110	eDP1_TX2- / LVDS_B2-
111	LVDS_PPEN	112	LVDS_BLEN
113	eDP0_TX3+ / LVDS_A3+	114	eDP1_TX3+ / LVDS_B3+
115	eDP0_TX3- / LVDS_A3-	116	eDP1_TX3- / LVDS_B3-
117	GND	118	GND
119	eDP0_AUX+ / LVDS_A_CLK+	120	eDP1_AUX+ / LVDS_B_CLK+
121	eDP0_AUX- / LVDS_A_CLK-	122	eDP1_AUX- / LVDS_B_CLK-
123	LVDS_BLT_CTRL /GP_PWM_OUT0	124	GP_1-Wire_Bus
125	GP2_I2C_DAT / LVDS_DID_DAT	126	eDP0_HPD# / LVDS_BLC_DAT
127	GP2_I2C_CLK / LVDS_DID_CLK	128	eDP1_HPD# / LVDS_BLC_CLK
129	CAN0_TX	130	CAN0_RX
131	DP_LANE3+ / TMDS_CLK+	132	RSVD (Differential Pair)
133	DP_LANE3- / TMDS_CLK-	134	RSVD (Differential Pair)
135	GND	136	GND
137	DP_LANE1+ / TMDS_LANE1+	138	DP_AUX+
139	DP_LANE1- / TMDS_LANE1-	140	DP_AUX-
141	GND	142	GND
143	DP_LANE2+ / TMDS_LANE0+	144	RSVD (Differential Pair)
145	DP_LANE2- / TMDS_LANE0-	146	RSVD (Differential Pair)
147	GND	148	GND
149	DP_LANE0+ / TMDS_LANE2+	150	HDMI_CTRL_DAT
151	DP_LANE0- / TMDS_LANE2-	152	HDMI_CTRL_CLK
153	DP_HDMI_HPD#	154	RSVD
155	PCIE_CLK_REF+	156	PCIE_WAKE#
157	PCIE_CLK_REF-	158	PCIE_RST#

Pin	Signal	Pin	Signal
159	GND	160	GND
161	PCIE3_TX+	162	PCIE3_RX+
163	PCIE3_TX-	164	PCIE3_RX-
165	GND	166	GND
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_TX-	170	PCIE2_RX-
171	UART0_TX	172	UART0_RTS#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_TX-	176	PCIE1_RX-
177	UART0_RX	178	UART0_CTS#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_TX-	182	PCIE0_RX-
183	GND	184	GND
185	LPC_AD0 / GPIO0	186	LPC_AD1 / GPIO1
187	LPC_AD2 / GPIO2	188	LPC_AD3 / GPIO3
189	LPC_CLK / GPIO4	190	LPC_FRAME# / GPIO5
191	SERIRQ / GPIO6	192	LPC_LDRQ# / GPIO7
193	VCC_RTC	194	SPKR / GP_PWM_OUT2
195	FAN_TACHOIN / GP_TIMER_IN	196	FAN_PWMOUT / GP_PWM_OUT1
197	GND	198	GND
199	SPI_MOSI	200	SPI_CS0#
201	SPI_MISO	202	SPI_CS1#
203	SPI_SCK	204	MFG_NC4
205	VCC_5V_SB	206	VCC_5V_SB
207	MFG_NC0	208	MFG_NC2
209	MFG_NC1	210	MFG_NC3
211	VCC	212	VCC
213	VCC	214	VCC
215	VCC	216	VCC
217	VCC	218	VCC
219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

Note

The conga-QMX6 does not support the signals marked with asterisk symbol (*).

9.1 PCI Express™

Table 6 PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.0a.
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.0a.
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	I PCIE		Not supported.
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Not supported.
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	I PCIE		Not supported.
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Not supported.
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	I PCIE		Not supported.
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Not supported.
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock Signals for Lanes 0 to 3.	O PCIE		
PCIE_WAKE#	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I 3.3VSB	PU 1k 3.3VSB	connected to GPIO
PCIE_RST#	158	Reset Signal for external devices.	O 3.3V		

9.2 UART

Table 7 UART Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
UART0_TX	171	Serial Data Transmitter	O 3.3V		UART3_TX signal from Processor
UART0_RX	177	Serial Data Reciever	I 3.3V		UART3_RX signal from Processor
UART0_CTS#	178	Handshake signal, ready to send data	I 3.3V		UART3_CTS# signal from Processor
UART0_RTS#	172	Handshake signal, ready to receive data	O 3.3V		UART3_RTS# signal from Processor

9.3 Gigabit Ethernet

Table 8 Ethernet Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GBE_MDI0+ GBE_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI1+ GBE_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI2+ GBE_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI3+ GBE_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_CTREF	15	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		Not Supported
GBE_LINK#	13	Ethernet controller 0 link indicator, active low.	O 3.3V PP	PD 1k	GBE0_LINK# is a bootstrap signal (see note below)
GBE_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3V PP	PU 4k99 2,5VSB	Not Supported. Internally connected to GBE_ACT#. GBE0_LINK100# is a bootstrap signal (see note below)
GBE_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3V PP	PD 1k	Not Supported. Internally connected to GBE_LINK#. GBE0_LINK1000# is a bootstrap signal (see note below)
GBE_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 3.3V PP	PU 4k99 2,5VSB	GBE0_ACT# is a bootstrap signal (see note below)

Note

The theoretical maximum performance of 1 Gbps Ethernet is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For more information, consult Freescale's Errata ERR004512.

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module.

For more information refer to section 9.21 of this user's guide.

9.4 SATA

Table 9 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	I SATA		Not supported
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Not supported
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V		Not supported

9.5 USB 2.0

Table 10 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_P0+ USB_P0-	96 94	Universal Serial Bus Port 0 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P1+ USB_P1-	95 93	Universal Serial Bus Port 1 differential pair. If USB_ID is LOW (default) = USB Host If USB_ID is tied HIGH = USB device (Client)	I/O		If USB_ID is LOW (default) = USB 2.0 compliant Host. Backwards compatible to USB 1.1 If USB_ID is HIGH = USB 2.0 Client. Backwards compatible to USB 1.1
USB_P2+ USB_P2-	90 88	Universal Serial Bus Port 2 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P3+ USB_P3-	89 87	Universal Serial Bus Port 3 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P4+ USB_P4- USB_SSRX1+ USB_SSRX1-	84 82	Universal Serial Bus Port 4 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path.	I/O I		USB 2.0 compliant. Backwards compatible to USB 1.1. No USB 3.0 available
USB_P5+ USB_P5- USB_SSTX1+ USB_SSTX1-	83 81	Universal Serial Bus Port 5 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path	I/O O		Not supported

USB_P6+ USB_P6- USB_SSRX0+ USB_SSRX0-	78 76	Universal Serial Bus Port 6 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path	I/O I		Not supported
USB_P7+ USB_P7- USB_SSTX0+ USB_SSTX0-	77 75	Universal Serial Bus Port 7 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path	I/O O		Not supported
USB_0_1_OC#	86	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	I 3.3VSB	PU 10k 3.3V	
USB_2_3_OC#	85	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	I 3.3VSB	PU 10k 3.3V	
USB_4_5_OC#	80	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	I 3.3VSB	PU 10k 3.3V	
USB_6_7_OC#	79	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	I 3.3VSB	PU 10k 3.3VSB	Not supported
USB_ID	92	USB ID pin. Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the chip will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.	I 3.3VSB	PU 10k 3.3V	Connected to GPIO
USB_CC	91	USB Client Connect pin. If USB Port 1 is configured for client mode then an externally connected USB host should set this signal to high-active in order to properly make the connection with the module's internal USB client controller. If the external USB host is disconnected, this signal should be set to low-active in order to inform the USB client controller that the external host has been disconnected. A level shifter/protection circuitry should be implemented on the carrier board for this signal.	I 3.3VSB	PD 10k GND	

9.6 SDIO/MMC

Table 11 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	43	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I/O 3.3V	PU 10k 3.3V	
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	O 3.3V		
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O 3.3V OD/PP	PU 10k 3.3V	
SDIO_LED	44	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	O 3.3V	PU 10k 3.3V	
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I/O 3.3V	PU 10k 3.3V	
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/ MMC card device.	O 3.3V		Connected to GPIO
SDIO_DAT0 SDIO_DAT1 SDIO_DAT2 SDIO_DAT3 SDIO_DAT4 SDIO_DAT5 SDIO_DAT6 SDIO_DAT7	49 48 51 50 53 52 55 54	SDIO Data lines. These signals operate in push-pull mode.	I/O 3.3V PP		

9.7 HDA /I2S /SPDIF

Table 12 HDA/AC'97 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST# I2S_RST#	61	HD Audio/AC'97 Codec Reset. Multiplexed with I2S Codec Reset.	O 3.3V		Connected to GPIO.
HDA_SYNC I2S_WS	59	Serial Bus Synchronization. Multiplexed with I2S Word Select from Codec.	O 3.3V		
HDA_BITCLK I2S_CLK	63	HD Audio/AC'97 24 MHz Serial Bit Clock from Codec. Multiplexed with I2S Serial Data Clock from Codec.	O 3.3V		
HDA_SDO I2S_SDO	67	HD Audio/AC'97 Serial Data Output to Codec. Multiplexed with I2S Serial Data Output from Codec.	O 3.3V		
HDA_SDI I2S_SDI	65	HD Audio/AC'97 Serial Data Input from Codec. Multiplexed with I2S Serial Data Input from Codec.	I 3.3V		

Note

The conga-QMX6 currently supports only I2S format.

9.8 LVDS

Table 13 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_PPEN	111	Controls panel power enable.	O 3.3V		
LVDS_BLEN	112	Controls panel Backlight enable.	O 3.3V		
LVDS_BLT_CTRL /GP_PWM_OUT0	123	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
LVDS_A0+ LVDS_A0- eDP0_TX0+ eDP0_TX0-	99 101	LVDS primary channel differential pair 0. Display Port primary channel differential pair 0.	O LVDS		
LVDS_A1+ LVDS_A1- eDP0_TX1+ eDP0_TX1-	103 105	LVDS primary channel differential pair 1. Display Port primary channel differential pair 1.	O LVDS		
LVDS_A2+ LVDS_A2- eDP0_TX2+ eDP0_TX2-	107 109	LVDS primary channel differential pair 2. Display Port primary channel differential pair 2.	O LVDS		

LVDS_A3+ LVDS_A3- eDP0_TX3+ eDP0_TX3-	113 115	LVDS primary channel differential pair 3. Display Port primary channel differential pair 3.	O LVDS		
LVDS_A_CLK+ LVDS_A_CLK- eDP0_AUX+ eDP0_AUX-	119 121	LVDS primary channel differential pair clock lines. Display Port primary auxiliary channel.	O LVDS		
LVDS_B0+ LVDS_B0- eDP1_TX0+ eDP1_TX0-	100 102	LVDS secondary channel differential pair 0. Display Port secondary channel differential pair 0.	O LVDS		
LVDS_B1+ LVDS_B1- eDP1_TX1+ eDP1_TX1-	104 106	LVDS secondary channel differential pair 1. Display Port secondary channel differential pair 1.	O LVDS		
LVDS_B2+ LVDS_B2- eDP1_TX2+ eDP1_TX2-	108 110	LVDS secondary channel differential pair 2. Display Port secondary channel differential pair 2.	O LVDS		
LVDS_B3+ LVDS_B3- eDP1_TX3+ eDP1_TX3-	114 116	LVDS secondary channel differential pair 3. Display Port secondary channel differential pair 3.	O LVDS		
LVDS_B_CLK+ LVDS_B_CLK- eDP1_AUX+ eDP1_AUX-	120 122	LVDS secondary channel differential pair clock lines. Display Port secondary auxiliary channel.	O LVDS		
LVDS_DID_CLK /GP2_I2C_CLK	127	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used, it can be as General Purpose I²C bus clock line.	I/O 3.3V OD	PU 4k7 3.3V	
LVDS_DID_DAT /GP2_I2C_DAT	125	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus data line.	I/O 3.3V OD	PU 4k7 3.3V	
LVDS_BLC_CLK eDP1_HPD#	128	Control clock signal for external SSC clock chip. If the primary functionality is not used, it can be used as an emedded DisplayPort secondary Hotplug detection.	I/O 3.3V OD	PU 4k7 3.3V	Not supported
LVDS_BLC_DAT eDP0_HPD#	126	Control data signal for external SSC clock chip. If the primary functionality is not used, it can be used as an embedded DisplayPort primary Hotplug detection.	I/O 3.3V OD	PU 4k7 3.3V	Not supported

Note

The LVDS interface can be used either as a single channel or as a dual channel. It is also possible to use the LVDS interface as two independent single LVDS channels. To do this, it is recommended to configure the LVDS display in the bootloader.

9.9 DisplayPort

Table 14 DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP_LANE3+ DP_LANE3-	131 133	DisplayPort differential pair lines lane 3 (Shared with TMDS_CLK+ and TMDS_CLK-)	O PCIE		DisplayPort interface not supported
DP_LANE2+ DP_LANE2-	143 145	DisplayPort differential pair lines lane 2 (Shared with TMDS_LANE0+ and TMDS_LANE0-)	O PCIE		DisplayPort interface not supported
DP_LANE1+ DP_LANE1-	137 139	DisplayPort differential pair lines lane 1 (Shared with TMDS_LANE1+ and TMDS_LANE1-)	O PCIE		DisplayPort interface not supported
DP_LANE0+ DP_LANE0-	149 151	DisplayPort differential pair lines lane 0 (Shared with TMDS_LANE2+ and TMDS_LANE2-)	O PCIE		DisplayPort interface not supported
DP_AUX+ DP_AUX-	138 140	Auxiliary channel used for link management and device control. Differential pair lines.	I/O PCIE		DisplayPort interface not supported
DP_HDMI_ HPD#	154	Hot plug detection signal that serves as an interrupt request.	I 3.3V		DisplayPort interface not supported

Note

The conga-QMX6 does not offer DisplayPort interface because the interface is not supported by the Freescale® i.MX6 processor.

9.10 HDMI

Table 15 HDMI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS_CLK+ TMDS_CLK-	131 133	TMDS differential pair clock lines.	O TMDS		HDMI interface
TMDS_LANE0+ TMDS_LANE0-	143 145	TMDS differential pair lines lane 0.	O TMDS		HDMI interface
TMDS_LANE1+ TMDS_LANE1-	137 139	TMDS differential pair lines lane 1.	O TMDS		HDMI interface
TMDS_LANE2+ TMDS_LANE2-	149 151	TMDS differential pair lines lane 2.	O TMDS		HDMI interface
HDMI_CTRL_CLK	152	DDC based control signal (clock) for HDMI device.	I/O 3.3V OD	PU 4k7 3.3V	HDMI interface.
HDMI_CTRL_DAT	150	DDC based control signal (data) for HDMI device.	I/O 3.3V OD	PU 4k7 3.3V	HDMI interface. .
DP_HDMI_HPD#	153	Hot plug detection signal that serves as an interrupt request.	I 3.3V	PD 100k	HDMI interface

Note

On the conga-QMX6, only the HDMI interface supports the Transition Minimized Differential Signaling (TMDS)

9.11 LPC/GPIO

Table 16 LPC/GPIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD0 GPIO0	185	Multiplexed Command, Address and Data (LPC_AD[0..3]) shared with General Purpose Input/Output [0..3]	I/O 3.3V		Shared with GPIO0
LPC_AD1 GPIO1	186				Shared with GPIO1
LPC_AD2 GPIO2	187				Shared with GPIO2
LPC_AD3 GPIO3	188				Shared with GPIO3
LPC_FRAME# GPIO5	190	LPC frame indicates the start of a new cycle or the termination of a broken cycle. Shared with General Purpose Input/Output 5	I/O 3.3V		Shared with GPIO5
LPC_LDRQ# GPIO7	192	LPC DMA request. General Purpose Input/Output 7	I/O 3.3V		Shared with GPIO7
LPC_CLK GPIO4	189	LPC clock shared with General Purpose Input/Output 4	I/O 3.3V		The LPC clock output operates at 1/4th of FSB frequency. By default, the LPC clock is only active when LPC bus transfers occur. Because of this behavior, LPC clock must be routed directly to the bus device; they cannot go through a clock buffer or other circuit that could delay the signal going to the end device.
SERIRQ GPIO6	191	Serialized Interrupt. General Purpose Input/Output 6	I/O 3.3V	PU 10k 3.3V	Shared with GPIO6

Note

The eight LPC pins are configured by default as GPIO's. Additional eight GPIO pins can be achieved by configuring SDIO pins as GPIO. This can be programmed in the bootloader and in the kernel.

The conga-QMX6 does not support LPC interface.

9.12 SPI

Table 17 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_MOSI	199	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	O 3.3V		
SPI_MISO	201	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	I 3.3V		
SPI_SCK	203	SPI clock output.	O 3.3V		
SPI_CS0#	200	SPI chip select 0 output.	O 3.3V		
SPI_CS1#	202	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	O 3.3V		

9.13 CAN Bus

Table 18 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	129	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	O 3.3V		
CAN0_RX	130	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	I 3.3V		

9.14 Input Power

Table 19 Input Power Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	211-230	Power Supply +5VDC ±5%.	P		
VCC_5V_SB	205-206	Standby Power Supply +5VDC ±5%.	P		
VCC_RTC	193	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V).	P		

GND	1, 2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198	Power Ground.	P		

9.15 Power Control

Table 20 Power Control Signal Descriptions

Signal	Pin #	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	26	High active input for the Qseven® module indicates that power from the power supply is ready.	I 5V	PU 10k 5V	
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge.	I 3.3VSB	PU 10k 3.3V	

9.16 Power Management

Table 21 Power Management Signal Descriptions

Signal	Pin #	Description of Power Management signals	I/O	PU/PD	Comment
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module.	I 3.3V		
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	I 3.3VSB		Connected to GPIO
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	I 3.3VSB		
SUS_STAT#	19	Suspend Status: indicates that the system will be entering a low power state soon.			Not supported
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	O 3.3VSB		Connected to PMIC
SUS_S5#	16	S5 State: This signal indicates S4 or S5 (Soft Off) state.	O 3.3VSB		Connected to PMIC
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	I 3.3VSB	PU 10k 3.3VSB	Connected to GPIO
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again.	I 3.3VSB	PU 10k 3.3VSB	Connected to GPIO

9.17 Miscellaneous

Table 22 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	I 3.3V		Connected to GPIO
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	O 3.3V		Connected to GPIO
GP0_I2C_CLK	66	General Purpose I²C bus #0 clock line	I/O 3.3V OD	PU 4k7 3.3V	
GP0_I2C_DAT	68	General Purpose I²C bus #0 data line	I/O 3.3V OD	PU 4k7 3.3V	
SMB_CLK /GP1_I2C_CLK	60	Clock line of System Management Bus. Multiplexed with General Purpose I²C bus #1 clock line	I/O 3.3VSB OD	PU 4k7 3.3V	Connected to I2C
SMB_DAT /GP1_I2C_DAT	62	Data line of System Management Bus. Multiplexed with General Purpose I²C bus #1 data line	I/O 3.3VSB OD	PU 4k7 3.3V	Connected to I2C
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	I/O 3.3VSB OD	PU 10k 3.3V	Connected to GPIO.
SPKR /GP_PWM_OUT2	194	Primary functionality is output for audio enunciator, the “speaker” in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		Not supported.
BIOS_DISABLE# /BOOT_ALT#	41	Pin is used to select Boot mode.	I 3.3V	PU 4k7 3.3V	
RSVD	56,132,134,144, 146,154	Do not connect	NC		
GP_1-Wire_Bus	124	General Purpose 1-Wire bus interface. Can be used for consumer electronics control bus (CEC) of HDMI.	I/O 3.3V		Currently implemented as HDMI Consumer Electronics Control Bus.

9.18 Manufacturing/JTAG Interface

Table 23 Manufacturing Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
MFG_NC0	207	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC1	209	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	See caution statement below.
MFG_NC2	208	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	See caution statement below
MFG_NC3	210	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC4	204	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes.	NA	NA	

Note

The MFG_NC0..4 pins are reserved for manufacturing and debugging purposes. It's recommended to route the signals to a connector on the carrier board. The carrier board must not drive the MFG_NC-pins or have pull-up or pull-down resistors implemented for these signals. MFG_NC0...4 are defined to have a voltage level of 3.3V. It must be ensured that the carrier board has the correct voltage levels for JTAG/ UART signals originating from the module. For this reason, a level shifting device may be required on the carrier board to guarantee that these voltage levels are correct in order to prevent damage to the module.

More information about implementing a carrier board multiplexer can be found in the Qseven® Design Guide.

Caution

The MFG_NC4 pin is high active on the conga-QMX6 module. This means that the MFG interface on the edge connector functions by default as JTAG interface. Therefore, do not use the MFG interface for UART purposes or externally pull the MFG_NC4 pin to ground. Failure to adhere to this warning may result to back-driving which can damage the module.

If you need the UART function on the MFG interface, then you require a customized conga-QMX6. For more information, contact congatec support

9.19 Thermal Management

Table 24 Thermal Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I 3.3V	PU 10k 3.3V	Connected to GPIO
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off).	O 3.3V		Connected to GPIO

9.20 Fan Control

Table 25 Fan Control Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT /GP_PWM_OUT1	196	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V OC		
FAN_TACHOIN /GP_TIMER_IN	195	Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.	I 3.3V		Connected to GPIO

9.21 Bootstrap Signals

Table 26 Bootstrap Signal Descriptions

Signal	Pin #	Description of Bootstrap Signal	I/O	PU/PD	Comment
GBE_LINK#	13	Ethernet controller 0 link indicator, active low.	O 2.5VSB	PU 4k99	GBE0_LINK# is a bootstrap signal (see note below)
GBE_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 2.5VSB	PU 1k 3.3V	Not Supported. Internally connected to GBE_ACT#. GBE0_LINK100# is a bootstrap signal (see note below)
GBE_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 2.5VSB	PU 4k99	Not Supported. Internally connected to GBE_LINK# GBE0_LINK1000# is a bootstrap signal (see note below)
GBE_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 2.5VSB	PD 1k 3.3V	GBE0_ACT# is a bootstrap signal (see note below)

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either Qseven® internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the Qseven® module to malfunction and/or cause irreparable damage to the module.

Additionally, if it is necessary to have link and activity LEDs connected to GBE_LINK# and GBE_ACT# on the carrier board, then you have to use buffers. Without a buffer, the strapping becomes active and this causes the PHY to be programmed with wrong address.

10 Onboard Interfaces and Devices

10.1 UART/RS-232 Debug Port

The conga-QMX6 is equipped with a six-pin RS232 connector onboard the conga-QMX6. This RS-232 debug port is connected to the Freescale® i.MX6 UART1 and UART2 pins via the MAXIM-3232 transceiver. The transceiver is guaranteed to run at data rates of 250kbps in normal operating mode, while maintaining RS-232 output levels.

Refer to section 5.2 for more information about the UART interface.

Table 27 UART Signal Descriptions

Pin #	Signal (Molex Connector)	D-SUB 1 (Console)	D-SUB 2	Description	Color
1	DCE1_TXT	NC	Pin 2	i.MX6 UART 5 Serial Data Transmitter	Red
2	NC	NC	NC	Not Connected	-
3	GND	Pin 5	Pin 5	Ground	White
4	DCE2_TXT	Pin 2	NC	UART 2 Serial Data Transmitter	Black
5	DCE2_RX	Pin 3	NC	UART 2 Serial Data Receiver	Orange
6	DCE1_RX	NC	Pin 3	i.MX6 UART 5 Serial Data Receiver	Purple

Note

The RS232 adapter cable (PN: 48000023) for the onboard UART interface is included in the congatec Qseven Evaluation kit. You can also order this cable separately from congatec AG. For more information, contact your congatec sales representative.

10.2 MIPI/CMOS Camera

The Freescale® i.MX6 Image Processing Unit (IPU) provides connectivity to cameras via the MIPI/CSI-2 transmitter and maintains image manipulation and processing with adequate synchronization and control. The Camera Serial Interface (CSI) controls the camera port and provides interface to an image sensor or a related device. The role of the camera ports is to receive input from video sources and to provide support for time-sensitive signals to the camera. Non-time-sensitive controls such as configuration, reset are performed by the ARM platform through I2C interface or GPIO signals

Note

The conga-QMX6 BSPs do not currently support the camera interface.

10.3 JTAG Interface

The conga-QMX6 offers an onboard 10-pin JTAG interface. For compatible JTAG adapters, contact congatec support team or use the Nit6X_JTAG adapter Boundary Devices.

10.4 SPI Flash

Onboard the conga-QMX6 is a 32 Mbit SPI flash memory. This flash memory contains the bootloader and is directly connected to the ECSPI-1 interface of the i.MX6 processor.

The Freescale® i.MX6 processor is programmed to boot from the SPI flash.

10.5 Android Buttons

Table 28 Android Button Signal Descriptions

Onboard the conga-QMX6 is an eight pin connector for implementing android buttons. The signals are directly connected to the Freescale® i.MX6 processor.

Signal	Pin #	Description	I/O	Comment
PWRBTN#	1	Power button signal		
KEY_VOL_UP	2	Increases volume	GPIO7_13	
HOME	3	Returns to the main home screen	GPIO2_4	
SEARCH	4	Brings up the search function	GPIO2_3	
BACK	5	Takes you a level back in an app or a page back in a browser	GPIO2_2	
MENU	6	Displays additional options in an application	GPIO2_1	
KEY_VOL_DN	7	Decreases volume	GPIO4_5	
GND	8	Ground		

10.6 DDR3 Memory

The conga-QMX6 offers a 2GB DDR3 SDRAM memory onboard. The memory modules are connected directly to the DDR ports of the Freescale® i.MX6 processor.

10.7 eMMC

The conga-QMX6 offers a 4G eMMC module onboard. The onboard eMMC is a nand flash device and it is routed directly to the SDIO port 3 of the Freescale® i.MX6 processor. Eight lanes are used for data.

10.8 Micro SD

The conga-QMX6 offers an onboard micro SD connector (backside of the module). It is connected to the SDIO port 2 of the Freescale® i.MX6 processor. Four lanes are used for data.

11 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Qseven® Specification	http://www.qseven-standard.org/
Qseven® Design Guide	http://www.qseven-standard.org/
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications
Freescale website	http://www.freescale.com