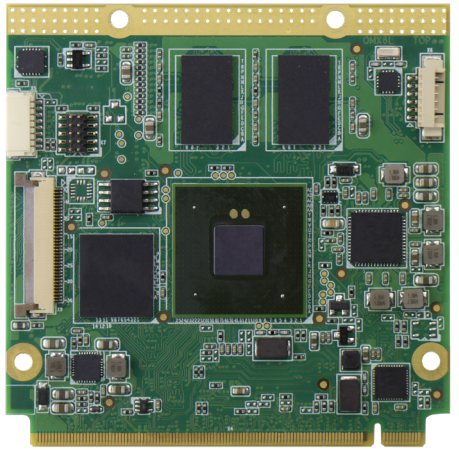

# conga-QMX6

Qseven® 2.1 Module with NXP® i.MX6 Processors

***User's Guide***

Revision 1.4

# Revision History

| Revision | Date (yyyy.mm.dd) | Author | Changes |
|---|---|---|---|
| 0.1 | 2013.03.28 | AEM | • Preliminary release |
| 0.2 | 2013.11.05 | AEM | • Corrected the LVDS data rates/resolutions supported in sections 2.1 "Feature List" and 5.8 "LVDS".<br>• Added information about the Atheros Quadcomm Ethernet PHY for conga-QMX6 revision B.0 in sections 2.1 "Feature List" and 5.3 "Gigabit Ethernet".<br>• Updated section 4 "Heatspreader". Added additional heatspreader variants.<br>• Updated section 5.2 "UART". Updated section 5.13 "Manufacturing/Jtag Interface".<br>• Added pin descriptions for the onboard UART connector and the RS-232 adapter cable in section 10.1 "UART/RS-232 Debug Port".<br>• Added section 10.3 "JTAG Interface". |
| 0.3 | 2014.02.28 | AEM | • Added the new Ethernet PHY (Qualcomm Atheros) for conga-QMX6 revision B.x to relevant sections.<br>• Changed the eMMC value of industrial variants from 2G to 4G.<br>• Deleted the row "RSVD" from table 23 " Manufacturing Signal Description".<br>• Edited section 5.2 "UART" and added caution statement.<br>• Corrected the pin number of signal DP_HDMI_HPD# in section 9.9 "DisplayPort".<br>• Updated the whole document. |
| 1.0 | 2015.09.03 | AEM | • Updated section 2.2 "Supported Operating Systems".<br>• Added note to table 7 "UART Signal Descriptions".<br>• Corrected the DP_HDMI_HPD# pin description in table 14 "DisplayPort".<br>• Corrected the LPC/GPIO6 (Pin 191) signal description in table 16 "LPC/GPIO".<br>• Changed Pin 56 from "RSVD" to "USB_VBUS_DRIVE" in various sections.<br>• Updated table 10 "USB 2.0 Signal Description" in compliance with the Qseven 2.0 Specification, Errata Document 1.0.<br>• Added table 28 "MIPI Signal Descriptions" and updated section 10.2 "MIPI/CMOS Camera".<br>• Updated document to revision B.x and C.x<br>• Official release |
| 1.1 | 2016.05.04 | AEM | • Updated the Options Information table in section 1 "Introduction". Also added Options Information table for revision C.x<br>• Updated section 2.3 "Mechanical Dimensions".<br>• Updated section 4 "Heatspreader".<br>• Replaced "Freescale" with "NXP" in the whole document. |
| 1.2 | 2020.01.10 | BEU | • Updated table references throughout the document<br>• Updated information about handling electrostatic sensitive devices in preface section<br>• Added new variant "PN:016318" to table 4<br>• Updated section 4 "Heatspreader"<br>• Updated reference to power supply design guide in section 5.14 "Power Control"<br>• Added note about min. pulse width to several button signals in table 23 and 24<br>• Added note about WDOUT signal below table 25<br>• Updated section 11 "Industry Specifications"<br>• Added information and note to section 10.7 "eMMC" |

| | | | |
|---|---|---|---|
| 1.3 | 2022.10.25 | BEU | • Updated document to revision D.x<br>• Updated congatec AG to congatec GmbH throughout the document<br>• Added software license information to preface section<br>• Restructured preface section<br>• Updated section 1 "Introduction"<br>• Updated table 7 "Feature Summary"<br>• Added module variant 016318 to table 8 "Cooling Solution Variants"<br>• Updated supported operating systems in section 2.2 "Supported Operating Systems"<br>• Added module variants to section 2.5 "Power Consumption"<br>• Updated storage temperature for commercial variants in section 2.7 "Environmental Specifications"<br>• Updated block diagram in section 3 "Block Diagram"<br>• Added note about revision D.x onboard PCIe clock generator in section 5.1 "PCI Express™"<br>• Added revision D.x transceiver in section 5.3 "Gigabit Ethernet"<br>• Added UART0_RTS# and UART0_CTS# assembly options to table 10 "Edge Finger Pinout"<br>• Added revision D.x UART0_CTS# and UART0_RTS# information to note below table 12 "UART Signal Descriptions"<br>• Updated USB_ID and USB_OTG_PEN signals descriptions in table 15<br>• Added revision D.x information to section 10.2 "MIPI/CMOS Camera"<br>• Renamed section 10.6 "DDR3 Memory" to "DD3RL Memory" and updated it<br>• Added revision D.x support for 1.8V micro SD cards to section 10.2 "Micro SD"<br>• Removed section 11 "Industry Specifications" |
| 1.4 | 2023.12.23 | BEU | • Updated title page<br>• Updated RoHS Directive in preface section<br>• Removed revision D.x throughout the document<br>• Added E.x to note in section 1 "Introduction"<br>• Removed Gen 2 from PCIe in section 2.1 "Feature List" and 3 "Block Diagram"<br>• Added note regarding long-term storage to section 2.7 "Environmental Specifications"<br>• Added note regarding long-term storage to section 4 "Heatspreader"<br>• Updated section 5.1 "PCI Express"<br>• Added revision E.x to section 5.3 "Gigabit Ethernet"<br>• Added comment for PCIe Clock signals to table 11<br>• Added revision E.x to note under table 12 "UART Signal Descriptions"<br>• Added revision E.x to section 10.2 "MIPI/CMOS Camera"<br>• Added revision E.x to section 10.7 "eMMC"<br>• Added revision E.x to section 10.8 "Micro SD" |

# Preface

This user's guide provides information about the components, features, connectors and signals available on the conga-QMX6 Revision E.x. It is one of four documents that you should refer to when designing an NXP® i.MX6 based Qseven® application. The other reference documents that should be used include the following:

Qseven® Design Guide

Qseven® Specification

NXP® i.MX6 Applications Processor Reference Manual (available at www.nxp.com)

The links to these documents can be found on the congatec GmbH website at www.congatec.com

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## Symbols

The following symbols are used in this user's guide:

**Warning**

*Warnings indicate conditions that, if not observed, can cause personal injury.*

**Caution**

*Cautions warn the user about how to prevent damage to hardware or loss of data.*

**Note**

*Notes call attention to important information that should be observed.*

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# Terminology

| Term | Description |
|---|---|
| PCI Express (PCIe) | Peripheral Component Interface Express – next-generation high speed Serialized I/O bus |
| ARM | Advanced RISC Machine |
| JTAG | Joint Test Action Group |
| eCSPI | Enhanced Configurable Serial Peripheral Interface |
| MIPI | Mobile Industry CPU Interface |
| GPIO | General Purpose Input Output |
| RGMII | Reduced Gigabit Media Independent Interface |
| PCI Express Lane | One PCI Express Lane is a set of 4 signals that contains two differential lines for transmitting and two differential lines for Receiving. Clocking information is embedded into the data stream. |
| PCI Express Mini Card | PCI Express Mini Card add-in card is a small size unique form factor optimized for mobile computing platforms. |
| eMMC | Embedded Multi Media Card is a non-volatile memory system, which frees the processor from low level flash memory management. |
| SDIO card | SDIO (Secure Digital Input Output) is a non-volatile memory card format developed for use in portable devices. |
| USB | Universal Serial Bus |
| SATA | Serial AT Attachment: serial-interface standard for hard disks |
| HDA | High Definition Audio |
| HDMI | High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. |
| TMDS | Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI. |
| DVI | Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG). |
| I²C Bus | Inter-Integrated Circuit Bus: is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system. |
| SM Bus | System Management Bus: is a popular derivative of the I²C-bus. |
| SPI Bus | Serial Peripheral Interface is a synchronous serial data link standard named by Motorola that operates in full duplex mode. |
| CAN Bus | Controller-area network is a vehicle bus standard designed to allow microcontrollers and devices to communicate with each other within a vehicle without a host computer. |
| AMBA | Advanced Microcontroller Bus Architecture |
| IOMUX | Input Output Multiplexer |
| GbE | Gigabit Ethernet |
| LVDS | Low-Voltage Differential Signaling |
| DDC | Display Data Channel is an I²C bus interface between a display and a graphics adapter. |
| N.C. | Not connected |
| N.A. | Not available |
| T.B.D. | To be determined |

# Contents

# List of Tables

# 1 INTRODUCTION

## Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Computer-On-Module that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector. The pinout remains the same regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express® graphics cards in notebooks.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The conga-QEVAL/Qseven® 2.0 evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose what are suitable for their application. Qseven® applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no need to redesign the carrier board.

**Note**

*The conga-QMX6 B.x and later revisions are designed based on the Qseven Specification 2.0. Revision C.x follows the Qseven Specification 2.0 Errata. Revision E.x follows the Qseven Specification 2.1.*

## conga-QMX6 Options Information (Revision B.x)

The conga-QMX6 revision B.x was available in eleven variants (seven commercial and four industrial). Below you will find an order table showing the base configuration modules that were offered by congatec GmbH. The part numbers are obsolete as of revision C.x. For more information about additional conga-QMX6 variants offered by congatec, contact your local congatec sales representative or visit the congatec website at www.congatec.com.

Table 1 Commercial variants

| Part-No. | 016100 | 016101 | 016102 | 016103 | 016104 | 016105 | 016106 |
|---|---|---|---|---|---|---|---|
| Processor | NXP® i.MX6 Cortex A9 1.0 GHz Single Core | NXP® i.MX6 Cortex A9 1.0 GHz Dual Lite | NXP® i.MX6 Cortex A9 1.0 GHz Dual Core | NXP® i.MX6 Cortex A9 1.0 GHz Quad Core | NXP® i.MX6 Cortex A9 1.0 GHz Quad Core | NXP® i.MX6 Cortex A9 1.0 GHz Quad Core | NXP® i.MX6 Cortex A9 1.0 GHz Quad Core |
| L2 Cache | 512 kB | 512 kB | 1 MB | 1 MB | 1 MB | 1 MB | 1 MB |
| Onboard Memory | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L | 2GB DDR3L | 2GB DDR3L | 1GB DDR3L |
| eMMC up to 8GB | 4GB | 4GB | 4GB | 4GB | 4GB | 8GB | 8GB |
| PCI Express Lane | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| CAN Bus | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Gigabit Ethernet | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| SATA | No | No | Yes | Yes | Yes | Yes | Yes |

Table 2 Industrial Variants

| Part-No. | 016110 | 016111 | 016112 | 016113 |
|---|---|---|---|---|
| Processor | NXP® i.MX6 Cortex A9 800 MHz Single Core | NXP® i.MX6 Cortex A9 800 MHz Dual Lite | NXP® i.MX6 Cortex A9 800 MHz Dual Core | NXP® i.MX6 Cortex A9 800 MHz Quad Core |
| L2 Cache | 512 kB | 512 kB | 1 MB | 1 MB |
| Onboard Memory | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L |
| eMMC up to 8GB | 4GB | 4GB | 4GB | 4GB |
| PCI Express Lane | Yes | Yes | Yes | Yes |
| CAN Bus | Yes | Yes | Yes | Yes |
| Gigabit Ethernet | Yes | Yes | Yes | Yes |
| SATA | No | No | Yes | Yes |

**Caution**

*Do not alter the conga-QMX6 boot fuse settings. These fuse settings are already programmed during production process and are not protected against alteration. Changing the boot fuse settings will void the congatec GmbH warranty.*

## conga-QMX6 Options Information (Revision C.x)

Revision C.x of the conga-QMX6 was available in twelve variants (seven commercial and five industrial). Below you will find an order table showing the base configuration modules that were offered by congatec GmbH. For more information about additional conga-QMX6 variants offered by congatec, contact your local congatec sales representative or visit the congatec website at www.congatec.com.

Table 3 Commercial Variants

| Part-No. | 016300 | 016301 | 016302 | 016303 | 016304 | 016305 | 016306 |
|---|---|---|---|---|---|---|---|
| Processor | NXP® i.MX6 Cortex A9 1.0 GHz Single Core | NXP® i.MX6 Cortex A9 1.0 GHz Dual Lite | NXP® i.MX6 Cortex A9 1.0 GHz Dual Core | NXP® i.MX6 Cortex A9 1.0 GHz Quad Core | NXP® i.MX6 Cortex A9 1.0 GHz Quad Core | NXP® i.MX6 Cortex A9 1.0 GHz Quad Core | NXP® i.MX6 Cortex A9 1.0 GHz Quad Core |
| L2 Cache | 512 kB | 512 kB | 1 MB | 1 MB | 1 MB | 1 MB | 1 MB |
| Onboard Memory | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L | 2GB DDR3L | 2GB DDR3L | 1GB DDR3L |
| eMMC up to 8GB | 4GB | 4GB | 4GB | 4GB | 4GB | 8GB | 8GB |
| PCI Express Lane | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| CAN Bus | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Gigabit Ethernet | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| SATA | No | No | Yes | Yes | Yes | Yes | Yes |

Table 4 Industrial Variants

| Part-No. | 016310 | 016311 | 016312 | 016313 | 016318 |
|---|---|---|---|---|---|
| Processor | NXP® i.MX6 Cortex A9 800 MHz Single Core | NXP® i.MX6 Cortex A9 800 MHz Dual Lite | NXP® i.MX6 Cortex A9 800 MHz Dual Core | NXP® i.MX6 Cortex A9 800 MHz Quad Core | NXP® i.MX6 Cortex A9 800 MHz Quad Core |
| L2 Cache | 512 kB | 512 kB | 1 MB | 1 MB | 1 MB |
| Onboard Memory | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L | 4GB DDR3L |
| eMMC up to 8GB | 4GB | 4GB | 4GB | 4GB | 4GB |
| PCI Express Lane | Yes | Yes | Yes | Yes | Yes |
| CAN Bus | Yes | Yes | Yes | Yes | Yes |
| Gigabit Ethernet | Yes | Yes | Yes | Yes | Yes |
| SATA | No | No | Yes | Yes | Yes |

**Caution**

*Do not alter the conga-QMX6 boot fuse settings. These fuse settings are already programmed during production process and are not protected against alteration. Changing the boot fuse settings will void the congatec GmbH warranty.*

## conga-QMX6 Options Information (Revision E.x)

Revision E.x of the conga-QMX6 is currently available in ten variants (five commercial and five industrial). Below you will find an order table showing the base configuration modules that are currently offered by congatec GmbH. For more information about additional conga-QMX6 variants offered by congatec, contact your local congatec sales representative or visit the congatec website at www.congatec.com.

Table 5 Commercial Variants

| Part-No. | 016300 | 016301 | 016302 | 016303 | 016304 |
|---|---|---|---|---|---|
| Processor | NXP® i.MX6 Cortex A9 1.0 GHz Single Core | NXP® i.MX6 Cortex A9 1.0 GHz Dual Lite | NXP® i.MX6 Cortex A9 1.0 GHz Dual Core | NXP® i.MX6 Cortex A9 1.0 GHz Quad Core | NXP® i.MX6 Cortex A9 1.0 GHz Quad Core |
| L2 Cache | 512 kB | 512 kB | 1 MB | 1 MB | 1 MB |
| Onboard Memory | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L | 2GB DDR3L |
| eMMC | 32GB | 32GB | 32GB | 32GB | 32GB |
| PCI Express Lane | Yes | Yes | Yes | Yes | Yes |
| CAN Bus | Yes | Yes | Yes | Yes | Yes |
| Gigabit Ethernet | Yes | Yes | Yes | Yes | Yes |
| SATA | No | No | Yes | Yes | Yes |

Table 6 Industrial Variants

| Part-No. | 016310 | 016311 | 016312 | 016313 | 016318 |
|---|---|---|---|---|---|
| Processor | NXP® i.MX6 Cortex A9 800 MHz Single Core | NXP® i.MX6 Cortex A9 800 MHz Dual Lite | NXP® i.MX6 Cortex A9 800 MHz Dual Core | NXP® i.MX6 Cortex A9 800 MHz Quad Core | NXP® i.MX6 Cortex A9 800 MHz Quad Core |
| L2 Cache | 512 kB | 512 kB | 1 MB | 1 MB | 1 MB |
| Onboard Memory | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L | 1GB DDR3L | 4GB DDR3L |
| eMMC | 32GB | 32GB | 32GB | 32GB | 32GB |
| PCI Express Lane | Yes | Yes | Yes | Yes | Yes |
| CAN Bus | Yes | Yes | Yes | Yes | Yes |
| Gigabit Ethernet | Yes | Yes | Yes | Yes | Yes |
| SATA | No | No | Yes | Yes | Yes |

**Caution**

*Do not alter the conga-QMX6 boot fuse settings. These fuse settings are already programmed during production process and are not protected against alteration. Changing the boot fuse settings will void the congatec GmbH warranty.*

# 2 Specifications

## 2.1 Feature List

Table 7 Feature Summary

| | | |
|---|---|---|
| Form Factor | Qseven \| 70x70mm | |
| Processor | NXP® i.MX6 Cortex A9 | |
| DRAM | Up to 4 GByte onboard DDR3L memory \| 1066 MT/s | |
| Ethernet | 1x Gbit Ethernet | |
| I/O Interfaces | 5x USB 2.0 (shared with 1x USB OTG client) \| SATA (only i.MX6 Dual/Quad) \| 1x SDIO \| 1x PCIe \| I²C Bus \| CAN Bus \| SPI | |
| Mass Storage | eMMC up to 32 GByte \| Onboard MicroSD socket | |
| Sound | 1x I²S | |
| Graphics | Integrated in NXP i.MX6 \| Video (VPU) \| 2D Graphics (GPU2D) and 3D Graphics (GPU3D) \| 3D graphics with 4 shaders up to 200MT/s dual stream 1080p/720p decoder/encoder \| OpenGL \| OpenCL \| OpenVG 1.1 | |
| Video Interfaces | HDMI v1.4 support supported by Qseven specification.2x LVDS (2x 24 bit) \| 1x LVDS (1x 24 bit) up to WUXGA resolution \| 1920x1200 pixel and HD1080 \| Supports 18bit and 24bit dual channel up to WUXGA 1920x1200 | |
| Features | Watchdog Timer \| JTAG debug interface \| MIPI CSI-2 camera interface on flat foil connector \| High Precision Real Time Clock | |
| Security | High Assurance Boot support \| TrustZone® \| RNG | |
| Boot Loader | U-Boot boot loader | |
| Operating Systems | Linux \| Android | |
| Power Consumption | Typical application 3-5W @ 5V | |
| Temperature Range | Operating Temperature Range: | 0 to +60°C commercial grade<br>-40 to +85°C industrial grade |
| | Storage Temperature Range: | -40 to +85°C |
| Humidty | Operating: 10 - 90% r. H. non cond. | Storage: 5 - 95% r. H. non cond. |

**Note**

*Some of the features mentioned in the above feature summary are optional. Check the article number of your module and compare it to the conga-QMX6 options information list on page 12 of this user's guide to determine what options are available on your particular module.*

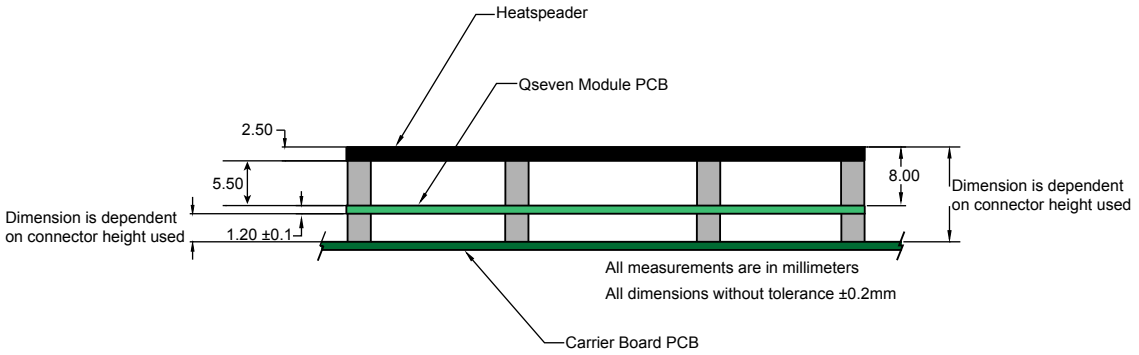
## 2.2 Supported Operating Systems

The conga-QMX6 supports the following operating systems.

- Android
- Linux

## 2.3 Mechanical Dimensions

- 70.0 mm x 70.0 mm @ (2 ¾" x 2 ¾")
- The Qseven™ module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.

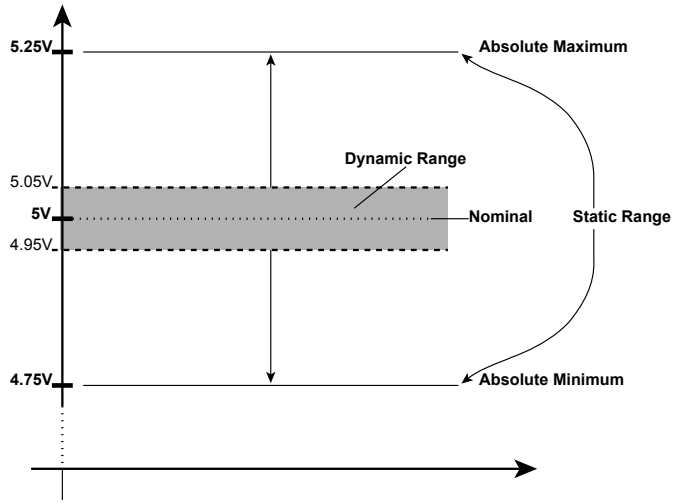



Rear View of Qseven Module

## 2.4 Supply Voltage Standard Power

- 5V DC ± 5%

The dynamic range shall not exceed the static range.




### 2.4.1 Electrical Characteristics

| Characteristics | | | Min. | Typ. | Max. | Units | Comment |
|---|---|---|---|---|---|---|---|
| 5V | Voltage | ± 5% | 4.75 | 5.00 | 5.25 | Vdc | |
| | Ripple | | - | - | ± 50 | $mV_{PP}$ | 0-20MHz |
| | Current | | | | | | |
| 5V_SB | Voltage | ± 5% | 4.75 | 5.00 | 5.25 | Vdc | |
| | Ripple | | | | ± 50 | $mV_{PP}$ | |

### 2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

**Note**

*For information about the input power sequencing of the Qseven® module, refer to the Qseven® specification.*

## 2.5 Power Consumption

The power consumption values listed in this section were measured under a controlled environment. The hardware used for testing includes a conga-QMX6 module, carrier board for Qseven ARM, TFT monitor, micro-SD card and USB keyboard. The carrier board was powered externally by a power supply unit so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. All recorded values were averaged over a 30 second time period. The modules were cooled by the heatspreader specific to the module variants

Each module was measured while running 32 bit Linaro Ubuntu 11.10. To measure the worst case power consumption, the cooling solution was removed and the CPU core temperature was allowed to run between 95° and 100°C at 100% workload. The peak current value was then recorded. This value should be taken into consideration when designing the system's power supply to ensure that the power supply is sufficient during worst case scenarios.

Power consumption values were recorded during the following stages:

Linaro Ubuntu 11.10 (32 bit)

- Desktop Idle
- 100% CPU workload
- 100% CPU workload at approximately 100°C peak power consumption

**Note**

With the Linux stress tool, we stressed the CPU to maximum frequency.

## Processor Information

The tables below provide additional information about the different variants offered by the conga-QMX6.

### 2.5.1 NXP® i.MX6 Cortex A9 1.0 GHz Single Core 512kB L2 cache

With 4GB onboard eMMC

| conga-QMX6 Art. No. 016100 / 016300 | NXP® i.MX6 Cortex A9 1.0 GHz 512kB L2 cache (40nm) | | |
|---|---|---|---|
| Memory Size | 1GB onboard | | |
| Operating System | Ubuntu | | |
| Power State | Desktop Idle | 100% workload | Max. Power Consumption |
| Power consumption (measured in Ampere/Watt) | 0.22 A / 1.1 W | 0.34 A / 1.7 W | 0.46 A /2.3 W |

### 2.5.2 NXP® i.MX6 Cortex A9 1.0 GHz Dual Lite 512kB L2 cache

With 4GB onboard eMMC

| conga-QMX6 Art. No. 016101 / 016301 | NXP® i.MX6 Cortex A9 1.0 GHz 512kB L2 cache (40nm) | | |
|---|---|---|---|
| Memory Size | 1GB onboard | | |
| Operating System | Ubuntu | | |
| Power State | Desktop Idle | 100% workload | Max. Power Consumption |
| Power consumption (measured in Ampere/Watt) | 0.26 A / 1.3 W | 0.44 A / 2.2 W | 0.66 A / 3.3 W |

### 2.5.3 NXP® i.MX6 Cortex A9 1.0 GHz Dual Core 1MB L2 cache

With 4GB onboard eMMC

| conga-QMX6 Art. No. 016102 / 016302 | NXP® i.MX6 Cortex A9 1.0 GHz 1MB L2 cache (40nm) | | |
|---|---|---|---|
| Memory Size | 1GB onboard | | |
| Operating System | Ubuntu | | |
| Power State | Desktop Idle | 100% workload | Max. Power Consumption |
| Power consumption (measured in Ampere/Watt) | 0.28 A / 1.4 W | 0.5 A / 2.5 W | 0.7 A / 3.2 W |

## 2.5.4 NXP® i.MX6 Cortex A9 1.0 GHz Quad Core 1MB L2 cache

With 4GB onboard eMMC

| conga-QMX6 Art. No. 016103 / 016303 | NXP® i.MX6 Cortex A9 1.0 GHz 1MB L2 cache (40nm) | | |
|---|---|---|---|
| Memory Size | 1GB onboard | | |
| Operating System | Ubuntu | | |
| Power State | Desktop Idle | 100% workload | Max. Power Consumption |
| Power consumption (measured in Ampere/Watt) | 0.3 A / 1.5 W | 0.72 A / 3.6 W | 0.92 A / 4.6 W |

## 2.5.5 NXP® i.MX6 Cortex A9 1.0 GHz Quad Core 1MB L2 cache

With 4GB onboard eMMC

| conga-QMX6 Art. No. 016104 / 016304 | NXP® i.MX6 Cortex A9 1.0 GHz 1MB L2 cache (40nm) | | |
|---|---|---|---|
| Memory Size | 2GB onboard | | |
| Operating System | Ubuntu | | |
| Power State | Desktop Idle | 100% workload | Max. Power Consumption |
| Power consumption (measured in Ampere/Watt) | 0.3 A / 1.5 W | 0.74 A / 3.7 W | 0.94 A / 4.7 W |

## 2.5.6 NXP® i.MX6 Cortex A9 800 MHz Single Core 512kB L2 cache (2GB eMMC)

With 2GB onboard eMMC

| conga-QMX6 Art. No. 016110 / 016310 | NXP® i.MX6 Cortex A9 800 MHz 512kB L2 cache (40nm) | | |
|---|---|---|---|
| Memory Size | 1GB onboard | | |
| Operating System | Ubuntu | | |
| Power State | Desktop Idle | 100% workload | Max. Power Consumption |
| Power consumption (measured in Ampere/Watt) | 0.24 A / 1.2 W | 0.30 A / 1.5 W | 0.48 A / 2.1 W |

## 2.5.7 NXP® i.MX6 Cortex A9 800 MHz Dual Lite 512kB L2 cache (2GB eMMC)

With 2GB onboard eMMC

| conga-QMX6 Art. No. 016111 / 016311 | NXP® i.MX6 Cortex A9 800 MHz 512kB L2 cache (40nm) | | |
|---|---|---|---|
| Memory Size | 1GB onboard | | |
| Operating System | Ubuntu | | |
| Power State | Desktop Idle | 100% workload | Max. Power Consumption |
| Power consumption (measured in Ampere/Watt) | TBD A / W | TBD A / W | TBD A / W |

## 2.5.8 NXP® i.MX6 Cortex A9 800 MHz Dual Core 1MB L2 cache (2GB eMMC)

With 2GB onboard eMMC

| conga-QMX6 Art. No. 016112 / 016312 | NXP® i.MX6 Cortex A9 800 MHz 1MB L2 cache (40nm) | | |
|---|---|---|---|
| Memory Size | 1GB onboard | | |
| Operating System | Ubuntu | | |
| Power State | Desktop Idle | 100% workload | Max. Power Consumption |
| Power consumption (measured in Ampere/Watt) | 0.30 A / 1.5W | 0.42 A / 2.1 W | 0.60 A / 3.0 W |

## 2.5.9 NXP® i.MX6 Cortex A9 800 MHz Quad Core 1MB L2 cache (2GB eMMC)

With 2GB onboard eMMC

| conga-QMX6 Art. No. 016113 / 016313 | NXP® i.MX6 Cortex A9 800 MHz 1MB L2 cache (40nm) | | |
|---|---|---|---|
| Memory Size | 1GB onboard | | |
| Operating System | Ubuntu | | |
| Power State | Desktop Idle | 100% workload | Max. Power Consumption |
| Power consumption (measured in Ampere/Watt) | 0.30 A / 1.5 W | 0.54 A / 2.7 W | 0.72 A / 3.6 W |

### 2.5.10 NXP® i.MX6 Cortex A9 800 MHz Quad Core 1MB L2 cache (4GB eMMC)

With 4GB onboard eMMC

| conga-QMX6 Art. No. 016318 | NXP® i.MX6 Cortex A9 800 MHz 1MB L2 cache (40nm) | | |
|---|---|---|---|
| Memory Size | 4GB onboard | | |
| Operating System | Ubuntu | | |
| Power State | Desktop Idle | 100% workload | Max. Power Consumption |
| Power consumption (measured in Ampere/Watt) | TBD A/ W | TBD A/ W | TBD A/ W |

**Note**

*All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.*

## 2.6 Supply Voltage Battery Power

- 2.0V-3.6V DC
- Typical 3V DC

### 2.6.1 CMOS Battery Power Consumption

| RTC @ 20°C | Voltage | Current |
|---|---|---|
| RTC onboard the conga-QMX6 module | 3V DC | 1.45 µA |

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec GmbH website at www.congatec.com.

**Note**

*To improve the lifetime of the CMOS battery, congatec implemented an external real-time clock onboard the conga-QMX6 module.*

## 2.7 Environmental Specifications

| | | |
|---|---|---|
| Temperature | Operation: 0° to 60°C | Storage: -40° to +85°C (commercial grade variants of conga-QMX6) |
| Temperature | Operation: -40° to 85°C | Storage: -40° to +85°C (industrial grade variants of conga-QMX6) |
| Humidity | Operation: 10% to 90% | Storage: 5% to 95% (humidity specifications are for non-condensing conditions) |

**Caution**

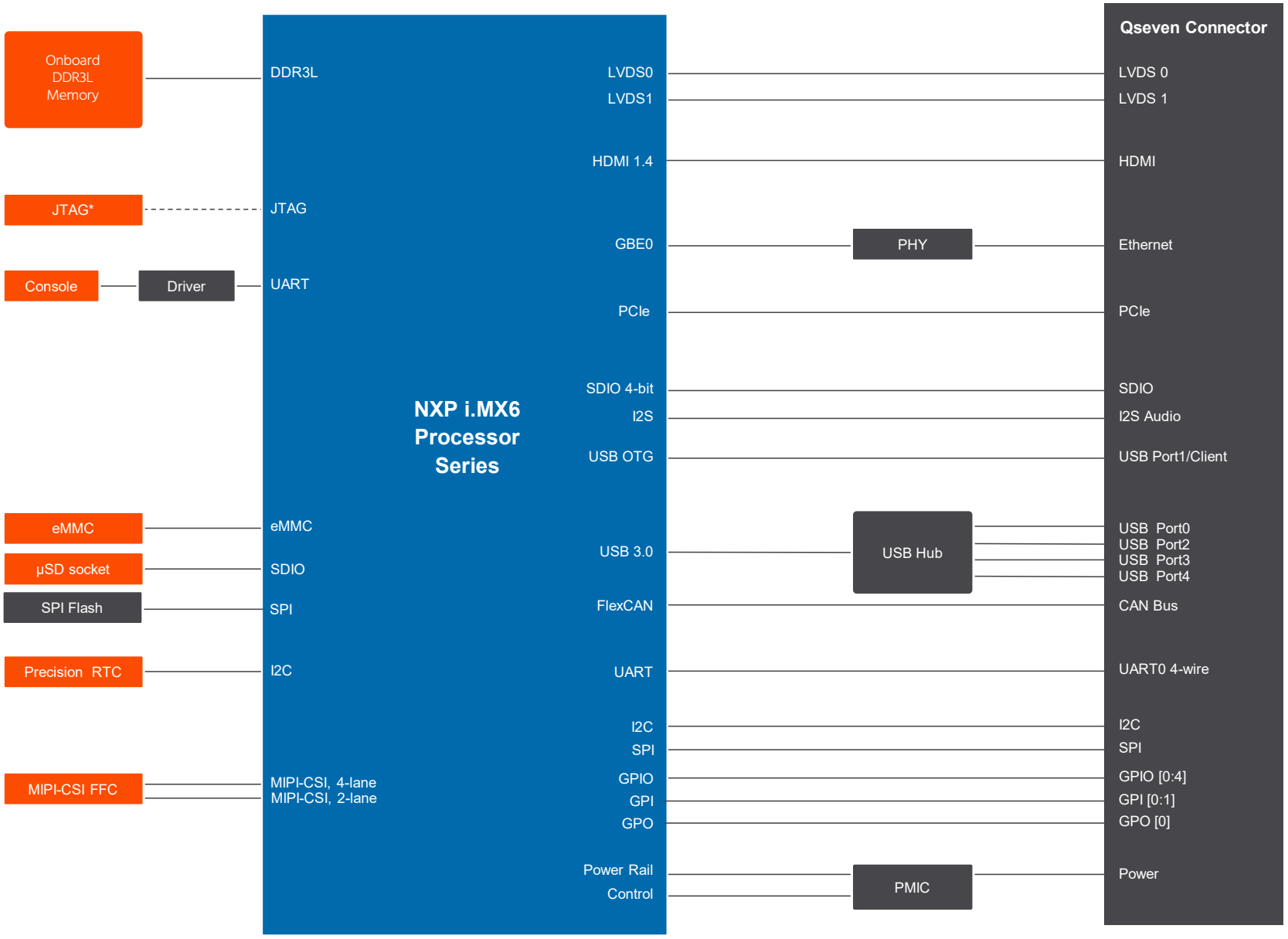
*The above operating temperatures must be strictly adhered to at all times.*

**Note**

*For long term storage of the conga-QMX6 (more than six months), keep the conga-QMX6 in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.*

*We do not recommend storing the conga-QMX6 for more than five years under these conditions.*

# 3 Block Diagram




* Assembly Option

# 4 Heatspreader

congatec GmbH offers three heatspreader variants for the conga-QMX6. Each heatspreader variant is intended for specific conga-QMX6 modules as shown in the table below. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 8 Cooling Solution Variants

| Heatspreader Variant | Heatspreader Part No. (PN) | Compatible conga-QMX6 Variants (PN) | Comment |
|---|---|---|---|
| conga-QMX6/HSP1-T | 016160 | 016112, 016113, 016312, 016313, 016318 | For modules equipped with lidded FC-PBGA CPU (1mm Gap Pad) |
| conga-QMX6/HSP2-T | 016161 | 016100, 016101, 016110, 016111<br>016300, 016301, 016310, 016311 | For modules equipped with MA-PBGA CPU (2mm Gap Pad) |
| conga-QMX6/HSP3-T | 016162 | 016102, 016103, 016104, 016105, 016106<br>016302, 016303, 016304, 016305, 016306 | For modules equipped with non-lidded FC-PBGA CPU (heatstack solution) |

**Note**

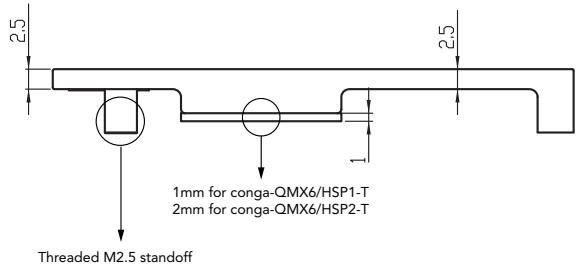
1. *We recommend a maximum torque of 0.4 Nm for the mounting screws and to start with the two screws furthest from the CPU die.*
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*
3. *Only a few NXP® iMX6 on-chip devices are enabled by default in the bootloader. With this default configuration, the conga-QMX6 power consumption is low. However, power consumption may increase significantly depending on your application and the workload of the CPU.*
4. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

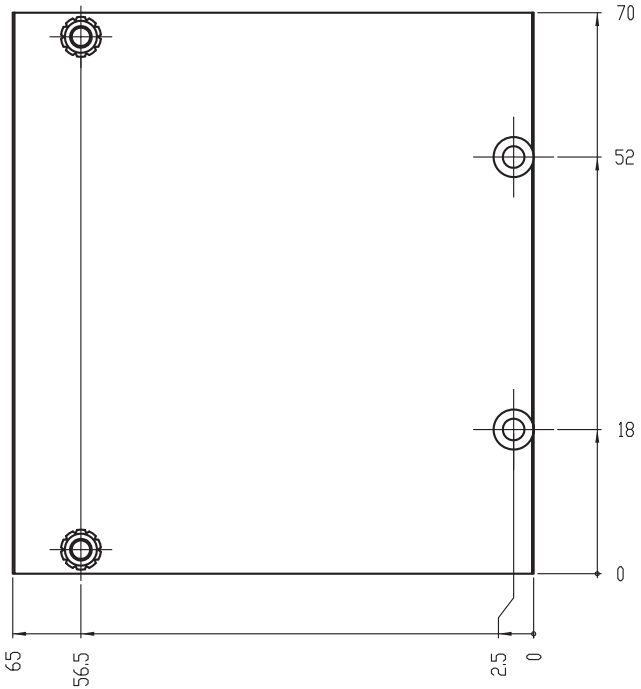
**Caution**

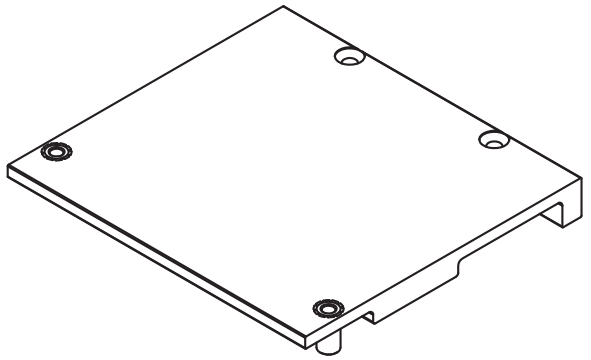
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
4. *When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.*

# 4.1 Heatspreader Dimensions

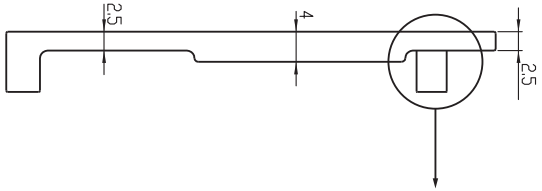
## conga-QMX6/HSP1-T and HSP2-T



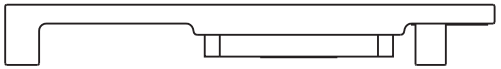



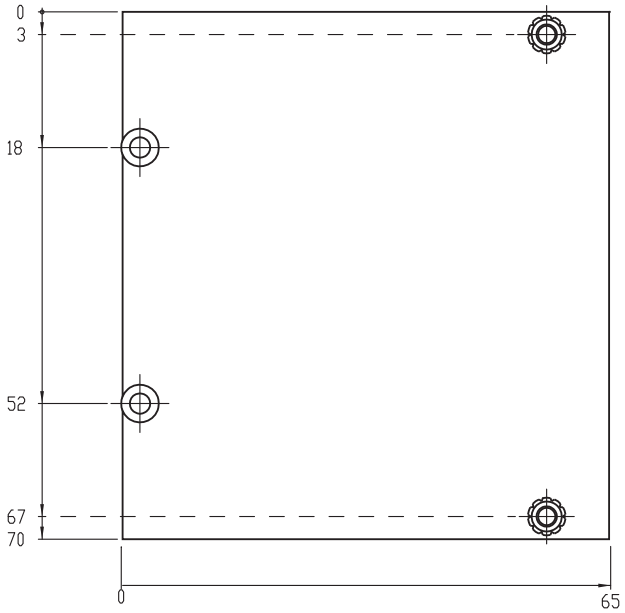



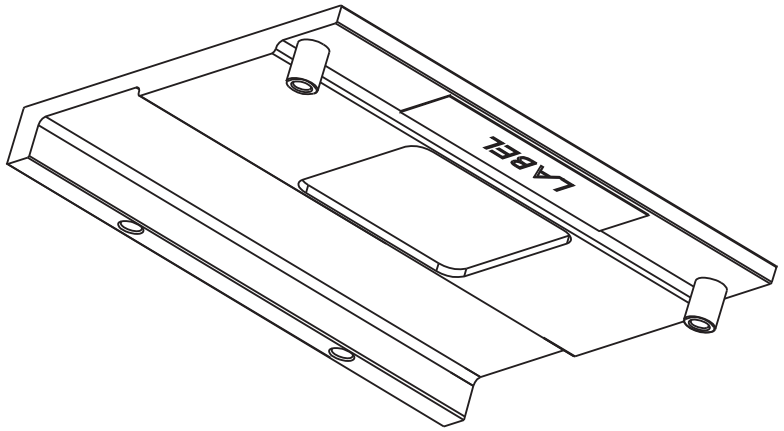
## conga-QMX6/HSP3-T




Threaded M.25 standoff

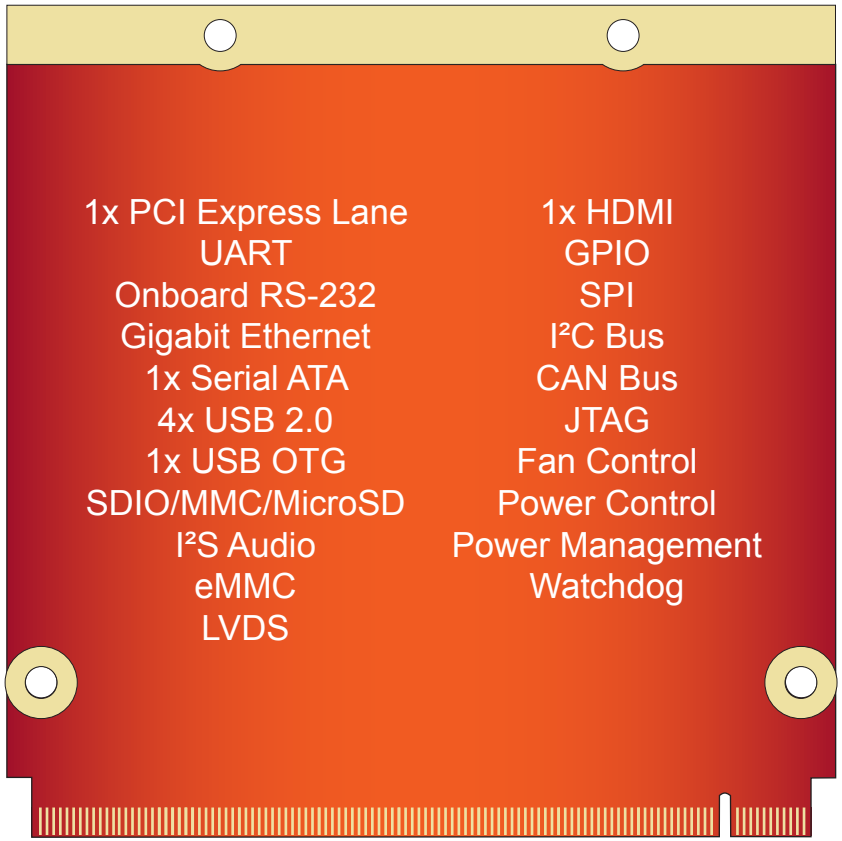




# 5 Connector Subsystems

The conga-QMX6 is based on the Qseven® standard and therefore has 115 edge fingers on the top and bottom side of the module that mate with the 230-pin card-edge MXM connector located on the carrier board. This connector provides the ability to interface the available signals of the conga-QMX6 with the carrier board peripherals.



## 5.1 PCI Express

The conga-QMX6 offers one PCI Express lane. The PCIe signals are routed from the NXP® i.MX6 SoC to the PCI Express port 0 of the conga-QMX6 edge finger. The clock from the SoC imits the speed of the PCI Express interface to Gen 1. Only x1 PCI Express link configuration is possible.

For more information about the PCI Express interface on the edge finger, refer to Table 11.

## 5.2 UART/RS-232

The conga-QMX6 offers one UART interface on the MXM connector and two RS-232 interfaces onboard. The UART offered on the MXM connector is fully featured with control signals (4 pin UART) and is connected directly to UART3 port of the NXP® i.MX6 Cortex A9 processor.

The conga-QMX6 offers the two onboard RS-232 interfaces via a 6-pin Molex connector. This connector is provided by routing the UART2 and UART5 pins of the NXP® i.MX6 processor to the MAXIM-3232 transceiver. The transceiver converts the Qseven® UART CMOS level (3.3V) to RS-232 voltage levels (5v) and is guaranteed to run at data rates of 250 kbps in the normal operating mode, while maintaining RS-232 output levels. With the Molex connector, you can output data to the console by using the appropriate RS-232 adapter cable.

The UART interfaces support speeds up to 4.0 Mbps and Non-Return-To-Zero encording format, RS-485 compatible 9 bit data format and IrDA compatible infrared slow data rate format.

**Note**

*You can realize a second UART interface on the MFG interface. This implementation however requires a customized conga-QMX6 variant. Contact congatec support for more information.*

*To display the u-boot output to console, you need an RS-232 adapter cable (PN: 48000023). See section 10.1 "UART/RS-232 Debug Port" for more information about the RS-232 adapter cable and the UART pin description.*

**Caution**

*The MFG_NC4 pin is high active on the conga-QMX6 module. This means that the MFG interface on the edge connector functions as JTAG interface by default. Therefore, do not use the MFG interface for UART purposes or externally pull the MFG_NC4 pin to ground. Failure to adhere to this warning may result to back-driving which can damage the module.*

*If you need the UART function on the MFG interface, then you require a customized conga-QMX6. For more information, contact congatec support.*

## 5.3 Gigabit Ethernet

The conga-QMX6 revision E.x offers Gigabit Ethernet with the integration of Texas Instruments DP83867. This transceiver is implemented via the RGMII interface of the i.MX6 processor. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MDI0± to GBE0_MDI3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

The conga-QMX6 revision C.x and B.x offer Gigabit Ethernet with the integration of Qualcomm Atheros Gigabit Transceiver. Earlier revisions offer Gigabit Ethernet with the integration of Micrel KSZ 9031 Ethernet PHY.

**Note**

*The theoretical maximum performance of 1 Gbps Ethernet is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For more information, consult NXP's Errata ERR004512.*

*Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information, refer to section 9.1 "Bootstrap Signals" of this user's guide.*

## 5.4 SATA

The NXP® i.MX6 Cortex A9 processor on the conga-QMX6 supports one SATA port only. The supported signals are coupled with 10nF capacitors and then routed to conga-QMX6 edge finger. The conga-QMX6 offers this SATA port on the MXM connector. This port supports SATA I (1.5Gbps) and SATA II (3Gbps) and is compliant with SATA specification 3.0, AHCI specification 1.3 and Advanced Microcontroller Bus Architecture (AMBA) specification 2.0.

**Note**

*SATA interface is only supported on conga-QMX6 quad and dual core variants. Solo core and dual lite variants do not support SATA.*

## 5.5 USB 2.0

The conga-QMX6 offers five USB ports via USB 2.0 host controllers provided by the NXP® i.MX6 Cortex A9 processor. These controllers provide high performance USB functionality that complies with USB 2.0 specification and with OTG supplement.

The offered ports comprise of one USB OTG port and four USB hosts. These four USB hosts are derived through the integration of an SMSC USB hub, and are implemented by routing the USB H1 port of the processor to the SMSC Hub. The USB OTG port (OTG client) is connected directly to the USB_OTG port of the i.MX6 processor.

The OTG client port can drop the hosting role and act as a normal USB device when conga-QMX6 is attached to another host. The direction of OTG port depends on the USB control signal (USB_ID). If asserted high, the OTG is set to client and if low, the OTG port is set to host. All ports are capable of supporting USB 1.1 and 2.0 compliant devices.

## 5.6 SD/SDIO/MMC

SDIO stands for Secure Digital Input Output. Devices that support SDIO can use small devices such as SD-Card or MMC-Card flash memories. The SD/SDIO/MMC cards communicate with the host system via the Ultra Secured Digital Host Controller (uSDHC). This controller acts as a bridge by sending commands and accessing data to and from the cards. The NXP® i.MX6 processor on the conga-QMX6 provides SD/SDIO/MMC controllers (SD1-SD4) for communicating with different SD, SDIO and MMC devices.

The conga-QMX6 offers one SDIO interface on the MXM connector via the NXP® i.MX6 SD4 port. Two other SDIO ports provided by the NXP® i.MX6 processor are supported onboard the conga-QMX6. These ports (SD2 and SD3) connect the onboard 4 bit micro SD and the onboard 8 bit eMMC respectively

The SDIO ports support SDIO Revision 1.1, SD Memory Card Specification Revision 3.0 and MMC Revision 4.4.

## 5.7 HDA/I2S/AC'97

The conga-QMX6 uses the I2S format for audio signals. These signals are derived from the Synchronous Serial Interface (SSI) of the NXP® i.MX6 processor. The SSI is a full duplex serial port that allows communication with external devices using a variety of serial protocols. The I2S protocol is part of the protocols supported by the NXP® i.MX6 Cortex A9 processor. The SSI supports up to 1.4 Mbps.

**Note**

*The conga-QMX6 currently supports only I2S format.*

## 5.8 LVDS

The LVDS Display Bridge (LDB) from the NXP® i.MX6 Cortex A9 processor found on the conga-QMX6 offers two LVDS channels, with up to 170 Mhz pixel clock. Each channel consists of one clock pair and four data pairs. The LDB supports the flow of synchronous RGB data from the Image Processing Unit (IPU) to external display devices through LVDS interface.

The LVDS interface supports 18 bit and 24 bit dual channel. The LVDS interface also supports various resolutions but with stipulated maximum data rates. The data rates supported are as follows:

For single channel output: Up to 85 MHz per interface (e.g 1366x768 @ 60 Hz + 35 % blanking).

For dual channel output: Up to 170 MHz pixel clock (e.g 1600x1200 @ 60Hz + 35 % blanking)

The LVDS ports support the following configurations:

- One single channel output
- One dual channel output single input split to two output channels
- Two identical outputs: single input sent to both output channels
- Two independent outputs: two inputs sent, each to a different output channel

**Note**

*The LVDS interface can be configured as a single channel, a dual channel or as two independent single LVDS channels. The actual configuration depends on the Operating System. For more information, contact congatec technical solution center.*

*Three independent displays are possible when connected as two single LVDS channel and one HDMI interface.*

## 5.9 HDMI®

High-Definition Multimedia Interface (HDMI®) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI® encodes the video data into TMDS for digital transmission and is backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video.

The conga-QMX6 provides HDMI® connection directly from the NXP® i.MX6 processor. Video data is provided through three differential TMDS data pairs (TMDS_LANE0± to TMDS_LANE2±) and one differential clock pair (TMDS_CLK±). In addition, the conga-QMX6 includes one standard I2C interface (I2C2_SDA and I2C2_SCL) for configuring and testing the HDMI 3D Tx PHY and a pin (DP_HDMI_HPD) for HDMI® hot plug detection support.

## 5.10 LPC/GPIO

The conga-QMX6 does not support the Low Pin Count (LPC) signals, instead eight GPIO pins shared with the LPC pins according to Qseven specification 2.0 are supported.

The General Purpose Input/Output pins can be configured as inputs or outputs. When configured as output, it is possible to write to an internal register to control the state driven on the output pin. When configured as input, the input state can be detected by reading the status of an internal register. To select the GPIO mode, configure the IOMUX.

## 5.11 SPI

The NXP® i.MX6 processor provides Enhanced Configurable Serial Peripheral Interfaces (ECSPIs) capable of up to 66 Mbps write speed and 31 Mbps read speed. The ECSPI interfaces offer full-duplex, synchronous serial interface with maximum operation frequency up to the reference clock frequency. It can be configured to support Master/Slave modes and four chip selects to support multiple peripherals.

The conga-QMX6 offers one SPI interface on the edge finger connector. Another SPI interface from the NXP® i.MX6 processor is connected to the 32 Mbit SPI Flash memory onboard the conga-QMX6. The NXP® i.MX6 processor is programmed to boot from the bootloader contained in the SPI flash memory.

## 5.12 CAN Bus

The conga-QMX6 supports CAN bus. The CAN controller performs communication in accordance with the CAN Protocol Version 2.0B Active1 (standard format and extended format). The bit rate can be programmed to a maximum of 1 Mbit/s, based on the technology used. To connect the CAN controller module to the CAN bus, it is necessary to add transceiver hardware. A complete description of the CAN controller registers and functionality is beyond the scope of this user's guide. Consult NXP's i.MX6 processor reference manual for additional information about this interface.

## 5.13 Manufacturing/JTAG Interface

The manufacturing signals defined in Qseven Specification 2.0 are reserved for either manufacturing or debugging purposes. The conga-QMX6 offers this interface as a 10-pin JTAG interface, for debugging purposes. This interface is connected to the JTAG controller of the NXP® i.MX6 processor. The JTAG control fuses are used to allow or disallow JTAG access to secured resources.

**Note**

*For compatible JTAG adapters, contact the congatec support team or order the Nit6X_JTAG from Boundary Devices.*

## 5.14 Power Control

### PWGIN

The PWGIN (pin 26) can be connected to an external power good circuit or it may also be utilized as a manual reset input. To use PWGIN as a manual reset input, the pin must be grounded through the use of a momentary-contact push-button switch. When external circuitry asserts this signal, it is necessary that an open-drain driver drives this signal causing it to be held low for a minimum of 16ms to initiate a reset. Using this input is optional. For more information, see the note below.

### SUS_S3#

The SUS_S3# (pin 18) signal shuts off power to all runtime system components that are not maintained during suspend mode. This signal is an output signal and is connected to the Power Management Integrated Circuit (PMIC). See Table 26 for more information.

### PWRBTN#

When using ATX-style power supplies, PWRBTN# (pin 20) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off.

**Note**

*The conga-QMX6 boots up immediately power is applied to the module's +5v input rail. To shutdown the system, use the the linux command "poweroff". Depending on the operating system, the shutdown can also be performed by pressing the power button. If the system is in shutdown or standby state, pressing the power button restores the system back to full-on state. When the chip main power supply is Off, a button press greater in duration than 750 ms asserts an output signal to request power from a power IC to power up the SoC.*

*If it's desired to keep the system switched off even when the +5V input power rail is initially powered on (ATX-style), an external logic has to be used that prevents the system from booting by means of the power good signal (PWGIN). It is the responsibility of the external logic to release the PWGIN signal, when the desired event (e.g. pressing the power button) occurs.*

## Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-QMX6. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. When designing a power supply for a conga-QMX6 application, a carrier board designer should be aware of the important information below:

- It has been noticed that on some occasions, problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

## Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush-current on the conga-QMX6 VCC_5V_SB power rail can go up as high as 2.3A for a maximum of 100µS. Sufficient decoupling capacitance must be implemented to ensure proper power-up sequencing. The maximum peak-current on the conga-QMX6 VCC (5V) power rail can be as high as 3.0A. This requires that the power supply be properly dimensioned.

**Note**

*For more information about power control event signals refer to the Qseven® specification.*

# 5.15 Power Management

Onboard the conga-QMX6 is a 14 channel configurable Power Management Integrated Circuit (PMIC). The PMIC provides a cost effective programmable power management solution for a wide range of applications. This high efficiency, configurable power management IC is designed to work seamlessly with NXP® processors. The NXP® i.MX6 cortex A9 processor uses advanced integration Power Management Unit (PMU) to reduce supply connections. The PMIC complements the processor's internal regulators in providing a complete and simple way to supply voltage domain with different voltages when needed.

The PMIC features four bulk regulators (up to six independent outputs), one boost regulator, six general purpose LDOs, one switch/LDO combination and a DDR voltage reference to supply voltages for the application processor and peripheral devices.

With integrated memory power, RTC supply and additional bulk and linear regulators to power system peripherals, multiple point of power supply across the PCB is drastically reduced.

## 5.16 Watchdog

The watchdog timer (WDOG) protects against system failures by providing a method of escaping from unexpected events or programming errors. The software must periodically service the watchdog timer once the WDOG is activated. Without the servicing, the timer times out.

The NXP® i.MX6 processor on the conga-QMX6 offers two watchdog timers - a watchdog timer integrated within the ARM Cortex A9 platform and a TrustZone watchdog timer.

## 5.17 I2C Bus

The I2C bus is suitable for applications requiring occasional communications over a short distance between many devices. The I2C interfaces offered by the NXP® i.MX6 processor support up to 400 kbps, depending on pin loading and timing characteristics

The conga-QMX6 offers three I2C interfaces (I2C1, I2C2 and I2C3) on the Qseven edge connector. The I2C2 and I2C3 buses on the edge connector are shared with some onboard devices - I2C3 is shared with LVDS and RTC while I2C2 is shared with camera interface and HDMI®. The I2C1 bus is routed directly without sharing on the edge connector.

**Note**

*On the conga-QMX6 revision B.x and later, we implemented a multiplexer on the I2C2 interface. The multiplexer separates the PMIC functions from other devices (camera, HDMI®) that share the bus. Due to this implementation, the user needs to download the latest kernel from git.congatec.com/public or at least ensure the congatec I2C multiplexer patches (CGT000031, CGT000032) are applied to the desired kernel, to achieve proper behaviour.*

*The I2C3 is also available on the SMBus signals (pin 60 and 62) of the Qseven edge connector.*

# 6 Additional Features

## 6.1 High Assurance Boot (HAB)

The High Assurance Boot is a software library executed in internal ROM on the NXP® processor at boot time, which among other things, authenticates software in external memory by verifying digital signatures. The HAB enables the ROM to authenticate software which executes immediately after ROM, by using digital signatures. This software is usually a bootloader. The High Assurance Boot component of the ROM protects against the potential threat of attackers modifying areas of code or data in programmable memory to make it behave in an incorrect manner.

## 6.2 Dedicated Hardware Accelerators

The NXP® i.MX6 processor uses dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption while having the CPU core relatively free for performing other tasks. The hardware accelerators available in the processor are VPU, IPUv3H, 3D GPU, 2D GPU, OpenVG 1.1 GPU and Asynchronous Sample Rate Converter (ASRC).

## 6.3 Power Management

The NXP® i.MX6 processor integrates power management functions to simplify system power management requirements. The processor provides power management units for offering power to various Soc domains. Temperature sensor for monitoring the die temperature is also provided.

Dynamic Voltage and Frequency Scaling techniques, software state retention, power gating and various levels of system power mode are supported. The use of simple and low-cost power regulators in place of complicated external power management ICs reduces system design cost.

## 6.4 Dynamic Voltage and Frequency Scaling

Dynamic Voltage and Frequency Scaling is a power management technique used in changing the clock frequency and/or the operating voltage of a processor based on system performance requirements at any point in time. This scaling is normally carried out during less demanding periods of nominal run speed. In General, it helps in balancing the performance demands of processor with the high amount of power needed to satisfy those demands.

## 6.5 Smart Speed Technology

The NXP's Smart Speed Technology with enhanced Cycles Per Instruction (eCPI) determines the speed of the processor by the set of tasks to be performed instead of the clock speed. The set of tasks determines the execution units needed to make sure the system work more efficiently. This ensures that the system provides enough performance without wasting resources.

With the Smart Speed Technology, several execution units work in parallel, thereby providing higher processor speed at lower power consumption. System parallelism is accomplished via the Smart Speed crossbar switch that nearly eliminates wait states. This results in improved processor performance without power consumption penalty associated with higher operating frequencies.

By employing Smart Speed Technology, portable devices can run longer, retain smaller form factors and support more innovative applications without substantially increasing the battery power.

## 6.6 Suspend Mode

The Suspend Mode feature is available on the conga-QMX6.

# 7 ARM Technologies

## 7.1 Media Processing Engine (MPE-NEON)

The Media Processing Engine (MPE-NEON) is a single instruction multiple data (SIMD) instruction set that provides flexible and powerful acceleration for media and signal processing applications. Support for a wide range of multimedia codecs with fewer cycles helps in enhancing user experience. NEON is used for multimedia data processing.

## 7.2 Jazelle DBX

The Jazelle is an instruction set that introduces technological infrastructure for running java codes faster than the software based java virtual machine. The Jazelle DBX (Direct Bytecode eXecution) enabled cores execute the majority of Java bytecodes in hardware. No modification is required in the application code to take advantage of this technology. To configure and turn on the Jazelle DBX, the software support code needs to be integrated into a Java Virtual Machine (JVM). Contact ARM for further information on how to obtain the software support code.

## 7.3 TrustZone

The ARM TrustZone technology is a security extension that provides additional dedicated security to a System on Chip (SoC). This technology aims to provide a framework that enables a device to counter many of the specific threats that it will experience. The security of the system is achieved by partitioning all of the SoC's hardware and software resources so that they exist in one of two worlds - the secure world (more trusted) and the normal world (less trusted). The memory and peripherals are then made aware of the operating world of the core and may use this to provide access control to secrets and code in the device.

## 7.4 Floating Point Unit

The Floating Point Unit (FPU) provides significant acceleration for both single and double precision scalar Floating-Point operations. It provides industry leading image processing, graphics and scientific computation capabilities. The FPU provides an optimized solution in performance, power and area for embedded applications and high performance for general purpose applications.

# 8 conga Tech Notes

The conga-QMX6 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

## 8.1 NXP® i.MX6 Processor Features

### 8.1.1 Temperature Monitor (TEMPMON)

The NXP® i.MX6 Cortex A9 processors have a temperature sensor module that implements a temperature sensor/conversion function based on a temperature-dependent voltage to time conversion.

The module features an alarm function that can raise an interrupt signal if the temperature is above a specified threshold. A self repeating mode can also be programmed which executes a temperature sensing operation based on a programmed delay.

Software can use this module to monitor the on-die temperature and take appropriate actions such as throttling back the core frequency when a temperature interrupt is set.

During normal system operation, software can use the temperature sensor counter output in conjunction with the fused temperature calibration data to determine the on-die operational temperature or to set an over-temperature interrupt alarm to within a couple of degree centigrade.

## 8.2 Thermal Management

To meet low power design requirement while maintaining a high performance operation, the NXP® iMX6 incorporated several low power design techniques. Even with these techniques, it is vital to manage the heat dissipation of the module in accordance with internal and external conditions.

The conga-QMX6 employs basically two types of thermal management strategies:

**Active Cooling**

During this cooling policy, the operating system turns the fan on/off. Though the active thermal management technique provides better heat dissipation and lower thermal resistances, the cooling solutions are however expensive and have large form factors.

### Passive Cooling

The passive cooling policy employs the technique of enhancing conduction and natural convection. This passive thermal management procedure provides cost effective cooling solutions up to certain power levels without introducing reliability concerns. Some of these techniques typically used are thermal gap fillers, heatspreaders and heat shields.

## 8.3 Audio Mux

Audio Mux (AUDMUX) is one of the modules found in the audio subsystem of the NXP® i.MX6 processor. It provides flexible programmable routing of the on-chip serial interfaces to and from off-chip devices. The AUDMUX includes internal port that connect to the processor serial interfaces and external ports that connect to off-chip audio devices. Connection is established by configuring the appropriate host and peripheral ports. Though controlled by ARM, the AUDMUX can route data even when the ARM is in a low-power mode.

## 8.4 LVDS Bridge

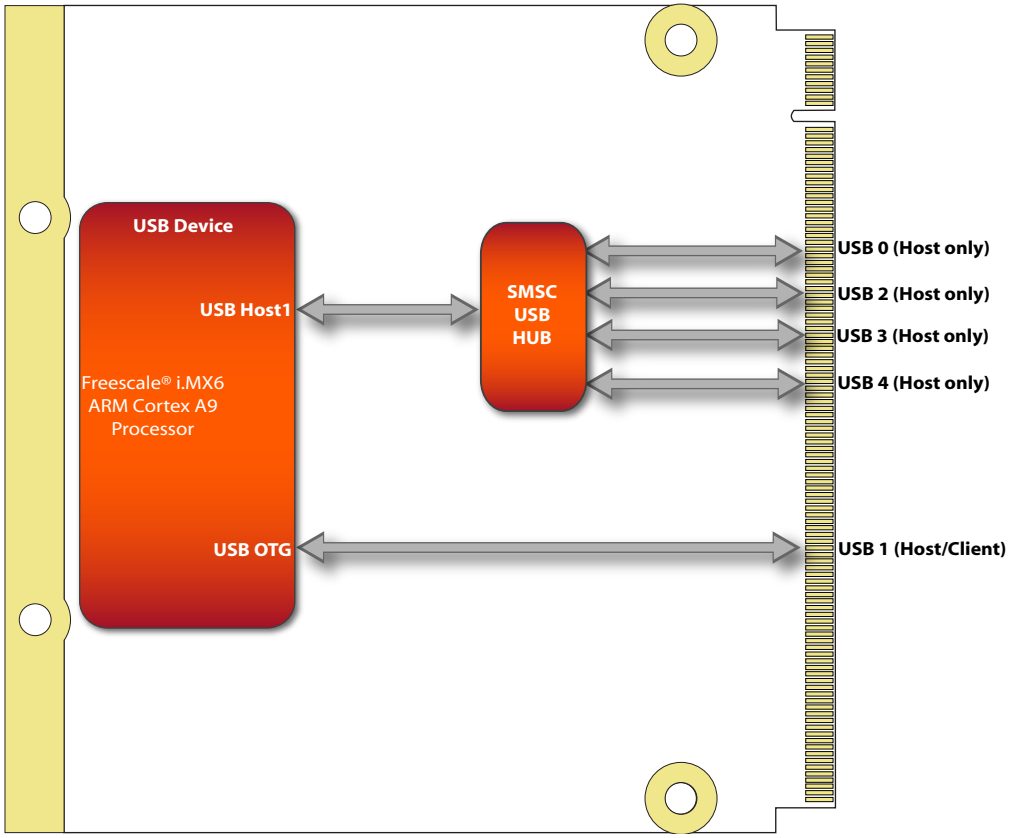
The LVDS Bridge (LDB) supports the flow of synchronous RGB data from the Image Processing Unit to external devices through LVDS interface. This support includes synchronization and control capabilities, connectivitity to relevant devices as well as proper data arrangement as required by the external display receiver and by LVDS display standards.

## 8.5 USB Port Connections

The conga-QMX6 offers a total of 5 USB ports (one USB OTG port and four Host-only ports). The four Host-only ports found on the conga-QMX6 are implemented by routing one Host-only port (USB H1) from the NXP® i.MX6 processor to the conga-QMX6 edge finger via a SMSC USB Hub.

The USB_OTG port (OTG client) of the conga-QMX6 is routed directly to the USB_OTG port of the i.MX6 processor. This port can drop the hosting role and act as a normal USB device when conga-QMX6 is attached to another host. It is also used as a downstream and upstream port while the Host-only cores are used as downstream ports.

For more information refer to the conga-QMX6 USB routing diagram shown below:



# 9 Interface - Signal Descriptions and Pinout Tables

The following section describes the signals found on Qseven® module's edge fingers and the interfaces implemented on the conga-QMX6.

The table below describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a Qseven® module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

**Note**

*The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.*

*Not all the signals described in this section are available on all conga-QMX6 variants. Use the article number of the module and refer to the options table on page 8 to determine the options available on the module.*

Table 9 Signal Tables Terminology Descriptions

| Term | Description |
|---|---|
| I | Input pin |
| O | Output pin |
| OC | Open collector |
| OD | Open drain |
| PP | Push pull |
| I/O | Bi-directional Input/Output Pin |
| 3.3VSB | 3.3V tolerant active in standby state |
| P | Power input |
| NA | Not applicable |
| NC | Not connected |
| PCIE | PCI Express differential pair signals. In compliance with the PCI Express Base Specification 1.0a. |
| GB_LAN | Gigabit Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet Specification. |
| USB | Universal Serial Bus differential pair signals. In compliance with the Universal Serial Bus Specification 2.0 |
| SATA | Serial Advanced Technology Attachment differential pair signals. In compliance with the Serial ATA High Speed Serialized AT Attachment Specification 1.0a. |
| SPI | Serial Peripheral Interface bus is a synchronous serial data link that operates in full duplex mode. |
| CAN | Controller Area Network bus is a vehicle bus standard that allows microcontrollers and devices to communicate with each other within a vehicle without a host computer. |
| LVDS | Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0. |
| TMDS | Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0. |
| CMOS | Logic input or output. |

Table 10 Edge Finger Pinout

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | GND | 2 | GND |
| 3 | GBE_MDI3- | 4 | GBE_MDI2- |
| 5 | GBE_MDI3+ | 6 | GBE_MDI2+ |
| 7 | GBE_LINK100# | 8 | GBE_LINK1000# |
| 9 | GBE_MDI1- | 10 | GBE_MDI0- |
| 11 | GBE_MDI1+ | 12 | GBE_MDI0+ |
| 13 | GBE_LINK# | 14 | GBE_ACT# |
| 15 | GBE_CTREF (*) | 16 | SUS_S5# |
| 17 | WAKE# | 18 | SUS_S3# |
| 19 | SUS_STAT#* | 20 | PWRBTN# |
| 21 | SLP_BTN# | 22 | LID_BTN# |
| 23 | GND | 24 | GND |
| 25 | GND | 26 | PWGIN |
| 27 | BATLOW# | 28 | RSTBTN# |
| 29 | SATA0_TX+ | 30 | SATA1_TX+(*) |
| 31 | SATA0_TX- | 32 | SATA1_TX- (*) |
| 33 | SATA_ACT# | 34 | GND |
| 35 | SATA0_RX+ | 36 | SATA1_RX+ (*) |
| 37 | SATA0_RX- | 38 | SATA1_RX- (*) |
| 39 | GND | 40 | GND |
| 41 | BIOS_DISABLE# / BOOT_ALT# | 42 | SDIO_CLK |
| 43 | SDIO_CD# | 44 | SDIO_LED |
| 45 | SDIO_CMD | 46 | SDIO_WP |
| 47 | SDIO_PWR# | 48 | SDIO_DAT1 |
| 49 | SDIO_DAT0 | 50 | SDIO_DAT3 |
| 51 | SDIO_DAT2 | 52 | SDIO_DAT5 |
| 53 | SDIO_DAT4 | 54 | SDIO_DAT7 |
| 55 | SDIO_DAT6 | 56 | USB_DRIVE_VBUS |
| 57 | GND | 58 | GND |
| 59 | HDA_SYNC / I2S_WS | 60 | SMB_CLK / GP1_I2C_CLK |
| 61 | HDA_RST# / I2S_RST# | 62 | SMB_DAT / GP1_I2C_DAT |
| 63 | HDA_BITCLK / I2S_CLK | 64 | SMB_ALERT# |
| 65 | HDA_SDI / I2S_SDI | 66 | GP0_I2C_CLK |
| 67 | HDA_SDO / I2S_SDO | 68 | GP0_I2C_DAT |
| 69 | THRM# | 70 | WDTRIG# |
| 71 | THRMTRIP# | 72 | WDOUT |
| 73 | GND | 74 | GND |
| 75 | USB_P7- / USB_SSTX0- | 76 | USB_P6- / USB_SSRX0- |
| 77 | USB_P7+ / USB_SSTX0+ | 78 | USB_P6+ / USB_SSRX0+ |

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 79 | USB_6_7_OC# | 80 | USB_4_5_OC# |
| 81 | USB_P5- / USB_SSTX1- | 82 | USB_P4- / USB_SSRX1- |
| 83 | USB_P5+ / USB_SSTX1+ | 84 | USB_P4+ / USB_SSRX1+ |
| 85 | USB_2_3_OC# | 86 | USB_0_1_OC# |
| 87 | USB_P3- | 88 | USB_P2- |
| 89 | USB_P3+ | 90 | USB_P2+ |
| 91 | USB_VBUS | 92 | USB_ID |
| 93 | USB_P1- | 94 | USB_P0- |
| 95 | USB_P1+ | 96 | USB_P0+ |
| 97 | GND | 98 | GND |
| 99 | eDP0_TX0+ / LVDS_A0+ | 100 | eDP1_TX0+ / LVDS_B0+ |
| 101 | eDP0_TX0- / LVDS_A0- | 102 | eDP1_TX0- / LVDS_B0- |
| 103 | eDP0_TX1+ / LVDS_A1+ | 104 | eDP1_TX1+ / LVDS_B1+ |
| 105 | eDP0_TX1- / LVDS_A1- | 106 | eDP1_TX1- / LVDS_B1- |
| 107 | eDP0_TX2+ / LVDS_A2+ | 108 | eDP1_TX2+ / LVDS_B2+ |
| 109 | eDP0_TX2- / LVDS_A2- | 110 | eDP1_TX2- / LVDS_B2- |
| 111 | LVDS_PPEN | 112 | LVDS_BLEN |
| 113 | eDP0_TX3+ / LVDS_A3+ | 114 | eDP1_TX3+ / LVDS_B3+ |
| 115 | eDP0_TX3- / LVDS_A3- | 116 | eDP1_TX3- / LVDS_B3- |
| 117 | GND | 118 | GND |
| 119 | eDP0_AUX+ / LVDS_A_CLK+ | 120 | eDP1_AUX+ / LVDS_B_CLK+ |
| 121 | eDP0_AUX- / LVDS_A_CLK- | 122 | eDP1_AUX- / LVDS_B_CLK- |
| 123 | LVDS_BLT_CTRL /GP_PWM_OUT0 | 124 | GP_1-Wire_Bus |
| 125 | GP2_I2C_DAT / LVDS_DID_DAT | 126 | eDP0_HPD# / LVDS_BLC_DAT |
| 127 | GP2_I2C_CLK / LVDS_DID_CLK | 128 | eDP1_HPD# / LVDS_BLC_CLK |
| 129 | CAN0_TX | 130 | CAN0_RX |
| 131 | DP_LANE3+ / TMDS_CLK+ | 132 | RSVD (Differential Pair) |
| 133 | DP_LANE3- / TMDS_CLK- | 134 | RSVD (Differential Pair) |
| 135 | GND | 136 | GND |
| 137 | DP_LANE1+ / TMDS_LANE1+ | 138 | DP_AUX+ |
| 139 | DP_LANE1- / TMDS_LANE1- | 140 | DP_AUX- |
| 141 | GND | 142 | GND |
| 143 | DP_LANE2+ / TMDS_LANE0+ | 144 | RSVD (Differential Pair) |
| 145 | DP_LANE2- / TMDS_LANE0- | 146 | RSVD (Differential Pair) |
| 147 | GND | 148 | GND |
| 149 | DP_LANE0+ / TMDS_LANE2+ | 150 | HDMI_CTRL_DAT |
| 151 | DP_LANE0- / TMDS_LANE2- | 152 | HDMI_CTRL_CLK |
| 153 | DP_HDMI_HPD# | 154 | RSVD |
| 155 | PCIE_CLK_REF+ | 156 | PCIE_WAKE# |
| 157 | PCIE_CLK_REF- | 158 | PCIE_RST# |
| 159 | GND | 160 | GND |

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 161 | PCIE3_TX+ | 162 | PCIE3_RX+ |
| 163 | PCIE3_TX- | 164 | PCIE3_RX- |
| 165 | GND | 166 | GND |
| 167 | PCIE2_TX+ | 168 | PCIE2_RX+ |
| 169 | PCIE2_TX- | 170 | PCIE2_RX- |
| 171 | UART0_TX | 172 | UART0_RTS# (optionally, UART0_CTS#) |
| 173 | PCIE1_TX+ | 174 | PCIE1_RX+ |
| 175 | PCIE1_TX- | 176 | PCIE1_RX- |
| 177 | UART0_RX | 178 | UART0_CTS# (optionally, UART0_RTS#) |
| 179 | PCIE0_TX+ | 180 | PCIE0_RX+ |
| 181 | PCIE0_TX- | 182 | PCIE0_RX- |
| 183 | GND | 184 | GND |
| 185 | LPC_AD0 / GPIO0 | 186 | LPC_AD1 / GPIO1 |
| 187 | LPC_AD2 / GPIO2 | 188 | LPC_AD3 / GPIO3 |
| 189 | LPC_CLK / GPIO4 | 190 | LPC_FRAME# / GPIO5 |
| 191 | SERIRQ / GPIO6 | 192 | LPC_LDRQ# / GPIO7 |
| 193 | VCC_RTC | 194 | SPKR / GP_PWM_OUT2 |
| 195 | FAN_TACHOIN / GP_TIMER_IN | 196 | FAN_PWMOUT / GP_PWM_OUT1 |
| 197 | GND | 198 | GND |
| 199 | SPI_MOSI | 200 | SPI_CS0# |
| 201 | SPI_MISO | 202 | SPI_CS1# |
| 203 | SPI_SCK | 204 | MFG_NC4 |
| 205 | VCC_5V_SB | 206 | VCC_5V_SB |
| 207 | MFG_NC0 | 208 | MFG_NC2 |
| 209 | MFG_NC1 | 210 | MFG_NC3 |
| 211 | VCC | 212 | VCC |
| 213 | VCC | 214 | VCC |
| 215 | VCC | 216 | VCC |
| 217 | VCC | 218 | VCC |
| 219 | VCC | 220 | VCC |
| 221 | VCC | 222 | VCC |
| 223 | VCC | 224 | VCC |
| 225 | VCC | 226 | VCC |
| 227 | VCC | 228 | VCC |
| 229 | VCC | 230 | VCC |

**Note**

*The conga-QMX6 does not support the signals marked with asterisk symbol (*).*

Table 11 PCI Express Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| PCIE0_RX+<br>PCIE0_RX- | 180<br>182 | PCI Express channel 0, Receive Input differential pair. | I PCIE | | Supports PCI Express Base Specification, Revision 1.0a. |
| PCIE0_TX+<br>PCIE0_TX- | 179<br>181 | PCI Express channel 0, Transmit Output differential pair. | O PCIE | | Supports PCI Express Base Specification, Revision 1.0a. |
| PCIE1_RX+<br>PCIE1_RX- | 174<br>176 | PCI Express channel 1, Receive Input differential pair. | I PCIE | | Not supported. |
| PCIE1_TX+<br>PCIE1_TX- | 173<br>175 | PCI Express channel 1, Transmit Output differential pair. | O PCIE | | Not supported. |
| PCIE2_RX+<br>PCIE2_RX- | 168<br>170 | PCI Express channel 2, Receive Input differential pair. | I PCIE | | Not supported. |
| PCIE2_TX+<br>PCIE2_TX- | 167<br>169 | PCI Express channel 2, Transmit Output differential pair. | O PCIE | | Not supported. |
| PCIE3_RX+<br>PCIE3_RX- | 162<br>164 | PCI Express channel 3, Receive Input differential pair. | I PCIE | | Not supported. |
| PCIE3_TX+<br>PCIE3_TX- | 161<br>163 | PCI Express channel 3, Transmit Output differential pair. | O PCIE | | Not supported. |
| PCIE_CLK_REF+<br>PCIE_CLK_REF- | 155<br>157 | PCI Express Reference Clock Signals for Lanes 0 to 3. | O PCIE | | The clock from the SoC limits the speed of the PCI Express interface to Gen 1. |
| PCIE_WAKE# | 156 | PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup. | I 3.3VSB | PU 1k 3.3VSB | Connected to GPIO |
| PCIE_RST# | 158 | Reset Signal for external devices. | O 3.3V | | |

Table 12 UART Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| UART0_TX | 171 | Serial Data Transmitter | O 3.3V | | UART3_TX signal from Processor |
| UART0_RX | 177 | Serial Data Reciever | I 3.3V | | UART3_RX signal from Processor |
| UART0_CTS# | 178 | Handshake signal, ready to send data | I 3.3V | | UART3_CTS# signal from Processor |
| UART0_RTS# | 172 | Handshake signal, ready to receive data | O 3.3V | | UART3_RTS# signal from Processor |

**Note**

*The UART0_CTS# and UART0_RTS# signals are switched in revisions A.x and B.x. The switched signals have been corrected in revision C.x and E.x. Optionally, the signals can be switched back to their incorrect configuration (assembly option).*

Table 13 Ethernet Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| GBE_MDI0+<br>GBE_MDI0- | 12<br>10 | Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes.<br>This signal pair is used for all modes. | I/O Analog | | Twisted pair signals for external transformer. |
| GBE_MDI1+<br>GBE_MDI1- | 11<br>9 | Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes.<br>This signal pair is used for all modes. | I/O Analog | | Twisted pair signals for external transformer. |
| GBE_MDI2+<br>GBE_MDI2- | 6<br>4 | Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes.<br>This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode. | I/O Analog | | Twisted pair signals for external transformer. |
| GBE_MDI3+<br>GBE_MDI3- | 5<br>3 | Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes.<br>This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode. | I/O Analog | | Twisted pair signals for external transformer. |
| GBE_CTREF | 15 | Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V.<br>The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less. | REF | | Not Supported |
| GBE_LINK# | 13 | Ethernet controller 0 link indicator, active low. | O 3.3V PP | PD 1k | GBE0_LINK# is a bootstrap signal (see note below) |
| GBE_LINK100# | 7 | Ethernet controller 0 100Mbit/sec link indicator, active low. | O 3.3V PP | PU 4k99 2,5VSB | Not Supported. Internally connected to GBE_ACT#.<br>GBE0_LINK100# is a bootstrap signal (see note below) |
| GBE_LINK1000# | 8 | Ethernet controller 0 1000Mbit/sec link indicator, active low. | O 3.3V PP | PD 1k | Not Supported. Internally connected to GBE_LINK#.<br>GBE0_LINK1000# is a bootstrap signal (see note below) |
| GBE_ACT# | 14 | Ethernet controller 0 activity indicator, active low. | O 3.3V PP | PU 4k99 2,5VSB | GBE0_ACT# is a bootstrap signal (see note below) |

**Note**

*The theoretical maximum performance of 1 Gbps Ethernet is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For more information, consult NXP's Errata ERR004512.*

*Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information, refer to section 9.1 of this user's guide.*

Table 14 SATA Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| SATA0_RX+<br>SATA0_RX- | 35<br>37 | Serial ATA channel 0, Receive Input differential pair. | I SATA | | Supports Serial ATA specification, Revision 3.0 |
| SATA0_TX+<br>SATA0_TX- | 29<br>31 | Serial ATA channel 0, Transmit Output differential pair. | O SATA | | Supports Serial ATA specification, Revision 3.0 |
| SATA1_RX+<br>SATA1_RX- | 36<br>38 | Serial ATA channel 1, Receive Input differential pair. | I SATA | | Not supported |
| SATA1_TX+<br>SATA1_TX- | 30<br>32 | Serial ATA channel 1, Transmit Output differential pair. | O SATA | | Not supported |
| SATA_ACT# | 33 | Serial ATA Led. Open collector output pin driven during SATA command activity. | OC 3.3V | | Not supported |

**Note**

*The NXP® i.MX6 does not support SATA on Solo and Dual Core Lite CPUs. Only Quad Core and Dual Core variants support SATA.*

Table 15 USB 2.0 Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| USB_P0+<br>USB_P0- | 96<br>94 | Universal Serial Bus Port 0 differential pair. | I/O | | USB 2.0 compliant. Backwards compatible to USB 1.1 |
| USB_P1+<br>USB_P1- | 95<br>93 | Universal Serial Bus Port 1 differential pair.<br>If USB_ID is LOW (default) = USB Host<br>If USB_ID is tied HIGH = USB device (Client) | I/O | | If USB_ID is LOW (default) = USB 2.0 compliant Host. Backwards compatible to USB 1.1<br>If USB_ID is HIGH = USB 2.0 Client. Backwards compatible to USB 1.1 |
| USB_P2+<br>USB_P2- | 90<br>88 | Universal Serial Bus Port 2 differential pair. | I/O | | USB 2.0 compliant. Backwards compatible to USB 1.1 |
| USB_P3+<br>USB_P3- | 89<br>87 | Universal Serial Bus Port 3 differential pair. | I/O | | USB 2.0 compliant. Backwards compatible to USB 1.1 |
| USB_P4+<br>USB_P4-<br>USB_SSRX1+<br>USB_SSRX1- | 84<br>82 | Universal Serial Bus Port 4 differential pair.<br><br>Multiplexed with receive signal differential pairs for the Superspeed USB data path. | I/O<br><br>I | | USB 2.0 compliant. Backwards compatible to USB 1.1.<br>No USB 3.0 available |
| USB_P5+<br>USB_P5-<br>USB_SSTX1+<br>USB_SSTX1- | 83<br>81 | Universal Serial Bus Port 5 differential pair.<br><br>Multiplexed with transmit signal differential pairs for the Superspeed USB data path | I/O<br><br>O | | Not supported |
| USB_P6+<br>USB_P6-<br>USB_SSRX0+<br>USB_SSRX0- | 78<br>76 | Universal Serial Bus Port 6 differential pair.<br><br>Multiplexed with receive signal differential pairs for the Superspeed USB data path | I/O<br><br>I | | Not supported |

| | | | | | |
|---|---|---|---|---|---|
| USB_P7+<br>USB_P7-<br>USB_SSTX0+<br>USB_SSTX0- | 77<br>75 | Universal Serial Bus Port 7 differential pair.<br><br>Multiplexed with transmit signal differential pairs for the Superspeed USB data path | I/O<br><br>O | | Not supported |
| USB_0_1_OC# | 86 | Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1. | I 3.3VSB | PU 10k 3.3V | |
| USB_2_3_OC# | 85 | Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3. | I 3.3VSB | PU 10k 3.3V | |
| USB_4_5_OC# | 80 | Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5. | I 3.3VSB | PU 10k 3.3V | |
| USB_6_7_OC# | 79 | Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7. | I 3.3VSB | PU 10k 3.3VSB | Not supported |
| USB_ID | 92 | USB ID pin.<br>Configures the mode of the USB Port 1. The resistance of this pin measured to ground is used to determine whether USB Port 1 is going to be used as USB Client to enable/ disable USB Client support. Please check the USB-OTG Reference of your chip manufacturer for further details. | Analog Output | | Functions as USB_OTG_PEN<br>"Added possibility to use Qseven goldfinger contact 92 (one wire bus) for HDMI-CEC or ENET 1588." |
| USB_VBUS | 91 | USB VBUS pin:<br>- 5V tolerant<br>- VBUS resistance has to be placed on the module<br>- VBUS capacitance has to be placed on the carrier board | I 5.0V Passive Analog | PD 10k GND | |
| USB_OTG_PEN | 56 | USB Power enable pin for USB Port 1<br>Enables the Power for the USB-OTG port on the carrier board. | O CMOS 3.3V | | |

Table 16 SDIO/MMC Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| SDIO_CD# | 43 | SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. | I/O 3.3V | PU 10k 3.3V | |
| SDIO_CLK | 42 | SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz. | O 3.3V | | |
| SDIO_CMD | 45 | SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. | I/O 3.3V OD/PP | PU 10k 3.3V | |
| SDIO_LED | 44 | SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus. | O 3.3V | PU 10k 3.3V | |
| SDIO_WP | 46 | SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. | I/O 3.3V | PU 10k 3.3V | |
| SDIO_PWR# | 47 | SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device. | O 3.3V | | Connected to GPIO |

| | | | | | |
|---|---|---|---|---|---|
| SDIO_DAT0<br>SDIO_DAT1<br>SDIO_DAT2<br>SDIO_DAT3<br>SDIO_DAT4<br>SDIO_DAT5<br>SDIO_DAT6<br>SDIO_DAT7 | 49<br>48<br>51<br>50<br>53<br>52<br>55<br>54 | SDIO Data lines. These signals operate in push-pull mode. | I/O 3.3V<br>PP | | |

Table 17 HDA/I2S/SPDIF Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| HDA_RST#<br>I2S_RST# | 61 | HD Audio/AC'97 Codec Reset.<br>Multiplexed with I2S Codec Reset. | O 3.3V | | Connected to GPIO |
| HDA_SYNC<br>I2S_WS | 59 | Serial Bus Synchronization.<br>Multiplexed with I2S Word Select from Codec. | O 3.3V | | |
| HDA_BITCLK<br>I2S_CLK | 63 | HD Audio/AC'97 24 MHz Serial Bit Clock from Codec.<br>Multiplexed with I2S Serial Data Clock from Codec. | O 3.3V | | |
| HDA_SDO<br>I2S_SDO | 67 | HD Audio/AC'97 Serial Data Output to Codec.<br>Multiplexed with I2S Serial Data Output from Codec. | O 3.3V | | |
| HDA_SDI<br>I2S_SDI | 65 | HD Audio/AC'97 Serial Data Input from Codec.<br>Multiplexed with I2S Serial Data Input from Codec. | I 3.3V | | |

**Note**

*The conga-QMX6 currently supports only I2S format.*

Table 18 LVDS Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| LVDS_PPEN | 111 | Controls panel power enable. | O 3.3V | | |
| LVDS_BLEN | 112 | Controls panel Backlight enable. | O 3.3V | | |
| LVDS_BLT_CTRL<br>/GP_PWM_OUT0 | 123 | Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output. | O 3.3V | | |
| LVDS_A0+<br>LVDS_A0-<br>eDP0_TX0+<br>eDP0_TX0- | 99<br>101 | LVDS primary channel differential pair 0.<br><br>Display Port primary channel differential pair 0. | O LVDS | | |
| LVDS_A1+<br>LVDS_A1-<br>eDP0_TX1+<br>eDP0_TX1- | 103<br>105 | LVDS primary channel differential pair 1.<br><br>Display Port primary channel differential pair 1. | O LVDS | | |

| | | | | | |
|---|---|---|---|---|---|
| LVDS_A2+<br>LVDS_A2-<br>eDP0_TX2+<br>eDP0_TX2- | 107<br>109 | LVDS primary channel differential pair 2.<br><br>Display Port primary channel differential pair 2. | O LVDS | | |
| LVDS_A3+<br>LVDS_A3-<br>eDP0_TX3+<br>eDP0_TX3- | 113<br>115 | LVDS primary channel differential pair 3.<br><br>Display Port primary channel differential pair 3. | O LVDS | | |
| LVDS_A_CLK+<br>LVDS_A_CLK-<br>eDP0_AUX+<br>eDP0_AUX- | 119<br>121 | LVDS primary channel differential pair clock lines.<br><br>Display Port primary auxiliary channel. | O LVDS | | |
| LVDS_B0+<br>LVDS_B0-<br>eDP1_TX0+<br>eDP1_TX0- | 100<br>102 | LVDS secondary channel differential pair 0.<br><br>Display Port secondary channel differential pair 0. | O LVDS | | |
| LVDS_B1+<br>LVDS_B1-<br>eDP1_TX1+<br>eDP1_TX1- | 104<br>106 | LVDS secondary channel differential pair 1.<br><br>Display Port secondary channel differential pair 1. | O LVDS | | |
| LVDS_B2+<br>LVDS_B2-<br>eDP1_TX2+<br>eDP1_TX2- | 108<br>110 | LVDS secondary channel differential pair 2.<br><br>Display Port secondary channel differential pair 2. | O LVDS | | |
| LVDS_B3+<br>LVDS_B3-<br>eDP1_TX3+<br>eDP1_TX3- | 114<br>116 | LVDS secondary channel differential pair 3.<br><br>Display Port secondary channel differential pair 3. | O LVDS | | |
| LVDS_B_CLK+<br>LVDS_B_CLK-<br>eDP1_AUX+<br>eDP1_AUX- | 120<br>122 | LVDS secondary channel differential pair clock lines.<br><br>Display Port secondary auxiliary channel. | O LVDS | | |
| LVDS_DID_CLK<br>/GP2_I2C_CLK | 127 | Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used, it can be as General Purpose I²C bus clock line. | I/O 3.3V OD | PU 4k7 3.3V | |
| LVDS_DID_DAT<br>/GP2_I2C_DAT | 125 | Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus data line. | I/O 3.3V OD | PU 4k7 3.3V | |
| LVDS_BLC_CLK<br>eDP1_HPD# | 128 | Control clock signal for external SSC clock chip. If the primary functionality is not used, it can be used as an emedded DisplayPort secondary Hotplug detection. | I/O 3.3V OD | PU 4k7 3.3V | Not supported |
| LVDS_BLC_DAT<br>eDP0_HPD# | 126 | Control data signal for external SSC clock chip.<br>If the primary functionality is not used, it can be used as an embedded DisplayPort primary Hotplug detection. | I/O 3.3V OD | PU 4k7 3.3V | Not supported |

**Note**

*The LVDS interface can be used either as a single channel or as a dual channel. It is also possible to use the LVDS interface as two independent single LVDS channels. To do this, it is recommended to configure the LVDS display in the bootloader.*

Table 19 DisplayPort Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| DP_LANE3+<br>DP_LANE3- | 131<br>133 | DisplayPort differential pair lines lane 3 (Shared with TMDS_CLK+ and TMDS_CLK-) | O PCIE | | DisplayPort interface not supported |
| DP_LANE2+<br>DP_LANE2- | 143<br>145 | DisplayPort differential pair lines lane 2 (Shared with TMDS_LANE0+ and TMDS_LANE0-) | O PCIE | | DisplayPort interface not supported |
| DP_LANE1+<br>DP_LANE1- | 137<br>139 | DisplayPort differential pair lines lane 1 (Shared with TMDS_LANE1+ and TMDS_LANE1-) | O PCIE | | DisplayPort interface not supported |
| DP_LANE0+<br>DP_LANE0- | 149<br>151 | DisplayPort differential pair lines lane 0 (Shared with TMDS_LANE2+ and TMDS_LANE2-) | O PCIE | | DisplayPort interface not supported |
| DP_AUX+<br>DP_AUX- | 138<br>140 | Auxiliary channel used for link management and device control. Differential pair lines. | I/O PCIE | | DisplayPort interface not supported |
| DP_HDMI_<br>HPD# | 153 | Hot plug detection signal that serves as an interrupt request. | I 3.3V | | DisplayPort interface not supported |

**Note**

*The conga-QMX6 does not offer DisplayPort interface because the interface is not supported by the NXP® i.MX6 processor.*

Table 20 HDMI® Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | |
|---|---|---|---|---|---|
| TMDS_CLK+<br>TMDS_CLK- | 131<br>133 | TMDS differential pair clock lines. | O TMDS | | HDMI® interface |
| TMDS_LANE0+<br>TMDS_LANE0- | 143<br>145 | TMDS differential pair lines lane 0. | O TMDS | | HDMI® interface |
| TMDS_LANE1+<br>TMDS_LANE1- | 137<br>139 | TMDS differential pair lines lane 1. | O TMDS | | HDMI® interface |
| TMDS_LANE2+<br>TMDS_LANE2- | 149<br>151 | TMDS differential pair lines lane 2. | O TMDS | | HDMI® interface |
| HDMI_CTRL_CLK | 152 | DDC based control signal (clock) for HDMI® device. | I/O 3.3V OD | PU 4k7 3.3V | HDMI® interface |
| HDMI_CTRL_DAT | 150 | DDC based control signal (data) for HDMI® device. | I/O 3.3V OD | PU 4k7 3.3V | HDMI® interface |
| DP_HDMI_HPD# | 153 | Hot plug detection signal that serves as an interrupt request. | I 3.3V | PD 100k | HDMI® interface |

**Note**

*On the conga-QMX6, only the HDMI® interface supports the Transition Minimized Differential Signaling (TMDS)*

Table 21 LPC/GPIO Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| LPC_AD0<br>GPIO0 | 185 | Multiplexed Command, Address and Data (LPC_AD[0..3]).<br>Shared with General Purpose Input/Output [0..3] | I/O 3.3V | | Shared with GPIO0 |
| LPC_AD1<br>GPIO1 | 186 | | | | Shared with GPIO1 |
| LPC_AD2<br>GPIO2 | 187 | | | | Shared with GPIO2 |
| LPC_AD3<br>GPIO3 | 188 | | | | Shared with GPIO3 |
| LPC_FRAME#<br>GPIO5 | 190 | LPC frame indicates the start of a new cycle or the termination of a broken cycle. Shared with General Purpose Input/Output 5 | I/O 3.3V | | Shared with GPIO5 |
| LPC_LDRQ#<br>GPIO7 | 192 | LPC DMA request.<br>General Purpose Input/Output 7 | I/O 3.3V | | Shared with GPIO7 |
| LPC_CLK<br>GPIO4 | 189 | LPC clock.<br>General Purpose Input/Output 4 | I/O 3.3V | | |
| SERIRQ<br>GPIO6 | 191 | Serialized Interrupt.<br>General Purpose Input/Output 6 | I/O 3.3V | | Shared with GPIO6 |

**Note**

*The eight LPC pins are configured by default as GPIO's. Additional eight GPIO pins can be achieved by configuring SDIO pins as GPIO. This can be programmed in the bootloader and in the kernel.*

*The conga-QMX6 does not support LPC interface.*

Table 22 SPI Interface Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| SPI_MOSI | 199 | Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device. | O 3.3V | | |
| SPI_MISO | 201 | Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module. | I 3.3V | | |
| SPI_SCK | 203 | SPI clock output. | O 3.3V | | |
| SPI_CS0# | 200 | SPI chip select 0 output. | O 3.3V | | |
| SPI_CS1# | 202 | SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used. | O 3.3V | | |

Table 23 CAN Bus Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| CAN0_TX | 129 | CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board. | O 3.3V | | |
| CAN0_RX | 130 | RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board. | I 3.3V | | |

Table 24 Input Power Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| VCC | 211-230 | Power Supply +5VDC ±5%. | P | | |
| VCC_5V_SB | 205-206 | Standby Power Supply +5VDC ±5%. | P | | |
| VCC_RTC | 193 | 3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V). | P | | |
| GND | 1, 2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198 | Power Ground. | P | | |

Table 25 Power Control Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| PWGIN | 26 | High active input for the Qseven® module indicates that power from the power supply is ready. | I 5V | PU 10k 5V | |
| PWRBTN# | 20 | Power Button: Low active power button input. This signal is triggered on the falling edge. **Note:** For proper detection, assert a pulse width of at least 16 ms. | I 3.3VSB | PU 10k 3.3V | |

Table 26 Power Management Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| RSTBTN# | 28 | Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module.<br>**Note:** For proper detection, assert a pulse width of at least 16 ms. | I 3.3V | | |
| BATLOW# | 27 | Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event. | I 3.3VSB | | Connected to GPIO |
| WAKE# | 17 | External system wake event. This may be driven active low by external circuitry to signal an external wake-up event. | I 3.3VSB | | |
| SUS_STAT# | 19 | Suspend Status: indicates that the system will be entering a low power state soon. | | | Not supported |
| SUS_S3# | 18 | S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states.<br>The signal SUS_S3# is necessary in order to support the optional S3 cold power state. | O 3.3VSB | | Connected to PMIC |
| SUS_S5# | 16 | S5 State: This signal indicates S4 or S5 (Soft Off) state. | O 3.3VSB | | Connected to PMIC |
| SLP_BTN# | 21 | Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.<br>**Note:** For proper detection, assert a pulse width of at least 16 ms. | I 3.3VSB | PU 10k 3.3VSB | Connected to GPIO |
| LID_BTN# | 22 | LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again.<br>**Note:** For proper detection, assert a pulse width of at least 16 ms. | I 3.3VSB | PU 10k 3.3VSB | Connected to GPIO |

Table 27 Miscellaneous Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| WDTRIG# | 70 | Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse. | I 3.3V | | Connected to GPIO |
| WDOUT | 72 | Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down. | O 3.3V | | Connected to GPIO<br>See note below |
| GP0_I2C_CLK | 66 | General Purpose I²C bus #0 clock line | I/O 3.3V OD | PU 4k7 3.3V | |
| GP0_I2C_DAT | 68 | General Purpose I²C bus #0 data line | I/O 3.3V OD | PU 4k7 3.3V | |
| SMB_CLK<br>/GP1_I2C_CLK | 60 | Clock line of System Management Bus.<br>Multiplexed with General Purpose I²C bus #1 clock line | I/O 3.3VSB OD | PU 4k7 3.3V | Connected to I2C |
| SMB_DAT<br>/GP1_I2C_DAT | 62 | Data line of System Management Bus.<br>Multiplexed with General Purpose I²C bus #1 data line | I/O 3.3VSB OD | PU 4k7 3.3V | Connected to I2C |
| SMB_ALERT# | 64 | System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus. | I/O 3.3VSB OD | PU 10k 3.3V | Connected to GPIO. |
| SPKR<br>/GP_PWM_OUT2 | 194 | Primary functionality is output for audio enunciator, the “speaker” in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output. | O 3.3V | | Not supported. |
| BIOS_DISABLE#<br>/BOOT_ALT# | 41 | Pin is used to select Boot mode. | I 3.3V | PU 4k7 3.3V | |

| | | | | | |
|---|---|---|---|---|---|
| RSVD | 132, 134, 144, 146, 154 | Do not connect | NC | | |
| GP_1-Wire_Bus | 124 | General Purpose 1-Wire bus interface. Can be used for consumer electronics control bus (CEC) of HDMI®. | I/O 3.3V | | Currently implemented as HDMI® Consumer Electronics Control Bus. |

**Note**

*The WDOUT signal is high by default on the conga-QMX6. Implement a reverse circuit on the carrier board to set the signal low by default.*

Table 28 Manufacturing/JTAG Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| MFG_NC0 | 207 | This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal. | NA | NA | |
| MFG_NC1 | 209 | This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal. | NA | NA | See caution statement below |
| MFG_NC2 | 208 | This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal. | NA | NA | See caution statement below |
| MFG_NC3 | 210 | This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal. | NA | NA | |
| MFG_NC4 | 204 | This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 ( JTAG / UART ). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes. | NA | NA | |

**Note**

*The MFG_NC0..4 pins are reserved for manufacturing and debugging purposes. It's recommended to route the signals to a connector on the carrier board. The carrier board must not drive the MFG_NC-pins or have pull-up or pull-down resistors implemented for these signals. MFG_NC0...4 are defined to have a voltage level of 3.3V. It must be ensured that the carrier board has the correct voltage levels for JTAG/ UART signals originating from the module. For this reason, a level shifting device may be required on the carrier board to guarantee that these voltage levels are correct in order to prevent damage to the module. More information about implementing a carrier board multiplexer can be found in the Qseven® Design Guide.*

**Caution**

*The MFG_NC4 pin is high active on the conga-QMX6 module. This means that the MFG interface on the edge connector functions by default as JTAG interface. Therefore, do not use the MFG interface for UART purposes or externally pull the MFG_NC4 pin to ground. Failure to adhere to this warning may result to back-driving which can damage the module.*

*If you need the UART function on the MFG interface, then you require a customized conga-QMX6. For more information, contact congatec support.*

Table 29 Thermal Management Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| THRM# | 69 | Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling. | I 3.3V | PU 10k 3.3V | Connected to GPIO |
| THRMTRIP# | 71 | Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off). | O 3.3V | | Connected to GPIO |

Table 30 Fan Control Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| FAN_PWMOUT /GP_PWM_OUT1 | 196 | Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output. | O 3.3V OC | | |
| FAN_TACHOIN /GP_TIMER_IN | 195 | Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input. | I 3.3V | | Connected to GPIO |

## 9.1 Bootstrap Signals

Table 31 Bootstrap Signal Descriptions

| Signal | Pin # | Description of Bootstrap Signal | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| GBE_LINK# | 13 | Ethernet controller 0 link indicator, active low. | O 2.5VSB | PU 4k99 | GBE0_LINK# is a bootstrap signal (see note below) |
| GBE_LINK100# | 7 | Ethernet controller 0 100Mbit/sec link indicator, active low. | O 2.5VSB | PU 1k 3.3V | Not Supported. Internally connected to GBE_ACT#. GBE0_LINK100# is a bootstrap signal (see note below) |
| GBE_LINK1000# | 8 | Ethernet controller 0 1000Mbit/sec link indicator, active low. | O 2.5VSB | PU 4k99 | Not Supported. Internally connected to GBE_LINK# GBE0_LINK1000# is a bootstrap signal (see note below) |
| GBE_ACT# | 14 | Ethernet controller 0 activity indicator, active low. | O 2.5VSB | PD 1k 3.3V | GBE0_ACT# is a bootstrap signal (see note below) |

**Caution**

*The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either Qseven® internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the Qseven® module to malfunction and/or cause irreparable damage to the module.*

*Additionally, if it is necessary to have link and activity LEDs connected to GBE_LINK# and GBE_ACT# on the carrier board, then you have to use buffers. Without a buffer, the strapping becomes active and this causes the PHY to be programmed with wrong address.*

# 10 Onboard Interfaces and Devices

## 10.1 UART/RS-232 Debug Port

The conga-QMX6 is equipped with a six-pin RS232 connector onboard the conga-QMX6. This RS-232 debug port is connected to the NXP® i.MX6 UART1 and UART2 pins via the MAXIM-3232 transceiver. The transceiver is guaranteed to run at data rates of 250kbps in normal operating mode, while maintaining RS-232 output levels.

Refer to section 5.2 for more information about the UART interface.

Table 32 UART Signal Descriptions

| Pin # | Signal (Molex Connector) | D-SUB 1 (Console) | D-SUB 2 | Description | Color |
|---|---|---|---|---|---|
| 1 | DCE1_TXT | NC | Pin 2 | i.MX6 UART 5 Serial Data Transmitter | Red |
| 2 | NC | NC | NC | Not Connected | - |
| 3 | GND | Pin 5 | Pin 5 | Ground | White |
| 4 | DCE2_TXT | Pin 2 | NC | UART 2 Serial Data Transmitter | Black |
| 5 | DCE2_RX | Pin 3 | NC | UART 2 Serial Data Receiver | Orange |
| 6 | DCE1_RX | NC | Pin 3 | i.MX6 UART 5 Serial Data Receiver | Purple |

**Note**

*The RS232 adapter cable (PN: 48000023) for the onboard UART interface is included in the congatec Qseven Evaluation kit. You can also order this cable separately from congatec GmbH. For more information, contact your congatec sales representative.*

## 10.2 MIPI/CMOS Camera

The NXP® i.MX6 Image Processing Unit (IPU) provides connectivity to cameras via the MIPI/CSI-2 transmitter and maintains image manipulation and processing with adequate synchronization and control. The Camera Serial Interface (CSI) controls the camera port and provides interface to an image sensor or a related device. The role of the camera ports is to receive input from video sources and to provide support for time-sensitive signals to the camera. Non-time-sensitive controls such as configuration, reset are performed by the ARM platform through I2C interface or GPIO signals

The table below shows the conga-QMX6 revision C.x and E.x MIPI pinout description. The pinout complies with the SGET Qseven Camera Feature Specification (an addendum to the Qseven Specification 2.0).

Table 33 MIPI Signal Descriptions

| Pin | Signal | Description | I/O Type | I/O | Comment |
|---|---|---|---|---|---|
| 1 | CAM_PWR | 3.3V +/- 5% supply voltage to power the camera device | 3.3V Power Output | P | |
| 2 | CAM_PWR | 3.3V +/- 5% supply voltage to power the camera device | 3.3V Power Output | P | |
| 3 | CAM0_CSI_D0+ | CSI2 Camera 0 Data Lane 0+ | D-PHY | I | |
| 4 | CAM0_CSI_D0- | CSI2 Camera 0 Data Lane 0- | D-PHY | I | |
| 5 | GND | | | P | |
| 6 | CAM0_CSI_D1+ | CSI2 Camera 0 Data Lane 1+ | D-PHY | I | |
| 7 | CAM0_CSI_D1- | CSI2 Camera 0 Data Lane 1- | D-PHY | I | |
| 8 | GND | | | P | |
| 9 | CAM0_CSI_D2+ | CSI2 Camera 0 Data Lane 2+ | D-PHY | I | |
| 10 | CAM0_CSI_D2- | CSI2 Camera 0 Data Lane 2- | D-PHY | I | |
| 11 | CAM0_RST# | Camera 0 Reset (low active) | CMOS 1.8V | O | |
| 12 | CAM0_CSI_D3+ | CSI2 Camera 0 Data Lane 3+ | D-PHY | I | |
| 13 | CAM0_CSI_D3- | CSI2 Camera 0 Data Lane 3- | D-PHY | I | |
| 14 | GND | | | P | |
| 15 | CAM0_CSI_CLK+ | CSI2 Camera 0 Differential Clock+ (Strobe) | D-PHY | I | |
| 16 | CAM0_CSI_CLK- | CSI2 Camera 0 Differential Clock- (Strobe) | D-PHY | I | |
| 17 | GND | | | P | |
| 18 | CAM0_I2C_CLK | Camera 0 Control Interface, CLK. (I²C like interface) | CMOS 1.8V OD | O | |
| 19 | CAM0_I2C_DAT | Camera 0 Control Interface, DATA. (I²C like interface) | CMOS 1.8V OD | I/O | |
| 20 | CAM0_ENA# | Camera 0 Enable (low active) | CMOS 1.8V | O | |
| 21 | MCLK | Master Clock. May be used by Cameras to drive it's internal PLL Frequency range: 6...27 MHz | CMOS 1.8V | O | |
| 22 | CAM1_ENA# | Camera 1 Enable (low active) | CMOS 1.8V | O | |
| 23 | CAM1_I2C_CLK | Camera 1 Control Interface, CLK. (I²C like interface) | CMOS 1.8V OD | O | Not Connected |
| 24 | CAM1_I2C_DAT | Camera 1 Control Interface, DATA. (I²C like interface) | CMOS 1.8V OD | I/O | Not Connected |

| | | | | | |
|---|---|---|---|---|---|
| 25 | GND | | | P | |
| 26 | CAM1_CSI_CLK+ | CSI2 Camera 1 Differential Clock+ (Strobe) | D-PHY | I | Not Connected |
| 27 | CAM1_CSI_CLK- | CSI2 Camera 1 Differential Clock- (Strobe) | D-PHY | I | Not Connected |
| 28 | GND | | | P | |
| 29 | CAM1_CSI_D0+ | CSI2 Camera 1 Data Lane 0+ | D-PHY | I | Not Connected |
| 30 | CAM1_CSI_D0- | CSI2 Camera 1 Data Lane 0- | D-PHY | I | Not Connected |
| 31 | CAM1_RST# | Camera 1 Reset (low active) | CMOS 1.8V | O | |
| 32 | CAM1_CSI_D1+ | CSI2 Camera 1 Data Lane 1+ | D-PHY | I | Not Connected |
| 33 | CAM1_CSI_D1- | CSI2 Camera 1 Data Lane 1- | D-PHY | I | Not Connected |
| 34 | GND | | | P | |
| 35 | CAM0_GPIO | GPIO for Camera 0 | CMOS 1.8V | I/O | |
| 36 | CAM1_GPIO | GPIO for Camera 1 | CMOS 1.8V | I/O | Also for alternative camera functions like flashlight (not specified in SGET spec.) |

**Note**

*conga-QMX6 Revision B.x:*

*For the camera interface on conga-QMX6 revision B.x to function correctly:*

1. *Use the latest kernel on the congatec git server. If you use older kernels (3.0.35_1.1.0 and 3.0.35_4.1.0), then you require a patch (available on the git server) to provide the correct supply voltage for the camera module. You do not need this patch if the camera is connected on the conga-MCB mini carrier board.*

2. *If you intend to connect camera module ACA1 to the camera interface, then make sure you use hardware revision X.1 of camera module ACA1 to provide 2.5V compliant signals.*

3. *Set the voltage level of the camera interface to 2.5V. You can achieve this voltage level in QMX6 bootloader version 2013.04 (cgt_imx_v2013.04_3.10.17_1.0.0) by setting the environment variable "lv_mipi" to the value "2V5".*

*For more information about the camera interface and the related requirements/modifications to the hardware, contact your dedicated congatec support representative.*

*conga-QMX6 Revision C.x and E.x:*

*The conga-QMX6 revision C.x provides 3.3V to the camera interface as defined by the SGET Camera Feature Specification. Because of this voltage level, the ACA1 hardware revision X.x is not compatible with the camera interface of conga-QMX6 revision C.x and E.x. Therefore, use only hardware revision A.x of the camera module ACA1 (See the caution below).*

**Caution**

*The ACA1 camera module, hardware revision X.x is not compatible with the conga-QMX6 C.x and E.x because of the difference in supply voltage levels. Therefore, use only hardware revision A.x of camera module ACA1 or newer on conga-QMX6 revision C.x and E.x.*

*Do not use hardware revision X.x of the ACA1 camera module on the conga-QMX6 C.x or E.x. You will damage the camera module and/or the QMX6 module if you do not adhere to this instruction.*

## 10.3 JTAG Interface

The conga-QMX6 offers an onboard 10-pin JTAG interface. For compatible JTAG adapters, contact congatec support team or use the Nit6X_JTAG adapter Boundary Devices.

Table 34 JTAG Interface Signal Descriptions

| Pin # | Signal |
|---|---|
| 1 | P3V3_DELAYED |
| 2 | JTAG_TMS_B |
| 3 | GND |
| 4 | JTAG_TCK_B |
| 5 | GND |
| 6 | JTAG_TDO_B |
| 7 | JTAG_MOD_B |
| 8 | JTAG_TDI_B |
| 9 | JTAG_nTRST |
| 10 | JTAG_RSTBTN# |

## 10.4 SPI Flash

Onboard the conga-QMX6 is a 32 Mbit SPI flash memory. This flash memory contains the bootloader and is directly connected to the ECSPI-1 interface of the i.MX6 processor.

The NXP® i.MX6 processor is programmed to boot from the SPI flash.

## 10.5 Android Buttons

Table 35 Android Button Signal Descriptions

Onboard the conga-QMX6 is an eight pin connector for implementing android buttons. The signals are directly connected to the NXP® i.MX6 processor.

| Signal | Pin # | Description | I/O |
|---|---|---|---|
| PWRBTN# | 1 | Power button signal | |
| KEY_VOL_UP | 2 | Increases volume | GPIO7_13 |
| HOME | 3 | Returns to the main home screen | GPIO2_4 |
| SEARCH | 4 | Brings up the search function | GPIO2_3 |
| BACK | 5 | Takes you a level back in an app or a page back in a browser | GPIO2_2 |
| MENU | 6 | Displays additional options in an application | GPIO2_1 |
| KEY_VOL_DN | 7 | Decreases volume | GPIO4_5 |
| GND | 8 | Ground | |

## 10.6 DDR3L Memory

The conga-QMX6 offers up to 4GB DDR3L SDRAM memory onboard. The memory modules are connected directly to the DDR ports of the NXP® i.MX6 processor.

## 10.7 eMMC

The conga-QMX6 revision E.x offers a 32GB eMMC module onboard. The onboard eMMC is a nand flash device and it is routed directly to the SDIO port 3 of the NXP® i.MX6 processor. Eight lanes are used for data. Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology. The performance of the newer eMMC may vary depending on the eMMC technology.

**Note**

*For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions.*

## 10.8 Micro SD

The conga-QMX6 offers an onboard micro SD connector (backside of the module). It is connected to the SDIO port 2 of the NXP® i.MX6 processor. Four lanes are used for data. Revision E.x supports 1.8V and 3.3V cards. Previous revisions only support 3.3V cards.