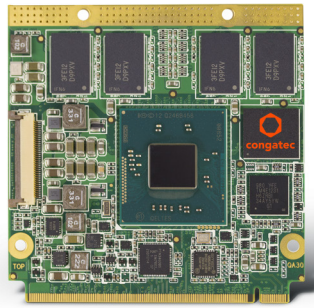
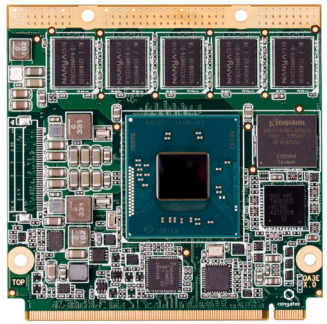


conga-QA3/QA3E

Qseven® 2.0 Module with 3rd Generation Intel® Processors



User's Guide

Revision 1.5

congatec

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
1.0	2015.10.16	AEM	• Merged the conga-QA30 with the conga-QA3E user's guide, to create a single user's guide. Revision 1.0 is the first revision for the combined user's guide • Added note about USB overcurrent protection in section 5.5 "USB 2.0", section 7.3 "xHCI & EHCI Port Mapping" and table 9 "USB Signal Description"
1.1	2017.06.20	AEM	• Corrected and updated the Intel® Atom™ E3805 processor features in section 1.2 "conga-QA3 Variants". Also added note about the default serial direction settings of the headless variants • Updated section 2.5 "Power Consumption" • Updated section 5.15 "Power Control" • Added note about UART limitation in section 5.8 "UART" • Corrected the list of reserved pins in table 21 "Miscellaneous Signal Descriptions" • Updated section 10 "BIOS Setup Description" and section 11 "Additional BIOS Features"
1.2	2019.01.07	BEU	• Updated table numbering and references throughout the document • Updated information about handling electrostatic sensitive devices in preface section • Updated section 2.1 "Feature List" • Removed references to conga-MA3/MA3E in section 4 "Block Diagram" • Updated entire section 4 "Cooling Solutions" • Updated reference to power supply design guide in section 5.15 "Power Control" • Added lifespan information and usage note to section 6.1.2 "eMMC 4.5" • Added note about min. pulse width to several button signals in table 27 and 28 • Updated support flash device in section 11.4 "Supported Flash Devices" • Updated section 12 "Industry Specifications"
1.3	2021.02.19	BEU	• Corrected the storage temperature for industrial variants in section 2.7 "Environmental Specifications"
1.4	2021.04.15	BEU	• Updated display interfaces in table 1, 2, 3, 12, 22 and section 3 "Block Diagram", 5 "Connector Subsystems", 5.10 "Digital Display Interface", 5.10.2 "DP++ Port" • Deleted section 5.10.3 "HDMI", 5.10.4 "DVI", 12 "Industry Specifications"
1.5	2024.01.15	BEU	• Updated title page • Updated congatec AG to congatec GmbH • Updated RoHS Directive • Added note to section 2.7 "Environmental Specifications" • Added note and caution to section 4 "Cooling Solutions" • Corrected UART assembly option in section 3 "Block Diagram", 5.8 "UART", and Table 14 "UART Signal Descriptions"

Preface

This user's guide provides information about the components, features, connector and BIOS Setup menus available on the conga-QA3/QA3E. It is one of three documents that should be referred to when designing a Qseven® application. The other reference documents that should be used include the following:

Qseven® Design Guide

Qseven® Specification

The links to these documents can be found on the congatec GmbH website at www.congatec.com

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Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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Terminology

Term	Description
PCIe	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4, x8, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4, x8, or x16 link.
eMMC	Embedded Multi-media Controller
SD card	Secure Digital card is a non-volatile memory card format developed for use in portable devices.
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial-interface standard for hard disks
HDA	High Definition Audio
DDI	Digital Display Interface
DP	DisplayPort is a VESA open digital communications interface.
TMDS	Transition Minimized Differential Signaling
LPC	Low Pin-Count is a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy device support into a single IC.
I²C Bus	Inter-Integrated Circuit Bus is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system.
SM Bus	System Management Bus is a popular derivative of the I²C-bus.
SPI Bus	Serial Peripheral Interface is a synchronous serial data link standard that operates in full duplex mode.
GbE	Gigabit Ethernet
LVDS	Low-Voltage Differential Signaling
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

Contents

List of Tables

1 Introduction

1.1 Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector. The pinout remains the same regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The Qseven® evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose what are suitable for their application. Qseven® applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no need to redesign the carrier board.

This document describes the features available on the Qseven® evaluation carrier board. Additionally, the schematics for the Qseven® evaluation carrier board can be found on the congatec website.

1.2 conga-QA3 Options Information

The conga-QA3 is available in various variants (commercial and industrial).This user's guide describes all of these variants and the table below shows the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Table 1 conga-QA3 (Commercial Variants)

Part-No	015100	015101	015102	015103	015104	015105
Processor	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3827 (Dual Core, 1.75 GHz)	Intel® Atom™ E3826 (Dual Core, 1.46 GHz)	Intel® Atom™ E3825 (Dual Core, 1.33 GHz)	Intel® Atom™ E3815 (Single Core, 1.46 GHz)	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)
L2 Cache	2 MB	1 MB	1 MB	1 MB	512kB	2 MB
Onboard Memory	2GB DDR3L-1333 dual channel	2GB DDR3L-1333 dual channel	2GB DDR3L-1066 dual channel	2GB DDR3L-1066 single channel	2GB DDR3L-1066 single channel	4GB DDR3L-1333 dual channel
Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics
GFX Normal/ Burst	542 / 792	542 / 792	533 / 667	533 / N.A	400 / N.A	542 / 792
LVDS	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit
DDI	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)
eMMC	4 GB	4 GB	4 GB	4 GB	4 GB	8 GB
SD Card	Yes	Yes	Yes	Yes	Yes	Yes
Max. TDP	10 W	8 W	7 W	6 W	5 W	10 W

Part-No.	015106	015107	015108	015109	015111
Processor	Intel® Atom™ E3815 (Single Core, 1.46 GHz)	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3827 (Dual Core, 1.75 GHz)	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Celeron® J1900 (Quad Core, 2.0/2.42 GHz)
L2 Cache	512kB	2 MB	1 MB	2 MB	2 MB
Onboard Memory	1GB DDR3L-1066 single channel	4GB DDR3L-1333 dual channel	4GB DDR3L-1333 dual channel	2GB DDR3L-1333 dual channel	2GB DDR3L-1333 dual channel
Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics
GFX Normal/ Burst	400 / N.A	542 / 792	542 / 792	542 / 792	688 / 854
LVDS	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit
DDI	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)
eMMC	N.A	N.A	N.A	N.A	N.A
SD Card	Yes	Yes	Yes	Yes	Yes
Max. TDP / SDP	5 W	10 W	8 W	10 W	10 W

Part-No.	015112	015113	015130	015131
Processor	Intel® Celeron® N2930 (Quad Core, 1.83/2.16 GHz)	Intel® Celeron® N2807 (Dual Core, 1.58/2.16 GHz)	Intel® Atom™ E3805 (Dual Core, 1.33 GHz)	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)
L2 Cache	2 MB	1 MB	1 MB	2 MB
Onboard Memory	2GB DDR3L-1333 dual channel	2GB DDR3L-1333 single channel	2GB DDR3L-1066 single channel	8GB DDR3L-1333 dual channel
Graphics	Intel® HD Graphics	Intel® HD Graphics	None	Intel® HD Graphics
GFX Normal/Burst	313 / 854	313 / 750	N.A	542 / 792
LVDS	Single/Dual 18/24bit	Single/Dual 18/24bit	N.A	Single/Dual 18/24bit
DDI	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)
eMMC	N.A	N.A	4 GB	16 GB
SD Card	Yes	Yes	Yes	Yes
Max. TDP / SDP	7.5 / 4.5 W	4.3 / 2.5 W	3 W / N.A	10 W

Table 2 conga-QA3 (Industrial Variants)

Part-No	015120	015121	015123	015124	015125	015126
Processor	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3827 (Dual Core, 1.75 GHz)	Intel® Atom™ E3825 (Dual Core, 1.33 GHz)	Intel® Atom™ E3815 (Single Core, 1.46 GHz)	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3805 (Dual Core, 1.33 GHz)
L2 Cache	2 MB	1 MB	1 MB	512kB	2 MB	1 MB
Onboard Memory	2GB DDR3L-1333 dual channel	2GB DDR3L-1333 dual channel	2GB DDR3L-1066 single channel	2GB DDR3L-1066 single channel	4GB DDR3L-1333 dual channel	2GB DDR3L-1066 single channel
Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	None
GFX Normal/Burst	542 / 792	542 / 792	533 / N.A	400 / N.A	542 / 792	N.A
LVDS	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	Single/Dual 18/24bit	N.A
DDI	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)
eMMC	4 GB	4 GB	4 GB	4 GB	8 GB	4 GB
SD Card	Yes	Yes	Yes	Yes	Yes	Yes
Max. TDP / SDP	10 W / N.A	8 W / N.A	6 W / N.A	5 W / N.A	10 W / N.A	3 W / N.A

Note

On the conga-QA3 variant that features the Intel Atom E3805 (variants without graphic engine), serial redirection is enabled in the BIOS by default and outputted via the onboard UART.

1.3 conga-QA3E Options Information

The conga-QA3E is available in two variants. The table below shows the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Table 3 conga-QA3E (Commercial Variants)

Part-No	018104	018105
Processor	Intel® Atom™ E3815 (Single Core, 1.46 GHz)	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)
L2 Cache	512kB	2 MB
Onboard Memory	2GB DDR3L-1066 single channel ECC	4GB DDR3L-1333 single channel ECC
Graphics	Intel® HD Graphics	Intel® HD Graphics
GFX Normal/Burst	400 / N.A	542 / 792
LVDS	Single/Dual 18/24bit	Single/Dual 18/24bit
DDI	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)
eMMC	4 GB (MLC)	8 GB (MLC)
SD Card	Yes	Yes
Max. TDP / SDP	5 W / N.A	10 W / N.A

2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	Based on Qseven® form factor specification revision 2.0	
Processor	Intel®Atom™ E3845 /E3827 /E3826 /E3825 /E3815 Intel® Celeron J1900 /N2930 /N2807	
Memory	**conga:QA3:** Up to 4 GB single channel or up to 8 GB dual channel non-ECC DDR3L onboard memory interface with data rates up to 1333 MT/s. Variants equipped with Intel Atom E3815 or Intel Celeron N2807 feature single channel memory interface. For more information, see Options Information tables on page 11, 12 and 13. **conga:QA3E:** Single channel ECC DDR3L onboard memory interface with up to 8 GB and data rates up to 1333 MT/s. For more information, see conga-QA3E Options Information table on page 13.	
Chipset	Integrated in SoC	
Onboard Storage	eMMC 4.5 onboard flash up to 32 GB (optional only for variants equipped with Intel® Atom™)	
Audio	High Definition Audio (HDA) interface with support for multiple codecs	
Ethernet	Gigabit Ethernet via the onboard Intel® Ethernet controller I210.	
Graphics Options	Intel® HD Graphics with support for DirectX11, OpenGL 3.2, OpenCL 1.2, OpenGLES 2.0, full HW acceleration for decode/encode of MPEG2, H.264, MVC and dual simultaneous display support	
	Flat LVDS (Integrated flat panel interface with 25-112MHz single/dual-channel LVDS Transmitter). Supports: - Single-channel LVDS interface: 1 x 18 bpp or 1 x 24 bpp. - Dual-channel LVDS interface : 2 x 18 bpp or 2 x 24 bpp. - VESA LVDS color mappings - Automatic Panel Detection via Embedded Panel Interface based on VESA EDID™ 1.3. - Resolution up to 1920x1200 in dual LVDS bus mode. Optional eDP interface **NOTE**: Either eDP or LVDS signals supported, not both signal types simultaneously.	1x DDI with support for DP++ (DP/HDMI™/DVI) **NOTE**: The conga-QA3/QA3E does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.
Peripheral Interfaces	2x Serial ATA® up to 3Gb/s 3x PCI Express® Gen2 links up to 5.0 GT/s per lane USB Interfaces: - 6x USB 2.0 or - 1x USB 3.0 and 5x USB 2.0 1x SD/MMC	MIPI-CSI 2.0 (supported only on conga-QA3/QA3E revision B.x or newer) UART SPI Bus LPC Bus I²C Bus, multimaster
BIOS Features	AMI Aptio® UEFI 5.x firmware; 8 MByte serial SPI with congatec Embedded BIOS features (OEM Logo, OEM CMOS Defaults, LCD Control, Display Auto Detection, Backlight Control, Flash Update)	
Power Mgmt.	ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).	
congatec Board Controller	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, bios setup data backup, I²C bus (fast mode, 400 kHz, multi-master), power loss control	

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on pages 11, 12 and 13 of this user's guide to determine what options are available on your particular module.

2.2 Supported Operating Systems

The conga-QA3/QA3E supports the following operating systems:

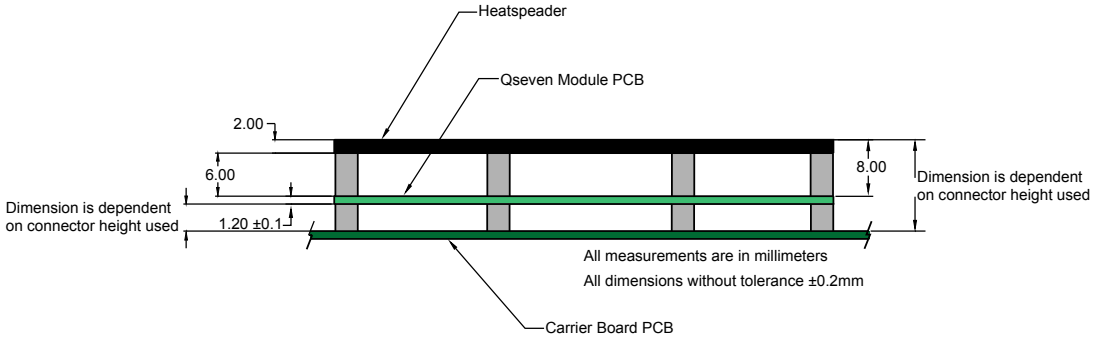
- Microsoft® Windows® 7
- Microsoft® Windows® Embedded Compact 7
- Microsoft® Windows® Embedded Standard 7
- Microsoft® Windows® 8
- Microsoft® Windows® Embedded Standard 8
- Microsoft® Windows® 10
- Linux (Timesys Fedora 18)

Note

For the installation of Windows 7/8 and WES7/8, congatec GmbH recommends a minimum storage capacity of 16 GB. congatec will not offer support for systems with less than 16 GB storage space.

2.3 Mechanical Dimensions

- 70.0 mm x 70.0 mm @ (2 ¾" x 2 ¾")
- The Qseven™ module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.

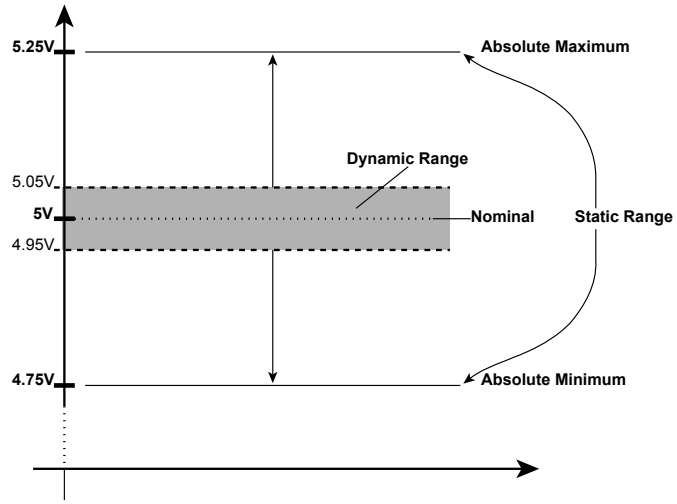


Rear View of Qseven Module

2.4 Supply Voltage Standard Power

- 5V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Characteristics			Min.	Typ.	Max.	Units	Comment
5V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV_{PP}	0-20MHz
	Current						
5V_SB	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple				± 50	mV_{PP}	

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

Note

For information about the input power sequencing of the Qseven® module refer to the Qseven® specification.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-QA3/QA3E COM
- modified congatec carrier board
- conga-QA3/QA3E cooling solution
- Microsoft Windows 7 (64 bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool

The power consumption values were recorded during the following system states:

Table 5 Measurement Description

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle.	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency.
S0: Peak value	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.
S3	COM is powered by VCC_5V_SBY.	
S5	COM is powered by VCC_5V_SBY.	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Processor Information

The table below provide additional information about the power consumption data for each of the conga-QA3/QA3E variants offered. The values are recorded at various operating mode.

Table 6 Power Consumption Values

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (Amp.)				
					Variant	Cores	Freq/Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5
015100 015120	2 GB	A.1	QA30R004	Windows 7	Intel® Atom™ E3845	4	1.91/N.A	0.63	1.45	2.21	0.08	0.06
015101 015121	2 GB	A.1	QA30R004	Windows 7	Intel® Atom™ E3827	2	1.75/N.A	0.78	1.10	1.92	0.07	0.05
015102 015122	2 GB	A.2	QA30R004	Windows 7	Intel® Atom™ E3826	2	1.46/N.A	0.63	1.45	2.21	0.07	0.07
015103 015123	2 GB	A.1	QA30R000	Windows 7	Intel® Atom™ E3825	2	1.33/N.A	0.38	0.61	1.00	0.09	0.07
015104 015124	2 GB	A.2	QA30R000	Windows 7	Intel® Atom™ E3815	1	1.46/N.A	0.37	0.54	0.79	0.07	0.06
015111	2 GB	A.2	QA30R004	Windows 7	Intel® Celeron® J1900	4	2.00/2.42	0.77	2.02	3.01	0.07	0.05
015112	2 GB	A.4	QA32R013	Windows 7	Intel® Celeron® N2930	4	1.83/2.16	0.63	1.55	1.96	0.06	N.A
015113	2 GB	A.3	QC31R115	Windows 7	Intel® Celeron® N2807	2	1.58/2.16	0.40	0.96	1.55	0.06	0.05
015130	2 GB	A.4	QA30R004	Windows 7	Intel® Atom™ E3805	2	1.33/N.A	0.20	0.27	0.29	0.07	0.05
018104	2 GB	A.0	QA30R004	Windows 7	Intel® Atom™ E3815	1	1.46/N.A	0.42	0.60	0.99	0.07	N.A
018105	2 GB	A.0	QA30R004	Windows 7	Intel® Atom™ E3845	4	1.91/N.A	0.45	1.36	2.10	0.06	N.A

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 7 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	N.A
20°C	3V DC	1.23 µA
70°C	3V DC	N.A

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider also the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-QA3/QA3E.*

2.7 Environmental Specifications

Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to +85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.

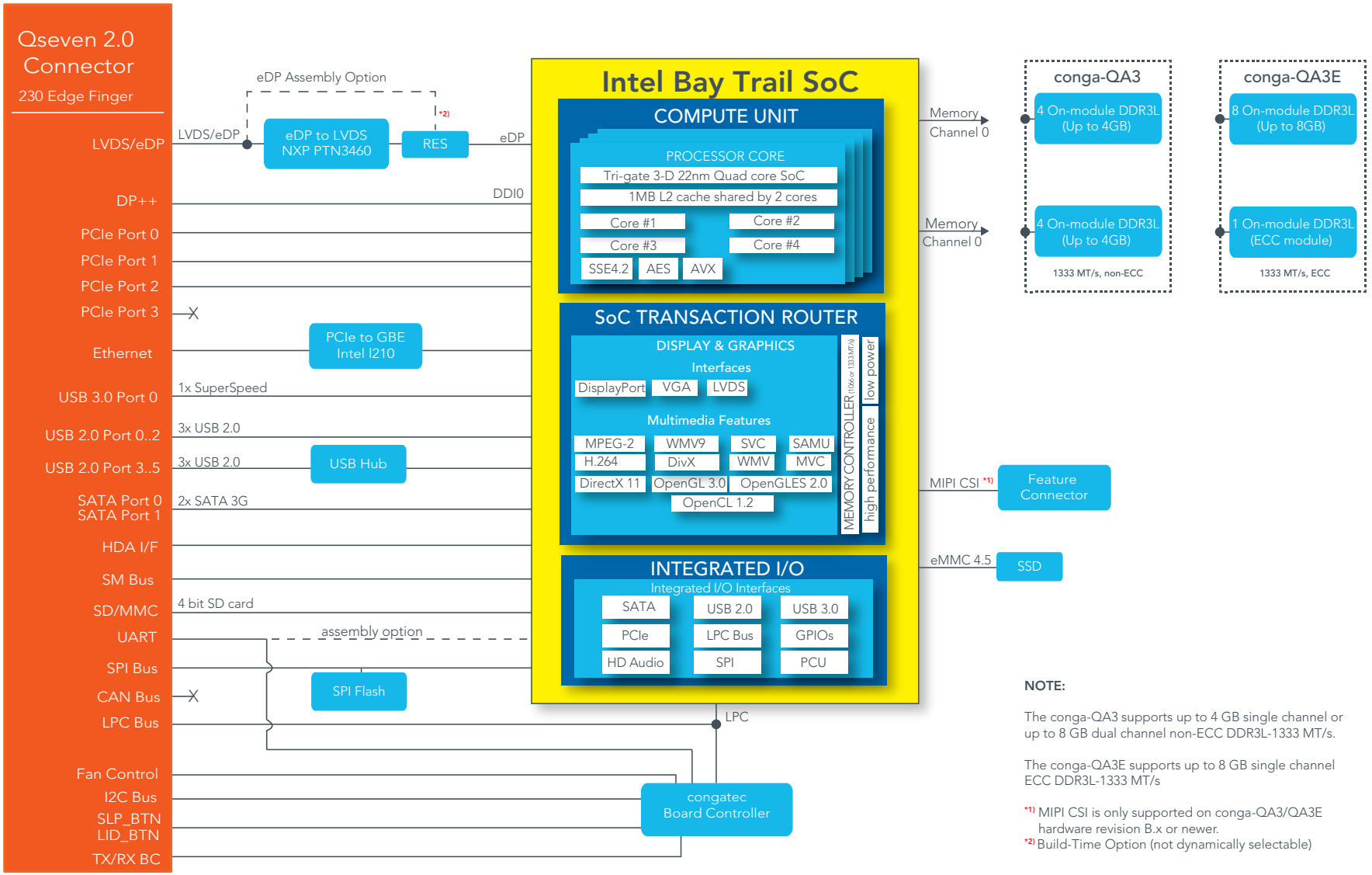
Humidity specifications are for non-condensing conditions.

Note

For long term storage of the conga-QA3/QA3E (more than six months), keep the conga-QA3/QA3E in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

We do not recommend storing the conga-QA3/QA3E for more than five years under these conditions.

3 Block Diagram



NOTE:

The conga-QA3 supports up to 4 GB single channel or up to 8 GB dual channel non-ECC DDR3L-1333 MT/s.

The conga-QA3E supports up to 8 GB single channel ECC DDR3L-1333 MT/s

*1) MIPI CSI is only supported on conga-QA3/QA3E hardware revision B.x or newer.
*2) Build-Time Option (not dynamically selectable)

4 Cooling Solutions

congatec GmbH offers the cooling solutions listed in Table 8 for conga-QA3/QA3E. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 8 Cooling Solution Variants

	Cooling Solution	Part No	Description
1	HSP	015191	Heatspreader with 2.7 mm bore-hole standoff.
		015190	Heatspreader with M2.5 mm threaded standoff.
2	CSP	015193	Passive cooling with 2.7 mm bore-hole standoffs.
		015192	Passive cooling with M2.5 mm threaded standoffs.

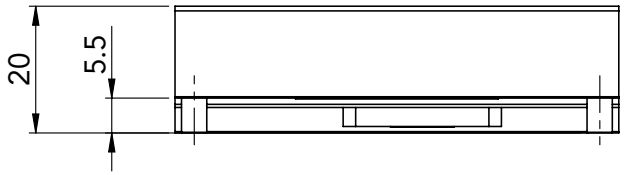
Note

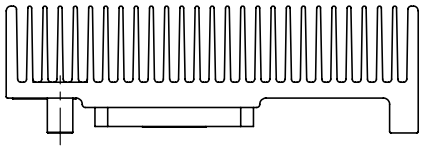
1. *We recommend a maximum torque of 0.4 Nm for the mounting screws and to start with the two screws furthest from the CPU die.*
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*
3. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

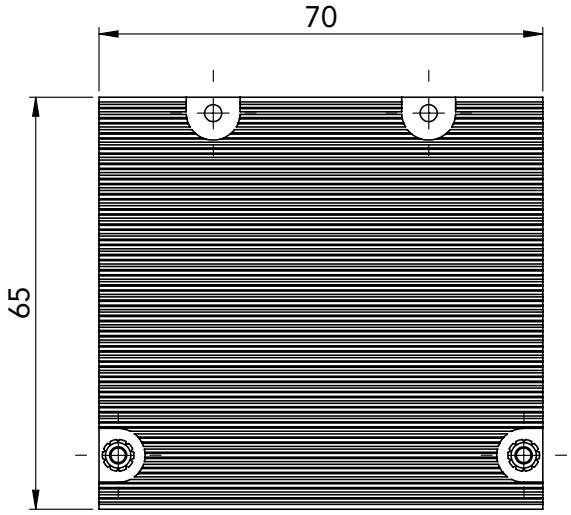
Caution

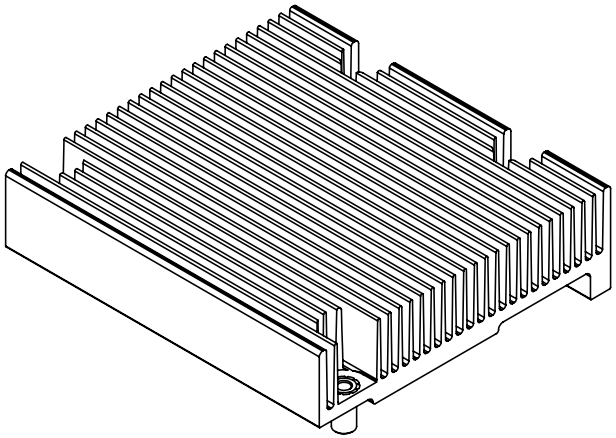
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

4.1 CSP Dimensions

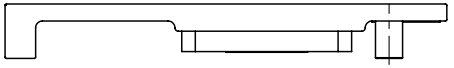


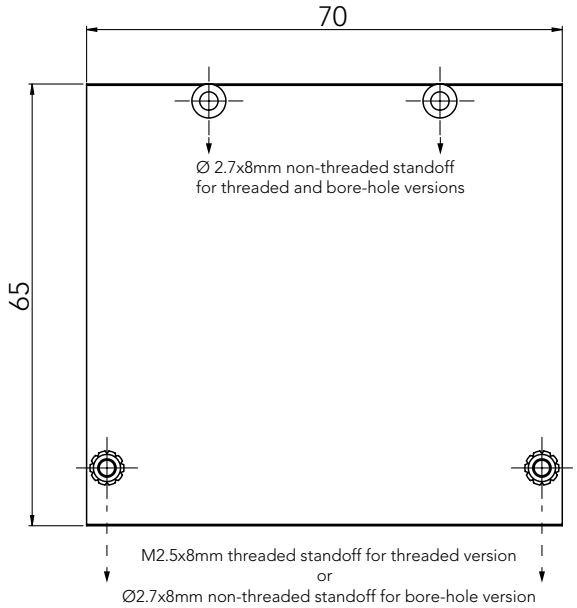


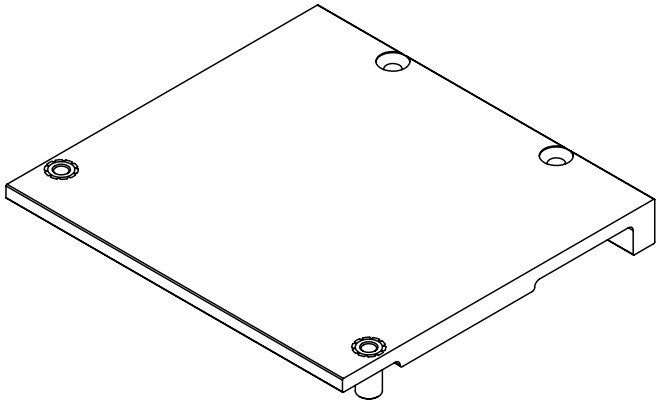




4.2 HSP Dimensions

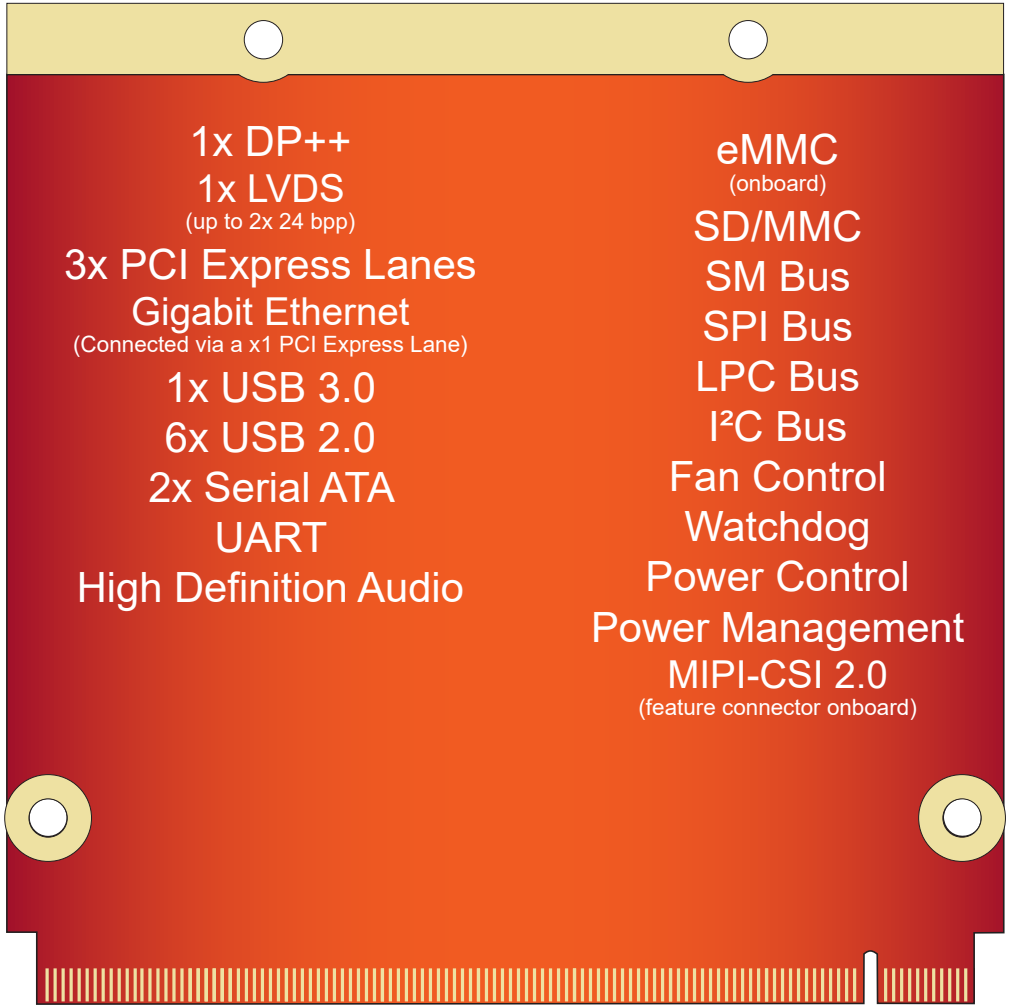






5 Connector Subsystems

The conga-QA3/QA3E is based on the Qseven® standard. It therefore has 115 edge fingers on the top and bottom side of the module that mate with the 230-pin card-edge MXM connector located on the carrier board. This connector is able to interface the available signals of the conga-QA3/QA3E with the carrier board peripherals.



5.1 PCI Express™

The conga-QA3/QA3E offers 3 PCI Express externally on the Edge finger. The lanes are Gen 2 compliant and offer support for full 5 Gb/s bandwidth in each direction per x1 link. Default configuration for the lanes is 3 x1 link. A 1 x2 + 1 x1 link configuration is also possible but requires a special/customized BIOS firmware. Contact congatec technical support for more information about this subject.

The PCI Express interface is based on the PCI Express Specification 2.0 with Gen 1 (2.5Gb/s) and Gen 2 (5 Gb/s) speed. For more information refer to the PCI Express pinout table in section 8 "Signal Descriptions and Pinout Tables.".

5.2 ExpressCard™

The conga-QA3/QA3E does not support ExpressCard.

5.3 Gigabit Ethernet

The conga-QA3/QA3E offers a Gigabit Ethernet interface on the edge finger via the onboard Intel® I210 Gigabit Ethernet controller. This controller is connected to the Intel® Bay Trail SoC through the fourth PCI Express lane. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

5.4 Serial ATA™ (SATA)

The conga-QA3/QA3E offers 2 SATA interfaces on the edge finger via a SATA host controller integrated in the Intel® Bay Trail SoC. The SATA host controller supports indepedent DMA operation and data transfer rates of 1.5 Gb/s and 3.0 Gb/s. It also supports two modes of operation - a legacy mode and AHCI mode. Software that uses legacy mode will not have AHCI capabilities. For more information, refer to section 10 "BIOS Setup Description".

5.5 USB 2.0

The conga-QA3/QA3E offers 6 USB 2.0 interfaces on the Edge finger. These interfaces are provided by routing three of the four ports provided by the Bay Trail SoC directly to the edge finger. The fourth port provided by the SoC is routed to the edge finger via a USB hub, thereby providing additional three ports. The EHCI host controller in the SoC supports these interfaces with high-speed, full-speed and low-speed USB signalling. The controller complies with USB standard 1.1 and 2.0.

Note

The USB overcurrent protection is disabled by default on USB ports 0 and 1 (native ports). To enable this function, you require a customized BIOS. Contact congatec technical support department for more information.

5.6 USB 3.0

The conga-QA3/QA3E offers one USB 3.0 interface on the Edge finger. This interface is controlled by an xHCI host controller in the SoC. The host controller allows data transfers of up to 5 Gb/s and supports SuperSpeed, high-speed, full-speed and low-speed USB signalling. The USB SuperSpeed signals should be paired with USB 2.0 port 0 on the carrier board. See section 7.3 for more information about xHCI and EHCI port mapping.

5.7 SD Card

The conga-QA3/QA3E offers a 4-bit SD interface for SD/MMC cards on the Edge finger. The SD card controller in the Storage Control Cluster of the SoC supports the SD interface with up to 832 Mb/s data rate using 4 parallel data lines.

Note

The conga-QA3/QA3E celeron variants do not offer SD card Interface.

5.8 UART

The conga-QA3/QA3E offers a UART interface on the edge connector. The UART signals are routed from the congatec Board Controller by default. The signals do not support hardware handshaking and flow control. For more information, see Table 14.

Optionally, the signals can be routed from the SoC instead (assembly option).

Note

The onboard UART cannot be used in combination with an external, Super IO based UART. They are mutually exclusive.

5.9 High Definition Audio (HDA)

The conga-QA3/QA3E provides an interface that supports the connection of HDA audio codecs.

5.10 Digital Display Interface

The Bay Trail SoC provides two DDI ports to enable eDP 1.3 or DP 1.1a. One of the ports (DDI0) is routed directly to the edge finger for the support of eDP/DP++. The other port (DDI1) is routed to the edge finger via an eDP to LVDS bridge. This port supports only LVDS by default. An optional eDP support on this port is possible but only as an assembly option

The conga-QA3/QA3E supports up to two independent displays. The display combination must be 1 DDI and 1 LVDS as shown below:

Table 9 Display Combination

Display 1 (DDI 0)	Display 2 (DDI 1)	Display 1 Max. Resolution	Display 2 Max. Resolution
DP	LVDS	2560x1600 @60Hz	1920x1200 @60Hz (dual LVDS mode)

5.10.1 LVDS/eDP

The conga-QA3/QA3E offers a single/dual channel LVDS/eDP interface on the edge finger. The interface is provided by routing the onboard PTN3460 eDP to LVDS bridge to the DDI port 1 of the Bay Trail SoC. The bridge processes incoming DisplayPort stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format.

The LVDS/eDP interface supports single and dual channel signalling with color depths of 18 bits or 24 bits per pixel and pixel clock frequency up to 112 MHz. It also supports automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3, with resolution up to 1920x1200 in dual LVDS bus mode. The interface is designed to provide only LVDS signals. However, an assembly option exists for the support of eDP signals. For more information, contact congatec technical support.

5.10.2 DP++ Port

DisplayPort is an open, industry standard digital display interface, that has been developed within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

The DP++ interface is provided by DDI0 of the Bay Trail SoC. The supported resolution is up to 2560x1600@60Hz.

5.11 LPC

The conga-QA3/QA3E offers the LPC (Low Pin Count) bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals and functionality. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific carrier board using this bus. Only certain devices such as Super I/O or TPM 1.2 chips can be implemented on the carrier board.

Note

The conga-QA3/QA3E Atom variants operate at a frequency of 33 MHz while the Celeron variants at 25 MHz.

5.12 SPI

The conga-QA3/QA3E offers the SPI interface only for booting a BIOS from an SPI Flash device placed on the carrier board.

5.13 I²C Bus

The conga-QA3/QA3E supports I2C bus. Thanks to the I2C host controller in the cBC, the I²C bus is multi-master capable and runs at fast mode.

5.14 CAN Bus

The conga-QA3/QA3E does not support CAN bus.

5.15 Power Control

The conga-QA3/QA3E supports ATX-style power supplies control. In order to do this the power supply must provide a constant source of VCC_5V_SB power. The AT-style power supply (5V only) is also supported. In this case, the conga-QA3's pin PWRBTN# should be left unconnected, pin SUS_S3# should control the main power regulators on the carrier board (+3.3V...) and pins VCC_5V_SB should be connected to the 5V input power rail according to the Qseven specification.

PWGIN

PWGIN (pin 26) can be connected to an external power good circuit. This input is optional and should be left unconnected when not used. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies, the conga-QA3/QA3E module is capable of generating its own power-on good.

SUS_S3#

The SUS_S3# (pin 18) signal is an active-low output that can be used to control the main 5V rail of the power supply for module and all other main power supplies on carrier board. In order to accomplish this, the signal must be inverted with an inverter/transistor that is supplied by standby voltage (ATX-style) or system input voltage (AT-style) and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 20) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3.3V_SB using a 10k resistor.

When PWRBTN# is asserted, it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Note

To initiate an ACPI event, the Bay Trail SoC expects a rising edge on the PWRBTN# signal.

Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-QA3/QA3E. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-QA3/QA3E application:

- It has also been noticed that on some occasions, problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush current on the conga-QA3/QA3E VCC_5V_SB power rail can go up as high as 6.5A and as high as 12.5A on the conga-QA3/QA3E VCC power rail within a short time (approx 100µs) and with a voltage rise time of 100µs.

Sufficient decoupling capacitance must be implemented to ensure proper power-up sequencing.

Note

For more information about power control event signals refer to the Qseven® specification.

5.16 Power Management

ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3). No support for legacy APM.

6 Additional Features

6.1 Onboard Interfaces

6.1.1 MIPI-CSI 2.0

The conga-QA3/QA3E revision B.x and later offer an onboard camera interface via the feature connector. The interface supports up to two independent cameras - four data lanes for the first camera and one data lane for the second camera. Each lane operates at up to 1 GT/s depending on the camera resolution. It also supports up to 24 MP image capture @ 15fps, full HD 1080p60.

The MIPI-CSI-2 interfaces follow the CSI-2 specification as defined by the MIPI Alliance and support YUV420, YUV422, RGB444, RGB555, RGB565, RGB888, JPEG and RAW 8/10/12/14. The MIPI interface is also compliant with the SGET Camera Feature Specification.

For the signal descriptions, see Table 33.

Note

The conga-QA3/QA3E celeron variants do not support MIPI-CSI 2.0.

6.1.2 eMMC 4.5

The conga-QA3/QA3E offers an optional eMMC 4.5 flash onboard the Intel Atom variants, with up to 32 GB capacity. The conga-QA3/QA3E celeron variants do not offer eMMC. Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology. The performance of the newer eMMC may vary depending on the eMMC technology.

Note

For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions.

6.2 congatec Board Controller (cBC)

The conga-QA3/QA3E is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRBI microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

6.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.2.2 Fan Control

The conga-QA3/QA3E has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

6.2.3 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are "Always On", "Remain Off" and "Last State".

6.2.4 Watchdog

The conga-QA3/QA3E is equipped with a multi stage watchdog solution that can be triggered by software of external hardware. For more information about the watchdog feature, see the BIOS setup description in section 10.4.1 of this document and the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

6.3 Embedded BIOS

The conga-QA3/QA3E is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. These are the most important embedded PC features:

6.3.1 CMOS Backup in Non Volatile Memory

A copy of the CMOS memory (SRAM) is stored in the BIOS flash device. This prevents the system from booting up with incorrect system configuration if the backup battery (RTC battery) fails. Additionally, it provides the ability to create systems that do not require a CMOS backup battery.

6.3.2 OEM CMOS Default Settings and OEM BIOS Logo

This feature allows system designers to create and store their own CMOS default configuration and BIOS logo (splash screen) within the BIOS flash device. Customized BIOS development by congatec for these changes is no longer necessary because customers can easily do these changes by themselves using the congatec system utility CGUTIL.

6.3.3 OEM BIOS Code

With the congatec embedded BIOS it is even possible for system designers to add their own code to the BIOS POST process. Except for custom specific code, this feature can also be used to support Window 7 SLIC table, verb tables for HDA codecs, rare graphic modes and Super I/O controllers.

For more information about customizing the congatec embedded BIOS, refer to the congatec system utility user's guide (CGUTLm1x.pdf) and can be found on the congatec GmbH website at www.congatec.com or contact congatec technical support.

6.3.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a smart battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI-capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for additional modifications to the system BIOS.

The conga-QA3/QA3E BIOS fully supports this interface. For more information about this subject, visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

6.3.5 API Support (CGOS/EAPI)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux and QNX. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

Other COM (Computer on Modules) vendors offer similar driver solutions for these kind of embedded PC features, which are by nature proprietary. All the API solutions that can be found on the market are not compatible to each other. As a result, writing application software that can run on more than one vendor's COM is not so easy. Customers have to change their application software when switching to another COM vendor.

EAPI (Embedded Application Programming Interface) is a programming interface defined by the PICMG that addresses this problem. With this unified API it is now possible to run the same application on all vendor's COMs that offer EAPI driver support. Contact congatec technical support for more information about EAPI.

6.4 Suspend to RAM

The conga-QA3/QA3E supports Suspend to RAM.

6.5 ECC Memory Support

Error-Correcting Code (ECC) memory is a memory system that tests for and corrects errors automatically, very often without the operating system being aware of it, let alone the user. As data are written into memory, ECC circuitry generates checksums from the binary sequences in the bytes and stores them in an additional seven bits of memory for 32-bit data paths or eight bits for 64-bit paths. When data are retrieved from memory, the checksum is recomputed to determine if any of the data bits have been corrupted.

Note

The conga-QA3 does not support ECC memory. Only the conga-QA3E supports ECC memory. The ECC memory can detect and correct single bit errors. It can detect but not correct double bit errors.

7 conga Tech Notes

The conga-QA3/QA3E has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the system resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

7.1 Intel Bay Trail SoC Features

7.1.1 Processor Core

The Intel Bay Trail Soc features Single, Dual or Quad Out-of-Order Execution processor cores. The cores are sub-divided into dual-core modules with each module sharing a 1 MB L2 cache (512 KB per core). Some of the features supported by the core are:

- Intel 64 architecture
- Intel Streaming SIMD Extensions 4.1 and 4.2
- Support for Intel VT-x
- Thermal management support vial Intel Thermal Monitor
- Uses Power Aware Interrupt Routing
- Uses 22 nm process technology

Note

Intel Hyper-Threading technology is not supported (four cores execute four threads)

7.1.1.1 Intel Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel® VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

7.1.1.2 AHCI

The Intel Bay Trail SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

7.1.1.3 IDE Mode (Native Vs. Legacy)

Legacy Mode

When operating in legacy mode, the SATA controllers need two legacy IRQs (14 and 15) and are unable to share these IRQs with other devices. This is because the SATA controllers emulate the primary and secondary legacy IDE controllers.

Native Mode

Native mode allows the SATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources. This means they can be configured anywhere within the system. When either SATA controller 1 or 2 runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system. Setting "IDE Mode" in the BIOS setup program will automatically enable Native mode. See section 10.4.12 for more information about this. Running in native mode frees up interrupt resources (IRQs 14 and 15) and decreases the chance that there may be a shortage of interrupts when installing devices.

Note

If your operating system supports native mode then congatec GmbH recommends you enable it.

7.1.1.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-QA3/QA3E ACPI thermal solution currently offers two different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.2 ACPI Suspend Modes and Resume Events

conga-QA3/QA3E supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 10.4.6 "ACPI Configuration Submenu".

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

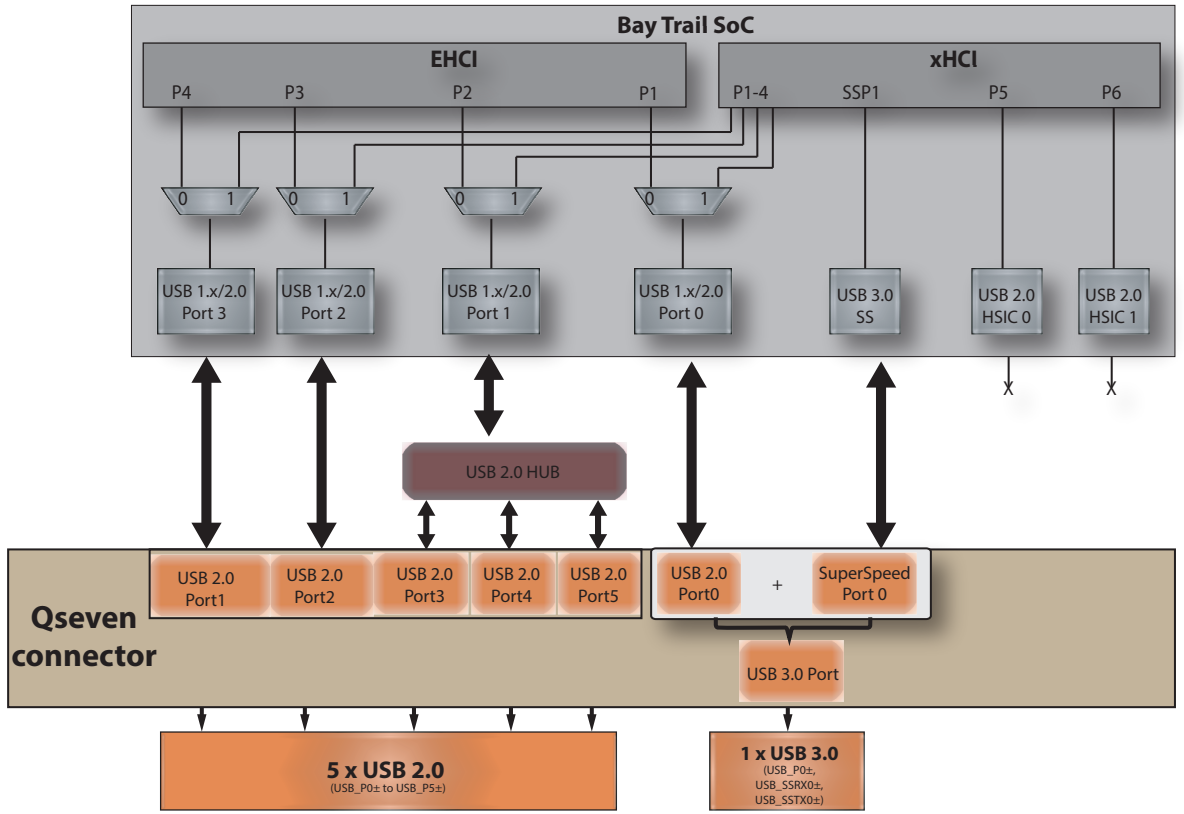
- Windows 7, Windows Vista, Windows XP and Linux

This table lists the "Wake Events" that resume the system from S3 unless otherwise stated in the "Conditions/Remarks" column:

Table 10 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

7.3 xHCI and EHCI Port Mapping



NOTE:
Possible USB configurations are:

(*) Up to 6x USB 2.0
(*) Up to 5x USB 2.0 and 1x USB 3.0

Note

The USB overcurrent protection is disabled by default on USB ports 0 and 1 (native ports). To enable this function, you require a customized BIOS. Contact congatec technical support department for more information.

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on Qseven® module's edge fingers.

The table below describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

Not all the signals described in this section are available on all conga-QA3/QA3E variants. Use the article number of the module and refer to the options table in section 1 to determine the options available on the module.

Table 11 Signal Tables Terminology Descriptions

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PP	Push Pull
I/O	Bi-directional Input/Output Pin
P	Power Input
NA	Not applicable
NC	Not Connected
PCIE	PCI Express differential pair signals. In compliance with the PCI Express Base Specification 2.0
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet Specification.
USB	Universal Serial Bus differential pair signals. In compliance with the Universal Serial Bus Specification 2.0
SATA	Serial Advanced Technology Attachment differential pair signals. In compliance with the Serial ATA High Speed Serialized AT Attachment Specification 2.6.
SPI	Serial Peripheral Interface bus is a synchronous serial data link that operates in full duplex mode.
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

Table 12 Edge Finger Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Power Ground	2	GND	Power Ground
3	GBE_MDI3-	Gigabit Ethernet MDI3-	4	GBE_MDI2-	Gigabit Ethernet MDI2-
5	GBE_MDI3+	Gigabit Ethernet MDI3+	6	GBE_MDI2+	Gigabit Ethernet MDI2+
7	GBE_LINK100#	100 Mbps link speed	8	GBE_LINK1000#	1000 Mbps link speed
9	GBE_MDI1-	Gigabit Ethernet MDI1-	10	GBE_MDI0-	Gigabit Ethernet MDI0-
11	GBE_MDI1+	Gigabit Ethernet MDI1+	12	GBE_MDI0+	Gigabit Ethernet MDI0+
13	GBE_LINK#	Gigabit Ethernet Link indicator	14	GBE_ACT#	Gigabit Ethernet Activity indicator
15	GBE_CTREF	Reference voltage for GBE	16	SUS_S5#	S5 (Soft OFF) – shutdown state
17	WAKE#	External system wake event	18	SUS_S3#	S3 (Suspend to RAM) – SLP
19	SUS_STAT#	Suspend status	20	PWRBTN#	Power button
21	SLP_BTN#	Sleep button	22	LID_BTN#	LID button
23	GND	Power Ground	24	GND	Power Ground
25	GND	Power Ground	26	PWGIN	Power good input
27	BATLOW#	Battery low input	28	RSTBTN#	Reset button input
29	SATA0_TX+	Serial ATA Channel 0 TX+	30	SATA1_TX+	Serial ATA Channel 1 TX+
31	SATA0_TX-	Serial ATA Channel 0 TX-	32	SATA1_TX-	Serial ATA Channel 1 TX-
33	SATA_ACT#	Serial ATA Activity	34	GND	Power Ground
35	SATA0_RX+	Serial ATA Channel 0 RX+	36	SATA1_RX+	Serial ATA Channel 1 RX+
37	SATA0_RX-	Serial ATA Channel 0 RX-	38	SATA1_RX-	Serial ATA Channel 1 RX-
39	GND	Power Ground	40	GND	Power Ground
41	BIOS_DISABLE# /BOOT_ALT#	BIOS Module disable Boot Alternative Enable	42	SDIO_CLK	SDIO Clock Output
43	SDIO_CD#	SDIO Card Detect	44	SDIO_LED	SDIO LED
45	SDIO_CMD	SDIO Command/Response	46	SDIO_WP	SDIO Write Protect
47	SDIO_PWR#	SDIO Power Enable	48	SDIO_DAT1	SDIO Data Line 1
49	SDIO_DAT0	SDIO Data Line 0	50	SDIO_DAT3	SDIO Data Line 3
51	SDIO_DAT2	SDIO Data Line 2	52	SDIO_DAT5 (*)	SDIO Data Line 5
53	SDIO_DAT4 (*)	SDIO Data Line 4	54	SDIO_DAT7 (*)	SDIO Data Line 7
55	SDIO_DAT6 (*)	SDIO Data Line 6	56	USB_DRIVE_VBUS (*)	USB power enable pin for USB Port 1
57	GND	Power Ground	58	GND	Power Ground
59	HDA_SYNC (**) / I2S_WS	HD Audio/AC'97 Synchronization. Multiplexed with I2S Word Select from Codec	60	SMB_CLK / GP1_I2C_CLK	SMBus Clock line. Multiplexed with General Purpose I²C bus #1 clock line
61	HDA_RST# / I2S_RST#	HD Audio/AC'97 Codec Reset. Multiplexed with I2S Codec Reset	62	SMB_DAT / GP1_I2C_DAT	SMBus Data line. Multiplexed with General Purpose I²C bus #1 data line.
63	HDA_BITCLK (**) / I2S_CLK	HD Audio/AC'97 Serial Bit Clock. Multiplexed with I2S Serial Data Clock from Codec.	64	SMB_ALERT#	SMBus Alert input
65	HDA_SDI (**) / I2S_SDI	HD Audio/AC'97 Serial Data In. Multiplexed with I2S Serial Data Input from Codec	66	GP0_I2C_CLK	General Purpose I2C Bus No 0 clock line

Pin	Signal	Description	Pin	Signal	Description
67	HDA_SDO (**) / I2S_SDO	HD Audio/AC'97 Serial Data Out. Multiplexed with I2S Serial Data Output from Codec	68	GP0_I2C_DAT	General Purpose I2C Bus No 0 data line
69	THRM#	Thermal Alarm active low	70	WDTRIG#	Watchdog trigger signal
71	THRMTRIP#	Thermal Trip indicates an overheating condition	72	WDOUT	Watchdog event indicator
73	GND	Power Ground	74	GND	Power Ground
75	USB_P7- / USB_SSTX0-	USB Port 7 Differential Pair- . Multiplexed with Superspeed USB transmit differential pair-	76	USB_P6- / USB_SSRX0-	USB Port 6 Differential Pair-. Multiplexed with Superspeed USB transmit differential pair-
77	USB_P7+ / USB_SSTX0+	USB Port 7 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+	78	USB_P6+ / USB_SSRX0+	USB Port 6 Differential Pair+. Multiplexed with Superspeed USB transmit differential pair+
79	USB_6_7_OC# (*)	Over current detect input 6/7 USB	80	USB_4_5_OC#	Over current detect input 4/5 USB
81	USB_P5- / USB_SSTX1-	USB Port 5 Differential Pair-	82	USB_P4- / USB_SSRX1-	USB Port 4 Differential Pair-
83	USB_P5+ / USB_SSTX1+	USB Port 5 Differential Pair+	84	USB_P4+ / USB_SSRX1+	USB Port 4 Differential Pair+
85	USB_2_3_OC#	Over current detect input 2/3 USB	86	USB_0_1_OC#	Over current detect input 0/1 USB
87	USB_P3-	USB Port 3 Differential Pair-	88	USB_P2-	USB Port 2 Differential Pair-
89	USB_P3+	USB Port 3 Differential Pair+	90	USB_P2+	USB Port 2 Differential Pair+
91	USB_VBUS (*)	USB VBUS pin	92	USB_ID (*)	USB ID pin
93	USB_P1-	USB Port 1 Differential Pair-	94	USB_P0-	USB Port 0 Differential Pair-
95	USB_P1+	USB Port 1 Differential Pair+	96	USB_P0+	USB Port 0 Differential Pair+
97	GND	Power Ground	98	GND	Power Ground
99	eDP0_TX0+ / LVDS_A0+	eDP Primary Channel 0+ LVDS Primary channel 0+	100	eDP1_TX0+ / LVDS_B0+	eDP Secondary channel 0+ LVDS Secondary channel 0+
101	eDP0_TX0- / LVDS_A0-	eDP Primary channel 0- LVDS Primary channel 0-	102	eDP1_TX0- / LVDS_B0-	eDP Secondary channel 0- LVDS Secondary channel 0-
103	eDP0_TX1+ / LVDS_A1+	eDP Primary channel 1+ LVDS Primary channel 1+	104	eDP1_TX1+ / LVDS_B1+	eDP Secondary channel 1+ LVDS Secondary channel 1+
105	eDP0_TX1- / LVDS_A1-	eDP Primary channel 1- LVDS Primary channel 1-	106	eDP1_TX1- / LVDS_B1-	eDP Secondary channel 1- LVDS Secondary channel 1-
107	eDP0_TX2+ / LVDS_A2+	eDP Primary channel 2+ LVDS Primary channel 2+	108	eDP1_TX2+ / LVDS_B2+	eDP Secondary channel 2+ LVDS Secondary channel 2+
109	eDP0_TX2- / LVDS_A2-	eDP Primary channel 2- LVDS Primary channel 2-	110	eDP1_TX2- / LVDS_B2-	eDP Secondary channel 2- LVDS Secondary channel 2-
111	LVDS_PPEN	LVDS Power enable	112	LVDS_BLEN	LVDS Backlight enable
113	eDP0_TX3+ / LVDS_A3+	eDP Primary channel 3+ LVDS Primary channel 3+	114	eDP1_TX3+ / LVDS_B3+	eDP Secondary channel 3+ LVDS Secondary channel 3+
115	eDP0_TX3- / LVDS_A3-	eDP Primary channel 3- LVDS Primary channel 3-	116	eDP1_TX3- / LVDS_B3-	eDP Secondary channel 3- LVDS Secondary channel 3-
117	GND	Power Ground	118	GND	Power Ground
119	eDP0_AUX+ / LVDS_A_CLK+	eDP Primary Auxilliary channel+ LVDS Primary channel CLK+	120	eDP1_AUX+ / LVDS_B_CLK+	eDP Secondary Auxiliary channel CLK+ LVDS Secondary channel CLK+

Pin	Signal	Description	Pin	Signal	Description
121	eDP0_AUX- / LVDS_A_CLK-	eDP Primary Auxilliary channel- LVDS Primary channel CLK-	122	eDP1_AUX- / LVDS_B_CLK-	eDP Secondary Auxiliary channel CLK- LVDS Secondary channel CLK-
123	LVDS_BLT_CTRL / GP_PWM_OUT0	PWM Backlight brightness General Purpose PWM Output	124	GP_1-Wire_Bus (*)	General Purpose 1-wire bus interface
125	LVDS_DID_DAT / GP_I2C_DAT	DDC Display ID Data line General Purpose I2C Data line	126	eDP0_HPD# / LVDS_BLC_DAT (*)	SSC clock chip data line. Can be used as eDP primary hotplug detect
127	LVDS_DID_CLK / GP_I2C_CLK	DDC Display ID Clock line General Purpose I2C Clock line	128	eDP1_HPD# / LVDS_BLC_CLK (*)	SSC clock chip clock line. Can be used as eDP secondary hotplug detect
129	CAN0_TX (*)	CAN TX Output for CAN Bus Channel 0	130	CAN0_RX (*)	CAN RX Input for CAN Bus Channel 0
131	DP_LANE3+ / TMDS_CLK+	DisplayPort differential pair line lane 3. Multiplexed with TMDS differential pair clock+	132	RSVD (Differential)	Reserved
133	DP_LANE3- / TMDS_CLK-	DisplayPort differential pair line lane 3. Multiplexed with TMDS differential pair clock-	134	RSVD (Differential)	Reserved
135	GND	Power Ground	136	GND	Power Ground
137	DP_LANE1+ / TMDS_LANE1+	DisplayPort differential pair line lane 1 Multiplexed with TMDS differential pair lane1	138	DP_AUX+	DisplayPort auxiliary channel
139	DP_LANE1- / TMDS_LANE1-	DisplayPort differential pair line lane 1 Multiplexed with TMDS differential pair lane1	140	DP_AUX-	DisplayPort auxiliary channel
141	GND	Power Ground	142	GND	Power Ground
143	DP_LANE2+ / TMDS_LANE0+	DisplayPort differential pair line lane 2	144	RSVD (Differential Pair)	Reserved
145	DP_LANE2- / TMDS_LANE0-	DisplayPort differential pair line lane 2	146	RSVD (Differential Pair)	Reserved
147	GND	Power Ground	148	GND	Power Ground
149	DP_LANE0+ / TMDS_LANE2+	DisplayPort differential pair line lane 0 Multiplexed with TMDS differential pair lane2	150	HDMI_CTRL_DAT	DDC based control signal (data) for TMDS device.
151	DP_LANE0- / TMDS_LANE2-	DisplayPort differential pair line lane 0 Multiplexed with TMDS differential pair lane2	152	HDMI_CTRL_CLK	DDC based control signal (clock) for TMDS device.
153	DP_HDMI_HPD#	Hot plug detection for TMDS	154	DP_HPD#	Hot plug detection for DP
155	PCIE_CLK_REF+	PCI Express Reference Clock+	156	PCIE_WAKE# (**)	PCI Express Wake event
157	PCIE_CLK_REF-	PCI Express Reference Clock-	158	PCIE_RST#	Reset Signal for external devices
159	GND	Power Ground	160	GND	Power Ground
161	PCIE3_TX+ (*)	PCI Express Channel 3 Output+	162	PCIE3_RX+ (*)	PCI Express Channel 3 Input+
163	PCIE3_TX- (*)	PCI Express Channel 3 Output-	164	PCIE3_RX- (*)	PCI Express Channel 3 Input-
165	GND	Power Ground	166	GND	Power Ground
167	PCIE2_TX+	PCI Express Channel 2 Output+	168	PCIE2_RX+	PCI Express Channel 2 Input+
169	PCIE2_TX-	PCI Express Channel 2 Output-	170	PCIE2_RX-	PCI Express Channel 2 Input-
171	UART0_TX (**)	Serial Data Transmitter	172	UART0_RTS# (**)	Handshake signal, ready to receive data
173	PCIE1_TX+	PCI Express Channel 1 Output+	174	PCIE1_RX+	PCI Express Channel 1 Input+
175	PCIE1_TX-	PCI Express Channel 1 Output-	176	PCIE1_RX-	PCI Express Channel 1 Input-
177	UART0_RX (**)	Serial Data Receiver	178	UART0_CTS# (**)	Handshake signal, ready to send data
179	PCIE0_TX+	PCI Express Channel 0 Output+	180	PCIE0_RX+	PCI Express Channel 0 Input+
181	PCIE0_TX-	PCI Express Channel 0 Output-	182	PCIE0_RX-	PCI Express Channel 0 Input-

Pin	Signal	Description	Pin	Signal	Description
183	GND	Power Ground	184	GND	Power Ground
185	LPC_AD0	LPC Interface Address Data 0	186	LPC_AD1	LPC Interface Address Data 1
187	LPC_AD2	LPC Interface Address Data 2	188	LPC_AD3	LPC Interface Address Data 3
189	LPC_CLK	LPC Interface Clock	190	LPC_FRAME#	LPC frame indicator
191	SERIRQ (**)	Serialized interrupt	192	LPC_LDRQ# (*)	LPC DMA request
193	VCC_RTC	3V backup cell input	194	SPKR /GP_PWM_OUT2	Output for audio enunciator General Purpose PWM Output
195	FAN_TACHOIN	Fan tachometer input General Purpose Timer In	196	FAN_PWMOUT	Fan speed control (PWM) General Purpose PWM Output
197	GND	Power Ground	198	GND	Power Ground
199	SPI_MOSI (**)	SPI Master serial output/Slave serial input	200	SPI_CS0# (**)	SPI Chip Select 0 Output
201	SPI_MISO (**)	SPI Master serial input/Slave serial output signal	202	SPI_CS1# (*)	SPI Chip Select 1 Output
203	SPI_SCK (**)	SPI Clock Output	204	MFG_NC4	Do not connect on carrier board
205	VCC_5V_SB	+5VDC,Standby ±5%	206	VCC_5V_SB	+5VDC Standby ±5%
207	MFG_NC0	Do not connect on carrier board	208	MFG_NC2	Do not connect on carrier board
209	MFG_NC1	Do not connect on carrier board	210	MFG_NC3	Do not connect on carrier board
211	VCC	Power supply +5VDC ±5%	212	VCC	Power supply +5VDC ±5%
213	VCC	Power supply +5VDC ±5%	214	VCC	Power supply +5VDC ±5%
215	VCC	Power supply +5VDC ±5%	216	VCC	Power supply +5VDC ±5%
217	VCC	Power supply +5VDC ±5%	218	VCC	Power supply +5VDC ±5%
219	VCC	Power supply +5VDC ±5%	220	VCC	Power supply +5VDC ±5%
221	VCC	Power supply +5VDC ±5%	222	VCC	Power supply +5VDC ±5%
223	VCC	Power supply +5VDC ±5%	224	VCC	Power supply +5VDC ±5%
225	VCC	Power supply +5VDC ±5%	226	VCC	Power supply +5VDC ±5%
227	VCC	Power supply +5VDC ±5%	228	VCC	Power supply +5VDC ±5%
229	VCC	Power supply +5VDC ±5%	230	VCC	Power supply +5VDC ±5%

Note

The signals marked with asterisk symbol (*) are not supported on the conga-QA3/QA3E.

On Intel Bay Trail SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

Table 13 PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0.
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	I PCIE		Not connected
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Not connected
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock for Lanes 0 to 3.	O PCIE		
PCIE_WAKE# (**)	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I 3.3VSB	PU 100k 3.3VSB	
PCIE_RST#	158	Reset Signal for external devices.	O 3.3V		

Note

On Intel Bay Trail SoC, the signal marked with asterisks (**) has a voltage level that is different from the level defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

Table 14 UART Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
UART0_TX (**)	171	Serial Data Transmitter	O 3.3V		
UART0_RX (**)	177	Serial Data Reciever	I 3.3VSB	PU 20k 3.3VSB	
UART0_CTS# (**)	178	Handshake signal, ready to send data	I 3.3VSB	PU 20k 3.3VSB	Not available by default (requires a customized variant)
UART0_RTS# (**)	172	Handshake signal, ready to receive data	O 3.3V		Not available by default (requires a customized variant)

Note

The UART signals are provided by the congatec Board Controller by default.

Optionally, the signals can be provided by the SoC instead (assembly option). The signals of the SoC have voltage levels that are different from the levels defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module. The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

Table 15 Ethernet Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GBE_MDI0+ GBE_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI1+ GBE_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI2+ GBE_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI3+ GBE_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_CTREF	15	Reference voltage for carrier board Ethernet magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		Not connected
GBE_LINK#	13	Ethernet controller 0 link indicator, active low.	O 3.3VSB PP		
GBE_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB PP		
GBE_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB PP		
GBE_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 3.3VSB PP		

Note

The conga-QA3/QA3E can drive GbE LEDs directly with up to 10mA.

Table 16 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	O 3.3V		up to 10mA

Table 17 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_P0+ USB_P0-	96 94	Universal Serial Bus Port 0 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Can be used to form a USB 3.0 Port together with USB_SSRX0, USB_SSTX0 signals.
USB_P1+ USB_P1-	95 93	Universal Serial Bus Port 1 differential pair. This port may be optionally used as USB client port.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P2+ USB_P2-	90 88	Universal Serial Bus Port 2 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P3+ USB_P3-	89 87	Universal Serial Bus Port 3 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P4+ USB_P4- USB_SSRX1+ USB_SSRX1-	84 82	Universal Serial Bus Port 4 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path.	I/O I		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P5+ USB_P5- USB_SSTX1+ USB_SSTX1-	83 81	Universal Serial Bus Port 5 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path	I/O O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P6+ USB_P6- USB_SSRX0+ USB_SSRX0-	78 76	Universal Serial Bus Port 6 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path	I PCIE		USB 2.0 compliant. Backwards compatible to USB 1.1 AC coupled off module **Note:** This port has only Superspeed signals on the Qseven connector.
USB_P7+ USB_P7- USB_SSTX0+ USB_SSTX0-	77 75	Universal Serial Bus Port 7 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path	O PCIE		USB 2.0 compliant. Backwards compatible to USB 1.1 AC coupled on module. **Note:** This port has only Superspeed signals on the Qseven connector.

USB_0_1_OC#	86	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	I 3.3VSB	PU 20k 3.3VSB	
USB_2_3_OC#	85	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	I 3.3VSB	PU 20k 3.3VSB	
USB_4_5_OC#	80	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	I 3.3VSB	PU 20k 3.3VSB	
USB_6_7_OC#	79	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	I 3.3VSB	PU 10k 3.3VSB	Not supported
USB_ID	92	USB ID pin. Configures the mode of the USB Port 1. Refer to the Qseven Design guide for further details.	O Analog		Not connected
USB_VBUS#	91	USB VBUS pin 5V tolerant VBUS resistance to be placed on the module VBUS capacitance to be placed on the carrier board	I 5V Passive Analog		Not connected
USB_DRIVE_ VBUS	56	USB power enable pin for USB Port 1. Enables the power for the USB-OTG port on the carrier	O 3.3V CMOS		Not connected

Note

The USB overcurrent protection is disabled by default on USB ports 0 and 1 (native ports). To enable this function, you require a customized BIOS. Contact congatec technical support department for more information.

Table 18 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	43	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I/O 3.3V	PU 10k 3.3V	
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	O 3.3V		
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O 3.3V OD/PP	PU 20k 3.3V	
SDIO_LED	44	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	O 3.3V		Bay Trail SD Card controller does not provide any SDIO_LED signal. SDIO_ LED signal is therefore generated by a logic gate. LED blinking might differ from blinking behavior of other modules
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I/O 3.3V	PU 10k 3.3V	

SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/ MMC card device.	O 3.3V	PU 10k 3.3V	
SDIO_DAT0 SDIO_DAT1 SDIO_DAT2 SDIO_DAT3 SDIO_DAT4 SDIO_DAT5 SDIO_DAT6 SDIO_DAT7	49 48 51 50 53 52 55 54	SDIO Data lines. These signals operate in push-pull mode.	I/O 3.3V OD/PP	PU 20k 3.3V	Only 4-bit SDIO interface. SDIO_DAT[7:4] are not connected

Note

The 20k pull-ups on the Data and CMD lines are internal Bay Trail pull-ups. The pull-ups are disabled once a high speed transfer is established.

Table 19 HDA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST# I2S_RST#	61	HD Audio Codec Reset. Multiplexed with I2S Codec Reset.	O 3.3V		
HDA_SYNC (**) I2S_WS	59	HD Audio Serial Bus Synchronization. Multiplexed with I2S Word Select from Codec.	O 3.3V		
HDA_BITCLK (**) I2S_CLK	63	HD Audio 24 MHz Serial Bit Clock from Codec. Multiplexed with I2S Serial Data Clock from Codec.	O 3.3V		
HDA_SDO (**) I2S_SDO	67	HD Audio Serial Data Output to Codec. Multiplexed with I2S Serial Data Output from Codec.	O 3.3V		
HDA_SDI (**) I2S_SDI	65	HD Audio Serial Data Input from Codec. Multiplexed with I2S Serial Data Input from Codec.	I 3.3V	PD 100k	

Note

On Intel Bay Trail SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

Table 20 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_PPEN	111	Controls panel power enable.	O 3.3V	PD 10k	
LVDS_BLEN	112	Controls panel Backlight enable.	O 3.3V	PD 10k	
LVDS_BLT_CTRL /GP_PWM_OUT0	123	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
LVDS_A0+ LVDS_A0- eDP0_TX0+ eDP0_TX0-	99 101	LVDS primary channel differential pair 0. Display Port primary channel differential pair 0.	O LVDS		
LVDS_A1+ LVDS_A1- eDP0_TX1+ eDP0_TX1-	103 105	LVDS primary channel differential pair 1. Display Port primary channel differential pair 1.	O LVDS		
LVDS_A2+ LVDS_A2- eDP0_TX2+ eDP0_TX2-	107 109	LVDS primary channel differential pair 2. Display Port primary channel differential pair 2.	O LVDS		
LVDS_A3+ LVDS_A3- eDP0_TX3+ eDP0_TX3-	113 115	LVDS primary channel differential pair 3. Display Port primary channel differential pair 3.	O LVDS		
LVDS_A_CLK+ LVDS_A_CLK- eDP0_AUX+ eDP0_AUX-	119 121	LVDS primary channel differential pair clock lines. Display Port primary auxiliary channel.	O LVDS		
LVDS_B0+ LVDS_B0- eDP1_TX0+ eDP1_TX0-	100 102	LVDS secondary channel differential pair 0. Display Port secondary channel differential pair 0.	O LVDS		
LVDS_B1+ LVDS_B1- eDP1_TX1+ eDP1_TX1-	104 106	LVDS secondary channel differential pair 1. Display Port secondary channel differential pair 1.	O LVDS		
LVDS_B2+ LVDS_B2- eDP1_TX2+ eDP1_TX2-	108 110	LVDS secondary channel differential pair 2. Display Port secondary channel differential pair 2.	O LVDS		
LVDS_B3+ LVDS_B3- eDP1_TX3+ eDP1_TX3-	114 116	LVDS secondary channel differential pair 3. Display Port secondary channel differential pair 3.	O LVDS		

LVDS_B_CLK+ LVDS_B_CLK- eDP1_AUX+ eDP1_AUX-	120 122	LVDS secondary channel differential pair clock lines. Display Port secondary auxiliary channel.	O LVDS		
LVDS_DID_CLK /GP2_I2C_CLK	127	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus clock line.	I/O 3.3V OD	PU 2.2k 3.3V	
LVDS_DID_DAT /GP2_I2C_DAT	125	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus data line.	I/O 3.3V OD	PU 2.2k 3.3V	
LVDS_BLC_CLK eDP1_HPD#	128	Control clock signal for external SSC clock chip. If the primary functionality is not used, it can be used as an emedded DisplayPort secondary Hotplug detection.	I/O 3.3V OD	PU 10k 3.3V	Not supported
LVDS_BLC_DAT eDP0_HPD#	126	Control data signal for external SSC clock chip. If the primary functionality is not used, it can be used as an emedded DisplayPort primary Hotplug detection.	I/O 3.3V OD	PU 10k 3.3V	Not supported

Table 21 DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP_LANE3+ DP_LANE3-	131 133	DisplayPort differential pair lines lane 3 (Shared with TMDS_CLK+ and TMDS_CLK-)	O PCIE		AC coupled on module.
DP_LANE2+ DP_LANE2-	143 145	DisplayPort differential pair lines lane 2 (Shared with TMDS_LANE0+ and TMDS_LANE0-)	O PCIE		AC coupled on module.
DP_LANE1+ DP_LANE1-	137 139	DisplayPort differential pair lines lane 1 (Shared with TMDS_LANE1+ and TMDS_LANE1-)	O PCIE		AC coupled on module.
DP_LANE0+ DP_LANE0-	149 151	DisplayPort differential pair lines lane 0 (Shared with TMDS_LANE2+ and TMDS_LANE2-)	O PCIE		AC coupled on module.
DP_AUX+ DP_AUX-	138 140	Auxiliary channel used for link management and device control. Differential pair lines.	I/O PCIE		
DP_HPD#	154	Hot plug detection signal that serves as an interrupt request.	I 3.3V	PU 4.99k 1.8V	Supports open drain and PushPull driver. Onboard PU is protected with a diode

Note

The DisplayPort interface signals are shared with TMDS signals.

Table 22 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	
TMDS_CLK+ TMDS_CLK-	131 133	TMDS differential pair clock lines. (Shared with DP_LANE3- and DP_LANE3+)	O TMDS		Passive level shifter shall use PD 620R.
TMDS_LANE0+ TMDS_LANE0-	143 145	TMDS differential pair lines lane 0. (Shared with DP_LANE2- and DP_LANE2+)	O TMDS		Passive level shifter shall use PD 620R.
TMDS_LANE1+ TMDS_LANE1-	137 139	TMDS differential pair lines lane 1. (Shared with DP_LANE1- and DP_LANE1+)	O TMDS		Passive level shifter shall use PD 620R.
TMDS_LANE2+ TMDS_LANE2-	149 151	TMDS differential pair lines lane 2. (Shared with DP_LANE0- and DP_LANE0+)	O TMDS		Passive level shifter shall use PD 620R.
HDMI_CTRL_CLK	152	DDC based control signal (clock) for TMDS device.	I/O 3.3V OD	PU 4k 3.3V	Level shifter FET and 2.2k PU to 5V shall be placed between module and TMDS connector.
HDMI_CTRL_DAT	150	DDC based control signal (data) for TMDS device.	I/O 3.3V OD	PU 4k 3.3V	Level shifter FET and 2.2k PU to 5V shall be placed between module and TMDS connector.
DP_HDMI_HPD#	153	Hot plug active low detection signal that serves as an interrupt request.	I 3.3V	PU 4.99k 1.8V	Supports open drain and PushPull Driver. Onboard PU is protected with a diode

Note

The conga-QA3/QA3E does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.

Table 23 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	185 186 187 188	Multiplexed Command, Address and Data (LPC_AD[0..3])	I/O 3.3V		
LPC_FRAME#	190	LPC frame indicates the start of a new cycle or the termination of a broken cycle.	I/O 3.3V		
LPC_LDRQ#	192	LPC DMA request.	I/O 3.3V	PU 10k	
LPC_CLK	189	LPC clock	I/O 3.3V		33 MHz on modules with Bay Trail-I SoC (Intel Atom E3800 series) 25 MHz on modules with Bay Trail-M/D SoC (Intel Celeron series)
SERIRQ (**)	191	Serialized Interrupt.	I/O 3.3V		

Note

On Intel Bay Trail SoC, the signal marked with asterisks (**) has a voltage level that is different from the level defined in the Qseven Specification.

To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

The conga-QA3/QA3E does not support GPIOs on the LPC interface.

Table 24 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_MOSI (**)	199	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	O 3.3VSB		
SPI_MISO (**)	201	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	I 3.3VSB		
SPI_SCK (**)	203	SPI clock output.	O 3.3VSB		
SPI_CS0# (**)	200	SPI chip select 0 output.	O 3.3VSB		
SPI_CS1#	202	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	O 3.3VSB		Not connected

Note

The SPI interface is for external BIOS only.

On Intel Bay Trail SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the Qseven Specification. To comply with the Qseven Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

Table 25 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	129	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	O 3.3V		Not connected
CAN0_RX	130	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	I 3.3V		Not connected

Table 26 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	211-230	Power Supply +5VDC ±5%.	P		
VCC_5V_SB	205-206	Standby Power Supply +5VDC ±5%.	P		
VCC_RTC	193	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.5 - 3.3 V).	P		
GND	1, 2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198	Power Ground.	P		

Table 27 Power Control Signal Descriptions

Signal	Pin #	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	26	High active input for the Qseven® module indicates that power from the power supply is ready.	I 5V	PU 1M 5V	
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	

Table 28 Power Management Signal Descriptions

Signal	Pin #	Description of Power Management signals	I/O	PU/PD	Comment
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB OD	PU 10k 3.3VSB	
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	I 3.3VSB	PU 10k 3.3VSB	
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	I 3.3VSB	PU 10k 3.3VSB	
SUS_STAT#	19	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3VSB		
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	O 3.3VSB		
SUS_S5#	16	S5 State: This signal indicates S4 or S5 (Soft Off) state.	O 3.3VSB		
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	

Table 29 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	I 3.3V	PU 10k 3.3V	
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	O 3.3V		
GP0_I2C_CLK	66	Clock line of I²C bus.	I/O 3.3V OD	PU 2.2k 3.3V	
GP0_I2C_DAT	68	Data line of I²C bus.	I/O 3.3V OD	PU 2.2k 3.3V	
GP1_SMB_CLK	60	Clock line of System Management Bus.	I/O 3.3VSB OD	PU 10k 3.3VSB	
GP1_SMB_DAT	62	Data line of System Management Bus.	I/O 3.3VSB OD	PU 10k 3.3VSB	
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	I/O 3.3VSB OD	PU 10k 3.3V	
SPKR /GP_PWM_OUT2	194	Primary functionality is output for audio enunciator, the “speaker” in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
BIOS_DISABLE# /BOOT_ALT#	41	Module BIOS disable input signal. Pull low to disable module’s onboard BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a bootloader.	I 3.3VSB	PU 10k 3.3VSB	
RSVD	132,134,144, 146	Do not connect	NC		
GP_1-Wire_Bus	124	General Purpose 1-Wire bus interface.	I/O 3.3V		Not connected

Table 30 Manufacturing Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
MFG_NC0	207	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC1	209	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC2	208	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC3	210	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC4	204	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes.	NA	NA	

Note

The carrier board must not drive the MFG_NC-pins or have pull-up or pull-down resistors implemented for these signals.

Table 31 Thermal Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I 3.3V	PU 6.7k 3.3V	
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off).	O 3.3V		

Table 32 Fan Control Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT	196	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. .	O 3.3V		
FAN_TACHOIN	195	Primary functionality is fan tachometer input.	I 3.3V	PU 10k 3.3V	

Table 33 Onboard Camera Interface Signal Descriptions

Signal	Pin #	Description	I/O Type	Comment
CAM_PWR	1	3.3V +/- 5% supply voltage to power the camera device	3.3V O	
CAM_PWR	2	3.3V +/- 5% supply voltage to power the camera device	3.3V O	
CAM0_CSI_D0+	3	CSI2 Camera 0 Data Lane 0+	I	
CAM0_CSI_D0-	4	CSI2 Camera 0 Data Lane 0-	I	
GND	5			Ground
CAM0_CSI_D1+	6	CSI2 Camera 0 Data Lane 1+	I	
CAM0_CSI_D1-	7	CSI2 Camera 0 Data Lane 1-	I	
GND	8			Ground
CAM0_CSI_D2+	9	CSI2 Camera 0 Data Lane 2+	I	
CAM0_CSI_D2-	10	CSI2 Camera 0 Data Lane 2-	I	
CAM0_RST#	11	Camera 0 Reset (low active)	CMOS 1.8V	
CAM0_CSI_D3+	12	CSI2 Camera 0 Data Lane 3+	I	
CAM0_CSI_D3-	13	CSI2 Camera 0 Data Lane 3-	I	
GND	14			Ground
CAM0_CSI_CLK+	15	CSI2 Camera 0 Differential Clock+ (Strobe)	I	
CAM0_CSI_CLK-	16	CSI2 Camera 0 Differential Clock- (Strobe)	I	
GND	17			Ground
CAM0_I2C_CLK	18	Camera 0 Control Interface, CLK. (I²C like interface)	CMOS 1.8V OD	
CAM0_I2C_DAT	19	Camera 0 Control Interface, DATA. (I²C like interface)	CMOS 1.8V OD	
CAM0_ENA#	20	Camera 0 Enable (low active)	CMOS 1.8V	
MCLK	21	Master Clock. May be used by Cameras to drive it's internal PLL Frequency range: 6...27 MHz	CMOS 1.8V O	
CAM1_ENA#	22	Camera 1 Enable (low active)	CMOS 1.8V	
CAM1_I2C_CLK	23	Camera 1 Control Interface, CLK. (I²C like interface)	CMOS 1.8V OD	
CAM1_I2C_DAT	24	Camera 1 Control Interface, DATA. (I²C like interface)	CMOS 1.8V OD	
GND	25			Ground
CAM1_CSI_CLK+	26	CSI2 Camera 1 Differential Clock+ (Strobe)	I	
CAM1_CSI_CLK-	27	CSI2 Camera 1 Differential Clock- (Strobe)	I	
GND	28			Ground
CAM1_CSI_D0+	29	CSI2 Camera 1 Data Lane 0+	I	
CAM1_CSI_D0-	30	CSI2 Camera 1 Data Lane 0-	I	
CAM1_RST#	31	Camera 1 Reset (low active)	CMOS 1.8V	
CAM1_CSI_D1+	32	CSI2 Camera 1 Data Lane 1+	I	
CAM1_CSI_D1-	33	CSI2 Camera 1 Data Lane 1-	I	
GND	34			Ground
CAM0_GPIO	35	GPIO for Camera 0	CMOS 1.8V	
CAM1_GPIO	36	GPIO for Camera 1	CMOS 1.8V	

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-QA3/QA3E module is functionally identical with a standard PC/AT. The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.1.1 LPC Bus

On the conga-QA3/QA3E the Platform Controller Hub (PCH) acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCH and the LPC Bus. Some fixed I/O space ranges seen by the processor are listed below:

Table 34 IO Space Ranges

Device	IO Address
8259 Master	20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39h, 3Ch-3Dh
8254s	40h-43h, 50h-53h
Ps2 Control	60h, 64h
NMI Controller	61h, 63h, 65h, 67h
RTC	70h-77h
Port 80h	80h-83h
Init Register	92h
8259 Master	A0h- A1h, A4h-A5h, A8h-A9h, Ach-ADh, B0h-B1h, B4h-B5h, B8h-B9h, Bch-BDh, 4D0h-4D1h
PCU UART	3F8h-3FFh
Reset Control	CF9h
Active Power Management	B2h-B3h

Some of these ranges are used by a Super I/O if implemented on the carrier board or are occupied by the Qseven on-module UARTs if these are enabled in the setup. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 35 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	SoC Transaction Router
00h	02h	00h	Graphics and Display
00h	12h	00h	SD Port
00h	13h	00h	SATA AHCI/IDE Controller
00h	14h	00h	XHCI USB
00h	17h	01h	eMMC 4.5 Port
00h	1Ah	00h	Trusted Execution Engine
00h	1Bh	00h	HD Audio
00h	1Ch	00h	PCI Express Root Port 0
00h	1Ch	01h	PCI Express Root Port 1
00h	1Ch	02h	PCI Express Root Port 2
00h	1Ch	03h	PCI Express Root Port 3
00h	1Dh	00h	EHCI USB
00h	1Fh	00h	LPC: Bridge to Intel Legacy Port
00h	1Fh	03h	SMBus Port
04h	00h	00h	Intel I210 Ethernet Network

Note

1. *The PCI Express Ports are visible only if they are set to "Enabled" in the BIOS setup program and a device attached to the corresponding PCI Express port on the carrier board.*

2. *The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on the actual configuration of the hardware.*

9.3 PCI Interrupt Routing Map

Table 36 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line [1]	APIC Mode IRQ	Graphic	SD Card	SATA	XHCI	eMMC 4.5 Port	TXE	HD Audio	PCI-EX Root Port 0	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	EHCI USB	SMBus Port	I210 Ethernet Network
A	INTA	16	x	x	x	x	x	x	x	x				x		x [2]
B	INTB	17									x				x	x [3]
C	INTC	18										x				x [4]
D	INTD	19											x			x [5]
E		20														
F		21														
G		22														
H		23														

Note

[1] *These interrupt lines are virtual (message based).*

[2] *Interrupt used by single function PCI Express devices (INTA).*

[3] *Interrupt used by multifunction PCI Express devices (INTB).*

[4] *Interrupt used by multifunction PCI Express devices (INTC).*

[5] *Interrupt used by multifunction PCI Express devices (INTD).*

9.4 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.5 SM Bus

System Management (SM) bus signals are connected to the Intel® Bay Trail SoC and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

10 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

10.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <ESC> key during POST.

10.1.1 Boot Selection Popup

Press the <F11> key during POST to access the Boot Selection Popup menu. A selection menu displays immediately after POST, allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

10.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar, left frame and right frame. The menu bar is shown below:

Main	Advanced	Chipset	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

10.3 Main Setup Screen

When you first enter the BIOS setup, you will see the main setup screen. The main setup screen reports BIOS, processor, memory and board information and is for configuring the system date and time. You can always return to the main setup screen by selecting the 'Main' tab.

Feature	Options	Description
Main BIOS Version	No option	Displays the main BIOS version.
OEM BIOS Version	No option	Displays the additional OEM BIOS version.
Build Date	No option	Displays the date the BIOS was built.
Product Revision	No option	Displays the hardware revision of the board.
Serial Number	No option	Displays the serial number of the board.
BC Firmware Revision	No option	Displays the firmware revision of the congatec board controller.
MAC Address	No option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	No option	Displays the number of boot-ups. (max. 16777215).
Microcode Patch	No option	Displays the microcode patch loaded for the onboard CPU.
Baytrail SoC	No option	B3 Stepping.
Total Memory	No option	Total amount of low voltage DDR3 present on the system.
System Date	Day of week, month/ day/year	Specifies the current system date. **Note:** The date is in month/day/year format.
System Time	Hour:Minute:Second	Specifies the current system time. **Note:** The time is in 24 hour format.

10.4 Advanced Setup

Select the advanced tab from the setup menu to enter the advanced BIOS setup screen. The menu is used for setting advanced features and only features described within this user's guide are listed.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Watchdog				
	Graphics				
	Hardware Health Monitoring				
	Trusted Computing				
	RTC Wake				
	Module Serial Ports				
	Reserve Legacy Interrupt				
	ACPI				
	Super IO				
	Intel(R) Smart Connect Technology				
	Serial Port Console Redirection				
	CPU Configuration				
	PPM Configuration				
	Thermal Configuration				
	IDE Configuration				
	Miscellaneous Configuration				
	SCC Configuration				
	PCI Subsystem Settings				
	Network Stack				
	CSM Configuration				
	SDIO				
	USB				
	Platform Trust Technology				
	Security Configuration				
	Intel(R) I210 Gigabit Network				
	Driver Health				

10.4.1 Watchdog Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup of the boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One-time Trigger Single Event Repeated Event	Select the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to 'One-time Trigger' the watchdog will be disabled after the first trigger. If set to 'Single Event', every stage will be executed only once, then the watchdog will be disabled. If set to 'Repeated Event' the last stage will be executed repeatedly until a reset occurs.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Select the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event, see note below.
Event 2	**Disabled** ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** ACPI Event Reset Power Button	Select the type of event that will be generated when timeout 3 is reached.

Feature	Options	Description
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Select the timeout value for the first stage watchdog event.
Timeout 2	See above	Select the timeout value for the second stage watchdog event.
Timeout 3	See above	Select the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

In ACPI mode, it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

10.4.2 Graphics Submenu

Feature	Options	Description
Boot Display Device	VBIOS Default	
CRT	**Enable** Disable	Enable or disable CRT video interface.
Active LFP	No LVDS **LVDS**	Select the active local flat panel configuration.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel. If no external EDID data set is found, the data set selected under 'Local Flat Panel Type' will then be used as a fallback data set.
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 2x24 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.
Backlight Inverter Type	None **PWM** I2C	Select the type of backlight inverter used. PWM = Use IGD PWM signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.
Digital Display Interface 1 (DDI1)	Disabled DisplayPort **HDMI™/DVI** Auto	Select the output type of the digital display interface.
PWM Inverter Frequency (Hz)	**200** - 40000	Set the PWM inverter frequency in Hz. Only visible if 'Backlight Inverter Type' is set to 'PWM'.
PWM Inverter Polarity	**Normal** Inverted	Select PWM inverter polarity. Only visible if 'Backlight Inverter Type' is set to 'PWM' .

Feature	Options	Description
Backlight Setting	0% 10% 25% 40% 50% 60% 75% 90% **100%**	Actual backlight value in percent of the maximum setting.
Force LVDS Backlight	**No** Yes	If set to 'Yes', the board controller forces backlight enable signal unconditionally (independently from SoC Backlight Signal).
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Backlight Delay	**No Delay** 100ms Delay 250ms Delay 500ms Delay 1s Delay	The board controller will add a delay on the backlight signal coming from the SoC according this setup node. This delay is intended to adjust some LVDS Panel Timings.
LVDS SSC	**Disabled** 0.5% 1.0% 1.5% 2.0% 2.5%	Configure LVDS Spread Spectrum Clock Modulation depth. It performs a center spreading and a fixed modulation frequency of 32.9kHz.

10.4.3 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	No option	Displays the actual CPU Temperature in °C.
Board Temperature	No option	Displays the actual Board Temperature in °C.
12V Standard	No option	Displays the actual 12V Standard Voltage.
5Volts Standby	No option	Displays the actual 5V Standby Voltage.
Input Current (12V Standard)	No option	Displays the actual Input current of 12V Standard power plane.
CPU Fan Speed	No option	Displays the actual CPU Fan Speed in RPM.
Fan PWM Frequency Mode	Low Frequency High Frequency	Select the fan PWM base frequency mode: 'Low Frequency' - 11.0 to 88.2Hz 'High Frequency' - 1k to 63kHz
Fan PWM Frequency (kHz)	1 - 63	Select the fan PWM base frequency. Default: 31kHz.

10.4.4 Trusted Computing Submenu

Feature	Options	Description
Security Device Support	**Disabled** Enabled	Enable or disable TPM support. System reset is required after change.
User Confirmation	Disabled **Enabled**	Enable or disable user confirmation requests for certain transactions.
TPM State	**Disabled** Enabled	Enable or disable TPM chip. **Note:** System might restart several times during POST to acquire target state.
Pending operation	**None** Enable Take Ownership Disable Take Ownership TPM Clear	Perform selected TPM chip operation. **Note:** System might restart several times during POST to perform selected operation.

10.4.5 RTC Wake Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour		Specify wake up hour. For example, enter "3" for 3am and "15" for 3pm.
Wake up minute		Specify wake up minute.
Wake up second		Specify wake up second.

10.4.6 Module Serial Ports Submenu

Feature	Options	Description
Serial Port 0	**Disabled** Enabled	Enable or disable module serial port 0.
Serial Port 1	**Disabled** Enabled	Enable or disable module serial port 1.

10.4.7 Reserve Legacy Interrupt Submenu

Feature	Options	Description
Reserve Legacy Interrupt 1/2/3	**None** IRQ3 IRQ4 IRQ5 IRQ6 IRQ10 IRQ11 IRQ14 IRQ15	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.

10.4.8 ACPI Submenu

Feature	Options	Description
Enable ACPI Auto Configuration	Disabled Enabled	Enable or disable BIOS ACPI Auto Configuration
Enable Hibernation	Disabled **Enabled**	Enable or disable system's ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend.
Lock Legacy Resources	**Disabled** Enabled	Enable or disable locking of legacy resources.
LID Support	Disabled **Enabled**	Activate ACPI LID button support
Sleep Button Support	Disabled **Enabled**	Activate ACPI sleep button support

10.4.9 SIO Submenu

Feature	Options	Description
AMI SIO Driver Version		
SIO Clock	24 MHz, **48 MHz**	Select Super IO base clock
▶Serial Port 1	No option	Serial Port 1 Submenu
▶Serial Port 2	No option	Serial Port 2 Submenu
▶Parallel Port	No option	Parallel Port Submenu

Note

In ACPI mode, it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec

10.4.10 Serial Port 1 Submenu

Feature	Options	Description
Serial Port	**Enable** Disable	Enable or disable Serial Port (COM).
Change Settings	**Auto** IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11, 12; DMA;	Select optimal settings for Super IO device.

10.4.11 Serial Port 2 Submenu

Feature	Options	Description
Serial Port	**Enable** Disable	Enable or disable Serial Port (COM).
Change Settings	**Use Automatic Settings** IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11, 12; DMA;	Serial Port 2 configuration options.
Device Mode	**Standard Serial Port Mode** IrDA Active pulse 1.6 uS IrDA Active pulse 3/16 bit time ASKIR Mode	Change the Serial Port mode.

10.4.12 Parallel Port Submenu

Feature	Options	Description
Parallel Port	Enabled **Disabled**	Enable or disable Parallel Port (LPT/LPTE).

10.4.13 Intel(R) Smart Connect Technology Submenu

Feature	Options	Description
ISCT Support	**Disabled** Enabled	Enable or disable Intel(R) Smart Connection Support. When this setup node is set to Disabled, all the other Nodes will not be visible.
ISCT Notification Control	Disabled **Enabled**	Enable or Disable ISCT Notification Control.
ISCT WLAN Power Control	Disabled **Enabled**	Enable or Disable ISCT WLAN Power Control.
ISCT WWAN Power Control	Disabled **Enabled**	Enable or Disable ISCT WWAN Power Control
ISCT Sleep Duration Value Format	**Duration in Seconds**	ISCT Sleep Duration in seconds.
ISCT RF Kill Switch Type	Software **Hardware**	Select ISCT RF Kill Switch Type
ISCT RTC Timer Support	**Disabled** Enabled	Enable ISCT RTC Timer

10.4.14 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
▶Console Redirection Settings (COM0)	Submenu	Opens console redirection configuration sub menu.
COM1 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
▶Console Redirection Settings (COM1)	Submenu	Opens console redirection configuration submenu.
Serial Port for Out-of-Band Management / EMS Console Redirection	**Disabled** Enabled	Enable or disable Serial Port for Out-of-Band Management / Windows Emergency Management Services.
▶Console Redirection Settings	Submenu	Opens console redirection configuration submenu.

10.4.14.1 Console Redirection Settings COM0 Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.
Baudrate	9600 19200 38400 57600 **115200**	Select baud rate.
Data Bits	7 **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enable or disable extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select Function Key and KeyPad on Putty.

10.4.14.2 Console Redirection Settings COM1 Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.
Baudrate	9600 19200 38400 57600 **115200**	Select baud rate.
Data Bits	7 **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enable or disable extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select Function Key and KeyPad on Putty.

10.4.14.3 Console Redirection Settings Out-of-Band Management Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ **VT-UTF8** ANSI	Select terminal type.
Bits Per Second	9600, 19200, 38400, 57600, **115200**	Select baud rate.
Data Bits	**8**	Set number of data bits.
Parity	**None**	Select parity.
Stop Bits	**1**	Set number of stop bits.

10.4.15 CPU Configuration Submenu

Feature	Options	Description
▶Socket 0 CPU Information	Submenu	Socket specific CPU information.
▶CPU Thermal Configuration	Submenu	CPU thermal configuration options.
CPU Speed	No option	Displays the CPU clock frequency.
64-bit	No option	Displays whether 64-bit is supported.
Limit CPUID Maximum	**Disabled** Enabled	When enabled, the processor limits the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When disabled, the processor returns the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Execute Disable Bit	Disabled **Enabled**	Enable or disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled, certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting operating system.
Hardware Prefetcher	Disabled **Enabled**	Enable or disable the Mid Level Cache (MLC) streamer prefetcher.
Adjacent Cache Line Prefetch	Disabled **Enabled**	Enable or disable prefetching of adjacent cache lines.
Intel Virtualization Technology	Disabled **Enabled**	Enable or disable support for the Intel virtualization technology.
Power Technology	Disable **Energy Efficient** Custom	Configure the power technology schema for the CPU.

10.4.15.1 Socket 0 CPU Information Submenu

Feature	Options	Description
CPU Name	No option	Displays socket specific CPU name.
CPU Signature	No option	Displays CPU signature number.
Microcode Patch	No option	Displays the CPU microcode patch number.
Max. CPU Speed	No option	Displays the maximal CPU clock frequency.
Min. CPU Speed	No option	Displays the minimal CPU clock frequency.
Processor Cores	No option	Displays the number of CPU core on Socket CPU.
Intel HT Technology	No option	Displays the Intel HT Technology support information.
Intel VT-x Technology	No option	Displays the Intel VT-x Technology support information.
L1 Data Cache	No option	Displays the Socket L1 data cache information.
L1 Code Cache	No option	Displays the Socket L1 code cache information.
L2 Cache	No option	Displays the Socket L2 data cache information.
L3 Cache	No option	Displays the Socket L3 data cache information.

10.4.15.2 CPU Thermal Configuration Submenu

Feature	Options	Description
DTS	Enabled **Disabled**	Enable or Disable CPU Digital Thermal Sensor (DTS). DTS is used on ACPI functions to read the CPU temperature. This value is read from MSR.

10.4.16 PPM Configuration Submenu

Feature	Options	Description
CPU C state Report	Disabled **Enabled**	Enable/Disable CPU state Report to Operating System.
Max CPU C state	C7 C6 **C1**	Maximal CPU C state supported by the CPU.
SOix	**Disabled** Enabled	Enable/Disable CPU SOix state support.

10.4.17 Thermal Configuration

Feature	Options	Description
Critical Trip Point	110 C 105 C 100 C 95 C **90 C** 87 C 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Temperature of the ACPI critical Trip Point in which the OS will shut the system off.
Passive Trip Point	110 C 105 C 100 C 95 C **90 C** 87 C 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Temperature of the ACPI passive Trip Point in which the OS will begin throttling the processor.

Feature	Options	Description
Active Trip Point High	110 C 105 C 100 C 95 C 90 C 87 C 85 C **79 C** 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	This value controls the temperature of the ACPI active Trip Point – the point at which the operating system will enable the active cooling device at maximum capacity. DST must be enabled on the CPU Submenu to make this node effective.
Active Trip Point Low	110 C 105 C 100 C 95 C 90 C 87 C 85 C 79 C **71 C** 63 C 55 C 47 C 39 C 31 C 23 C 15 C	This value controls the temperature of the ACPI active Trip Point – the point at which the operating system will enable the active cooling device at half capacity. DST must be enabled on the CPU Submenu to make this node effective.

10.4.18 IDE Configuration Submenu

Feature	Options	Description
Serial-ATA (SATA)	**Enabled** Disabled	Enable or disable the onboard SATA controller.
SATA Test Mode	Enabled **Disabled**	Should be set to Disabled. Test Mode is used just for verification measurements.
SATA Speed Support	Gen1 **Gen2**	Indicates the maximum speed the SATA controller can support.

Feature	Options	Description
SATA ODD Port	Port 0 ODD Port 1 ODD **No ODD**	Configure which SATA Port is ODD.
SATA Mode	IDE Mode **AHCI Mode**	Configure SATA Port Mode.
Serial-ATA Port 0	**Enabled** Disabled	Enable or disable the SATA Port 0.
mSATA Interface	mSATA mPCIe **Auto**	Configures the physical interface to support mSATA or mPCIE.
SATA Port 0 Hot Plug	**Disabled** Enabled	Select hot plug support for SATA Port 0. Not possible in Native IDE mode.
Serial-ATA Port 1	**Enabled** Disabled	Enable or disable the SATA Port 1.
SATA Port 1 Hot Plug	**Disabled** Enabled	Select hot plug support for SATA Port 1. Not possible in Native IDE mode.
SATA Port 0 Information	No Option	Displays Information of device detected on SATA Port 0.
SATA Port 1 Information	No Option	Displays Information of device detected on SATA Port 1.

10.4.19 Miscellaneous Configuration Submenu

Feature	Options	Description
High Precision Timer	**Enabled** Disabled	Enable or disable the high precision event timer.
Boot Timer with HPET Timer	Enabled **Disabled**	Allow boot timer calculation with the high precision event timer.
PCI Express Dynamic Clock Gating	Enabled **Disabled**	Enable dynamic clock gating.

10.4.20 SCC Configuration Submenu

Feature	Options	Description
SCC Device Mode	ACPI Mode **PCI Mode**	Configure the storage control cluster working mode.
SCC eMMC Support	Enable eMMC 4.5 Support Enable eMMC 4.41 Support **eMMC AUTO MODE** Disable	Enable SCC eMMC support and configure eMMC mode.
SCC 4.5 DDR50 eMMC Support	**Enabled** Disabled	Enable DDR50 eMMC support.

Feature	Options	Description
SCC 4.5 HS200 eMMC Support	Enabled **Disabled**	Enable DDR50 eMMC support.
eMMC Secure Erase	Enabled **Disabled**	Enable eMMC secure erase support.
SCC SD Card Support	**Enabled** Disabled	Enable storage control cluster SD Card support
SDR25 Support for SD Card	**Enabled** Disabled	Enable SDR25 Support for SD Card
DDR50 Support for SD Card	Enabled **Disabled**	Enable DDR50 Support for SD Card
MIPI Camera Support	**Disabled** Enabled for Windows Enabled for Linux	Enable or disable support for ISP device, MIPI CSI interface and dedicated camera I2C bus. ISP can either be a part of IGD device (for Windows) or a separate device (for Linux).

10.4.21 PCI Subsystem Settings Submenu

Feature	Options	Description
PCI Settings		
PCI Latency Timer	**32** 64 96 128 160 192 224 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
PCI-X Latency Timer	**32** 64 96 128 160 192 224 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate SERR#.

Feature	Options	Description
Above 4G Decoding	**Disabled** Enabled	Enable or disable 64bit capable devices to be decoded in above 4G address space (Only if system supports 64 bit PCI decoding).
SR-IOV Support	**Disabled** Enabled	If the system has a SR-IOV capable PCIe Devices, this option enables or disables Single Root IO Virtualization support.
▶PCI Express Settings	Submenu	Opens the PCI Express Settings submenu.
▶PCI Express GEN 2 Settings	Submenu	Opens the PCI Express Generation 2 Settings submenu.

10.4.22 PCI Express Settings Submenu

Feature	Options	Description
Relaxed Ordering	**Disabled** Enabled	Enables or Disables PCI Express Device Relaxed Ordering.
Extended Tag	**Disabled** Enabled	If enabled, allows device to use 8-bit Tag field as a requester.
No Snoop	**Enabled** Disabled	Enables or Disables PCI Express Device No Snoop option.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 1096 Bytes	Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 1096 Bytes	Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.
ASPM Support	**Disabled** Auto Force L0s	Set the ASPM Level: Force L0s – Force all links to L0s State. Auto – BIOS auto configure. Disable – Disables ASPM
Extended Synch	**Disabled** Enabled	If enabled, allows generation of Extended Synchronization patterns.
SR-IOV Support	**Disabled** Enabled	If the system has a SR-IOV capable PCIe Devices, this option enables or disables Single Root IO Virtualization support.
Link Training Retry	Disabled 2 3 **5**	Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

Feature	Options	Description
Link Training Timeout (uS)	10 - 10000	Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status Register. Value range from 10 to 10000 uS. Default: 1000
Unpopulated Links	**Keep Link ON** Disabled	In order to save power, software will disable unpopulated PCI Express links if this option set to 'Disable Link'.
Restore PCIE Registers	Enabled **Disabled**	On non-PCI Express aware operating systems (Pre Windows Vista) some devices may not be correctly reinitialized after S3. Enabling this restores PCI Express device configurations on S3 resume. **Warning:** Enabling this may cause issues with other hardware after S3 resume.

10.4.23 PCI Express GEN 2 Settings Submenu

Feature	Options	Description
Completion Timeout	**Default** Shorter Longe Disabled	In device Functions that support Completion Timeout programmability, allows system software to modify the Completion Timeout value. 'Default' 50us to 50ms. If 'Shorter' is selected, software will use shorter timeout ranges supported by hardware. If 'Longer' is selected, software will use longer timeout ranges.
ARI Forwarding	**Disabled** Enabled	Set to 'Enabled', the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type1 Configuration Request into a Type0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
AtomicOp Requester Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this function initiates AtomicOp Requests only if Bus Master Enable bit is in the Command Register Set.
AtomicOp Egress Blocking	**Disabled** Enabled	If supported by hardware and set to 'Enabled', outbound AtomicOp Requests via Egress Ports will be blocked.
IDO Request Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated.
IDO Completion Enable	**Disabled** Enabled	If supported by hardware and set to 'Enable', this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated.
LTR Mechanism Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this enables the Latency Tolerance Reporting (LTR) Mechanism.
End-End TLP Prefix Blocking	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this function will block forwarding of TLPs containing End-End TLP Prefixes.
Target Link Speed	**Auto** Force to 2.5 GT/s Force to 5.0 GT/s	If supported by hardware and set to 'Force to 2.5 GT/s' for Downstream Ports, this sets an upper limit an Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.
Clock Power Management	**Disabled** Enabled	If supported by hardware and set to 'Enabled', the device is permitted to use CLKREQ# signal for power management of Link clock in accordance to protocol defined in appropriate form factor specification.
Compliance SOS	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this will force LTSSM to send SKP Ordered Sets between sequences when sending Compliance Pattern or Modified Compliance Pattern.
Hardware Autonomous Width	**Disabled** Enabled	If supported by hardware and set to 'Disabled', this will disable the hardware´s ability to change link width except for the purpose of correcting unstable link operation.
Hardware Autonomous Speed	**Disabled** Enabled	If supported by hardware and set to 'Disabled', this will disable the hardware´s ability to change link speed except speed rate reduction for the purpose of correcting unstable link operation.

10.4.24 Network Stack

Feature	Options	Description
Network Stack	Enabled **Disabled**	Enable or disable the UEFI network stack.
Ipv4 PXE Support	Enabled **Disabled**	Enable Ipv4 PXE boot support. If disabled IPV4 PXE boot option will not be created.
Ipv6 PXE Support	Enabled **Disabled**	Enable Ipv6 PXE boot support. If disabled IPV6 PXE boot option will not be created.
PXE boot wait time	0 - **5**	Wait time to press ESC to abort PXE Boot

10.4.25 CSM Submenu

Feature	Options	Description
Launch CSM	**Enabled** Disabled	Enable the Compatibility Support Module.
CSM16 Module Version	No option	Display CSM Module Version number.
Gate A20 Active	**Upon Request** Always	Configure legacy Gate A behavior.
Option ROM Messages	**Force BIOS** Keep Current	Enable Option ROM message
Boot Option Filter	UEFI and Legacy **Legacy Only** UEFI Only	Controls which devices / boot loaders the system should boot to.
Network	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and legacy Network option ROMs.
Storage	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and legacy Storage option ROMs.
Video	Do not launch UEFI only **Legacy only**	Controls the execution of UEFI and legacy Video option ROMs
Other PCI Devices	**UEFI only** Legacy only	Controls the execution of UEFI and legacy option ROMs for any other PCI device different to Network, Video and Storage.

10.4.26 SDIO Submenu

Feature	Options	Description
SDIO Access Mode	**Auto** DMA PIO	Controls the SDIO Access mode to the device.

10.4.27 USB Submenu

Feature	Options	Description
USB Module Version	No option	Displays the version of the USB module.
USB Devices	No option	Displays the detected USB devices.
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
xHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without xHCI hand-off support. The xHCI ownership change should be claimed by xHCI OS driver.
EHCI Hand-off	**Disabled** Enabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI OS driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable Mass Storage Driver Support.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device start unit command timeout.
USB Transfer Timeout	1 sec 5 sec 10 sec **20 sec**	The timeout value for control, bulk, and interrupt transfers.
Device Power -Up Delay Selection	**Auto** Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power -Up Delay Value	0 - 40	Actual power-up delay value in seconds. Default: 5

10.4.28 Platform Trust Technology

Feature	Options	Description
fTPM	**Disabled** Enabled	Enable Trusted Platform Module support.

10.4.29 Security Configuration

Feature	Options	Description
TXE	**Enabled** Disabled	Enable Trusted Execution Engine.
TXE HMRFPO	Enable **Disable**	Enable Host ME Region Flash Protection Overwrite.
TXE Firmware Update	**Enabled** Disabled	Enable Firmware update.
TXE EOP Message	**Enabled** Disabled	Enable TXE End of Post Message.
TXE Unconfiguration Perform	No option	Execute a TXE unconfiguration command
Intel(R) Anti-Theft Technology Configuration	No option	
Intel(R) AT	Enabled Disabled	Enable Anti-Theft technology.
Intel(R) AT Platform PBA	Enabled **Disabled**	Enable Anti-Theft Platform Pre-boot Authentication.
Intel(R) AT Suspend Mode	Enabled **Disabled**	Enable Anti-Theft Suspend Mode.

10.4.30 Intel(R) Ethernet Connection I210 Submenu

At this submenu additionally to its title the MAC address is displayed at the end of the title.

Feature	Options	Description
► NIC Configuration	submenu	Opens the NIC Configuration submenu.
Blink LEDs	**0** - 15	The Ethernet LEDs will blink so many seconds long as entered.
UEFI Driver	No option	Displays the UEFI Driver version.
Adapter PBA	No option	Displays the Adapter PBA.
Chip Type	No option	Displays the type of the Chip in which the Ethernet controller is integrated.
PCI Device ID	No option	Displays the PCI Device ID of the Ethernet controller.
Bus:Device:Function	No option	Displays the PCI Bus:Device:Function number of the Ethernet controller.
Link Status	No option	Displays the Link Status.
MAC Address	No option	Displays the MAC Address.

10.4.30.1 NIC Configuration Submenu

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake on LAN	Disabled **Enabled**	Enables Wake on LAN (WOL) feature

10.4.31 Driver Health Submenu

Feature	Options	Description
► Intel(R) PRO/1000	No option	Provides Health Status for the drivers/Controllers connected to the System

10.4.31.1 Intel(R) PRO/1000 Submenu

Feature	Options	Description
Controller Information	No option	Provides Health Status of the controller

10.5 Chipset Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.5.1 North Bridge Submenu

Feature	Options	Description
Memory Information		
Total Memory	No option	Total amount of memory detected by the system
Memory Slot 0	No option	Memory detected by the system on Slot 0
Memory Slot 1	No option	Memory detected by the system on Slot 1
Max TOLUD	**Dynamic** 2GB 2.25 GB 2.5 GB 2.75 GB 3 GB	Selects the maximal Top of Low Usable DRAM.

Feature	Options	Description
Aperture Size	128MB **256MB** 512MB	Selects Aperture Size value.
PAVC	Enable **Disable**	Enable or disable Protected Audio Video Control.

10.5.2 South Bridge Submenu

Feature	Options	Description
▶Azalia HD Audio	Submenu	Azalia HD Audio Submenu.
▶ USB	Submenu	USB Submenu.
▶ PCI Express Configuration	Submenu	PCI Express Configuration Submenu.
High Precision Timer	**Enabled** Disabled	Enable High Precision Event Timer.
Serial IRQ	Quiet **Continuous**	Configure IRQ Serial Mode
CLKRUN# Logic	Enabled **Disabled**	Enable the CLKRUN# logic to stop the LPC clocks when possible. Requires Serial IRQ Mode to be set to Quiet as well
Global SMI Lock	**Enabled** Disabled	Enable or Disable SMI Lock
BIOS Read/Write Protection	Enabled **Disabled**	Enable BIOS SPI Region read/write protection.
Isolate SMBus Segments	Never During POST **Always**	Allows to isolate the off-module/external SMBus segment from the on-module SMBus segment. This can be a workaround for non-spec conform external SMBus devices.

10.5.2.1 Azalia HD Audio

Feature	Options	Description
LPE Audio Support	**Disable** LPE Audio PCI Mode LPE Audio ACPI Mode	Enable LPE Audio Support.
Audio Controller	**Enabled** Disabled	Enable Audio Controller.
Azalia Vci Enable	**Enabled** Disabled	Enable Azalia Vci.
Azalia Docking Support Enable	Enable **Disable**	Enable Azalia Docking support.
Azalia PME Enable	**Enabled** Disabled	Enable Azalia PME support.

Feature	Options	Description
Azalia HDMI™ Codec	**Enabled** Disabled	Enable Azalia HDMI™ Codec
HDMI™ Port B	**Enabled** Disabled	Enable HDMI™ Port B Audio.
HDMI™ Port C	Enabled **Disabled**	Enable HDMI™ Port C Audio.

10.5.2.2 USB Submenu

Feature	Options	Description
USB OTG Support	**Disabled** Enabled	Enable USB OTG support.
USB VBUS	**On** Off	VBUS should be On in Host Mode and it should be Off in OTG device Mode.
XHCI Mode	Enabled Disabled Auto **Smart Auto**	Select mode for all USB ports (0-3): 'Enabled' - USB ports will function in USB 3.0 mode but require driver on the operating system. USB ports will not function in pre-operating time time if USB 3.0 support in BIOS is disabled (see the USB 3.0 support in BIOS item). 'Disabled' - USB ports will function in USB 2.0 mode only and routed to the EHCI1 controller. 'Auto' - USB ports will initially function in USB 2.0 mode but the operating system driver can switch to USB 3.0. 'Smart Auto' - Identical to 'Auto', except the BIOS will take over the operating system driver setting after each restart. This mode is not available if USB3.0 support is disabled.
USB2 Link Power Management	Disabled **Enabled**	Enable USB2 Link Power Management
USB 2.0(EHCI) Support	**Disabled** Enabled	Control USB EHCI (USB 2.0) functions.
USB Per Port Control	Disabled **Enabled**	Control each of the USB ports (0-3).
USB Port 0	Disabled **Enabled**	Enable Port 0
USB Port 1	Disabled **Enabled**	Enable Port 1
USB Port 2	Disabled **Enabled**	Enable Port 2
USB Port 3	Disabled **Enabled**	Enable Port 3

10.5.2.3 PCI Express Configuration Submenu

Feature	Options	Description
PCIe noncompliance Card	**Not Supported** Supported	Enable PCIe 1.0 Device Support
PCI Express Port 0	Disabled **Enabled**	Enable PCIe Port 0.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 0 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 1	Disabled **Enabled**	Enable PCIe Port 1.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 1 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 2	Disabled **Enabled**	Enable PCIe Port 2.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 2 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 3	Disabled **Enabled**	Enable PCIe Port 3.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 3 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.

10.6 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.6.1 Boot Settings Configuration

Feature	Options	Description
Setup Prompt Timeout	0 - 65535	Number of seconds to wait for setup activation key. Default: 1 0 means no wait for fastest boot (not recommended), 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. **Note:** The default OEM logo is a dark screen.

Feature	Options	Description
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The "Device Based" boot priority list allows you to select from a list of currently detected devices only. The "Type Based" boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the "Device Based" boot priority list might change dynamically in cases when devices are physically removed or added to the system. The "Type Based" boot menu is static and can only be changed by the user.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. Note: Only works with an ATX type power supply.
AT Shutdown Mode	System Reboot **Hot S5**	Determines the behavior of an AT-powered system after a shutdown.
Battery Support	**Auto (Battery Manager)** Battery-Only On I2C Bus Battery-Only On I2C Bus	Select the Battery System Support Bus.It can be I2C, SMBus or Auto.
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
Fast Boot	**Disabled** Enabled	Enable or disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS / legacy boot options.

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

10.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

10.7.1 Security Settings

Feature	Options	Description
Administrator Password	Enter password	Specifies the setup administrator password.
HDD Security Configuration		
List of all detected hard disks supporting the security feature set	Select device to open device security configuration submenu	

10.7.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

10.8 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen. You can display a Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
Boot Override	
List of all boot devices currently detected	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to “Device Based”.

11 Additional BIOS Features

11.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

11.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-QA3 is identified as QA31R1xx, QA32R1xx, QC31R1xx and QC32R1xx where:

- QA31 is the BIOS for modules with Baytrail Single Channel Memory SoC
- QA32 is the BIOS for modules with Baytrail Dual Channel Memory SoC
- R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

The binary size of QA31, QA32, QC31, QC32 and QA3E BIOS is 8MB.

11.3 Updating the BIOS

OEMs often use BIOS updates to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS. The conga-QA3 uses a congatec/AMI AptioEFI firmware, which is stored in an onboard flash ROM chip and can be updated using the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line, Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

11.4 Supported Flash Devices

The conga-QA3 supports the following flash devices:

- Winbond W25Q64JVSSIQ (8MB)

The flash device listed above has been tested and can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.