congatec Application Note

Affected Products	All COM Express® Products
Subject	PCIe® 4.0 Design Considerations for COM Express® Carrier Boards
Confidential/Public	Public
Author	KOL

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
1.0	2023-02-10	KOL	Initial Release

Preface

This application note provides recommendations for COM Express® Computer-On-Module (COM) carrier board designs to comply with PCIe® 4.0 requirements.

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Symbols

The following are symbols used in this application note.

Note

Notes call attention to important information that should be observed.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

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Terminology

Term	Description
PCIe®	Peripheral Component Interconnect Express®
Tx	Transmit Differential Pair
Rx	Receive Differential Pair
COM	Computer-On-Module
SMD	Surface Mount Device
AC	Alternating Current
AIC	Add-In Card
IL	Insertion Loss
N/FEXT	Near/Far-End Crosstalk

1 Introduction

PCIe® 4.0 poses increasingly demanding design and layout requirements. This application note provides recommendations that are crucial—but not always sufficient—for COM Express® carrier board designs to comply with these requirements.

As additional considerations may be required, congatec highly recommends reading the following documents:

- PCIe® 4.0 specification (PCI-SIG®)
- COM Express® specification (Rev. 3.1 added information for PCIe® 4.0)
- COM Express® carrier board design guide

Note

Following the recommendations in this application note is not always sufficient to comply with all the PCIe® 4.0 requirements.

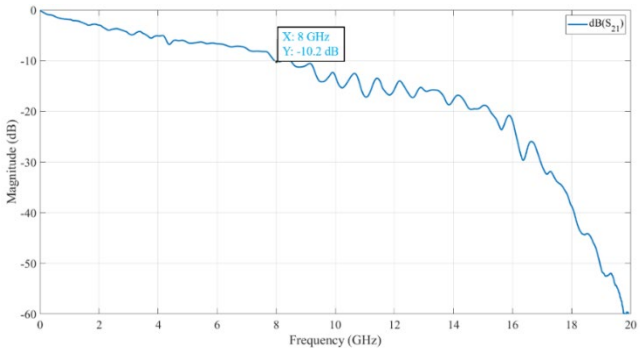
2 Recommendations

2.1 Device-Up Systems

The table below provides recommendations for COM Express® device-up systems to comply with PCIe® 4.0 requirements:

Parameter	Recommendation
Trace length for COM Express® carrier board	4.0 Inches Defined for material with dielectric constant ≈3.57 and dissipation factor ≤0.046 Max. trace length strongly depends on dielectric loss tangent of PCB material
AC coupling capacitors	0201 capacitors preferred and GND cutouts underneath are recommended AC coupling capacitors are placed on the module for PCIe Tx AC coupling capacitors are required for PCIe Rx for device down topology
Max. Intra-Pair Skew	Max. 5 mils
Max. Inter-Pair Skew	No electrical requirements Should not exceed 3 inches to minimize latency
Differential Impedance	85 Ω ± 10 % Impedance-controlled manufacturing is recommended
Microstrip/Stripline	Microstrip only for short routing if vias can be avoided Stripline preferred
Via Usage	2 vias with maximum stub length of 30 mil and removal of unused pads
Via anti-pad	Single oval anti-pad for differential pair Via optimization to match impedance and reduce loss is recommended
Current Return Via	One for each signal
Reference plane	Continuous ground
PCIe® Connector	SMD connector Foxconn 2EF5827-DA9DB-8H or Amphenol 10146067-123Y0LF
COM Express® Connector	ept Colibri Plug 401-55103-51

Based on the recommendations above, congatec measured an insertion loss of - 10.2 dB @ 8 GHz for one of its device-up systems:



This measurement was performed with a VNA. It shows the IL of the channel containing the COM Express® connector, the PCB trace routing of a proprietary congatec test card, the PCIe® Connector, and the PCI-SIG® AIC test fixture.

Figure 1 Insertion Loss Diagram

Note

Perform a signal integrity analysis to ensure proper functionality of the customer system.

2.2 Crosstalk

To prevent problems due to crosstalk:

- Consider interleaved routing when FEXT is more significant than NEXT.
- Consider non-interleaved routing when NEXT is more significant than FEXT.

Alternatively, place ground or low speed signals to both sides of a high-speed differential pair as shown in the table below.

Pin #	Row A	Row B
57	GND	GPO2
58 59	PCIE_TX3+ PCIE_TX3-	PCIE_RX3+ PCIE_RX3-
60	GND	GND
61 62	PCIE_TX2+ PCIE_TX2-	PCIE_RX2+ PCIE_RX2-
63	GPI1	GPO3
64 65	PCIE_TX1+ PCIE_TX1-	PCIE_RX1+ PCIE_RX1-
66	GND	WAKE0#
68 69	PCIE_TX0+ PCIE_TX0-	PCIE_RX0+ PCIE_RX0-
70	GND	GND

The alternative method cannot completely prevent crosstalk at higher clock rates like PCIe® 4.0. It is possible for the high-speed signals to cross-couple via the sideband signal onto the adjacent high-speed line pair. This effect can be counteracted by a capacitor to GND to all sideband signals that are placed between the PCIe® signals.

2.3 Length of Differential Pairs

To compensate for a mismatch between the positive and negative lines of a pair, route the lines in the form of serpentines. The recommended parameters for the serpentines are included in the figure and note below:

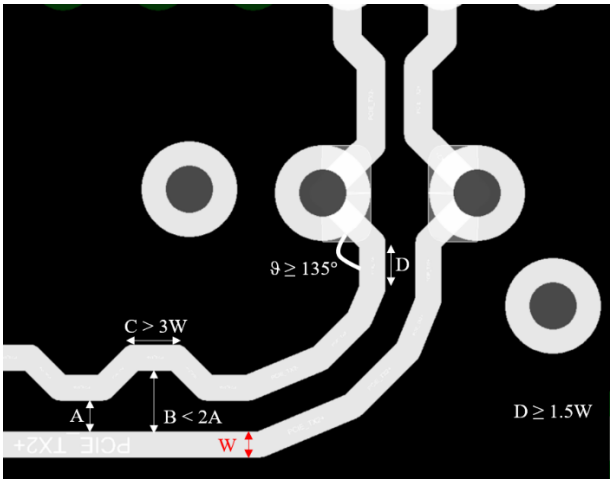


Figure 2 Length-Matching of Differential Pairs

Note

Angles of 90° should be avoided and reduced to a maximum of 45° to ensure proper signal routing. The length C of the serpentines should always be three times the width of the line and distance B should be greater than twice the differential distance of the line pair.

2.4 Fiber Weave Effect

When implementing high-speed lanes into your system, the fiber weave effect must be considered. This effect describes the occurrence of a time delay in the signal between two or more transmission lines of equal length due to the glass fiber reinforced dielectric substrate.

A glass fabric structure is illustrated in the figure below:

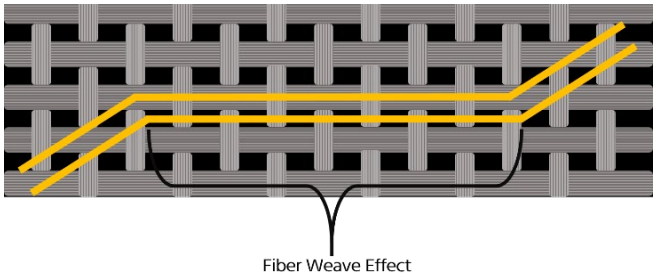


Figure 3 Glass Weave Skew (GWS)

If a line proceeds for a certain length on the yarn of the glass fabric, the propagation velocity differs from the adjacent line of the same length, which extends mostly over the epoxy resin. Differences in propagation velocity can cause a timing skew of up to 7ps.

The figure below shows how to significantly reduce the timing skew:

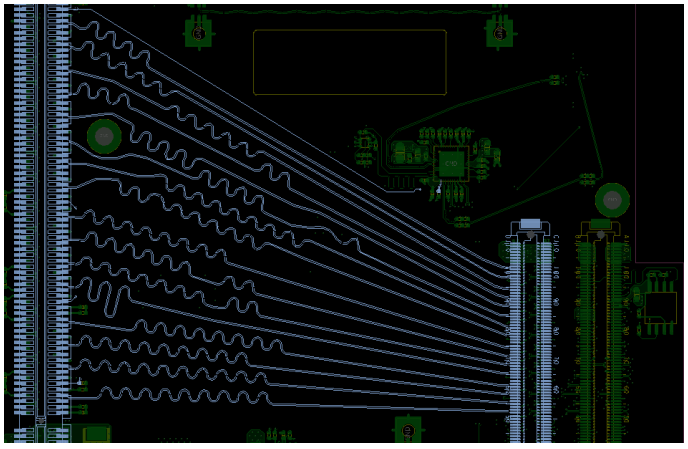


Figure 4 Layout Consideration

The differential pairs are implemented with a slight slope on the PCB. This averages the changes in the material and reduces the variation in the signal speed to a minimum.