QEV2

Qseven 2.0 Evaluation Baseboard

Rev. B.3

Content

Variants

Base Components used on all options

for Qseven module assembly

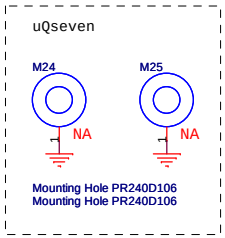
#57000002 MQ7ALUBAR4H, Qseven aluminum bar, 4x M2.5, 70mmx5mmx5mm

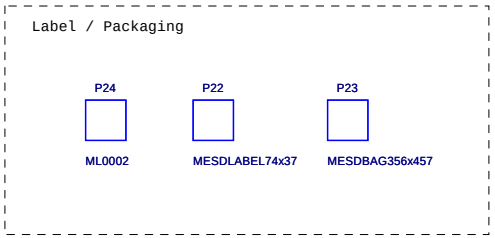
#53000001 4x Machine Screw M2.5x5mm, pan head, philips, DIN7985/ISO7045

#52500001 4x Flat Washer dia. 2.7mm, thickness 0.5mm

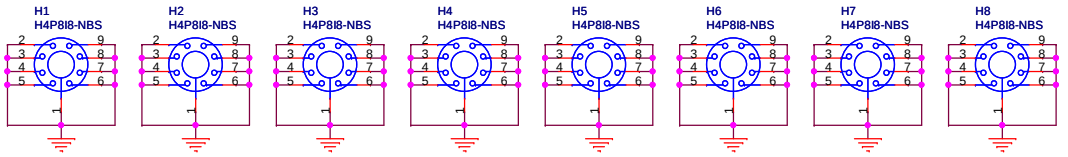
firmware

#63000025 QEVAP001 (to be programmed to U32)

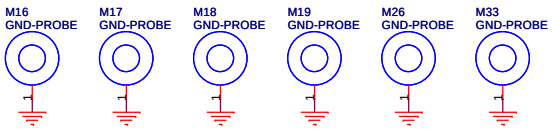




H1-H8 NA



Place close to Qseven PCB cooling plane



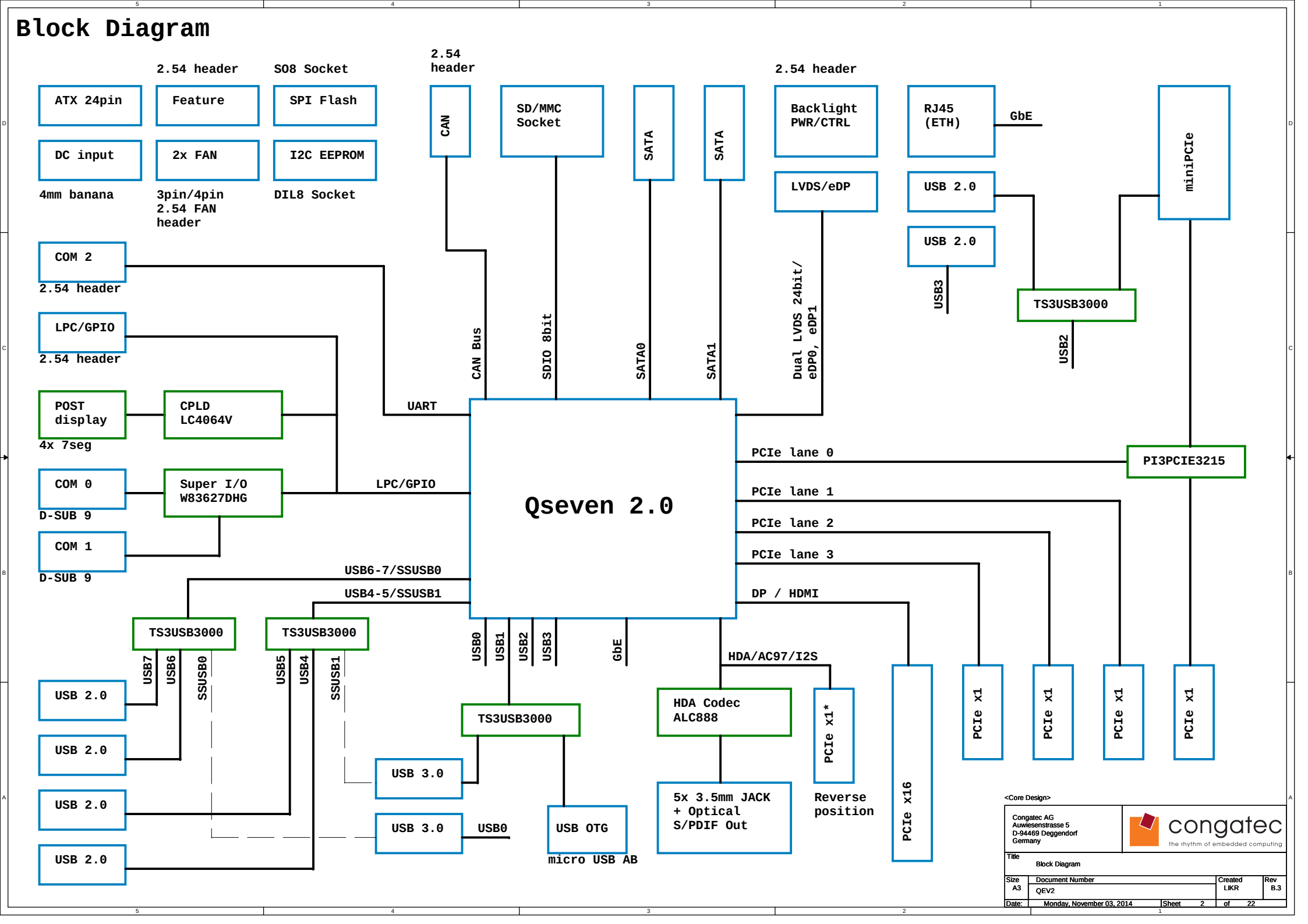
<Core Design>

Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

congatec
the rhythm of embedded computing

Title: MAIN			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 1 of 22		

Block Diagram

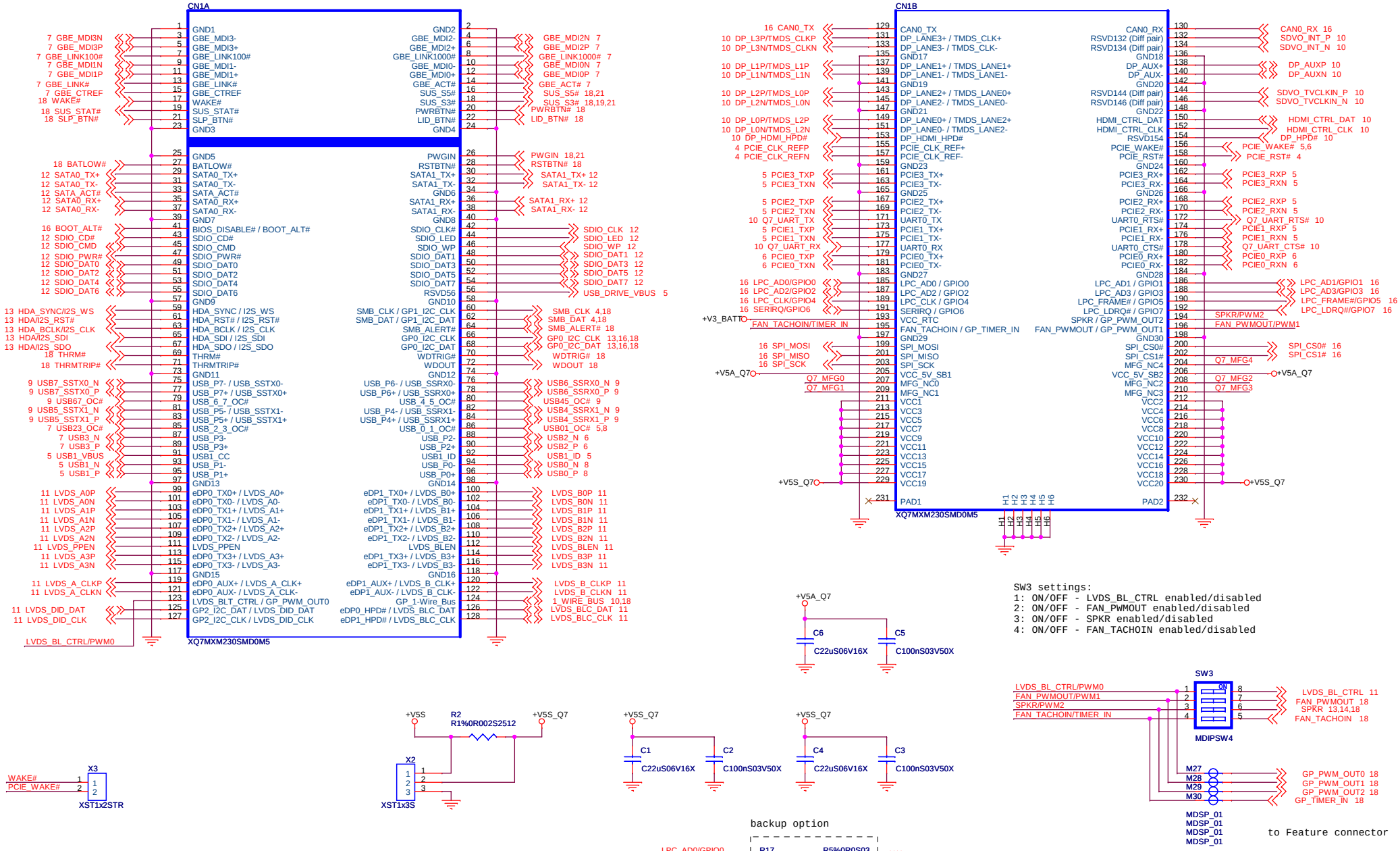


<Core Design>

Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

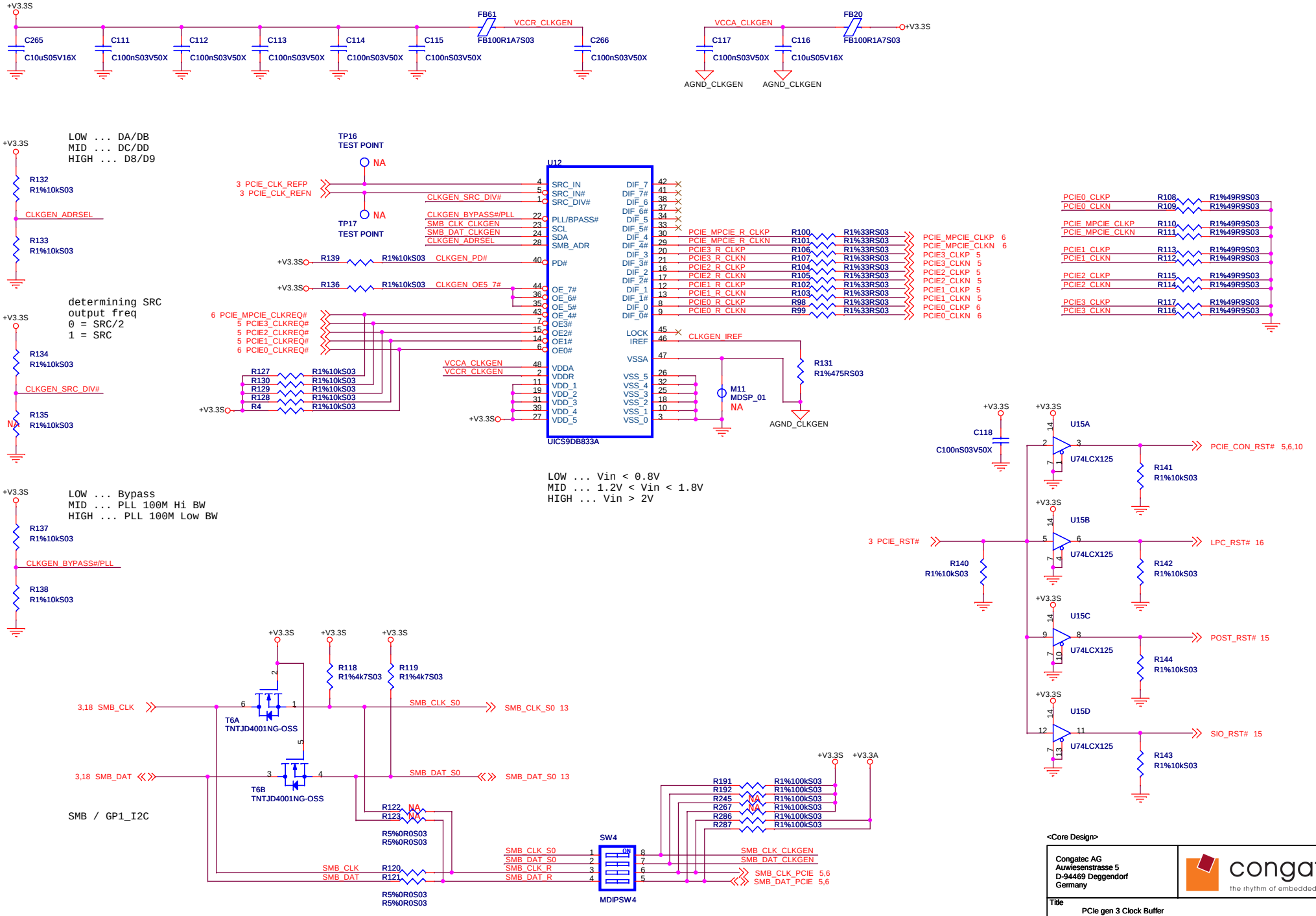
congatec
the rhythm of embedded computing

Title: Block Diagram			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 2 of 22		

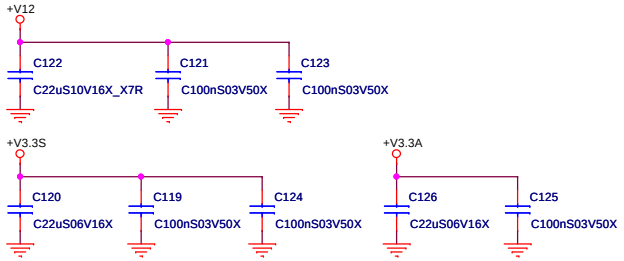


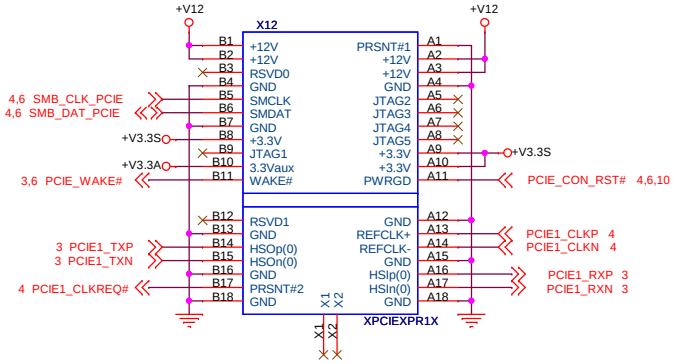
<Core Design>

Congatec AG Auwiesenstrasse 5 D-94469 Deggendorf Germany			
Title: Qseven 2.0 Connector			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 3 of 22		

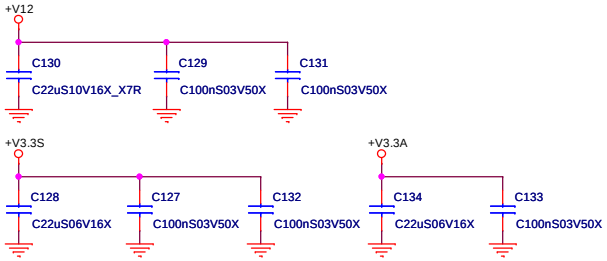

+V3.3S
C265
C10uS05V16X
C111
C100nS03V50X
C112
C100nS03V50X
C113
C100nS03V50X
C114
C100nS03V50X
C115
C100nS03V50X
FB61
FB100R1A7S03
VCCR_CLKGEN
C266
C100nS03V50X
VCCA_CLKGEN
C117
C100nS03V50X
C116
C10uS05V16X
FB20
FB100R1A7S03
+V3.3S
AGND_CLKGEN
AGND_CLKGEN
LOW ... DA/DB
MID ... DC/DD
HIGH ... D8/D9
R132
R1%10kS03
CLKGEN_ADRSEL
R133
R1%10kS03
TP16
TEST POINT
NA
TP17
TEST POINT
NA
U12
3 PCIE_CLK_REFP
3 PCIE_CLK_REFN
SRC_IN
SRC_IN#
SRC_DIV#
CLKGEN_SRC_DIV#
PLL/BPASS#
SCL
SDA
SMB_ADR
CLKGEN_BYPASS#/PLL
SMB_CLK_CLKGEN
SMB_DAT_CLKGEN
CLKGEN_ADRSEL
PD#
CLKGEN_PD#
R139
R1%10kS03
OE_7#
OE_6#
OE_5#
OE_4#
OE3#
OE2#
OE1#
OE0#
CLKGEN_OE5_7#
R136
R1%10kS03
6 PCIE_MPCIE_CLKREQ#
5 PCIE3_CLKREQ#
5 PCIE2_CLKREQ#
5 PCIE1_CLKREQ#
6 PCIE0_CLKREQ#
R127
R130
R129
R128
R4
R1%10kS03
VCCA_CLKGEN
VCCR_CLKGEN
VDDA
VDDR
VDD_1
VDD_2
VDD_3
VDD_4
VDD_5
DIF_7
DIF_7#
DIF_6
DIF_6#
DIF_5
DIF_5#
DIF_4
DIF_4#
DIF_3
DIF_3#
DIF_2
DIF_2#
DIF_1
DIF_1#
DIF_0
DIF_0#
LOCK
IREF
CLKGEN_IREF
VSSA
VSS_5
VSS_4
VSS_3
VSS_2
VSS_1
VSS_0
M11
MDSP_01
NA
R131
R1%475RS03
AGND_CLKGEN
UICS9DB833A
PCIE_MPCIE_R_CLKP
PCIE_MPCIE_R_CLKN
PCIE3_R_CLKP
PCIE3_R_CLKN
PCIE2_R_CLKP
PCIE2_R_CLKN
PCIE1_R_CLKP
PCIE1_R_CLKN
PCIE0_R_CLKP
PCIE0_R_CLKN
R100
R101
R106
R107
R104
R105
R102
R103
R98
R99
R1%33RS03
PCIE_MPCIE_CLKP 6
PCIE_MPCIE_CLKN 6
PCIE3_CLKP 5
PCIE3_CLKN 5
PCIE2_CLKP 5
PCIE2_CLKN 5
PCIE1_CLKP 5
PCIE1_CLKN 5
PCIE0_CLKP 6
PCIE0_CLKN 6
PCIE0_CLKP
PCIE0_CLKN
PCIE_MPCIE_CLKP
PCIE_MPCIE_CLKN
PCIE1_CLKP
PCIE1_CLKN
PCIE2_CLKP
PCIE2_CLKN
PCIE3_CLKP
PCIE3_CLKN
R108
R109
R110
R111
R113
R112
R115
R114
R117
R116
R1%49R9S03
determining SRC
output freq
0 = SRC/2
1 = SRC
R134
R1%10kS03
CLKGEN_SRC_DIV#
R135
R1%10kS03
NA
LOW ... Vin < 0.8V
MID ... 1.2V < Vin < 1.8V
HIGH ... Vin > 2V
LOW ... Bypass
MID ... PLL 100M Hi BW
HIGH ... PLL 100M Low BW
R137
R1%10kS03
CLKGEN_BYPASS#/PLL
R138
R1%10kS03
C118
C100nS03V50X
U15A
U15B
U15C
U15D
U74LCX125
PCIE_CON_RST# 5,6,10
LPC_RST# 16
POST_RST# 15
SIO_RST# 15
3 PCIE_RST#
R140
R1%10kS03
R141
R142
R144
R143
R1%10kS03
R118
R1%4k7S03
R119
R1%4k7S03
3,18 SMB_CLK
3,18 SMB_DAT
T6A
TNTJD4001NG-OSS
T6B
TNTJD4001NG-OSS
SMB_CLK_S0
SMB_DAT_S0
SMB_CLK_S0 13
SMB_DAT_S0 13
SMB / GP1_I2C
R122
R123
NA
R5%0R0S03
R120
R121
SMB_CLK
SMB_DAT
SW4
MDIPSW4
SMB_CLK_R
SMB_DAT_R
R191
R192
R245
R267
R286
R287
R1%100kS03
SMB_CLK_CLKGEN
SMB_DAT_CLKGEN
SMB_CLK_PCIE 5,6
SMB_DAT_PCIE 5,6
+V3.3A
SW4 - disconnecting SMBus devices from I2C bus if not compatible
<Core Design>
Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany
congatec
the rhythm of embedded computing
Title
PCIe gen 3 Clock Buffer
Size
A3
Document Number
QEV2
Created
LIKR
Rev
B.3
Date:
Monday, November 03, 2014
Sheet
4
of
22

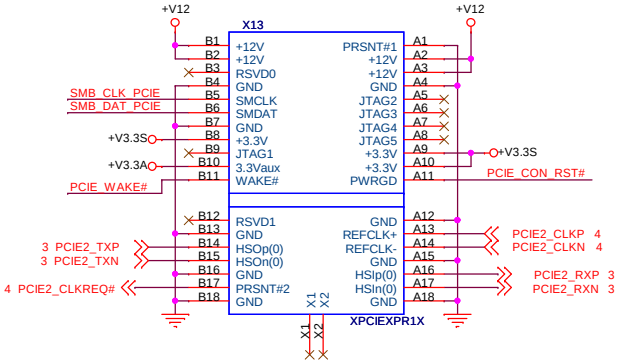
PCIe Lane 1



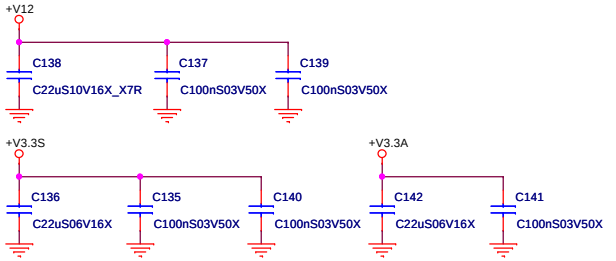


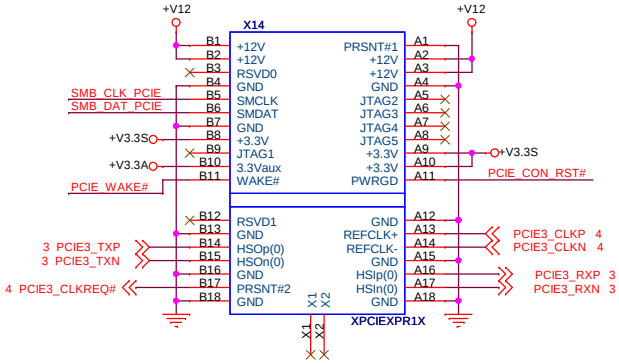
PCIe Lane 2



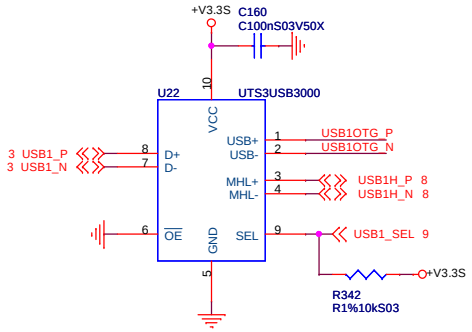


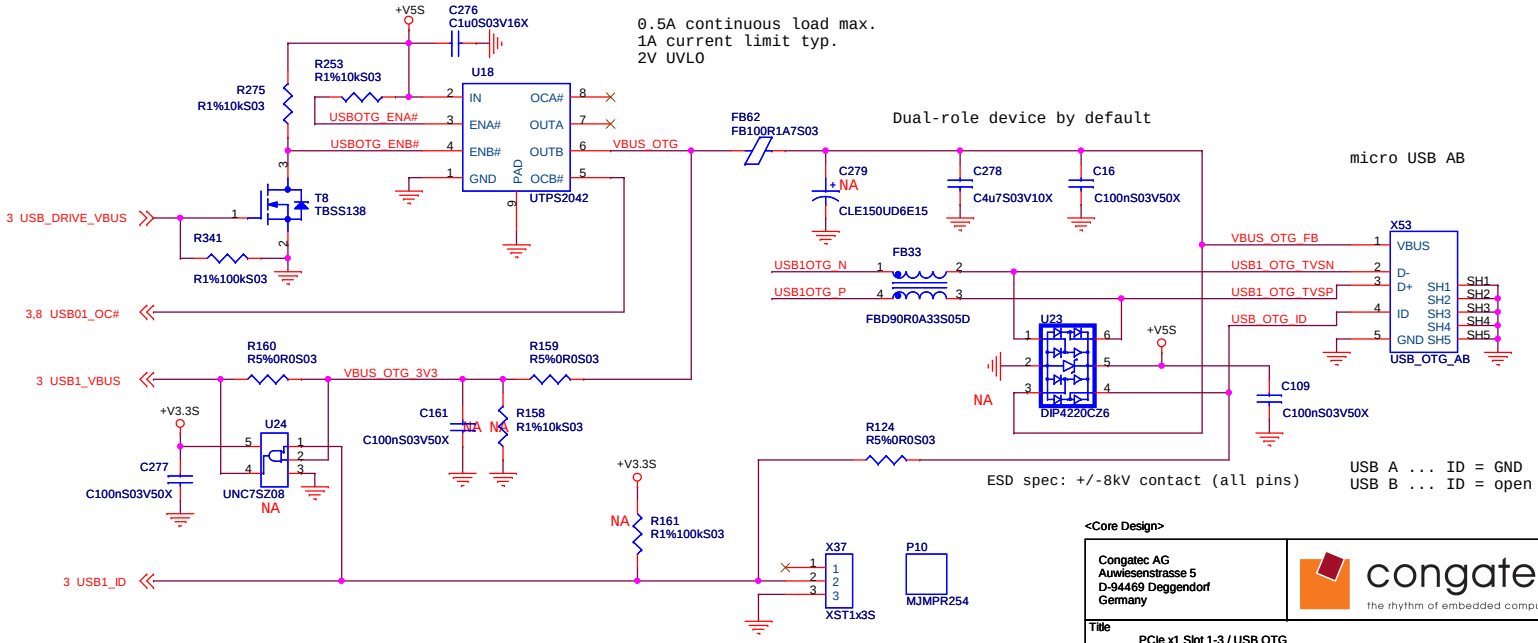
PCIe Lane 3





USB OTG





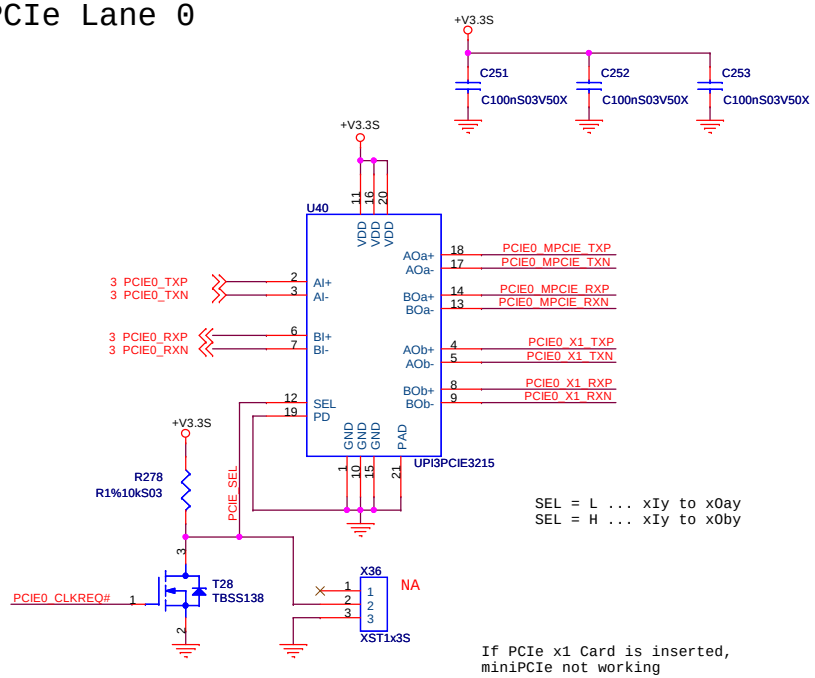
<Core Design>

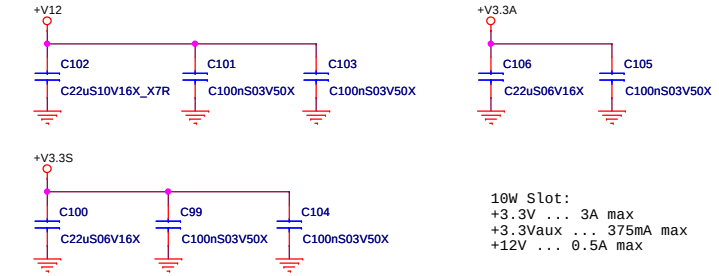
Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

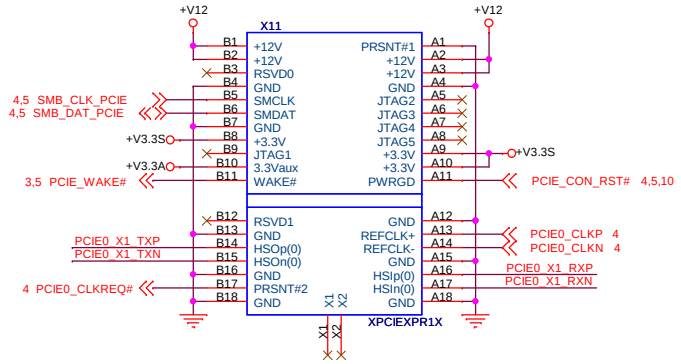
congatec
the rhythm of embedded computing

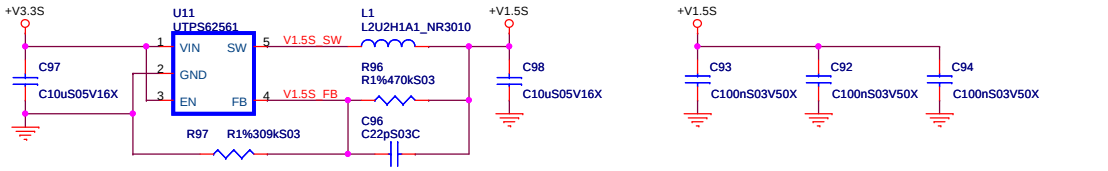
Title	PCIe x1 Slot 1-3 / USB OTG		
Size A3	Document Number QEV2	Created LIKR	Rev B.3
Date: Monday, November 03, 2014	Sheet 5 of 22		

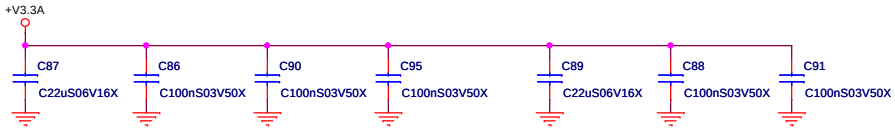
PCIe Lane 0

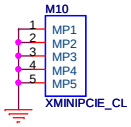


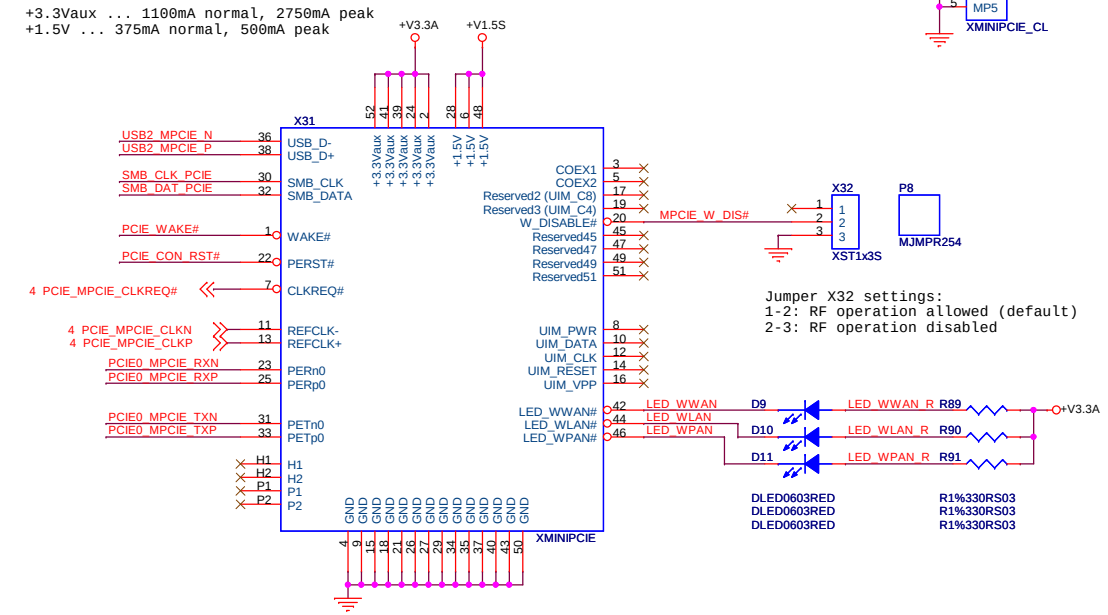


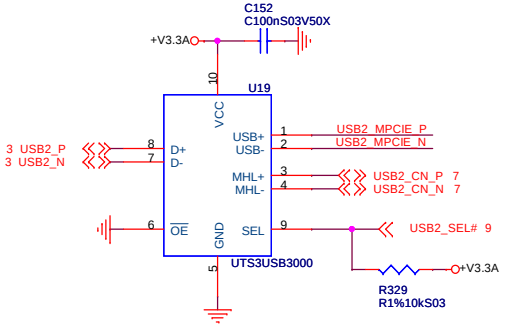










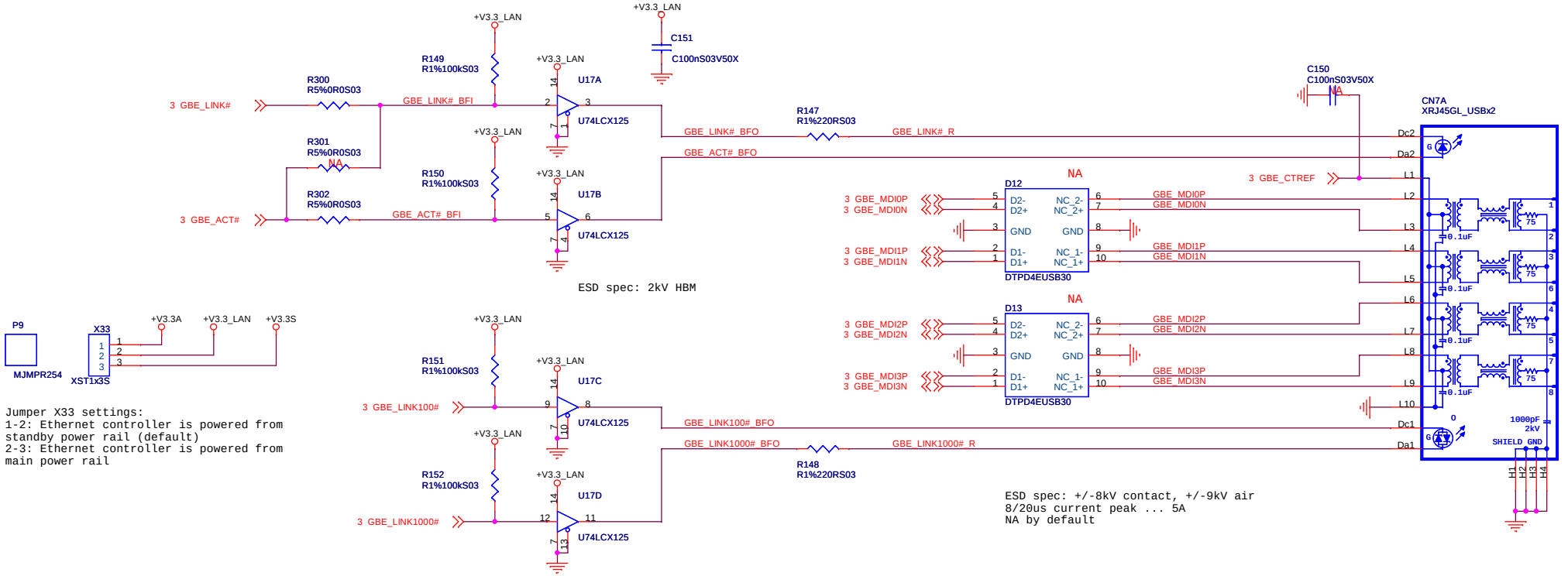


<Core Design>
Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

congatec
the rhythm of embedded computing

Title: PCIe x1 Slot 0 / miniPCIe			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 6 of 22		

Gigabit Ethernet (RJ45)

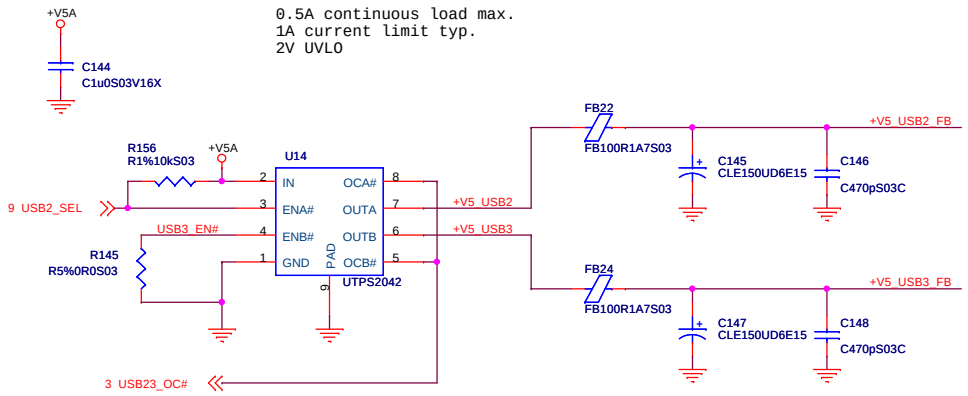


ESD spec: 2kV HBM

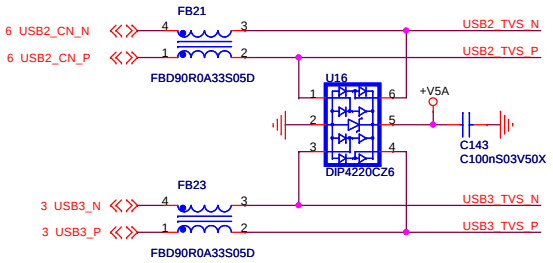
Jumper X33 settings:
1-2: Ethernet controller is powered from standby power rail (default)
2-3: Ethernet controller is powered from main power rail

ESD spec: +/-8kV contact, +/-9kV air
8/20us current peak ... 5A
NA by default

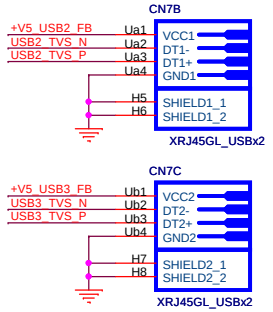
USB 2.0 with Wake On USB



0.5A continuous load max.
1A current limit typ.
2V UVLO



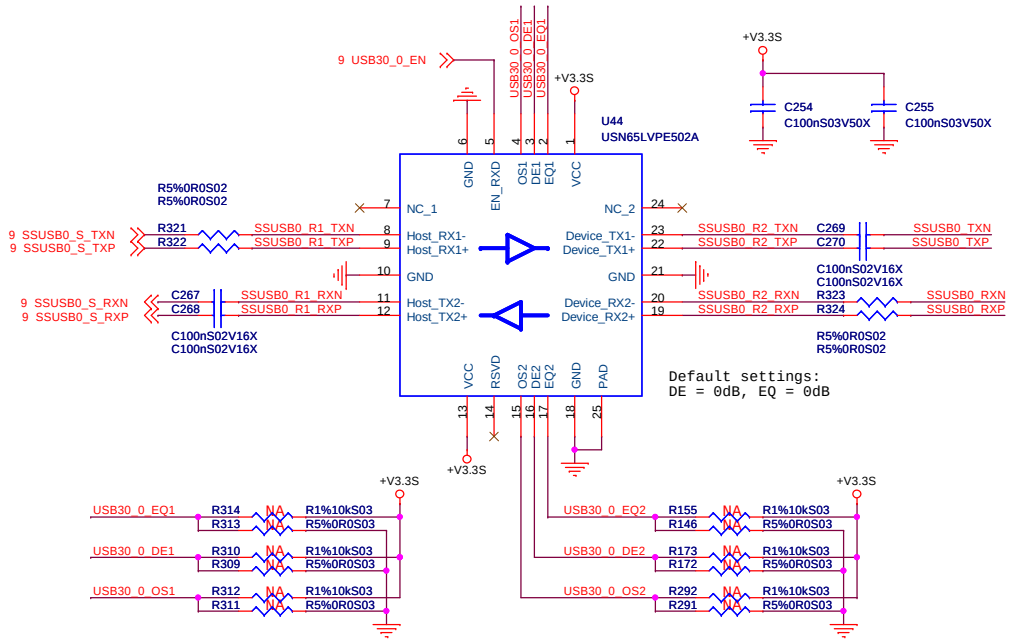
ESD spec: +/-8kV contact (all pins)

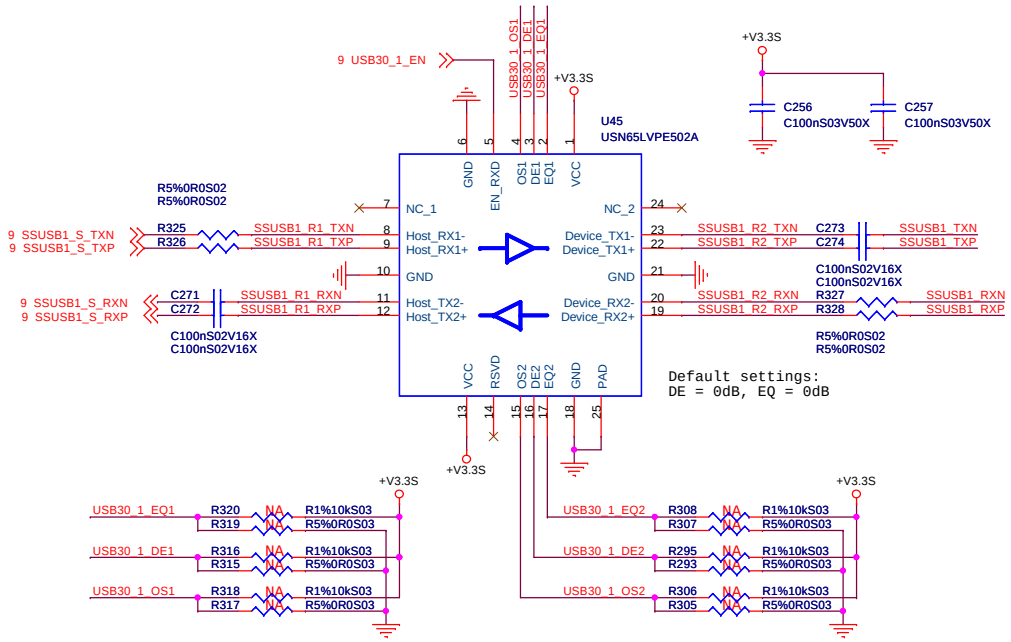


<Core Design>

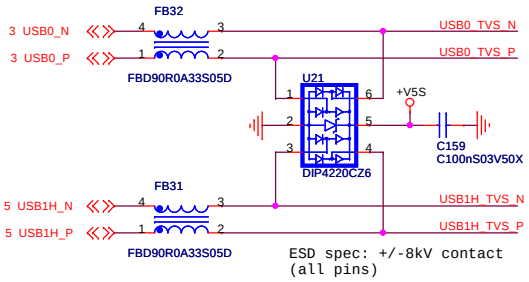
Congatec AG Auwiesenstrasse 5 D-94469 Deggendorf Germany			
Title: Ethernet / 2x USB 2.0			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 7 of 22		

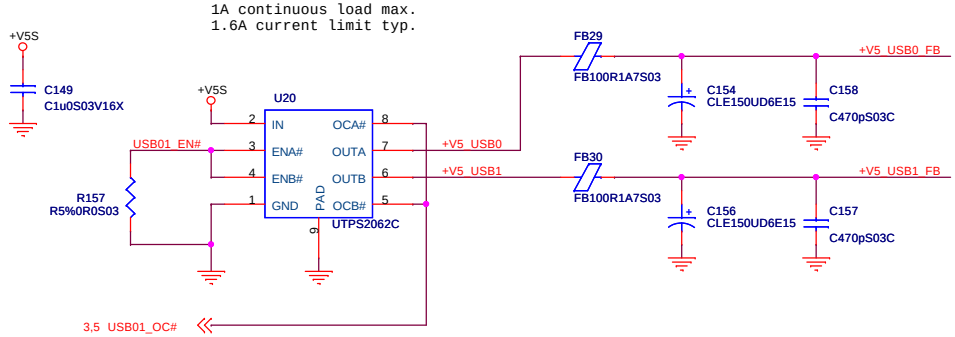
USB ReDriver

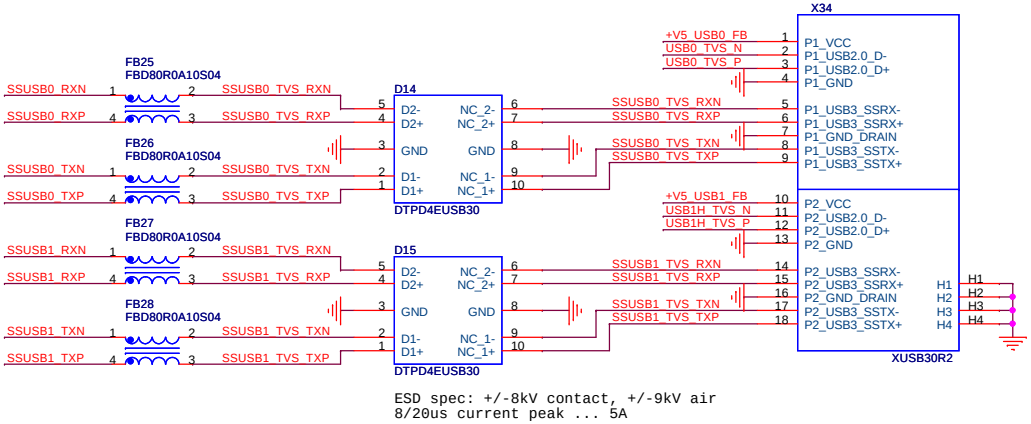




USB 3.0







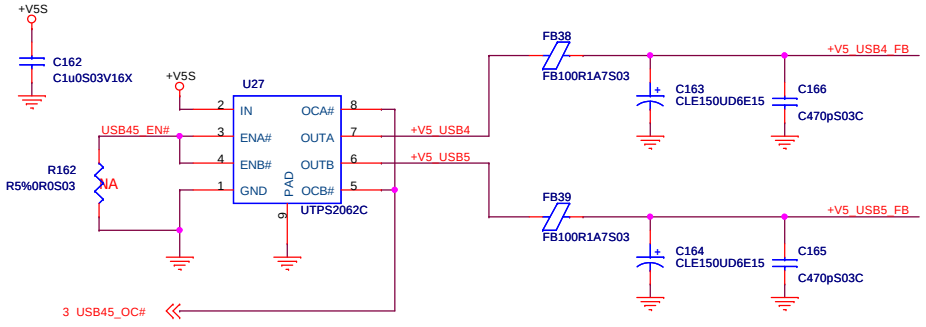
<Core Design>

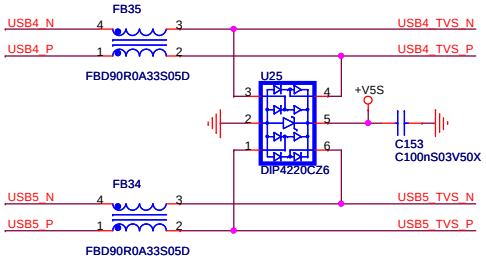
Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

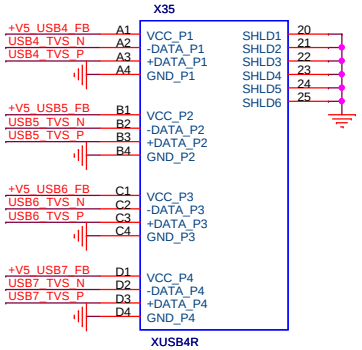
congatec
the rhythm of embedded computing

Title: USB ReDriver / 2x USB 3.0			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 8 of 22		

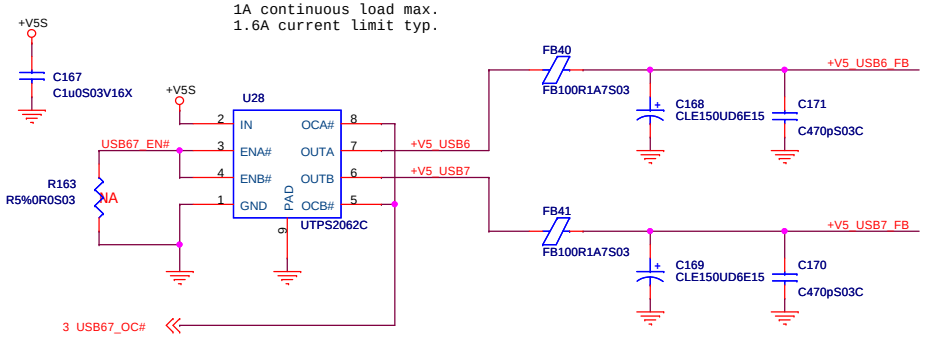
USB 2.0

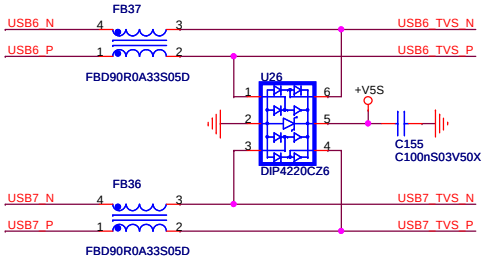






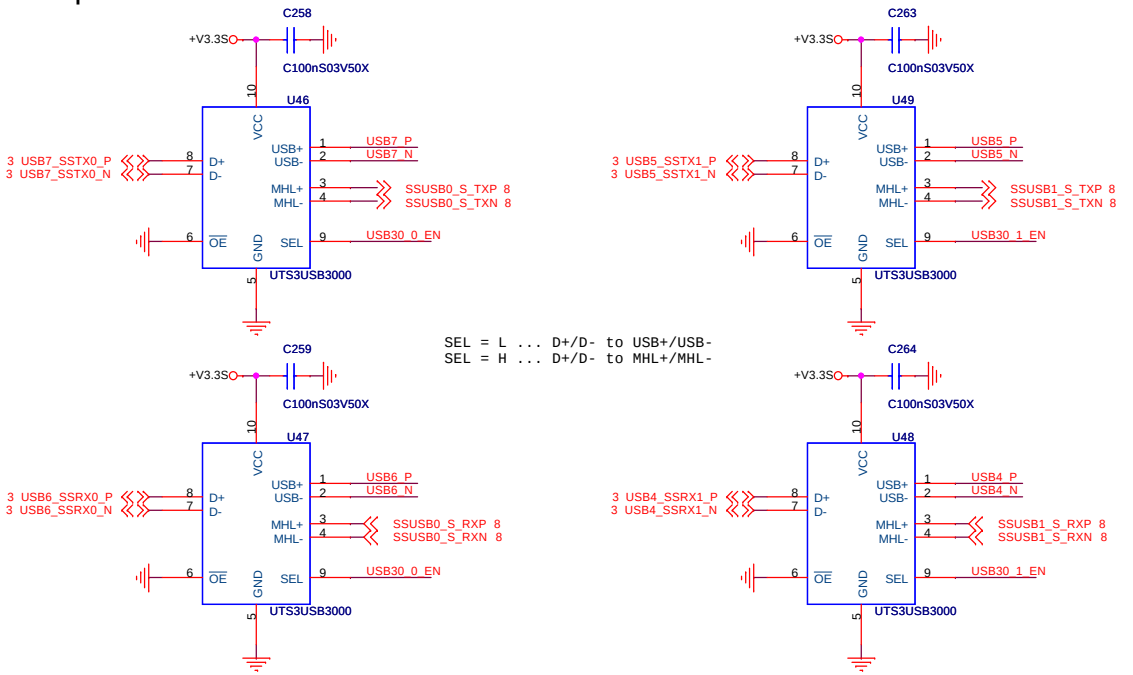
1A continuous load max.
1.6A current limit typ.



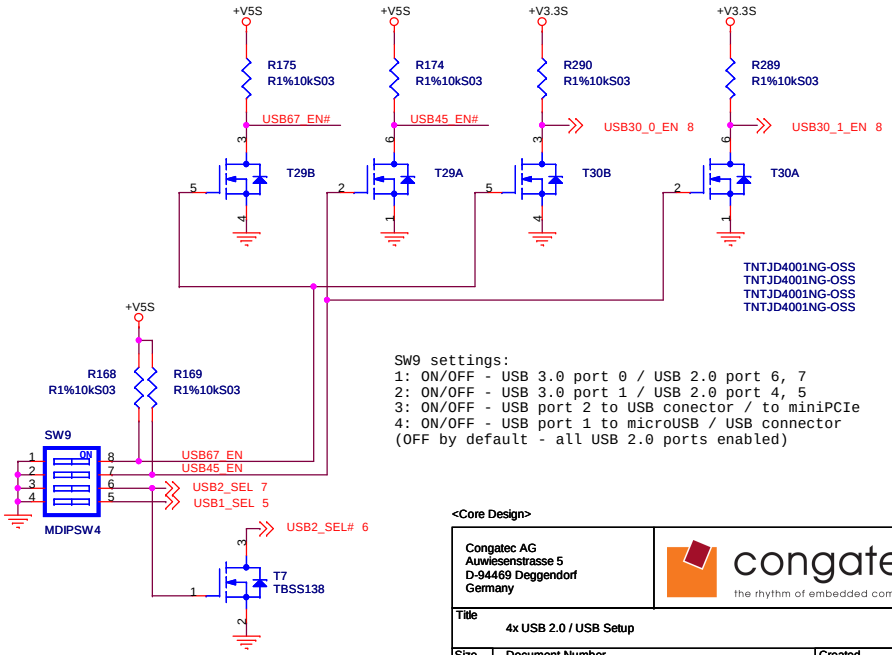


ESD spec: +/-8kV contact (all pins)

USB setup



SEL = L ... D+/D- to USB+/USB-
SEL = H ... D+/D- to MHL+/MHL-



SW9 settings:
1: ON/OFF - USB 3.0 port 0 / USB 2.0 port 6, 7
2: ON/OFF - USB 3.0 port 1 / USB 2.0 port 4, 5
3: ON/OFF - USB port 2 to USB conector / to miniPCIe
4: ON/OFF - USB port 1 to microUSB / USB connector
(OFF by default - all USB 2.0 ports enabled)

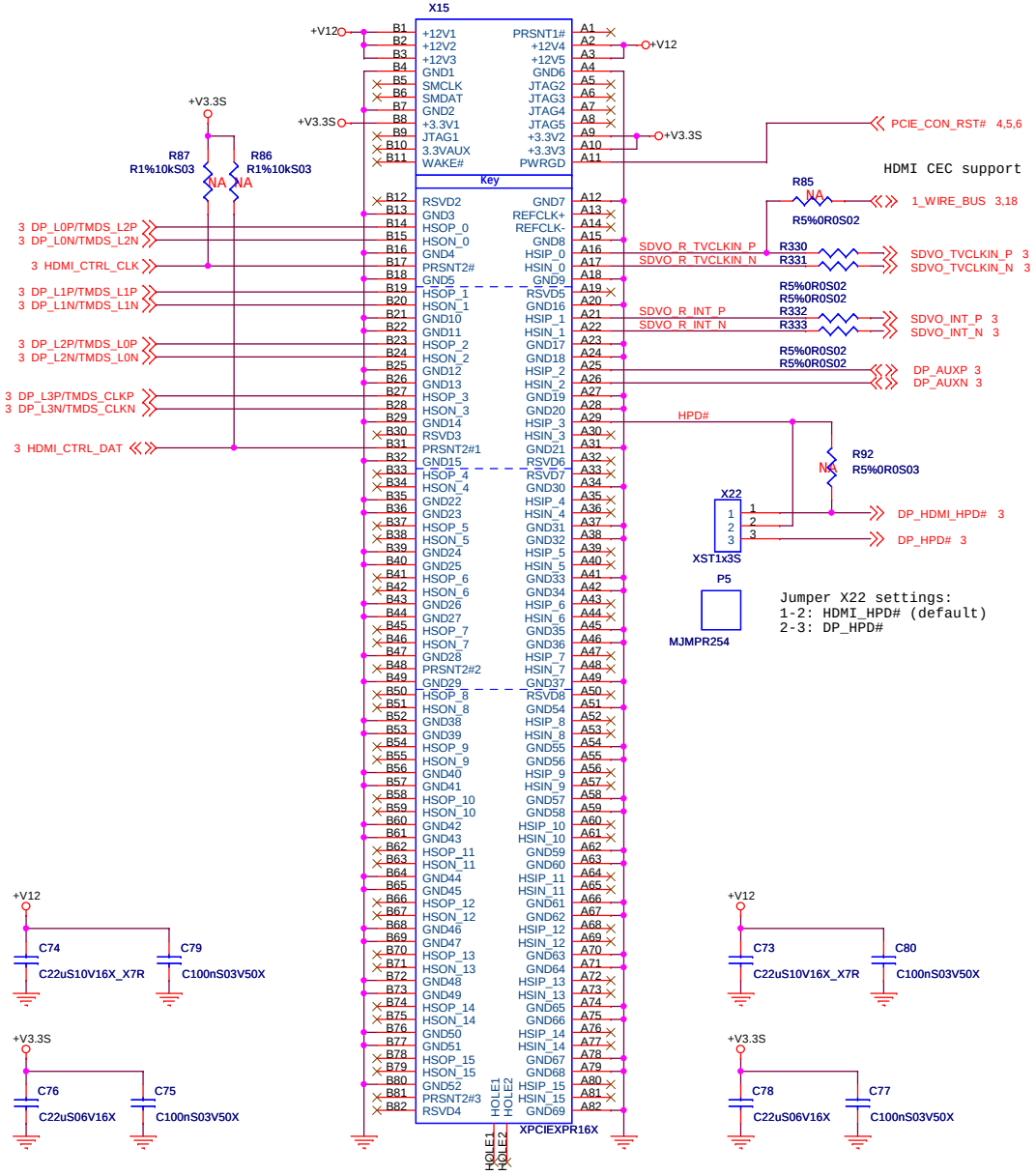
<Core Design>

Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

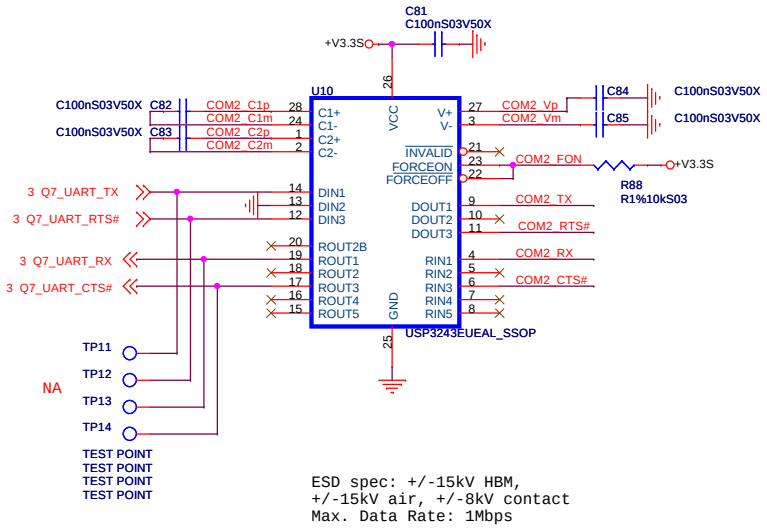
congatec
the rhythm of embedded computing

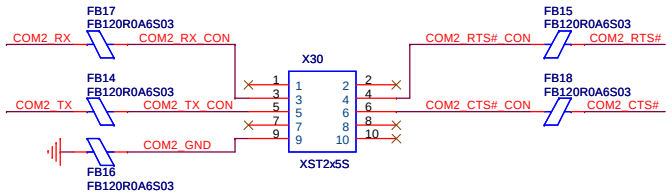
Title: 4x USB 2.0 / USB Setup			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 9 of 22		

PCIe x16 for Graphic Card Adapter (MGCA, HGCA)



Serial port from Qseven module (COM2)



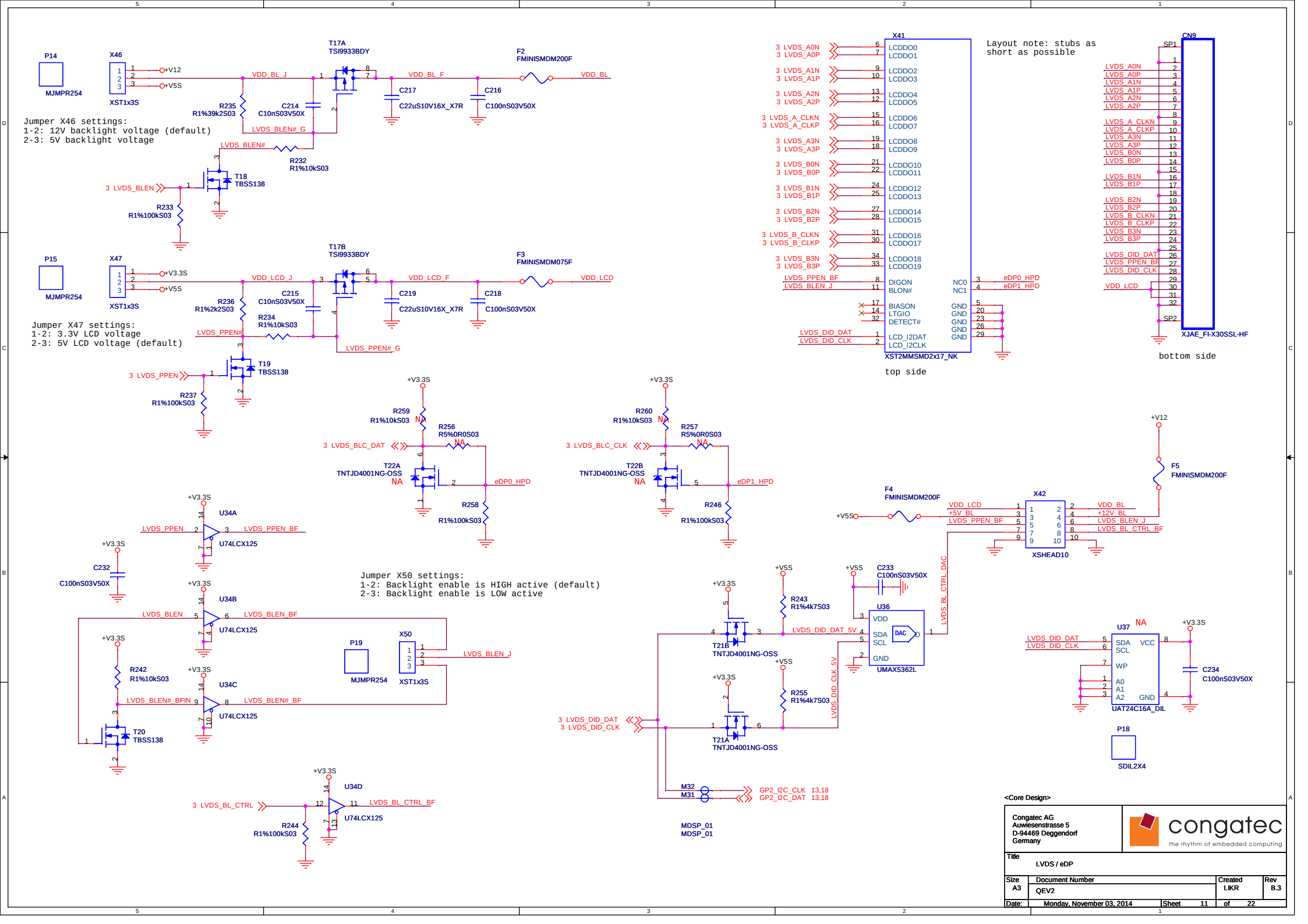


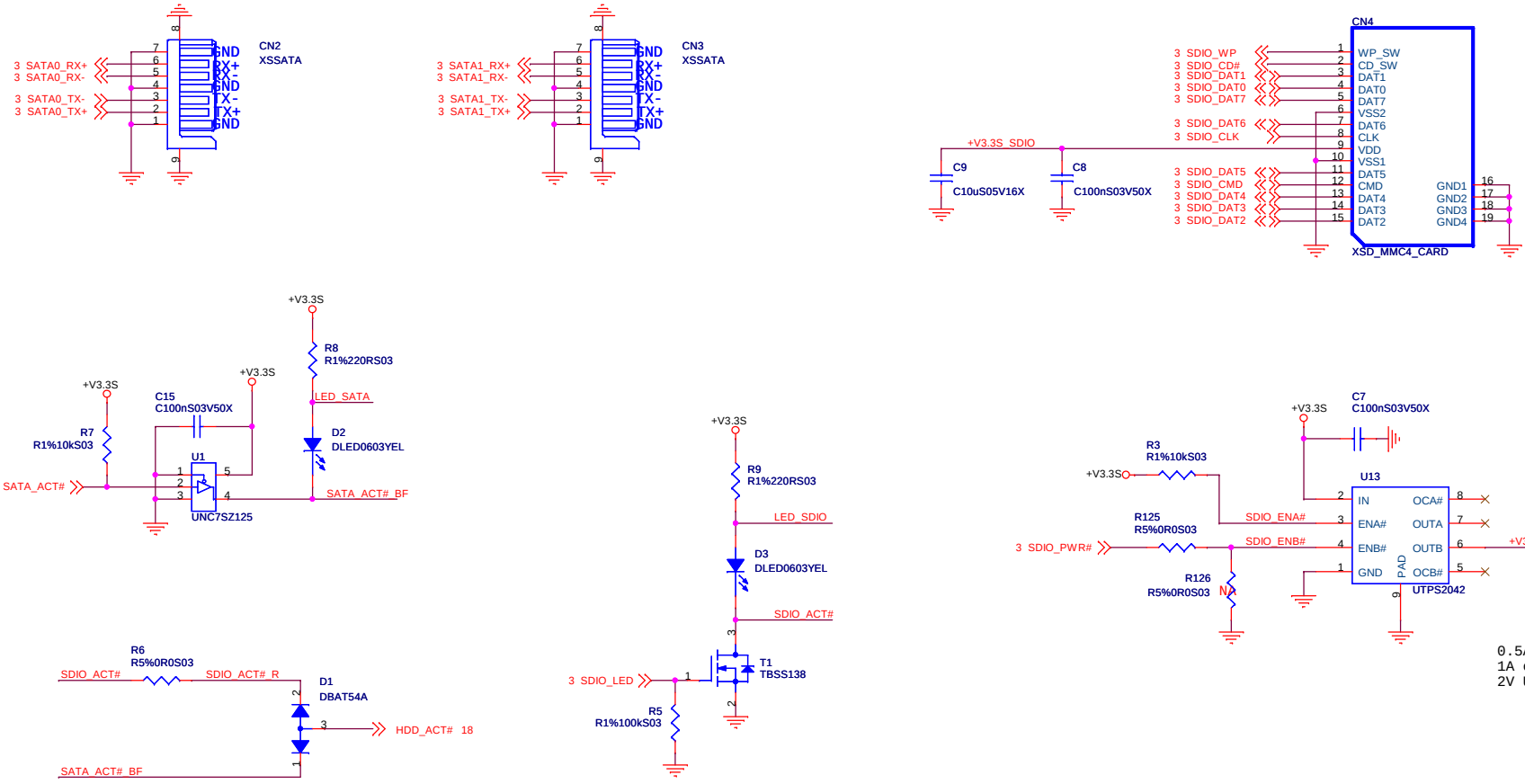
<Core Design>

Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

congatec
the rhythm of embedded computing

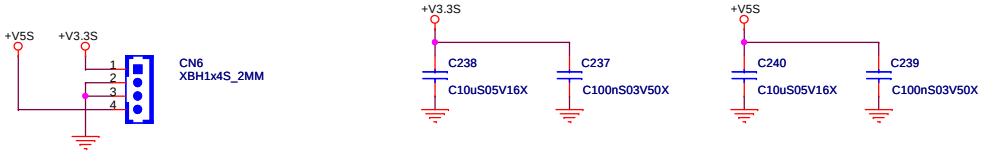
Title: PCIe x16 for GCA / COM 2			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 10 of 22		


P14
MJMPR254
X46
XST1x3S
+V12
+V5S
T17A
TSI9933BDY
VDD_BL_J
VDD_BL_F
F2
FMINISMDM200F
VDD_BL
C217
C22uS10V16X_X7R
C216
C100nS03V50X
R235
R1%39k2S03
C214
C10nS03V50X
LVDS_BLEN#_G
LVDS_BLEN#
R232
R1%10kS03
T18
TBSS138
3 LVDS_BLEN
R233
R1%100kS03
Jumper X46 settings:
1-2: 12V backlight voltage (default)
2-3: 5V backlight voltage
P15
MJMPR254
X47
XST1x3S
+V3.3S
+V5S
T17B
TSI9933BDY
VDD_LCD_J
VDD_LCD_F
F3
FMINISMDM075F
VDD_LCD
C219
C22uS10V16X_X7R
C218
C100nS03V50X
R236
R1%2k2S03
C215
C10nS03V50X
R234
R1%10kS03
LVDS_PPEN#
LVDS_PPEN#_G
T19
TBSS138
3 LVDS_PPEN
R237
R1%100kS03
Jumper X47 settings:
1-2: 3.3V LCD voltage
2-3: 5V LCD voltage (default)
X41
LCDDO0
LCDDO1
LCDDO2
LCDDO3
LCDDO4
LCDDO5
LCDDO6
LCDDO7
LCDDO8
LCDDO9
LCDDO10
LCDDO11
LCDDO12
LCDDO13
LCDDO14
LCDDO15
LCDDO16
LCDDO17
LCDDO18
LCDDO19
DIGON
BLON#
BIASON
LTGIO
DETECT#
LCD_I2DAT
LCD_I2CLK
NC0
NC1
GND
3 LVDS_A0N
3 LVDS_A0P
3 LVDS_A1N
3 LVDS_A1P
3 LVDS_A2N
3 LVDS_A2P
3 LVDS_A_CLKN
3 LVDS_A_CLKP
3 LVDS_A3N
3 LVDS_A3P
3 LVDS_B0N
3 LVDS_B0P
3 LVDS_B1N
3 LVDS_B1P
3 LVDS_B2N
3 LVDS_B2P
3 LVDS_B_CLKN
3 LVDS_B_CLKP
3 LVDS_B3N
3 LVDS_B3P
LVDS_PPEN_BF
LVDS_BLEN_J
LVDS_DID_DAT
LVDS_DID_CLK
eDP0_HPD
eDP1_HPD
XST2MMSMD2x17_NK
top side
Layout note: stubs as short as possible
CN9
SP1
SP2
LVDS_A0N
LVDS_A0P
LVDS_A1N
LVDS_A1P
LVDS_A2N
LVDS_A2P
LVDS_A_CLKN
LVDS_A_CLKP
LVDS_A3N
LVDS_A3P
LVDS_B0N
LVDS_B0P
LVDS_B1N
LVDS_B1P
LVDS_B2N
LVDS_B2P
LVDS_B_CLKN
LVDS_B_CLKP
LVDS_B3N
LVDS_B3P
LVDS_DID_DAT
LVDS_PPEN_BF
LVDS_DID_CLK
VDD_LCD
XJAE_FI-X30SSL-HF
bottom side
T22A
TNTJD4001NG-OSS
NA
3 LVDS_BLC_DAT
R259
R1%10kS03
R256
R5%0R0S03
R258
R1%100kS03
T22B
3 LVDS_BLC_CLK
R260
R257
R246
U34A
U74LCX125
LVDS_PPEN
LVDS_PPEN_BF
C232
C100nS03V50X
U34B
LVDS_BLEN
LVDS_BLEN_BF
U34C
LVDS_BLEN#_BFIN
LVDS_BLEN#_BF
R242
R1%10kS03
T20
TBSS138
P19
MJMPR254
X50
XST1x3S
LVDS_BLEN_J
Jumper X50 settings:
1-2: Backlight enable is HIGH active (default)
2-3: Backlight enable is LOW active
U34D
3 LVDS_BL_CTRL
LVDS_BL_CTRL_BF
R244
R1%100kS03
F4
FMINISMDM200F
F5
FMINISMDM200F
X42
XSHEAD10
VDD_LCD
+5V_BL
LVDS_PPEN_BF
VDD_BL
+12V_BL
LVDS_BLEN_J
LVDS_BL_CTRL_BF
T21B
TNTJD4001NG-OSS
T21A
R243
R1%4k7S03
R255
R1%4k7S03
LVDS_DID_DAT_5V
LVDS_DID_CLK_5V
LVDS_BL_CTRL_DAC
C233
C100nS03V50X
U36
VDD
SDA
SCL
GND
DAC
UMAX5362L
3 LVDS_DID_DAT
3 LVDS_DID_CLK
M32
M31
GP2_I2C_CLK 13,18
GP2_I2C_DAT 13,18
MDSP_01
MDSP_01
U37
NA
WP
A0
A1
A2
VCC
UAT24C16A_DIL
C234
C100nS03V50X
P18
SDIL2X4
<Core Design>
Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany
congatec
the rhythm of embedded computing
Title
LVDS / eDP
Size
A3
Document Number
QEV2
Created
LIKR
Rev
B.3
Date:
Monday, November 03, 2014
Sheet
11
of
22



0.5A continuous load max.
1A current limit typ.
2V UVLO

SATA Aux Power



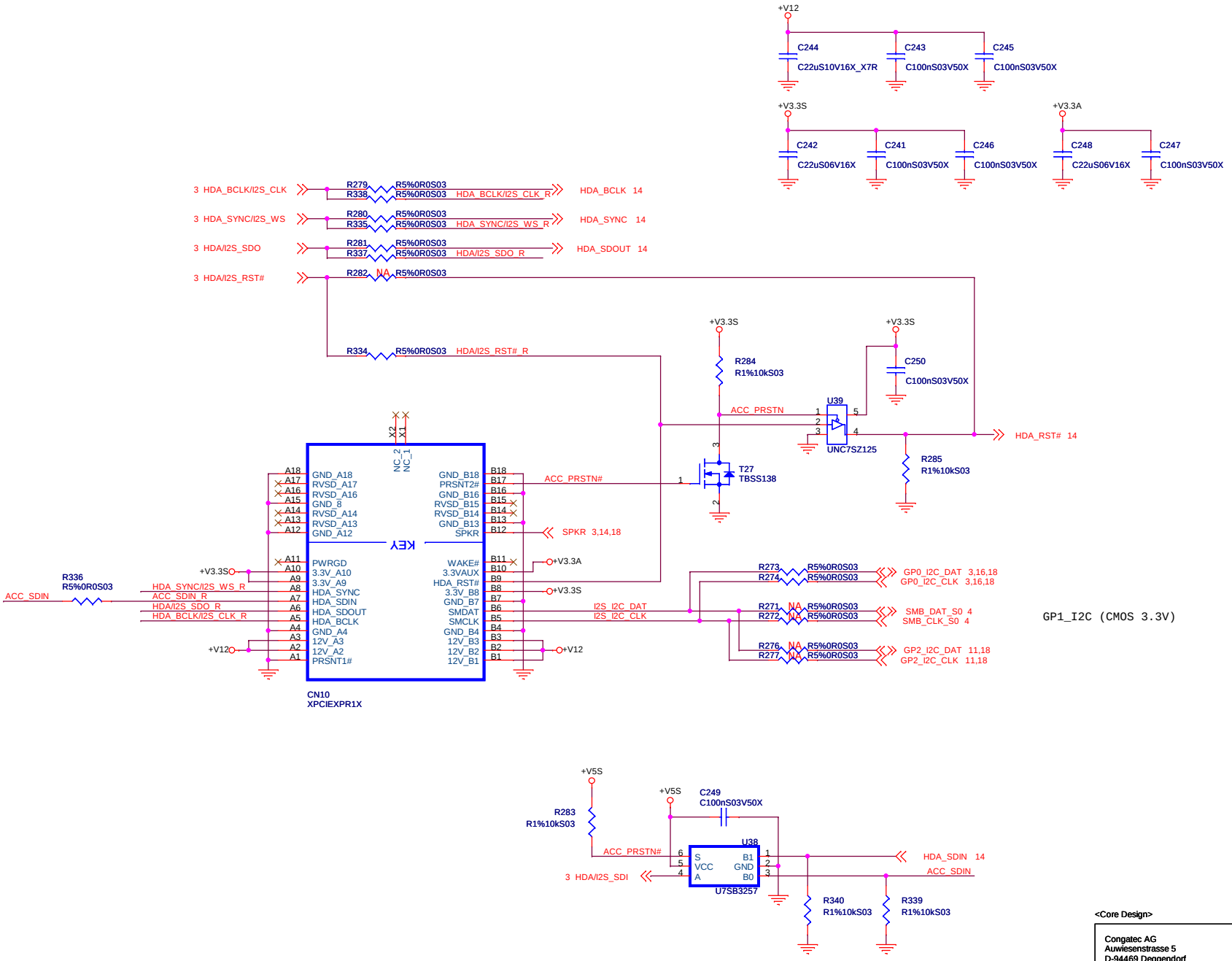
cable Item# 14000032
2.5" HDD only

<Core Design>

Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

congatec
the rhythm of embedded computing

Title: SATA / SDIO			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 12 of 22		



<Core Design>

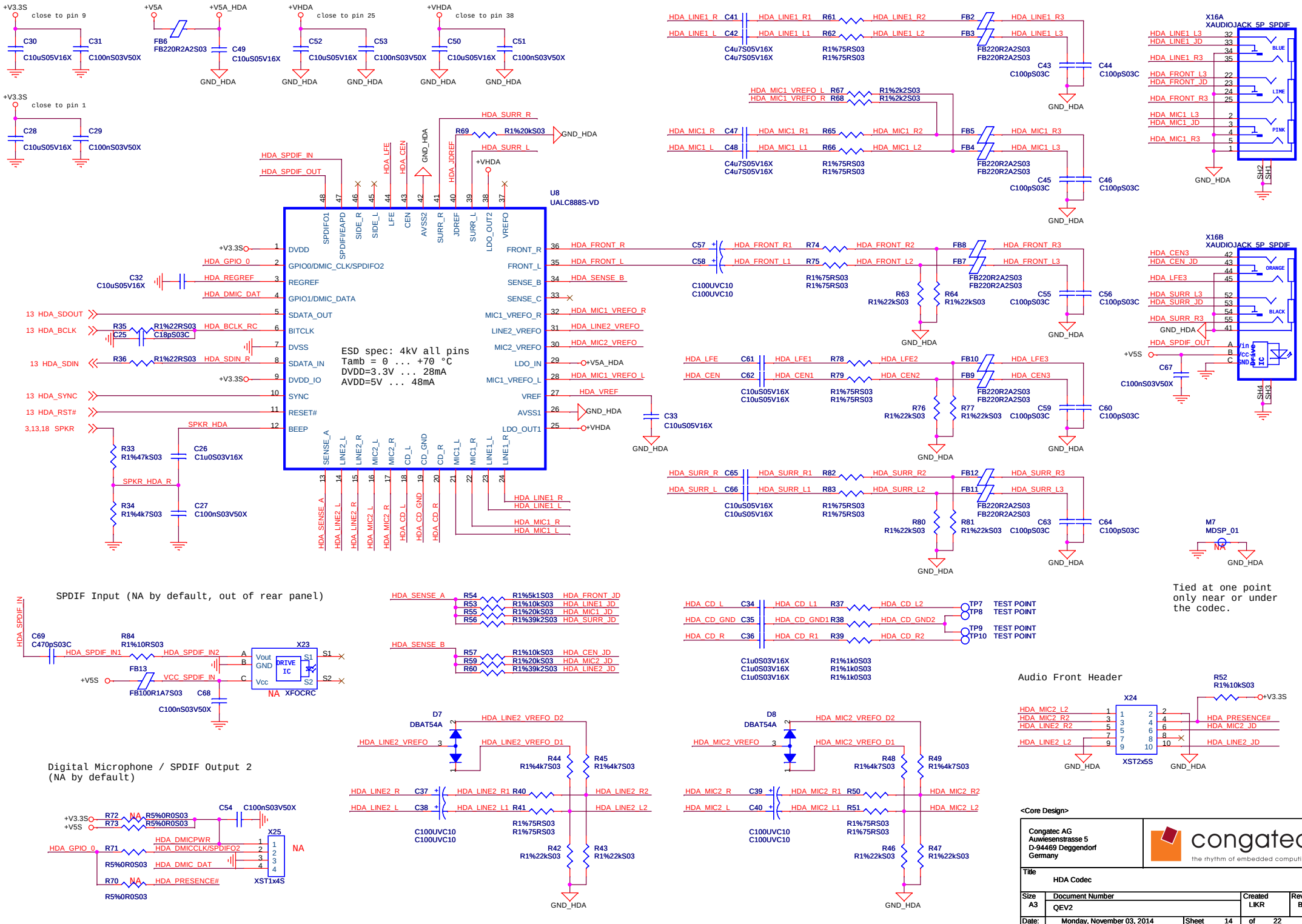
Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

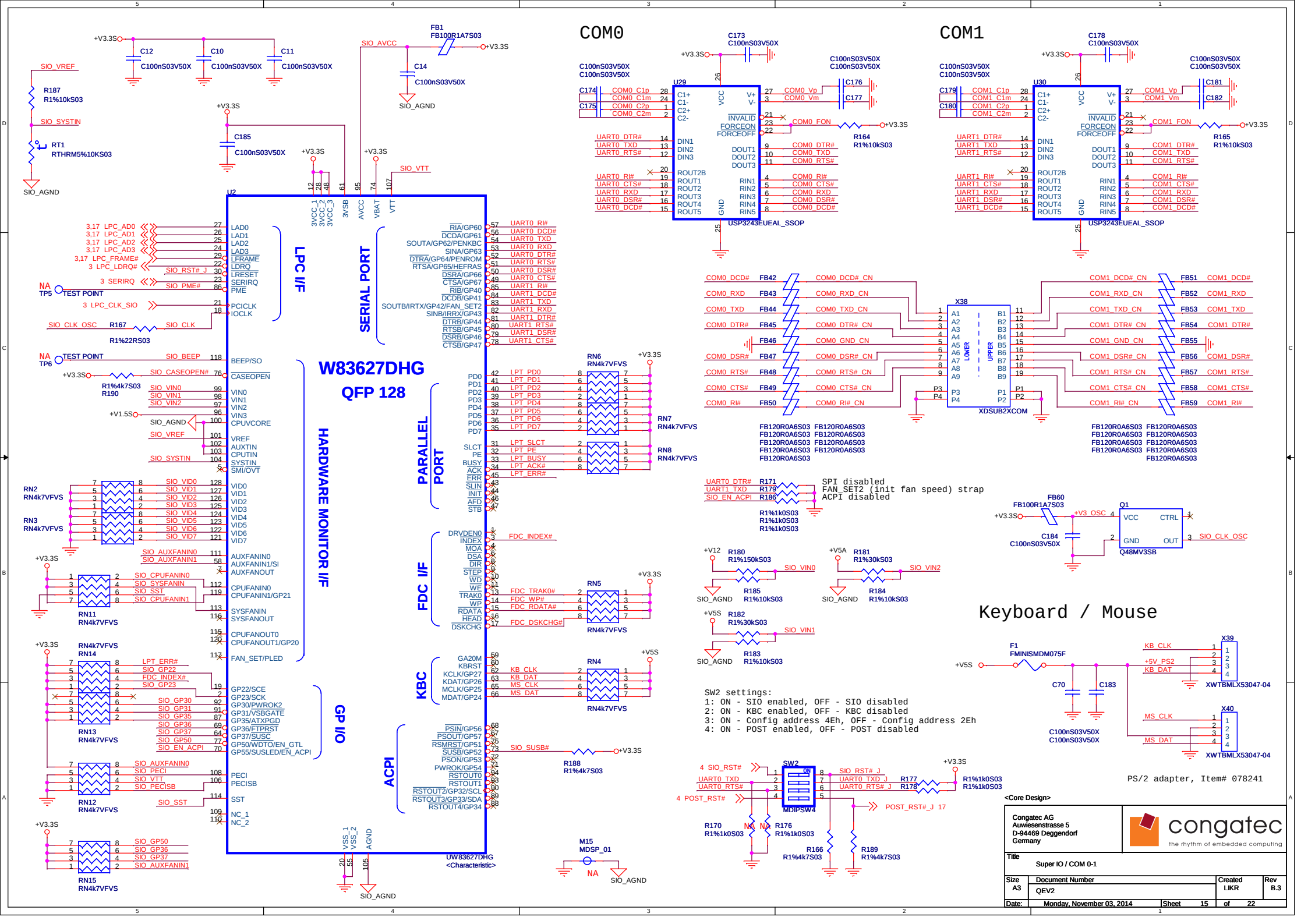
congatec
the rhythm of embedded computing

Title: Audio Codec Card Slot

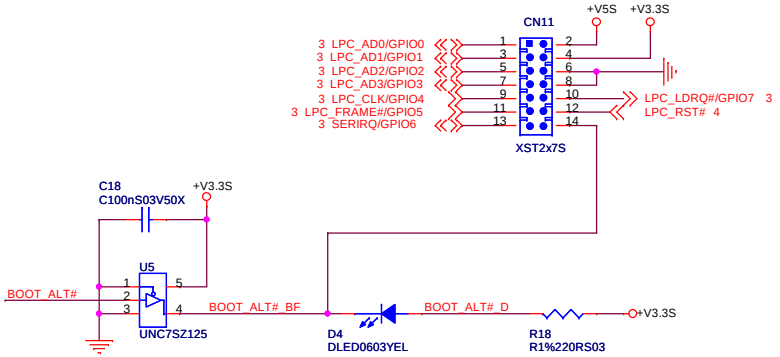
Size	Document Number	Created	Rev
A3	QEV2	LIKR	B.3

Date: Monday, November 03, 2014 Sheet 13 of 22

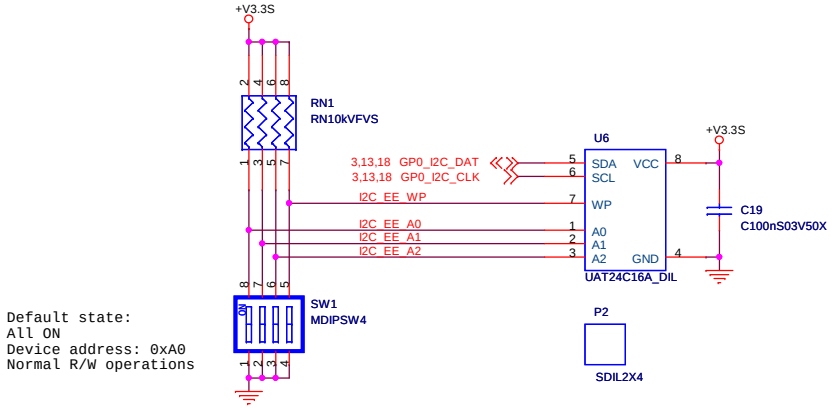

+V3.3S close to pin 9
C30 C10uS05V16X
C31 C100nS03V50X
+V5A
+V5A_HDA
FB6 FB220R2A2S03
C49 C10uS05V16X
GND_HDA
+VHDA close to pin 25
C52 C10uS05V16X
C53 C100nS03V50X
+VHDA close to pin 38
C50 C10uS05V16X
C51 C100nS03V50X
+V3.3S close to pin 1
C28 C10uS05V16X
C29 C100nS03V50X
U8
UALC888S-VD
HDA_SURR_R
HDA_SURR_L
R69 R1%20kS03
HDA_SPDIF_IN
HDA_SPDIF_OUT
HDA_LFE
HDA_CEN
HDA_JDREF
SPDIFO1
SPDIF/EAPD
SIDE_R
SIDE_L
LFE
CEN
AVSS2
SURR_R
JDREF
SURR_L
LDO_OUT2
VREFO
DVDD
GPIO0/DMIC_CLK/SPDIFO2
REGREF
GPIO1/DMIC_DATA
SDATA_OUT
BITCLK
DVSS
SDATA_IN
DVDD_IO
SYNC
RESET#
BEEP
FRONT_R
FRONT_L
SENSE_B
SENSE_C
MIC1_VREFO_R
LINE2_VREFO
MIC2_VREFO
LDO_IN
MIC1_VREFO_L
VREF
AVSS1
LDO_OUT1
C32 C10uS05V16X
HDA_GPIO_0
HDA_REGREF
HDA_DMIC_DAT
13 HDA_SDOUT
13 HDA_BCLK
R35 R1%22RS03
C25 C18pS03C
HDA_BCLK_RC
13 HDA_SDIN
R36 R1%22RS03
HDA_SDIN_R
13 HDA_SYNC
13 HDA_RST#
3,13,18 SPKR
R33 R1%47kS03
C26 C1u0S03V16X
SPKR_HDA
SPKR_HDA_R
R34 R1%4k7S03
C27 C100nS03V50X
ESD spec: 4kV all pins
Tamb = 0 ... +70 °C
DVDD=3.3V ... 28mA
AVDD=5V ... 48mA
C33 C10uS05V16X
HDA_FRONT_R
HDA_FRONT_L
HDA_SENSE_B
HDA_MIC1_VREFO_R
HDA_LINE2_VREFO
HDA_MIC2_VREFO
+V5A_HDA
HDA_MIC1_VREFO_L
HDA_VREF
+VHDA
HDA_SENSE_A
HDA_LINE2_L
HDA_LINE2_R
HDA_MIC2_L
HDA_MIC2_R
HDA_CD_L
HDA_CD_GND
HDA_CD_R
HDA_LINE1_R
HDA_LINE1_L
HDA_MIC1_R
HDA_MIC1_L
HDA_LINE1_R C41
HDA_LINE1_L C42
C4u7S05V16X
HDA_LINE1_R1 R61 R1%75RS03
HDA_LINE1_L1 R62 R1%75RS03
HDA_LINE1_R2
HDA_LINE1_L2
FB2 FB220R2A2S03
FB3 FB220R2A2S03
HDA_LINE1_R3
HDA_LINE1_L3
C43 C100pS03C
C44 C100pS03C
HDA_MIC1_VREFO_L R67 R1%2k2S03
HDA_MIC1_VREFO_R R68 R1%2k2S03
HDA_MIC1_R C47
HDA_MIC1_L C48
HDA_MIC1_R1 R65
HDA_MIC1_L1 R66
HDA_MIC1_R2
HDA_MIC1_L2
FB5 FB220R2A2S03
FB4 FB220R2A2S03
HDA_MIC1_R3
HDA_MIC1_L3
C45 C100pS03C
C46 C100pS03C
X16A
XAUDIOJACK_5P_SPDIF
HDA_LINE1_L3
HDA_LINE1_JD
HDA_LINE1_R3
HDA_FRONT_L3
HDA_FRONT_JD
HDA_FRONT_R3
HDA_MIC1_L3
HDA_MIC1_JD
HDA_MIC1_R3
BLUE
LINE
PINK
FH2
FH1
HDA_FRONT_R C57
HDA_FRONT_L C58
C100UVC10
HDA_FRONT_R1 R74 R1%75RS03
HDA_FRONT_L1 R75 R1%75RS03
HDA_FRONT_R2
HDA_FRONT_L2
FB8 FB220R2A2S03
FB7 FB220R2A2S03
HDA_FRONT_R3
HDA_FRONT_L3
R63 R1%22kS03
R64 R1%22kS03
C55 C100pS03C
C56 C100pS03C
X16B
XAUDIOJACK_5P_SPDIF
HDA_CEN3
HDA_CEN_JD
HDA_LFE3
HDA_SURR_L3
HDA_SURR_JD
HDA_SURR_R3
HDA_SPDIF_OUT
ORANGE
BLACK
Bi-Live IC
+V5S
C67 C100nS03V50X
FH4
FH3
HDA_LFE C61
HDA_CEN C62
C10uS05V16X
HDA_LFE1 R78 R1%75RS03
HDA_CEN1 R79 R1%75RS03
HDA_LFE2
HDA_CEN2
FB10 FB220R2A2S03
FB9 FB220R2A2S03
HDA_LFE3
HDA_CEN3
R76 R1%22kS03
R77 R1%22kS03
C59 C100pS03C
C60 C100pS03C
HDA_SURR_R C65
HDA_SURR_L C66
HDA_SURR_R1 R82 R1%75RS03
HDA_SURR_L1 R83 R1%75RS03
HDA_SURR_R2
HDA_SURR_L2
FB12 FB220R2A2S03
FB11 FB220R2A2S03
HDA_SURR_R3
HDA_SURR_L3
R80 R1%22kS03
R81 R1%22kS03
C63 C100pS03C
C64 C100pS03C
M7
MDSP_01
NA
Tied at one point only near or under the codec.
SPDIF Input (NA by default, out of rear panel)
HDA_SPDIF_IN
C69 C470pS03C
R84 R1%10RS03
HDA_SPDIF_IN1
HDA_SPDIF_IN2
FB13 FB100R1A7S03
VCC_SPDIF_IN
C68 C100nS03V50X
+V5S
X23
Vout
GND
Vcc
DRIVE IC
S1
S2
NA XFOCRC
HDA_SENSE_A
R54 R1%5k1S03 HDA_FRONT_JD
R53 R1%10kS03 HDA_LINE1_JD
R55 R1%20kS03 HDA_MIC1_JD
R56 R1%39k2S03 HDA_SURR_JD
HDA_SENSE_B
R57 R1%10kS03 HDA_CEN_JD
R59 R1%20kS03 HDA_MIC2_JD
R60 R1%39k2S03 HDA_LINE2_JD
HDA_CD_L C34
HDA_CD_GND C35
HDA_CD_R C36
C1u0S03V16X
HDA_CD_L1 R37 R1%1kS03
HDA_CD_GND1 R38 R1%1kS03
HDA_CD_R1 R39 R1%1kS03
HDA_CD_L2
HDA_CD_GND2
HDA_CD_R2
TP7 TEST POINT
TP8 TEST POINT
TP9 TEST POINT
TP10 TEST POINT
Audio Front Header
X24
HDA_MIC2_L2
HDA_MIC2_R2
HDA_LINE2_R2
HDA_LINE2_L2
HDA_PRESENCE#
HDA_MIC2_JD
HDA_LINE2_JD
R52 R1%10kS03
+V3.3S
XST2x5S
Digital Microphone / SPDIF Output 2
(NA by default)
+V3.3S
+V5S
R72 NA R5%0R0S03
R73 R5%0R0S03
C54 C100nS03V50X
HDA_GPIO_0
R71 R5%0R0S03
R70 NA R5%0R0S03
HDA_DMICPWR
HDA_DMICCLK/SPDIFO2
HDA_DMIC_DAT
HDA_PRESENCE#
X25
XST1x4S
NA
D7 DBAT54A
HDA_LINE2_VREFO
HDA_LINE2_VREFO_D2
HDA_LINE2_VREFO_D1
R44 R1%4k7S03
R45 R1%4k7S03
HDA_LINE2_R C37
HDA_LINE2_L C38
C100UVC10
HDA_LINE2_R1 R40 R1%75RS03
HDA_LINE2_L1 R41 R1%75RS03
HDA_LINE2_R2
HDA_LINE2_L2
R42 R1%22kS03
R43 R1%22kS03
D8 DBAT54A
HDA_MIC2_VREFO
HDA_MIC2_VREFO_D2
HDA_MIC2_VREFO_D1
R48 R1%4k7S03
R49 R1%4k7S03
HDA_MIC2_R C39
HDA_MIC2_L C40
C100UVC10
HDA_MIC2_R1 R50 R1%75RS03
HDA_MIC2_L1 R51 R1%75RS03
HDA_MIC2_R2
HDA_MIC2_L2
R46 R1%22kS03
R47 R1%22kS03
GND_HDA
<Core Design>
Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany
congatec
the rhythm of embedded computing
Title
HDA Codec
Size A3
Document Number QEV2
Created LIKR
Rev B.3
Date: Monday, November 03, 2014
Sheet 14 of 22


W83627DHG
QFP 128
HARDWARE MONITOR I/F
LPC I/F
SERIAL PORT
PARALLEL PORT
FDC I/F
KBC
GP I/O
ACPI
COM0
COM1
Keyboard / Mouse
SW2 settings:
1: ON - SIO enabled, OFF - SIO disabled
2: ON - KBC enabled, OFF - KBC disabled
3: ON - Config address 4Eh, OFF - Config address 2Eh
4: ON - POST enabled, OFF - POST disabled
SPI disabled
FAN_SET2 (init fan speed) strap
ACPI disabled
PS/2 adapter, Item# 078241
<Core Design>
Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany
Super IO / COM 0-1
QEV2
LIKR
B.3
Monday, November 03, 2014
15
22

LPC / GPIO

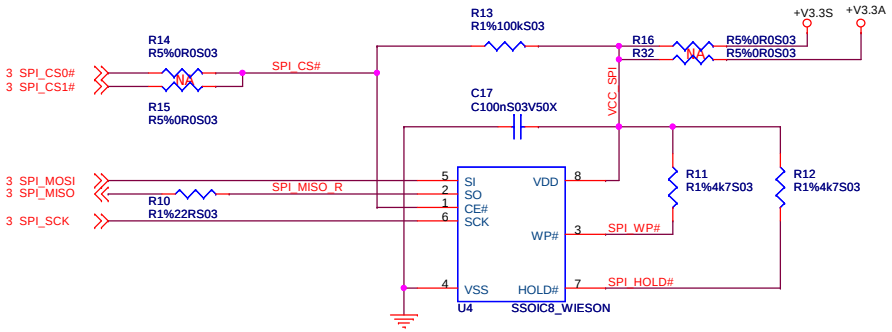


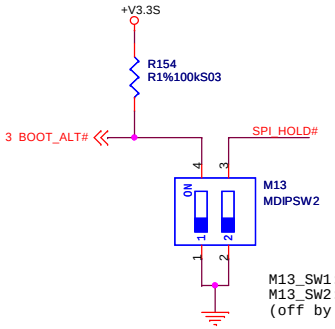
I2C EEPROM

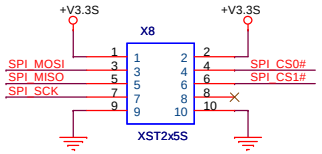


Default state:
All ON
Device address: 0xA0
Normal R/W operations

SPI socket (SOIC8) / SPI header

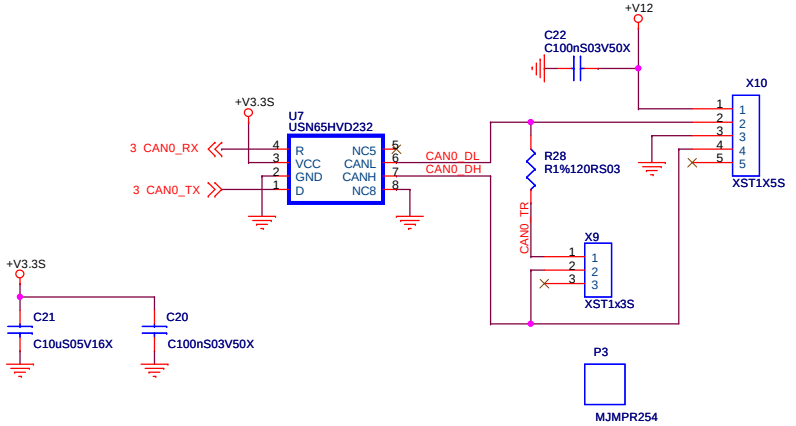






M13_SW1: Boot from OFF module BIOS flash
M13_SW2: On-board SPI Flash is hold (paused)
(off by default)

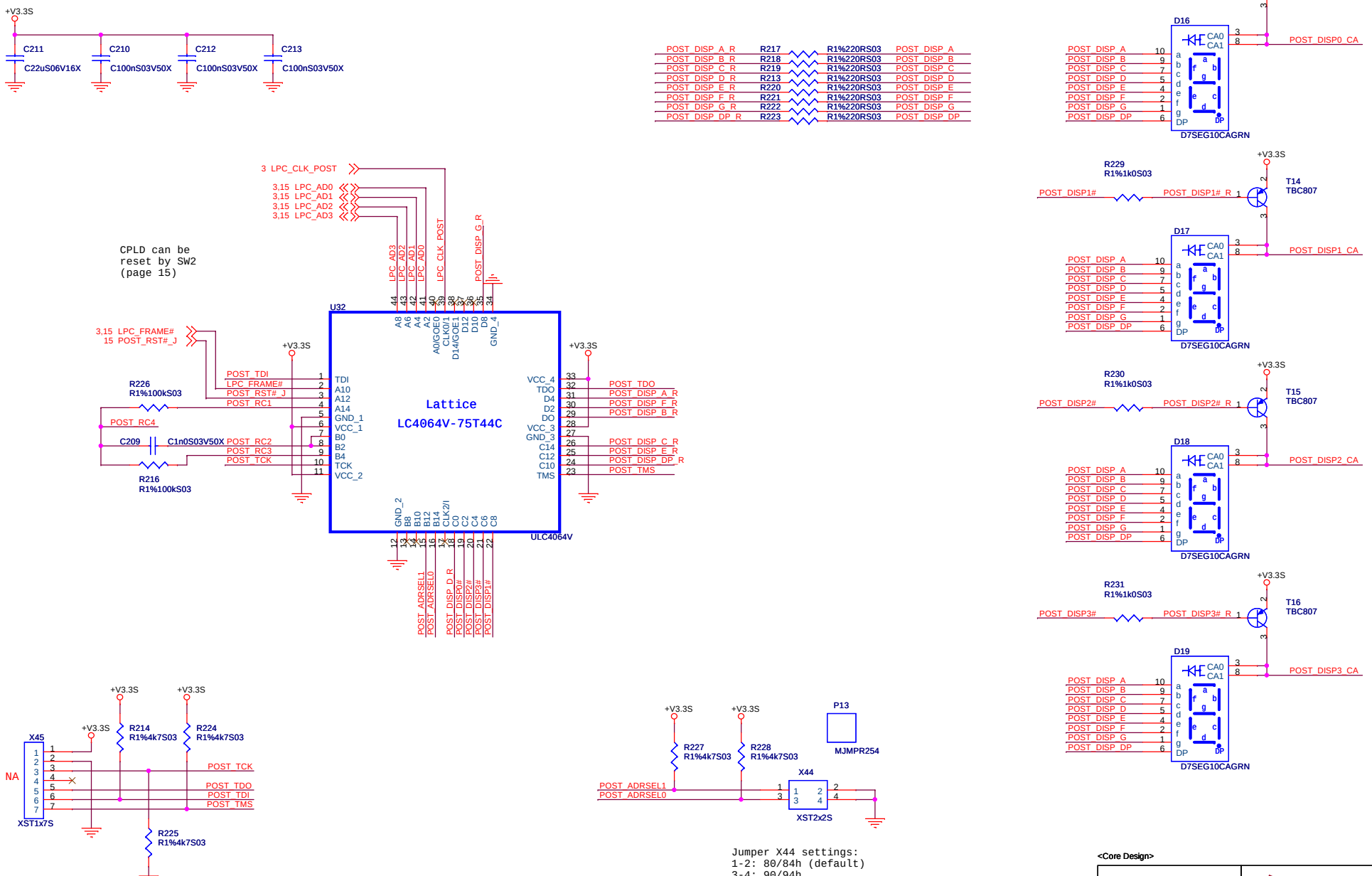
CAN transceiver



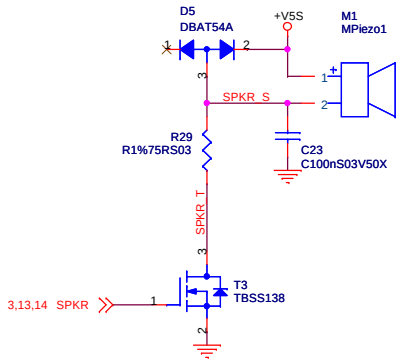
Jumper X9 settings:
1-2: CAN termination enabled
2-3: CAN termination disabled (default)

<Core Design>

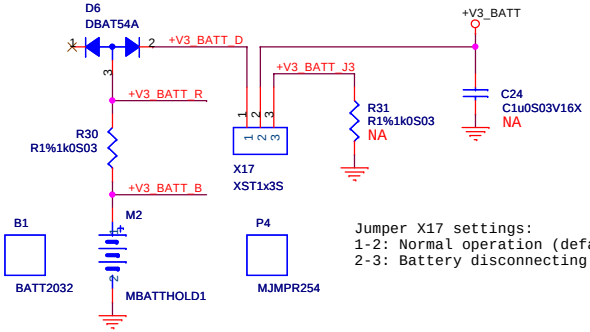
Congatec AG Auwiesenstrasse 5 D-94469 Deggendorf Germany	congatec the rhythm of embedded computing
Title: LPC (GPIO) / SPI / I2C EEPROM / CAN	
Size: A3	Document Number: QEV2 — Created: LIKR — Rev: B.3
Date: Monday, November 03, 2014	Sheet 16 of 22


+V3.3S
C211
C22uS06V16X
C210
C100nS03V50X
C212
C100nS03V50X
C213
C100nS03V50X
POST_DISP_A_R R217 R1%220RS03 POST_DISP_A
POST_DISP_B_R R218 R1%220RS03 POST_DISP_B
POST_DISP_C_R R219 R1%220RS03 POST_DISP_C
POST_DISP_D_R R213 R1%220RS03 POST_DISP_D
POST_DISP_E_R R220 R1%220RS03 POST_DISP_E
POST_DISP_F_R R221 R1%220RS03 POST_DISP_F
POST_DISP_G_R R222 R1%220RS03 POST_DISP_G
POST_DISP_DP_R R223 R1%220RS03 POST_DISP_DP
R215 R1%1k0S03
POST_DISP0#
POST_DISP0#_R
T13 TBC807
D16
POST_DISP0_CA
D7SEG10CAGRN
R229 R1%1k0S03
POST_DISP1#
POST_DISP1#_R
T14 TBC807
D17
POST_DISP1_CA
D7SEG10CAGRN
R230 R1%1k0S03
POST_DISP2#
POST_DISP2#_R
T15 TBC807
D18
POST_DISP2_CA
D7SEG10CAGRN
R231 R1%1k0S03
POST_DISP3#
POST_DISP3#_R
T16 TBC807
D19
POST_DISP3_CA
D7SEG10CAGRN
3 LPC_CLK_POST
3,15 LPC_AD0
3,15 LPC_AD1
3,15 LPC_AD2
3,15 LPC_AD3
CPLD can be
reset by SW2
(page 15)
U32
Lattice
LC4064V-75T44C
ULC4064V
3,15 LPC_FRAME#
15 POST_RST#_J
R226 R1%100kS03
R216 R1%100kS03
C209 C1n0S03V50X
POST_TDI
POST_TDO
POST_TMS
POST_TCK
POST_RC1
POST_RC2
POST_RC3
POST_RC4
POST_DISP_A_R
POST_DISP_B_R
POST_DISP_C_R
POST_DISP_D_R
POST_DISP_E_R
POST_DISP_F_R
POST_DISP_G_R
POST_DISP_DP_R
POST_ADRSEL1
POST_ADRSEL0
X45
NA
XST1x7S
R214 R1%4k7S03
R224 R1%4k7S03
R225 R1%4k7S03
R227 R1%4k7S03
R228 R1%4k7S03
P13
MJMPR254
X44
XST2x2S
Jumper X44 settings:
1-2: 80/84h (default)
3-4: 90/94h
<Core Design>
Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany
congatec
the rhythm of embedded computing
Title
POST display
Size A3
Document Number QEV2
Created LIKR
Rev B.3
Date: Monday, November 03, 2014
Sheet 17 of 22

PC BEEP

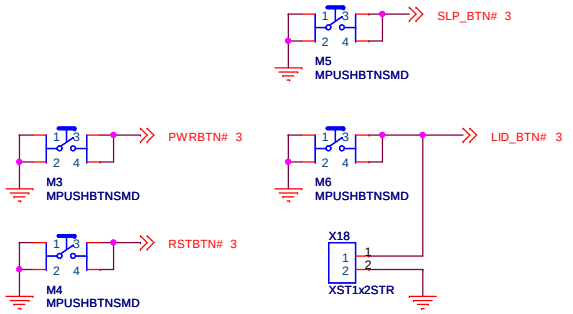


RTC/CMOS Battery

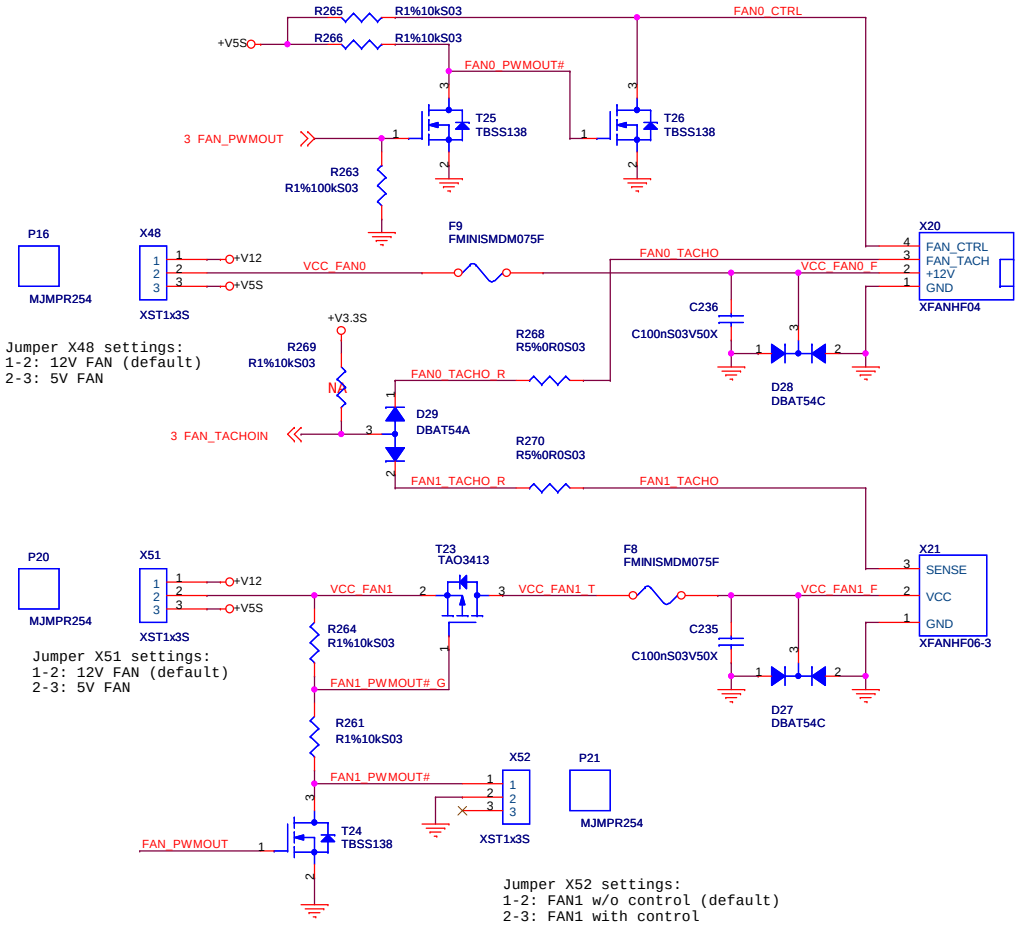


Jumper X17 settings:
1-2: Normal operation (default)
2-3: Battery disconnecting

Buttons



FAN

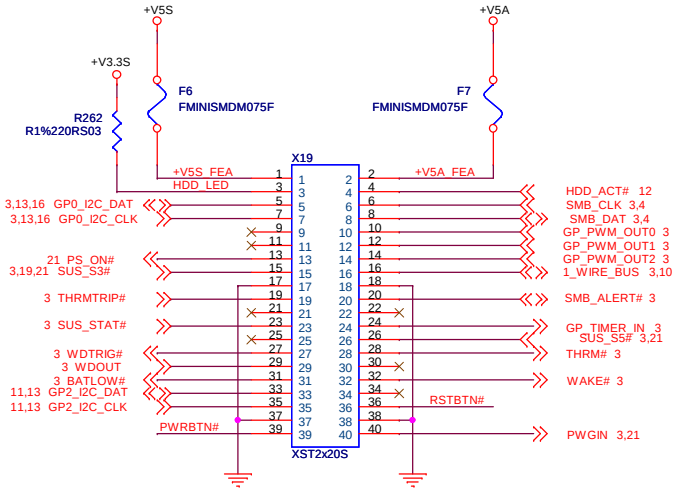


Jumper X48 settings:
1-2: 12V FAN (default)
2-3: 5V FAN

Jumper X51 settings:
1-2: 12V FAN (default)
2-3: 5V FAN

Jumper X52 settings:
1-2: FAN1 w/o control (default)
2-3: FAN1 with control

Feature



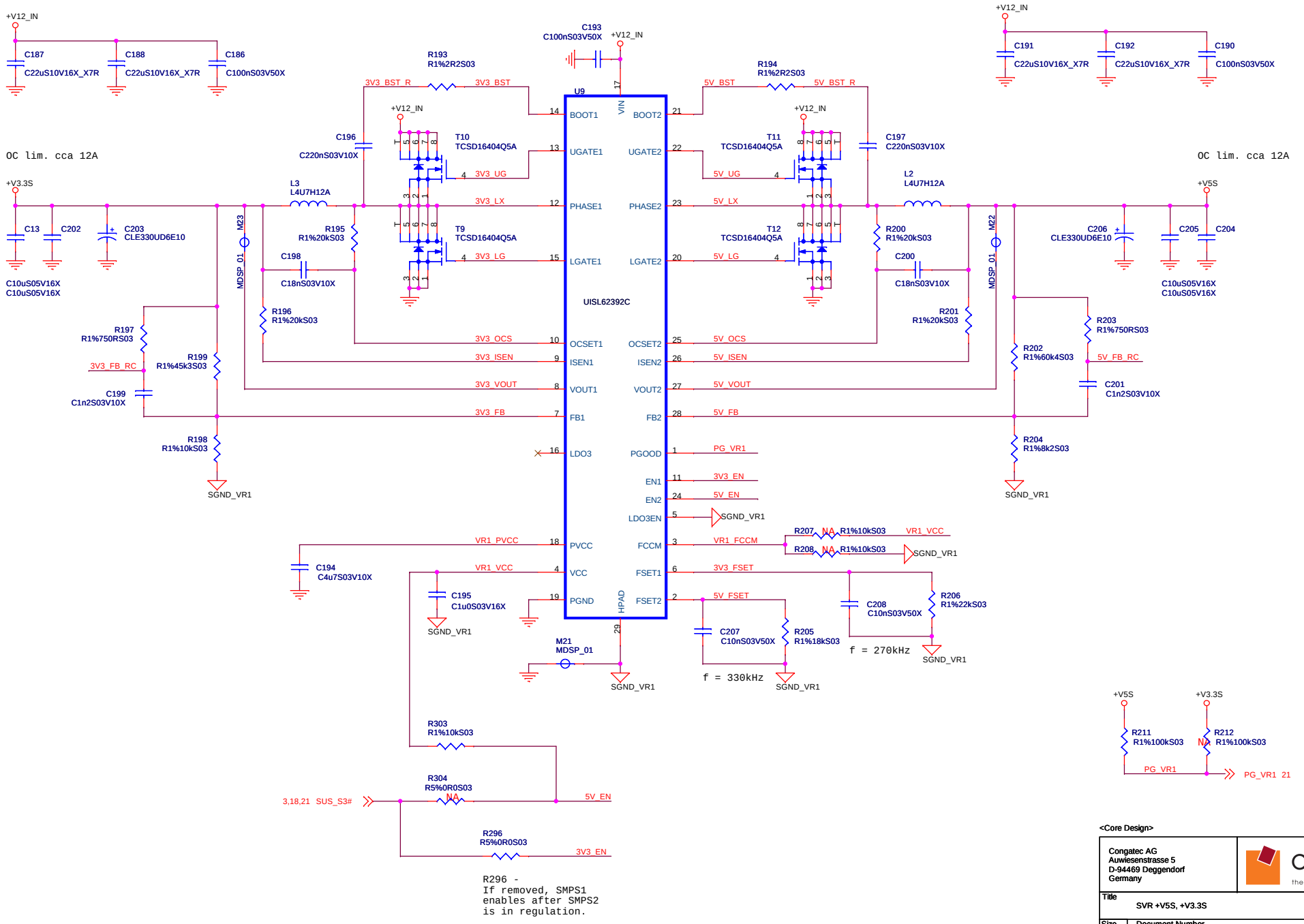
SMBus / GP1_I2C
(CMOS 3.3V
Suspend)

<Core Design>

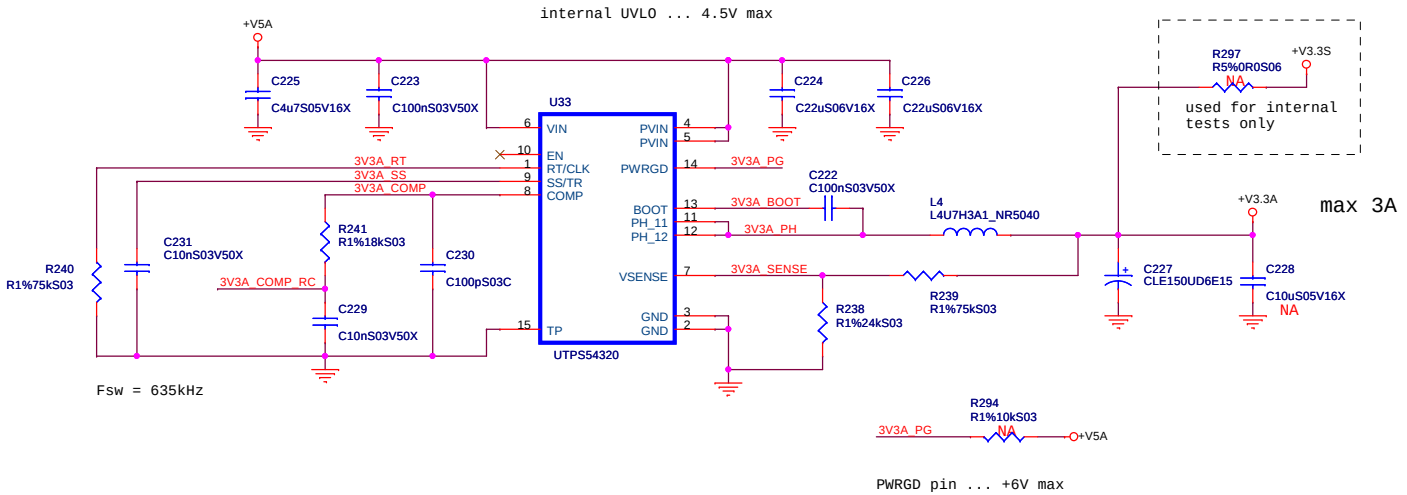
Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

congatec
the rhythm of embedded computing

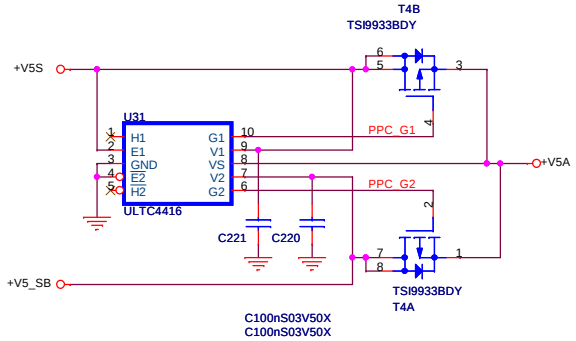
Title: BATT / SPKR / Feature / FAN			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 18 of 22		


+V12_IN
C187
C22uS10V16X_X7R
C188
C22uS10V16X_X7R
C186
C100nS03V50X
C193
C100nS03V50X
R193
R1%2R2S03
3V3_BST_R
3V3_BST
U9
VIN
BOOT1
BOOT2
UGATE1
UGATE2
PHASE1
PHASE2
LGATE1
LGATE2
OCSET1
OCSET2
ISEN1
ISEN2
VOUT1
VOUT2
FB1
FB2
LDO3
PGOOD
EN1
EN2
LDO3EN
PVCC
FCCM
FSET1
FSET2
PGND
HPAD
UISL62392C
R194
R1%2R2S03
5V_BST
5V_BST_R
C191
C22uS10V16X_X7R
C192
C22uS10V16X_X7R
C190
C100nS03V50X
OC lim. cca 12A
OC lim. cca 12A
+V3.3S
+V5S
C13
C202
C203
CLE330UD6E10
C10uS05V16X
C10uS05V16X
C206
CLE330UD6E10
C205
C204
C10uS05V16X
C10uS05V16X
L3
L4U7H12A
L2
L4U7H12A
C196
C220nS03V10X
C197
C220nS03V10X
T10
TCSD16404Q5A
T11
TCSD16404Q5A
T9
TCSD16404Q5A
T12
TCSD16404Q5A
3V3_UG
3V3_LX
3V3_LG
5V_UG
5V_LX
5V_LG
R195
R1%20kS03
R200
R1%20kS03
C198
C18nS03V10X
C200
C18nS03V10X
MDSP_01
M23
M22
R196
R1%20kS03
R201
R1%20kS03
R197
R1%750RS03
R199
R1%45k3S03
3V3_FB_RC
C199
C1n2S03V10X
R198
R1%10kS03
SGND_VR1
R203
R1%750RS03
R202
R1%60k4S03
5V_FB_RC
C201
C1n2S03V10X
R204
R1%8k2S03
3V3_OCS
3V3_ISEN
3V3_VOUT
3V3_FB
5V_OCS
5V_ISEN
5V_VOUT
5V_FB
PG_VR1
3V3_EN
5V_EN
VR1_PVCC
VR1_VCC
VR1_FCCM
3V3_FSET
5V_FSET
C194
C4u7S03V10X
C195
C1u0S03V16X
R207
NA
R1%10kS03
R208
NA
R1%10kS03
C208
C10nS03V50X
R206
R1%22kS03
f = 270kHz
C207
C10nS03V50X
R205
R1%18kS03
f = 330kHz
M21
MDSP_01
R303
R1%10kS03
R304
R5%0R0S03
NA
3,18,21 SUS_S3#
5V_EN
R296
R5%0R0S03
3V3_EN
R296 -
If removed, SMPS1
enables after SMPS2
is in regulation.
+V5S
+V3.3S
R211
R1%100kS03
R212
NA
R1%100kS03
PG_VR1
PG_VR1 21
<Core Design>
Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany
congatec
the rhythm of embedded computing
Title
SVR +V5S, +V3.3S
Size
A3
Document Number
QEV2
Created
LIKR
Rev
B.3
Date:
Monday, November 03, 2014
Sheet
19
of
22

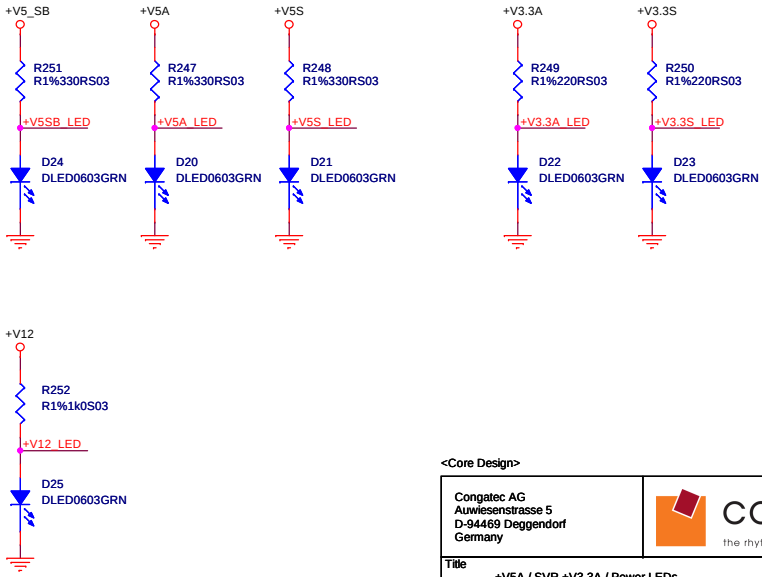
+3.3V Standby



+5V Standby



Power LEDs

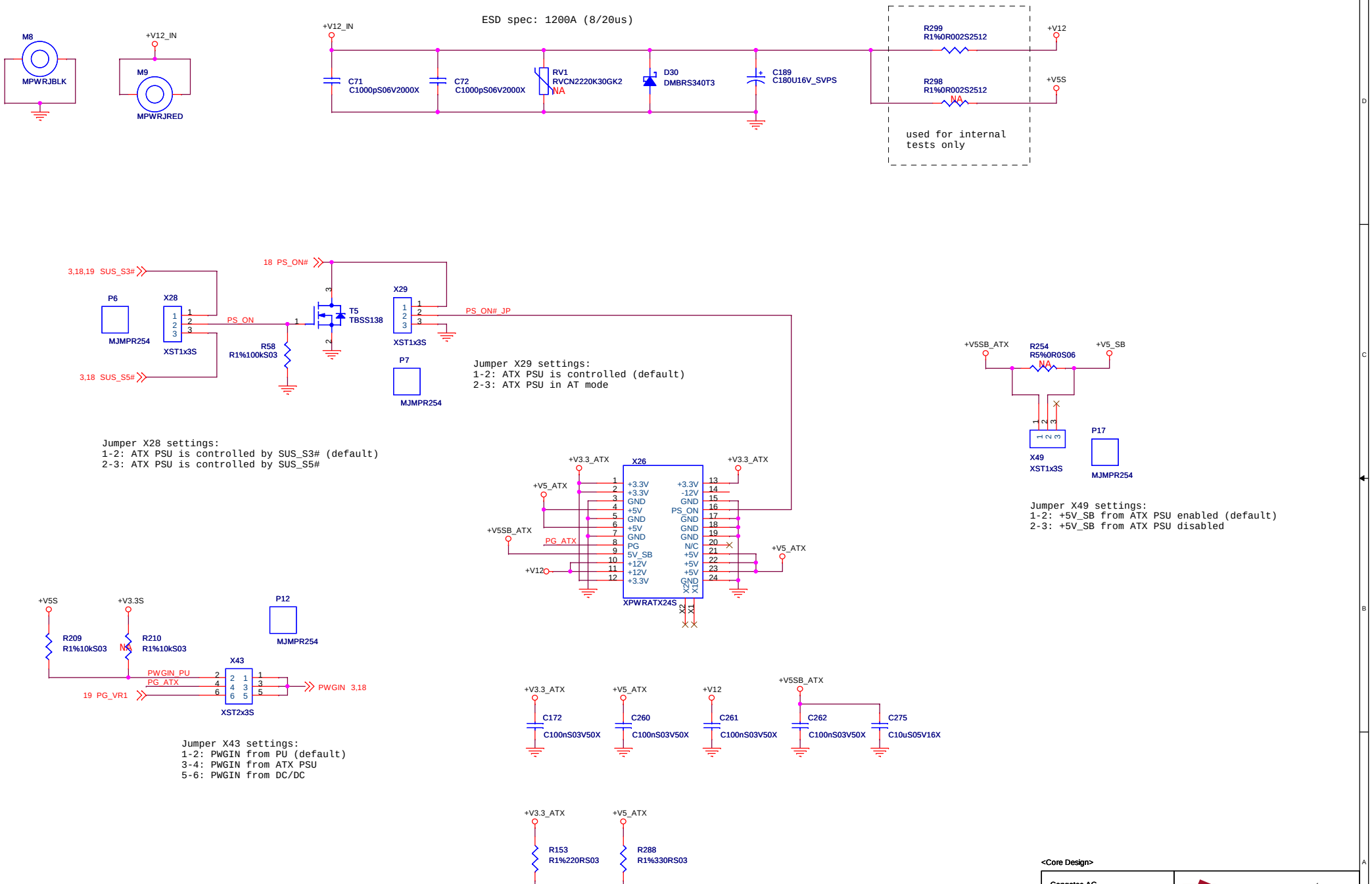


<Core Design>

Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

congatec
the rhythm of embedded computing

Title: +V5A / SVR +V3.3A / Power LEDs			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 20 of 22		



<Core Design>

Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

congatec
the rhythm of embedded computing

Title: ATX / DC Power Input

Size	Document Number	Created	Rev
A3	QEV2	LIKR	B.3

Date: Monday, November 03, 2014 Sheet 21 of 22

Revision History

Rev. X.0	MAY/16/2013	LIKR	all	design created
Rev. A.0	OCT/25/2013	LIKR	all	Test points were changed to the same type.
			1	H8 connected to GND. Probe M33 was added.
			3	SDVO signals were connected to module. TP1-TP4 were removed.
			4	Test points were added - TP16, TP17.
			6	R275 was replaced by X36.
			10	SDVO signals were added for supporting Qseven 1.2 modules.
			14	Connection of S/PDIF IN and S/PDIF OUT was corrected.
			16	Option for supplying SPI socket from standby power rail was added. Connection of M13 switch was changed (M13 pin 3 is connected to SPI_HOLD# now). U43 and C16 were removed.
			18	Value of R264 was updated. U4 was changed for a new type.
			19	DC/DC converter connected to +V12_IN. Values of R200,R201,C200,R195,R196,C198 were updated.
			20	+V3.3A DC/DC converter was updated (R240,U33,L4).
			21	C189 connection was changed from +V12 to +V12_IN. C275 and D30 were added.
Rev. B.0	JUN/04/2014	LIKR	5	USB OTG implementation (USB B connector was changed for micro USB AB)
			10	R92 was added (NA by default)
			13	HDA topology improvement
Rev. B.1	JUL/29/2014	LIKR	5	USB OTG updated to achieve compatibility with Qseven 1.2 (R158, R159), U23 set to NA
Rev. B.2	SEP/22/2014	LIKR	5	USB OTG updated. Jumper X37 was added to drive USB ID pin manually.
Rev. B.3	NOV/03/2014	LIKR	5	USB OTG updated. R158 is set to NA, R159 is changed to 0R (QEV2 is no longer backward compatible with Qseven 1.2 modules).

<Core Design>

Congatec AG
Auwiesenstrasse 5
D-94469 Deggendorf
Germany

congatec
the rhythm of embedded computing

Title: Revision History			
Size: A3	Document Number: QEV2	Created: LIKR	Rev: B.3
Date: Monday, November 03, 2014	Sheet 22 of 22		