congatec
the rhythm of embedded computing

ETX®
conga-ELXeco

AMD Geode™ LX processors with an AMD Geode™ CS5536 companion device and onboard memory

User's Guide

Revision 1.1

Revision History

Revision	Date (dd.mm.yy)	Author	Changes
0.1	12.11.07	GDA	Preliminary release
1.0	17.01.08	GDA	Official release
1.1	04.04.08	GDA	Added new conga-ELXeco variants (LVDS with 256MB onboard memory and TTL with 256MB onboard memory) and updated document throughout to reflect these new variants. Improved section 1.4.1 and added 1.4.2. Added 'Note' to section 6 'Signal Descriptions and Pinout Tables'.

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-ELXeco. It is one of three documents that should be referred to when designing an ETX® application. The other reference documents that should be used include the following:

- ETX® Design Guide
- ETX® Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

Disclaimer

The information contained within this user's guide, including but not limited to any product specification, is subject to change without notice.

congatec AG provides no warranty with regard to this user's guide or any other information contained herein and hereby expressly disclaims any implied warranties of merchantability or fitness for any particular purpose with regard to any of the foregoing. congatec AG assumes no liability for any damages incurred directly or indirectly from any technical or typographical errors or omissions contained herein or for discrepancies between the product and the user's guide. In no event shall congatec AG be liable for any incidental, consequential, special, or exemplary damages, whether based on tort, contract or otherwise, arising out of or in connection with this user's guide or any other information contained herein or the use thereof.

Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHZ	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
T.O.M.	Top of memory = max. DRAM installed
PATA	Parallel ATA
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

Copyright Notice

Trademarks

AMD is a trademark of Advanced Micro Devices, Inc. Expresscard is a registered trademark of Personal Computer Memory Card International Association (PCMCIA). PCI Express is a registered trademark of Peripheral Component Interconnect Special Interest Group (PCI-SIG). I²C is a registered trademark of Philips Corporation. CompactFlash is a registered trademark of CompactFlash Association. Winbond is a registered trademark of Winbond Electronics Corp. AVR is a registered trademark of Atmel Corporation. ETX is a registered trademark of Kontron AG. XpressROM is a registered trademark of Insyde Technology, Inc. Microsoft®, Windows®, Windows NT®, Windows CE and Windows XP® are registered trademarks of Microsoft Corporation. VxWorks is a registered trademark of WindRiver. conga and congatec are registered trademark of congatec AG. All product names and logos are property of their owners.

Warranty

congatec AG makes no representation, warranty or guaranty, express or implied regarding the products except its standard form of limited warranty ("Limited Warranty"). congatec AG may in its sole discretion modify its Limited Warranty at any time and from time to time.

Beginning on the date of shipment to its direct customer and continuing for the published warranty period, congatec AG represents that the products are new and warrants that each product failing to function properly under normal use, due to a defect in materials or workmanship or due to non conformance to the agreed upon specifications, will be repaired or exchanged, at congatec AG's option and expense.

Customer will obtain a Return Material Authorization ("RMA") number from congatec AG prior to returning the non conforming product freight prepaid. congatec AG will pay for transporting the repaired or exchanged product to the customer.

Repaired, replaced or exchanged product will be warranted for the repair warranty period in effect as of the date the repaired, exchanged or replaced product is shipped by congatec AG, or the remainder of the original warranty, whichever is longer. This Limited Warranty extends to congatec AG's direct customer only and is not assignable or transferable.

Except as set forth in writing in the Limited Warranty, congatec AG makes no performance representations, warranties, or guarantees, either express or implied, oral or written, with respect to the products, including without limitation any implied warranty (a) of merchantability, (b) of fitness for a particular purpose, or (c) arising from course of performance, course of dealing, or usage of trade.

congatec AG shall in no event be liable to the end user for collateral or consequential damages of any kind. congatec AG shall not otherwise be liable for loss, damage or expense directly or indirectly arising from the use of the product or from any other cause. The sole and exclusive remedy against congatec AG, whether a claim sound in contract, warranty, tort or any other legal theory, shall be repair or replacement of the product only

Technical Support

congatec AG technicians and engineers are committed to providing the best possible technical support for our customers so that our products can be easily used and implemented. We request that you first visit our website at www.congatec.com for the latest documentation, utilities and drivers, which have been made available to assist you. If you still require assistance after visiting our website then contact our technical support department by email at support@congatec.com

ETX® Concept

The ETX® concept is an off the shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific baseboard. ETX® modules have a standardized form factor of just 95mm x 114mm and have identical pinouts on the four system connectors. The ETX® module provides most of the functional requirements for any application. These functions include, but are not limited to, graphics, sound, keyboard/mouse, IDE, Ethernet, parallel, serial and USB ports. Four ruggedized connectors provide the baseboard interface and carry all the I/O signals to and from the ETX® module.

Baseboard designers can utilize as little or as many of the I/O interfaces as deemed necessary. The baseboard can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly ETX® applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class ETX® modules. Simply unplug one module and replace it with another, no redesign is necessary.

Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Certification

congatec AG is certified to DIN EN ISO 9001:2000 standard.

Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

conga-ELXeco Options Information

The conga-ELXeco is currently available in three different optional variants. This user's guide describes all of these options. Below you will find an order table showing the different configurations that are currently offered by congatec AG. Check the table for the Part no./Order no. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Part-No.	078944	085431	012247
CPU	AMD Geode™ LX800 500MHz	AMD Geode™ LX800 500MHz	AMD Geode™ LX800 500MHz
Cache	128 kByte	128 kByte	128 kByte
Onboard Memory	128MB	256MB	256MB
LVDS	Yes	Yes	No
TTL	No	No	Yes

Contents

1 Specifications

1.1 Feature List

Table 1 Feature Summary

Form Factor	ETX® standard (Rev. 2.7)
Processor	AMD Geode™ LX800 500MHz with 128 kByte cache
Memory	128MB or 256MB of onboard soldered DDR RAM (TTL variant only available with 256MB onboard DDR RAM)
Chipset	AMD Geode™ CS5536 companion device
Audio	Realtek ALC203 AC'97 Rev. 2.3 compatible.
Ethernet	Davicom DM9102D
Graphics Options	Similar to GX graphics core but with strong improvements. Unified Memory Architecture (UMA) with a maximum of 16MB hardware frame buffer compression. 2-254MB graphics memory space. • CRT Interface 350 MHz RAMDAC Resolutions up to 1920x1440 @ 85Hz • Flat panel Interface External LVDS Transmitter Supports 1x18Bit TFT configurations Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3) Resolutions 640x480 up to 1024x768 (XGA) Optional variant with direct TTL interface, max. resolution 1024x768 1x18Bit *Note: TTL pinout is based on ETX Specifications older the Rev. 2.6* • Motion Video Support Hardware Up- and Downscaling High definition digital video support Alpha blending and color keying
Super I/O	Winbond 83627HG
Peripheral Interfaces	• PCI Bus Rev. 2.3 • ISA Bus • Primary EIDE (UDMA-33) • Secondary IDE (UDMA-33 Shared with Primary IDE) • Onboard CompactFlash (Shared with Primary IDE) • 4x USB 2.0 (EHCI) • I²C Bus, Fast Mode (400 kHz) • LPT (EEP/ECP) • PS/2 Keyboard, Mouse • 2 x COM Ports, TTL Level • 1 x IrDA Port
BIOS	Based on Insyde XpressROM 1MByte Flash BIOS with congatec Embedded BIOS features
Power Management	APM 1.2 compliant

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 7 of this user's guide to determine what options are available on your particular module.

1.2 Supported Operating Systems

The conga-ELXeco supports the following operating systems.

- Microsoft® Windows® XP/2000
- Microsoft® Windows ®XP Embedded
- Microsoft® Windows® CE 5.0 / 6.0
- Linux
- QNX

1.3 Mechanical Dimensions

- 95.0 mm x 114.0 mm (3.75” x 4.5”)
- Height approx. 12mm (0.4”)

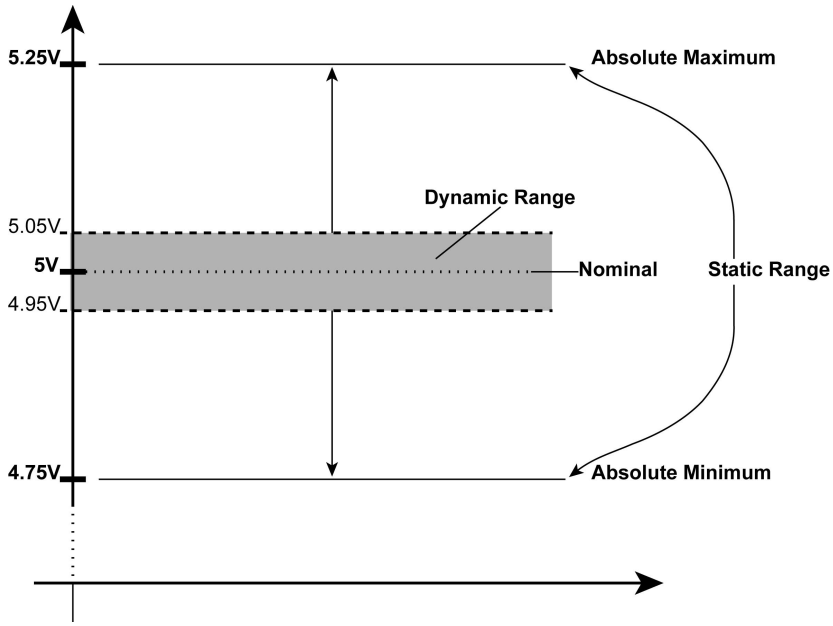
1.4 Electrical Characteristics

Characteristics			Min	Typ	Max	Units	Comment
5V	Voltage	+/-5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	100	mV_{pp}	0-20MHz
	Current	See section 1.5 'Power Consumption' for supply current information.					
5V_SB	Voltage	+/-5%	4.75	5.00	5.25	Vdc	
	Current			100	250	mA	

1.4.1 Supply Voltage Ripple

- Maximum 100mV peak to peak over a frequency band of 10Hz to 20MHz

The dynamic range shall not exceed the static range.



1.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum rise time of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

1.5 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The ETX® module was mounted into a special baseboard. This baseboard has two Hirose connectors that connect to the corresponding X3 and X4 connectors on the module. The special baseboard does not have any power consuming components mounted on it. It provides one connector for a CRT monitor connection, a PS2 keyboard and mouse connection, and an IDE device connection. The baseboard is powered by a Direct Current (DC) power supply that is set to output 5 Volts and is connected directly to the special baseboard. Additionally, positive and negative sense lines are connected to the baseboard in order to measure the current consumption of the module. This current consumption value is displayed by the DC power supply's readout and this is the value that is recorded as the power consumption measurement. All recorded values are approximate.

All external peripheral devices, such as the hard drive, are externally powered so that they do not influence the power consumption value that is measured for the module. This ensures the value measured reflects the true power consumption of the module and only the module. A keyboard is used to configure the module and then it is disconnected before the measurement is recorded. If the keyboard remained

connected, an additional current consumption of approximately 10 mA is noticed.

Each module was measured while running Windows XP Professional with SP2 (service pack 2) and the “Power Scheme” was set to “Portable/Laptop”. The screen resolution was set to 800x600 32bit High Color. The “Performance Control” was set to “Manual Strapping” BIOS default values, which is CPU clock speed at 500MHz. Power consumption values were recorded during the following stages:

Windows XP Professional SP2

- Desktop Idle
- 100% CPU workload *(see note below)*

Note

A software tool was used to stress the CPU to 100% workload.

1.5.1 conga-ELXeco 500MHz LVDS 128MB

With 128MB onboard memory

conga-ELXeco Art. No. 078944	AMD Geode™ LX800 500MHz with 128 kByte cache Layout Rev. E900LX0 /BIOS Rev. E900R003		
Memory Size	128MB		
Operating System	Windows XP Professional SP2		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	**0.7 A/3.5 W**	**0.9 A/4.5 W**	Not supported by Windows XP when in APM mode

1.5.2 conga-ELXeco 500MHz LVDS 256MB

With 256MB onboard memory

conga-ELXeco Art. No. 085431	AMD Geode™ LX800 500MHz with 128 kByte cache Layout Rev. E900LX0 /BIOS Rev. E900R003		
Memory Size	256MB		
Operating System	Windows XP Professional SP2		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	**0.8 A/4 W**	**1.0 A/5 W**	Not supported by Windows XP when in APM mode

1.5.3 conga-ELXeco 500MHz TTL 256MB

With 256MB onboard memory

conga-ELXeco Art. No. 012247	AMD Geode™ LX800 500MHz with 128 kByte cache Layout Rev. E900LX0 /BIOS Rev. E900R003		
Memory Size	256MB		
Operating System	Windows XP Professional SP2		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	**0.8 A/4 W**	**1.0 A/5 W**	Not supported by Windows XP when in APM mode

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Power consumption results will vary depending on the workload of other components such as the graphics engine.

1.6 Supply Voltage Battery Power

- 2.4-3.6V
- Typical 3.0V

1.6.1 CMOS Battery Power Consumption

RTC @ 20ºC	Voltage	Current
Integrated in the AMD Geode™ CS5536 companion device	3V DC	1.24 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

1.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

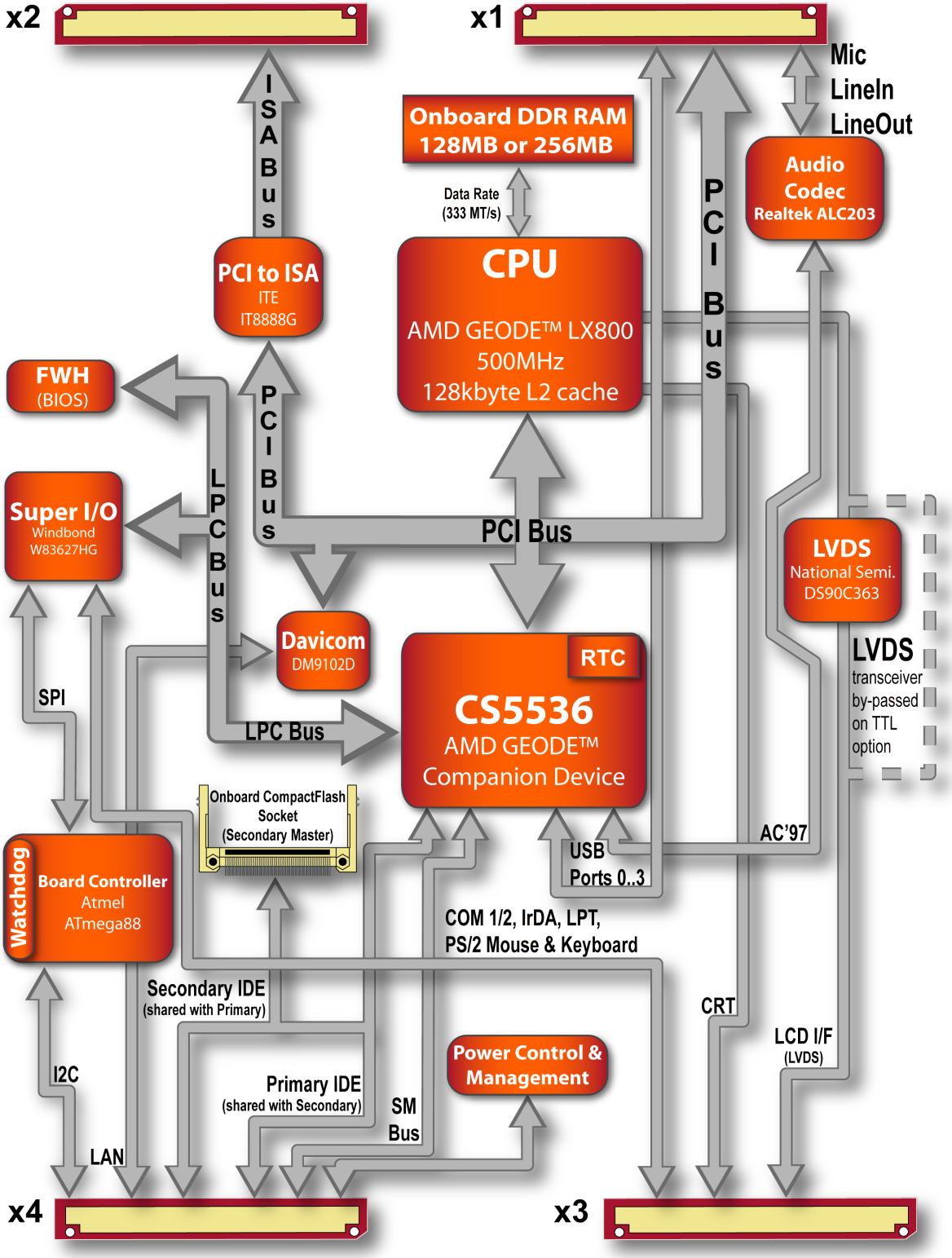
congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.

If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

For more information about operating a congatec module without heatspreader contact congatec technical support.

Humidity specifications are for non-condensing conditions.

2 Block Diagram



3 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module. It is a 2mm thick aluminum plate.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

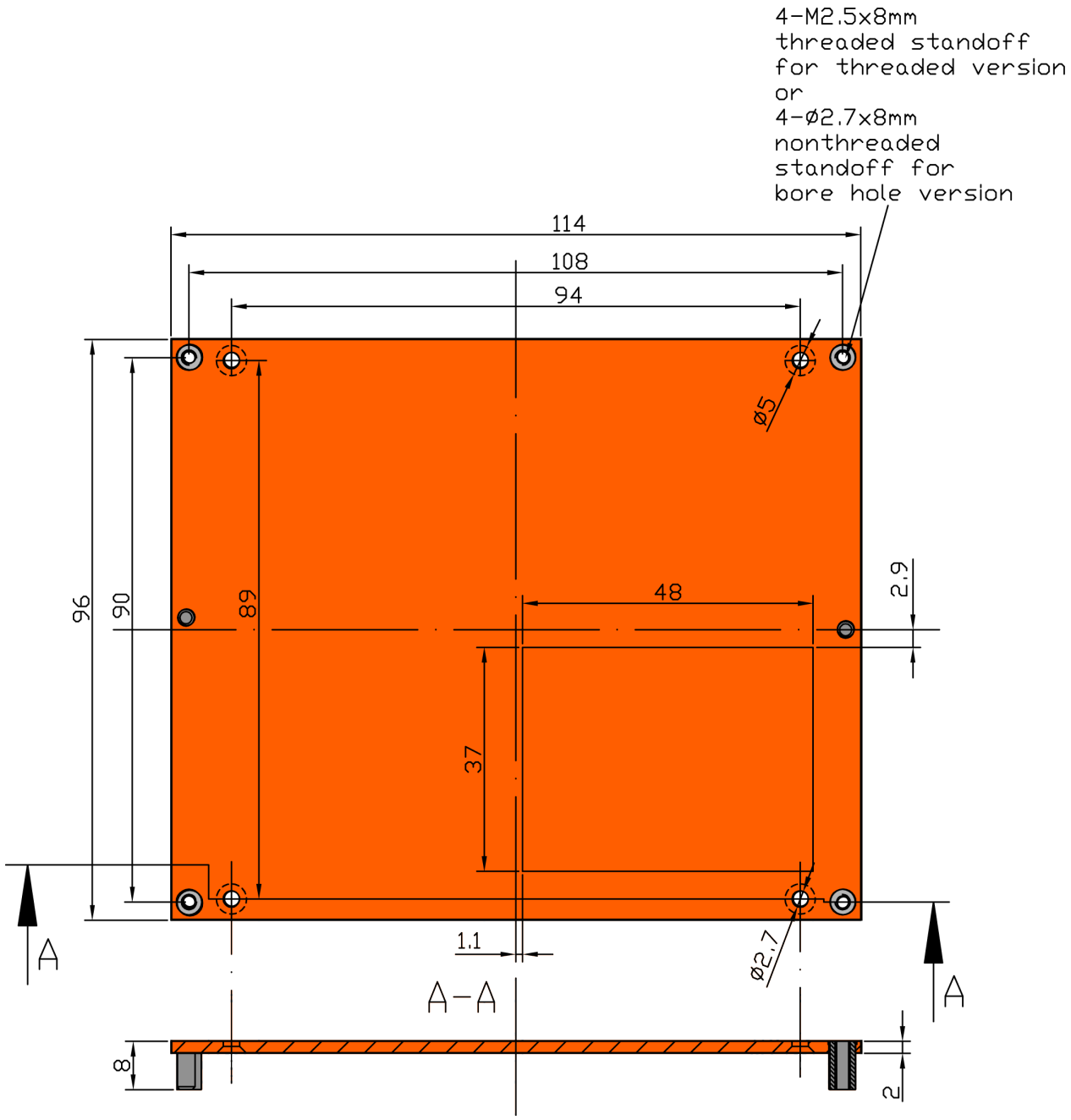
Caution

The center mounting hole on the heatspreader must be used to ensure that all components that are required to make contact with heatspreader do so. Failure to utilize the center mounting hole will result in improper contact between these components and heatspreader thereby reducing heat dissipation efficiency.

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

For more information about this subject refer to Application Note AN14_ETX_XTX_Mounting_Solutions.pdf that can be found on the congatec website.

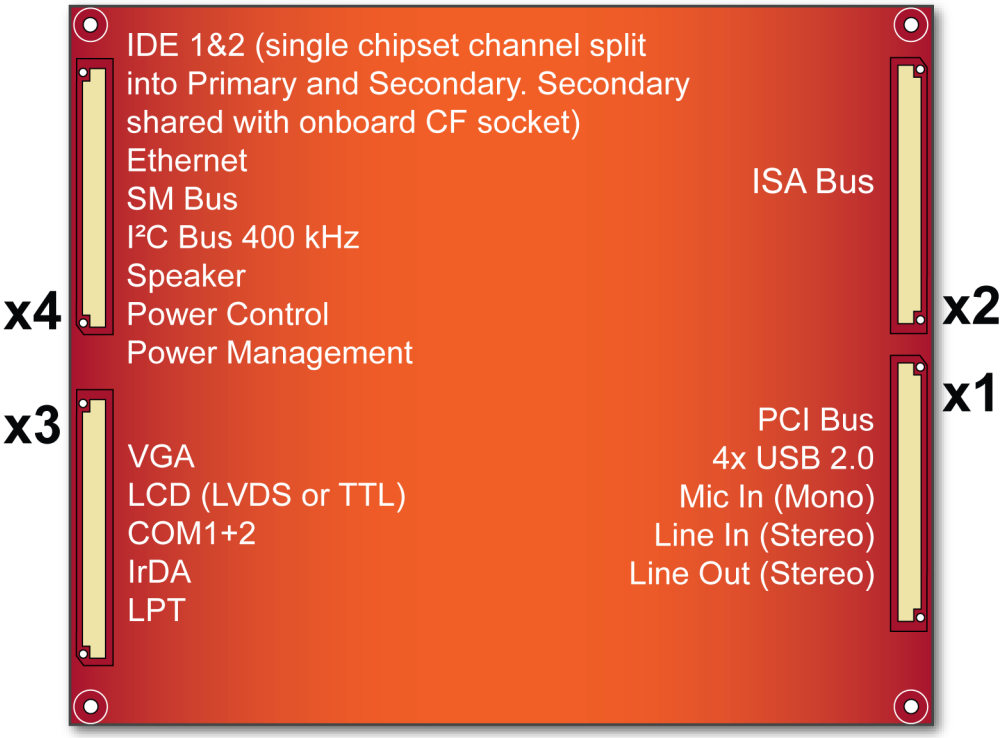
3.1 Heatspreader Dimensions



Note

All measurements are in millimeters. Torque specification for heatspreader screws is 0.5 Nm.

4 Connector Subsystems



In this view the connectors are seen “through” the module.

4.1 Connector X1

The following subsystems can be found on connector X1.

4.1.1 PCI Bus

The implementation of the PCI bus complies with PCI specification Rev. 2.3 and ETX® specification Rev. 2.7. The following signals are not supported by the AMD Geode™ CS5536 companion device.

- #PERR
- #SERR
- #LOCK

4.1.2 USB 2.0

The conga-ELXeco offers one OHCI and one EHCI USB host controller via the AMD Geode™ CS5536 companion device. These controllers comply with USB standard 1.1 and 2.0 and provide a total of four USB ports on the X1 connector that support the connection of USB 2.0 compliant devices.

4.1.3 Audio

The conga-ELXeco is equipped with a Realtek ALC203 audio codec. It is AC'97 2.3 specification compliant. The audio controller is integrated into the AMD Geode™ CS5536 companion device.

Note

The USB and Audio controllers are PCI bus devices. The BIOS allocates the necessary system resources when configuring the PCI devices.

4.1.4 Onboard Generated Supply Voltage

Pins 12, 16 and 24 on the X1 connector provide the ability to connect external devices to the modules onboard generated supply voltage (3.3V±5%). 3.3V external devices can be connected to these pins but must not exceed a maximum external load of 500mA. For more information about this feature contact congatec AG technical support.

Caution

Do not connect pins 12, 16 and 24 to a 3.3V external power supply. This will cause a current cross-flow and may result in either a system malfunction and/or damage to the external power supply and the module.

4.2 Connector X2 (ISA Bus)

4.2.1 ISA Bus

The ISA bus on the conga-ELXeco is implemented through the use of the the ITE8888 PCI to ISA bridge device. All I/O and memory ranges that are to be mapped to the ISA bus must be configured using the 'ISA I/O and Memory Configuration' setup nodes found in the BIOS Setup Program described in section 9.5.8 of this document.

The conga-ELXeco supports 8 and 16 bit DMA. For more information about this subject refer to 'Distributed DMA Channel Configuration' setup nodes found in the BIOS Setup Program described in section 9.5.9 of this document.

Note

For information about the limitations of the the ISA bus see section 7.

4.3 Connector X3

The following subsystems can be found on connector X3. The implementation of all the subsystems comply with ETX® specification 2.7. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

4.3.1 Graphics

The conga-ELXeco graphics are driven by the graphics processor, which is incorporated into the AMD Geode™ LX800 chip found on the conga-ELXeco.

4.3.2 LCD

The user interface for flat panels is called EPI (Embedded Panel Interface based on VESA EDID™ 1.3) and is implemented for both LVDS (National Semi. DS90C363 transmitter) and Digital (AMD Geode™ CS5536 companion device) flat panels. Auto detection and backlight control are also supported.

4.3.3 Serial Ports (1 and 2)

The conga-ELXeco offers two serial interfaces (TTL) that are provided by the I/O controller, which is a Winbond W83627HG super I/O located on the conga-ELXeco.

4.3.4 Serial Infrared Interface

Serial port 2 can be configured as a serial infrared interface. The Infrared (IrDA) function provides point-to-point (or multi-point to multi-point) wireless communication, which can operate under various transmission protocols including IrDA SIR. This feature is also implemented by the onboard Winbond W83627HG super I/O.

4.3.5 Parallel Port

The parallel port interface can be configured as a conventional LPT parallel port.

Note

Onboard legacy floppy is not supported on the conga-ELXeco and therefore not shared with the parallel port.

4.3.6 Keyboard/Mouse

The implementation of these subsystems comply with ETX® specification 2.7.

4.4 Connector X4

The following subsystems can be found on connector X4. The implementation of all the subsystems comply with ETX® specification 2.7. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

4.4.1 IDE

The conga-ELXeco provides one chipset IDE channel. This IDE channel originates from the CS5536 AMD Geode™ companion device and is capable of UDMA33 operation. The channel has been split in order to provide the ability to implement a Primary as well as Secondary IDE channel from the EXT connector to the carrier board. There is also an onboard CompactFlash socket that is shared with the Secondary IDE channel of the ETX connector (X4). The ComplactFlash operates as a master IDE device when present.

Due to the interconnection between the Primary and Secondary IDE channels on the ETX connector only the following IDE device configurations are permitted:

Configuration	IDE device 1	IDE device 2
1	Master Primary IDE device connected	No other IDE device connected
2	Master Primary IDE device connected	Primary Slave IDE device connected
3	CompactFlash card in socket	No other IDE device connected
4	CompactFlash card in socket	Secondary Slave IDE device connected
5	CF socket empty, Master Secondary IDE device connected	No other IDE device connected
6	CF socket empty, Master Secondary IDE device connected	Secondary Slave IDE device connected

4.4.2 Ethernet

Ethernet interface is provided by a Davicom DM9102D Single Chip Fast Ethernet NIC controller. The controller is IEEE 802.3u, 100Base-Tx fast Ethernet compatible and supports 100 Mbit/s transfer rates. The interface provides single-ended differential signals that have to be routed through an Ethernet transformer.

Note

The conga-ELXeco does not support 10 Mbit/s transfer rates.

4.4.3 I²C Bus 400kHz

The I²C bus is implemented through the use of ATMEL ATmega88 microcontroller. It provides a Fast Mode (400kHz max.) multi-master I²C Bus that has maximum I²C bandwidth.

4.4.4 Power Control

PWGIN

PWGIN (pin 4 on the X4 connector) can be connected to an external power good circuit or it may also be utilized as a manual reset input. In order to use PWGIN as a manual reset the pin must be grounded through the use of a momentary-contact pushbutton switch. When external circuitry asserts this signal, it's necessary that an open-drain driver drives this signal causing it to be held low for a minimum of 15ms to initiate a reset. Using this input is optional. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies the conga-ELXeco module is capable of generating its own power-on reset.

The conga-ELXeco provides support for controlling ATX-style power supplies. In order to do this the power supply must provide a constant source of 5V power. When not using an ATX power supply then the conga-ELXeco's pins PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

PS_ON#

The PS_ON (pin 5 on the X4 connector) signal is an active-low output that turns on the main outputs of an ATX-style power supply. This open-collector signal can be pulled up to the 5V_SB supply voltage through the use of a 1K resistor. Usually there is a pull-up resistor internally implemented in the power supply itself yet it is also good practice to implement a footprint for the pull-up resistor in the baseboard circuitry.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 7 on the X4 connector) is used to connect to a momentary-contact, active-low pushbutton input while the other terminal on the pushbutton must be connected to ground. This signal is ETX® internally pulled up to 5V_SB using a 4k7 resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-ELXeco. The remaining necessary voltages are internally generated on the module using onboard power supplies. A baseboard designer should be aware of the following important information when designing a power supply for a conga-ELXeco application:

- As mentioned earlier in section 4.1.4 the conga-ELXeco is capable of generating an onboard 3.3V supply with an output current that is limited to 500mA. If an external device requires more then this 500mA limit then it's necessary to design a 3.3V

supply into the baseboard.

Caution

It is not possible to connect an external 3.3V supply to the onboard generate 3.3V supply pins on the conga-ELXeco module. This will cause a current cross-flow and may result in either a system malfunction and/or damage to the external power supply and the module.

- Sometimes when designing baseboards, baseboard designers choose to fuse power to some external devices such as keyboards or USB devices by using solid-state or polyswitch overcurrent protection devices. This results in the protective devices typically only opening after they pass several times their rated current for long periods of time. When the application power supply is incapable of generating the necessary current needed to open these protective devices it's possible that the application crashes as a result of an external fault and therefore will reduce the applications reliability as well as make a fault diagnosis of the application difficult.

- It has also been noticed that on some occasions problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document “ATX12V Power Supply Design Guide V2.2”.

4.4.5 Power Management

APM 1.2 compliant.

5 Additional Features

5.1 Watchdog

The conga-ELXeco is equipped with a multi stage watchdog solution that is triggered by software. The ETX® Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-ELXeco does not support external hardware triggering. For more information about the Watchdog feature see the BIOS setup description section 9.5.10 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

5.2 Onboard Microcontroller

The conga-ELXeco is equipped with an ATMEL Atmega88 microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

5.3 Embedded BIOS

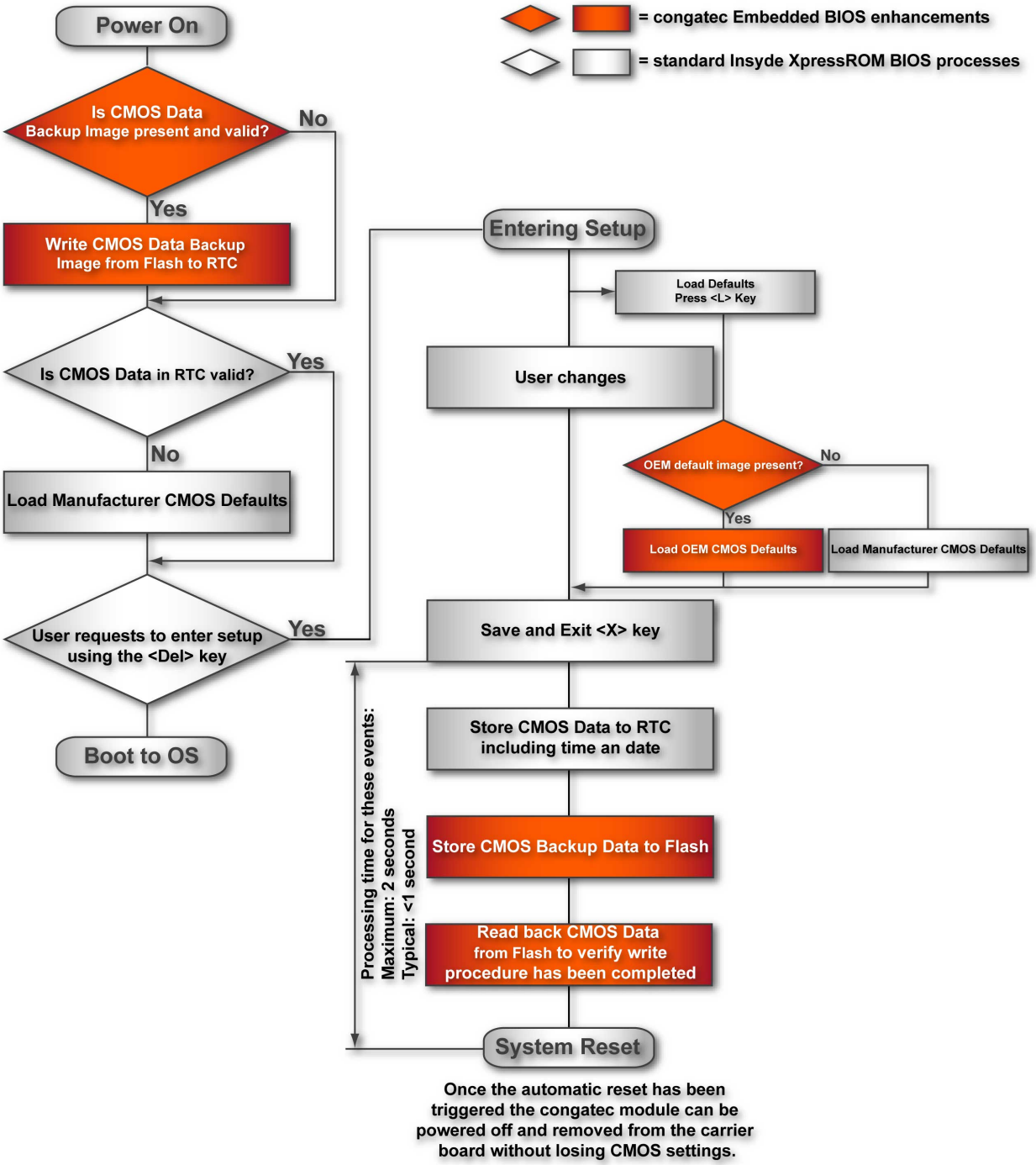
The conga-ELXeco is equipped with congatec Embedded BIOS and has the following features:

- Supports Customer Specific CMOS Defaults
- Multistage Watchdog
- User Data Storage
- Manufacturing Data and Board Information
- OEM Splash Screen
- Flat Panel Auto Detection
- BIOS Setup Data Backup
- Fast Mode I²C Bus
- Real Headless Operation

Note

The conga-ELXeco embedded BIOS is based on the Insyde XpressROM BIOS and therefore does not support 'System Plug and Play' mechanism.

5.3.1 Simplified Overview of BIOS Setup Data Backup



The above diagram provides an overview of how the BIOS Setup Data is backed up on conga-ELXeco.

Once the BIOS Setup Program has been entered and the settings have been changed,

the user saves the settings and exits the BIOS Setup Program using the X key feature. After the X function has been invoked, the CMOS Data is stored in a dedicated non-volatile CMOS Data Backup area located in the BIOS Flash Memory chip as well as RTC. The CMOS Data is written to and read back from the CMOS Data Backup area in order to verify that the write procedure was successful. Once verified the X key Save and Exit function continues to perform some minor processing tasks and finally reaches an automatic reset point, which instructs the module to reboot. After the Automatic Reset has been triggered the congatec module can be powered off and, if need be, removed from the baseboard without losing the new CMOS settings.

6 Signal Descriptions and Pinout Tables

The following section describes the signals found on the four X connectors located on the bottom of the module. Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if an ETX® module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the silicon chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 2 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
P	Power Input/Output
DDC	Display Data Channel
LVDS	Low Voltage Differential Signal-350mV nominal; 450mV maximum differential signal

6.1 X1 Connector Signal Descriptions

Table 3 Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC ±5%	P		External supply
GND	Power Ground	P		External supply
3V	Power Supply +3.3VDC	P		See section 4.1.4
N.C.	Not Connected	N.A.		Do not connect
SERIRQ	Serial Interrupt request	I		Used in conjunction with LPC bus

Table 4 PCI Signal Descriptions

Signal	Description of PCI Bus Signals	I/O	PU/PD	Comment
PCICLK1..4.	Clock output	O 3.3V		
REQ0..3#	Bus request	I 3.3V		Not 5V compliant (see Note and Caution below)
GNT0..3#	Bus grant	O 3.3V		
AD0..31	Address/Data bus lines	I/O 3.3V		Not 5V compliant (see Note and Caution below)
CBE0..3#	Bus command/byte enables	I/O 3.3V		Not 5V compliant (see Note and Caution below)
PAR	Bus parity	I/O 3.3V		Not 5V compliant (see Note and Caution below)
SERR#	Bus system error	I/O 3.3V	PU 10k 3.3V	Not supported by chipset
GPERR#	Bus grant parity error	I/O 3.3V	PU 10k 3.3V	Not supported by chipset
PME#	Bus power management event	I/O 3.3VSB	PU 5k6 3.3VSB	
LOCK#	Bus lock	I/O 3.3V		Not supported by chipset
DEVSEL#	Bus device select	I/O 3.3V	PU 10k 3.3V	Not 5V compliant (see Note and Caution below)
TRDY#	Bus target ready	I/O 3.3V	PU 10k 3.3V	Not 5V compliant (see Note and Caution below)
IRDY#	Bus initiator ready	I/O 3.3V	PU 10k 3.3V	Not 5V compliant (see Note and Caution below)
STOP#	Bus stop	I/O 3.3V	PU 10k 3.3V	Not 5V compliant (see Note and Caution below)
FRAME#	Bus frame	I/O 3.3V	PU 10k 3.3V	Not 5V compliant (see Note and Caution below)
PCIRST#	Bus reset	O 3.3V		Asserted during system reset
INTA#	Bus interrupt A	I 3.3V	PU 10k 3.3V	Not 5V compliant (see Note and Caution below)
INTB#	Bus interrupt B	I 3.3V	PU 10k 3.3V	Not 5V compliant (see Note and Caution below)
INTC#	Bus interrupt C	I 3.3V	PU 10k 3.3V	Not 5V compliant (see Note and Caution below)
INTD#	Bus interrupt D	I 3.3V	PU 10k 3.3V	Not 5V compliant (see Note and Caution below)

Note

The PCI bus on the conga-ELXeco is not 5V tolerant.

Caution

Connecting 5V PCI devices to the conga-ELXeco will cause damage to hardware and/or loss of data.

Table 5 USB Signal Descriptions

Signal	Description of USB Signals	I/O	PU/PD	Comment
USB0	USB Port 0, data + or D+	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB0#	USB Port 0, data - or D-	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB1	USB Port 1, data + or D+	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB1#	USB Port 1, data - or D-	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB2	USB Port 2, data + or D+	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB2#	USB Port 2, data - or D-	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB3	USB Port 3, data + or D+	I/O		USB 2.0 compliant and backwards compatible to USB 1.1
USB3#	USB Port 3, data - or D-	I/O		USB 2.0 compliant and backwards compatible to USB 1.1

Table 6 Audio Signal Descriptions

Signal	Description of Audio Signals	I/O	PU/PD	Comment
SNDL	Line-Level stereo output left	O		Analog output (1 Vrms)
SNDR	Line-Level stereo output right	O		Analog output (1 Vrms)
AUXAL	Auxiliary input A left	I	22k PD	Analog input (1 Vrms)
AUXAR	Auxiliary input A right	I	22k PD	Analog input (1 Vrms)
MIC	Microphone input	I	2k2 PU to Audio Vref (2,5V)	Analog input (1 Vrms)
ASGND	Analog ground of sound controller	P		For signal ground; don't supply power through this pin.
ASVCC	Analog supply of sound controller	P		5V power output (Can be used as an analog supply for analog amplifier maximum 30mA)

6.2 Connector X1 Pinout

Table 7 X1 Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	PCICLK3	4	PCICLK4	53	PAR	54	SERR# (*)
5	GND	6	GND	55	GPERR# (*)	56	Reserved
7	PCICLK1	8	PCICLK2	57	PME#	58	USB2#
9	REQ3#	10	GNT3#	59	LOCK# (*)	60	DEVSEL#
11	GNT2#	12	3V	61	TRDY#	62	USB3#
13	REQ2#	14	GNT1#	63	IRDY#	64	STOP#
15	REQ1#	16	3V	65	FRAME#	66	USB2
17	GNT0#	18	RESERVED	67	GND	68	GND
19	VCC	20	VCC	69	AD16	70	CBE2#
21	SERIRQ	22	REQ0#	71	AD17	72	USB3
23	AD0	24	3V	73	AD19	74	AD18
25	AD1	26	AD2	75	AD20	76	USB0#
27	AD4	28	AD3	77	AD22	78	AD21
29	AD6	30	AD5	79	AD23	80	USB1#
31	CBE0#	32	AD7	81	AD24	82	CBE3#
33	AD8	34	AD9	83	VCC	84	VCC
35	GND	36	GND	85	AD25	86	AD26
37	AD10	38	AUXAL	87	AD28	88	USB0
39	AD11	40	MIC	89	AD27	90	AD29
41	AD12	42	AUXAR	91	AD30	92	USB1
43	AD13	44	ASVCC	93	PCIRST#	94	AD31
45	AD14	46	SNDL	95	INTC#	96	INTD#
47	AD15	48	ASGND	97	INTA#	98	INTB#
49	CBE1#	50	SNDR	99	GND	100	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-ELXeco.

6.3 X2 Connector Signal Descriptions

Table 8 Signal Descriptions

Signal	Description	I/O	Comment
VCC	Power Supply +5VDC, ±5%	I	External supply
GND	Power Ground	I	External supply
N.C.	Not connected	N.A.	Do not connect

Table 9 ISA Bus Signal Descriptions

Signal	Description of ISA Bus Signals	I/O	PU/PD	Comment
SD0..15	ISA Data bus	I/O 5V	PU 10k 5V	
SA0..19, LA17..20	ISA Address bus	O 5V		
SBHE#	ISA Byte High Enable	O 5V	PU 10k 5V	
BALE	ISA Address Latch Enable	O 5V	PD 10k	BALE is a boot strap signal (see note below)
AEN	ISA Address Enable	O 5V	PD 10k	AEN is a boot strap signal (see note below)
MEMR#	ISA memory read	O 5V	PU 10k 5V	
SMEMR#	ISA memory read in lowest 1MB address range	O 5V	PU 10k 5V	
MEMW#	ISA memory write	O 5V	PU 10k 5V	
SMEMW#	ISA memory write in lowest 1MB address range	O 5V	PU 10k 5V	
IOR#	ISA IO read	O 5V	PU 10k 5V	
IOW#	ISA IO write	O 5V	PU 10k 5V	
IOCHK#	ISA IO check	I 5V	PU 10k 5V	Not Supported
IOCHRDY	ISA IO channel ready	I 5V	PU 1k 5V	
M16#	ISA 16Bit memory device	I 5V	PU 330R 5V	
IO16#	ISA 16Bit IO device	I 5V	PU 330R 5V	
REFSH#	ISA memory refresh cycle pending	O 5V	PU 1k 5V	Not Supported
NOWS#	ISA No wait states	I 5V	PU 330R 5V	
MASTER#	ISA Master	I 5V	PU 330R 5V	Not Supported
SYSCLK	ISA System clock (8 MHz)	O 5V		
OSC	ISA Oscillator (14,31818 MHz)	O 5V		
RSTDRV	ISA Reset signal	O 5V		
DREQ [0,1,2,3,5,6,7]	ISA DMA request	I 5V	PD 10k	DRQ0 not supported, limited support following DDMA R6.0
DACK# [0,1,2,3,5,6,7]	ISA DMA acknowledge	O 5V	PU 50k 5V	DACK#0 not supported, limited support following DDMA R6.0

Signal	Description of ISA Bus Signals	I/O	PU/PD	Comment
TC	ISA DMA end	O 5V	PD 10k	TC is a boot strap signal (see note below)
IRQ [3..7, 9..15]	ISA Interrupt request	I/O 5V	PU 50k 5V	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 6.8 of this user's guide.

6.4 X2 Connector Pinout

Table 10 Connector X2 Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	SD14	4	SD15	53	SA6	54	IRQ5
5	SD13	6	MASTER# (*)	55	SA7	56	IRQ6
7	SD12	8	DREQ7	57	SA8	58	IRQ7
9	SD11	10	DACK7#	59	SA9	60	SYSCLK
11	SD10	12	DREQ6	61	SA10	62	REFSH# (*)
13	SD9	14	DACK6#	63	SA11	64	DREQ1
15	SD8	16	DREQ5	65	SA12	66	DACK1#
17	MEMW#	18	DACK5#	67	GND	68	GND
19	MEMR#	20	DREQ0 (*)	69	SA13	70	DREQ3
21	LA17	22	DACK0# (*)	71	SA14	72	DACK3#
23	LA18	24	IRQ14	73	SA15	74	IOR#
25	LA19	26	IRQ15	75	SA16	76	IOW#
27	LA20	28	IRQ12	77	SA18	78	SA17
29	LA21	30	IRQ11	79	SA19	80	SMEMR#
31	LA22	32	IRQ10	81	IOCHRDY	82	AEN
33	LA23	34	IO16#	83	VCC	84	VCC
35	GND	36	GND	85	SD0	86	SMEMW#
37	SBHE#	38	M16#	87	SD2	88	SD1
39	SA0	40	OSC	89	SD3	90	NOWS#
41	SA1	42	BALE	91	DREQ2	92	SD4
43	SA2	44	TC	93	SD5	94	IRQ9
45	SA3	46	DACK2#	95	SD6	96	SD7
47	SA4	48	IRQ3	97	IOCHK# (*)	98	RSTDRV
49	SA5	50	IRQ4	99	GND	100	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-ELXeco.

6.5 X3 Connector Signal Descriptions

Table 11 Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC, ±5%	P		External supply
GND	Power Ground	P		External supply
N.C.	Not connected	N.A.		Do not connect
LTGIO0	General Purpose I O	N.A.		Not supported

Table 12 CRT Signal Descriptions

Signal	Description of CRT signals	I/O	PU/PD	Comment
HSY	Horizontal Synchronization Pulse	O 3.3V		
VSY	Vertical Synchronization Pulse	O 3.3V		
R	Red channel RGB Analog Video Output	O		Analog output
G	Green channel RGB Analog Video Output	O		Analog output
B	Blue channel RGB Analog Video Output	O		Analog output
DDCK	Display Data Channel Clock	I/O	PU 2k2 5V	
DDDA	Display Data Channel Data	I/O	PU 2k2 5V	

Table 13 Keyboard and Infrared Signal Descriptions

Signal	Description of keyboard and infrared signals	I/O	PU/PD	Comment
KBDAT	Keyboard Data	I/O 5V	PU 4k7 5V	
KBCLK	Keyboard Clock	O 5V	PU 4k7 5V	
MSDAT	Mouse Data	I/O 5V	PU 4k7 5V	
MSCLK	Mouse Clock	O 5V	PU 4k7 5V	
IRTX	Infrared Transmit	O 5V		
IRRX	Infrared Receive	I 5V		

Table 14 COM Signal Descriptions

Signal	Description of COM signals	I/O	PU/PD	Comment
DTR1#	Data terminal ready for COM1	O 5V	PU 4k7 5V	DTR1# is a boot strap signal (see note below)
DTR2#	Data terminal ready for COM2	O 5V	PD 100k	
RI1#, RI2#	Ring indicator for COM1/COM2	I 5V	PD 100k	
TXD1, TXD2	Data transmit for COM1/COM2	O 5V	PU 4k7 5V	TXD1 and TXD2 are boot strap signals (see note below)
RXD1, RXD2	Data receive for COM1/COM2	I 5V	PD 100k	
CTS1#, CTS2#	Clear to send for COM1/COM2	I 5V	PD 100k	
RTS1#	Request to send for COM1	O 5V	PD 100k	RTS1# is a boot strap signal (see note below)
RTS2#	Request to send for COM2	O 5V	PD 100k	
DCD1#, DCD2#	Data carrier detect for COM1/COM2	I 5V	PD 100k	
DSR1#, DSR2#	Data set ready for COM1/COM2	I 5V	PD 100k	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 6.8 of this user's guide.

Table 15 LVDS Flat Panel Signals

Signal	Description of LVDS Flat Panel signals	I/O	PU/PD	Comment
BIASON	Controls display contrast voltage ON			Not supported
DIGON	Controls display Power ON	O 5V	PD 10k	
BLON#	Controls display Backlight ON	O 5V		
LCDDO0..19	LVDS channel data 0..19	O LVDS		LVDS 1 channel 18bit therefore LCDDO1..7 are only supported
DETECT#	Panel hot-plug detection	I		Not supported
FPDDC_CLK	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
FPDDC_DAT	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

Table 16 LVDS Interface Pinout

Pin	Signal Name	Signal Mapping	Pin	Signal Name	Signal Mapping
1	GND		2	GND	
3	R		4	B	
5	HSY		6	G	
7	VSY		8	DDCK	
9	DETECT# (*)		10	DDDA	
11	LCDDO[16] (*)	TX2OUTCLK-	12	LCDDO[18] (*)	TX2OUT3-
13	LCDDO[17] (*)	TX2OUTCLK+	14	LCDDO[19] (*)	TX2OUT3+
15	GND		16	GND	
17	LCDDO[13] (*)	TX2OUT1+	18	LCDDO[15] (*)	TX2OUT2+
19	LCDDO[12] (*)	TX2OUT1-	20	LCDDO[14] (*)	TX2OUT2-
21	GND		22	GND	
23	LCDDO[8] (*)	TX1OUT3-	24	LCDDO[11] (*)	TX2OUT0+
25	LCDDO[9] (*)	TX1OUT3+	26	LCDDO[10] (*)	TX2OUT0-
27	GND		28	GND	
29	LCDDO[4]	TX1OUT2-	30	LCDDO[7]	TX1OUTCLK+
31	LCDDO[5]	TX1OUT2+	32	LCDDO[6]	TX1OUTCLK-
33	GND		34	GND	
35	LCDDO[1]	TX1OUT0+	36	LCDDO[3]	TX1OUT1+
37	LCDDO[0]	TX1OUT0-	38	LCDDO[2]	TX1OUT1-
39	VCC		40	VCC	
41	FPDDC_DAT		42	LTGIO0 (*)	
43	FPDDC_CLK		44	BLON#	
45	BIASON (*)		46	DIGON	
47	COMP (*)		48	Y (*)	
49	SYNC (*)		50	C (*)	

TX1= Channel 1 transmit

TX2= Channel 2 transmit

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-ELXeco.

Table 17 TTL Flat Panel Signals

Signal	Description of TTL Flat Panel Signals	I/O	PU/PD	Comment
HSYNC	Horizontal synchronization pulse	O 3.3V		Also referred to as LP (Line Pulse)
VSYNC	Vertical synchronization pulse	O 3.3V		Also referred to as FLM (First Line Marker)
DIGON	Controls display Power ON	O 5V	PD 10k	
BLON#	Controls display Backlight ON	O 5V		
R[0..5], B[0..5], G[0..5]	RGB Signals	O 3.3V		
SHFCLK	Panel data clock	O 3.3V		
DE	Data Enable	O 3.3V		

Note

The conga-ELXeco TTL pinout is based on ETX Specification Rev. 2.5 and older.

Table 18 TTL Flat Panel Interface Pinout

TTL Interface Pinout			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DE	10	DDDA
11	B0	12	B2
13	B1	14	B3
15	GND	16	GND
17	G5	18	VSYNC
19	G4	20	HSYNC
21	GND	22	GND
23	G0	24	G3
25	G1	26	G2
27	GND	28	GND
29	R4	30	B5
31	R5	32	B4
33	GND	34	GND
35	R1	36	R3
37	R0	38	R2
39	VCC	40	VCC
41	FPDDC_DAT	42	N.C.
43	FPDDC_CLK	44	BLON#
45	N.C.	46	DIGON
47	N.C.	48	N.C.
49	N.C.	50	N.C.
51	FLPY# (*)	52	SHFCLK

Note

The conga-ELXeco TTL pinout is based on ETX Specification Rev. 2.5 and older. The signals marked with an asterisk symbol (*) are not supported on the conga-ELXeco.

Table 19 LPT Signal Descriptions

Signal	Description of LPT signals	I/O	PU/PD	Comment
LPT	LPT Interface configuration input	N.A.		Not supported
STB#	Strobe signal	O 5V		
AFD#	Automatic feed	O 5V		
PD0	Data bus D0	I/O 5V		
PD1	Data bus D1	I/O 5V		
PD2	Data bus D2	I/O 5V		
PD3	Data bus D3	I/O 5V		
PD4	Data bus D4	I/O 5V		
PD5	Data bus D5	I/O 5V		
PD6	Data bus D6	I/O 5V		
PD7	Data bus D7	I/O 5V		
ERR#	LPT error	I 5V		
INIT#	Initiate	O 5V		
SLIN#	Select	O 5V		
ACK#	Acknowledge	I 5V		
BUSY	Busy	I 5V		
PE	Paper empty	I 5V		
SLCT	Power On	I 5V		

Table 20 LPT Support Mode Pinout

Parallel Port Mode Pinout			
Pin	**Signal**	**Pin**	**Signal**
51	LPT (*)	52	RESERVED
53	VCC	54	GND
55	STB#	56	AFD#
57	RESERVED	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2#	80	PD0
81	VCC	82	VCC
83	RXD1	84	ACK#
85	RTS1#	86	BUSY
87	DTR1#	88	PE
89	DCD1#	90	SLCT
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-ELXeco.

6.6 X4 Connector Signal Descriptions

Table 21 Signal Descriptions

Signal	Description	I/O	Comment
VCC	Power Supply +5VDC, ±5%	I	external supply
GND	Power Ground	I	external supply
N.C.	Not connected	N.A.	Do not connect
PIDE	Refers to Primary IDE channel	I/O	
SIDE	Refers to Secondary IDE channel	I/O	Connected with PIDE

Table 22 IDE Signal Descriptions

Signal	Description of IDE signals	I/O	PU/PD	Comment
PIDE_D0..15	Primary IDE Data bus	I/O 3.3V		PD 10k on PIDE_D7
PIDE_A0..2	Primary IDE Address bus	O 3.3V		
PIDE_CS1#	Primary IDE chip select channel 0	O 3.3V		
PIDE_CS3#	Primary IDE chip select channel 1	O 3.3V		
PIDE_DRQ	Primary IDE DMA request	I 3.3V	PD 10k	
PIDED_AK#	Primary IDE DMA acknowledge	O 3.3V		
PIDE_RDY	Primary IDE ready	I 3.3V	PU 10k 3.3V	
PIDE_IOR#	Primary IDE IO read	O 3.3V		
PIDE_IOW#	Primary IDE IO write	O 3.3V		
PIDE_INTRQ	Primary IDE interrupt request	I 3.3V	PU 10k 3.3V	
SIDE_D0..15	Secondary IDE Data bus	I/O 3.3V		Connected with PIDE_D0..15
SIDE_A0..2	Secondary IDE Address bus	O 3.3V		Connected with PIDE_A0..2
SIDE_CS1#	Secondary IDE chip select channel0	O 3.3V		Connected with PIDE_CS1#
SIDE_CS3#	Secondary IDE chip select channel1	O 3.3V		Connected with PIDE_CS3#
SIDE_DRQ	Secondary IDE DMA request			Connected with PIDE_DRQ
SIDED_AK#	Secondary IDE DMA acknowledge	O 3.3V		Connected with PIDED_AK#
SIDE_RDY	Secondary IDE ready	I 3.3V		Connected with PIDE_RDY
SIDE_IOR#	Secondary IDE IO read	O 3.3V		Connected with PIDE_IOR#
SIDE_IOW#	Secondary IDE IO write	O 3.3V		Connected with PIDE_IOW#
SIDE_INTRQ	Secondary IDE interrupt request	I 3.3V		Connected with PIDE_INTRQ
DASP_S	Secondary IDE Drive active	O		Connected to onboard CF socket (sec. master)
PDIAG_S	Secondary IDE Master/Slave negotiation	I		
HDRST#	Hard Drive reset	O 5V		
CBLID_P#	Primary IDE 80pin cable detection	I 3.3V	PU 10k 3.3V	Connected with PDIAG_S

Table 23 Ethernet Signal Descriptions

Signal	Description of Ethernet signals	I/O	PU/PD	Comment
TXD#, TXD	Ethernet Twisted Pair transmit signal pair	O		Twisted pair signals for external transformer
RXD#, RXD	Ethernet Twisted Pair receive signal pair	I		Twisted pair signals for external transformer
ACTLED#	Ethernet activity LED	O 3.3V		
LILED#	Ethernet link LED	O 3.3V		
SPEEDLED#	Ethernet speed LED, ON at 100Mb/s	O 3.3V		

Table 24 Power Control Signals

Signal	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	Power good input	I	PU 4k7 5V	Also usable as reset input, make low with O.C. to cause reset.
5V_SB	Supply of internal suspend circuit	P		
PS_ON#	Power Save ON	O 5VSB	PU 10k 5VSB	
PWRBTN#	Power Button	I 5VSB	PU 10K 5VSB	

Table 25 Power Management Signals

Signal	Description of Power Management signals	I/O	PU/PD	Comment
RSMRST#	Resume / reset input	I 3.3VSB	PU 10k 3.3VSB	
SMBALRT#	System management bus alert input	I		Not supported
BATLOW#	Battery low input	I 3.3VSB	PU 10k 3.3VSB	
GPE1#	General purpose power management event input 1	I 3.3V	PU 10k 3.3V	
GPE2#	General purpose power management event input 2	I 3.3VSB	PU 5k6 3.3VSB	
EXTSMI#	System management interrupt input	I 3.3VSB	PU 10k 3.3VSB	

Table 26 Miscellaneous Signal Descriptions

Signal	Description of Miscellaneous signals	I/O	PU/PD	Comment
SPEAKER	Speaker output	O		
BATT	Battery supply	I		
I^2CLK	I^2C Bus clock	I/O 5V	PU 4k7 5V	
I^2DAT	I^2C Bus Data	I/O 5V	PU 4k7 5V	
SMBCLK	SM Bus clock	I/O 3.3V	PU 2k2 3.3V	
SMBDATA	SM Bus Data	I/O 3.3V	PU 2k2 3.3V	
KBINH#	Keyboard inhibit	I 5V		
OVCR#	Over current detect for USB	I 3.3V	PU 10k 3.3V	
ROMKBCS#	Do not connect	N.A.		Not available
EXT_PRG	Do not connect	N.A.		Not available
GPCS#	General purpose chip select	O		Not supported

6.7 X4 Connector Pinout

Table 27 Connector X4 Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	SIDE_IOW#	52	PIDE_IOR#
3	5V_SB	4	PWGIN	53	SIDE_DRQ	54	PIDE_IOW#
5	PS_ON#	6	SPEAKER	55	SIDE_D15	56	PIDE_DRQ
7	PWRBTN#	8	BATT	57	SIDE_D0	58	PIDE_D15
9	KBINH#	10	LILED#	59	SIDE_D14	60	PIDE_D0
11	RSMRST#	12	ACTLED#	61	SIDE_D1	62	PIDE_D14
13	ROMKBCS#	14	SPEEDLED#	63	SIDE_D13	64	PIDE_D1
15	EXT_PRG	16	I2CLK	65	GND	66	GND
17	VCC	18	VCC	67	SIDE_D2	68	PIDE_D13
19	OVCR#	20	GPCS# (*)	69	SIDE_D12	70	PIDE_D2
21	EXTSMI#	22	I2DAT	71	SIDE_D3	72	PIDE_D12
23	SMBCLK	24	SMBDATA	73	SIDE_D11	74	PIDE_D3
25	SIDE_CS3#	26	SMBALRT# (*)	75	SIDE_D4	76	PIDE_D11
27	SIDE_CS1#	28	DASP_S	77	SIDE_D10	78	PIDE_D4
29	SIDE_A2	30	PIDE_CS3#	79	SIDE_D5	80	PIDE_D10
31	SIDE_A0	32	PIDE_CS1#	81	VCC	82	VCC
33	GND	34	GND	83	SIDE_D9	84	PIDE_D5
35	PDIAG_S	36	PIDE_A2	85	SIDE_D6	86	PIDE_D9
37	SIDE_A1	38	PIDE_A0	87	SIDE_D8	88	PIDE_D6
39	SIDE_INTRQ	40	PIDE_A1	89	GPE2#	90	CBLID_P#
41	BATLOW#	42	GPE1#	91	RXD#	92	PIDE_D8
43	SIDE_AK#	44	PIDE_INTRQ	93	RXD	94	SIDE_D7
45	SIDE_RDY	46	PIDE_AK#	95	TXD#	96	PIDE_D7
47	SIDE_IOR#	48	PIDE_RDY	97	TXD	98	HDRST#
49	VCC	50	VCC	99	GND	100	GND

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-ELXeco.

Note

SIDE (secondary IDE) signals are connected to PIDE (primary IDE) signals and the onboard CompactFlash socket.

6.8 Boot Strap Signals

Table 28 Boot Strap signal Descriptions

Signal	Description of Boot Strap Signals	I/O	PU/PD	Comment
BALE	ISA Address Latch Enable	O 5V	PD 10k	BALE is a boot strap signal (see caution statement below)
AEN	ISA Address Enable	O 5V	PD 10k	AEN is a boot strap signal (see caution statement below)
TC	ISA DMA end	O 5V	PD 10k	TC is a boot strap signal (see caution statement below)
TXD1, TXD2	Data transmit for COM1/COM2	O 5V	PU 4k7 5V	TXD1 and TXD2 are boot strap signals (see caution statement below)
RTS1#	Request to send for COM1	O 5V	PD 100k	RTS1# is a boot strap signal (see caution statement below)

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either ETX® internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the ETX® module to malfunction and/or cause irreparable damage to the module.

If it is necessary to drive a TTL input (or another input which sources or sinks significant current) that uses the TXD1 signal, a CMOS-input buffer can be inserted in the signal path so that this line is not pulled up or down by external circuitry during system reset.

7 conga-ELXeco ISA Limitations

The performance of the ISA bus found on the conga-ELXeco is different due to the PCI to ISA bridge (IT8888G).

The following applies:

- Support for the following signals is missing: MASTER#, REFSH# and IOCHCK#
- The 'Virtual System Architecture' of the AMD Geode platform emulates the 'Distributed DMA' support for DMA channels 1-7 by programming the Distributed DMA slave controller of the IT8888G PCI to ISA bridge. This includes control of the signals DRQ0...7, and DACK0...7#. The emulation for these DMA channels can be enabled using the 'Distributed DMA Channel Configuration' setup node found in the 'BIOS Setup Program'.
- 8 and/or 16 bit I/O and/or Memory read and write commands on the ISA bus that are normally seen one time are actually seen two times on the following signals: IOR#, IOW#, MEMR#, MEMW#, SMEMR# and SMEMW#. This is a result of the 32 bit address decoding of the IT8888G PCI to ISA bridge.

For more information about the PCI to ISA bridge, refer to the IT8888G datasheet that can be found at www.ite.com.tw.

8 System Resources

8.1 System Memory Map

The memory addresses that should be mapped to the ISA bus must be programmed to the positive decoding registers of the IT8888 PCI to ISA bridge. The corresponding configuration settings to select the base address and the size of the ISA memory range are provided by the 'ISA I/O and Memory Configuration' setup nodes found in the BIOS Setup program and described in section 9.5.8 of this document.

Table 29 Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1296MB – 1304MB (logic)	51000000 – 51800000	8MB	Geode Link Interface Unit
1028MB – 1029MB (logic)	40400000 – 4043FFFF	256kB	VSA (Virtual System Architecture)
(TOM-24MB-64kB) – (TOM-64kB)	N.A.	24 MB	VGA graphics memory and frame buffer *
896 k – 1024 k	E0000 - FFFFF	128 kB	Runtime BIOS
800 k – 896 k	C8000 - DFFFF	96 kB	Upper memory area
640 k – 800 k	A0000 - C7FFF	160 kB	Video memory and BIOS
639 k – 640 k	9FC00 - 9FFFF	1 kB	Extended BIOS data
0 – 639k	00000 - 9FC00	512 kB	Conventional memory

Notes

T.O.M. = Top of memory = max. DRAM installed
** VGA graphics memory can be configured to 1MB in setup.*

8.2 I/O Address Assignment

The I/O address assignment of the conga-ELXeco module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

The I/O addresses that should be used on the ISA bus must be mapped to the ISA bus by programming the positive decoding registers of the IT8888 PCI to ISA bridge. The corresponding configuration settings to select the base address and the size of the ISA I/O range are provided by the 'ISA I/O and Memory Configuration' setup nodes found in the BIOS Setup program and described in section 9.5.8 of this document.

Table 30 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
0100 - 010F	16 bytes	No	congatec System Control
01F0 - 01F7	8 bytes	No	Primary IDE channel
02F8 - 02FF	8 bytes	Note	Serial Port 2 (COM2)
0370 - 0371	2 bytes	No	External Super I/O controller
0378 - 037F	8 bytes	Note	Parallel Port 1 (LPT1)
03B0 – 03DF	16 bytes	No	Video system
03F0 - 03F5	6 bytes	No	Floppy Drive Controller from external Super I/O
03F6	1 byte	No	Primary IDE channel command port
03F7	1 byte	No	Primary IDE channel status port
03F8 - 03FF	8 bytes	Note	Serial Port 1 (COM1)
0480 – 04BF	64 bytes	No	Motherboard resources
04D0 – 04D1	2 bytes	No	Motherboard resources
0800 – 087F	128 bytes	No	Motherboard resources
0A00 – 0A0F	16 bytes	No	Motherboard resources
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
6000 - 6008	8 bytes	No	System Management BUS
6100 - 61FF	256 bytes	No	GPIO Subsystem
6200 - 623F	64 bytes	No	MFGP timer register
9D00 - 9D7F	128 bytes	No	Power management register
9C00 - 9C40	128 bytes	No	ACPI register
AC1C - AC1F	4 bytes	No	VSA virtual register port
DE00 - DEFF	256 bytes	No	Ethernet controller registers
DF80 - DFFF	128bytes	No	Audio controller registers
EFF0 – EFFF	16 bytes	No	IDE controller registers

Note

Default, but can be changed to another address range.

8.3 Interrupt Request (IRQ) Lines

Table 31 IRQ Lines

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	Not Applicable
1	No	Keyboard	Not Applicable
2	No	Cascade Interrupt from Slave PIC	Not Applicable
3	Note	Serial Port 2 (COM2) / Generic	IRQ3
4	Note	Serial Port 1 (COM1) / Generic	IRQ4
5	Yes	Not Applicable	IRQ5
6	No	Floppy Drive Controller from external Super I/O	IRQ6
7	Note	Parallel Port 1 (LPT1) / Generic	IRQ7
8	No	Real-time Clock	Not Applicable
9	Yes	Not Applicable	IRQ9
10	Yes	Not Applicable	IRQ10
11	Yes	Not Applicable	IRQ11
12	No	PS/2 Mouse / Generic	IRQ12
13	No	Math processor	Not Applicable
14	No	IDE Channel 0 (IDE0)	IRQ14
15	Yes	Not Applicable	IRQ15

Note

Default, but can be changed to another interrupt.

8.4 Direct Memory Access (DMA) Channels

Table 32 DMA Channels

DMA#	Data Width	Available	Description
0	8 bits	Yes Note 3	
1	8 bits	Yes Note 3	
2	8 bits	Note 1 and 3	Floppy Drive Controller from external Super I/O
3	8 bits	Note 2 and 3	Parallel Port (LPT)
4	16 bits	No Note 3	Cascade DMA Controller
5	16 bits	Yes Note 3	
6	16 bits	Yes Note 3	
7	16 bits	Yes Note 3	

Notes

1. *If the corresponding device is disabled in BIOS setup then the DMA channel can be used by customers hardware. The DMA channel can be mapped to the ISA bus by using the 'Distributed DMA Channel Configuration' submenu setup nodes in the BIOS Setup program.*

2. *Not available if Parallel Port is used in ECP mode (Enhanced Parallel Port).*

3. *DMA channels 0-3 are mapped to LPC bus by default. If no device is using a DMA channel on the LPC bus, the DMA channel can be mapped to the ISA bus by using the BIOS Setup program. DMA channels 5-7 are not available on the LPC bus due to the limitations of the AMD CS5536 Geode companion chip. The DMA channels 5-7 can be mapped to the ISA bus by using the BIOS Setup program.*

8.5 PCI Configuration Space Map

Table 33 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	01h	00h	Internal	Host Bridge
00h	01h	01h	Internal	VGA Graphics
00h	01h	02h	Internal	Encryption
00h	08h	00h	None	IT8888 PCI to ISA Bridge (Note)
00h	0Fh	00h	Internal	CS5536 Bridge Device
00h	0Fh	02h	Internal	IDE Controller
00h	0Fh	03h	Internal	Audio Multimedia Device
00h	0Fh	04h	Internal	OHCI Host Controller
00h	0Fh	05h	Internal	EHCI Host Controller
00h	0F	06h	Internal	UDC Controller
00h	10h	00h	INTD	Davicom DM9102D Ethernet Controller

Note

The IT8888 PCI to ISA bridge doesn't use any PCI interrupt. The interrupts are routed via the serial interrupt line 'SERIRQ' of the CS5536 companion chip.

With the conga-ELXeco it is not possible to hide the IT8888 PCI to ISA bridge in the PCI configuration space map. Therefore, it's necessary to load a dummy driver in the operating system to avoid an unknown device flag in the PCI device list. This driver is a available in the conga-ELXeco driver section on the congatec website at www.congatec.com.

8.6 PCI Interrupt Routing Map

Table 34 PCI Interrupt Routing Map

PCI Bus INT line (see note below)	Geode LX800	Companion CS5536	Ethernet Davicom DM9102D
INTA	x	x	
INTB		x	
INTC		x	
INTD		x	x

Note

These interrupts are available for external devices/slots via the X1 connector.

8.7 PCI Bus Masters

The conga-ELXeco supports four external PCI Bus Masters. There are no limitations in connecting bus master PCI devices.

Note

If there are two devices connected to the same PCI REQ/GNT pair and they are transferring data at the same time then the latency time of these shared PCI devices can not be guaranteed.

8.8 SM Bus

System Management (SM) bus signals are connected to the AMD Geode™ CS5536 companion device and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

9 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

9.1 Starting the BIOS setup program

The BIOS setup program is accessed by pressing the <DEL> key during POST.

9.1.1 Manufacturer Default Settings

Pressing the <End> key repeatedly immediately after power is initiated will result in the manufacturer default settings being loaded for that particular boot sequence and only that boot sequence. This is helpful when a previous BIOS setting is no longer desired.

9.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of main frames, with submenu selections. The main frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured, only the highlighted options can be configured. An option setting can be chosen by pressing the ↑↓Up/Down keys. The actual available setting is displayed on the right side of the option. The bottom line of the frame displays a short help text related to the option. These text messages explain the options and the possible impacts when changing a setting of the selected option in the frame. The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Note

Entries in the option column displayed in bold print indicate BIOS default values.

Key	Description
← → Left/Right	Select a setup item or sub menu.
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select next item.
F1	Display General Help screen.
<L>	Load optimal default settings. (only valid in main menu)
<S>	Save changes without exit setup. (only valid in main menu)
<X>	Save changes and exit setup. (only valid in main menu)
<Q>	Discard changes and exit setup. (only valid in main menu)
ENTER	Set an option of a particular setup item or enter sub menu.
ESC	Confirm changes of the actual menu/submenu and go to next menu.

9.3 Main Menu

When you first enter the BIOS setup, you will enter the 'Main Menu' screen. You can always return to the 'Main Menu' screen by using the ESC key.

The 'Main Menu' screen allows you to configure the system date and time, displays the available submenus and defines the exit procedure. The headline in the 'Main Menu' screen shows the recent BIOS version and build date.

Feature / Submenu	Options	Description
A. Time	Hour:Minute:Second	Specifies the current time. *Note: The time is in 24-hour format.*
B. Date	Day of week, month/day/year	Specifies the current date. *Note: The date is in month-day-year format.*
C. Board Information		Displays the board information submenu.
D. Device Configuration		Displays the device configuration submenu.
E. Performance Control		Displays the performance control submenu.
F. Power Management		Displays the power management submenu.
G. Boot Order		Displays the boot order submenu.
L. Load Defaults		Load the system CMOS defaults of all the setup options.
S. Save Values Without Exit		Save changes made in the BIOS setup without exiting setup.
Q. Exit Without Save		Exit setup without saving any changes made in the BIOS setup.
X. Save values and Exit		Exit setup and reboot so the new system configuration parameters can take effect.

9.4 Board Information

The 'Board Information' screen shows the product revision, board serial number, board controller firmware revision and board statistics.

Feature	Options	Description
Product Revision	no option	Displays the hardware revision of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
Serial Number	no option	Displays the serial number of the board.
Boot Counter	no option	Displays the number of boot-ups (max. 16777215).
Running Time	no option	Displays the time the board is running [in h] (max. 65535).
OEM BIOS Version	no option	Displays the BIOS version defined by the OEM customer.

9.5 Device Configuration

Select the 'Device Configuration' submenu from the main setup menu and press enter or press the related letter in front of the menu to enter the 'Device Configuration' Setup screen. This menu is used for setting advanced features.

Submenu	Description
A. Drive Configuration	Set configuration for hard drive and flash devices
B. Graphics Configuration	Set the graphic interface configuration
C. Cache Configuration	Set the L1/L2 cache configuration
D. PCI Configuration	Set the PCI Bus configuration
E. I/O Interface Configuration	Set the I/O interface configuration
F. USB Configuration	Set the USB configuration
G. ISA I/O and Memory Configuration	Set the ISA I/O and memory address decode ranges configuration.
H. DDMA Channel Configuration	Set the Distributed DMA configuration
I. Watchdog Configuration	Set the watchdog configuration
J. Hardware Monitoring	Monitors the system temperature,voltages and the fan speed
K. Boot Screen Configuration	Set the boot screen configuration

9.5.1 Drive Configuration Submenu

Feature	Options	Description
Hard Drive Configuration	**No Option**	
IDE BIOS Support	**Enabled** Disabled	Use this option to enable/disable the INT 13h BIOS services for hard drives. If this option is enabled and an IDE controller isn't present in the system, there may be an extra delay during POST while the procedures attempt to access a device.
DMA/UDMA Support	**Enabled** Disabled	Set to *Enabled* to support DMA/UDMA BIOS support. Set to *Disabled* to force disk drives to use PIO even if DMA-capable.
Force Mode for Drive 1	**Auto** PIO0,1,2,3,4 MDMA0, 1, 2 UDMA0, 1, 2	Set to *AUTO* to let the BIOS auto detect the supported DMA mode. SWDMA = Single Word DMA MWDMA = Multi Word DMA UDMA = Ultra DMA
Force Mode for Drive 2	**Auto** PIO0,1,2,3,4 MDMA0, 1, 2 UDMA0, 1, 2	Set to *AUTO* to let the BIOS auto detect the supported DMA mode. SWDMA = Single Word DMA MWDMA = Multi Word DMA UDMA = Ultra DMA
CD-ROM Boot Support	**Enabled** Disabled	Enables/Disables the CD-ROM boot option. If the CD-ROM boot option is enabled, it will be boot from bootable CD-ROM.
Floppy Boot Support	**Enable** Disable	Enables/Disables the floppy boot option. If the floppy boot option is enabled, all the floppy boot ROM will be loaded and the floppy interface services are available. *Note: No onboard legacy floppy support.*
Network Boot Support	Enabled **Disabled**	Disable/Enable PXE network boot support to LAN. *Note: When set to 'Enabled', the system must be rebooted in order for the Intel Boot Agent device to be visible in the Boot Device Priority Menu.*

9.5.2 Graphics Configuration Submenu

Feature	Options	Description
Graphics Configuration	**No Option**	
Internal Adapter Mode	**Disabled** Primary Controller Secondary Controller	Mode for internal controller when an external video device is present.
Graphics Memory Size	2 - **24** - 254	Select graphics memory size in MBytes for the graphic system. Use even numbers of MBytes only.
Driver Control Initialization	Enabled **Disabled**	Uses OS driver for all graphics system initialization beyond internal initialization to secondary controller status.
Boot Display Device	**CRT only** LFP only TV only CRT&LFP	Select the display device used during bootup.
Local Flat Panel Type	**Auto** QVGA 1x18 VGA 1x18 SVGA 1x18 XGA 1x18 Customized EDID™	Select a predefined LFP type or set to AUTO to let the BIOS auto detect the attached LVDS panel. Auto detection is performed by reading an EDID™ data set via the panel DDC bus. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.*
Backlight Control	0%, 25%, 50%, 75%, **100%**	Set local flat panel backlight control value.

9.5.3 Cache Configuration Submenu

Feature	Options	Description
Cache Configuration	**No option**	
Cache Enable	**Enabled** Disabled	Enable/Disable the L1 and L2 system cache.
L2 Cache Enable	**Enabled** Disabled	Enable/Disable only the L2 system cache.
Cache Mode	**Write-Back** Write Through	Select the cache mode write-back or write-through
Cache Allocate	Enabled **Disabled**	Select, if a cache line should be allocated before write.

9.5.4 PCI Configuration Submenu

Feature	Options	Description
PCI Interrupt Steering	**No Option**	
PCI INTA#	3, 4, 5, 7, 9, **10**, 11, 12, 14, 15	Select fixed IRQ for PCI interrupt line. *Note: Make sure that the selected IRQ is not assigned to a legacy I/O.*
PCI INTB#	3, 4, 5, 7, 9, 10, **11**, 12, 14, 15	Select fixed IRQ for PCI interrupt line. *Note: Make sure that the selected IRQ is not assigned to a legacy I/O.*
PCI INTC#	3, 4, 5, 7, 9, **10**, 11, 12, 14, 15	Select fixed IRQ for PCI interrupt line. *Note: Make sure that the selected IRQ is not assigned to a legacy I/O.*
PCI INTD#	3, 4, 5, 7, 9, 10, **11**, 12, 14, 15	Select fixed IRQ for PCI interrupt line. *Note: Make sure that the selected IRQ is not assigned to a legacy I/O.*

9.5.5 I/O Interface Configuration Submenu

Feature	Options	Description
I/O Interface Configuration	**No Option**	
Serial Port 1	Disabled **3F8/IRQ4** 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Specifies the I/O base address and IRQ of serial port 1.
Serial Port 2	Disabled 3F8/IRQ4 **2F8/IRQ3** 3E8/IRQ4 2E8/IRQ3	Specifies the I/O base address and IRQ of serial port 2.
Parallel Port Address	**Disabled** 378 278 3BC	Specifies the I/O base address used by the parallel port.
Parallel Port Mode	**Compatible** Bi-directional EPP 1.7 EPP 1.9 ECP	Specifies the parallel port mode.
Parallel Port IRQ	**Disabled** IRQ5 IRQ7 IRQ9 IRQ10 IRQ11	Specifies the interrupt for the parallel port.
Parallel Port DMA	**None** DMA1 DMA3	Specifies the DMA channel for parallel port in ECP mode.
External Super I/O Configuration Menu	Submenu	Submenu for external Super I/O configuration. *Note: This submenu is only selectable if an external SMSC 37C669 Super I/O is present.*
Network Controller	Disabled **Enabled**	Enables/Disables the onboard PCI network controller.
System Beeper	Disabled **Enabled**	Enables/Disables the external system beeper.
Keyboard Support	**Enabled** Disabled	Enable/Disable the keyboard support. *Note: If the keyboard support is disabled it is not possible to enter system setup. If the keyboard is not used by the application, the POST process can be sped up by disabling keyboard support.*

9.5.6 External Super I/O Configuration Submenu

Feature	Options	Description
External Super I/O Configuration	**No Option**	
Floppy Support	Enabled **Disabled**	Enables/Disables floppy device of the external Super I/O controller.
Serial Port 1	**Disabled** 3E8/IRQ11 2E8/IRQ10 3E8/IRQ10 2E8/IRQ11	Specifies the I/O base address and IRQ of the serial port 1 of the external Super I/O controller. *Note: IRQ 10 and 11 are use by the PCI Interrupt Routing by default. In order to use these interrupts for external I/O COM ports you must reassign the PCI Interrupt Routing.*
Serial Port 2	**Disabled** 3E8/IRQ11 2E8/IRQ10 3E8/IRQ10 2E8/IRQ11	Specifies the I/O base address and IRQ of the serial port 2 of the external Super I/O controller. *Note: IRQ 10 and 11 are use by the PCI Interrupt Routing by default. In order to use these interrupts for external I/O COM ports you must reassign the PCI Interrupt Routing.*
Parallel Port	**Disabled** 378 278 3BC	Specifies the I/O base address used by the parallel port of the external Super I/O controller.
Parallel Port Mode	**SPP** EPP 1.7 EPP 1.9 ECP	Specifies the parallel port mode of the external Super I/O controller.
Parallel Port IRQ	Disabled **IRQ5** IRQ7	Specifies the interrupt for the parallel port of the external Super I/O controller.
Parallel Port DMA	**None** Channel 2	Specifies the DMA channel for parallel port in ECP mode.

Note

This submenu is only available if an external SMSC 37C669 Super I/O controller is present in the system. The configuration base I/O address of the Super I/O has to be 0x370 and 0x371h.

9.5.7 USB Configuration Submenu

Feature	Options	Description
USB 2.0 Configuration	**No Option**	
OHCI	Disabled **Enabled**	Enable/Disable OHCI PCI header.
EHCI	Disabled **Enabled**	Enable/Disable EHCI PCI header.
Legacy USB Support	**Enabled** Disabled	Enable/Disable legacy USB support for keyboard/mouse emulation and legacy USB boot support. *Note: If legacy USB support is disabled, it is not possible to enter the system Setup program using USB keyboard.*

9.5.8 ISA I/O and Memory Configuration Submenu

Feature	Options	Description
I/O Mapped to ISA	**No Option**	
I/O Range 0-5	Disabled **Enabled**	Enable/Disable mapping for selected I/O addresses to the ISA bus. The corresponding base address and size of the ISA mapped I/O range must be programmed to the positive decoding I/O space registers of the IT8888 PCI to ISA bridge.
I/O Range Size	1 Byte 2 Bytes 4 Bytes 8 Bytes 16 Bytes 32 Bytes 64 Bytes 128 Bytes	Select I/O address range size that should be mapped to ISA bus.
Base Address (A15-A08)	0x00-0xFF	Select I/O range base address high byte (A15-A08) in hex.
Base Address (A07-A00)	0x00-0xFF	Select I/O range base address low byte (A07-A00) in hex.

Note

The default configuration for the I/O addresses that are mapped to the ISA bus are programmed within the IT8888 PCI to ISA bridge according to the following list:

I/O Range 0: Enabled Size in Byte: 128 Base Address: 0x100
I/O Range 1: Enabled Size in Byte: 64 Base Address: 0x180
I/O Range 2: Enabled Size in Byte: 32 Base Address: 0x1C0
I/O Range 3: Enabled Size in Byte: 64 Base Address: 0x200
I/O Range 4: Enabled Size in Byte: 64 Base Address: 0x300
I/O Range 5: Enabled Size in Byte: 2 Base Address: 0x370

Feature	Options	Description
Memory Mapped to ISA	**No Option**	
Memory Range 0-3	Disabled Enabled	Enable/Disable mapping for selected memory addresses to the ISA bus. The corresponding base address and size of the ISA mapped memory range must be programmed to the positive decoding memory space registers of the IT8888 PCI to ISA bridge.
Memory Range Size	16 kByte 32 kByte 64 kByte 128 kByte 256 kByte 512 kByte 1 Mbyte 2 MByte	Select memory address range size that should be mapped to ISA bus.
Base Address (A23-A16)	0x00-0xFF	Select memory range base address high byte (A23-A16) in hex
Base Address (A15-A08)	0x00-0xFF	Select memory range base address low byte (A15-A08) in hex.

Note

The default configuration for the memory addresses that are mapped to the ISA bus is programmed to the IT8888 PCI to ISA bridge according to following list:

Memory Range 0:	*Enabled*	*Size in kByte: 32*	*Base Address: 0xC8000*
Memory Range 1:	*Enabled*	*Size in kByte: 64*	*Base Address: 0xD0000*
Memory Range 2:	*Disabled*	*Size in kByte: 16*	*Base Address: 0x0*
Memory Range 3:	*Disabled*	*Size in kByte: 16*	*Base Address: 0x0*

9.5.9 Distributed DMA Channel Configuration Submenu

Feature	Options	Description
DDMA Configuration	**No Option**	
DMA Channel 1 to ISA	**Disabled** Enabled	Enable/Disable the mapping of the 8 bit Distributed DMA channel 1 to the ISA bus.
DMA Channel 2 to ISA	**Disabled** Enabled	Enable/Disable the mapping of the 8 bit Distributed DMA channel 2 to the ISA bus.
DMA Channel 3 to ISA	Disabled **Enabled**	Enable/Disable the mapping of the 8 bit Distributed DMA channel 3 to the ISA bus.
DMA Channel 5 to ISA	Disabled **Enabled**	Enable/Disable the mapping of the 16 bit Distributed DMA channel 5 to the ISA bus.
DMA Channel 6 to ISA	**Disabled** Enabled	Enable/Disable the mapping of the 16 bit Distributed DMA channel 6 to the ISA bus.
DMA Channel 7 to ISA	**Disabled** Enabled	Enable/Disable the mapping of the 16 bit Distributed DMA channel 7 to the ISA bus.

9.5.10 Watchdog Configuration Submenu

Feature	Options	Description
Watchdog Parameter Configuration	**No Option**	
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during bootup by performing a reset.
Runtime Watchdog	**Disabled** One time trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to '*One time trigger*' the watchdog will be disabled after the first trigger. If set to *'Single event'*, every stage will be executed only once, then the watchdog will be disabled. If set to *'Repeated event'* the last stage will be executed repeatedly until a reset occurs.
Delay	See Post Watchdog	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	**NMI** Reset Power Button	Selects the type of event that will be generated when timeout 1 is reached.
Event 2	**Disabled** NMI Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** NMI Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	0.5sec 1sec 2sec 5sec **10sec** 30sec 1min 2min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.

9.5.11 Hardware Monitoring Submenu

Feature	Options	Description
CPU Temperature	no option	Current processor die temperature.
Board Temperature	no option	Current board temperature.
VCore	no option	Current Core voltage reading.
VMemory	no option	Current Memory voltage reading.
+3.3Vin	no option	Current 3.3V reading.
+5Vin	no option	Current 5V reading.
+5Vstandby	no option	Current 5V standby reading.
VBAT	no option	Current VBAT reading.

9.5.12 Boot Screen Configuration Submenu

Feature	Options	Description
Splash Screen	**Disabled** Enabled	*Disabled* displays normal POST diagnostic messages. *Enabled* displays OEM logo instead of POST messages. *Note: The default OEM logo is a dark screen.*
Clear Splash Screen	**Disabled** Enabled	Clear the splash screen after option ROM initialization.
Splash Screen Timeout	**0** - 65535	Determines the time, the splash screen is displayed during option ROM initialization.
Summary Screen	**Disabled** Enabled	Enable/Disable the summary screen during bootup.
Summary Screen Timeout	**0** - 65535	Determines the time, the summary screen is displayed before booting any OS.

9.6 Performance Control

Select the 'Performance Control' submenu from the main setup menu and press enter or press the related letter in front of the menu to enter the 'Performance Control' Setup screen. The menu is used for setting system clocks.

Feature	Options	Description
System Clock Mode	Hardware Strapping **Manual Settings**	Select if system clocks should be determined by manual settings or by hardware bootup straps. See note below.
CPU Clock Speed	333 Mhz 366 Mhz 400 Mhz 433 Mhz 466 Mhz **500 MHz**	Set the CPU clock speed. *Hardware Strapping = CPU Clock Speed: 400MHz*

Note

congatec strongly recommends that when using the 'Manual Settings' option the 'CPU Clock Speed' should be set to the default value, which is 500MHz. If an alternative setting for the 'CPU Clock Speed' must be used then it's recommended that this setting be extensively evaluated in conjunction with the complete system.

9.7 Power Management

Select the 'Power Management' submenu from the main setup menu and press enter or press the related letter in front of the menu to enter the 'Power Management' Setup screen. This menu is used for setting ACPI and APM configuration.

Feature	Options	Description
BIOS PM at Bootup	**Disabled** Enabled	BIOS will turn on Legacy PM before booting the OS.
APM Available	**Yes** No	Select APM Interface available for use.
CPU Clock Gating	Disabled **Enabled**	Set to *Enabled* for power savings.
Chipset Clock Gating	Disabled **Enabled**	Set to *Enabled* for power savings
Power Loss Control (see Note below)	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. *Remain Off* keeps the power off until the power button is pressed. *Turn On* restores power to the computer. *Last State* restores the previous power state before power loss occurred. *Note: Only works with an ATX type power supply.*
Power Button Control	Instant Off **AT Mode**	Use AT Mode with 4 seconds Soft Off or not.

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

3. *Unlike other module designs available in the embedded market, a CMOS battery is not required by congatec modules to support the 'Power Loss Control' feature.*

9.8 Boot Device Priority

Feature	Options	Description
Boot Order (Device Order 1-6)	None Floppy Disk USB Floppy Disk Hard Drive #1 Hard Drive #2 CD-ROM Drive USB Hard Drive/Flash Drive USB CD-ROM Drive Network Drive	Determines the boot order for each device. The default boot order is: 1. None 2. CD-ROM Drive 3. Hard Drive 1# 4. USB Hard Drive/Flash Drive 5. USB Floppy Disk 6. USB CD-ROM Drive 7. Network Boot

10 Additional BIOS Features

The conga-ELXeco uses an Insyde XpressROM based congatec Embedded BIOS that is stored in the Firmware Hub (FWH) and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as E900R110, where E900 is the congatec internal project name, R is the identifier for a BIOS ROM file, 1 is the so called feature number and 10 is the major and minor revision number.

10.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

11 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Audio Codec '97 Component Specification, Version 2.3 (AC '97)	http://www.intel.com/design/chipsets/audio/
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.2	http://www.pcisig.com/specifications