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XTX™ Design Guide

Guidelines for designing XTX™ carrier boards

Design Guide

Revision 1.2

Revision History

Revision	Date (dd.mm.yy)	Author	Changes
1.0	22.02.06	HCH/GDA	Official release
1.1	03.07.06	HCH	Corrected pinout of SATA connector diagram in section 5.4. Changed text in parts of section 6. Added note to the tables in section 7.
1.2	08.07.08	HCH/GDA	Added signals SPL_S5# and PP_TPM to Table 1 “Connector X2 Pinout” and Table 14 "Miscellaneous Signal Descriptions (Signals on XTX™ connector X2)". Changed section 5.1 that read “...PCIE0_TX (+ and -) to PCIE3_RX (+ and -)” to “...PCIE0_TX (+ and -) to PCIE3_TX (+ and -)“. Modified information about SATA coupling capacitors. Corrected ExpressCard pinout table. Added reference material list to section 8. Minor corrections throughout document.

Preface

This document provides information for designing a custom system carrier board for XTX™ modules. This guide includes reference schematics for the external circuitry required to implement the various XTX™ peripheral functions. This guide also explains how to extend the supported buses and how to add additional peripherals and expansion slots to an XTX™ based system.

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The typical application circuits described in this document may not be suitable for all applications. In particular, additional components may need to be added to these circuits in order to meet specific ESD, EMC or safety isolation requirements. Such regulatory requirements and the techniques for meeting them vary by industry and are beyond the scope of this document.

Intended Audience

This design guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols are used in this design guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
PCI Express (PCIe)	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2 or x4 link.
ExpressCard	A PCMCIA standard built on the latest USB 2.0 and PCI Express buses.
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial-interface standard for hard disks
AC '97 / HDA	Audio CODEC (Coder-Decoder) / High Definition Audio
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
SM Bus	System Management Bus
LVDS	Low-Voltage Differential Signaling
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

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ETX® Concept and XTX™ Extension

The ETX® concept is an off the shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. ETX® modules have a standardized form factor of 95mm x 114mm and have specified pinouts on the four system connectors that remain the same regardless of the vendor. The ETX® module provides most of the functional requirements for any application. These functions include, but are not limited to, graphics, sound, keyboard/mouse, IDE, Ethernet, parallel, serial and USB ports. Four ruggedized connectors provide the carrier board interface and carry all the I/O signals to and from the ETX® module.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly ETX® applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class ETX® modules. Simply unplug one module and replace it with another, no redesign is necessary.

XTX™ is an expansion and continuation of the well-established and highly successful ETX® standard. XTX™ offers the newest I/O technologies on this proven form factor. Now that the ISA bus is being used less and less in modern embedded applications congatec AG offers an array of different features on the X2 connector than those currently found on the ETX® platform. These features include new serial high speed buses such as PCI Express™ and Serial ATA®. All other signals found on connectors X1, X3, and X4 remain the same in accordance to the ETX® standard (Rev. 2.7) and therefore will be completely compatible. If the embedded PC application still requires the ISA bus then an ISA bridge can be implemented on the application specific carrier board or the readily available LPC bus located on the XTX™ module may be used. Contact congatec technical support for details.

Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Certification

congatec AG is certified to DIN EN ISO 9001:2000 standard.

Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

Contents

1 Customer Feedback

The XTX™ Design Guide has been created to help customers when designing XTX™ compliant carrier boards. It should be used in conjunction with the XTX™ Specification, ETX® Specification, ETX® Design Guide as well as any other relevant information with regards to the implementation of the interfaces mentioned within this document.

The guidelines set forth in this document have been carefully thought out by congatec AG engineers and are considered to be the most important factors when designing an XTX™ carrier board. congatec AG is committed to helping customers who are designing XTX™ compliant carrier boards by sharing our expertise and providing the best possible support and documentation. Therefore, we welcome any suggestions our valued customers may have with regards to additional information that should be included in this XTX™ Design Guide. Additionally, we encourage any feedback about the contents of this document with regards to clarity and understanding.

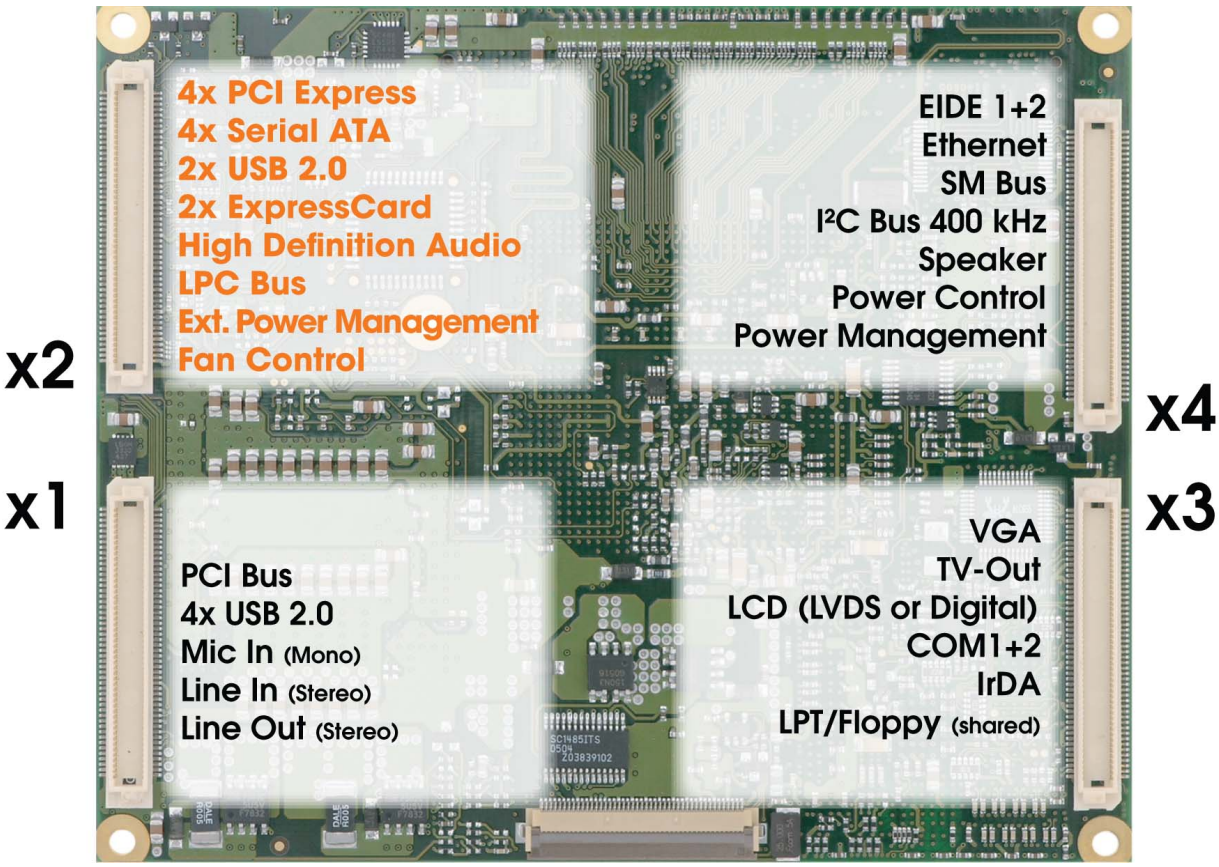
If you have any suggestions about additional content, or any questions about the existing content, contact congatec AG technical support via email at support@congatec.com

2 XTX™ Specification Overview

XTX™ is an ETX® Component SBC Specification extension. XTX™ is fully compliant to the ETX® Specification with the exception of the X2 (ISA bus) connector signal definition. The ISA bus signals on the X2 connector have been replaced by state of the art interface technologies such as:

- PCI Express™
- ExpressCard™
- Serial ATA
- USB 2.0
- Digital Audio Interface (AC'97 or HDA)
- LPC Interface
- Additional control signals

The XTX™ Specification can be downloaded from the XTX™ Standard website (www.xtx-standard.org). A design guide for ETX®, as well as the ETX® Specification, can be found on the ETX® Industrial Group website (www.etx-ig.com).



3 XTX™ Connector X2 Schematics

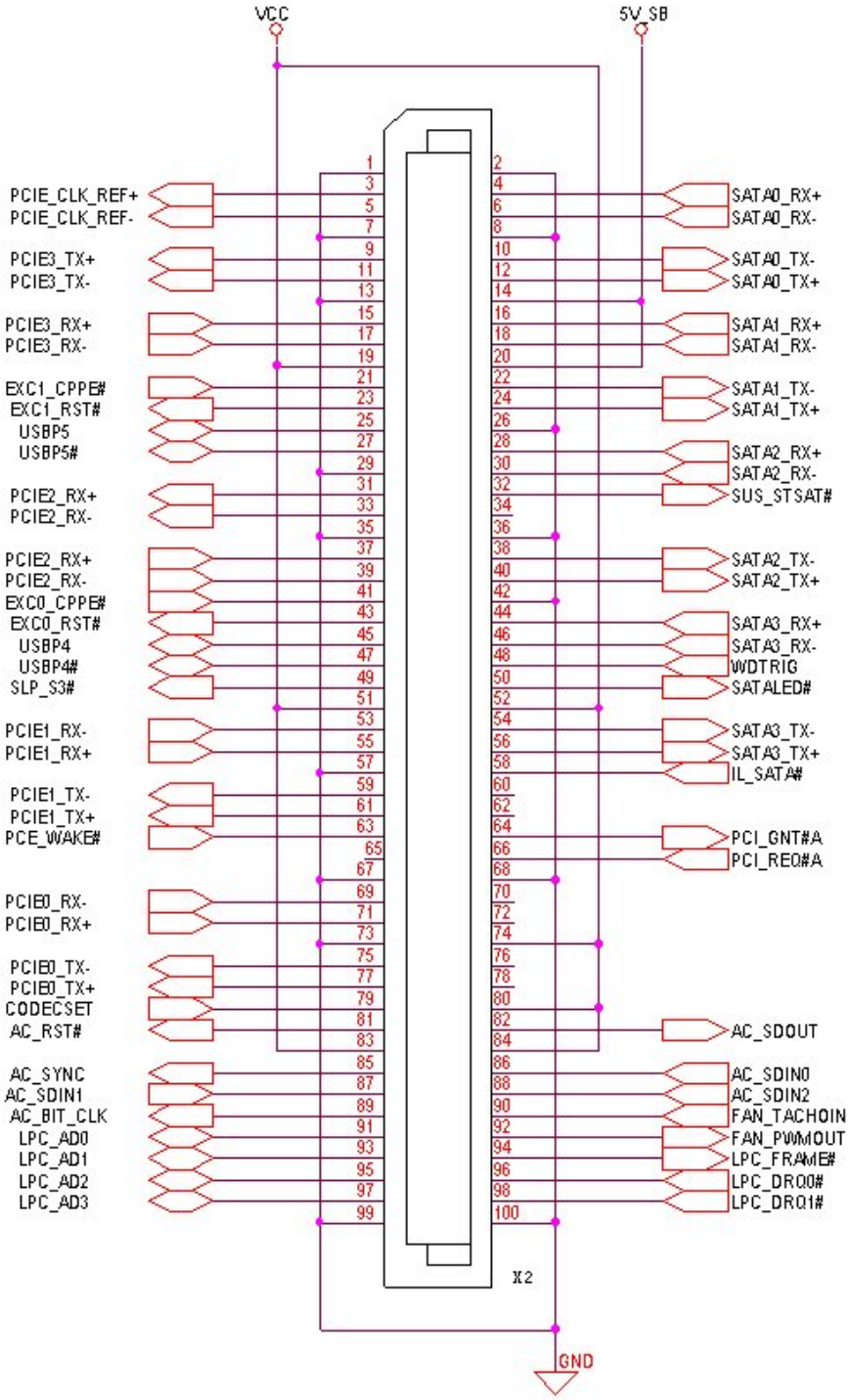


Image 1 XTX™ Connector X2

4 XTX™ Connector X2 Pinout

Table 1 Connector X2 Pinout

Pin	XTX™ Signal	Pin	XTX™ Signal	Pin	XTX™ Signal	Pin	XTX™ Signal
1	GND	2	GND	51	VCC	52	VCC
3	PCIE_CLK_REF+	4	SATA0_RX+	53	PCIE1_RX-	54	SATA3_TX-
5	PCIE_CLK_REF-	6	SATA0_RX-	55	PCIE1_RX+	56	SATA3_TX+
7	GND	8	GND	57	GND	58	IL_SATA#
9	PCIE3_TX+	10	SATA0_TX-	59	PCIE1_TX-	60	PP_TPM
11	PCIE3_TX-	12	SATA0_TX+	61	PCIE1_TX+	62	N.C.
13	GND	14	5V_SB	63	PCE_WAKE#	64	PCI_GNT#A
15	PCIE3_RX+	16	SATA1_RX+	65	SLP_S5#	66	PCI_REQ#A
17	PCIE3_RX-	18	SATA1_RX-	67	GND	68	GND
19	VCC	20	5V_SB	69	PCIE0_RX-	70	N.C.
21	EXC1_CPPE#	22	SATA1_TX-	71	PCIE0_RX+	72	N.C.
23	EXC1_RST#	24	SATA1_TX+	73	GND	74	VCC
25	USBP5	26	GND	75	PCIE0_TX-	76	N.C.
27	USBP5#	28	SATA2_RX+	77	PCIE0_TX+	78	N.C.
29	GND	30	SATA2_RX-	79	CODECSET	80	VCC
31	PCIE2_TX+	32	SUS_STAT#	81	AC_RST#	82	AC_SDOUT
33	PCIE2_TX-	34	N.C.	83	VCC	84	VCC
35	GND	36	GND	85	AC_SYNC	86	AC_SDIN0
37	PCIE2_RX+	38	SATA2_TX-	87	AC_SDIN1	88	AC_SDIN2
39	PCIE2_RX-	40	SATA2_TX+	89	AC_BIT_CLK	90	FAN_TACHOIN
41	EXC0_CPPE#	42	GND	91	LPC_AD0	92	FAN_PWMOUT
43	EXC0_RST#	44	SATA3_RX+	93	LPC_AD1	94	LPC_FRAME#
45	USBP4	46	SATA3_RX-	95	LPC_AD2	96	LPC_DRQ0#
47	USBP4#	48	WDTRIG	97	LPC_AD3	98	LPC_DRQ1#
49	SLP_S3#	50	SATALED#	99	GND	100	GND

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5 Signal Descriptions

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

The following terminology is used to describe the signals types in the I/O columns for the tables located below.

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector Output Pin
I/O	Bi-directional Input/Output Pin

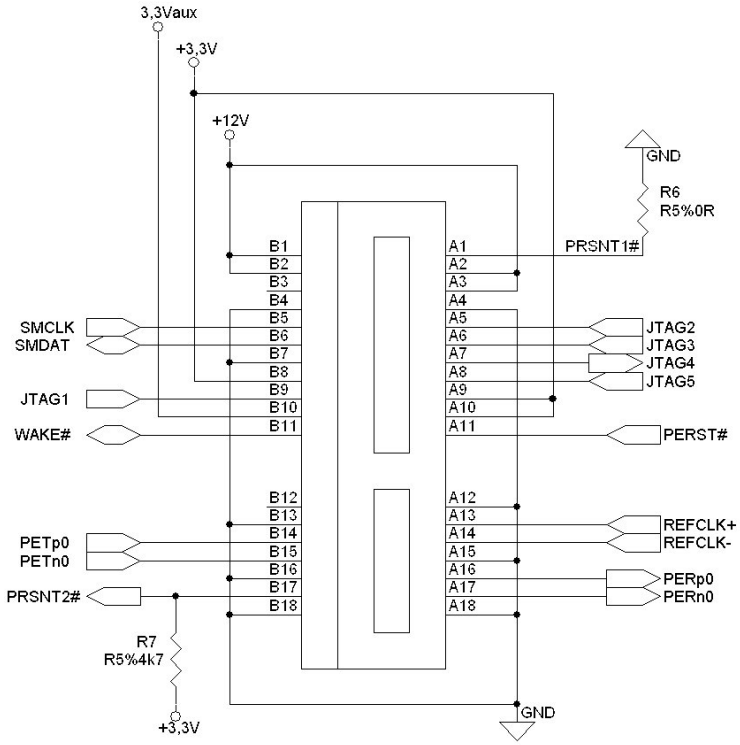
5.1 PCI Express™ (PCIe)

The PCI Express interface consists of up to 4 lanes, each with a receive and transmit differential signal pair designated from PCIE0_RX (+ and -) to PCIE3_RX (+ and -) and correspondingly from PCIE0_TX (+ and -) to PCIE3_TX (+ and -).

Table 2 PCI Express Signal Description (Signals on XTX™ Connector X2)

Signal	Pin#	Description	I/O	Comment
PCIE0_RX+ PCIE0_RX-	71 69	PCI Express channel 0, Receive Input differential pair.	I	
PCIE0_TX+ PCIE0_TX-	77 75	PCI Express channel 0, Transmit Output differential pair.	O	
PCIE1_RX+ PCIE1_RX-	55 53	PCI Express channel 1, Receive Input differential pair.	I	
PCIE1_TX+ PCIE1_TX-	61 59	PCI Express channel 1, Transmit Output differential pair.	O	
PCIE2_RX+ PCIE2_RX-	37 39	PCI Express channel 2, Receive Input differential pair.	I	
PCIE2_TX+ PCIE2_TX-	31 33	PCI Express channel 2, Transmit Output differential pair.	O	
PCIE3_RX+ PCIE3_RX-	15 17	PCI Express channel 3, Receive Input differential pair.	I	
PCIE3_TX+ PCIE3_TX-	9 11	PCI Express channel 3, Transmit Output differential pair.	O	
PCIE_CLK_REF+ PCIE_CLK_REF-	3 5	PCI Express Reference Clock for Lanes 0 to 3.	O	
PCE_WAKE#	63	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I	

a:



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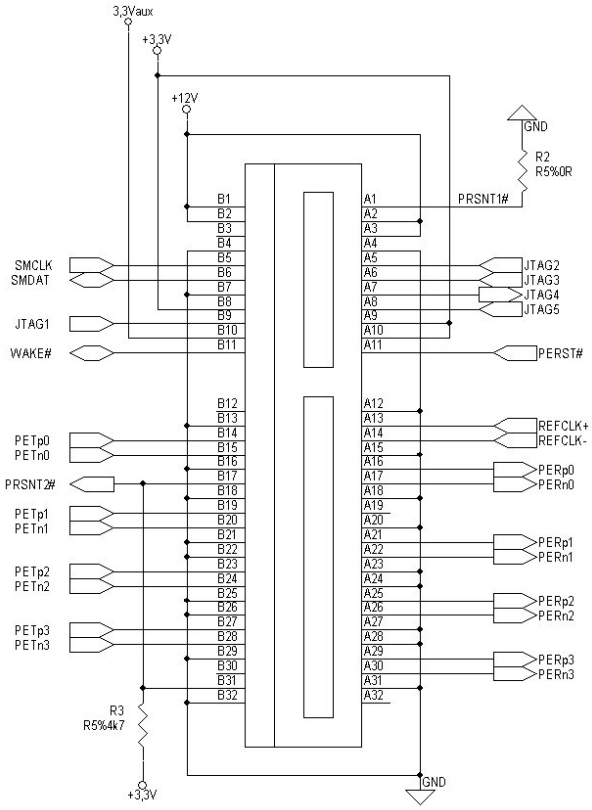


Image 2 PCI Express x1 (a) and x4 (b) Connector Diagrams

5.1.1 PCI Express x1 and x4 Connector

Signal fields in Table 3 that do not have any light grey shading describe the pinout for the PCI Express x1 slot (1 PCIe Lane) and the signal fields marked with light grey indicate the additional signals needed on a PCI Express x4 connector (4 PCIe Lanes).

Table 3 PCI Express x1 and x4 Connector Pinout and Signal Descriptions

Pin	Signal	Description	Pin	Signal	Description
1B	+12V	12V power	1A	PRSNT1#*	Hot-Plug presence detected
2B	+12V	12V power	2A	+12V	12V power
3B	RSVD	Reserved	3A	+12V	12V power
4B	GND	Ground	4A	GND	Ground
5B	SMCLK*	SMBus Clock (XTX™ connector X4, pin 23)	5A	JTAG2*	TCK - Boundary Scan Test Clock
6B	SMDAT*	SMBus Data (XTX™ connector X4, pin 24)	6A	JTAG3*	TDI – Boundary Scan Test Data Input
7B	GND	Ground	7A	JTAG4*	TDO - Boundary Scan Test Data Output
8B	+3.3V	3.3V power	8A	JTAG5*	TMS - Boundary Scan Test Mode Select
9B	JTAG1*	TRST# - Boundary Scan Test Reset	9A	+3.3V	3.3V power
10B	+3.3Vaux*	3.3V auxiliary power	10A	+3.3V	3.3V power
11B	WAKE#*	Link Reactivation	11A	PERST#*	Reset
		Mechanical Key			
12B	RSVD	Reserved	12A	GND	Ground
13B	GND	Ground	13A	REFCLK+*	Reference Clock differential pair positive signal
14B	PETp0	Transmitter differential pair positive Signal, Lane 0	14A	REFCLK-*	Reference Clock differential pair negative signal
15B	PETn0	Transmitter differential pair negative signal, Lane 0	15A	GND	Ground
16B	GND	Ground	16A	PERp0	Receiver differential pair positive signal, Lane 0
17B	PRSNT2#*	Hot-Plug presence detect	17A	PERn0	Receiver differential pair negative signal, Lane 0
18B	GND	Ground	18A	GND	Ground
19B	PETp1	Transmitter differential pair positive signal, Lane 1	19A	RSVD	Reserved
20B	PETn1	Transmitter differential pair negative signal, Lane 1	20A	GND	Ground
21B	GND	Ground	21A	PERp1	Receiver differential pair positive signal, Lane 1
22B	GND	Ground	22A	PERn1	Receiver differential pair negative signal, Lane 1
23B	PETp2	Transmitter differential pair positive signal, Lane 2	23A	GND	Ground

Pin	Signal	Description	Pin	Signal	Description
24B	PETn2	Transmitter differential pair negative signal, Lane 2	24A	GND	Ground
25B	GND	Ground	25A	PERp2	Receiver differential pair positive signal, Lane 2
26B	GND	Ground	26A	PERn2	Receiver differential pair negative signal, Lane 2
27B	PETp3	Transmitter differential pair positive signal, Lane 3	27A	GND	Ground
28B	PETn3	Transmitter differential pair negative signal, Lane 3	28A	GND	Ground
29B	GND	Ground	29A	PERp3	Receiver differential pair positive signal, Lane 3
30B	GND	Ground	30A	PERn3	Receiver differential pair negative signal, Lane 3
31B	PRSTN2#*	Hot-Plug presence detected	31A	GND	Ground
32B	GND	Ground	32A	RSVD	Reserved

Note

** Auxiliary signals. These signals are not required by the PCI Express Architecture.*

5.1.2 PCI Express Clock Signal

In an application where more than one PCI Express slot or device is needed, the PCI Express Reference Clock signal must be buffered. 'Image 3' shows an example implementing the ICS9DB106 (6 Output PCI Express Buffer with CLKREQ# Function) from *Integrated Circuit Systems (ICS)* (*http://www.icst.com*). This device is also used on congatec's conga-XEVAL evaluation carrier board.

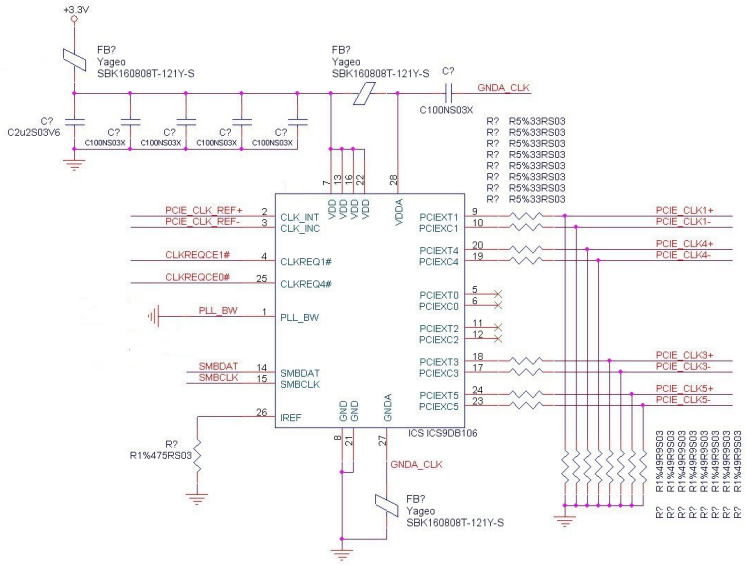


Image 3 PCI Express Clock Circuit

Routing Considerations for PCI Express

See section 7.1 'PCI Express Trace Routing Guidelines' and the XTX™ specification for more information about this subject.

5.2 Universal Serial Bus

Table 4 USB Signal Descriptions (Signals on XTX™ Connector X2)

Signal	Pin	Description	I/O	Comment
USBP4	45	Universal Serial Bus Port 4 positive differential signal.	I/O	
USBP4#	47	Universal Serial Bus Port 4 negative differential signal.	I/O	
USBP5	25	Universal Serial Bus Port 5 positive differential signal.	I/O	
USBP5#	27	Universal Serial Bus Port 5 negative differential signal.	I/O	

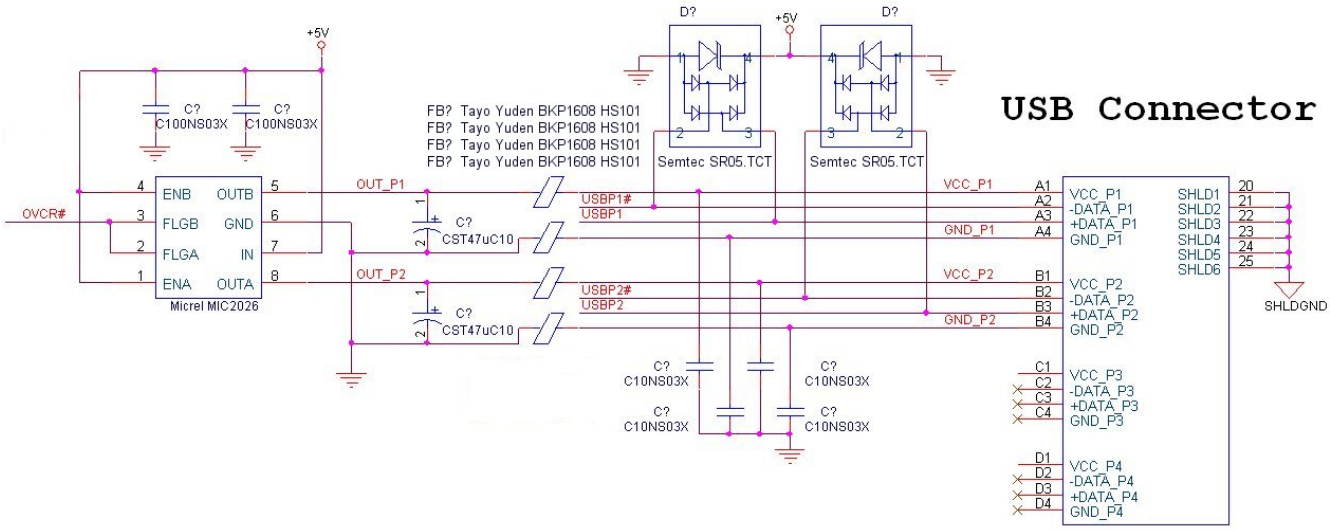


Image 4 USB Circuit Schematics

The power distribution for the two USB ports in the example above is handled by a Micrel MIC2026 Dual Channel Power Distribution Switch (*http://www.micrel.com*). This device is also used on congatec's conga-XEVAL evaluation carrier board.

The signal OVCR# (USB over-current detect signal) used in 'Image 4' can be found on the ETX® connector X4, pin 19 (see ETX® Specification).

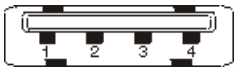


Image 5 USB Connector (Type A, female, front view)

Table 5 USB Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	VCC	+5V Power Supply	3	+DATA	Universal Serial Bus Data, positive differential signal.
2	-DATA	Universal Serial Bus Data, negative differential signal.	4	GND	Ground

Routing Considerations for USB

See section 7.2 'USB 2.0 Trace Routing Guidelines' and the XTX™ specification for more information about this subject.

5.3 ExpressCard™

ExpressCard™

XTX™ modules offer the optional support for two ExpressCard slots. ExpressCard is the successor of PCMCIA and PC Cards. ExpressCard takes advantage of the scalable, high-bandwidth serial PCI Express and USB 2.0 interfaces.

Table 6 ExpressCard Signal Descriptions (Signals on XTX™ Connector X2)

Signal	Pin	Description	I/O	Comment
EXEC0_CPPE#	41	ExpressCard capable card request, Slot 1	I	
EXEC1_CPPE#	21	ExpressCard capable card request, Slot 2	I	
EXEC0_RST#	43	ExpressCard Reset, Slot 1	O	
EXEC1_RST#	23	ExpressCard Reset, Slot 2	O	

Image 6 on the following page displays an example of how an ExpressCard slot can be connected to a XTX™ embedded module. Power management for the ExpressCard slot is handled by a Texas Instruments TPS2231 Power Interface Switch (*http://www.ti.com*) and the same solution has been implemented on congatec's conga-XEVAL evaluation carrier board.

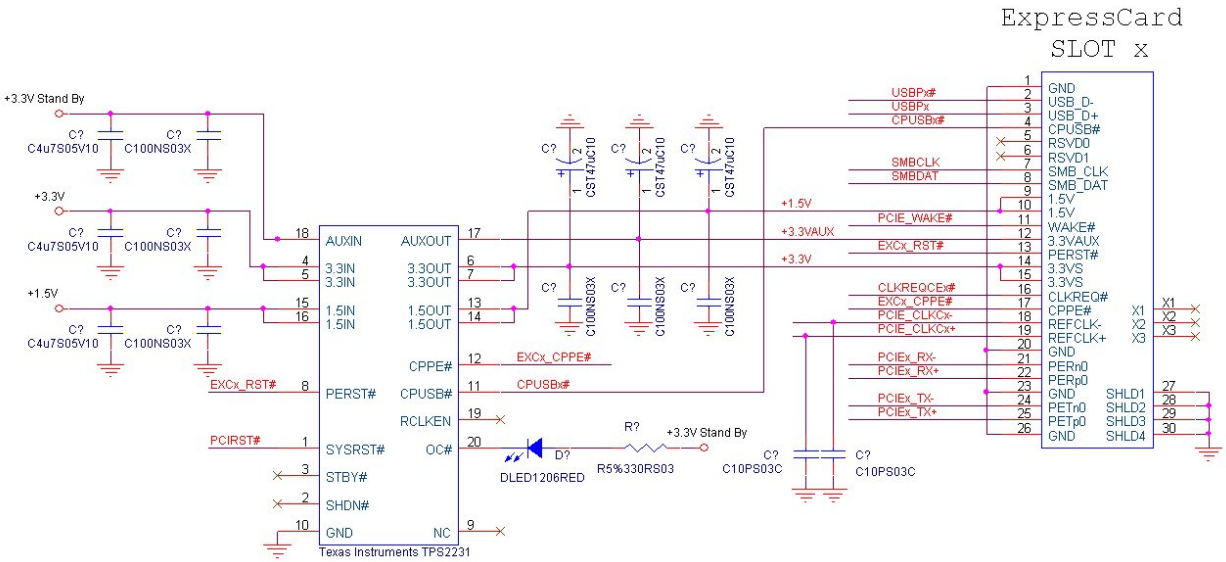


Image 6 ExpressCard Schematics

Table 7 ExpressCard Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	14	+3.3V	Primary voltage source, 3.3V
2	USB_D-	USB Serial Data Interface differential pair, negative signal	15	+3.3V	Primary voltage source, 3.3V
3	USB_D+	USB Serial Data Interface differential pair, positive signal	16	CLKREQ#	Request that REFCLK be enabled
4	CPUSB#	USB Interface presence detect	17	CPPE#	PCI Express interface presence detect
5	RSVD0	Reserved	18	REFCLK-	PCI Express reference clock differential pair, negative signal
6	RSVD1	Reserved	19	REFCLK+	PCI Express reference clock differential pair, positive signal
7	SMBCLK	System Management Bus Clock (Optional Signal)	20	GND	Ground
8	SMBDATA	System Management Bus Data (Optional Signal)	21	PERn0	PCI Express Receiver differential pair negative signal
9	+1.5V	Secondary voltage source, 1.5V	22	PERp0	PCI Express Receiver differential pair positive signal
10	+1.5V	Secondary voltage source, 1.5V	23	GND	Ground
11	WAKE#	Request that the host interface return to full operation and respond to PCI Express	24	PETn0	PCI Express Transmitter differential pair negative signal
12	+3.3VAUX	Auxiliary voltage source, 3.3V	25	PETp0	PCI Express Transmitter differential pair positive signal
13	PERST#	PCI Express Reset	26	GND	Ground

Note

The PCI Express Reference Clock used for ExpressCard slots must be buffered as shown in section 5.1.2 'PCI Express Clock Signal'.

In addition to the PCI Express and USB signals, the example displayed in 'Image 6' uses the following signals that are not located on the XTX™ connector X2.

Signal	XTX™ Connector	Pin	Description
SMBCLK	X4	23	System Management Bus Clock Signal
SMBDAT	X4	24	System Management Bus Data Signal
PCIRST#	X1	93	PCI Bus Reset
CLKREQCEx#	-	-	Request for PCI Express Reference Clock. See section 5.1.2 'PCI Express Clock Signal' for details.

Routing Considerations for PCI Express and USB

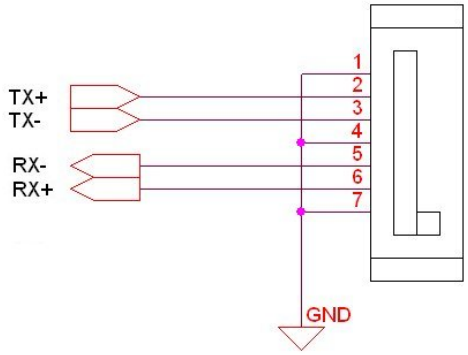
See section 7.1 'PCI Express Trace Routing Guidelines', 7.2 'USB 2.0 Trace Routing Guidelines' and the XTX™ specification for more information about this subject.

5.4 Serial ATA (SATA)

Table 8 Serial ATA Signal Descriptions (Signals on XTX™ connector X2)

Signal	Pin	Description	I/O	Comment
SATA0_RX+ SATA0_RX-	4 6	Serial ATA channel 0 Receive Input differential pair.	I	
SATA0_TX+ SATA0_TX-	12 10	Serial ATA channel 0 Transmit Output differential pair.	O	
SATA1_RX+ SATA1_RX-	16 18	Serial ATA channel 1 Receive Input differential pair.	I	
SATA1_TX+ SATA1_TX-	24 22	Serial ATA channel 1 Transmit Output differential pair.	O	
SATA2_RX+ SATA2_RX-	28 30	Serial ATA channel 2 Receive Input differential pair.	I	
SATA2_TX+ SATA2_TX-	40 38	Serial ATA channel 2 Transmit Output differential pair.	O	
SATA3_RX+ SATA3_RX-	44 46	Serial ATA channel 3 Receive Input differential pair.	I	
SATA3_TX+ SATA3_TX-	56 54	Serial ATA channel 3 Transmit Output differential pair.	O	
IL_SATA#	58	Serial ATA Interlock Switch Input.	I	
SATALED#	50	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC	

S-ATA DATA Connector



S-ATA DATA and Power Connector

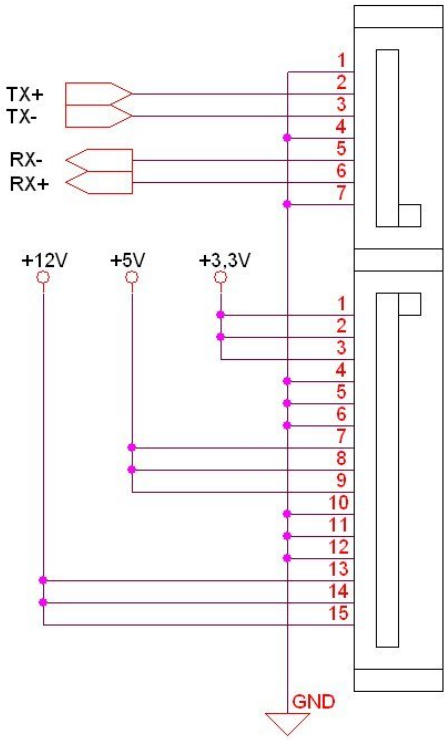


Image 7 Serial ATA Connector Diagram

Table 9 Serial ATA Data Connector Pinout and Signal Description

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	5	RX-	Receiver differential pair negative signal
2	TX+	Transmitter differential pair positive signal	6	RX+	Receiver differential pair positive signal
3	TX-	Transmitter differential pair negative signal	7	GND	Ground
4	GND	Ground			

Table 10 Serial ATA Power Connector Pinout and Signal Description

Pins	Signal	Description	Pins	Signal	Description
1 2 3	+3.3V	3.3V power supply	10 11 12	GND	Ground
4 5 6	GND	Ground	13 14 15	+12V	12V power supply
7 8 9	+5V	5V power supply			

Routing Considerations for Serial ATA

See section 7.3 'Serial ATA Trace Routing Guidelines' and the XTX™ specification for more information about this subject.

5.5 Low Pin Count Interface LPC

Table 11 LPC Interface Signal Descriptions (Signals on XTX™ connector X2)

Signal	Pin	Description	I/O	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	91 93 95 97	Multiplexed command, address and data	I/O	
LPC_FRAME#	94	Frame: Indicates start of a new cycle or termination of a broken cycle.	O	
LPC_DRQ0# LPC_DRQ1#	96 98	Encoded DMA/Bus master request	I	

The LPC devices used on the carrier board have to be clocked by one of the PCI Bus clocks provided by the XTX™ module's connector interface. The LPC devices should use the PCI Reset signal as a reset input. The clocks and reset can be found on the XTX™ module connectors listed below in table 12.

The PCI clock implementation required for the LPC device should follow the routing guidelines defined in both the ETX® Specification and ETX® Design Guide. The PCI clock signal on the carrier board should have a trace length of about 8.7 inches and be routed with a trace impedance in the range of 60 to 70Ω.

Only one PCI/LPC device should be driven per PCI clock signal and there are a total of four PCI clock signals available. If more than four PCI clock signals are required then a zero delay buffer, for example a Cypress 2305 (*http://www.cypress.com*), can be used to expand the number of clock lines.

Table 12 PCI Clocks and Reset Signal Descriptions (Signal locations)

Signal	XTX™ Connector	Pin	Description
PCICLK1	X1	7	PCI Clock output 1
PCICLK2	X1	8	PCI Clock output 2
PCICLK3	X1	3	PCI Clock output 3
PCICLK4	X1	4	PCI Clock output 4
PCIRST#	X1	93	PCI Bus Reset
SERIRQ	X1	21	Serial Interrupt request

5.5.1 Application Example: LPC Super I/O Controller

The XTX™ module's congatec Embedded BIOS contains built-in support for an external LPC Super I/O controller, which can be mounted on the XTX™ carrier board. This LPC Super I/O controller must be a Winbond W83627HG (*http://www.winbond-usa.com*) and it has to reside at LPC Bus address 4Eh. The implementation of this device on the XTX™ carrier board will provide two additional COM ports (COM3 and COM4) as well as one additional parallel port (LPT2). The other functions of this controller are not supported.

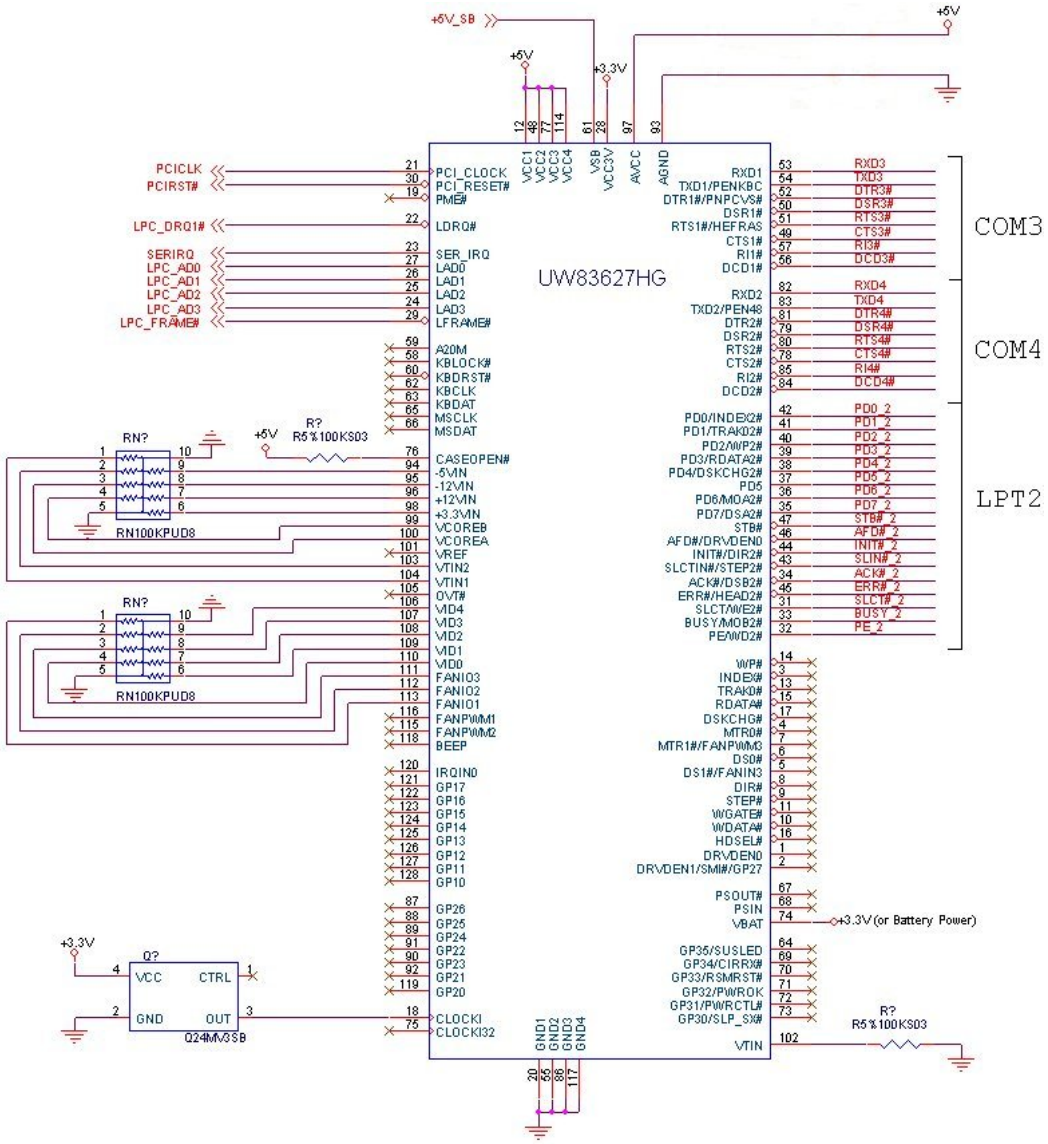


Image 8 Schematics of LPC Super I/O

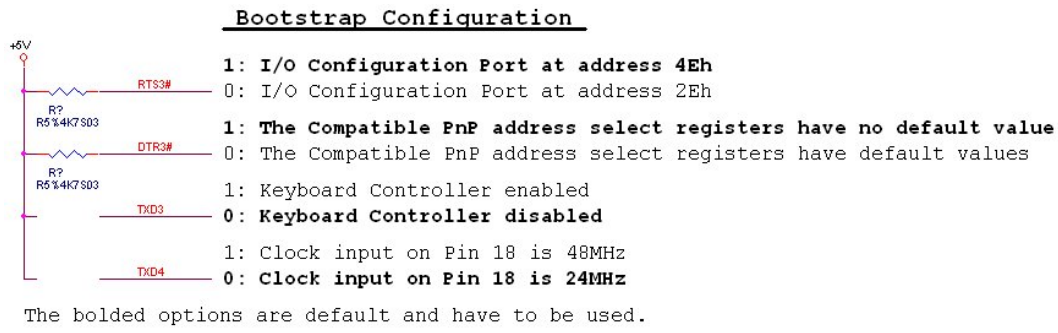


Image 9 Schematics of LPC Super I/O Configuration

5.5.2 Application Example: Serial and Parallel Port Circuit

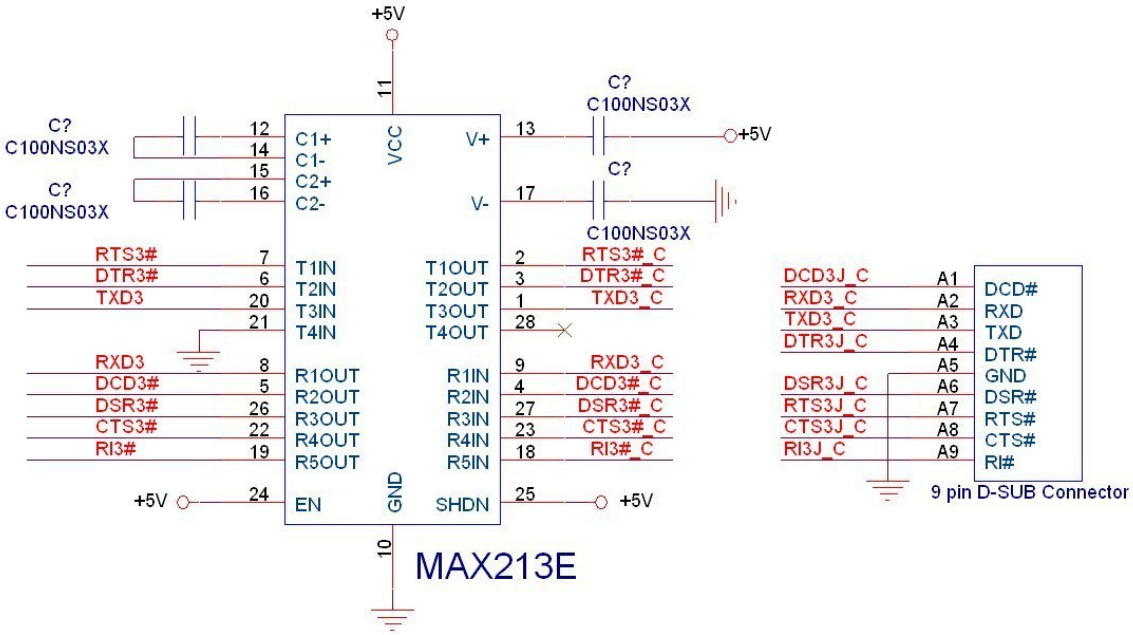


Image 10 RS232 Transceiver Circuit COM3

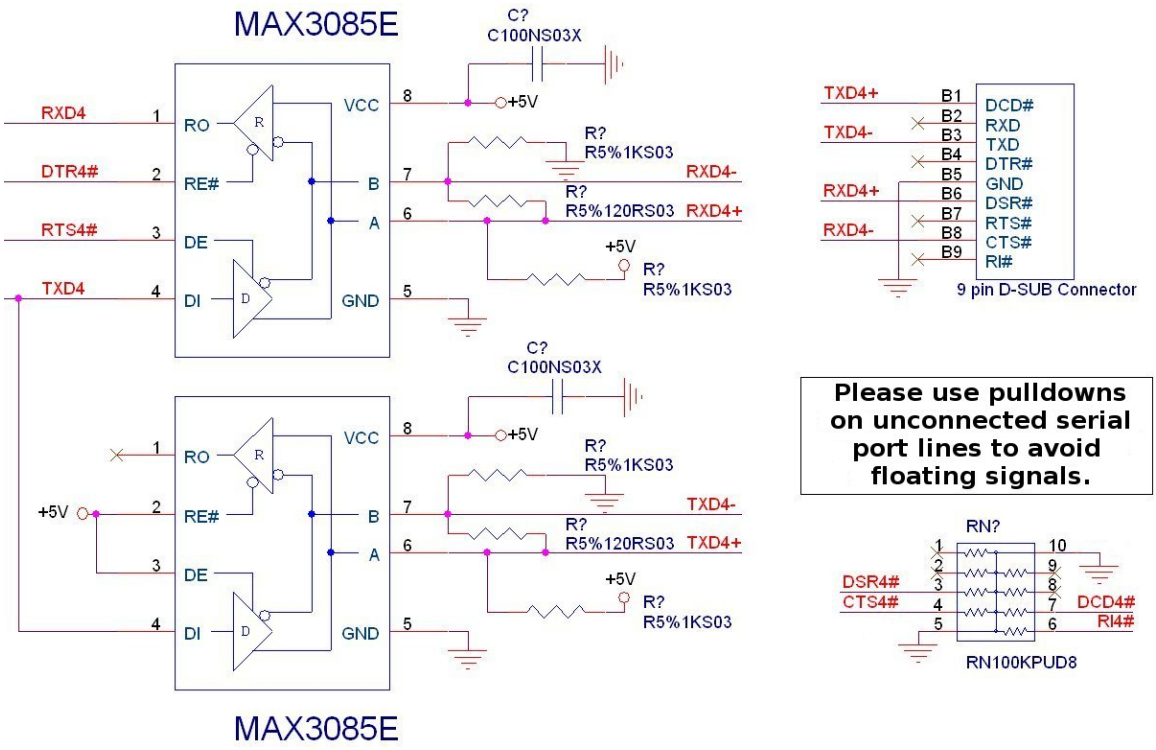


Image 11 RS485/RS422 Transceiver Circuit COM4

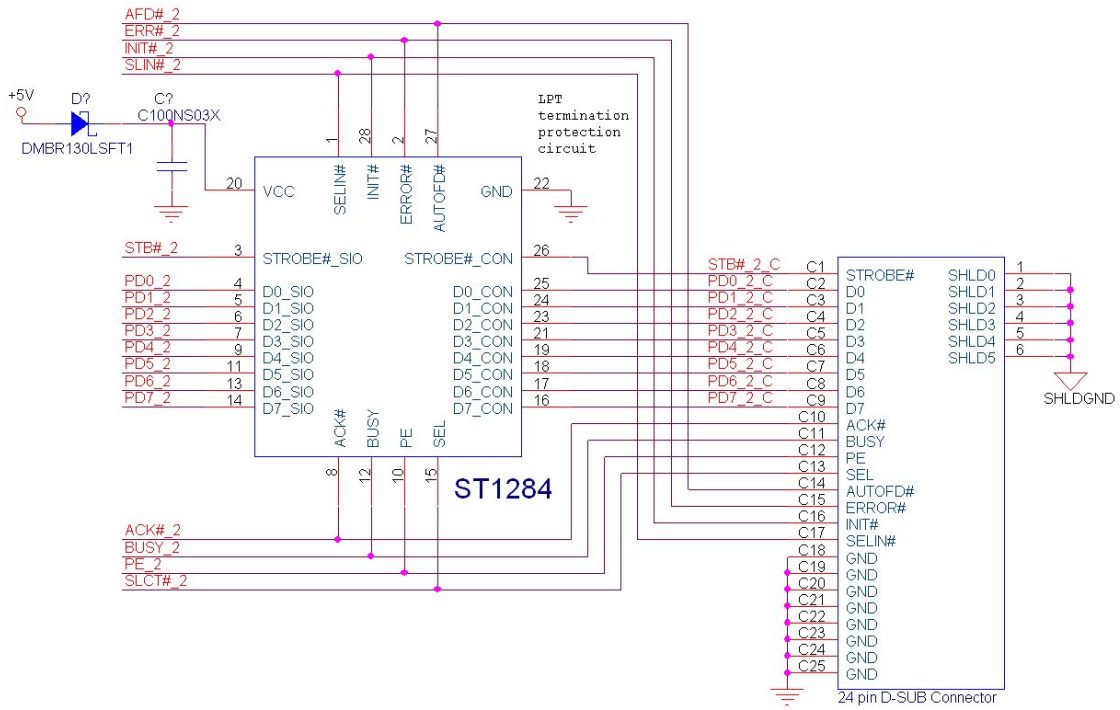


Image 12 Parallel Port Protection and Termination Circuit on LPT2

5.6 Audio Codec (AC'97/HDA)

XTX™ Modules support Audio Codec '97 and/or High Definition Audio (HDA) Digital Interface (AC-link) specifically designed for implementing audio and modem I/O functionality in a PC system. Information about which interface is supported on the XTX™ module can be found in the corresponding XTX™ module's User's Guide.

On XTX™ modules that support the AC'97 Digital Interface only, it is not possible to use HDA codecs. The High Definition Audio architecture (formerly called 'Azalia') and specification must be considered as an entirely separate specification from AC'97, which in turn means no backwards compatibility.

Some XTX™ modules support both the AC'97 and HDA Interface. In the XTX™ module's BIOS Setup Program it's possible to choose which interface should be utilized. Only audio codecs that match this setting will work properly. AC'97 and High Definition Audio codecs cannot be mixed on the same link or behind the same controller.

5.6.1 Audio Codec on XTX™ Modules

The onboard audio function on XTX™ modules is provided through an AC'97 codec. This leads to some important items that must be considered when designing AC'97 or HDA codecs on the carrier board.

The AC'97 codec on the XTX™ module is connected as primary codec with ID00 and uses data input line 2 (SDATA_IN2). Up to two additional codecs (secondary and tertiary) can be connected to the XTX™ module.

When a primary codec is to be used on the XTX™ carrier board, the codec on the XTX™ module must be disabled. This can be done with the XTX™ signal called CODECSET. If this signal is pulled to 3.3V on the carrier board, the XTX™ onboard codec will be disabled. If you choose to implement HDA codecs on the XTX™ carrier board, the codec on the XTX™ module can not be used and must be disabled.

Connect the primary codec to data-in signal (AC_SDIN2) and ensure that the clock input from the codec is connected to the AC'97/HDA Interface.

Clocking of the AC'97/HDA interface is provided from the primary codec on the link via BIT_CLK and is derived from a 24.576 MHz crystal or crystal oscillator. Refer to the primary codec vendor for crystal or crystal oscillator requirements.

congatec AG recommends the use of the VIA VT1616 (*http://www.via.com.tw*) AC'97 audio codec for XTX™ carrier board designs. If you choose to use a different primary AC'97 codec other than the one recommended, or if you wish to utilize secondary and tertiary codecs, contact congatec technical support for assistance before implementation.

Image 13 on the following page provides an overview of the XTX™ carrier board codec connection possibilities.

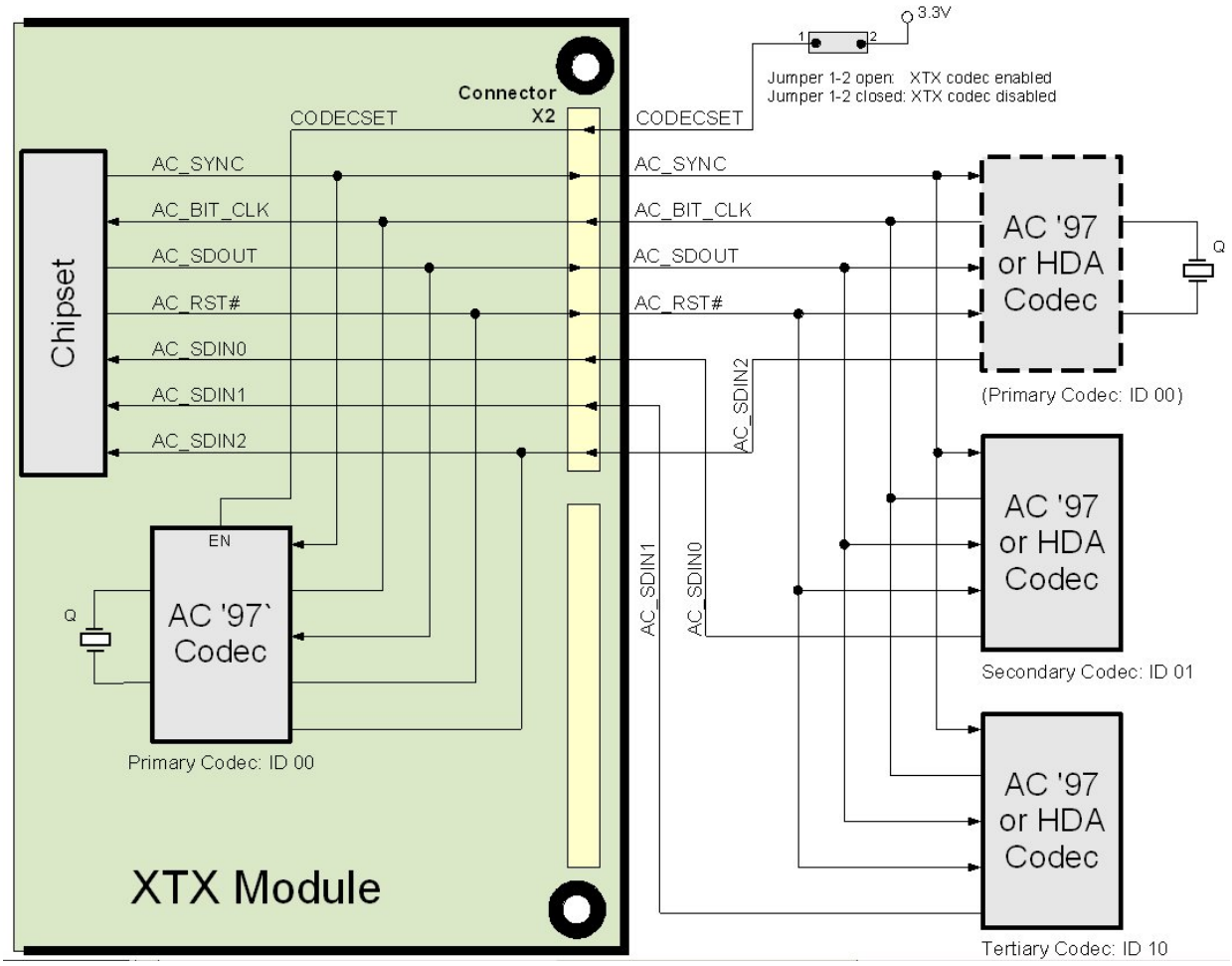


Image 13 AC'97 Audio Codec

Table 13 Audio Codec Signal Descriptions (Signals on XTX™ connector X2)

Signal	Pin	Description	I/O	Comment
AC_RST#	81	CODEC Reset	O	
AC_SYNC	85	Serial Bus Synchronization.	O	
AC_BIT_CLK	89	12.228 MHz Serial Bit Clock from CODEC.	O	
AC_SDOUT	82	Audio Serial Data Output to CODEC.	O	
AC_SDIN0 AC_SDIN1 AC_SDIN2	86 87 88	Audio Serial Data Input from CODEC0..CODEC2.	I	
CODECSET	79	Disable onboard Audio Codec.	I	

5.6.2 AC'97/HDA Placement and Routing Guidelines

The implementation of proper component placement and routing techniques will help to ensure that the maximum performance available from the codec is achieved. Routing techniques that should be observed include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the carrier board. This includes split planes and the proper routing of signals not associated with the audio section.

The following is a list of basic recommendations:

- Traces must be routed with a target impedance of 55Ω with an allowed tolerance of ± 15%.
- Ground return paths for the analog signals must be given special consideration.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Locate the analog and digital signals as far as possible from each other.
- Partition the carrier board with all analog components grouped together in one area and all digital components in another.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Provide separate analog and digital ground planes with the digital components over the digital ground plane and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Route analog power and signal traces over the analog ground plane.
- Route digital power and signal traces over the digital ground plane.
- Position the bypassing and decoupling capacitors close to the IC pins, or position the capacitors for the shortest connections to pins, with wide traces to reduce impedance.
- Do not completely isolate the analog/audio ground plane from the rest of the carrier board ground plane. Provide a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main carrier board ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.

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5.7 Miscellaneous Signals

Table 14 Miscellaneous Signal Descriptions (Signals on XTX™ connector X2)

Signal		Description	I/O	Comment
GND	1, 2, 7, 8 13, 26, 29 35, 36, 42, 57 67, 68, 73, 99, 100	Ground. All GND pins should be connected to the carrier board ground plane.	-	
5V_SB	14 20	Additional power input for the internal suspend and power-control circuitry. This signal is connected to ETX®-Connector X4/Pin3. Refer to ETX® Specification for further details.	I	
VCC	19, 51, 52 74, 80, 83, 84	+5V Power Input. All VCC pins should be connected to the carrier board +5V power plane.	I	
SUS_STAT#	32	Suspend Status: indicates that the system will be entering a low power state soon.	O	
SLP_S3#	49	S3 Sleep Control: This signal shuts off power to all non-critical systems when in S3 (Suspend to Ram), S4 or S5 states.	O	
SLP_S5#	65	S5 Sleep Control: This signal shuts off power to all non-critical systems when in S5 (Soft Off) state.	O	
PCI_GNT#A	64	reserved	O	
PCI_REQ#A	66	reserved	I	
FAN_PWMOUT	92	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	OC	
FAN_TACHOIN	90	Fan tachometer input (0 to +5V amplitude)	I	
WDTRIG	48	Watch Dog Trigger signal.	I	
PP_TPM	60	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I	

5.7.1 Fan Control Circuit

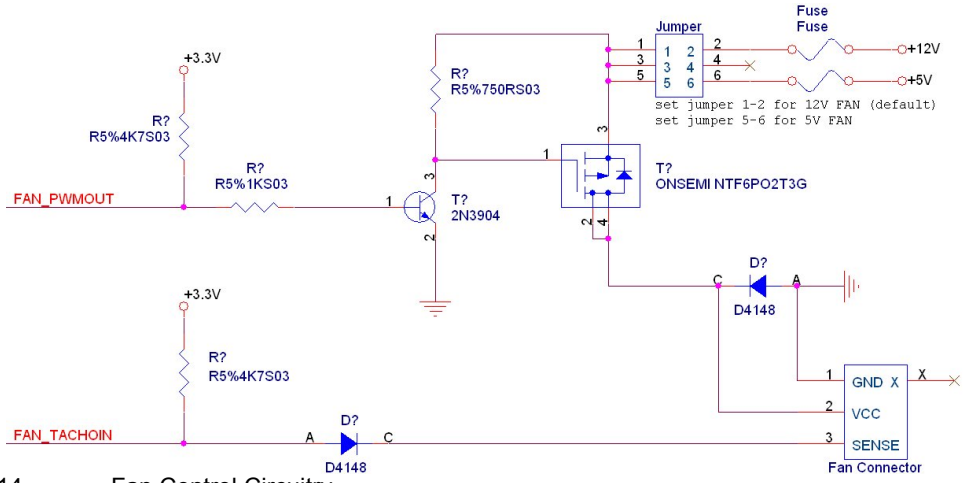

Image 14 Fan Control Circuitry

6 Layout Design Constraints

This chapter provides routing guidelines for layout and design of a printed circuit board using high-speed interfaces such as PCI Express, Serial ATA and USB 2.0. The signal integrity rules for high-speed interfaces need to be considered. In fact, it is highly recommended that the board design be simulated to determine optimum layout for signal integrity and quality.

Keep in mind that this document can only point to the most important issues that should be considered when designing an XTX™ carrier board. The designer has to take into account the corresponding information (specification, design guidelines, ect.) contained in the documentation for each interface that is to be implemented on their carrier board.

Note

For more information about PCB design considerations we recommend you refer to the book "PCI Express Electrical Interconnect Design" available form Intel (http://www.intel.com/intelpress/) ISBN 0-9743649-9-1.

6.1 Microstrip or Stripline

Either edge-coupled microstrip, edge-coupled stripline, or broad-side striplines are recommended for designs with differential signals.

Designs with microstrip lines offer the advantage that a lower number of layers can be used. Also, with microstrip lines it may be possible to route from a connector pad to the device pad without any via. This provides better signal quality on the signal path that connects devices. A limitation of microstrip lines is that they can only be routed on the two outside layers of the PCB, thus routing channel density is limited.

Stripline may be either edge-coupled or broad-side coupled lines. Stripline designs provide additional shielding since they are embedded in the board stack and are typically sandwiched between ground and power planes. This reduces radiation and coupling of noise onto the lines. Striplines have the disadvantage that they require the use of vias to connect to them.

6.2 Printed Circuit Board Stackup Example

It is recommended to use PCB's with at least a 4 layer stackup where the impedance controlled layer 1 (top layer) is used for differential signals and layer 4 (bottom layer) for other periodic signals (CMOS/TTL). The dedicated power planes (layer 2 – GND and layer 3 – VCC) are typically required for high-speed designs. The solid ground plane is necessary to establish a controlled (known) impedance for the transmission line interconnects. A narrow spacing between power and ground planes will additionally create an excellent high frequency bypass capacitance.

The following example shows a four layer PCB stackup using microstrip trace routing.

A good rule to follow for microstrip designs is to keep S < W and S < H ("H" = space

between differential signal layers and the reference plane). The best practice is to use the closest spacing, “S,” allowed by your PCB vendor and then adjust trace widths, “W,” to control differential impedance.

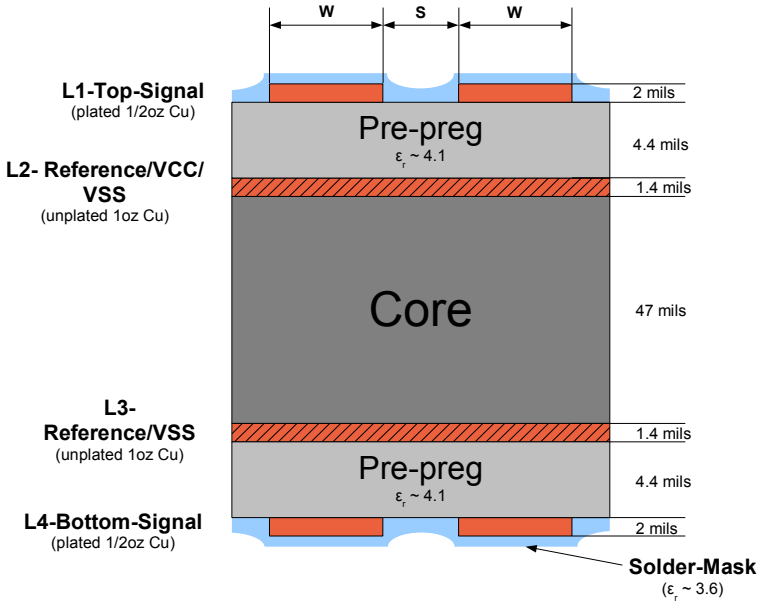

Image 15 4 Layer PCB – Microstrip Routing

For stripline routing, a PCB stackup of at least 6 layers is necessary. The internal layers (L3 and L4) can be used for routing differential signals as stripline traces while the outer layers (L1 and L6) can be used for microstrip routing.

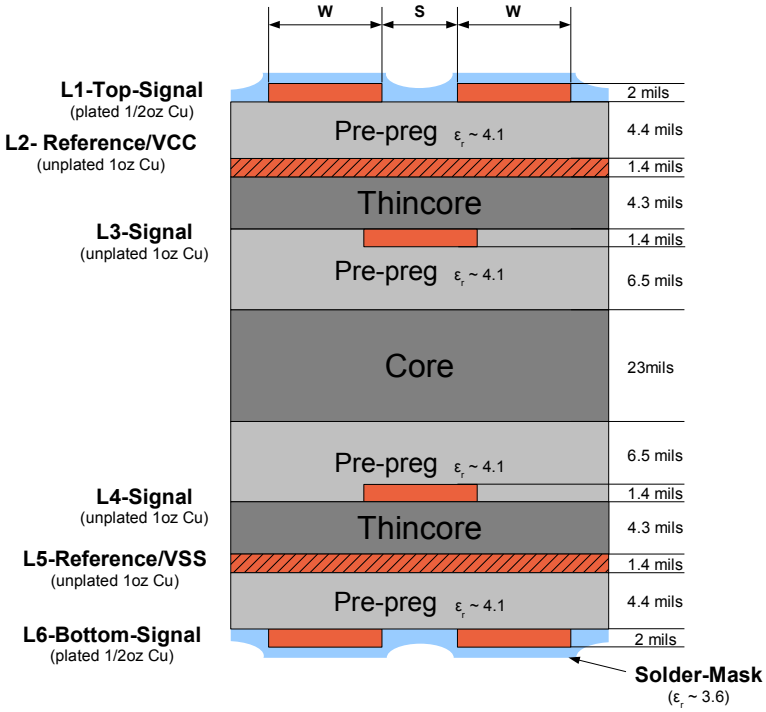

Image 16 6 Layer PCB – Stripline and microstrip routing

7 General Considerations for High-Speed Differential Interfaces

The following is a list of suggestions for designing with high-speed differential signals. They should help to implement these interfaces easily in a cost efficient way while shortening development time and provide maximum XTX™ carrier board performance.

- Use controlled impedance PCB traces that match the specified differential impedance.
- Keep the trace lengths of the differential signal pairs as short as possible.
- The differential signal pair traces should be trace-length matched and the maximum trace-length mismatch should not exceed the specified values. Match each differential pair per segment.
- Maintain parallelism and symmetry between differential signals with the trace spacing needed to achieve the specified differential impedance.
- Maintain maximum possible separation between the differential pairs and any high-speed clocks/periodic signals (CMOS/TTL) and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).
- Route differential signals on the signal layer nearest to the ground plane using a minimum of vias and corners. This will reduce signal reflections and impedance changes. Use GND stitching vias when changing layers.
- It is best to put CMOS/TTL and differential signals on a different layer(s), which should be isolated by the power and ground planes.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn.
- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use, and/or generate, clocks.
- Stubs on differential signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mil.
- Use a minimum of 20 mil spacing between the differential signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.
- Route all traces over continuous planes (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (split planes) increases inductance and radiation levels by forcing a greater loop area.

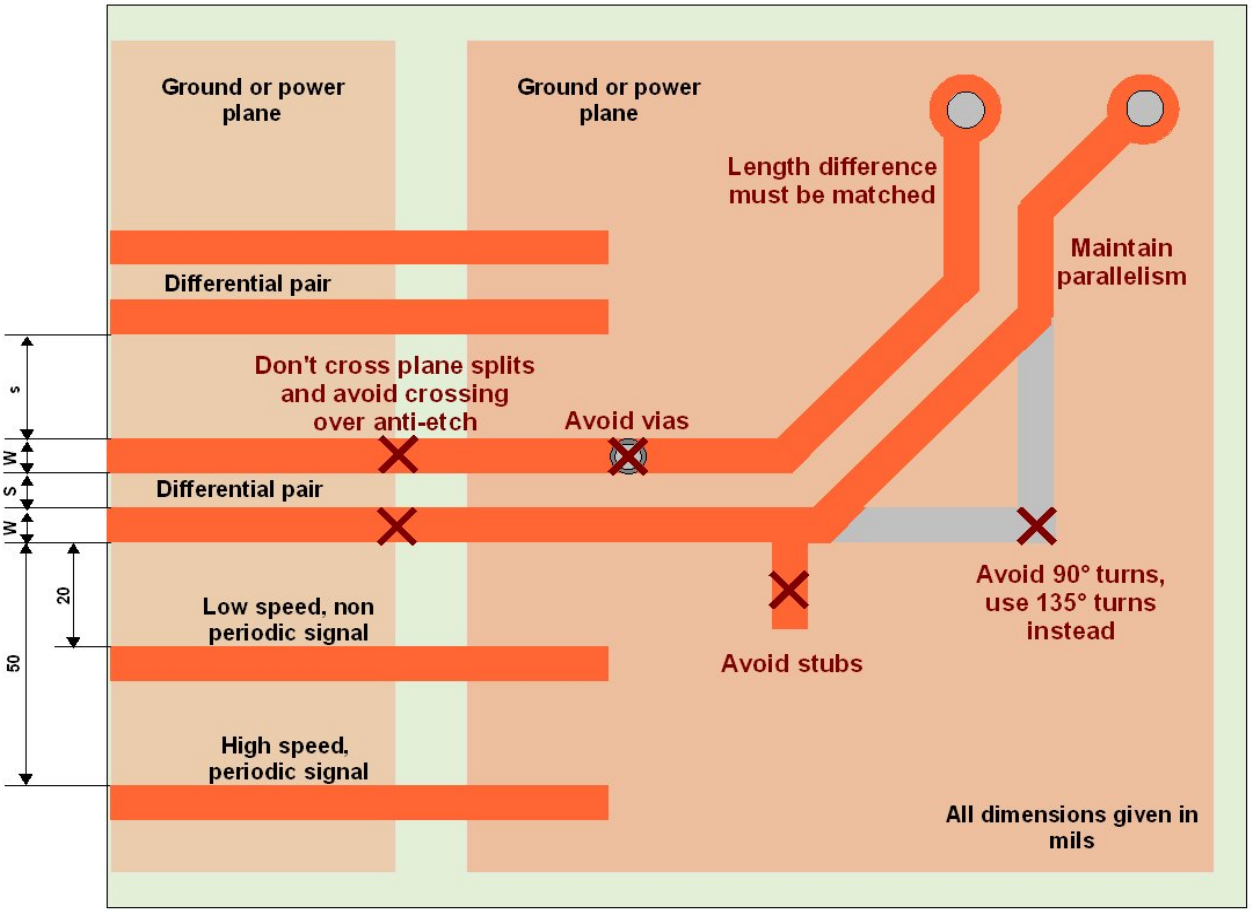

Image 17 Layout Considerations

In order to determine the necessary trace width and spacing needed to fulfill the requirements of the interface specification, it's necessary to use an impedance calculator.

7.1 PCI Express Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate	2.5 Gbit/s
Maximum signal line length (coupled traces)	TX path: 16.5 inches RX path: 17.7 inches
Signal length used on XTX™ module (including the XTX™ carrier board connector)	TX path: 2 inches RX path: 2 inches
Signal length available for the XTX™ carrier board	TX path: 14.5 inches to PCIe device and 7.7 inches to PCIe slot RX path: 15.7 inches to PCIe device and 7.7 inches to PCIe slot
Differential Impedance	100 Ohms +/-20%
Single-ended Impedance	60 Ohms +/-15%
Trace width (W)	5 mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	4 mils (microstrip routing) (*)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20 mils
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils
Length matching between differential pairs (intra-pair)	Max. 5 mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3 inch delta to minimize latency.
Length matching between reference clock differential pairs REFCLK+ and REFCLK- (intra-pair)	Max. 5 mils
Length matching between reference clock pairs (inter-pair)	No electrical requirements.
Spacing from edge of plane	Min. 40 mils
Via Usage	Max. 4 vias per TX trace Max. 2 vias per RX trace
Coupling capacitors	The coupling capacitors for the TX lines are incorporated on the XTX™ module. The coupling capacitors for RX signal lines have to be implemented on the customer XTX™ carrier board. Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.

Note

(*) In order to determine the value for trace width and differential pair spacing that matches the differential impedance determined by your PCB, it's necessary to use an adequate impedance calculator.

7.2 USB Trace Routing Guidelines

Parameter	Trace Routing
Transfer rate	480 Mbit/s
Maximum signal line length (coupled traces)	Max. 18 inches
Signal length used on XTX™ module (including the XTX™ carrier board connector)	3 inches
Signal length available for the XTX™ carrier board	15 inches
Differential Impedance	90 Ohms +/-15%
Single-ended Impedance	45 Ohms +/-10%
Trace width (W)	7 mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	5 mils (microstrip routing) (*)
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils
Length matching between differential pairs (intra-pair)	200 mils
Reference plain	GND Referenced preferred
Spacing from edge of plane	Min. 40 mils
Via Usage	Try to minimize number of vias

Note

(*) In order to determine the value for trace width and differential pair spacing that matches the differential impedance determined by your PCB, it's necessary to use an impedance calculator.

7.3 Serial ATA Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate	1.5 Gbit/s
Maximum signal line length (coupled traces)	6.5 inches on PCB (XTX™ module and carrier board. The length of the SATA cable is specified between 0 and 40 inches)
Signal length used on XTX™ module (including the XTX™ carrier board connector)	2.5 inches
Signal length available for the XTX™ carrier board	4 inches
Differential Impedance	100 Ohms +/-15%
Single-ended Impedance	Min. 40 Ohms
Trace width (W)	5 mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	4 mils (microstrip routing) (*)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20 mils
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils
Length matching between differential pairs (intra-pair)	Max. 5 mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3 inch delta to minimize latency.
Reference plain	GND Referenced preferred
Spacing from edge of plane	Min. 40 mils
Via Usage	Try to minimize number of vias
Coupling capacitors	The coupling capacitors for the TX and RX lines are incorporated on the XTX™ module.

Note

(*) In order to determine the value for trace width and differential pair spacing that matches the differential impedance determined by your PCB, it's necessary to use an impedance calculator.

Note

The congatec AG technical support team, as well as the engineers, are dedicated to helping customers design their XTX™ carrier boards. If you have any questions about the information contained in this design guide, or have additional questions, contact the congatec technical support team for assistance at support@congatec.com.

8 Industry Specifications

The list below provides links to industry specifications used to define the XTX™ interface specification.

Specification	Link
PCI Express Base Specification, Revision 1.0a	http://www.pcisig.com/specifications
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
ExpressCard Standard Release 1.0	http://www.expresscard.org/
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Audio Codec '97 Component Specification, Version 2.3	http://www.intel.com/design/chipsets/audio/
High Definition Audio Specification, Rev. 1.0	http://www.intel.com/standards/hdaudio/
LVDS Owner's Manual	http://www.national.com/appinfo/lvds/0,1798,100,00.html
ETX® Specification	http://www.etx-ig.com/specs/specs.php
XTX™ Specification	http://www.xtx-standard.org

The following reference material from Mindshare Books is recommend for use by congatec AG. For more information and additional books visit www.mindshare.com.

Title	Author
PCI Express System Architecture	Ravi Budruk, Don Anderson, Tom Shanley
PCI System Architecture (4th Edition)	Tom Shanley, Don Anderson
Universal Serial Bus System Architecture	Don Anderson
SATA Storage Technology	Don Anderson
Protected Mode Software Architecture (The PC System Architecture Series)	Tom Shanley
The Unabridged Pentium 4	Tom Shanley

Additional books covering various PC architecture subjects, that should be used as reference material, can be found at www.intel.com/intelpress.