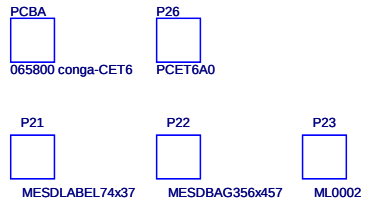
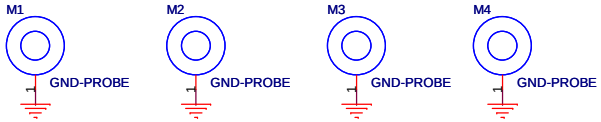
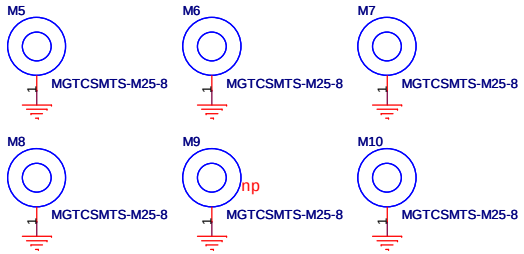
CET6

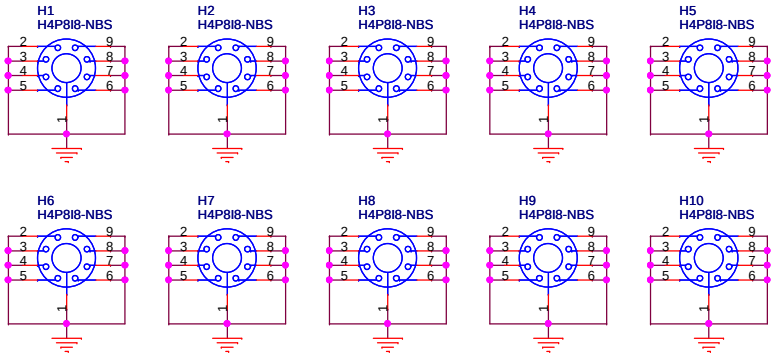
COM.0 Type 6 Evaluation Baseboard

Rev. A.0









Content

Variants

Base	Standard w/ SuperIO W83627-DHG-P

<Core Design>

Congatec AG
Auwiesenstrasse 5
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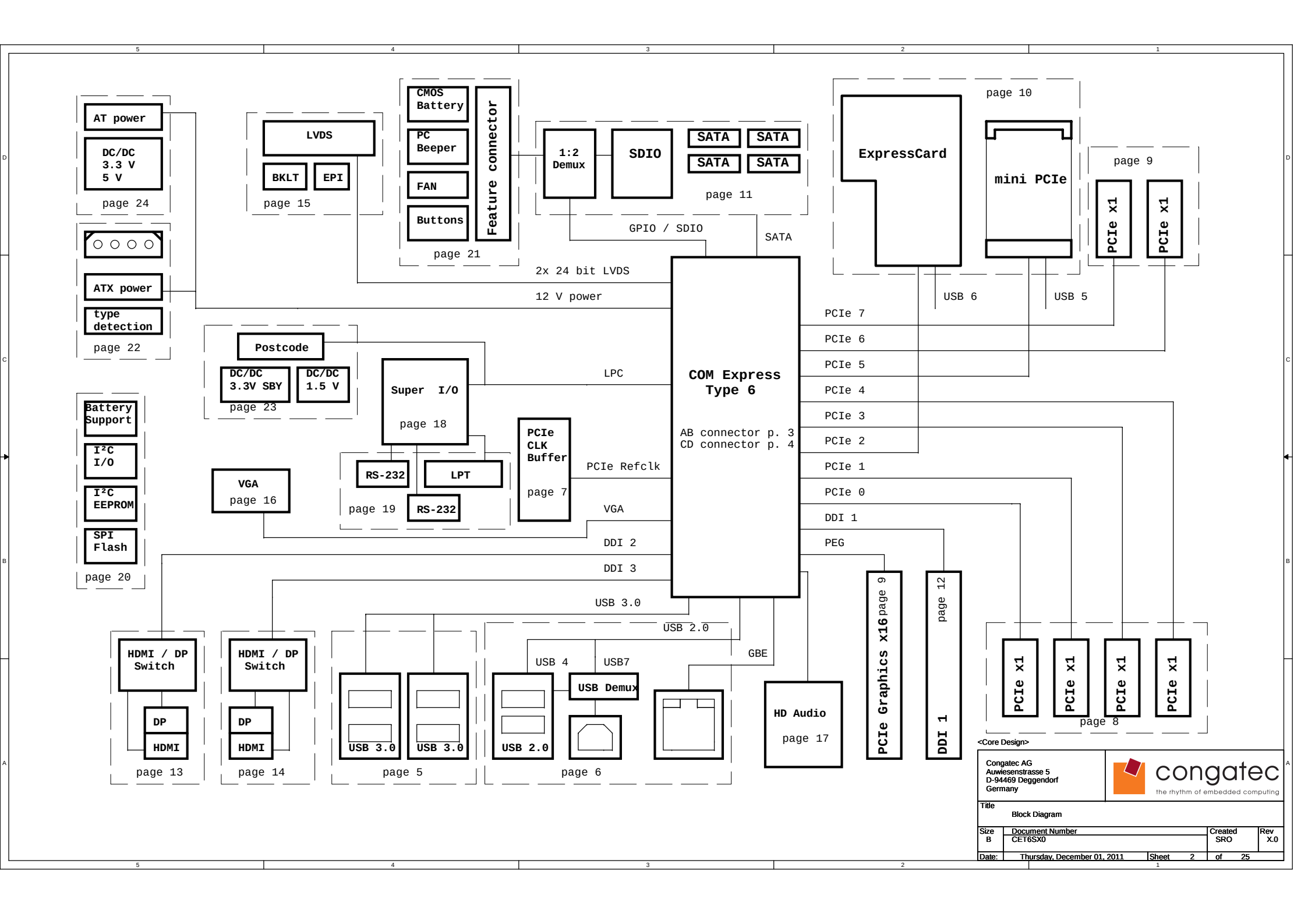
Title: CET6 - COM Express Type 6 Evaluation Backplane			
Size: B	Document Number: CET6SA0	Created: SRO	Rev: A.0
Date: Thursday, December 01, 2011	Sheet 1 of 25		



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Title: Block Diagram			
Size: B	Document Number: CET6SX0	Created: SRO	Rev: X.0
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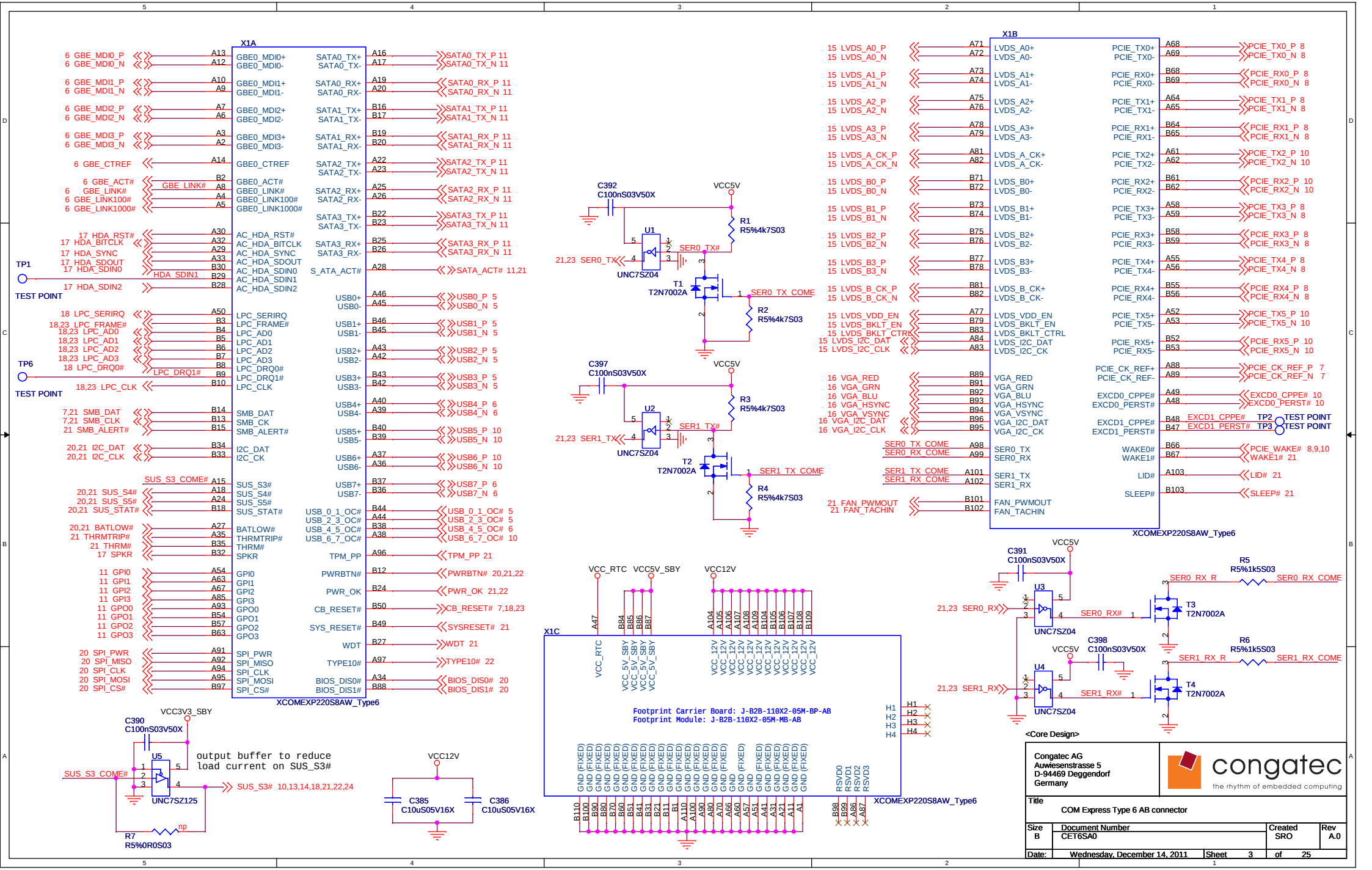
X1A
GBE0_MDI0+
GBE0_MDI0-
GBE0_MDI1+
GBE0_MDI1-
GBE0_MDI2+
GBE0_MDI2-
GBE0_MDI3+
GBE0_MDI3-
GBE0_CTREF
GBE0_ACT#
GBE0_LINK#
GBE0_LINK100#
GBE0_LINK1000#
AC_HDA_RST#
AC_HDA_BITCLK
AC_HDA_SYNC
AC_HDA_SDOUT
AC_HDA_SDIN0
AC_HDA_SDIN1
AC_HDA_SDIN2
LPC_SERIRQ
LPC_FRAME#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_DRQ0#
LPC_DRQ1#
LPC_CLK
SMB_DAT
SMB_CK
SMB_ALERT#
I2C_DAT
I2C_CK
SUS_S3#
SUS_S4#
SUS_S5#
SUS_STAT#
BATLOW#
THRMTRIP#
THRM#
SPKR
GPI0
GPI1
GPI2
GPI3
GPO0
GPO1
GPO2
GPO3
SPI_PWR
SPI_MISO
SPI_CLK
SPI_MOSI
SPI_CS#
SATA0_TX+
SATA0_TX-
SATA0_RX+
SATA0_RX-
SATA1_TX+
SATA1_TX-
SATA1_RX+
SATA1_RX-
SATA2_TX+
SATA2_TX-
SATA2_RX+
SATA2_RX-
SATA3_TX+
SATA3_TX-
SATA3_RX+
SATA3_RX-
S_ATA_ACT#
USB0+
USB0-
USB1+
USB1-
USB2+
USB2-
USB3+
USB3-
USB4+
USB4-
USB5+
USB5-
USB6+
USB6-
USB7+
USB7-
USB_0_1_OC#
USB_2_3_OC#
USB_4_5_OC#
USB_6_7_OC#
TPM_PP
PWRBTN#
PWR_OK
CB_RESET#
SYS_RESET#
WDT
TYPE10#
BIOS_DIS0#
BIOS_DIS1#
XCOMEXP220S8AW_Type6
TP1
TEST POINT
TP6
TEST POINT
HDA_SDIN1
LPC_DRQ1#
SUS_S3_COME#
GBE_LINK#
C392
C100nS03V50X
U1
UNC7SZ04
T1
T2N7002A
R1
R5%4k7S03
R2
R5%4k7S03
SER0_TX#
SER0_TX_COME
C397
C100nS03V50X
U2
UNC7SZ04
T2
T2N7002A
R3
R5%4k7S03
R4
R5%4k7S03
SER1_TX#
SER1_TX_COME
VCC5V
X1B
LVDS_A0+
LVDS_A0-
LVDS_A1+
LVDS_A1-
LVDS_A2+
LVDS_A2-
LVDS_A3+
LVDS_A3-
LVDS_A_CK+
LVDS_A_CK-
LVDS_B0+
LVDS_B0-
LVDS_B1+
LVDS_B1-
LVDS_B2+
LVDS_B2-
LVDS_B3+
LVDS_B3-
LVDS_B_CK+
LVDS_B_CK-
LVDS_VDD_EN
LVDS_BKLT_EN
LVDS_BKLT_CTRL
LVDS_I2C_DAT
LVDS_I2C_CK
VGA_RED
VGA_GRN
VGA_BLU
VGA_HSYNC
VGA_VSYNC
VGA_I2C_DAT
VGA_I2C_CK
SER0_TX
SER0_RX
SER1_TX
SER1_RX
FAN_PWMOUT
FAN_TACHIN
PCIE_TX0+
PCIE_TX0-
PCIE_RX0+
PCIE_RX0-
PCIE_TX1+
PCIE_TX1-
PCIE_RX1+
PCIE_RX1-
PCIE_TX2+
PCIE_TX2-
PCIE_RX2+
PCIE_RX2-
PCIE_TX3+
PCIE_TX3-
PCIE_RX3+
PCIE_RX3-
PCIE_TX4+
PCIE_TX4-
PCIE_RX4+
PCIE_RX4-
PCIE_TX5+
PCIE_TX5-
PCIE_RX5+
PCIE_RX5-
PCIE_CK_REF+
PCIE_CK_REF-
EXCD0_CPPE#
EXCD0_PERST#
EXCD1_CPPE#
EXCD1_PERST#
WAKE0#
WAKE1#
LID#
SLEEP#
XCOMEXP220S8AW_Type6
TP2
TP3
TEST POINT
TEST POINT
C391
C100nS03V50X
U3
UNC7SZ04
T3
T2N7002A
R5
R5%1k5S03
C398
C100nS03V50X
U4
UNC7SZ04
T4
T2N7002A
R6
R5%1k5S03
SER0_RX#
SER0_RX_COME
SER0_RX_R
SER1_RX#
SER1_RX_COME
SER1_RX_R
X1C
VCC_RTC
VCC5V_SBY
VCC12V
Footprint Carrier Board: J-B2B-110X2-05M-BP-AB
Footprint Module: J-B2B-110X2-05M-MB-AB
XCOMEXP220S8AW_Type6
C390
C100nS03V50X
U5
UNC7SZ125
VCC3V3_SBY
output buffer to reduce
load current on SUS_S3#
SUS_S3#
R7
R5%0R0S03
np
C385
C10uS05V16X
C386
C10uS05V16X
<Core Design>
Congatec AG
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Title
COM Express Type 6 AB connector
Size
B
Document Number
CET6SA0
Created
SRO
Rev
A.0
Date:
Wednesday, December 14, 2011
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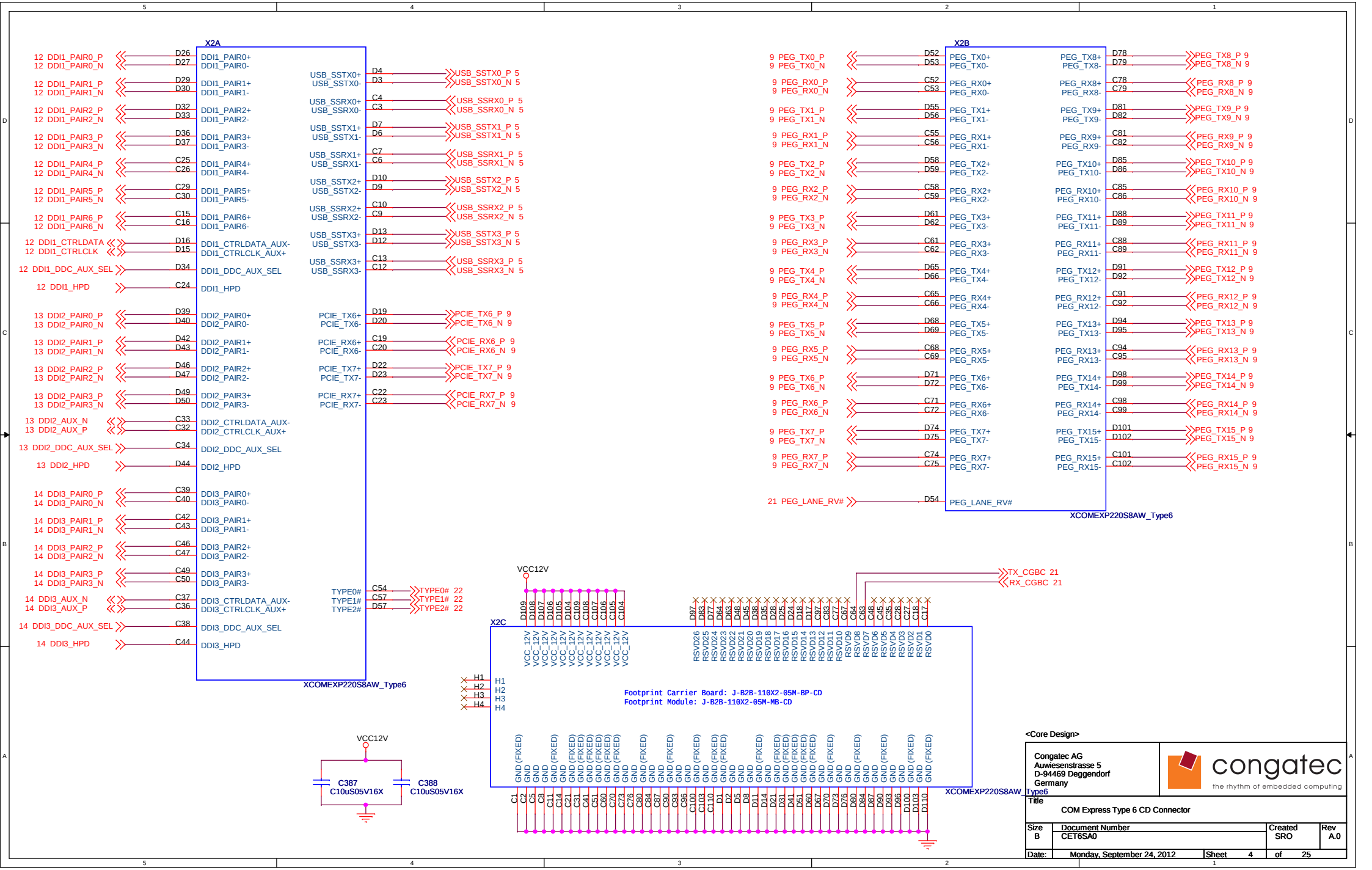
X2A
12 DDI1_PAIR0_P
12 DDI1_PAIR0_N
12 DDI1_PAIR1_P
12 DDI1_PAIR1_N
12 DDI1_PAIR2_P
12 DDI1_PAIR2_N
12 DDI1_PAIR3_P
12 DDI1_PAIR3_N
12 DDI1_PAIR4_P
12 DDI1_PAIR4_N
12 DDI1_PAIR5_P
12 DDI1_PAIR5_N
12 DDI1_PAIR6_P
12 DDI1_PAIR6_N
12 DDI1_CTRLDATA
12 DDI1_CTRLCLK
12 DDI1_DDC_AUX_SEL
12 DDI1_HPD
13 DDI2_PAIR0_P
13 DDI2_PAIR0_N
13 DDI2_PAIR1_P
13 DDI2_PAIR1_N
13 DDI2_PAIR2_P
13 DDI2_PAIR2_N
13 DDI2_PAIR3_P
13 DDI2_PAIR3_N
13 DDI2_AUX_N
13 DDI2_AUX_P
13 DDI2_DDC_AUX_SEL
13 DDI2_HPD
14 DDI3_PAIR0_P
14 DDI3_PAIR0_N
14 DDI3_PAIR1_P
14 DDI3_PAIR1_N
14 DDI3_PAIR2_P
14 DDI3_PAIR2_N
14 DDI3_PAIR3_P
14 DDI3_PAIR3_N
14 DDI3_AUX_N
14 DDI3_AUX_P
14 DDI3_DDC_AUX_SEL
14 DDI3_HPD
DDI1_PAIR0+
DDI1_PAIR0-
DDI1_PAIR1+
DDI1_PAIR1-
DDI1_PAIR2+
DDI1_PAIR2-
DDI1_PAIR3+
DDI1_PAIR3-
DDI1_PAIR4+
DDI1_PAIR4-
DDI1_PAIR5+
DDI1_PAIR5-
DDI1_PAIR6+
DDI1_PAIR6-
DDI1_CTRLDATA_AUX-
DDI1_CTRLCLK_AUX+
DDI1_DDC_AUX_SEL
DDI1_HPD
DDI2_PAIR0+
DDI2_PAIR0-
DDI2_PAIR1+
DDI2_PAIR1-
DDI2_PAIR2+
DDI2_PAIR2-
DDI2_PAIR3+
DDI2_PAIR3-
DDI2_CTRLDATA_AUX-
DDI2_CTRLCLK_AUX+
DDI2_DDC_AUX_SEL
DDI2_HPD
DDI3_PAIR0+
DDI3_PAIR0-
DDI3_PAIR1+
DDI3_PAIR1-
DDI3_PAIR2+
DDI3_PAIR2-
DDI3_PAIR3+
DDI3_PAIR3-
DDI3_CTRLDATA_AUX-
DDI3_CTRLCLK_AUX+
DDI3_DDC_AUX_SEL
DDI3_HPD
USB_SSTX0+
USB_SSTX0-
USB_SSRX0+
USB_SSRX0-
USB_SSTX1+
USB_SSTX1-
USB_SSRX1+
USB_SSRX1-
USB_SSTX2+
USB_SSTX2-
USB_SSRX2+
USB_SSRX2-
USB_SSTX3+
USB_SSTX3-
USB_SSRX3+
USB_SSRX3-
USB_SSTX0_P 5
USB_SSTX0_N 5
USB_SSRX0_P 5
USB_SSRX0_N 5
USB_SSTX1_P 5
USB_SSTX1_N 5
USB_SSRX1_P 5
USB_SSRX1_N 5
USB_SSTX2_P 5
USB_SSTX2_N 5
USB_SSRX2_P 5
USB_SSRX2_N 5
USB_SSTX3_P 5
USB_SSTX3_N 5
USB_SSRX3_P 5
USB_SSRX3_N 5
PCIE_TX6+
PCIE_TX6-
PCIE_RX6+
PCIE_RX6-
PCIE_TX7+
PCIE_TX7-
PCIE_RX7+
PCIE_RX7-
PCIE_TX6_P 9
PCIE_TX6_N 9
PCIE_RX6_P 9
PCIE_RX6_N 9
PCIE_TX7_P 9
PCIE_TX7_N 9
PCIE_RX7_P 9
PCIE_RX7_N 9
TYPE0#
TYPE1#
TYPE2#
TYPE0# 22
TYPE1# 22
TYPE2# 22
XCOMEXP220S8AW_Type6
X2B
9 PEG_TX0_P
9 PEG_TX0_N
9 PEG_RX0_P
9 PEG_RX0_N
9 PEG_TX1_P
9 PEG_TX1_N
9 PEG_RX1_P
9 PEG_RX1_N
9 PEG_TX2_P
9 PEG_TX2_N
9 PEG_RX2_P
9 PEG_RX2_N
9 PEG_TX3_P
9 PEG_TX3_N
9 PEG_RX3_P
9 PEG_RX3_N
9 PEG_TX4_P
9 PEG_TX4_N
9 PEG_RX4_P
9 PEG_RX4_N
9 PEG_TX5_P
9 PEG_TX5_N
9 PEG_RX5_P
9 PEG_RX5_N
9 PEG_TX6_P
9 PEG_TX6_N
9 PEG_RX6_P
9 PEG_RX6_N
9 PEG_TX7_P
9 PEG_TX7_N
9 PEG_RX7_P
9 PEG_RX7_N
21 PEG_LANE_RV#
PEG_TX0+
PEG_TX0-
PEG_RX0+
PEG_RX0-
PEG_TX1+
PEG_TX1-
PEG_RX1+
PEG_RX1-
PEG_TX2+
PEG_TX2-
PEG_RX2+
PEG_RX2-
PEG_TX3+
PEG_TX3-
PEG_RX3+
PEG_RX3-
PEG_TX4+
PEG_TX4-
PEG_RX4+
PEG_RX4-
PEG_TX5+
PEG_TX5-
PEG_RX5+
PEG_RX5-
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PEG_RX7-
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PEG_TX8-
PEG_RX8+
PEG_RX8-
PEG_TX9+
PEG_TX9-
PEG_RX9+
PEG_RX9-
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PEG_TX10-
PEG_RX10+
PEG_RX10-
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PEG_RX14-
PEG_TX15+
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PEG_RX15-
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PEG_TX8_N 9
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PEG_RX8_N 9
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PEG_TX10_P 9
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PEG_RX10_P 9
PEG_RX10_N 9
PEG_TX11_P 9
PEG_TX11_N 9
PEG_RX11_P 9
PEG_RX11_N 9
PEG_TX12_P 9
PEG_TX12_N 9
PEG_RX12_P 9
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PEG_TX13_P 9
PEG_TX13_N 9
PEG_RX13_P 9
PEG_RX13_N 9
PEG_TX14_P 9
PEG_TX14_N 9
PEG_RX14_P 9
PEG_RX14_N 9
PEG_TX15_P 9
PEG_TX15_N 9
PEG_RX15_P 9
PEG_RX15_N 9
XCOMEXP220S8AW_Type6
VCC12V
TX_CGBC 21
RX_CGBC 21
X2C
H1
H2
H3
H4
Footprint Carrier Board: J-B2B-110X2-05M-BP-CD
Footprint Module: J-B2B-110X2-05M-MB-CD
XCOMEXP220S8AW_Type6
VCC12V
C387
C10uS05V16X
C388
C10uS05V16X
<Core Design>
Congatec AG
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Title
COM Express Type 6 CD Connector
Size
B
Document Number
CET6SA0
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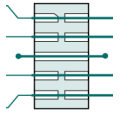
USB 3.0

USB 3.0 spec. requires
low ESR cap (>= 120 uF)
directly connected to I/O connector

Layout Note: Route USB 3.0 signals through
D44, D45, D46, D47 in the following style



Layout note:
Place D44, D45 close to X3 and X4

Layout note:
Place D46, D47 close to X3 and X4

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Title: USB 3.0			
Size: C	Document Number: CET6SA0	Created: SRO	Rev: A.0
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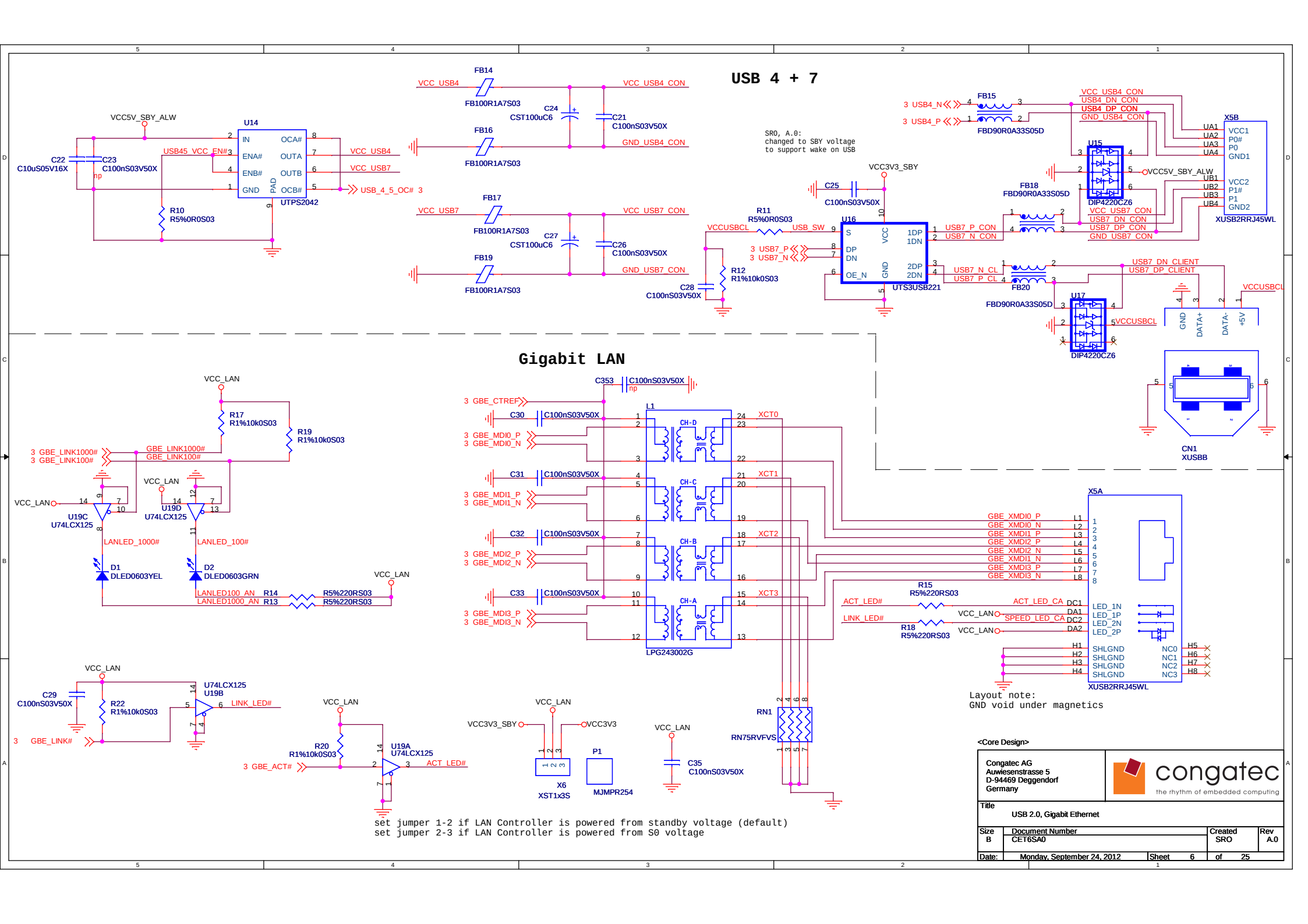
USB 4 + 7
Gigabit LAN
U14
UTPS2042
VCC5V_SBY_ALW
USB45_VCC_EN#
USB_4_5_OC# 3
VCC_USB4
VCC_USB7
FB14
FB16
FB17
FB19
FB100R1A7S03
VCC_USB4_CON
GND_USB4_CON
VCC_USB7_CON
GND_USB7_CON
SRO, A.0:
changed to SBY voltage
to support wake on USB
VCC3V3_SBY
U16
UTS3USB221
USB_SW
VCCUSBCL
USB7_P_CON
USB7_N_CON
USB7_P_CL
USB7_N_CL
FB15
FB18
FB20
FBD90R0A33S05D
U15
U17
DIP4220CZ6
X5B
XUSB2RRJ45WL
USB4_DN_CON
USB4_DP_CON
USB7_DN_CON
USB7_DP_CON
USB7_DN_CLIENT
USB7_DP_CLIENT
CN1
XUSBB
VCC_LAN
U19C
U19D
U74LCX125
LANLED_1000#
LANLED_100#
D1
DLED0603YEL
D2
DLED0603GRN
LANLED100_AN
LANLED1000_AN
L1
LPG243002G
CH-A
CH-B
CH-C
CH-D
XCT0
XCT1
XCT2
XCT3
RN1
RN75RVFVS
X5A
XUSB2RRJ45WL
ACT_LED#
LINK_LED#
ACT_LED_CA
SPEED_LED_CA
U19B
U19A
X6
XST1x3S
P1
MJMPR254
C35
Layout note:
GND void under magnetics
set jumper 1-2 if LAN Controller is powered from standby voltage (default)
set jumper 2-3 if LAN Controller is powered from S0 voltage
<Core Design>
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Germany
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Title
USB 2.0, Gigabit Ethernet
Size B
Document Number CET6SA0
Created SRO
Rev A.0
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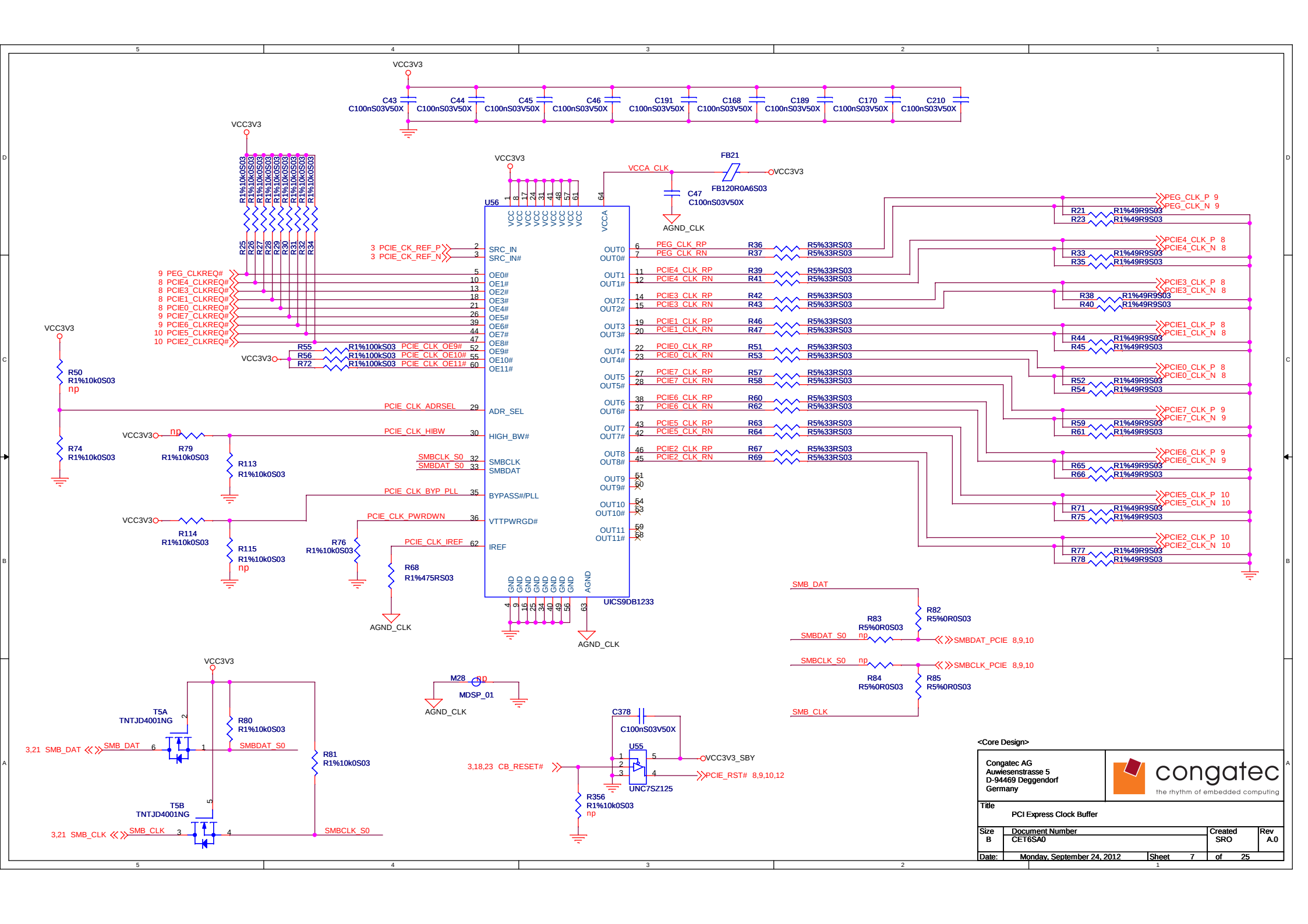
VCC3V3
C43 C100nS03V50X
C44 C100nS03V50X
C45 C100nS03V50X
C46 C100nS03V50X
C191 C100nS03V50X
C168 C100nS03V50X
C189 C100nS03V50X
C170 C100nS03V50X
C210 C100nS03V50X
R1%10k0S03
R25 R26 R27 R28 R29 R30 R31 R32 R34
U56
VCC
VCCA
VCCA_CLK
FB21
FB120R0A6S03
C47 C100nS03V50X
AGND_CLK
3 PCIE_CK_REF_P
3 PCIE_CK_REF_N
SRC_IN
SRC_IN#
9 PEG_CLKREQ#
8 PCIE4_CLKREQ#
8 PCIE3_CLKREQ#
8 PCIE1_CLKREQ#
8 PCIE0_CLKREQ#
9 PCIE7_CLKREQ#
9 PCIE6_CLKREQ#
10 PCIE5_CLKREQ#
10 PCIE2_CLKREQ#
OE0# OE1# OE2# OE3# OE4# OE5# OE6# OE7# OE8# OE9# OE10# OE11#
R55 R56 R72 R1%100kS03
PCIE_CLK_OE9# PCIE_CLK_OE10# PCIE_CLK_OE11#
R50 R1%10k0S03 np
R74 R1%10k0S03
PCIE_CLK_ADRSEL
ADR_SEL
R79 R1%10k0S03 np
R113 R1%10k0S03
PCIE_CLK_HIBW
HIGH_BW#
SMBCLK_S0
SMBDAT_S0
SMBCLK
SMBDAT
PCIE_CLK_BYP_PLL
BYPASS#/PLL
R114 R1%10k0S03
R115 R1%10k0S03 np
PCIE_CLK_PWRDWN
VTTPWRGD#
R76 R1%10k0S03
PCIE_CLK_IREF
IREF
R68 R1%475RS03
AGND_CLK
GND
AGND
UICS9DB1233
OUT0 OUT0# OUT1 OUT1# OUT2 OUT2# OUT3 OUT3# OUT4 OUT4# OUT5 OUT5# OUT6 OUT6# OUT7 OUT7# OUT8 OUT8# OUT9 OUT9# OUT10 OUT10# OUT11 OUT11#
PEG_CLK_RP PEG_CLK_RN
PCIE4_CLK_RP PCIE4_CLK_RN
PCIE3_CLK_RP PCIE3_CLK_RN
PCIE1_CLK_RP PCIE1_CLK_RN
PCIE0_CLK_RP PCIE0_CLK_RN
PCIE7_CLK_RP PCIE7_CLK_RN
PCIE6_CLK_RP PCIE6_CLK_RN
PCIE5_CLK_RP PCIE5_CLK_RN
PCIE2_CLK_RP PCIE2_CLK_RN
R36 R37 R39 R41 R42 R43 R46 R47 R51 R53 R57 R58 R60 R62 R63 R64 R67 R69
R5%33RS03
R21 R23 R33 R35 R38 R40 R44 R45 R52 R54 R59 R61 R65 R66 R71 R75 R77 R78
R1%49R9S03
PEG_CLK_P 9
PEG_CLK_N 9
PCIE4_CLK_P 8
PCIE4_CLK_N 8
PCIE3_CLK_P 8
PCIE3_CLK_N 8
PCIE1_CLK_P 8
PCIE1_CLK_N 8
PCIE0_CLK_P 8
PCIE0_CLK_N 8
PCIE7_CLK_P 9
PCIE7_CLK_N 9
PCIE6_CLK_P 9
PCIE6_CLK_N 9
PCIE5_CLK_P 10
PCIE5_CLK_N 10
PCIE2_CLK_P 10
PCIE2_CLK_N 10
SMB_DAT
SMBDAT_S0
SMBCLK_S0
SMB_CLK
R82 R5%0R0S03
R83 R5%0R0S03
R84 R5%0R0S03
R85 R5%0R0S03
SMBDAT_PCIE 8,9,10
SMBCLK_PCIE 8,9,10
T5A TNTJD4001NG
T5B TNTJD4001NG
R80 R1%10k0S03
R81 R1%10k0S03
3,21 SMB_DAT
3,21 SMB_CLK
M28 np
MDSP_01
C378 C100nS03V50X
U55
UNC7SZ125
3,18,23 CB_RESET#
VCC3V3_SBY
PCIE_RST# 8,9,10,12
R356 R1%10k0S03 np
<Core Design>
Congatec AG
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Title
PCI Express Clock Buffer
Size B
Document Number CET6SA0
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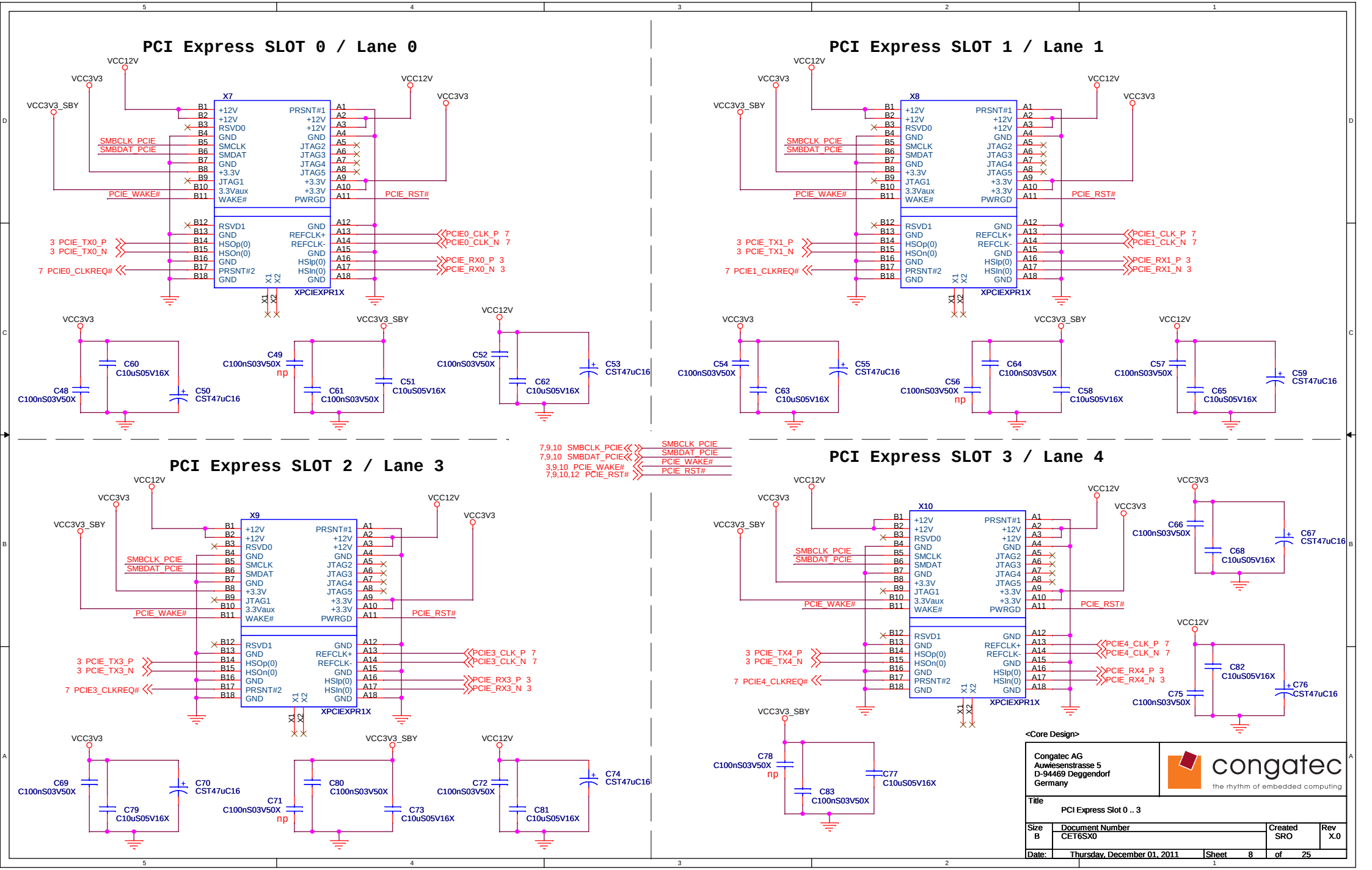
PCI Express SLOT 0 / Lane 0
PCI Express SLOT 1 / Lane 1
PCI Express SLOT 2 / Lane 3
PCI Express SLOT 3 / Lane 4
X7
X8
X9
X10
XPCIEXPR1X
SMBCLK_PCIE
SMBDAT_PCIE
PCIE_WAKE#
PCIE_RST#
3 PCIE_TX0_P
3 PCIE_TX0_N
7 PCIE0_CLKREQ#
PCIE0_CLK_P 7
PCIE0_CLK_N 7
PCIE_RX0_P 3
PCIE_RX0_N 3
3 PCIE_TX1_P
3 PCIE_TX1_N
7 PCIE1_CLKREQ#
PCIE1_CLK_P 7
PCIE1_CLK_N 7
PCIE_RX1_P 3
PCIE_RX1_N 3
3 PCIE_TX3_P
3 PCIE_TX3_N
7 PCIE3_CLKREQ#
PCIE3_CLK_P 7
PCIE3_CLK_N 7
PCIE_RX3_P 3
PCIE_RX3_N 3
3 PCIE_TX4_P
3 PCIE_TX4_N
7 PCIE4_CLKREQ#
PCIE4_CLK_P 7
PCIE4_CLK_N 7
PCIE_RX4_P 3
PCIE_RX4_N 3
7,9,10 SMBCLK_PCIE
7,9,10 SMBDAT_PCIE
3,9,10 PCIE_WAKE#
7,9,10,12 PCIE_RST#
VCC12V
VCC3V3
VCC3V3_SBY
C48 C100nS03V50X
C49 C100nS03V50X np
C50 CST47uC16
C51 C10uS05V16X
C52 C100nS03V50X
C53 CST47uC16
C54 C100nS03V50X
C55 CST47uC16
C56 C100nS03V50X np
C57 C100nS03V50X
C58 C10uS05V16X
C59 CST47uC16
C60 C10uS05V16X
C61 C100nS03V50X
C62 C10uS05V16X
C63 C10uS05V16X
C64 C100nS03V50X
C65 C10uS05V16X
C66 C100nS03V50X
C67 CST47uC16
C68 C10uS05V16X
C69 C100nS03V50X
C70 CST47uC16
C71 C100nS03V50X np
C72 C100nS03V50X
C73 C10uS05V16X
C74 CST47uC16
C75 C100nS03V50X
C76 CST47uC16
C77 C10uS05V16X
C78 C100nS03V50X np
C79 C10uS05V16X
C80 C100nS03V50X
C81 C10uS05V16X
C82 C10uS05V16X
C83 C100nS03V50X
<Core Design>
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Title
PCI Express Slot 0 .. 3
Size B
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Rev X.0
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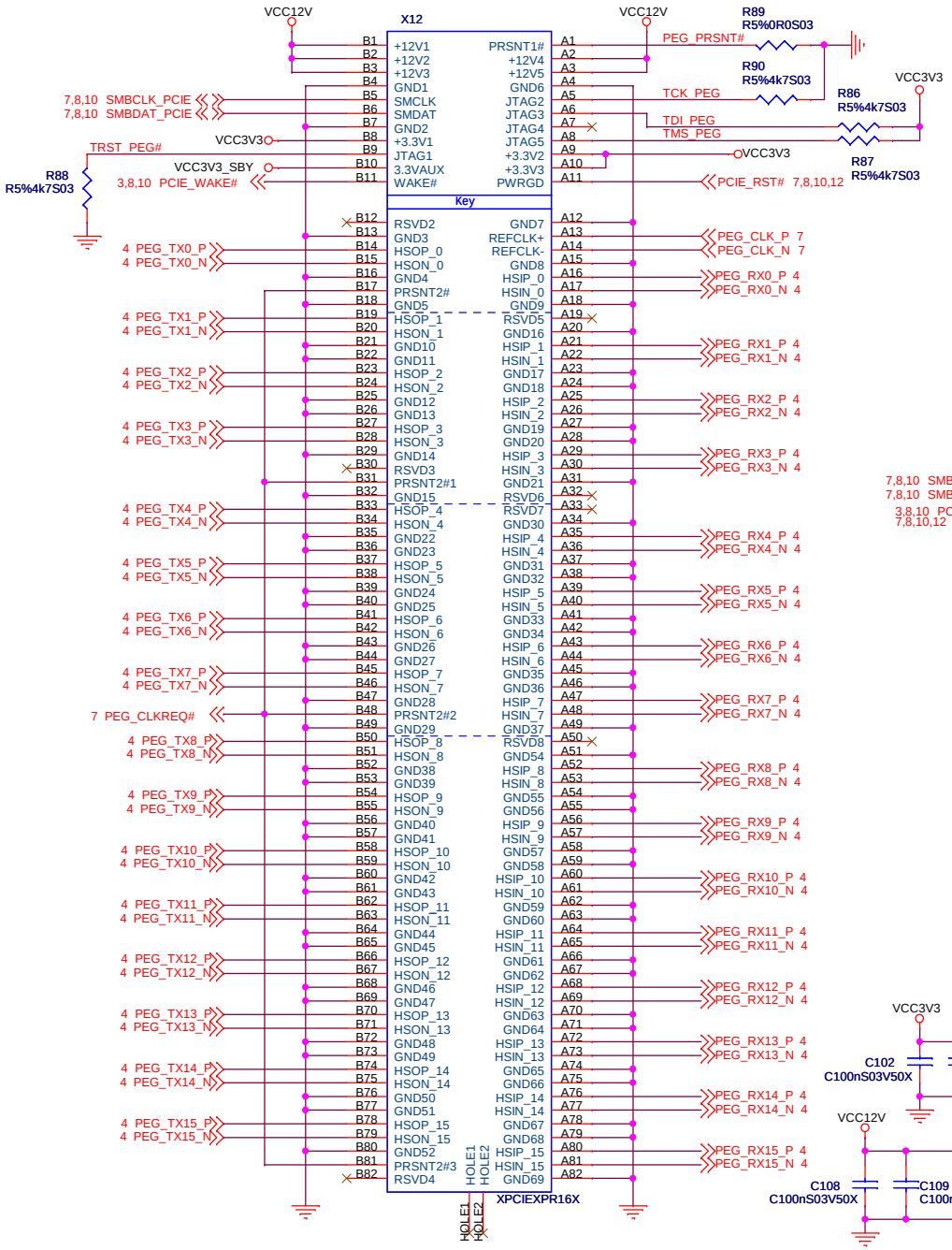
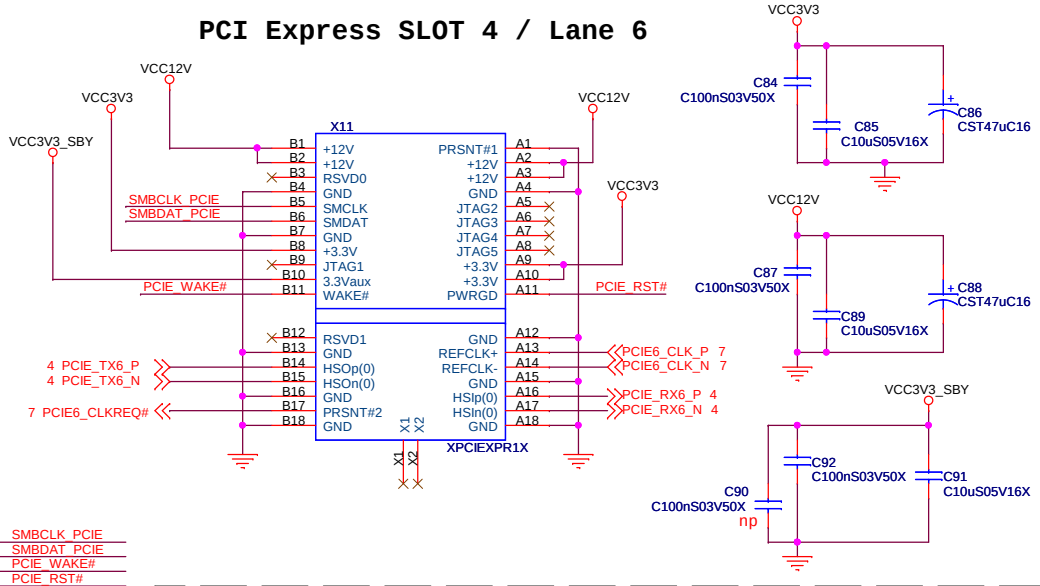
PCI Express for Graphics (PEG)

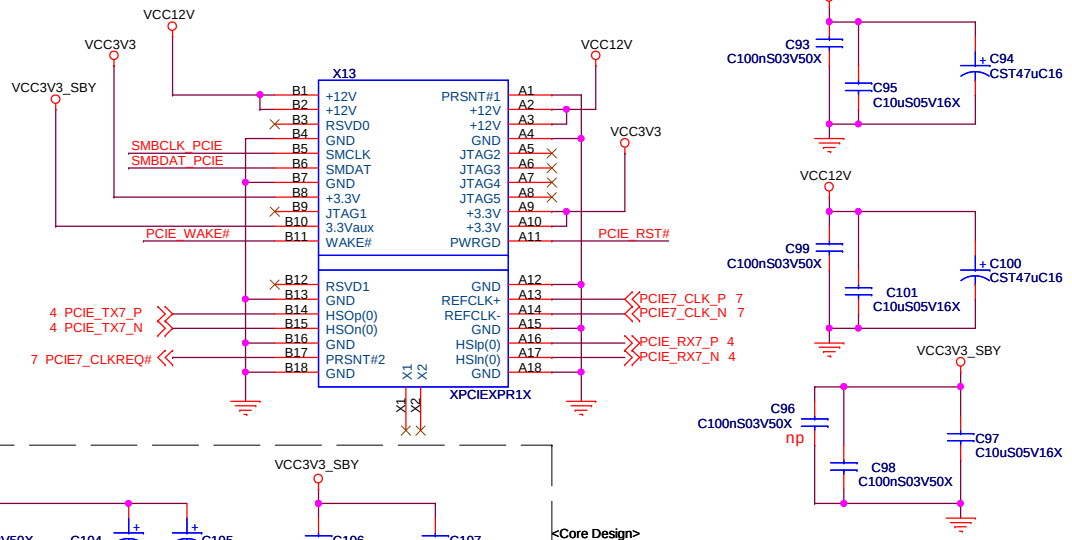


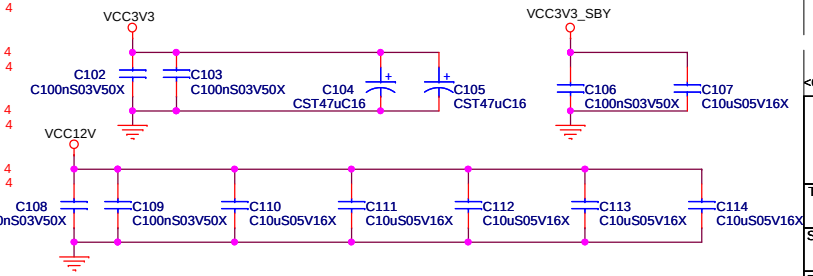
PCI Express SLOT 4 / Lane 6



7,8,10 SMBCLK_PCIE → SMBCLK_PCIE
7,8,10 SMBDAT_PCIE → SMBDAT_PCIE
3,8,10 PCIE_WAKE# → PCIE_WAKE#
7,8,10,12 PCIE_RST# → PCIE_RST#

PCI Express SLOT 5 / Lane 7





<Core Design>

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Title: PEG, PCIe 4 .. 5			
Size: B	Document Number: CET6SA0	Created: SRO	Rev: A.0
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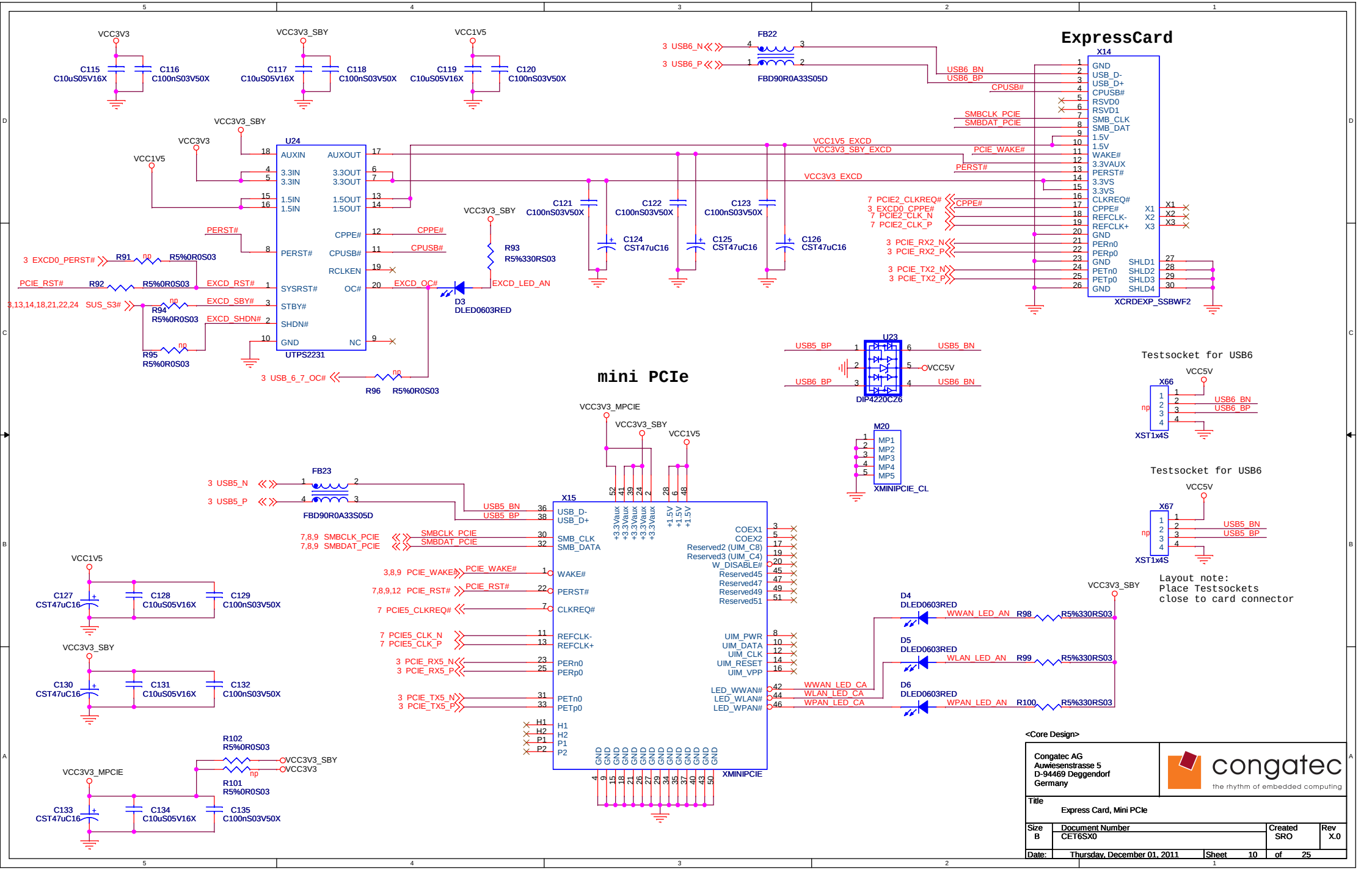
ExpressCard
mini PCIe
Testsocket for USB6
Testsocket for USB6
Layout note:
Place Testsockets
close to card connector
<Core Design>
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Title
Express Card, Mini PCIe
Size B
Document Number CET6SX0
Created SRO
Rev X.0
Date: Thursday, December 01, 2011
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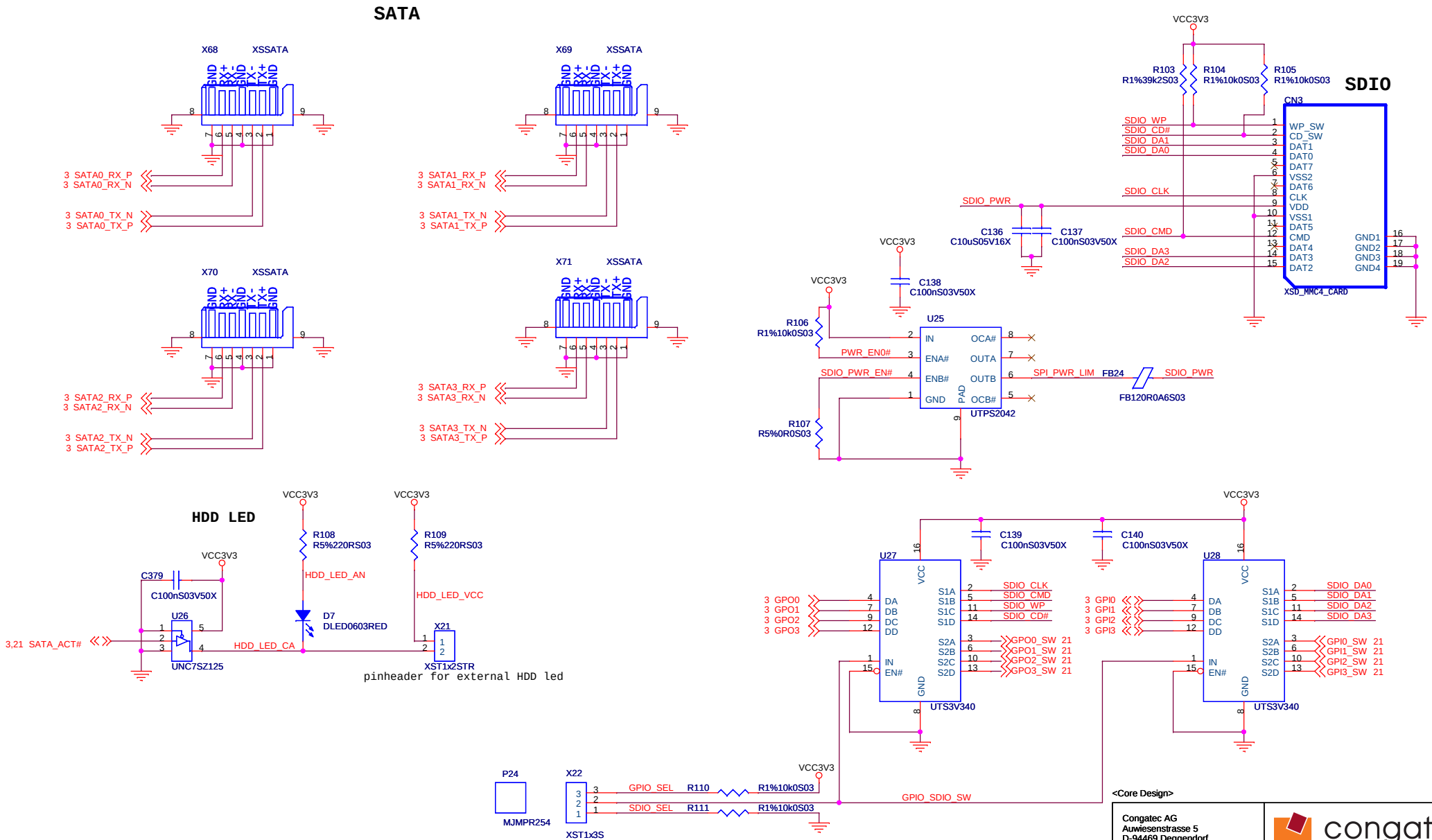
SATA
X68
XSSATA
GND
RX+
RX-
GND
TX-
TX+
GND
3 SATA0_RX_P
3 SATA0_RX_N
3 SATA0_TX_N
3 SATA0_TX_P
X69
XSSATA
3 SATA1_RX_P
3 SATA1_RX_N
3 SATA1_TX_N
3 SATA1_TX_P
X70
XSSATA
3 SATA2_RX_P
3 SATA2_RX_N
3 SATA2_TX_N
3 SATA2_TX_P
X71
XSSATA
3 SATA3_RX_P
3 SATA3_RX_N
3 SATA3_TX_N
3 SATA3_TX_P
SDIO
VCC3V3
R103
R1%39k2S03
R104
R1%10k0S03
R105
R1%10k0S03
CN3
SDIO_WP
SDIO_CD#
SDIO_DA1
SDIO_DA0
SDIO_CLK
SDIO_CMD
SDIO_DA3
SDIO_DA2
WP_SW
CD_SW
DAT1
DAT0
DAT7
VSS2
DAT6
CLK
VDD
VSS1
DAT5
CMD
DAT4
DAT3
DAT2
GND1
GND2
GND3
GND4
XSD_MMC4_CARD
SDIO_PWR
C136
C10uS05V16X
C137
C100nS03V50X
C138
C100nS03V50X
R106
R1%10k0S03
U25
IN
ENA#
ENB#
GND
PAD
OCA#
OUTA
OUTB
OCB#
UTPS2042
PWR_EN0#
SDIO_PWR_EN#
SPI_PWR_LIM
FB24
FB120R0A6S03
R107
R5%0R0S03
HDD LED
VCC3V3
R108
R5%220RS03
R109
R5%220RS03
HDD_LED_AN
HDD_LED_VCC
C379
C100nS03V50X
U26
UNC7SZ125
3,21 SATA_ACT#
HDD_LED_CA
D7
DLED0603RED
X21
XST1x2STR
pinheader for external HDD led
C139
C100nS03V50X
C140
C100nS03V50X
U27
U28
VCC
GND
DA
DB
DC
DD
IN
EN#
S1A
S1B
S1C
S1D
S2A
S2B
S2C
S2D
UTS3V340
3 GPO0
3 GPO1
3 GPO2
3 GPO3
3 GPI0
3 GPI1
3 GPI2
3 GPI3
SDIO_CLK
SDIO_CMD
SDIO_WP
SDIO_CD#
SDIO_DA0
SDIO_DA1
SDIO_DA2
SDIO_DA3
GPO0_SW 21
GPO1_SW 21
GPO2_SW 21
GPO3_SW 21
GPI0_SW 21
GPI1_SW 21
GPI2_SW 21
GPI3_SW 21
P24
MJMPR254
X22
XST1x3S
GPIO_SEL
R110
R1%10k0S03
SDIO_SEL
R111
R1%10k0S03
GPIO_SDIO_SW
set jumper 1-2 for SDIO
set jumper 2-3 for GPIO (default)
<Core Design>
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Title
SATA, SDIO
Size
B
Document Number
CET6SX0
Created
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X.0
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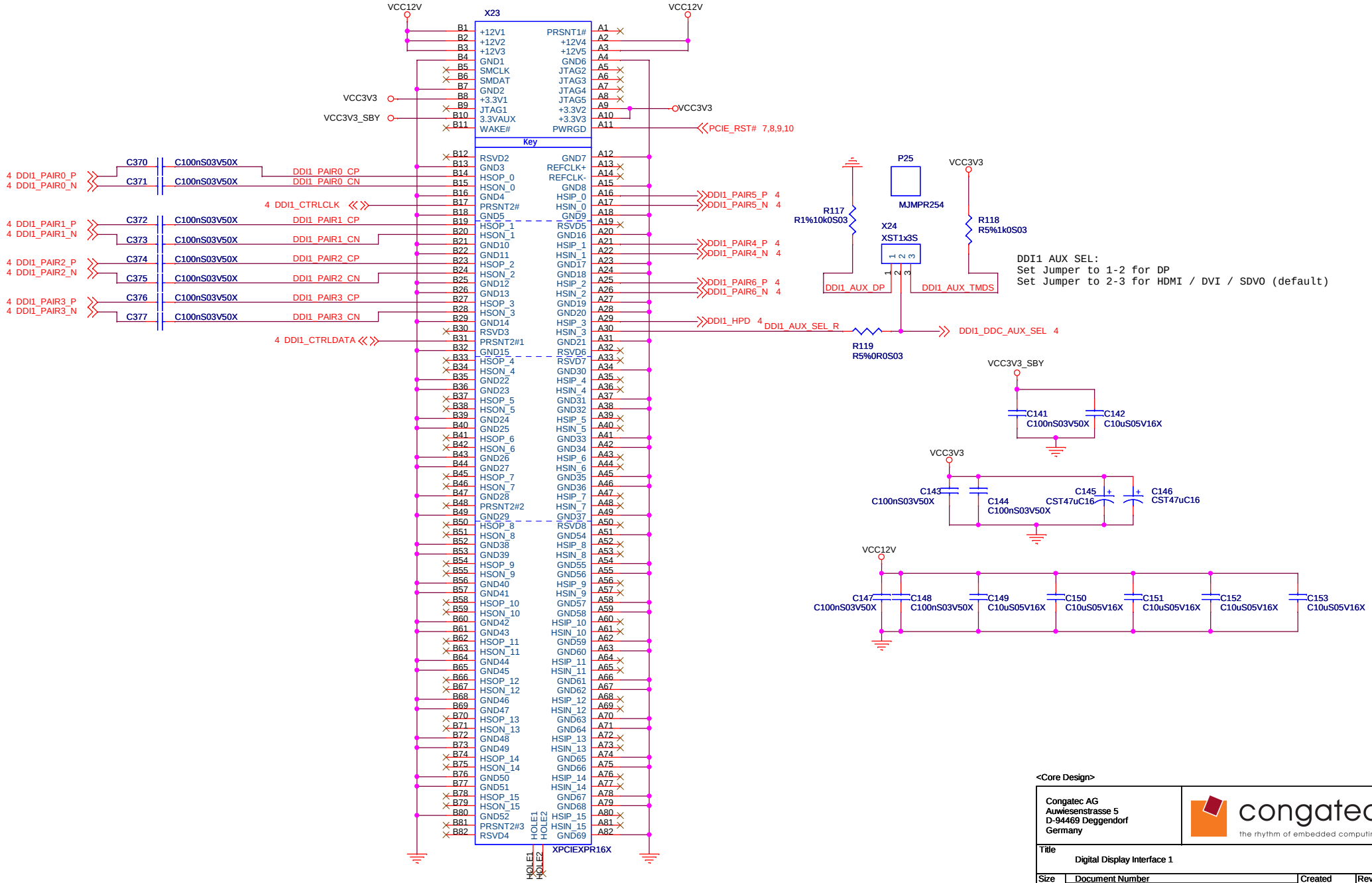

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Title: Digital Display Interface 1			
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Digital Display Interface 2 to HDMI / DISPLAY PORT

jumper 1-2: increased voltage swing
jumper 3-4: nominal voltage swing (default)
jumper 5-6: decreased voltage swing

NOTE: CAD (pin 39)
internally pulled high when TMDS is selected
CAD_SINK propagated when DP is selected

connects PU only
in TMDS mode

when using HDMI port:
jumper 1-2: I2C enabled (use with HDMI) (default)
jumper 2-3: I2C disabled (use with DVI adopter)

when using DP:
dont care about jumper setting

cable adaptors pull this pin high

in case of a simultaneous
connection of a HDMI and
a DP sink device, the DP sink
will be preferred

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Title: Digital Display Interface 2			
Size: B	Document Number: CET6SA0	Created: SRO	Rev: A.0
Date: Monday, September 24, 2012	Sheet 13 of 25		

Digital Display Interface 3 to HDMI / DISPLAY PORT

jumper 1-2: increased voltage swing
jumper 3-4: nominal voltage swing (default)
jumper 5-6: decreased voltage swing

when using HDMI port:
  jumper 1-2: I2C enabled (use with HDMI) (default)
  jumper 2-3: I2C disabled (use with DVI adopter)

when using DP:
  dont care about jumper setting

connects PU only
in TMDS mode

in case of a simultaneous
connection of a HDMI
and a DP sink device,
the DP sink will be preferred

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Title: Digital Display Interface 3			
Size: B	Document Number: CET6SA0	Created: SRO	Rev: A.0
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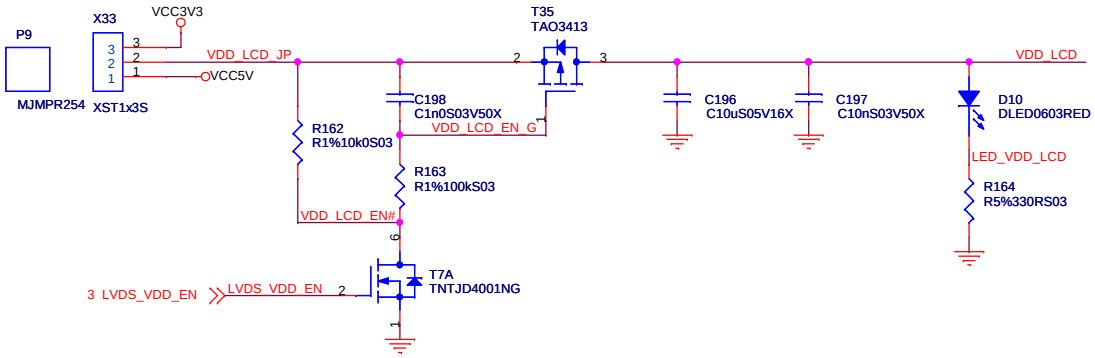
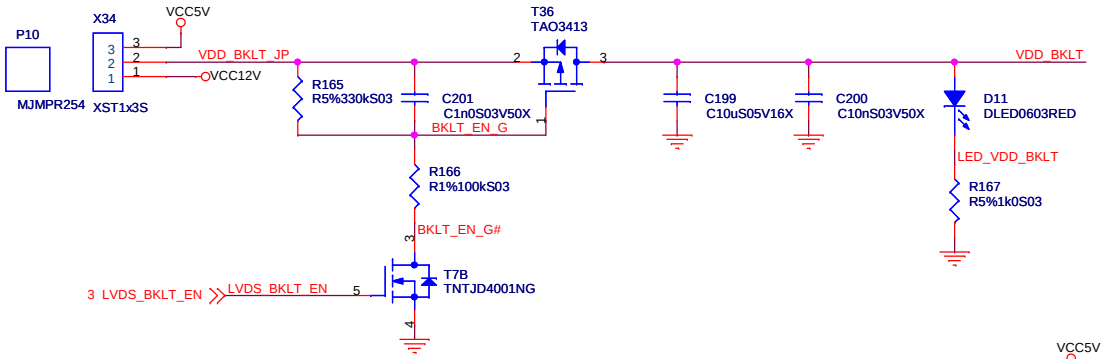
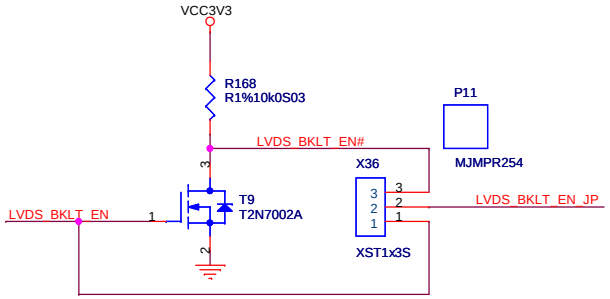
set jumper 1-2 for 5 V LCD supply voltage (default)
set jumper 2-3 for 3.3 V LCD supply voltage

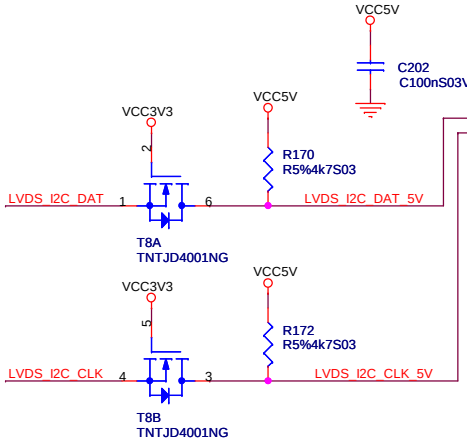


set jumper 1-2 for 12 V backlight voltage (default)
set jumper 2-3 for 5 V backlight voltage

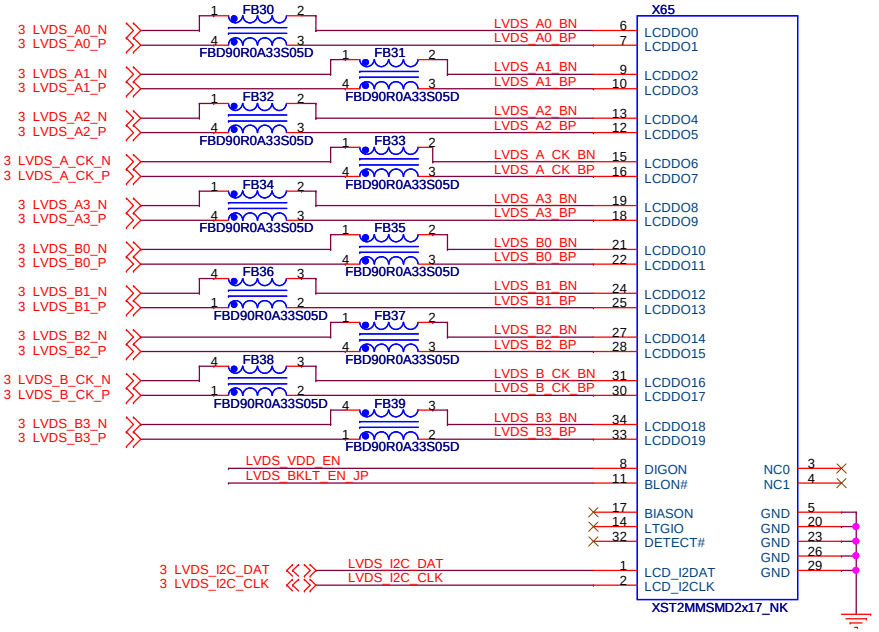




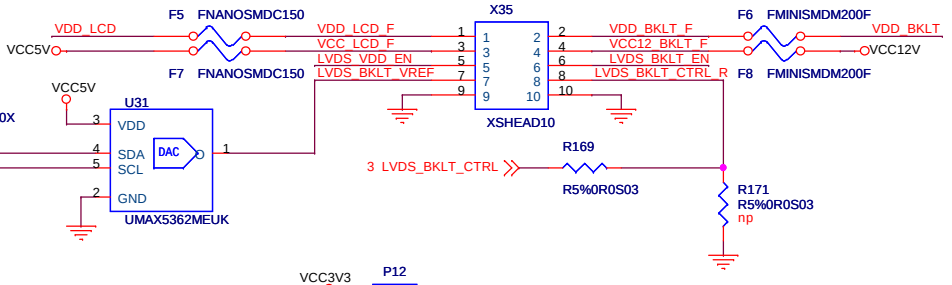
set jumper 1-2 for non-inverted BKLT_EN signal (default)
set jumper 2-3 for inverted BKLT_EN signal

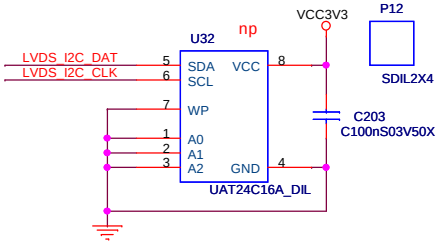


LCD



LCD / BKLT POWER





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Title: LVDS			
Size: B	Document Number: CET6SA0	Created: SRO	Rev: A.0
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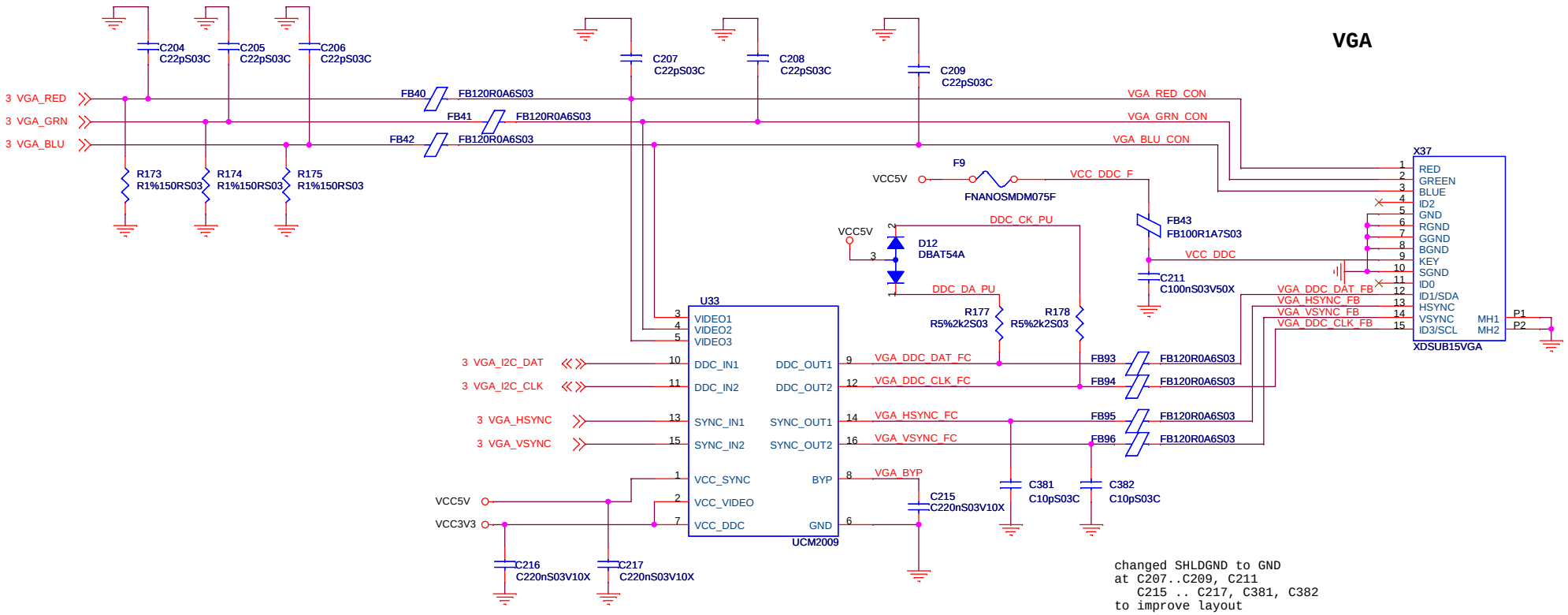

changed SHLDGND to GND
at C207..C209, C211
C215 .. C217, C381, C382
to improve layout

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Title: VGA			
Size: B	Document Number: CET6SX0	Created: SRO	Rev: X.0
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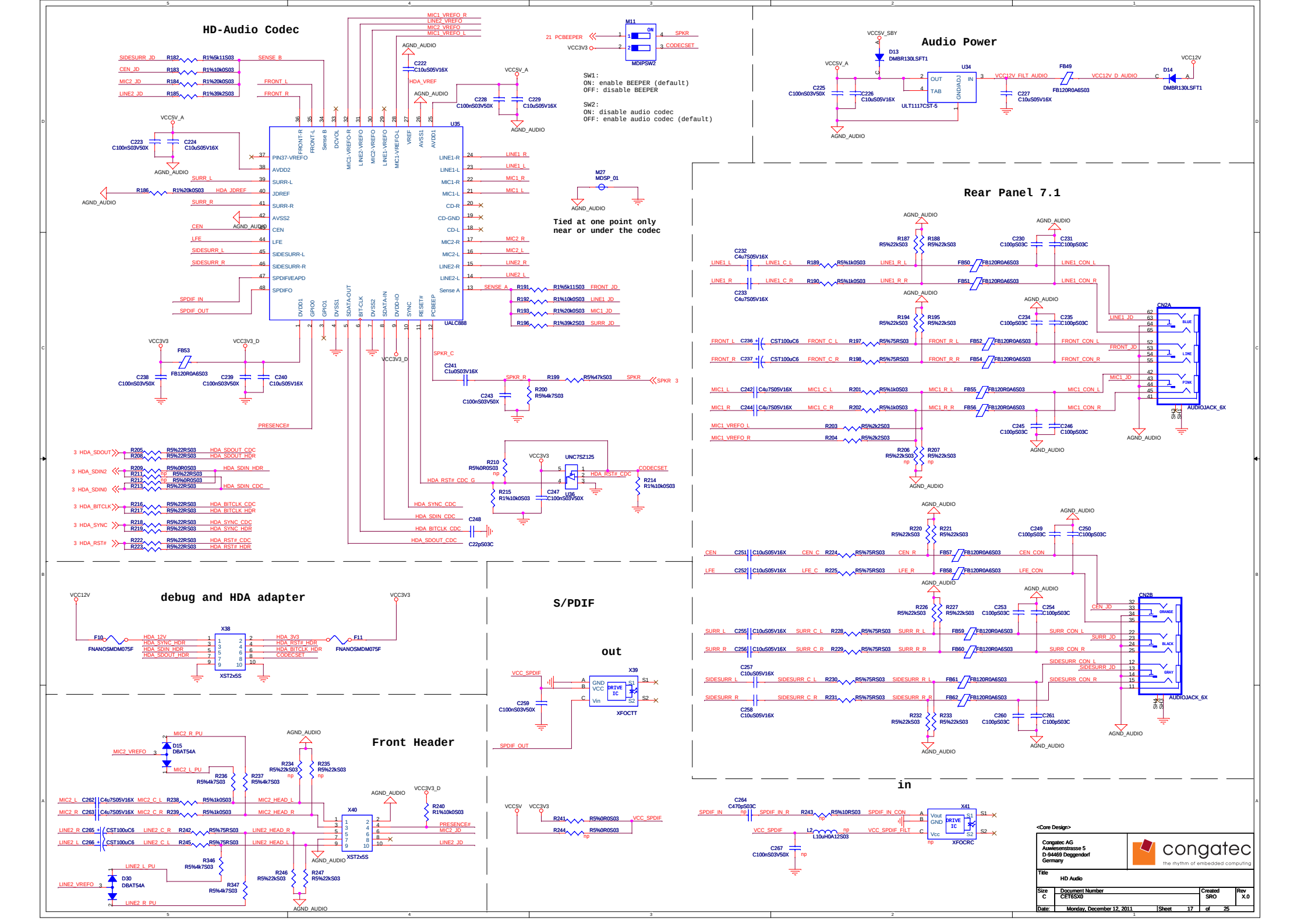
HD-Audio Codec
U35
UALC888
PIN37-VREFO
AVDD2
SURR-L
JDREF
SURR-R
AVSS2
CEN
LFE
SIDESURR-L
SIDESURR-R
SPDIFI/EAPD
SPDIFO
DVDD1
GPIO0
GPIO1
DVSS1
SDATA-OUT
BIT-CLK
DVSS2
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP
FRONT-R
FRONT-L
Sense B
DCVOL
MIC1-VREFO-R
LINE2-VREFO
MIC2-VREFO
LINE1-VREFO
MIC1-VREFO-L
VREF
AVSS1
AVDD1
LINE1-R
LINE1-L
MIC1-R
MIC1-L
CD-R
CD-GND
CD-L
MIC2-R
MIC2-L
LINE2-R
LINE2-L
Sense A
SIDESURR_JD
CEN_JD
MIC2_JD
LINE2_JD
SENSE_B
FRONT_L
FRONT_R
HDA_JDREF
SURR_L
SURR_R
CEN
LFE
SIDESURR_L
SIDESURR_R
SPDIF_IN
SPDIF_OUT
SENSE_A
FRONT_JD
LINE1_JD
MIC1_JD
SURR_JD
PRESENCE#
SPKR_C
SPKR_R
SPKR
SPKR_3
MIC1_VREFO_R
LINE2_VREFO
MIC2_VREFO
MIC1_VREFO_L
HDA_VREF
AGND_AUDIO
VCC5V_A
VCC3V3
VCC3V3_D
M11
MDIPSW2
21 PCBEEPER
SPKR
CODECSET
SW1:
ON: enable BEEPER (default)
OFF: disable BEEPER
SW2:
ON: disable audio codec
OFF: enable audio codec (default)
M27
MDSP_01
Tied at one point only
near or under the codec
Audio Power
VCC5V_SBY
D13
DMBR130LSFT1
U34
ULT1117CST-5
VCC12V_FILT_AUDIO
VCC12V_D_AUDIO
FB49
FB120R0A6S03
D14
VCC12V
Rear Panel 7.1
CN2A
AUDIOJACK_6X
LINE1_JD
FRONT_JD
MIC1_JD
LINE1_CON_L
LINE1_CON_R
FRONT_CON_L
FRONT_CON_R
MIC1_CON_L
MIC1_CON_R
CN2B
CEN_JD
SURR_JD
SIDESURR_JD
CEN_CON
LFE_CON
SURR_CON_L
SURR_CON_R
SIDESURR_CON_L
SIDESURR_CON_R
debug and HDA adapter
X38
XST2x5S
F10
F11
FNANOSMDM075F
HDA_12V
HDA_3V3
HDA_RST#_HDR
HDA_SDIN_HDR
HDA_BITCLK_HDR
HDA_SDOUT_HDR
CODECSET
S/PDIF
out
X39
XFOCTT
VCC_SPDIF
SPDIF_OUT
in
X41
XFOCRC
SPDIF_IN
SPDIF_IN_R
SPDIF_IN_CON
VCC_SPDIF_FILT
L10uH0A12S03
Front Header
X40
XST2x5S
D15
DBAT54A
D30
DBAT54A
MIC2_R_PU
MIC2_L_PU
LINE2_L_PU
LINE2_R_PU
MIC2_VREFO
LINE2_VREFO
MIC2_HEAD_L
MIC2_HEAD_R
LINE2_HEAD_R
LINE2_HEAD_L
PRESENCE#
MIC2_JD
LINE2_JD
UNC7SZ125
U36
HDA_RST#_CDC_G
HDA_RST#_CDC
HDA_SYNC_CDC
HDA_SDIN_CDC
HDA_BITCLK_CDC
HDA_SDOUT_CDC
HDA_SDOUT
HDA_SDIN2
HDA_SDIN0
HDA_BITCLK
HDA_SYNC
HDA_RST#
HDA_SDOUT_CDC
HDA_SDOUT_HDR
HDA_SDIN_HDR
HDA_SDIN_CDC
HDA_BITCLK_CDC
HDA_BITCLK_HDR
HDA_SYNC_CDC
HDA_SYNC_HDR
HDA_RST#_CDC
HDA_RST#_HDR
XFOCRC
ULT1117CST-5
MDIPSW2
AUDIOJACK_6X
BLUE
LINE
PINK
ORANGE
BLACK
GRAY
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Core Design
Title
HD Audio
Size
C
Document Number
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Created
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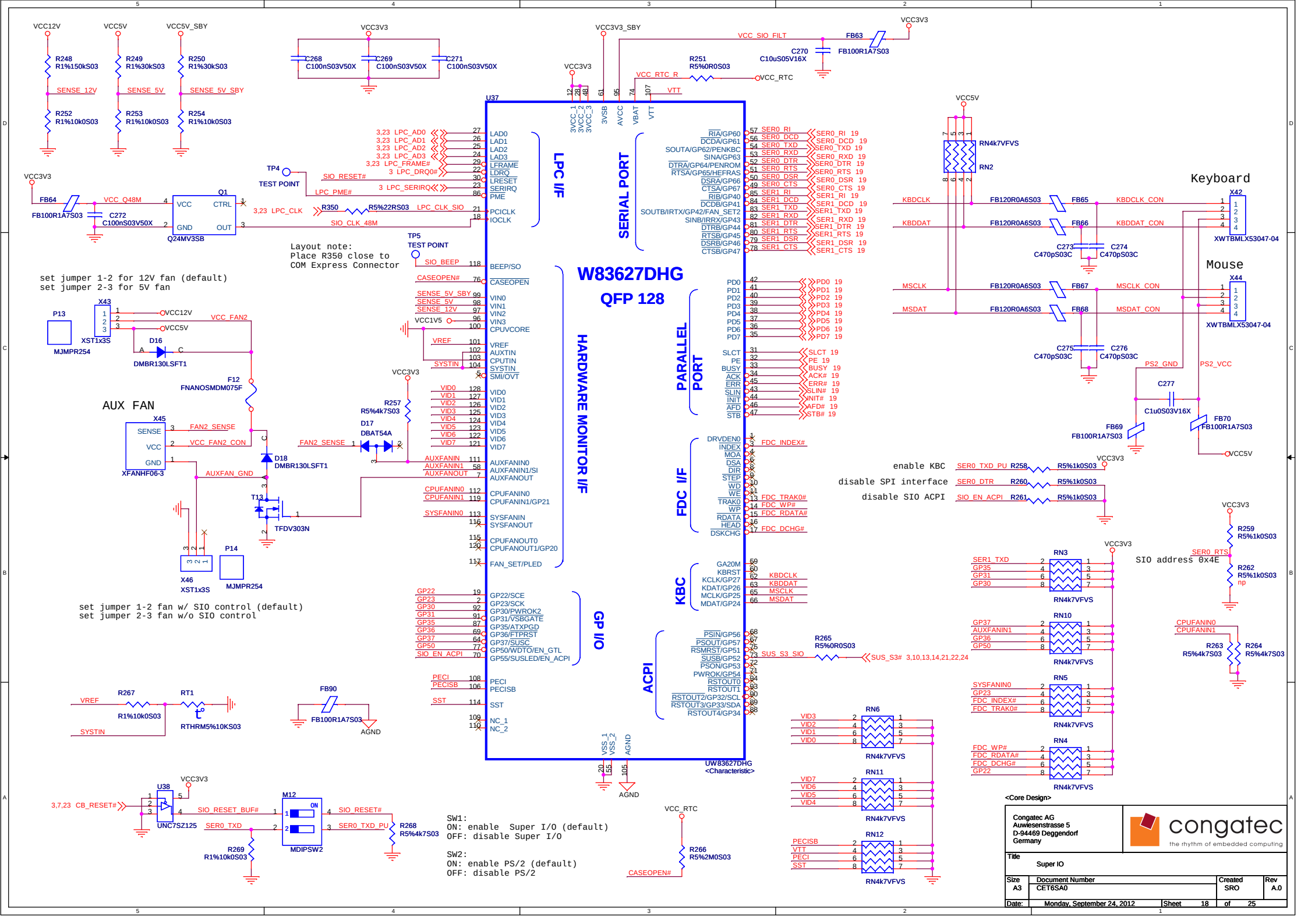
W83627DHG
QFP 128
UW83627DHG
<Characteristic>
LPC I/F
SERIAL PORT
PARALLEL PORT
HARDWARE MONITOR I/F
FDC I/F
KBC
GP I/O
ACPI
Keyboard
Mouse
AUX FAN
Layout note:
Place R350 close to
COM Express Connector
set jumper 1-2 for 12V fan (default)
set jumper 2-3 for 5V fan
set jumper 1-2 fan w/ SIO control (default)
set jumper 2-3 fan w/o SIO control
SW1:
ON: enable Super I/O (default)
OFF: disable Super I/O
SW2:
ON: enable PS/2 (default)
OFF: disable PS/2
enable KBC
disable SPI interface
disable SIO ACPI
SIO address 0x4E
<Core Design>
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D-94469 Deggendorf
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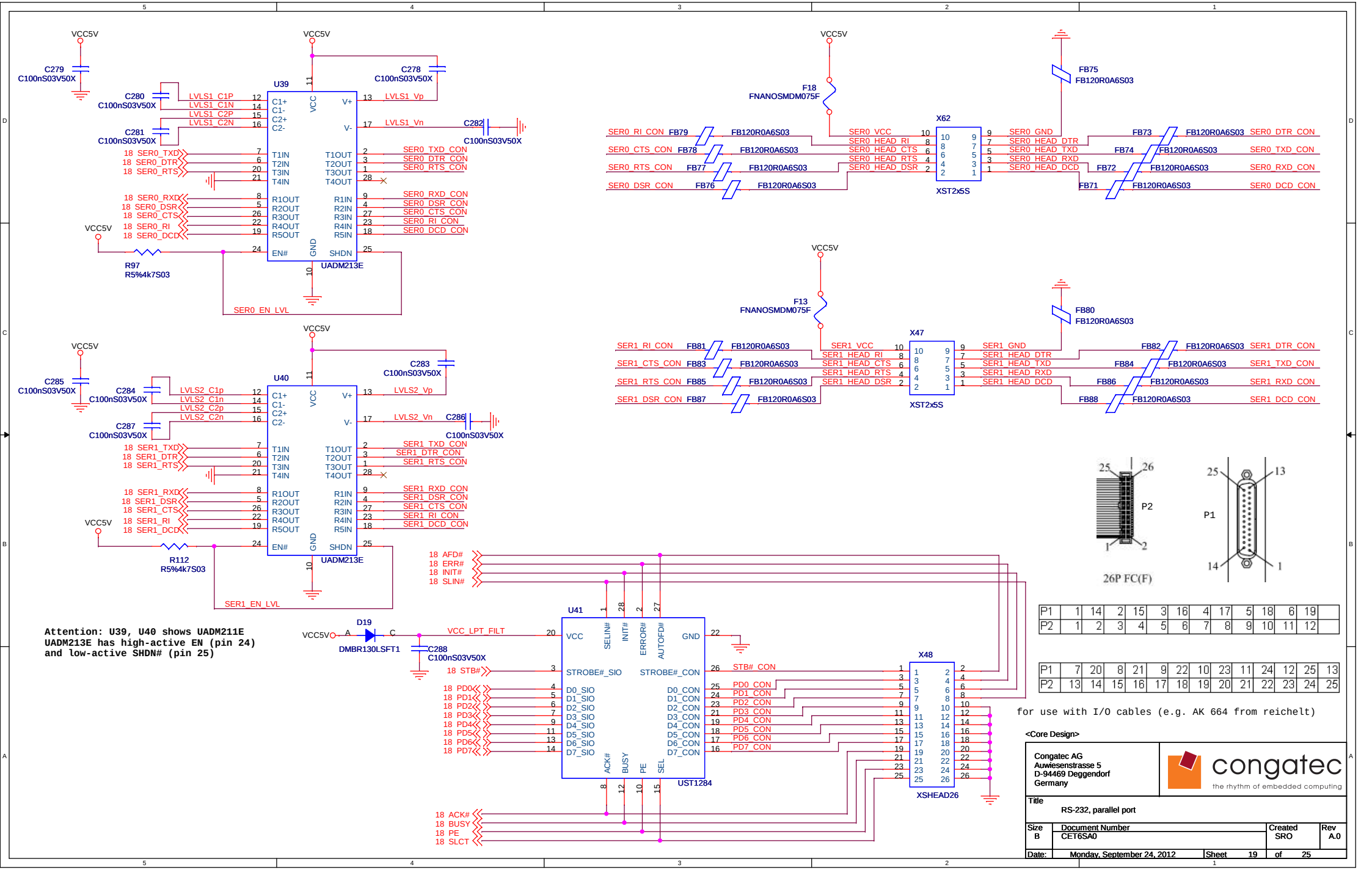
the rhythm of embedded computing
Title
Super IO
Size A3
Document Number CET6SA0
Created SRO
Rev A.0
Date: Monday, September 24, 2012
Sheet 18 of 25



Attention: U39, U40 shows UADM211E UADM213E has high-active EN (pin 24) and low-active SHDN# (pin 25)

P1	1	14	2	15	3	16	4	17	5	18	6	19	
P2	1	2	3	4	5	6	7	8	9	10	11	12	

P1	7	20	8	21	9	22	10	23	11	24	12	25	13
P2	13	14	15	16	17	18	19	20	21	22	23	24	25

for use with I/O cables (e.g. AK 664 from reichelt)

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Title: RS-232, parallel port

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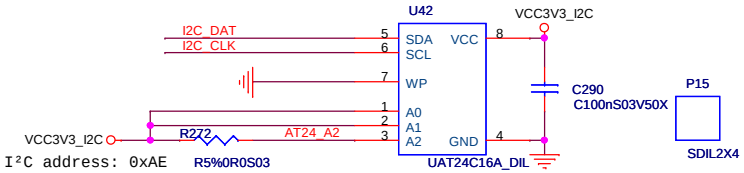
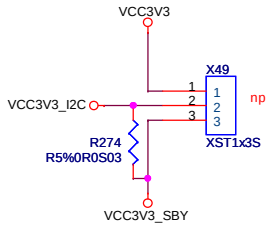
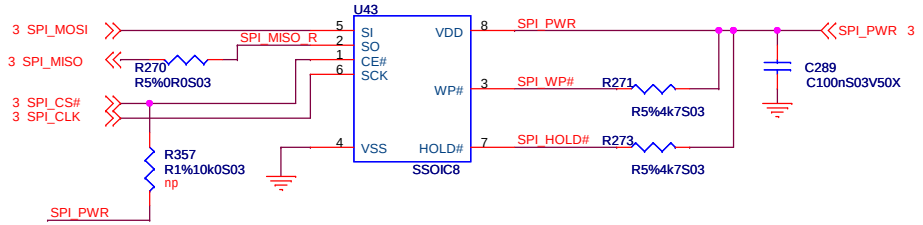
I²C EEPROM



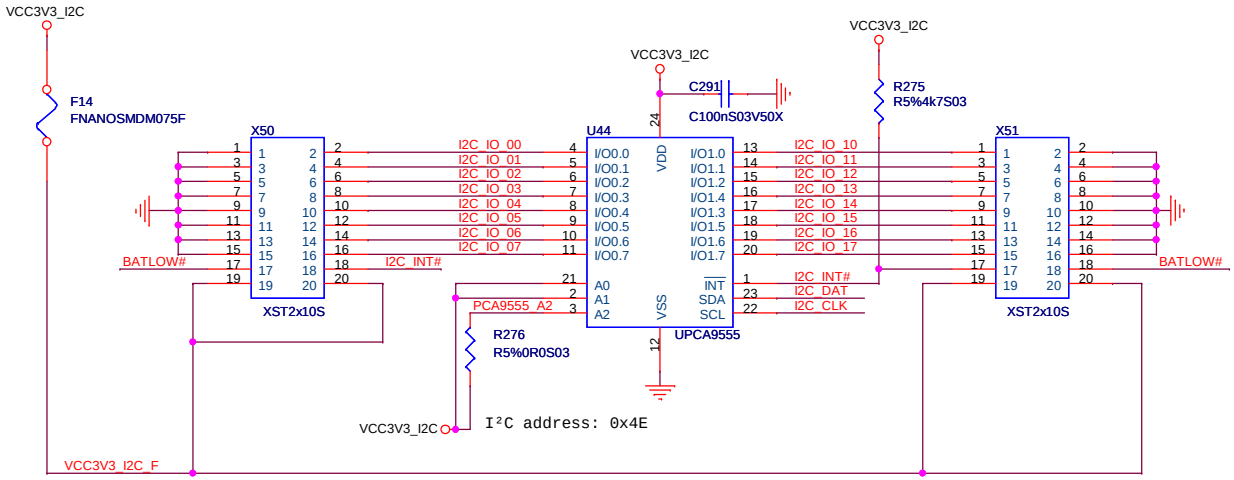


SPI BIOS Flash

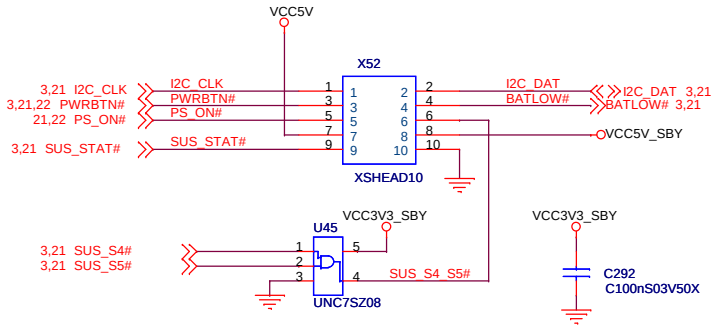


BIOS_DIS1#	BIOS_DIS0#	BIOS ENTRY / SPI_CS#
OFF	OFF	on-module firmware (default)
OFF	ON	carrier FWH (not supported)
ON	OFF	carrier firmware from SPI
ON	ON	on-module firmware, carrier SPI contains management data

Digital IO over I2C



Battery Support



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Title: SPI, I2C, Battery Support			
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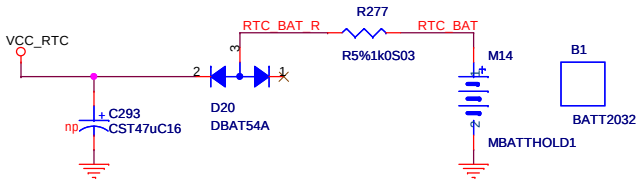
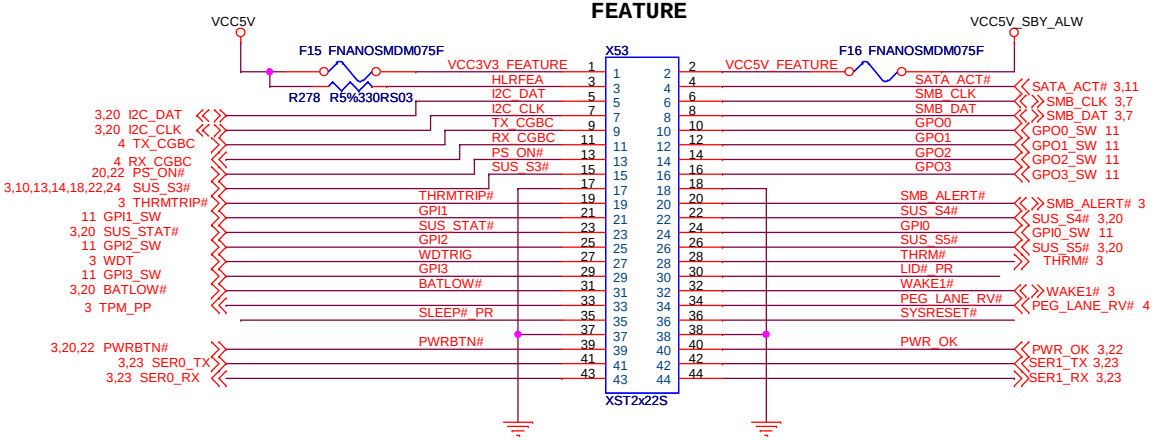
SRO, A.0:
changed to 5V to be compatible to previous platforms

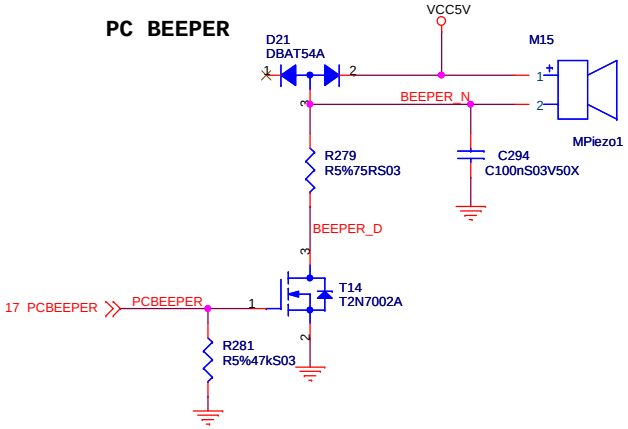
RTC / CMOS Battery



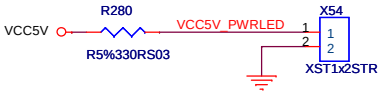
FEATURE



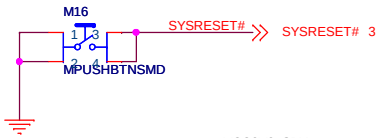
PC BEEPER



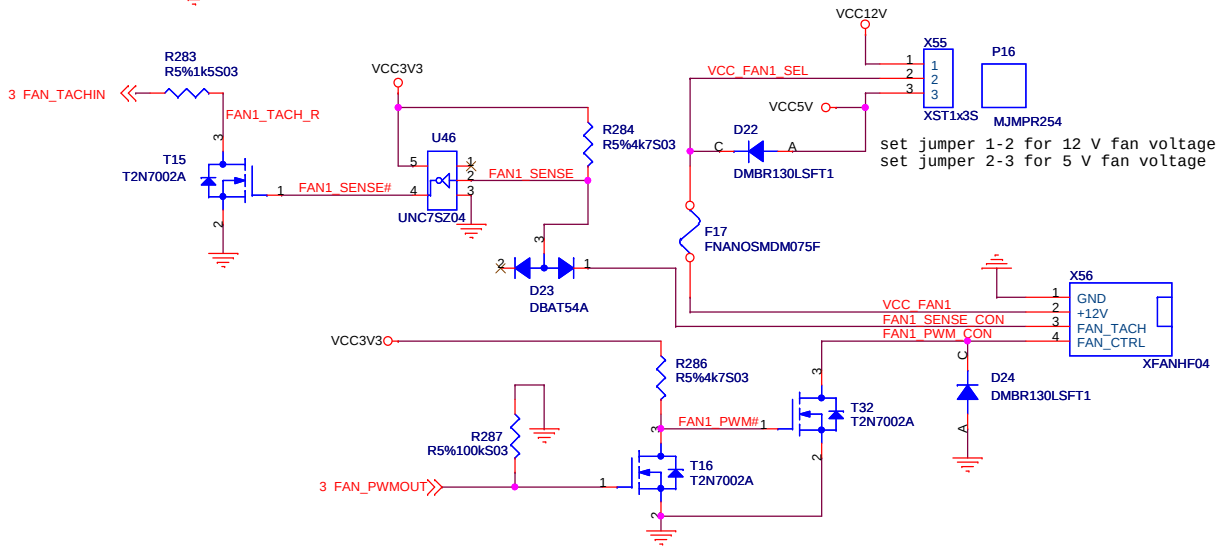
PWR LED



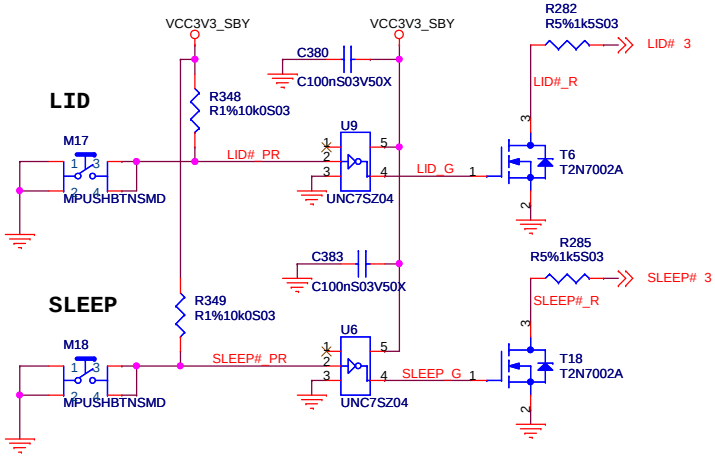
RESET



FAN Control



LID



SLEEP

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Title: CMOS Battery, Speaker, FAN, Feature Connector			
Size: B	Document Number: CET6SA0	Created: SRO	Rev: A.0
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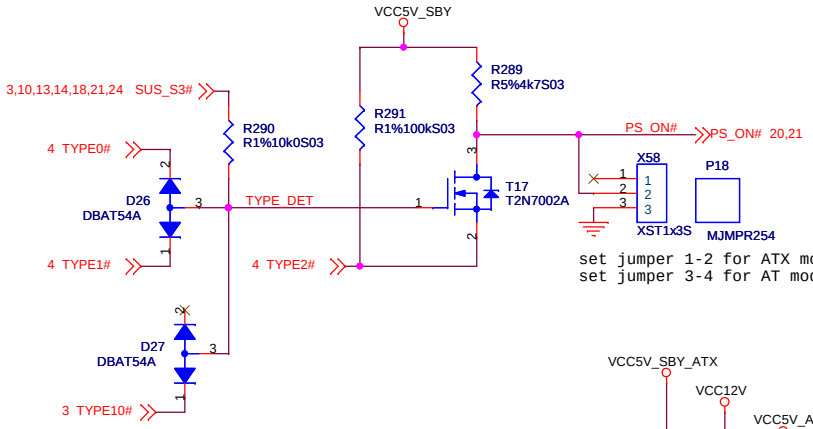
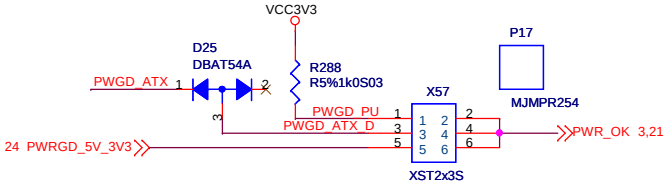
Type detection



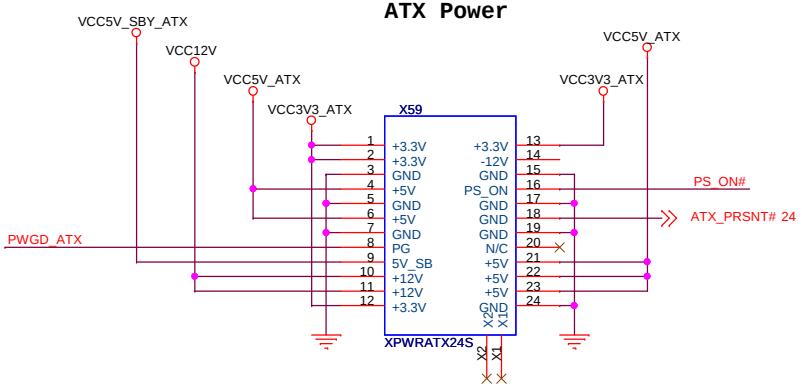
set jumper 1-2 for ATX mode (default)
set jumper 3-4 for AT mode

	Type10#	Type2#	Type1#	Type0#
Type 2 Rev 1.0:	12 V	N.C.	N.C.	N.C.
Type 2 Rev 2.0:	N.C.	N.C.	N.C.	N.C.
Type 6:	N.C.	GND	N.C.	N.C.

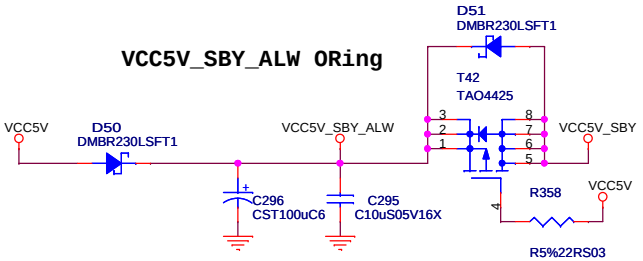


set jumper 1-2 for pull-up on PWR_OK; only for debug
set jumper 3-4 for PWR_OK from ATX supply (default)
set jumper 5-6 for PWR_OK from DC/DC (only in single 12 V mode)

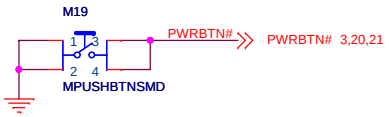
ATX Power



VCC5V_SBY_ALW ORing

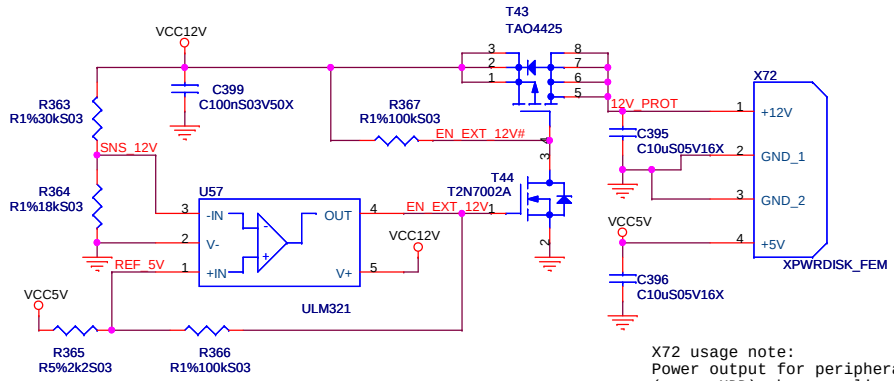


Power Button

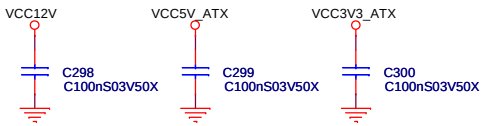


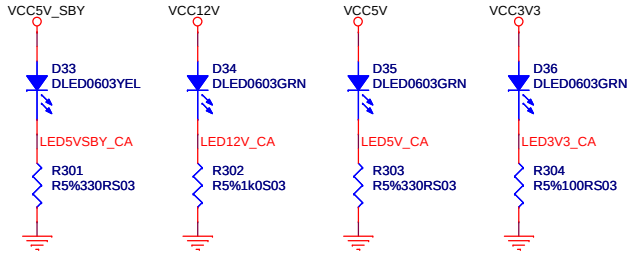
SRO, A.0: overvoltage protection:
disables +12V at X72 at about 13.6V

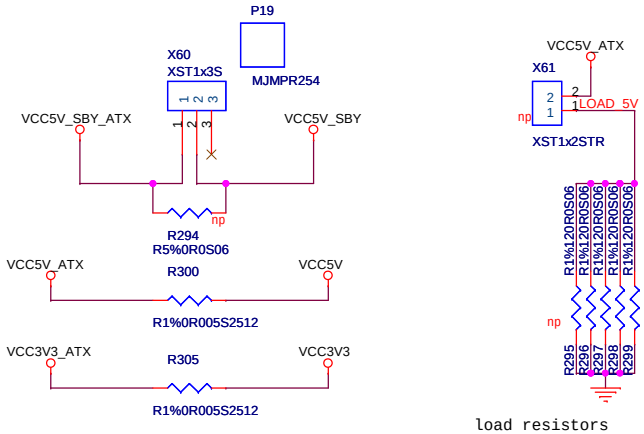
Disk Drive Power



X72 usage note:
Power output for peripherals
(e. g. HDD) when suppling
the system with 12 V only







load resistors
causing additional 200 mA
load current at 5V_ATX
helping ATX PSU to turn on

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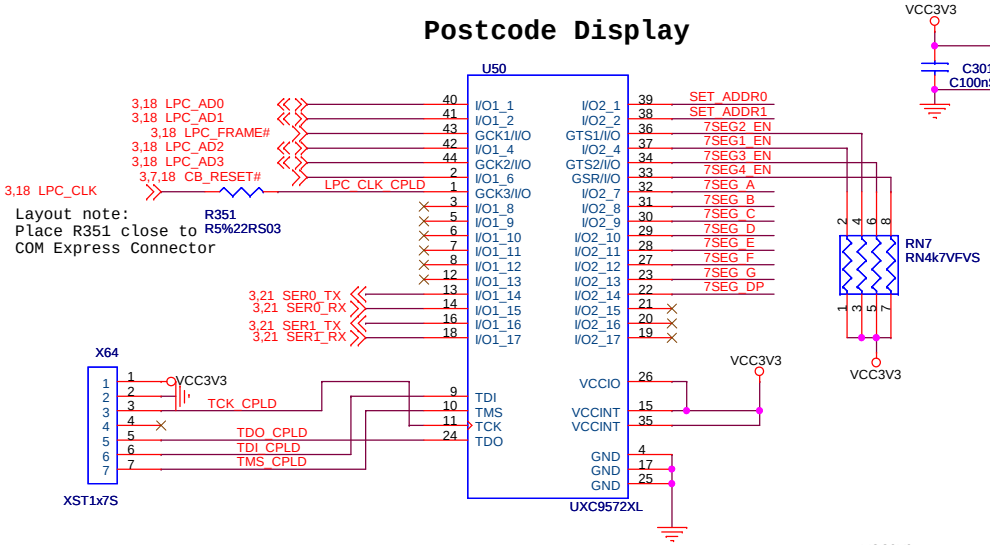
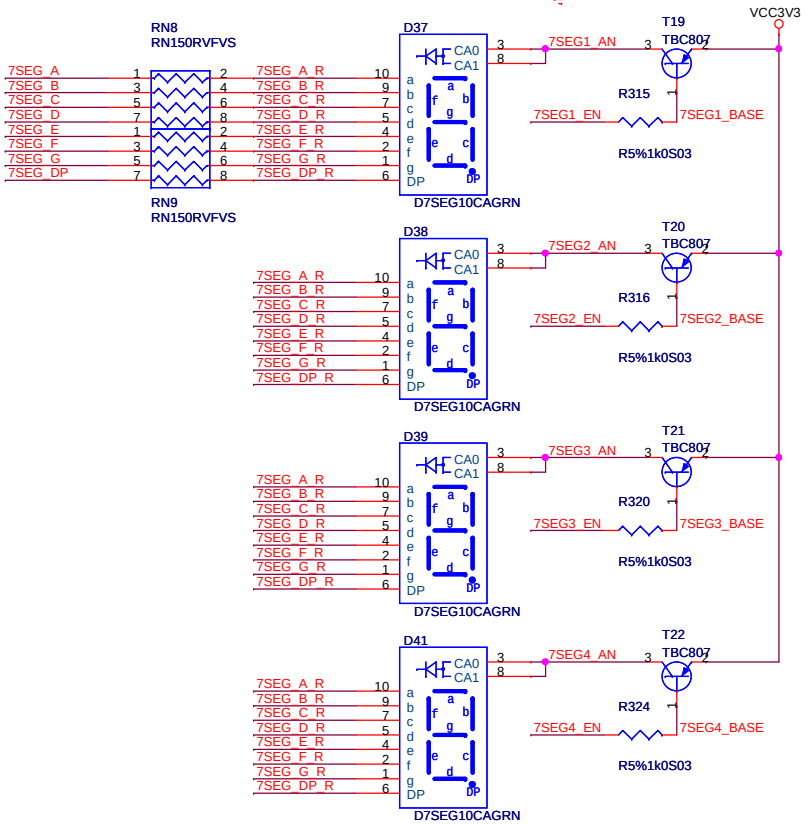
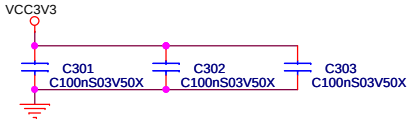
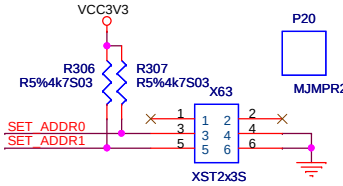
Title: ATX Power, 5V Standby Always			
Size: B	Document Number: CET6SA0	Created: SRO	Rev: A.0
Date: Monday, September 24, 2012	Sheet 22 of 25		

Postcode Display



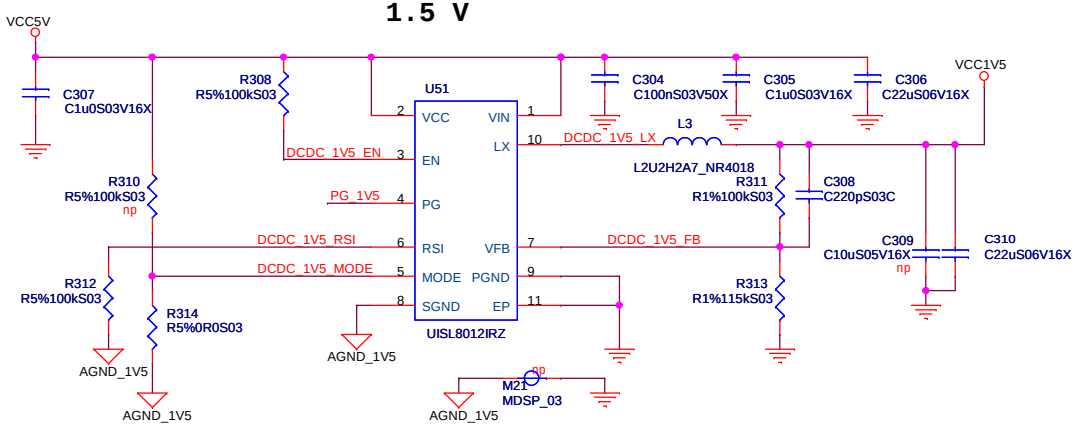




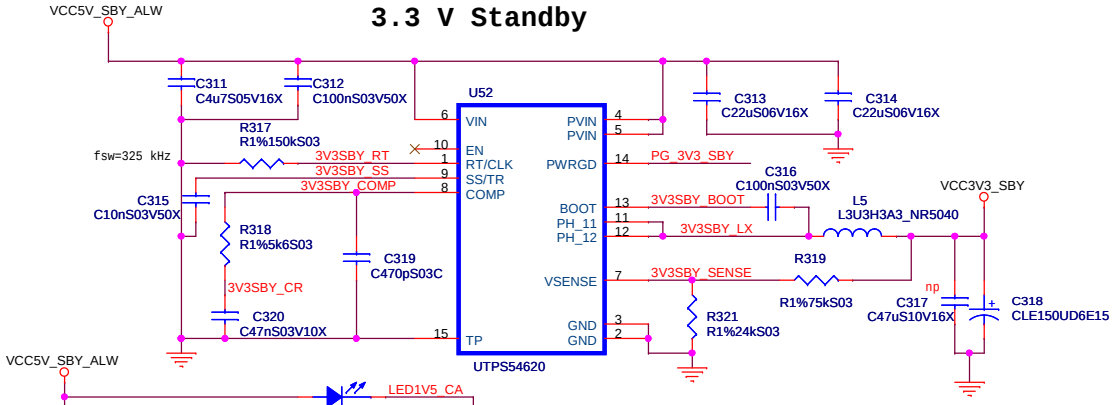


set jumper 1-2 for 80h / 84h (default)
set jumper 3-4 for 80h / 90h
set jumper 5-6 for 90h / 94h

1.5 V



3.3 V Standby



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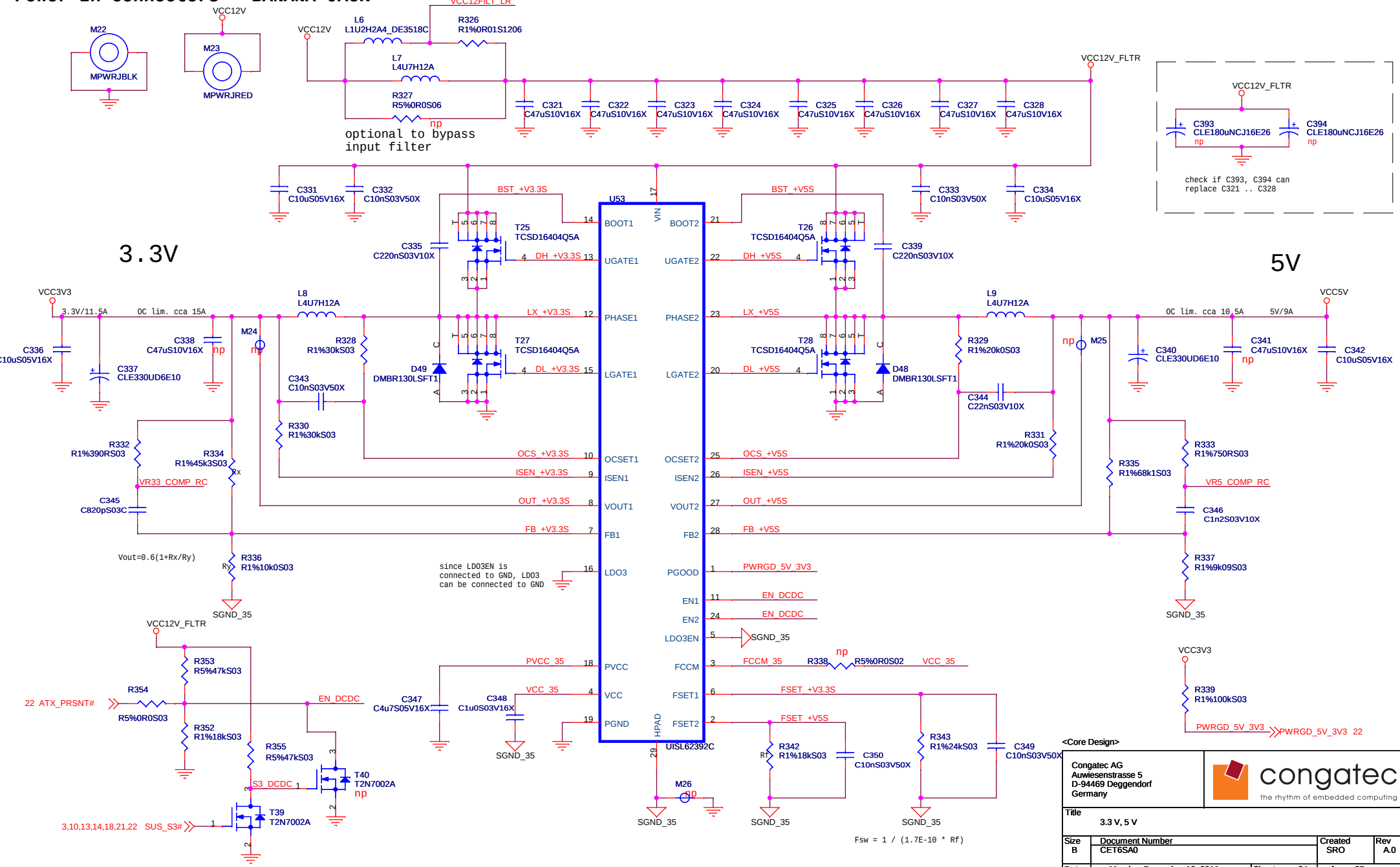
Title: 1.5 V, 3.3 V Standy, Postcode			
Size: B	Document Number: CET6SA0	Created: SRO	Rev: A.0
Date: Thursday, December 01, 2011	Sheet 23 of 25		

Power In connectors - BANANA JACK



HISTORY

10.01.2011	SRO	design created
19.08.2011	SRO	page 3: set SUS_S3# buffer to be populated page 4: swapped connection of DDI2_AUX, DDI3_AUX page 6: changed SHLDGND - GND connection page 7: exchanged UPI6C21200 by UICS9DB1233 (PCIe Gen. 3 compatible Clock Buffer) page 9: connected X12.B17, B31, B81 to B48, to enable PCIe RefClk also with x1, x4 and x16 cards page 11: exchanged SATA connectors page 13, 14: swapped connection of TMDS_B_CLK and TMDS_C_CLK at U29, U30, added circuitry to connect DDC-PU only in TMDS mode page 18: changed oscillator at Super I/O from 48 MHz to 24 MHz mirrored X42, X44 to be compatible to conga-adapPS2 page 19: connected U39.24, U39.25, U40.24, U40.25 to VCC5V to enable RS232 Levelshifter swapped DTR and TXD signals at X47, X62 to maintain compatibility to conga-CEVAL page 20: added PU at SPI_CS# to ensure stable level at SPI flash page 21: changed connection of X53.1 and X53.3 from 3.3V to 5V page 22: changed VCC5V_SBY_ALW Oring circuit added overvoltage protection circuit to Disk Drive Power Connector General: changed connection of I/O connector's shield from SHLDGND to GND General: changed CLE150UC6E25 to CLE150UD6E15

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Title: History				
Size: A4	Document Number: CET6SX0		Created: SRO	Rev: X.0
Date: Monday, December 12, 2011		Sheet 25 of 25		