COM Express™ conga-TC87

4th Generation Intel® Core™ i7, i5, i3 and Mobile Intel® Celeron Single Chip Ultra Low TDP Processors

User's Guide

Revision 1.7

congatec

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2013-11-14	AEM	• Preliminary release
1.0	2014-03-27	AEM	• Updated section 2.5 “Power Consumption” • Updated section 3 “Block Diagram” • Corrected the name of the congatec board controller in section 5.1.6 “I2C Bus Fast Mode” • Corrected pins D63 and D64 in section 8.4 “C-D Connector Pinout” • Added section 10 “BIOS Setup Description” • Official release
1.1	2014-07-09	AEM	• Updated section 10 “BIOS Setup Description”
1.2	2014-10-24	AEM	• Added three additional variants to conga-TC87 Options Information table in section 1 and updated section 2.5 “Power Consumption” • Added note about the high CMOS current drawn by rev. C.x and earlier in section 2.6.1 “CMOS Battery Power Consumption” • Added note about the ULP mode in section 6.1.4 “Gigabit Ethernet” • Updated section 6.2.3 “Digital Display Interface” • Updated section 7.3 “Watchdog” • Updated section 8.2.5 “Intel Virtualization Technology” • Updated section 11 “BIOS Setup Description” • Added note about the configuration of fan_pwm pin as push-pull in table 15 “Miscellaneous Signal Description” and section 11.4.6 “ACPI Submenu”
1.3	2016-08-26	AEM	• Updated section 1 “Introduction” and corrected the graphic information for the Intel Celeron 2980U in table 2 “conga-TC87 Variants” • Added Windows 10 to section 2.2 “Supported Operating Systems” • Updated section 2.5 “Power Consumption” and section 3 “Block Diagram” • Changed section 4 “Heatspreader” to “Cooling Solutions”. Added additional sub-sections • Updated section 6.1.10 “LVDS/eDP” • Corrected the description of PWRBTN# signal in table 17 “Power and System Management Signal Descriptions”. Also deleted the comment “not supported” for SUS_S4# signal • Updated section 11 “BIOS Setup Description”
1.4	2020-08-19	AEM	• Updated SMB_ALERT# pull-up column in table 27 “Power and System Management Signal Descriptions” • Added note about the minimum pulse width required for proper button detection in table 27 “Power and System Management Signal Descriptions” • Restructured and updated section 2.5 “Power Consumption” • Updated section 4 “Cooling Solutions” and added section 4.3 “CSA Dimensions” • Added section 6.1.4 “VGA” and section 7.1.5 “Fan Control” • Updated the link for the power supply implementation guidelines in section 6.1.12 “Power Control” • Added information about the congatec MLF file in section 12 “Additional BIOS Features” • Added section 12.1 “BIOS Versions” • Updated sections 12.2 “Updating the BIOS” and 12.3 “Supported Flash Devices” • Deleted section 13 “Industry Specifications”

1.5	2021-04-19		• Updated table 2 “conga-TC87 Variants”, table 3 “Feature Summary”, table 8 “Display Combination (U-processor line) and table 15 “HDMI Signal Descriptions” • Updated section 3 “Block Diagram”, section 6.1.3 “Digital Display Interface” • Deleted section 6.1.3.1 “HDMI” and section 6.1.3.2 “DVI”
1.6	2021-08-02	AEM	• Added Software License Information • Changed congatec AG to congatec GmbH • Updated the Power Supply Implementation Guidelines in section 6.1.12 “Power Control” • Updated section 7.3 “congatec Battery Management Interface”
1.7	2021-11-16	AEM	• Deleted HDMI references from section 1.2 “Options Information”, section 2.1 “Feature List”, section 3 “Block Diagram and section 6.1.3 “Display Interfaces”

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-TC87. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide
COM Express™ Specification

The links to these documents can be found on the congatec GmbH website at www.congatec.com

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Terminology

Term	Description
GB	Gigabyte
GHz	Gigahertz
kB	Kilobyte
MB	Megabyte
Mbit	Megabit
MHz	Megahertz
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
PCH	Platform Controller Hub
eDP	Embedded DisplayPort
HDA	High Definition Audio
N.C	Not connected
N.A	Not available
TMDS	Transition-Minimized Differential Signaling
TBD	To be determined
ULP	Ultra Low Power

Contents

List of Tables

1 Introduction

1.1 COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express™ modules are available in following form factors:

- Mini 84mm x 55mm
- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x110mm

Table 1 COM Express™ Specification 2.1 Pinout Types

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports	USB 2.0/ USB 3.0	Display Interfaces
Type 1	A-B	Up to 6			1	8 / 0	VGA, LVDS
Type 2	A-B C-D	Up to 22	32 bit	1	1	8 / 0	VGA, LVDS,PEG/SDVO
Type 3	A-B C-D	Up to 22	32 bit		3	8 / 0	VGA,LVDS,PEG/SDVO
Type 4	A-B C-D	Up to 32		1	1	8 / 0	VGA,LVDS,PEG/SDVO
Type 5	A-B C-D	Up to 32			3	8 / 0	VGA,LVDS,PEG/SDVO
Type 6	A-B C-D	Up to 24			1	8 / 4	VGA,LVDS,PEG, 3x DDI
Type 10	A-B	Up to 4			1	8 / 0	1x DDI

The conga-TC87 modules use the Type 6 pinout definition and comply with COM Express 2.1 specification. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 6 pinout provides the ability to offer PCI Express, Serial ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

1.2 Options Information

The conga-TC87 is currently available in seven variants. The table below shows the different configurations available.

Table 2 conga-TC87 Variants

Part-No.	046901	046902	046903	046904
Processor	Intel® Core™ i7-4650U 1.7 GHz Dual Core™	Intel® Core™ i5-4300U 1.9 GHz Dual Core™	Intel® Core™ i3-4010U 1.7 GHz Dual Core™	Intel® Celeron® 2980U 1.6 GHz Dual Core™
Intel® Smart Cache	4 MByte	3 MByte	3 MByte	2 MByte
Max. Turbo Frequency	3.3 GHz	2.9 GHz	N.A	N.A
Memory (DDR3L)	1600 MT/s dual channel	1600 MT/s dual channel	1600 MT/s dual channel	1600 MT/s dual channel
Processor Graphics	Intel® HD graphics 5000 (GT3)	Intel® HD graphics 4400 (GT2)	Intel® HD graphics 4400 (GT2)	Intel® HD graphics (GT1)
Graphics Max. Dynamic Freq	1.1 GHz	1.1 GHz	1.0 GHz	1.0 GHz
VGA	No	No	No	No
LVDS	Yes	Yes	Yes	Yes
DP++	Yes	Yes	Yes	Yes
Processor TDP (Max)	15 W	15 W	15 W	15 W

Part-No.	046906 (VGA)	046907 (VGA)	046908 (VGA)
Processor	Intel® Core™ i5-4300U 1.9 GHz Dual Core™	Intel® Core™ i3-4010U 1.7 GHz Dual Core™	Intel® Celeron® 2980U 1.6 GHz Dual Core™
Intel® Smart Cache	3 MByte	3 MByte	2 MByte
Max. Turbo Frequency	2.9 GHz	N.A	N.A
Memory (DDR3L)	1600 MT/s dual channel	1600 MT/s dual channel	1600 MT/s dual channel
Processor Graphics	Intel® HD graphics 4400 (GT2)	Intel® HD graphics 4400 (GT2)	Intel® HD graphics (GT1)
Graphics Max. Dynamic Freq	1.1 GHz	1.0 GHz	1.0 GHz
VGA	Yes	Yes	Yes
LVDS	Yes	Yes	Yes
DP++	Yes	Yes	Yes
Processor TDP (Max)	15 W	15 W	15 W

2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 6 Rev. 2.1 (Compact size 95 x 95 mm)	
Processor	4th Generation Intel® Core™ i7, i5, i3 and Intel® Celeron® SoCs	
Memory	Two memory sockets (located on the top and bottom side of the conga-TC87). Supports - SO-DIMM non-ECC DDR3L (low voltage @ 1.35V) modules - Data rates up to 1600 MT/s - Maximum 16 GB capacity	
Chipset	Intel® 8 Series PCH-LP integrated in the Multi-Chip Package (MCP)	
Audio	High Definition Audio interface with support for multiple codecs	
Ethernet	Gigabit Ethernet support via the onboard Intel® I218LM GbE Phy. Also offers AMT 9.5 support	
Graphics Options	Next Generation Intel® HD Graphics (4400/5000)	
	2x DP++ 1x LVDS Optional eDP interface (assembly option) Optional VGA interface (assembly option)	**NOTE**: [1] *LVDS will not be supported if optional eDP is implemented* [2] *Only hardware revisions C.x and later offer optional VGA* [3] *The conga-TC87 does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.*
Peripheral Interfaces	4x SATA® 6Gb/s with RAID 0/1/5/10 (Celeron variants support only 2x SATA) 4 PCI Express® Gen 2 Lanes. 8x USB 2.0 2x USB 3.0 2x UART	LPC Bus I²C Bus, Fast Mode, multi-master SM Bus SPI GPIOs
congatec Board Controller	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, hardware monitoring, fan control, I2C bus, Power loss control	
BIOS	AMI Aptio® V UEFI 2.x firmware, 8/16 MB serial SPI with congatec Embedded BIOS features	
Power Management	ACPI 4.0 compliant with battery support. Also supports Suspend to RAM (S3) and Intel AMT 9.5 Configurable TDP Ultra low standby power consumption, Deep Sx	
Security	Optional discrete Trusted Platform Module "TPM 1.2"; new AES Instructions for faster and better encryption	

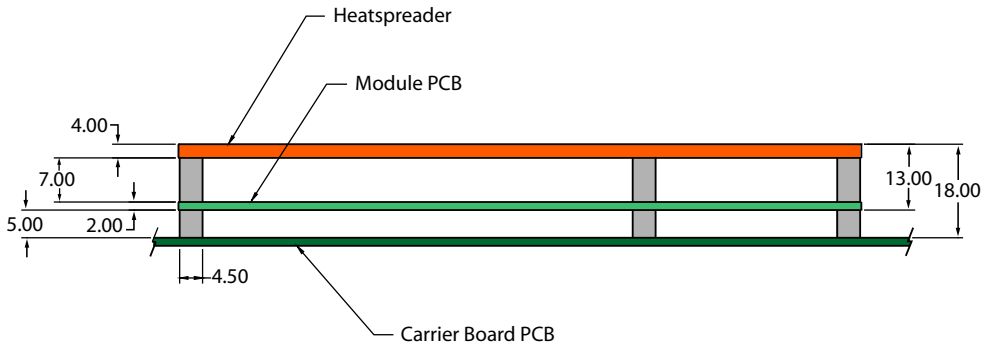
2.2 Supported Operating Systems

The conga-TC87 supports the following operating systems.

- Microsoft® Windows® 10
- Microsoft® Windows® 8
- Microsoft® Windows® 7
- Microsoft® Windows® Embedded Standard
- Linux

2.3 Mechanical Dimensions

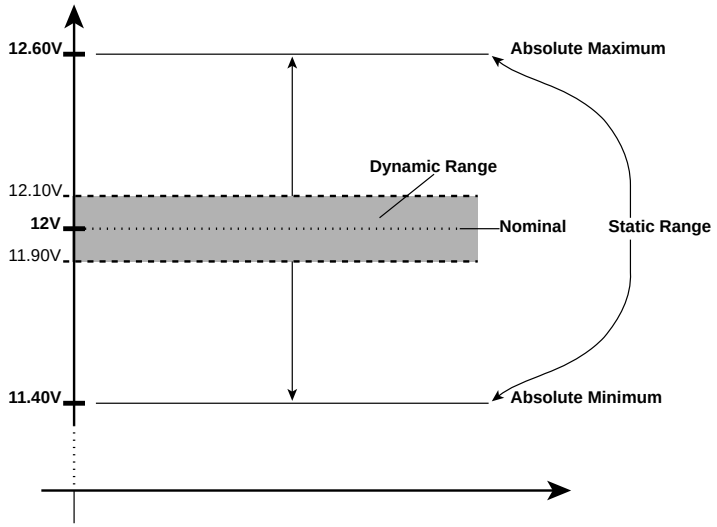
- 95.0 mm x 95.0 mm (3.74” x 3.74”)
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used, then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used, then approximate overall height is 21mm.



2.4 Supply Voltage Standard Power

- 12V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-TC87 COM
- modified congatec carrier board
- conga-TC87 cooling solution
- Microsoft Windows 7 (64 bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool

Table 4 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	The CPU was stressed to its maximum frequency
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency
S0: Peak value	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	COM is powered by VCC_5V_SBY	
S5	COM is powered by VCC_5V_SBY	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Table 5 Power Consumption Values

The table below provides additional information about the conga-TC87 power consumption. The values were recorded at various operating modes.

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (A)			
					Variant	Cores	Freq. /Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S3
046901	4 GB	B1	TU87R005	Windows 7	Intel® Core™ i7-4650U	2	1.7 / 3.3	0.23	2.41	2.60	0.06
046902	4 GB	B1	TU87R005	Windows 7	Intel® Core™ i5-4300U	2	1.9 / 2.9	0.28	1.95	2.35	0.06
046903	4 GB	B1	TU87R005	Windows 7	Intel® Core™ i3-4010U	2	1.7 / N.A	0.23	1.67	1.81	0.06
046904	4 GB	C0	TU87R005	Windows 7	Intel® Celeron® 2980U	2	1.6 / N.A	0.26	1.32	1.39	0.08

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 6 CMOS Battery Power Consumption

RTC @	Voltage	Current
20°C	3V DC	9.0 µA

Note

1. *The current drawn by the CMOS battery on hardware revision C.x and earlier is significantly higher than normal (see table above) because the PM_PCH_PWROK signal is not terminated to ground. This issue is resolved with conga-TC87 hardware revisions D.x and later. Contact congatec technical support center for more information.*

2. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*

3. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*

4. *Consider also the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*

5. *We recommend to always have a CMOS battery present when operating the conga-TC87.*

2.7 Environmental Specifications

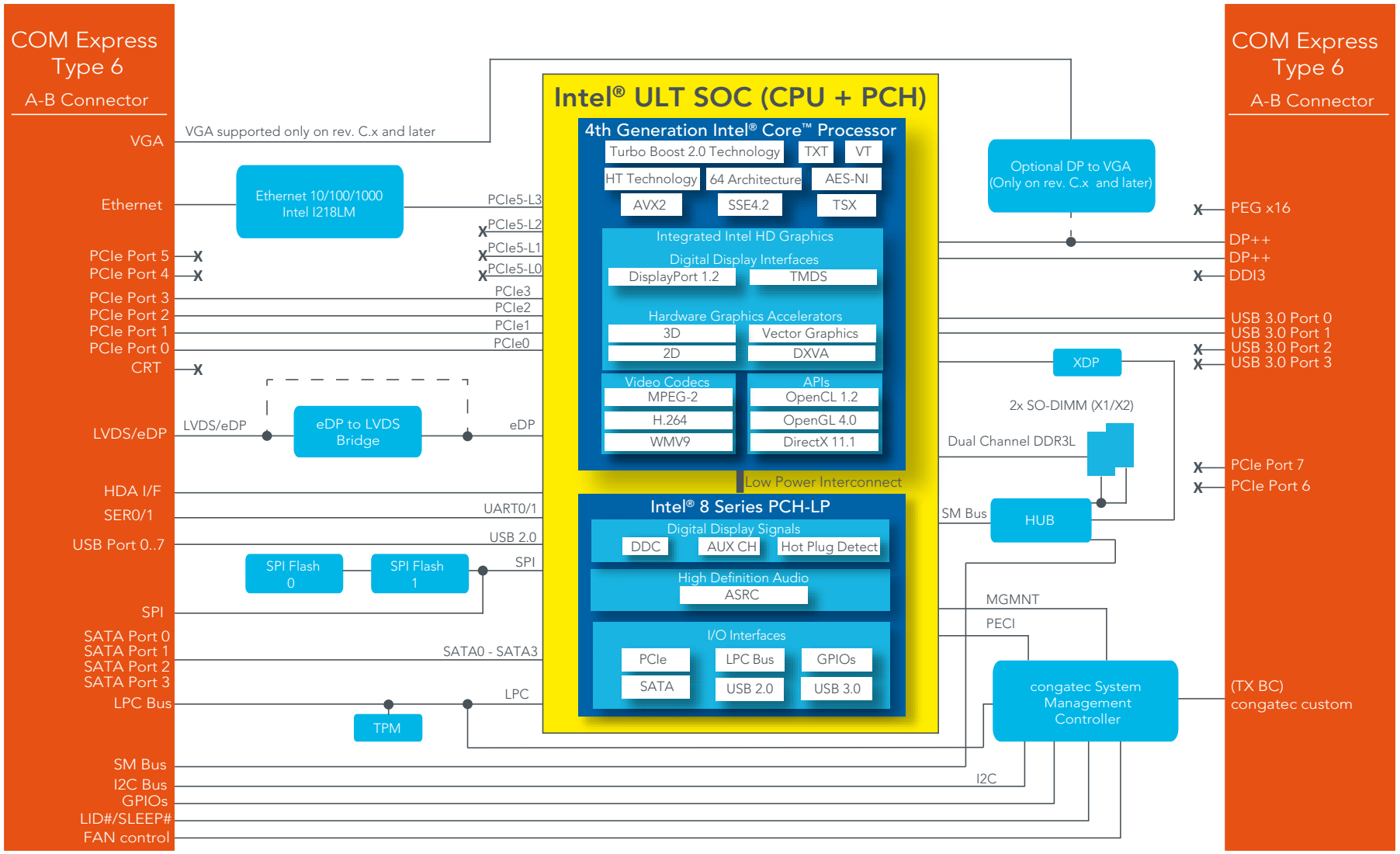
Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-TC87. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 7 Cooling Solution Variants

	Cooling Solution	Part No	Description
1	HSP	046953	Heatspreader with 2.7 mm bore-hole standoffs
		046954	Heatspreader with M2.5 mm threaded standoffs
2	CSP	046951	Passive cooling solution with 2.7 mm bore-hole standoffs
		046952	Passive cooling solution with M2.5 mm threaded standoffs
3	CSA	046955	Active cooling solution with 2.7 mm bore-hole standoffs
		046956	Active cooling with M2.5 mm threaded standoffs

Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*

2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

Caution

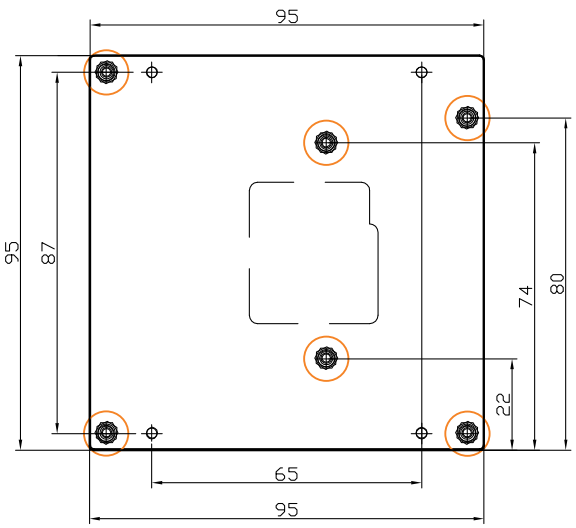
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

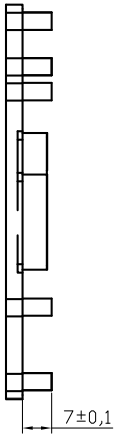
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

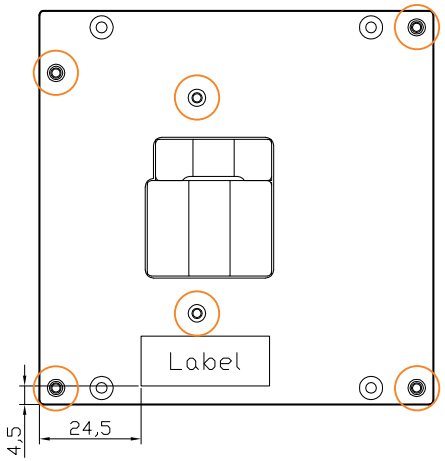
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

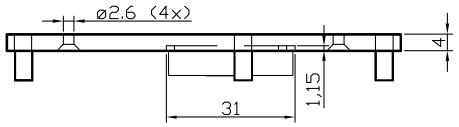
4.1 HSP Dimensions

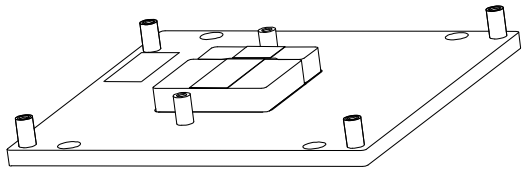




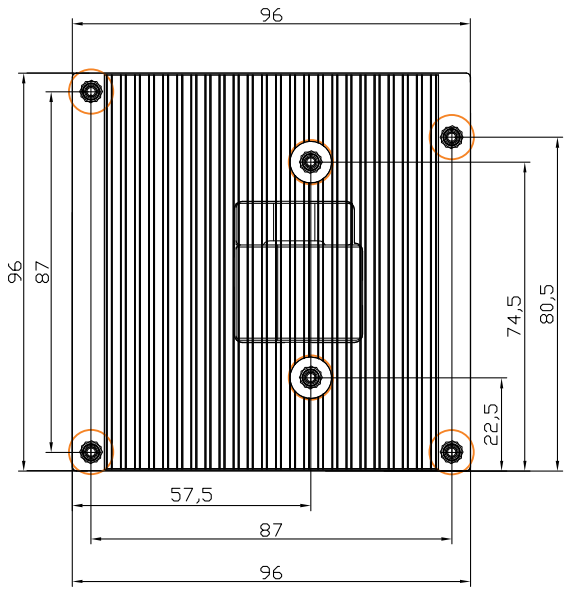


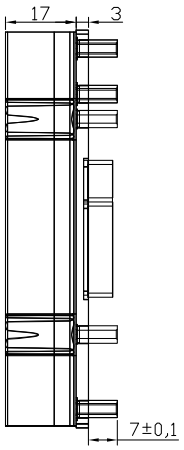
M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version

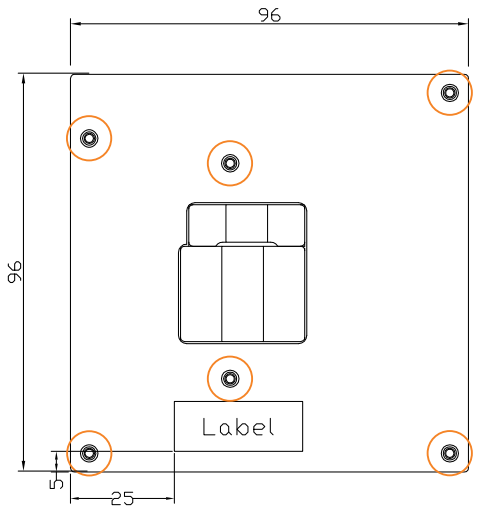


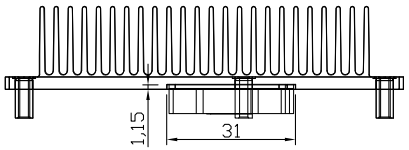


4.2 CSP Dimensions

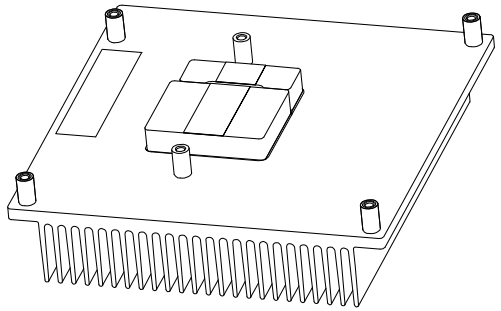




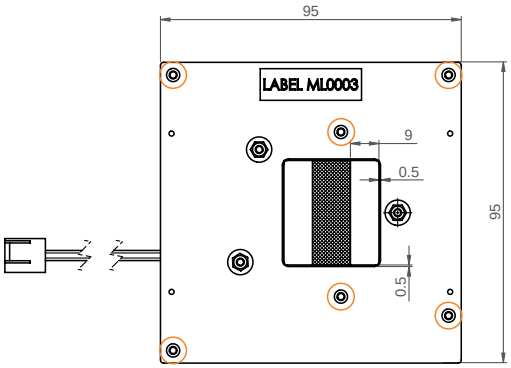


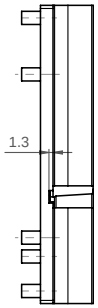


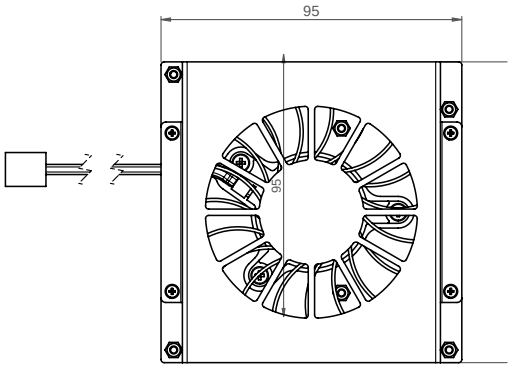
M2.5 x 10 mm
threaded standoff
for threaded version
or
ø2.7 x 10 mm
non-threaded standoff
for borehole version

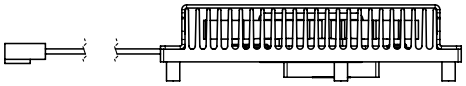


4.3 CSA Dimensions

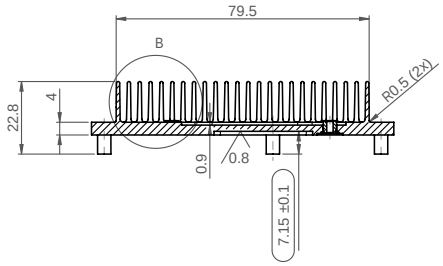


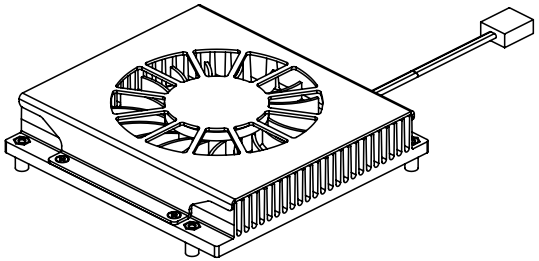


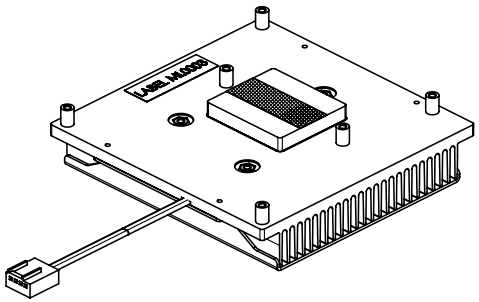


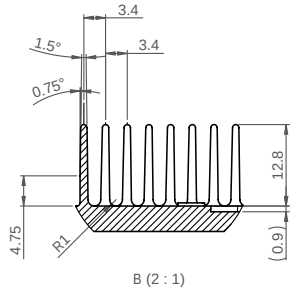


M2.5 x 10 mm
threaded standoff
for threaded version
or
ø2.7 x 10 mm
non-threaded standoff
for borehole version









5 Onboard Temperature Sensors

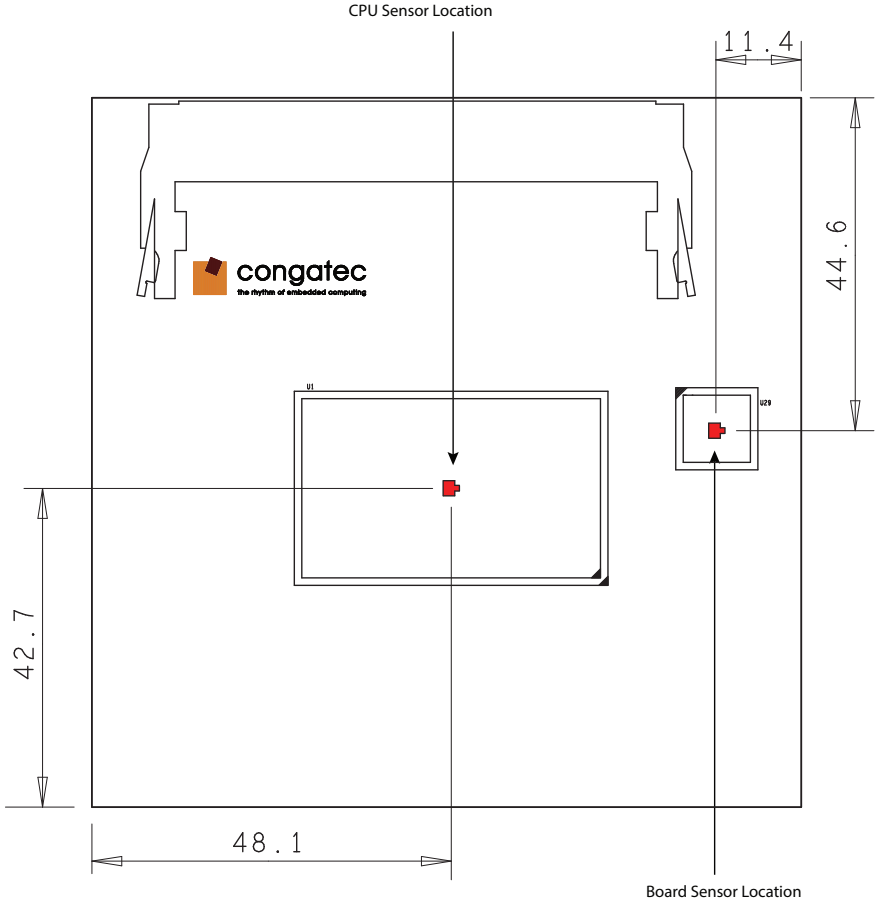
The conga-TC87 features two sensors on the top side of the module and an optional sensor (build-time) on the bottom side of the module.

Top-Side (CPU Temperature & Board Temperature Sensor) :

The CPU temperature sensor (T00) is located in the CPU (U1). This sensor measures the CPU temperature and is defined in CGOS API as CGOS_TEMP_CPU.

The board temperature sensor (T01) is located in the congatec Board Controller (cBC) . This sensor measures the board temperature and is defined in CGOS API as CGOS_TEMP_BOARD.

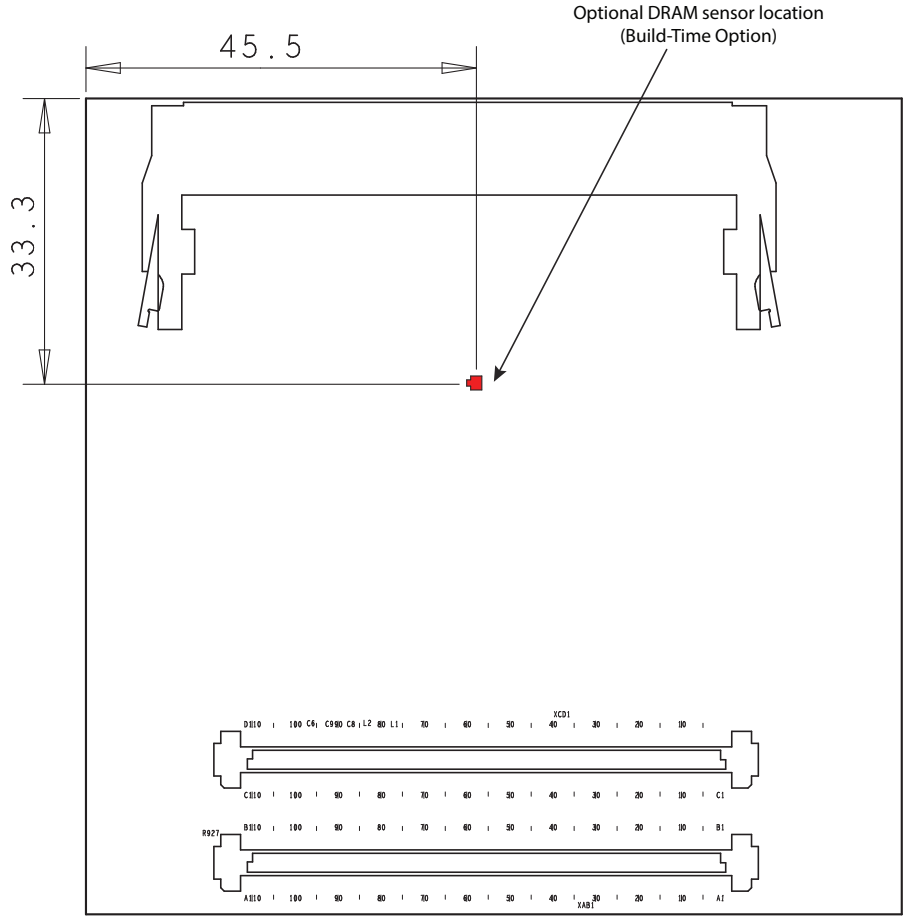
The sensor locations are shown below:



Bottom-Side (Optional DRAM Sensor):

The conga-TC87 offers an optional sensor on the bottom side of the module. This sensor measures the temperature of the DRAM module and is defined in CGOS API as CGOS_TEMP_BOTDIMM_ENV.

The DRAM sensor location is shown below:



Note

The DRAM sensor is not populated on conga-TC87 standard variants. The sensor is only available as a build time option.

6 Connector Subsystems Rows

The conga-TC87 is connected to the carrier board via two 220-pin connectors (COM Express Type 6 pinout). These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

6.1 Primary and Secondary Connector Rows

The following subsystems can be found on the primary and secondary connector rows.

6.1.1 PCI Express™

The conga-TC87 offers four PCI Express™ lanes on the A–B connector. The lanes support the following:

- up to 5 GT/s (Gen 2) speed
- default 4 x1 link configuration
- a 1 x4 link or a 2 x2 link via a special/customized BIOS firmware

6.1.2 PCI Express Graphics (PEG)

The Intel® ULT SoC does not support PEG interface.

6.1.3 Display Interfaces

The conga-TC87 supports the following:

- up to two DP++
- single- or dual-channel LVDS
- optional VGA [1] on revision C.x and later
- up to three independent displays (display combinations must be two DP++ (DP/TMDS) and one LVDS/eDP [2])

Note

1. *DDI2 supports optional VGA on revision C.x and later.*
2. *For revisions with VGA support, the combinations must be 1 x DDI1, 1 x VGA (DDI2) and 1 x LVDS/eDP.*

Table 8 Display Combination (U-processor line)

Display 1 (DDI1)	Display 2 (DDI2)	Display 3	Display 1 Max. Resolution	Display 2 Max. Resolution	Display 3 Max. Resolution
TMDS	TMDS	LVDS/eDP	4096x2304 @24Hz	4096x2304 @24Hz	3840x2160 @60Hz
DP	DP	LVDS/eDP	3840x2160 @60Hz	3840x2160 @60Hz	3840x2160 @60Hz
TMDS	DP	LVDS/eDP	4096x2304 @24Hz	3840x2160 @60Hz	3840x2160 @60Hz
DP	TMDS	LVDS/eDP	3840x2160 @60Hz	4096x2304 @24Hz	3840x2160 @60Hz

Note

1. *DP and eDP resolutions are supported for 4 lanes with link data rate HBR2 at 24 bits per pixel and single stream mode of operation.*
2. *DisplayPort Aux CH, DDC channel, panel power sequencing and HPD are supported through the PCH.*

6.1.3.1 DisplayPort (DP)

The conga-TC87 offers up to two DP ports. The ports support:

- VESA DisplayPort Standard
- data rate of 1.62 GT/s, 2.97 GT/s and 5.4 GT/s on 1, 2 or 4 data lanes
- up to 3840x2160 resolutions at 60 Hz
- Audio formats such as AC-3 Dolby Digital, Dolby Digital Plus, DTS-HD, LPCM, 192 KHz/24 bit, 8 channel, Dolby TrueHD, DTS-HD Master Audio (Lossless Blu-Ray Disc Audio Format)

Note

1. *The conga-TC87 supports a maximum of two independent DP displays.*
2. *Revisions equipped with optional VGA interface support only one DP interface.*

6.1.3.2 VGA

The Intel® ULT SoC does not support VGA interface; however, the conga-TC87 supports an optional VGA interface on DDI2 via NXP PTN3392BS Displayport to VGA controller.

Note

Revisions equipped with optional VGA interface support only one DP++ (DP/TMDS).

6.1.3.3 LVDS/eDP

The conga-TC87 offers an LVDS interface with optional eDP overlay on the A–B connector. The LVDS/eDP interface is configured to provide LVDS signals by default. The interface can optionally support eDP signals via a hardware change (assembly option).

The LVDS interface supports:

- single or dual channel LVDS (color depths of 18 bpp or 24 bpp)
- integrated flat panel interface with clock frequency up to 112 MHz
- automatic panel detection via Embedded Panel Interface
- VESA and OpenLDI LVDS color mappings
- resolution up to 1920x1200 in dual LVDS mode

Note

The LVDS/eDP interface supports either LVDS or eDP signals. Both signals are not supported simultaneously.

6.1.4 SATA

The conga-TC87 provides four SATA interfaces (SATA 0-3) on the A–B connector. The interfaces support:

- SATA specification, revision 3.0
- data transfer rates up to 6.0 Gb/s
- AHCI mode using memory space and RAID mode
- Hot-plug detect in non-native IDE mode

Note

1. *Celeron variants support only up to two SATA interfaces .*
2. *Legacy mode using I/O space is not supported.*

6.1.5 USB

The conga-TC87 offers eight USB 2.0 interfaces on the A–B connector and two SuperSpeed signals on the C–D connector. The EHCI host controller supports high-speed, full-speed and low-speed USB signaling and also complies with USB standard 1.1 and 2.0. The xHCI host controller allows data transfers of up to 5 Gb/s and supports SuperSpeed, high-speed, full-speed and low-speed traffic.

For more information about how the USB host controllers are routed, see section 8.4 "USB 2.0 EHCI Host Controller Support".

Note

The xHCI controller supports USB 3.0 debugging.

6.1.6 Gigabit Ethernet

The conga-TC87 offers a Gigabit Ethernet interface via an onboard Intel® i218-LM Phy. The interface supports full-duplex operation at 10/100/1000 Mbps and half-duplex operation at 10/100 Mbps.

Note

1. *The GBE0_LINK# output is not active during a 10 Mb connection. It is only active during a 100 Mb or 1 Gb connection. This is a limitation of Ethernet Phy since it has only three LED outputs—ACT#, LINK100# and LINK1000#.*

2. *The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TC87 module.*

3. *The Intel i218 device driver sets the controller's LED outputs to tri-state mode if in ULP mode. This may lit the Ethernet link and activity LEDs when Ethernet cable is not connected. This issue is common with older driver versions because their ULP feature is enabled by default and cannot be disabled. With newer driver versions, you can disable this feature. Therefore, for correct LED status, use the latest i218 device driver on the congatec website and also disable the ULP mode.*

6.1.7 High Definition Audio (HDA) Interface

The conga-TC87 provides an HDA interface for audio codec on the A–B connector.

6.1.8 LPC Bus

The conga-TC87 offers the LPC (Low Pin Count) bus through the Intel® 8 Series PCH-LP. For information about the decoded LPC addresses, see section 10.1.1 "LPC Bus".

6.1.9 I²C Bus Fast Mode

The I²C bus is implemented through the congatec board controller (Texas Instruments Tiva™ TM4E1231H6ZRB) and accessed through the congatec CGOS driver and API. The controller provides a fast mode multi-master I²C Bus that has maximum I²C bandwidth.

6.1.10 ExpressCard™

The conga-TC87 supports the implementation of ExpressCards, which requires the dedication of one USB 2.0 port or a x1 PCI Express link for each ExpressCard used.

6.1.11 General Purpose Serial Interface

The conga-TC87 offers two UART interfaces via two UART controllers integrated in the congatec Board Controller. These controllers support up to 1 MB/s and can operate in low-speed, full-speed and high-speed modes. The UART interfaces are routed to the A–B connector.

Note

1. *The UART interfaces require congatec driver to function.*

2. *The UART interfaces do not support legacy COM port emulation.*

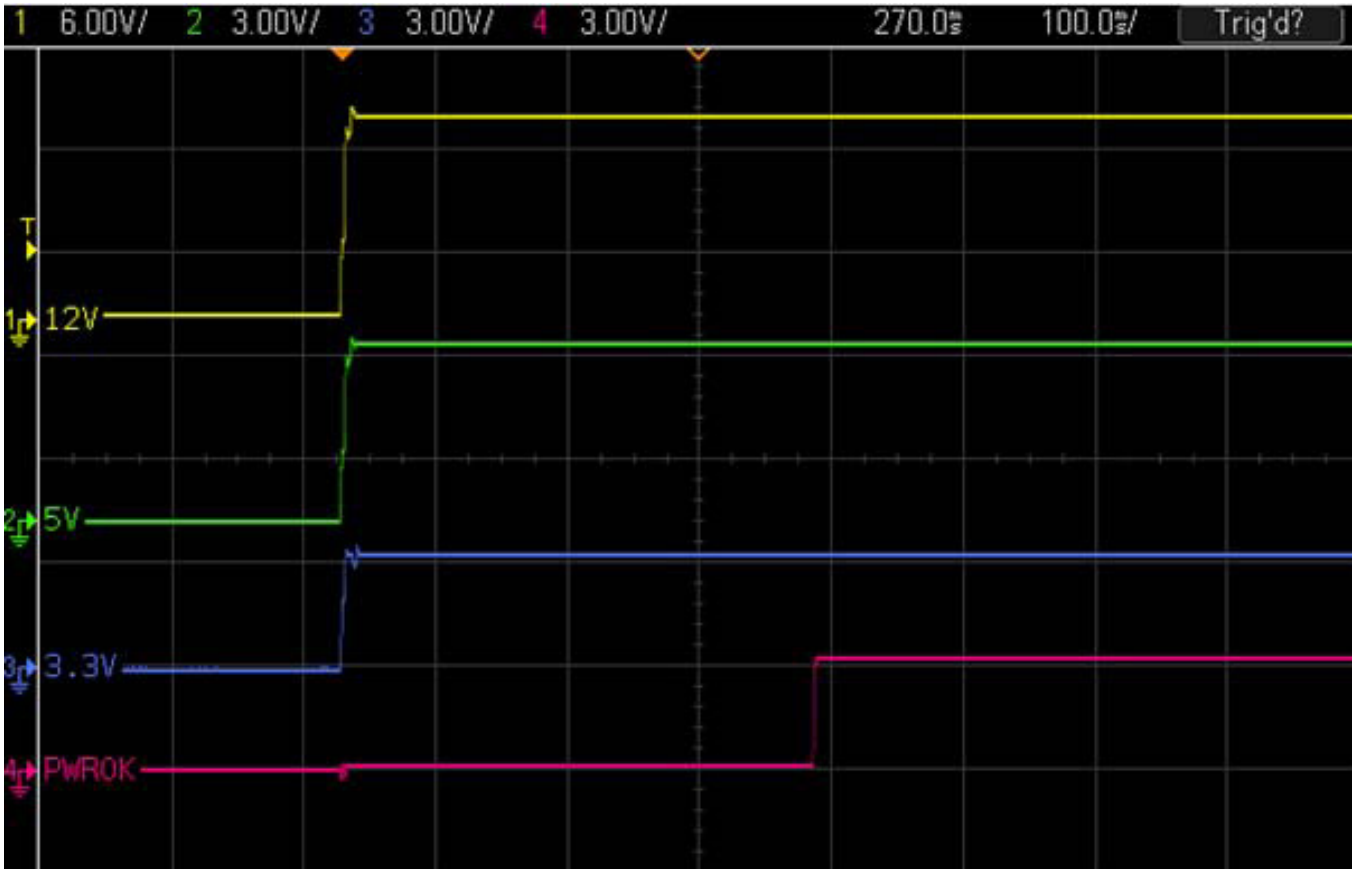
6.1.12 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system.

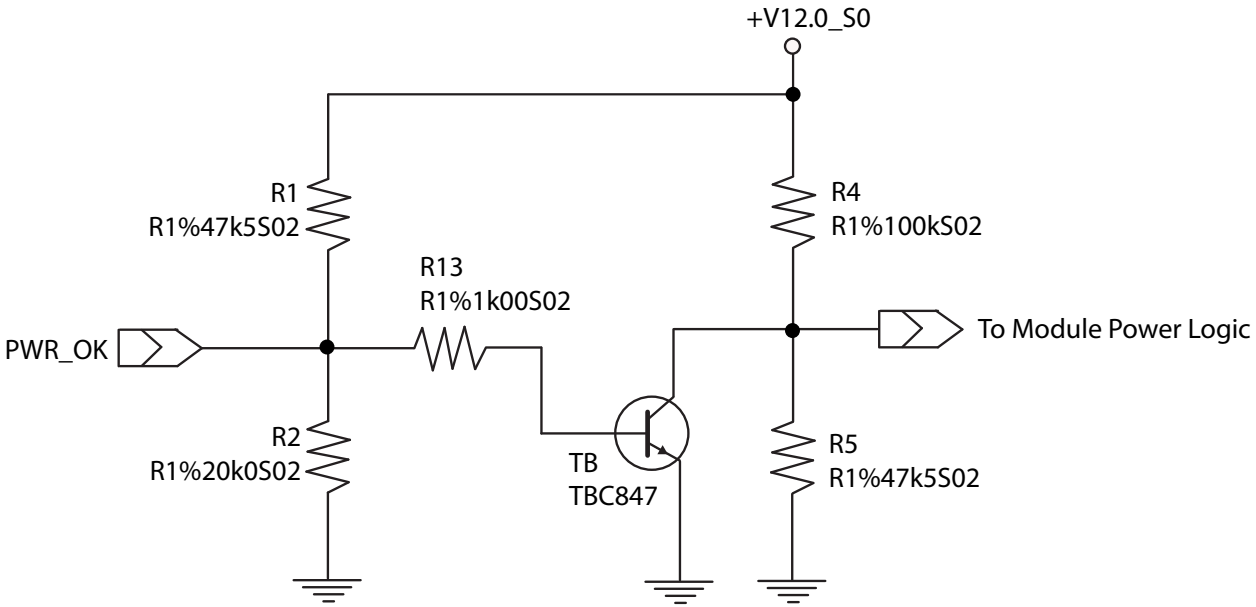
A sample screenshot is shown below:



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The conga-TC87 PWR_OK input circuitry is implemented as shown below:



The voltage divider ensures that the input complies with 3.3V CMOS characteristic and also allows for carrier board designs that are not driving PWR_OK. Although the PWR_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

When considering the above shown voltage divider circuitry and the transistor stage, the voltage measured at the PWR_OK input pin may be only around 0.8V when the 12V is applied to the module. Actively driving PWR_OK high is compliant to the COM Express specification but this can cause back driving. Therefore, congatec recommends driving the PWR_OK low to keep the module in reset and tri-state PWR_OK when the carrier board hardware is ready to boot.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the "power good" signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, it must be ensured that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-TC87 provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-TC87's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

The 12 volt input power is the sole operational power source for the conga-TC87. Other required voltages are generated internally on the module using onboard voltage regulators.

Note

When designing a power supply for a conga-TC87 application, be aware that the system may malfunction when a 12V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.

The cause of this problem is that some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.

To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope, during the power supply qualication phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

6.1.13 Power Management

ACPI

The conga-TC87 supports Advanced Configuration and Power Interface (ACPI) specification, revision 4.0a. It also supports Suspend to RAM (S3). For more information, see section 8.2 “ACPI Suspend Modes and Resume Events”.

DEEP Sx

The Deep Sx is a lower power state employed to minimize the power consumption while in S3/S4/S5. In the Deep Sx state, the system entry condition determines if the system context is maintained or not. All power is shut off except for minimal logic which supports limited set of wake events for Deep Sx. The Deep Sx on resumption, puts system back into the state it is entered from. In other words, if Deep Sx state was entered from S3 state, then the resume path will place system back into S3.

7 Additional Features

7.1 congatec Board Controller (cBC)

The conga-TC87 is equipped with Texas Instruments Tiva™ TM4E1231H6ZRB microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The board controller supports the following features:

7.1.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

7.1.2 Watchdog

The conga-TC87 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-TC87 does not support external hardware triggering. For more information about the Watchdog feature, see the BIOS setup description in section 11.4.2 “Watchdog Submenu” and application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

Note

The conga-TC87 module does not support the watchdog NMI mode.

7.1.3 I²C Bus

The conga-TC87 supports I²C bus. Thanks to the I²C host controller in the cBC, the I²C bus is multi-master capable and runs at fast mode.

7.1.4 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

7.1.5 Fan Control

The conga-TC87 has additional signals and functions to further improve system management. One of these signals is FAN_PWMOUT, an output signal that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

1. *A four wire fan must be used to generate the correct speed readout.*

2. *For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express Design Guide.*

7.2 OEM BIOS Customization

The conga-TC87 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide, which is called CGUTLm1x.pdf and can be found on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

7.2.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

7.2.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

7.2.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

7.2.4 OEM BIOS Code/Data

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table (OA2.0), Windows 8 OEM activation (OA3.0), verb tables for HDA codecs, PCI/PCIe opROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

7.2.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

7.3 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-TC87 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Manager interface, contact your local congatec sales representative.

7.4 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

7.5 Security Features

The conga-TC87 can be equipped optionally with a "Trusted Platform Module" (TPM 1.2).

7.6 Suspend to Ram

The Suspend to RAM feature is available on the conga-TC87.

8 conga Tech Notes

The conga-TC87 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

8.1 Intel® Processor Features

8.1.1 Thermal Monitor and Catastrophic Thermal Protection

Intel® Core™ i7/i5/i3 and Celeron® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu "CPU submenu".

The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel Speedstep transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.

THERMTRIP# signal is used by Intel®'s Core™ i7/i5/i3 and Celeron® processors for catastrophic thermal protection. If the processor's silicon reaches a temperature of approximately 125°C then the processor signal THERMTRIP# will go active and the system will automatically shut down to prevent any damage to the processor as a result of overheating. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

Note

1. *For THERMTRIP# to switch off the system automatically, use an ATX style power supply.*

2. *The maximum operating temperature for Intel® Core™ i7/i5/i3 and Celeron® processors is 100°C.*

3. *To ensure that the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Core™ i7/i5/i3 and Celeron® processor's respective datasheet can provide you with more information about this subject.*

8.1.2 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits. Intel® Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state. The maximum frequency of Intel® Turbo Boost Technology is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost 2 Technology state depends on the workload and operating environment. Any of the following can set the upper limit of Intel® Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase by 100 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached. For more information about Intel® Turbo Boost 2 Technology visit the Intel® website.

Note

Only conga-TC87 module variants that feature the Core™ i7 and i5 processors support Intel® Turbo Boost 2 Technology. Refer to the power consumption tables in section 2.5 "Power Consumption"for information about the maximum turbo frequency available for each conga-TC87 variant.

8.1.3 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel VT and is verified on all current congatec x86 hardware.

Note

congatec supports RTS Hypervisor.

8.1.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-TC87 supports Critical Trip Point. This cooling policy ensures that the operating system shuts down properly if the temperature in the thermal zone reaches a critical point, in order to prevent damage to the system as a result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

Use the setup nodes in the BIOS setup program to establish the appropriate trip points.

8.1.5 Processor Performance Control

Intel® Core™ i7/i5/i3 and Celeron® processors found on the conga-TC87 run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it's not being fully used. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that the power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

8.2 ACPI Suspend Modes and Resume Events

The conga-TC87 supports S3 (Suspend to RAM). For more information about S3 wake events, see section 11.4.6 “ACPI Submenu”.

Note

S4 (Suspend to Disk) is not supported.

Table 9 Wake Events

The table below lists the events that wake the system from S3.

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S3-S5.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device or set Resume On PME# to “Enabled” in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check ‘Allow this device to bring the computer out of standby’.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

8.3 Low Voltage Memory (DDR3L)

The Haswell ULT processor featured on the conga-TC87 supports low voltage system memory interface. The memory interface I/O voltage is 1.35V and supports non-ECC, unbuffered DDR3L SO-DIMMs. With this low voltage system memory interface on the processor, the conga-TC87 offers a system optimized for lowest possible power consumption. The reduction in power consumption due to lower voltage subsequently reduces the heat generated.

Caution

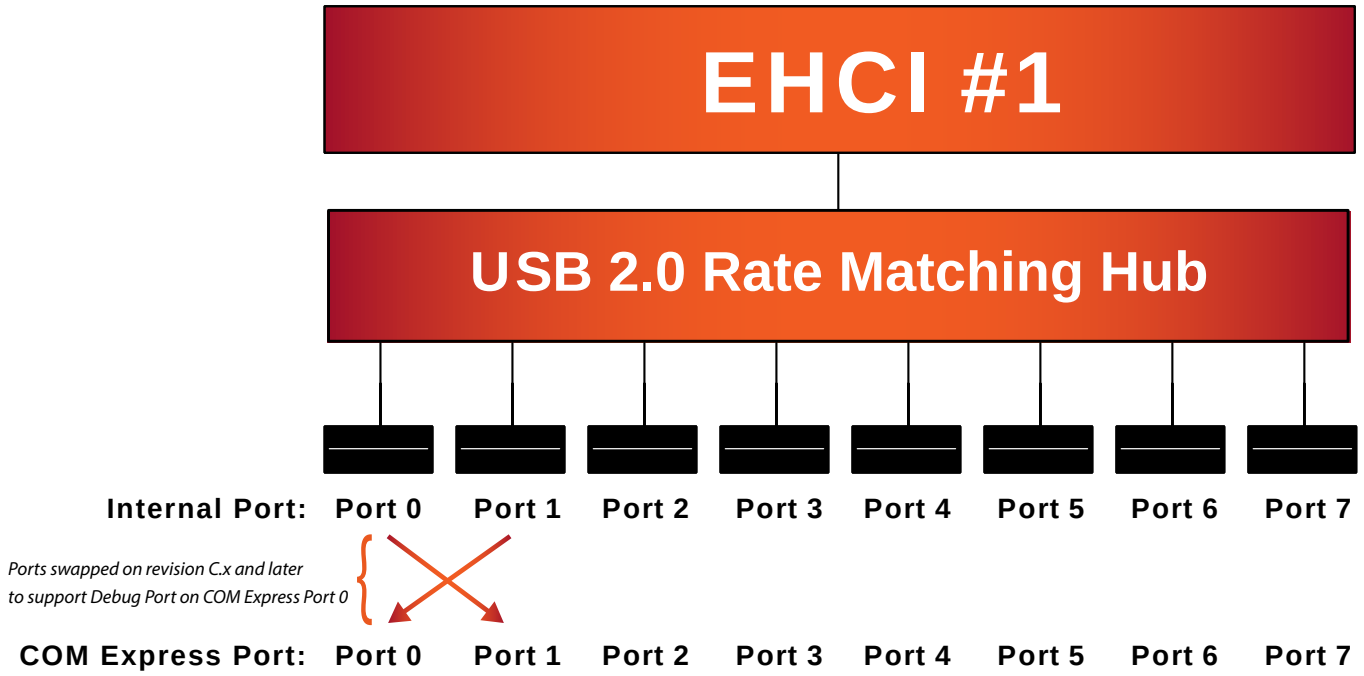
The usage of DDR3@1.5V SO-DIMM modules may affect the stability or boot-up of the conga-TC87. Therefore use only non-ECC, unbuffered DDR3L SO-DIMM memory modules up to 1600 MT/s on the conga-TC87.

8.4 USB 2.0 EHCI Host Controller Support

The 8 available USB ports are provided by a USB 2.0 Rate Matching Hub (RMH) integrated within the Intel® 8 Series PCH-LP . The EHCI controller is connected to the hub as shown below. The Hub convert low and full-speed traffic into high-speed traffic. When the RMHs are enabled, they will appear to software like an external hub is connected to Port 0 of the EHCI controller. In addition, port 1 of the RMH is multiplexed with Port 1 of the EHCI controller and is able to bypass the RMH for use as the Debug Port. The hub operates like any USB 2.0 Discrete Hub and will consume one tier of hubs allowed by the USB 2.0 Specification.

A maximum of four additional non-root hubs can be supported on any of the PCH USB Ports. The RMH will report the following Vendor ID = 8087h and Product ID = 8000h.

Routing Diagram



9 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type 6 connectors used for congatec GmbH modules. The pinout of the modules complies with COM Express Type 6 Rev. 2.1.

The table below describes the terminology used in this section. The PU/PD column indicates if a pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors; only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 10 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0
PEG	PCI Express Graphics
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

9.1 Connector Signal Descriptions

Table 11 Connector A–B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4- (*)	B56	PCIE_RX4- (*)
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	eDP_TX2+/LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	eDP_TX2-/LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	eDP_TX1+/LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	eDP_TX1-/LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	eDP_TX0+/LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	eDP_TX0-/LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+	B22	SATA3_TX+	A77	eDP/LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX-	B23	SATA3_TX-	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP/LVDS_BKLT_EN
A25	SATA2_RX+	B25	SATA3_RX+	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX-	B26	SATA3_RX-	A81	eDP_TX3+/LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	eDP_TX3-/LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2	A83	eDP_AUX+/LVDS_I2C_CK	B83	eDP/LVDS_BKLT_CTRL
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	A84	eDP_AUX-/LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA_BITCLK	B32	SPKR	A87	eDP_HPD	B87	VCC_5V_SBY
A33	AC/HDA_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED (*)
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN (*)
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU (*)
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC (*)
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC (*)
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK (*)
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT (*)
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+ (*)	B52	PCIE_RX5+ (*)	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5- (*)	B53	PCIE_RX5- (*)	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+ (*)	B55	PCIE_RX4+ (*)	A110	GND (FIXED)	B110	GND (FIXED)

Note

The signals marked with asterisk symbol (*) are not supported on the conga TC87.

Table 12 Connector C–D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1- (*)	D56	PEG_TX1- (*)
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+ (*)	D58	PEG_TX2+ (*)
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2- (*)	D59	PEG_TX2- (*)
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PEG_RX3+ (*)	D61	PEG_TX3+ (*)
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PEG_RX3- (*)	D62	PEG_TX3- (*)
C8	GND	D8	GND	C63	RSVD	D63	RSVD
C9	USB_SSRX2- (*)	D9	USB_SSTX2- (*)	C64	RSVD	D64	RSVD
C10	USB_SSRX2+ (*)	D10	USB_SSTX2+ (*)	C65	PEG_RX4+ (*)	D65	PEG_TX4+ (*)
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4- (*)	D66	PEG_TX4- (*)
C12	USB_SSRX3- (*)	D12	USB_SSTX3- (*)	C67	RSVD	D67	GND
C13	USB_SSRX3+ (*)	D13	USB_SSTX3+ (*)	C68	PEG_RX5+ (*)	D68	PEG_TX5+ (*)
C14	GND	D14	GND	C69	PEG_RX5- (*)	D69	PEG_TX5- (*)
C15	DDI1_PAIR6+ (*)	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	DDI1_PAIR6- (*)	D16	DDI1_CTRLDATA_AUX-	C71	PEG_RX6+ (*)	D71	PEG_TX6+ (*)
C17	RSVD	D17	RSVD	C72	PEG_RX6- (*)	D72	PEG_TX6- (*)
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	PCIE_RX6+ (*)	D19	PCIE_TX6+ (*)	C74	PEG_RX7+ (*)	D74	PEG_TX7+ (*)
C20	PCIE_RX6- (*)	D20	PCIE_TX6- (*)	C75	PEG_RX7- (*)	D75	PEG_TX7- (*)
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+ (*)	D22	PCIE_TX7+ (*)	C77	RSVD	D77	RSVD
C23	PCIE_RX7- (*)	D23	PCIE_TX7- (*)	C78	PEG_RX8+ (*)	D78	PEG_TX8+ (*)
C24	DDI1_HPD	D24	RSVD	C79	PEG_RX8- (*)	D79	PEG_TX8- (*)
C25	DDI1_PAIR4+ (*)	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	DDI1_PAIR4- (*)	D26	DDI1_PAIR0+	C81	PEG_RX9+ (*)	D81	PEG_TX9+ (*)
C27	RSVD	D27	DDI1_PAIR0-	C82	PEG_RX9- (*)	D82	PEG_TX9- (*)
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD
C29	DDI1_PAIR5+ (*)	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	DDI1_PAIR5- (*)	D30	DDI1_PAIR1-	C85	PEG_RX10+ (*)	D85	PEG_TX10+ (*)
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- (*)	D86	PEG_TX10- (*)
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-	C88	PEG_RX11+ (*)	D88	PEG_TX11+ (*)
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11- (*)	D89	PEG_TX11- (*)
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+ (*)	D36	DDI1_PAIR3+	C91	PEG_RX12+ (*)	D91	PEG_TX12+ (*)
C37	DDI3_CTRLDATA_AUX- (*)	D37	DDI1_PAIR3-	C92	PEG_RX12- (*)	D92	PEG_TX12- (*)
C38	DDI3_DDC_AUX_SEL (*)	D38	RSVD	C93	GND	D93	GND
C39	DDI3_PAIR0+ (*)	D39	DDI2_PAIR0+	C94	PEG_RX13+ (*)	D94	PEG_TX13+ (*)
C40	DDI3_PAIR0- (*)	D40	DDI2_PAIR0-	C95	PEG_RX13- (*)	D95	PEG_TX13- (*)
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+ (*)	D42	DDI2_PAIR1+	C97	RVSD	D97	RSVD
C43	DDI3_PAIR1- (*)	D43	DDI2_PAIR1-	C98	PEG_RX14+ (*)	D98	PEG_TX14+ (*)
C44	DDI3_HPD	D44	DDI2_HPD	C99	PEG_RX14- (*)	D99	PEG_TX14- (*)
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+ (*)	D46	DDI2_PAIR2+	C101	PEG_RX15+ (*)	D101	PEG_TX15+ (*)
C47	DDI3_PAIR2- (*)	D47	DDI2_PAIR2-	C102	PEG_RX15- (*)	D102	PEG_TX15- (*)
C48	RSVD	D48	RSVD	C103	GND	D103	GND
C49	DDI3_PAIR3+ (*)	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3- (*)	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+ (*)	D52	PEG_TX0+ (*)	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0- (*)	D53	PEG_TX0- (*)	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV# (*)	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+ (*)	D55	PEG_TX1+ (*)	C110	GND (FIXED)	D110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-TC87.

Table 13 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		Not supported
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 14 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs. *Note: Can also be used as PCI Express Receive Input differential pairs 16 through 31 known as PCIE_RX[16-31] + and -.*	I PCIE		Not supported.
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+ PEG_TX0- PEG_TX1+ PEG_TX1- PEG_TX2+ PEG_TX2- PEG_TX3+ PEG_TX3- PEG_TX4+ PEG_TX4- PEG_TX5+ PEG_TX5- PEG_TX6+ PEG_TX6- PEG_TX7+ PEG_TX7- PEG_TX8+ PEG_TX8- PEG_TX9+ PEG_TX9- PEG_TX10+ PEG_TX10- PEG_TX11+ PEG_TX11- PEG_TX12+ PEG_TX12- PEG_TX13+ PEG_TX13- PEG_TX14+ PEG_TX14- PEG_TX15+ PEG_TX15-	D52 D53 D55 D56 D58 D59 D61 D62 D65 D66 D68 D69 D71 D72 D74 D75 D78 D79 D81 D82 D85 D86 D88 D89 D91 D92 D94 D95 D98 D99 D101 D102	PCI Express Graphics Transmit Output differential pairs. *Note: Can also be used as PCI Express Transmit Output differential pairs 16 through 31 known as PCIE_TX[16-31] + and -.*	O PCIE		Not supported.
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I	PU 10k 3.3V	Not supported.

Note

The PCI Express Graphics interface is not supported on the conga-TC87.

Table 15 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with DP1_LANE0+ and TMDS1_DATA2+. Multiplexed with DP1_LANE0- and TMDS1_DATA2-.	O PCIE		
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with DP1_LANE1+ and TMDS1_DATA1+. Multiplexed with DP1_LANE1- and TMDS1_DATA1-.	O PCIE		
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with DP1_LANE2+ and TMDS1_DATA0+. Multiplexed with DP1_LANE2- and TMDS1_DATA0-.	O PCIE		
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with DP1_LANE3+ and TMDS1_CLK+. Multiplexed with DP1_LANE3- and TMDS1_CLK-.	O PCIE		
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	Multiplexed with SDVO1_INT+. Multiplexed with SDVO1_INT-.			Not supported
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	Multiplexed with SDVO1_TVCLKIN+. Multiplexed with SDVO1_TVCLKIN-.			Not supported
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	Multiplexed with SDVO1_FLDSTALL+. Multiplexed with SDVO1_FLDSTALL-.			Not supported
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD.	I 3.3V	PD 1M	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with DP1_AUX+ and HMDI1_CTRLCLK. DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PD100k	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with DP1_AUX- and HDMI1_CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PU 100k 3.3V	Boot strap signal (see note below). Enable strap is already populated.
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+ and TMDS2_DATA2+. Multiplexed with DP2_LANE0- and TMDS2_DATA2-.	O PCIE		
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+ and TMDS2_DATA1+. Multiplexed with DP2_LANE1- and TMDS2_DATA1-.	O PCIE		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+ and TMDS2_DATA0+. Multiplexed with DP2_LANE2- and TMDS2_DATA0-.	O PCIE		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+ and TMDS2_CLK+. Multiplexed with DP2_LANE3- and TMDS2_CLK-.	O PCIE		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD.	I 3.3V	PD 1M	
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+ and HDMI2_CTRLCLK. DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PD 100k	

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3V	PU 100k 3.3V	Boot strap signal (see note below). Enable strap is already populated.
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_ AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V		
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+. Multiplexed with DP3_LANE0- and TMDS3_DATA2-.	O PCIE		Not supported
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+. Multiplexed with DP3_LANE1- and TMDS3_DATA1-.	O PCIE		Not supported
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+. Multiplexed with DP3_LANE2- and TMDS3_DATA0-.	O PCIE		Not supported
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+. Multiplexed with DP3_LANE3- and TMDS3_CLK-.	O PCIE		Not supported
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD.	I 3.3V		Not supported
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK. DP AUX+ function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V		Not supported
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA. DP AUX- function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3V		Not supported
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_ AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V		Not supported

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.2 "Boot Strap Signals".

Table 16 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS1_CLK + TMDS1_CLK -	D36 D37	TMDS Clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
TMDS1_DATA0+ TMDS1_DATA0-	D32 D33	TMDS differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
TMDS1_DATA1+ TMDS1_DATA1-	D29 D30	TMDS differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-..	O PCIE		
TMDS1_DATA2+ TMDS1_DATA2-	D26 D27	TMDS differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
HDMI1_HPD	C24	TMDS Hot-plug detect. Multiplexed with DDI1_HPD.	I PCIE	PD 1M	
HDMI1_CTRLCLK	D15	TMDS I²C Control Clock Multiplexed with DDI1_CTRLCLK_AUX+	I/O OD 3.3V	PD 100k	
HDMI1_CTRLDATA [1]	D16	TMDS I²C Control Data Multiplexed with DDI1_CTRLDATA_AUX-	I/O OD 3.3V	PU 100k 3.3V	Boot strap signal (see note below). Enable strap is already populated.
TMDS2_CLK + TMDS2_CLK -	D49 D50	TMDS Clock output differential pair.. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-.	O PCIE		
TMDS2_DATA0+ TMDS2_DATA0-	D46 D47	TMDS differential pair. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-.	O PCIE		
TMDS2_DATA1+ TMDS2_DATA1-	D42 D43	TMDS differential pair. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-.	O PCIE		
TMDS2_DATA2+ TMDS2_DATA2-	D39 D40	TMDS differential pair. Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-..	O PCIE		
HDMI2_HPD	D44	TMDS Hot-plug detect. Multiplexed with DDI2_HPD	I PCIE	PD 1M	
HDMI2_CTRLCLK	C32	TMDS I²C Control Clock Multiplexed with DDI2_CTRLCLK_AUX+	I/O OD 3.3V	PD 100k	
HDM12_CTRLDATA [1]	C33	TMDS I²C Control Data Multiplexed with DDI2_CTRLDATA_AUX-	I/O OD 3.3V	PU 100k 3.3V	Boot strap signal (see note below). Enable strap is already populated.
TMDS3_CLK + TMDS3_CLK -	C49 C50	TMDS Clock output differential pair.. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		Not supported
TMDS3_DATA0+ TMDS3_DATA0-	C46 C47	TMDS differential pair. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		Not supported
TMDS3_DATA1+ TMDS3_DATA1-	C42 C43	TMDS differential pair. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-..	O PCIE		Not supported
TMDS3_DATA2+ TMDS3_DATA2-	C39 C40	TMDS differential pair. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		Not supported

Signal	Pin #	Description	I/O	PU/PD	Comment
HDMI3_HPD	C44	TMDS Hot-plug detect. Multiplexed with DDI3_HPD.	I PCIE		Not supported
HDMI3_CTRLCLK	C36	TMDS I²C Control Clock Multiplexed with DDI3_CTRLCLK_AUX+	I/O OD 3.3V		Not supported
HDMI3_CTRLDATA	C37	TMDS I²C Control Data Multiplexed with DDI3_CTRLDATA_AUX-	I/O OD 3.3V		Not supported

Note

1. *These signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.2 of this user's guide.*

2. *The conga-TC87 does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.*

Table 17 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE3+ DP1_LANE3-	D36 D37	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
DP1_LANE2+ DP1_LANE2-	D32 D33	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
DP1_LANE1+ DP1_LANE1-	D29 D30	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		
DP1_LANE0+ DP1_LANE0-	D26 D27	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
DP1_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI1_HPD.	I 3.3V	PD 1M	
DP1_AUX+	D15	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP1_AUX-	D16	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	Boot strap signal (see note below). Enable strap is already populated.
DP2_LANE3+ DP2_LANE3-	D49 D50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
DP2_LANE2+ DP2_LANE2-	D46 D47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		
DP2_LANE1+ DP2_LANE1-	D42 D43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		
DP2_LANE0+ DP2_LANE0-	D39 D40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR0+ and DDI1_PAIR0-	O PCIE		
DP2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI2_HPD.	I 3.3V	PD 1M	
DP2_AUX+	C32	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP2_AUX-	C33	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	Boot strap signal (see note below). Enable strap is already populated.
DP3_LANE3+ DP3_LANE3-	C49 C50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		Not supported
DP3_LANE2+ DP3_LANE2-	C46 C47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		Not supported
DP3_LANE1+ DP3_LANE1-	C42 C43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-.	O PCIE		Not supported
DP3_LANE0+ DP3_LANE0-	C39 C40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		Not supported
DP3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI3_HPD.	I 3.3V		Not supported
DP3_AUX+	C36	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE		Not supported
DP3_AUX-	C37	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE		Not supported

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.2 "Boot Strap Signals".

Table 18 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Optional on rev. C.x and later
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Optional on rev. C.x and later
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Optional on rev. C.x and later
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		Optional on rev. C.x and later
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		Optional on rev. C.x and later
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O OD 5V	PU 1k2 3.3V	Optional on rev. C.x and later
VGA_I2C_DAT	B96	DDC data line.	I/O OD 5V	PU 1k2 3.3V	Optional on rev. C.x and later

Table 19 Embedded DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eDP_TX3+ eDP_TX3- eDP_TX2+ eDP_TX2- eDP_TX1+ eDP_TX1- eDP_TX0+ eDP_TX0-	A81 A82 A71 A72 A73 A74 A75 A76	eDP differential pairs.	AC coupled off module.		eDP_TX2 and eDP_TX3 pairs are not supported on conga-TC87.
eDP_VDD_EN	A77	eDP power enable.	O 3.3V	PD 10k	
eDP_BKLT_EN	B79	eDP backlight enable.	O 3.3V	PD 10k	
eDP_BKLT_CTRL	B83	eDP backlight brightness control.	O 3.3V		
eDP_AUX+	A83	eDP AUX+.	AC coupled off module.		
eDP_AUX-	A84	eDP AUX-.	AC coupled off module.		
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification of the link layer.	I 3.3V		

Table 20 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10k	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10k	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	.

Table 21 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	I/O 3.3v		

Table 22 USB 2.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

Table 23 USB 3.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX0-	C3		I		
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX0-	D3		O		
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX1-	C6		I		
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX1-	D6		O		
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported.
USB_SSRX2-	C9		I		Not supported.
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported.
USB_SSTX2-	D9		O		Not supported.
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported.
USB_SSRX3-	C12		I		Not supported.
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported.
USB_SSTX3-	D12		O		Not supported.

Table 24 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/ PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		Twisted pair signals for external transformer.
			1000	100	10			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.				O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.				O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.				O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.						Not connected

Note

1. *The GBE0_LINK# output is not active during a 10 Mb connection. It is only active during a 100 Mb or 1 Gb connection. This is a limitation of Ethernet Phy since it has only three LED outputs—ACT#, LINK100# and LINK1000#.*

2. *The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TC87 module.*

3. *The Intel i218 device driver sets the controller's LED outputs to tri-state mode if in ULP mode. This may lit the Ethernet link and activity LEDs when Ethernet cable is not connected. This issue is common with older driver versions because their ULP feature is enabled by default and cannot be disabled. With newer driver versions, you can disable this feature. Therefore, for correct LED status, use the latest i218 device driver on the congatec website and also disable the ULP mode.*

Table 25 Intel® High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	**Intel® High Definition Audio Reset:** This signal is the master hardware reset to external codec(s).	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SYNC	A29	**Intel® High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_BITCLK	A32	**Intel® High Definition Audio Bit Clock Output:** This signal is a 24.000MHz serial data clock generated by the Intel® High Definition Audio controller.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SDOUT	A33	**Intel® High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3VSB	PU 1K 3.3VSB	AC'97 codecs are not supported. AC/HDA_SDOUT is a boot strap signal (see note below)
AC/HDA_SDIN[2:0]	B28-B30	**Intel® High Definition Audio Serial Data In [0]:** These signals are serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	I 3.3VSB		AC'97 codecs are not supported.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.2 "Boot Strap Signals".

Table 26 ExpressCard Support Pins Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request.	I 3.3V	PU 10k 3.3V	
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3V	PU 10k 3.3V	

Table 27 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V	PU 10k 3.3V	
LPC_SERIRQ	A50	LPC serial interrupt	I/O OD 3.3V	PU 10k 3.3V	
LPC_CLK	B10	LPC clock output - 24 MHz nominal	O 3.3V		

Table 28 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB		Carrier shall pull to SPI_POWER when external SPI provided but not used.
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	+ 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall be left as no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall be left as no-connect

Table 29 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O 3.3V	PU 2K2 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O 3.3V	PU 2K2 3.3VSB	
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		SPEAKER is a boot strap signal (see note below)
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PD 10K	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V	PU 10K 3.3V	
FAN_TACHIN	B102	Fan tachometer input.	I OD	PU 10K 3.3V	Requires a fan with a two pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V		Trusted Platform Module chip is optional.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 9.2 "Boot Strap Signals".

Table 30 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3V		SDIO interface is not supported on the conga-TC87
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3V		SDIO interface is not supported on the conga-TC87
GPO2	B57	General purpose output pins. Shared with SD_WP. Output from COM Express, input to SD	O 3.3V		SDIO interface is not supported on the conga-TC87
GPO3	B63	General purpose output pins. Shared with SD_CD. Output from COM Express, input to SD	O 3.3V		SDIO interface is not supported on the conga-TC87
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3V	PU 10K 3.3V	SDIO interface is not supported on the conga-TC87
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3V	PU 10K 3.3V	SDIO interface is not supported on the conga-TC87
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3V	PU 10K 3.3V	SDIO interface is not supported on the conga-TC87
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3V	PU 10K 3.3V	SDIO interface is not supported on the conga-TC87

Table 31 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V	PD 100k	
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V		Set by resistor divider to accept 3.3V.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB	PU 10k 3.3VSB	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		

Signal	Pin #	Description	I/O	PU/PD	Comment
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 1k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10k 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 10k 3.3V	
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10k 3.3V	
SMB_CK	B13	System Management Bus bidirectional clock line.	I/O 3.3VSB	PU 2k2 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line.	I/O OD 3.3VSB	PU 2k2 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3VSB		Revisions A.x and B.x have 10k pull-up
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch. Note: For proper detection, assert a pulse width of at least 16 ms.	I OD 3.3V	PU 10k 3.3VSB	
SLEEP	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again. Note: For proper detection, assert a pulse width of at least 16 ms.	I OD 3.3V	PU 10k 3.3VSB	

Table 32 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O 3.3V		
SER1_TX	A101	General purpose serial port transmitter	O 3.3V		
SER0_RX	A99	General purpose serial port receiver	I 3.3V	PU 50k 3.3V	
SER1_RX	A102	General purpose serial port receiver	I 3.3V	PU 50k 3.3V	

Table 33 Module Type Definition Signal Description

<table>
<tr><th>Signal</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>TYPE0#
TYPE1#
TYPE2#</td><td>C54
C57
D57</td><td>The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don’t care (X).
<table>
<tr><th>TYPE2#</th><th>TYPE1#</th><th>TYPE0#</th><th></th></tr>
<tr><td>X
NC
NC
NC
NC
GND</td><td>X
NC
NC
GND
GND
NC</td><td>X
NC
GND
NC
GND
NC</td><td>Pinout Type 1
Pinout Type 2
Pinout Type 3 (no IDE)
Pinout Type 4 (no PCI)
Pinout Type 5 (no IDE, no PCI)
Pinout Type 6 (no IDE, no PCI)</td></tr>
<tr><td colspan="4">The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.</td></tr>
</table></td><td>PDS</td><td>TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard.
The conga-TC87 is based on the COM Express Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.</td></tr>
<tr><td>TYPE10#</td><td>A97</td><td>Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed.
<table>
<tr><th>TYPE10#</th><th></th></tr>
<tr><td>NC
PD
12V</td><td>Pinout R2.0
Pinout Type 10 pull down to ground with 4.7k resistor
Pinout R1.0</td></tr>
<tr><td colspan="2">This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7k resistor.</td></tr>
</table></td><td>PDS</td><td>Not connected to indicate “Pinout R2.0”.</td></tr>
</table>

Table 34 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109 C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110 C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

9.2 Boot Strap Signals

Table 35 Boot Strap Signal Descriptions

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
AC/HDA_SDOUT	A33	**High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for High Definition Audio.	O 3.3VSB	PU 1K 3.3VSB	AC/HDA_SDOUT is a boot strap signal (see caution statement below)
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		SPKR is a boot strap signal (see caution statement below)
DDI1_CTRLDATA_AUX-	D16	Multiplexed with DP1_AUX- and HDMI1_CTRLDATA	I/O PCIE or I/O OD 3.3V	PU100k 3.3V	DDI1_CTRLDATA_AUX- is a boot strap signal (see not below).
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA	I/O PCIE or I/O OD 3.3V	PU100k 3.3V	DDI2_CTRLDATA_AUX- is a boot strap signal (see not below).

Caution

1. *The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either COM Express™ internally implemented resistors or chipset internally implemented resistors that are located on the module.*

2. *No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM Express™ module to malfunction and/or cause irreparable damage to the module.*

10 System Resources

10.1 I/O Address Assignment

The I/O address assignment of the conga-TC87 module is functionally identical with a standard PC/AT.

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

10.1.1 LPC Bus

On the conga-TC87, the PCI Express Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the internal PCI Bus not the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus. In the congatec Embedded BIOS, the following I/O address ranges are sent to the LPC Bus:

2Eh – 2Fh

4Eh – 4Fh

60h, 64h

A00h – BFFh

C00h – CFFh (always used internally)

Parts of these ranges are not available if a Super I/O is used on the carrier board. If a Super I/O is not implemented on the carrier board, then these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

10.2 PCI Configuration Space Map

Table 36 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	Host Bridge
00h	02h	00h	Graphics
00h	03h	00h	Intel High Definition Audio controller
00h	14h	00h	XHCI Host Controller
00h(Note1)	16h	00h	Management Engine (ME) Interface 1
00h(Note1)	16h	01h	Intel ME Interface 2
00h(Note1)	16h	02h	ME IDE Redirection (IDE-R) Interface
00h(Note1)	16h	03h	ME KT (Remote Keyboard and Text)
00h	19h	00h	Onboard Gigabit LAN Controller
00h (Note2)	1Ch	00h	PCI Express Root Port 0
00h (Note2)	1Ch	01h	PCI Express Root Port 1
00h (Note2)	1Ch	02h	PCI Express Root Port 2
00h (Note2)	1Ch	03h	PCI Express Root Port 3
00h	1Dh	00h	EHCI Host Controller
00h	1Fh	00h	PCI to LPC Bridge
00h	1Fh	02h	Serial ATA Controller
00h	1Fh	03h	SMBus Host Controller
00h	1Fh	06h	Thermal Subsystem
01h (Note3)	00h	00h	PCI Express Port 0
02h (Note3)	00h	00h	PCI Express Port 1
03h (Note3)	00h	00h	PCI Express Port 2
04h (Note3)	00h	00h	PCI Express Port 3

Note

1. *In the standard configuration, the Intel Management Engine (ME) related devices are partly present or not present at all.*
2. *The PCI Express Ports are visible only if a device is attached behind them to the PCI Express Slot on the carrier board.*
3. *The table represents a case when a single function PCI/PCIe device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

10.3 PCI Interrupt Routing Map

Table 37 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line [1]	APIC Mode IRQ	Graphic	HDA	XHCI	EHCI	SM Bus + Thermal	LAN	SATA	PCI-EX Root Port 0	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	PCI-EX Port 0	PCI-EX Port 1	PCI-EX Port 2	PCI-EX Port 3
A	INTA	16	x	x	x					x				x [2]	x [5]	x [4]	x [3]
B	INTB	17									x			x [3]	x [2]	x [5]	x [4]
C	INTC	18					x					x		x [4]	x [3]	x [2]	x [5]
D	INTD	19							x				x	x [5]	x [4]	x [3]	x [2]
E		20						x									
F		21															
G		22															
H		23				x											

Note

[1] *These interrupt lines are virtual (message based).*

[2] *Interrupt used by single function PCI Express devices (INTA).*

[3] *Interrupt used by multifunction PCI Express devices (INTB).*

[4] *Interrupt used by multifunction PCI Express devices (INTC).*

[5] *Interrupt used by multifunction PCI Express devices (INTD).*

10.4 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

10.5 SM Bus

System Management (SM) bus signals are connected to the Intel® 8 Series PCH-LP and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject, contact congatec technical support.

11 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

11.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

11.1.1 Boot Selection Popup

Press the <F11> key during POST to access the Boot Selection Popup menu. A selection menu displays immediately after POST, allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

11.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar, left frame and right frame. The menu bar is shown below:

Main Advanced Chipset Boot Security Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

11.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the main setup screen. The main setup screen reports BIOS, processor, memory and board information and is for configuring the system date and time. You can always return to the main setup screen by selecting the 'Main' tab.

Feature	Options	Description
Main BIOS Version	No option	Displays the main BIOS version.
OEM BIOS Version	No option	Displays the additional OEM BIOS version.
Build Date	No option	Displays the date the BIOS was built.
Product Revision	No option	Displays the hardware revision of the board.
Serial Number	No option	Displays the serial number of the board.
BC Firmware Revision	No option	Displays the firmware revision of the congatec board controller.
MAC Address	No option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	No option	Displays the number of boot-ups. (max. 16777215).
Running Time	No option	Displays the time the board is running [in hours max. 65535].
▶Platform Information	Submenu	Opens the platform information submenu.
System Date	Day of week, month/ day/year	Specifies the current system date *Note: The date is in month/day/year format.*
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24 hour format.*

11.3.1 Platform Information Submenu

The platform information submenu offers additional hardware and software information.

Feature	Options	Description
Processor Information	No option	Subtitle
Processor Type	No option	Displays the processor ID string. The "Processor Type" text itself is not displayed just the ID string.
Codename	No option	Displays the processor codename
Processor Speed	No option	Displays the processor speed.
Processor Signature	No option	Displays the processor signature.
Stepping	No option	Displays the processor stepping.
Processor Cores	No option	Displays the number of processor cores.
Microcode Revision	No option	Displays the processor microcode revision .
IGD HW Version	No option	Displays the version of the graphics controller.
IGD VBIOS Version	No option	Displays the video BIOS version.
Total Memory	No option	Displays the total amount of installed memory.
PCH Information	No option	subtitle
Codename	No option	Displays the codename of the platform controller hub (PCH).
PCH SKU	No option	Displays the SKU name of the PCH.
Stepping	No option	Displays the PCH stepping.

11.4 Advanced Setup

Select the advanced tab from the setup menu to enter the advanced BIOS setup screen. The menu is used for setting advanced features and only features described within this user's guide are listed.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Graphics				
	Watchdog				
	Module Serial Ports				
	Hardware Health Monitoring				
	PCI & PCI Express				
	ACPI				
	RTC Wake				

Trusted Computing
CPU
SATA
Intel(R) Rapid Start Technology
Acoustic Management
USB
SMART Settings
Super IO
Serial Port Console Redirection
UEFI Network Stack
PC Speaker Configuration
Intel(R) Ethernet Connection I218-LM

11.4.1 Graphics Submenu

Feature	Options	Description
Primary Graphics Device	Auto **IGD** PCI/PCIe	Select primary graphics adapter to be used during boot up. Auto: BIOS will select it automatically. IGD: Internal Graphics Device (IGD) located in chipset. PCI/PCIe: PCI/PCIe graphics card attached to some other (not PEG) PCI/PCIe port.
Internal Graphics Device	**Auto** Disabled Enabled	Enable or disable Internal Graphics Device (IGD).
IGD Pre-Allocated Graphics Memory	32M**, 64M**, 96M, 128M, 160M, 192M, 224M, 256M, 288M, 320M, 352M, 384M, 416M, 448M, 480M, 512M, 1024M	Select amount of pre-allocated (fixed) graphics memory used by the Internal Graphics Device.
IGD Total Graphics Memory	128MB **256MB** MAX	Select amount of total graphics memory that may be used by the Internal Graphics Device. Memory above the fixed graphics memory will be dynamically allocated by the graphics driver according to DVMT 5.0 specification. MAX = Use as much graphics memory as possible. Depends on total system memory installed and the operating system used (see DVMT 5.0 specification).

Feature	Options	Description
Primary IGD Boot Display Device	**Auto** LFP EFP EFP2	Select the Primary IGD display device(s) used for boot up. LFP (Local Flat Panel) selects a LVDS panel connected to the integrated LVDS port. EFPx (External Flat Panel) selects a HDMI/DVI or DisplayPort device connected to the Digital Display Interfaces DDI1, DDI2 and DDI3. Examples for EFPx name assignment to DDI1, DDI2, DDI3: 1. If only DDI2 is enabled then the EFP name is assigned to DDI2. 2. If both port DDI1 and DDI2 are enabled then EFP is assigned to DDI1 and EFP2 is assigned to DDI2. EFP selections are valid only when DDI1, DDI2 and/or DDI3 are enabled.
Secondary IGD Boot Display Device	**Disabled** LFP EFP EFP2	Select the Secondary IGD display device(s) used for boot up. VGA modes will be supported only on Primary display. For other details see Primary IGD Boot Display Device.
Active LFP Configuration	No Local Flat Panel **Integrated LVDS** eDP	Select the active local flat panel configuration.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel. Only if no external EDID data set can be found, the data set selected under 'Local Flat Panel Type' will be used as a fallback data set.
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x18 (01Fh) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x800 1x18 (01Eh) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 2x24 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.*
Backlight Inverter Type	None **PWM** I2C	Select the type of backlight inverter used. PWM = Use IGD PWM signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.

Feature	Options	Description
PWM Inverter Polarity	**Normal** Inverted	Select PWM inverter polarity. Only visible if Backlight Inverter Type is set to PWM .
PWM Inverter Frequency (Hz)	**200** - 40000	Set the PWM inverter frequency in Hz. Only visible if Backlight Inverter Type is set to PWM.
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%**	Actual backlight value in percent of the maximum setting.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Setting	**No** Yes	Allow to invert backlight control values if required for the actual I2C type backlight hardware controller.
LVDS SSC	**Disabled**, 0.5%, 1.0%, 1.5%, 2.0%, 2.5%	Configure LVDS spread spectrum clock modulation depth with center spreading and fixed modulation frequency of 32.9kHz.
Digital Display Interface 1 (DDI1)	**Auto Selection** Disabled Display Port HDMI/DVI	Select the output type of the digital display interface.
Digital Display Interface 2 (DDI2)	**Auto Selection** Disabled Display Port HDMI/DVI	Select the output type of the digital display interface.
▶GOP Configuration	Submenu	Configure graphics output when using the UEFI Graphics Output Protocol (GOP) driver instead of legacy video BIOS. Only visible if GOP driver is configured to be used in the 'Video Option ROM Launch Policy' setup node.

11.4.1.1 GOP Configuration Submenu

Feature	Options	Description
Output Device	(options depend on detected display devices)	Select boot display device in GOP driver mode.
BIST Enable	**Disabled** Enabled	Starts or stops the BIST (built in self test) on the integrated display panel.

11.4.2 Watchdog Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One-time Trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to '*One-time Trigger*' the watchdog will be disabled after the first trigger. If set to *'Single Event'*, every stage will be executed only once, then the watchdog will be disabled. If set to *'Repeated Event'* the last stage will be executed repeatedly until a reset occurs.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event, see note below.
Event 2	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.

Feature	Options	Description
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

In ACPI mode, it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

Additionally, the conga-TC87 module does not support the watchdog NMI mode.

11.4.3 Module Serial Ports Submenu

Feature	Options	Description
Serial Port 0	**Disabled** Enabled	Enable or disable module serial port 0.
I/O Base Address	3F8h, 2F8h, 220h, 228h, 238h, 2E8h, 338h, **3E8h**	Set serial port base address.
Interrupt	None, IRQ3, IRQ4, IRQ5, IRQ6, **IRQ10**, IRQ11, IRQ14, IRQ15	Set serial port interrupt.
PNP ID	None PNP0501 **CGT0501**	Set serial port ACPI ID.
Baudrate	**2400**, 4800, 9600, 19200, 38400, 57600, 115200	Set serial port initial baudrate.
Serial Port 1	**Disabled** Enabled	Enable or disable module serial port 1.
I/O Base Address	3F8h, 2F8h, 220h, 228h, 238h, **2E8h**, 338h, 3E8h	Set serial port base address.
Interrupt	None, IRQ3, IRQ4, IRQ5, IRQ6, IRQ10, **IRQ11**, IRQ14, IRQ15	Set serial port interrupt.
PNP ID	None PNP0501 CGT0501 **CGT0502**	Set serial port ACPI ID.
Baudrate	**2400**, 4800, 9600, 19200, 38400, 57600, 115200	Set serial port initial baudrate.

11.4.4 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	No option	Displays the actual CPU temperature in °C.
Board Temperature	No option	Displays the actual module board temperature in °C
12V Standard	No option	Displays the actual voltage of the 12V standard power supply.
5V Standby	No option	Displays the actual voltage of the 5V standby power supply.
Input Current (12V Standard)	No option	Displays the module's input current from 12V standard voltage.
CPU Fan Speed	No option	Displays the actual CPU fan speed in RPM.
Fan PWM Frequency Mode	Low Frequency **High Frequency**	Select fan PWM base frequency mode. Low Frequency: 11.0Hz - 88.2Hz High Frequency: 1kHz - 63kHz
Fan PWM Frequency	11.0 Hz, 14.7 Hz, 22.1 Hz, 29.4 Hz, **35.3 Hz**, 44.1 Hz, 58.8 Hz, 88.2 Hz	Select fan PWM base frequency (11.0Hz-88.2Hz). (Only visible in low frequency mode)
Fan PWM Frequency (kHz)	1-63 default: **31**	Select fan PWM base frequency (1kHz-63kHz). (Only visible in high frequency mode)
Fan Speed Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%**	Boot up fan speed in percent of the maximum supported speed.

11.4.5 PCI & PCI Express Submenu

Feature	Options	Description
PCI Settings		
PCI Latency Timer	**32**, 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate SERR#.

Feature	Options	Description
Generate EXCD0/1_PERST#	Disabled 1ms 5ms **10ms** 50ms 100ms 150ms 200ms 250ms	Select whether the COM Express EXCD0_PERST# and EXCD1_PERST# pins should be driven low during POST and how long it will be, if enabled.
▶PCI Express Settings	Submenu	PCI Express device and link settings.
▶PCI Express GEN 2 Settings	Submenu	PCI Express Gen2 device and link settings
▶PIRQ Routing & IRQ Reservation	Submenu	Manual PIRQ routing and interrupt reservation for legacy devices.
PCIE Root Port Function Swapping	**Disabled** Enabled	Enable or disable PCI Express root port function swapping.
Subtractive Decode	**Disabled** Enabled	Enable or disable PCI Express subtractive decode.
▶PCI Express Port 0	Submenu	Opens the PCI Express Port submenu
▶PCI Express Port 1	Submenu	Opens the PCI Express Port submenu
▶PCI Express Port 2	Submenu	Opens the PCI Express Port submenu
▶PCI Express Port 3	Submenu	Opens the PCI Express Port submenu

11.4.5.1 PCI Express Settings Submenu

Feature	Options	Description
Relaxed Ordering	**Disabled** Enabled	Enable or disable PCI Express device relaxed ordering.
Extended Tag	**Disabled** Enabled	If enabled a device may use an 8-bit tag filed as a requester.
No Snoop	Disabled **Enabled**	Enable or disable PCI Express device 'No Snoop' option.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum payload of PCI Express devices or allow system BIOS to select the value.

Feature	Options	Description
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum read request size of PCI Express devices or allow system BIOS to select the value.
ASPM	**Disabled** Auto Force L0s	PCI Express Active State Power Management settings.
Extended Synch	**Disabled** Enabled	If enabled, the generation of extended PCI Express synchronization patterns is allowed.
Link Training Retry	Disabled, 2, 3, **5**	Defines number of retry attempts software will take to retrain the link if previous training attempt was unsuccessful.
Link Training Timeout (us)	10-10000 **Default : 100**	Defines number of microseconds software will wait before polling link training bit in the link status register. Value ranges from 10 to 10000 us.
Unpopulated Links	**Keep Link On** Disabled	In order to save power, software will disable unpopulated PCI Express links, if this option is set to disabled.
Restore PCIe Registers	Enabled **Disabled**	On non-PCI Express aware operating systems some devices may not be re-initialized correctly after S3. Setting this node to Enabled restores PCI Express configuration on S3 resume. Warning: Enabling this may cause issues with other hardware after S3 resume.

11.4.5.2 PCI Express GEN 2 Settings Submenu

Feature	Options	Description
Completion Timeout	**Default** Shorter Longer Disabled	Device functions that support completion timeout
ARI Forwarding	**Disabled** Enabled	
AtomicOp Requester Enable	**Disabled** Enabled	
AtomicOp Egress Blocking	**Disabled** Enabled	
IDO Request Enable	**Disabled** Enabled	
IDO Completion Enable	**Disabled** Enabled	

Feature	Options	Description
LTR Mechanism Enable	**Disabled** Enabled	
End-End TLP Prefix Blocking	**Disabled** Enabled	
Target Link Speed	**Auto** Force to 2.5 GT/s Force to 5.0 GT/s	
Clock Power Management	**Disabled** Enabled	
Compliance SOS	**Disabled** Enabled	
Hardware Autonomous Width	Disabled **Enabled**	
Hardware Autonomous Speed	Disabled **Enabled**	

11.4.5.3 PIRQ Routing & IRQ Reservation Submenu

Feature	Options	Description
PIRQA	**Auto**, IRQ3, IRQ4, IRQ5, IRQ6, IRQ10, IRQ11, IRQ14, IRQ15	Set interrupt for selected PIRQ. Please refer to the board's resource list for a detailed list of devices connected to the respective PIRQ. NOTE: These settings will only be effective while operating in PIC (non-IOAPIC) interrupt mode.
PIRQB	same as PIRQA	same as PIRQA
PIRQC	same as PIRQA	same as PIRQA
PIRQD	same as PIRQA	same as PIRQA
PIRQE	same as PIRQA	same as PIRQA
PIRQF	same as PIRQA	same as PIRQA
PIRQG	same as PIRQA	same as PIRQA
PIRQH	same as PIRQA	same as PIRQA
Reserve Legacy Interrupt 1	**None**, IRQ3, IRQ4, IRQ5, IRQ6, IRQ10, IRQ11, IRQ14, IRQ15	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.
Reserve Legacy Interrupt 2	same as Reserve Legacy Interrupt 1	same as Reserve Legacy Interrupt 1

11.4.5.4 PCI Express Port Submenu

Feature	Options	Description
PCI Express Port x	Disabled **Enabled**	Enable or disable the respective PCI Express port x. Note: Unless the Always Enable Port (see below) is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
ASPM	**Disabled** L0s L1 L0sL1 Auto	PCI Express Active State Power Management settings.
L1 Substates	**Disabled** L1.1 L1.2 L1.1 & L1.2	PCI Express L1 substates settings.
URR	**Disabled** Enabled	Enable or disable PCI Express Unsupported Request Reporting.
FER	**Disabled** Enabled	Enable or disable PCI Express device Fatal Error Reporting.
NFER	**Disabled** Enabled	Enable or disable PCI Express device Non-Fatal Error Reporting.
CER	**Disabled** Enabled	Enable or disable PCI Express device Correctable Error Reporting.
CTO	**Disabled** Enabled	Enable or disable PCI Express Completion Timeout timer.
SEFE	**Disabled** Enabled	Enable or disable Root PCI Express System Error on Fatal Error.
SENFE	**Disabled** Enabled	Enable or disable Root PCI Express System Error on Non-Fatal Error.
SECE	**Disabled** Enabled	Enable or disable Root PCI Express System Error on Correctable Error.
PME SCI	Disabled **Enabled**	Enable or disable PCI Express PME (power management event) SCI.
Always Enable Port	**Disabled** Enabled	Disabled = Disable the internal PCI Express interface device if no device is detected on the port. Enabled = Enable the internal PCI Express interface device also if no device is detected on the port.
PCIe Speed	**Auto** Gen1	Maximum speed of the PCIe port. Auto = Gen1 or Gen2 Gen1 = 2.5GT/s Some older non-compliant PCI Express devices will function only if Gen1 is selected. Some Gen2 devices start up in Gen1 mode and then their OS driver sets them to Gen2 mode.

Feature	Options	Description
Detect Non-compliant Device	**Disabled** Enabled	Try to detect also a non-compliant PCI Express device. If enabled, POST time will be longer.
Extra Bus Reserved	0-7 Default : **0**	Extra bus reserved (0-7) for bridges behind this root bridge.
Reserved Memory	1-20 Default : **10**	Reserved memory range for this root bridge.
Prefetchable Memory	1-20 Default : **10**	Prefetchable memory range for this root bridge.
Reserved I/O	4-20 Default : **4**	Reserved I/O range for this root bridge.
PCIe LTR	Disabled **Enabled**	Enable or disable PCI Express Latency Tolerance Reporting (LTR).
PCIe LTR Lock	Disabled **Enabled**	PCIe LTR configuration lock.
Snoop Latency Override	Disabled Manual **Auto**	Snoop latency override for PCH PCIe.
Snoop Latency Multiplier	1 ns, 32 ns, **1024 ns** 32768 ns, 1048576 ns 33554432 ns	Snoop latency multiplier for PCH PCIe.
Snoop Latency Value	0-252 Default : **60**	Snoop latency value for PCH PCIe.
No-Snoop Latency Override	Disabled Manual **Auto**	No-Snoop latency override for PCH PCIe.
No-Snoop Latency Multiplier	1 ns, 32 ns, 1024 **ns** 32768 ns, 1048576 ns 33554432 ns	No-Snoop latency multiplier for PCH PCIe.
No-Snoop Latency Value	0-252 Default : **60**	No-Snoop latency override for PCH PCIe.

11.4.6 ACPI Submenu

Feature	Options	Description
Hibernation Support	Disabled **Enabled**	Enable or disable system ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled S1 only (CPU Stop Clock) **S3 (Suspend to RAM)** Both S1 and S3 available for OS to choose from	Select the state used for ACPI system sleep/suspend.
Lock Legacy Resources	**Disabled** Enabled	Enable or disable locking of legacy resources.
S3 Video Repost	**Disabled** Enabled	Enable or disable video BIOS re-post on S3 resume. Required by some operating systems.
ACPI Low Power S0 Idle	**Disabled** Enabled	Enable or disable ACPI Low Power S0 Idle support.
Native PCI Express Support	Disabled **Enabled**	Enable or disable native OS PCI Express support.
Native ASPM	**Disabled** Enabled	Enabled = The OS will control the ASPM support of the PCI Express device. Disabled = The BIOS will control the ASPM support of the PCI Express device.
ACPI Debug	**Disabled** Enabled	Open a memory buffer for storing debug strings. Use method ADBG to write strings to buffer.
ACPI 5.0 CPPC Support	**Disabled** Enabled	Enable ACPI 5.0 Collaborative Processor Performance Control (CPPC) support. When enabled, platform exposes CPPC interfaces to operating system. When disabled, platform exposes legacy (non-CPPC) processor interfaces to operating system.
ACPI 5.0 CPPC Platform SCI	**Disabled** Enabled	Enable ACPI 5.0 platform generation of SCI on CPPC command completion. When enabled, platform generates GPE/SCI. When disabled platform does not generate GPE/SCI and OS polls for command completion.
Active Trip Point	Disabled, 15 C, 23 C, 31 C, 39 C, 47 C, 55 C, 63 C, **71 C**, 79 C, 87 C, 95 C, 103 C, 111 C, 119 C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Automatic Critical Trip Point	**Disabled** Enabled	Enabled = Configure the critical trip point - the temperature threshold at which the ACPI aware OS performs a critical shutdown - automatically to recommended value. Disabled = Configure the critical trip point manually.
Critical Trip Point Value	71 C, 79 C, 87 C, 95 C, 103 C, **106 C**, 111 C, 119 C, 127 C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Lid Support	**Disabled** Enabled	Configure COM Express LID# Signal to act as ACPI lid.
Sleep Button Support	**Disabled** Enabled	Configure COM Express SLEEP# signal to act as ACPI sleep button.

11.4.7 RTC Wake Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour		Specify wake up hour. For example, enter "3" for 3am and "15" for 3pm.
Wake up minute		Specify wake up minute.
Wake up second		Specify wake up second.

11.4.8 Trusted Computing Submenu

Feature	Options	Description
Security Device Support	**Disabled** Enabled	Enable or disable TPM support. System reset is required after change.
TPM State	**Disabled** Enabled	Enable or disable TPM chip. Note: System might restart several times during POST to acquire target state.
Pending operation	**None,** Enable Take Ownership, Disable Take Ownership, TPM Clear	Perform selected TPM chip operation. Note: System might restart several times during POST to perform selected operation.

11.4.9 CPU Submenu

Feature	Options	Description
Processor Type	No option	Displays the processor ID string. The "Processor Type" is not displayed, just the ID string.
CPU Signature	No option	Displays the CPU Signature.
Microcode Patch	No option	Displays the revision of the Microcode Patch.
FSB Speed	No option	Displays the FSB Speed.
Max CPU Speed	No option	Displays the Max CPU Speed.
Min CPU Speed	No option	Displays the Min CPU Speed.
CPU Speed	No option	Displays the current CPU Speed.
Processor Cores	No option	Displays the number of the Processor Cores.

Feature	Options	Description
Intel HT Technology	No option	Displays whether Intel HT Technology is supported.
Intel VT-x Technology	No option	Displays whether Intel VT-x Technology is supported.
Intel SMX Technology	No option	Displays whether Intel SMX Technology is supported.
64-bit	No option	Displays whether 64-bit is supported.
EIST Technology	No option	Displays whether Enhanced Intel SpeedStep Technology (EIST) is supported.
CPU C3 State	No option	Displays whether CPU C3 State is supported.
CPU C6 State	No option	Displays whether CPU C6 State is supported.
CPU C7 State	No option	Displays whether CPU C7 State is supported.
L1 Data Cache	No option	Displays the size of the L1 Data Cache.
L1 Code Cache	No option	Displays the size of the L1 Code Cache.
L2 Cache	No option	Displays the size of the L2 Cache.
L3 Cache	No option	Displays the size of the L3 Cache.
Set Boot Freq Ratio	8-23 Default : 255	Range: 8 - 23. This sets the boot ratio. If ratio is out of range, maximum ratio is used. Non-ACPI OSes will use this ratio. The range 8-23 is just an example as the possible range depends on processor variant.
Hyper-Threading	Disabled **Enabled**	Enable or Disable Hyper-Threading technology.
Active Processor Cores	All 1 2 3	Set number of cores to be enabled.
Overclocking Lock	**Disabled** Enabled	FLEX_RATIO(194) MSR
Limit CPUID Maximum	**Disabled** Enabled	When enabled, the processor limits the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When disabled, the processor returns the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Execute Disable Bit	Disabled **Enabled**	Enable or disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled, certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting OS.
Intel Virtualization Technology	Disabled **Enabled**	When enabled, a VMM can utilize the integrated hardware virtualization support.
Hardware Prefetcher	Disabled **Enabled**	Enable or disable the Mid Level Cache (L2) streamer prefetcher.
Adjacent Cache Line Prefetch	Disabled **Enabled**	Enable or disable the Mid Level Cache (L2) prefetching of adjacent cache lines.
CPU AES	Disabled **Enabled**	Enable or disable CPU Advanced Encryption Standard (AES) instructions.

Feature	Options	Description
EIST	Disabled **Enabled**	Enable or disable Enhanced Intel SpeedStep Technology (EIST).
Energy Performance	**Performance** Balanced Perform. Balanced Energy Energy Efficient	Optimize between performance and power savings.
Turbo Mode	Disabled **Enabled**	Enable or disable Turbo Mode.
Package Power Limit Lock	Disabled **Enabled**	When enabled, PACKAGE_POWER_LIMIT MSR will be locked and a reset will be required to unlock the register.
CPU Power Limit1	0-255 Default : 0	CPU Power Limit1 value
CPU Power Limit1 Time	0-255 Default : 0	Time window in which the Power Limit1 is maintained.
CPU Power Limit2	0-255 Default : 0	CPU Power Limit2 value
Platform Power Limit Lock	Disabled **Enabled**	When enabled, PLATFORM_POWER_LIMIT MSR will be locked and a reset will be required to unlock the register.
CPU Power Limit3	0-255 Default : 0	CPU Power Limit3 value
CPU Power Limit3 Time	0-255 Default : 0	Time window in which the Power Limit3 is maintained.
CPU Power Limit3 Duty Cycle	0-100 Default : 0	Specify in percentage the duty cycle that the CPU is required to maintain over the configured Power Limit3 time windows.
DDR Power Limit1	0-255 Default : 0	DDR Power Limit1 value
DDR Power Limit1 Time	0-255 Default : 0	Time window in which the DDR Power Limit1 is maintained.
DDR Power Limit2	0-255 Default : 0	DDR Power Limit2 value
1-Core Ratio Limit	0-255 Default : 0	Limit for 1 active core. 0 means using the factory-configured value.
2-Core Ratio Limit	0-255 Default : 0	Limit for 2 active cores. 0 means using the factory-configured value.
3-Core Ratio Limit	0-255 Default : 0	Limit for 3 active cores. 0 means using the factory-configured value.
4-Core Ratio Limit	0-255 Default : 0	Limit for 4 active cores. 0 means using the factory-configured value.

Feature	Options	Description
VR Current Value Lock	Disabled **Enabled**	Locks VR current value from further writes until a reset.
VR Current Value	0-8191 Default : 0	Voltage regulator current limit. 0 means automatic.
CPU C States	**Disabled** Enabled	Enable or disable CPU C states.
Enhanced C1 State	**Disabled** Enabled	Enhanced C1 state
CPU C3 Report	Disabled **Enabled**	Enable or disable CPU C3 report to OS.
CPU C6 Report	Disabled **Enabled**	Enable or disable CPU C6 report to OS.
C6 Latency	**Short** Long	Configure Short/Long latency for C6.
CPU C7 Report	Disabled CPU C7 **CPU C7s**	Enable or disable CPU C7 report to OS.
C7 Latency	Short **Long**	Configure Short/Long latency for C7.
CPU C8 Report	Disabled **Enabled**	Enable or disable CPU C8 report to OS. Note: Not displayed/supported on all Processors types.
CPU C9 Report	Disabled **Enabled**	Enable or disable CPU C9 report to OS. Note: Not displayed/supported on all Processors types.
CPU C10 Report	Disabled **Enabled**	Enable or disable CPU C10 report to OS. Note: Not displayed/supported on all Processors types.
C1 State Auto Demotion	Disabled **Enabled**	Processor will conditionally demote C3/C6/C7 requests to C1 based on uncore auto-demote information.
C3 State Auto Demotion	Disabled **Enabled**	Processor will conditionally demote C6/C7 requests to C3 based on uncore auto-demote information.
Package C State Demotion	Disabled **Enabled**	Enable or disable package C state demotion.
C1 State Auto Undemotion	Disabled **Enabled**	Enable or disable Un-demotion from demoted C1.
C3 State Auto Undemotion	Disabled **Enabled**	Enable or disable Un-demotion from demoted C3.
Package C State Undemotion	Disabled **Enabled**	Enable or disable package C state undemotion.
C State Pre-Wake	Disabled **Enabled**	Enable or disable C state Pre-Wake feature.

Feature	Options	Description
CFG Lock	Disabled **Enabled**	Configure MSR 0xE2[15], CFG lock bit.
Package C State Limit	C0/C1, C2, C3, C6, C7, C7s, C8, C9, C10, **AUTO**	Set Package C state limit
Lake Tiny Feature	**Disabled** Enabled	Enable or disable Lake Tiny feature for C state configuration.
ACPI CTDP BIOS	**Disabled** Enabled	Enable or disable ACPI CTDP BIOS support.
Configurable TDP Level	**TDP NOMINAL** TDP DOWN TDP UP Disabled	Allow reconfiguration of TDP levels base on current power and thermal delivery capabilities of the system.
Config TDP Lock	**Disabled** Enabled	Lock the config TDP control register.
TCC Activation Offset	0-50 Default : **0**	Offset from the Intel factory Thermal Control Circuit (TCC) activation temperature. TCC activation will lower CPU core and graphics core frequency, voltage or both. The factory TCC activation temperature is normally 100C. By entering 10 for TCC offset, the TCC will be activated at 90C.
Intel TXT(LT) Support	**Disabled** Enabled	Enable or disable Intel(R) TXT(LT) support.
Debug Interface	**Disabled** Enabled	Enable or disable CPU debug feature.
Debug Interface Lock	**Disabled** Enabled	Lock CPU debug feature setting.
IOUT Offset Sign	0-1 Default : **0**	0 means positive offset. 1 means negative offset.
IOUT Offset	0-625 Default : **0**	VR IOUT offset configuration The range is 0 - 625.
IOUT Slope	0-1023 Default : **512**	VR IOUT slope configuration The range is 0 - 1023.

11.4.10 SATA Submenu

Feature	Options	Description
SATA Controller(s)	**Enabled** Disabled	Enable or disable the onboard SATA controller(s).
SATA Mode Selection	**AHCI** RAID	Select SATA controller mode. RAID option is not supported on all chipsets.
SATA Test Mode	Enabled **Disabled**	Should be set to Disabled. Test Mode is used just for verification measurements.
Aggressive LPM Support	**Enabled** Disabled	Enable PCH to aggressively enter link power state.
SATA Controller Speed	**Default** Gen1 Gen2 Gen3	Indicates the maximum speed the SATA controller can support. Default = maximum speed supported by the chipset Gen1 = 1.5 Gbit/s Gen2 = 3 Gbit/s Gen3 = 6 Gbit/s On conga-TC87, the supported maximum speed is 6 Gbit/s.
► Software Feature Mask Configuration	Submenu	RAID option ROM and Intel Rapid Storage Technology driver will refer to the Software Feature Mask Configuration to enable or disable the storage features.
Alternate ID	Enabled **Disabled**	Report alternate Device ID. Displayed just for RAID SATA Mode.
Serial ATA Port 0, 1, 2, 3	No option	Displays the name of the connected Hard Disk or DVDROM when the port is enabled. Empty is displayed when the port is disabled or when the port is enabled but nothing is connected to it. On conga-TC87 variants equipped with mainstream chipset, the SATA ports 2 and 3 are not available.
Software Preserve	No option	Displays whether the detected drive supports Software Settings Preservation.
SATA Port	Disabled **Enabled**	Enable or disable the relevant SATA port.
Hot Plug	**Disabled** Enabled	Select hot plug support for relevant SATA port.
External SATA	**Disabled** Enabled	Enable or disable external SATA support on relevant SATA port.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify if the relevant SATA port is connected to solid state drive or hard disk drive.
Spin Up Device	**Disabled** Enabled	When enabled, the controller runs an initialization sequence for the connected device during startup at the relevant SATA port. Some hard disks and special Solid-state Drives (SSD) will function correctly only when this feature is enabled.

11.4.10.1 Software Feature Mask Configuration Submenu

Feature	Options	Description
RAID0	Disabled **Enabled**	Enable or disable RAID0 feature.
RAID1	Disabled **Enabled**	Enable or disable RAID1 feature.
RAID10	Disabled **Enabled**	Enable or disable RAID10 feature.
RAID5	Disabled **Enabled**	Enable or disable RAID5 feature.
Intel Rapid Recovery Technology	Disabled **Enabled**	Enable or disable Intel Rapid Recovery Technology.
Option ROM UI and Banner	Disabled **Enabled**	If enabled, then the option ROM user interface is shown. Otherwise, no option ROM banner or information will be displayed if all disks and RAID volumes are normal.
HDD Unlock	Disabled **Enabled**	If enabled, indicates that the HDD password unlock in the OS is enabled.
LED Locate	Disabled **Enabled**	LED locate
IRRT Only on eSATA	Disabled **Enabled**	If enabled, then only Intel Rapid Recovery Technology (IRRT) volumes can span internal and external SATA (eSATA) drives. If disabled, then any RAID volume can span internal and eSATA drives.
Intel Smart Response Technology	Disabled **Enabled**	Enable or disable Intel Smart Response Technology.
Option ROM UI Delay	**2 Seconds** 4 Seconds 6 Seconds 8 Seconds	If enabled, indicates the delay of the option ROM user interface splash screen in a normal status.

11.4.11 Intel(R) Rapid Start Technology Submenu

Feature	Options	Description
Intel(R) Rapid Start Technology	**Disabled** Enabled	Enable or disable Intel(R) Rapid Start Technology.
No valid partition	No option	Warning message when the Intel(R) Rapid Start Technology is not completely set up.
Entry on S3 RTC Wake	Disabled **Enabled**	Rapid Start invocation upon S3 RTC wake.
Entry After	0-120 Default : **10**	Enable RTC wake timer at S3 entry. Value range is from 0 (immediately) to 120 minutes.

Feature	Options	Description
Active Page Threshold Support	**Disabled** Enabled	Support RST with small partition.
Active Memory Threshold	0-65535 Default : **0**	Try to support RST when partition size > Active Page Threshold size in MB. Value 0 means automatic mode.
Hybrid Hard Disk Support	**Disabled** Enabled	Hybrid Hard Disk Support
Rapid Start Display Save/ Restore	**Disabled** Enabled	Rapid Start Display Save/Restore
Rapid Start Display Type	**BIOS Save/Restore** Desktop Save/Restore	Rapid Start Display Type

11.4.12 Acoustic Management Submenu

Feature	Options	Description
Automatic Acoustic Management	Enabled **Disabled**	Enable or disable Automatic Acoustic Management (AAM) on optical or hard disk drives.
SATA Port 0 Disk drive name Acoustic Mode	**Bypass** Quiet Max Performance	Acoustic noise level and performance optimization of optical or hard disk drives Bypass: Use drive's preset value. Quiet: Drive is slower, but quieter. Max Performance: Drive is faster, but possibly noisier.
SATA Port 1 Disk drive name Acoustic Mode	**Bypass** Quiet Max Performance	Same as at SATA Port 0.
SATA Port 2 Disk drive name Acoustic Mode	**Bypass** Quiet Max Performance	Same as at SATA Port 0.
SATA Port 3 Disk drive name Acoustic Mode	**Bypass** Quiet Max Performance	Same as at SATA Port 0.

Note

This menu displays only the SATA ports on which the optical or hard disk drive is detected.

11.4.13 USB Submenu

Feature	Options	Description
USB Devices	No option	Displays the detected USB devices.
xHCI Mode	Smart Auto **Auto** Enabled Disabled Manual	Smart Auto – The BIOS will store the USB mode set by the OS and at next boot the BIOS will set this previously used mode. At G3 boot (first boot after mechanical disconnection of the power supply) the USB ports will function identically as in Auto mode. Auto – All USB ports are initially set to operate in USB2.0 Mode and the USB3.0 OS driver (if available) will switch the USB3.0 capable ports to USB3.0 mode. If USB3.0 OS driver is not available then the ports will function correctly but will operate in USB2.0 mode. Enabled – USB2.0 and USB3.0 ports will function correctly in BIOS but will not function at all under OS if the USB3.0 OS driver is not installed. Disabled – All USB ports will function in USB2.0 mode only. No USB3.0 OS driver required. Manual – Using the settings under USB2.0 Pins Routing and USB3.0 Pins, the characteristics of the USB ports can be set individually.
EHCI (Ports USB0-7)	Disabled **Enabled**	Enable or disable EHCI (USB 2.0) controller. One EHCI controller must always be enabled.
USB2.0 Pins Routing	Route Per-Pin **Route all Pins to EHCI** Route all Pins to xHCI	Route USB2.0 pins to EHCI or xHCI controller.
USB2.0 Port 0 Pins	**Route to EHCI** Route to xHCI	Route the respective USB2.0 port to EHCI or xHCI controller.
USB2.0 Port 1 Pins	**Route to EHCI** Route to xHCI	Route the respective USB2.0 port to EHCI or xHCI controller.
USB2.0 Port 2 Pins	**Route to EHCI** Route to xHCI	Route the respective USB2.0 port to EHCI or xHCI controller.
USB2.0 Port 3 Pins	**Route to EHCI** Route to xHCI	Route the respective USB2.0 port to EHCI or xHCI controller.
USB2.0 Port 4 Pins	**Route to EHCI** Route to xHCI	Route the respective USB2.0 port to EHCI or xHCI controller.
USB2.0 Port 5 Pins	**Route to EHCI** Route to xHCI	Route the respective USB2.0 port to EHCI or xHCI controller.
USB2.0 Port 6 Pins	**Route to EHCI** Route to xHCI	Route the respective USB2.0 port to EHCI or xHCI controller.
USB2.0 Port 7 Pins	**Route to EHCI** Route to xHCI	Route the respective USB2.0 port to EHCI or xHCI controller.

Feature	Options	Description
USB3.0 Pins	Select Per-Pin **Disable all Pins** Enable all Pins	Enable or disable xHCI SuperSpeed support.
USB3.0 Port 0 Pins	**Disabled** Enabled	Enable or disable the xHCI SuperSpeed support on respective USB port.
USB3.0 Port 1 Pins	**Disabled** Enabled	Enable or disable the xHCI SuperSpeed support on respective USB port.
Overcurrent Protection	**Disabled** Enabled	Enable or disable overcurrent protection chipset handling (e.g send operating system overcurrent condition inofmration) on all USB ports
► USB Ports Per-Port Disable Control	Submenu	Individual disabling of USB ports
Legacy USB Support	**Enabled** Disabled Auto	Enable USB legacy support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and BIOS setup.
xHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without xHCI hand-off support. The xHCI ownership change should be claimed by xHCI OS driver.
EHCI Hand-off	**Disabled** Enabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI OS driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable or disable USB mass storage driver support.
USB Transfer Timeout	1 sec 5 sec 10 sec **20 sec**	The timeout value for control, bulk, and interrupt transfers.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command timeout.
Device Power -Up Delay Selection	**Auto** Manual	Define the maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power -Up Delay Value	1-40 Default : **5**	Actual power-up delay value in seconds.

Feature	Options	Description
USB Mass Storage Device Name (Auto detected USB mass storage devices are listed here dynamically)	**Auto** Floppy Forced FDD Hard Disk CD-ROM	Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. *Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.* Select AUTO to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. Forced FDD allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. Hard disk allows the device to be emulated as hard disk. CDROM assumes the CD-ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

11.4.13.1 USB Ports Per-Port Disable Control Submenu

Feature	Options	Description
USB Ports Per-Port Disable Control	**Disabled** Enabled	Individual disabling of USB ports.
USB Port 0	Disabled **Enabled**	Enable or disable the respective USB2.0 port.
USB Port 1	Disabled **Enabled**	Enable or disable the respective USB2.0 port.
USB Port 2	Disabled **Enabled**	Enable or disable the respective USB2.0 port.
USB Port 3	Disabled **Enabled**	Enable or disable the respective USB2.0 port.
USB Port 4	Disabled **Enabled**	Enable or disable the respective USB2.0 port.
USB Port 5	Disabled **Enabled**	Enable or disable the respective USB2.0 port.
USB Port 6	Disabled **Enabled**	Enable or disable the respective USB2.0 port.
USB Port 7	Disabled **Enabled**	Enable or disable the respective USB2.0 port.
USB3.0 Port 0	Disabled **Enabled**	Enable or disable the respective USB3.0 port.
USB3.0 Port 1	Disabled **Enabled**	Enable or disable the respective USB3.0 port.

11.4.14 SMART Settings Submenu

Feature	Options	Description
SMART Self Test	**Disabled** Enabled	Run SMART self test on all hard disk drives during POST. Self-Monitoring, Analysis and Reporting Technology (SMART) predicts hard disk drives degradation and/or faults.

11.4.15 Super I/O Submenu

Feature	Options	Description
SIO Clock	**24MHz** 48MHz	Select Super I/O base clock
PS/2 Keyboard/Mouse Support	**Disabled** Enabled	Enable or disable PS/2 keyboard/mouse controller support.
Serial Port 0	Disabled **Enabled**	Enable or disable serial port 0.
Device Settings	*IO=3F8h; IRQ=4;*	*Fixed configuration of serial port 0 if enabled.*
Serial Port 1	Disabled **Enabled**	Enable or disable serial port 1.
Device Settings	*IO=2F8h; IRQ=3;*	*Fixed configuration of serial port 1 if enabled.*
Parallel Port	**Disabled** Enabled	Enable or disable parallel port.
Device Settings	*IO=378h; IRQ=7;*	*Fixed configuration of the parallel port if enabled.*
Device Mode	**Standard Parallel Mode** EPP Mode ECP Mode EPP Mode & ECP Mode	Set the parallel port mode.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

11.4.16 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
▶Console Redirection Settings	Submenu	Opens console redirection configuration sub menu.

Feature	Options	Description
COM1 Console Redirection	**Disabled** Enabled	Enable or disable serial port 1 console redirection.
►Console Redirection Settings	Submenu	Opens console redirection configuration sub menu.

Note

The Serial Port Console Redirection can be enabled (functional) only if an external Super I/O offering UARTs has been implemented on the carrier board

11.4.16.1 Console Redirection Settings Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.
Baudrate	9600, 19200, 38400, 57600, **115200**	Select baud rate.
Data Bits	7, **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.

Feature	Options	Description
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Enabled** Disabled	Select whether serial redirection should be continued after POST.

11.4.17 UEFI Network Stack Submenu

Feature	Options	Description
UEFI Network Stack	**Disabled** Enabled	Enable or disable the UEFI network stack.
IPv4 PXE Support	Disabled **Enabled**	Enable IPv4 PXE boot support. If disabled IPv4 PXE boot option will not be created.
IPv6 PXE Support	Disabled **Enabled**	Enable IPv6 PXE boot support. If disabled IPv6 PXE boot option will not be created.

11.4.18 PC Speaker Configuration Submenu

Feature	Options	Description
Debug Beeps	Disabled **Enabled**	Enable or disable general debug / status beep generatioin.
Input Device Debug Beeps	**Disabled** Enabled	Enable or disable input device debug beeps.
Output Device Debug Beeps	**Disabled** Enabled	Enable or disable output device debug beeps.
USB Driver Beeps	**Disabled** Enabled	Enable or disable USB driver beeps.

11.4.19 Intel (R) Ethernet Connection I218-LM Submenu

Feature	Options	Description
► NIC Configuration	Submenu	Opens the NIC Configuration submen.
Blink LEDs	0-15 Default : **0**	The Ethernet LEDs will blink so many seconds long as entered.
UEFI Driver	No option	Displays the UEFI Driver version.
Adapter PBA	No option	Displays the Adapter PBA.
Chip Type	No option	Displays the type of the Chip in which the Ethernet controller is integrated.
PCI Device ID	No option	Displays the PCI Device ID of the Ethernet controller.
Bus:Device:Function	No option	Displays the PCI Bus:Device:Function number of the Ethernet controller.
Link Status	No option	Displays the Link Status.
MAC Address	No option	Displays the MAC Address.

Note

The MAC address is also displayed in the submenu title.

11.4.20 NIC Configuration Submenu

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake On LAN	Disabled **Enabled**	Enables the server to be powered on using an in-band magic packet.

11.5 Chipset Setup

Select the Chipset tab from the setup menu to enter the Chipset BIOS Setup screen. The menu is used for setting chipset features.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Platform Controller Hub (PCH)				
	Processor (Integrated Components)				

11.5.1 Platform Controller Hub (PCH) Submenu

Feature	Options	Description
Intel PCH SKU Name	No option	Displays the SKU Name of the PCH.
PCI Express Clock Gating	**Disabled** Enabled	Enable or disable PCI Express clock gating for each root port.
DMI Link ASPM PCH Side	**Disabled** Enabled	Active State Power Management (ASPM) of DMI link PCH side. DMI link is the main bus between the Processor and Platform Controller Hub (PCH).
DMI Link Extended Synch Control	**Disabled** Enabled	The control of extended synch on PCH side of the DMI link.
Isolate SMBus Segments	Never During POST **Always**	Allows to cut off the off-board SMBus segment. This can be a workaround for external SMBus devices that do not conform to specification.
PCIe-USB Glitch W/A	**Disabled** Enabled	PCIe-USB glitch W/A for bad USB device(s) connected behind PCIe/PEG port.
USB Precondition	**Disabled** Enabled	Precondition work on USB host controller and root ports for faster enumeration.
xHCI Idle L1	**Enabled** Disabled	Enable or disable xHCI Idle L1. The xHCI Idle L1 should be set to 'Disabled' for PCH Ax stepping (early prototype) to work around USB3.0 hot plug failure after one hot plug removal.
BTCG	**Enabled** Disabled	Enable or disable USB related trunk clock gating.
HDA Controller	Disabled Enabled **Auto**	Control activation of the HDA controller device. Disabled = HDA Controller will be unconditionally disabled. Enabled = HDA Controller will be unconditionally enabled. Auto = HDA Controller will be enabled if HDA codec present, disabled otherwise.
Onboard HDA Codec Configuration	**Auto** High Definition Front Panel Legacy Front Panel Disable	Select different output configuration verb tables for the onboard HDA codec.

Feature	Options	Description
HDA PME	**Disabled** Enabled	Enable or disable the power management capability of the audio controller.
PCH LAN Controller	**Enabled** Disabled	Enable or disable the onboard, PCH integrated ethernet controller.
Wake on LAN	**Enabled** Disabled	Enable or disable the wake on LAN capability of the onboard, PCH integrated ethernet controller.
SLP_LAN# Low on DC Power	Disabled **Enabled**	Enable or disable SLP_LAN# low on DC power.
Board Capability	**SUS_PWR_DN_ACK** DeepSx	SUS_PWR_DN_ACK = Send disabled to PCH. DeepSx = Show DeepSx policies.
DeepSx Power Policies	**Disabled** Enabled in S5/Battery Enabled in S4-S5/Battery Enabled in S3-S4-S5/Battery	Configure the DeepSx mode configuration. Activate DeepSx transition generally or in DC/battery powered mode only for selected Sx state.
GP27 Wake From DeepSx	Disabled **Enabled**	Wake from DeepSx by the assertion of GP27 pin.
PCIe Wake From DeepSx	**Disabled** Enabled	Wake from DeepSx by the assertion of PCIe.
Serial IRQ Mode	Quiet **Continuous**	Configure serial IRQ mode.
SB CRID	**Disabled** Enabled	Enable or disable southbridge compatible revision ID support.
PCH Cross Throttling	**Disabled** Enabled	Enable or disable the PCH cross throttling feature.
SLP_S4 Assertion Width	Disabled 1-2 Seconds 2-3 Seconds 3-4 Seconds **4-5 Seconds**	Select a minimum assertion width of the SLP_S4# signal.
Port 80h Redirection	**LPC Bus** PCIe Bus	Control where the port 80h cycles are sent.

11.5.2 Processor (Integrated Components) Submenu

Feature	Options	Description
Processor Codename	No option	Displays the Processor codename.
VT-d Capability	No option	Displays whether the VT-d is supported by the Processor.
VT-d	Disabled **Enabled**	Enable or disable VT-d support. Displayed only if the VT-d capability is supported by the Processor.
Thermal Device (B0:D4:F0)	Enabled **Disabled**	Enable or disable thermal device.
Audio Device (B0:D3:F0)	**Enabled** Disabled	Enable or disable the integrated audio device in the Processor.
NB CRID	**Disabled** Enabled	Enable or disable northbridge compatible revision ID support.
BDAT ACPI Table Support	Enabled **Disabled**	Enable support for the BDAT ACPI table.
▶DMI Configuration	Submenu	Control various DMI functions. DMI link is the main, but exclusively internal bus between the Processor and Platform Controller Hub (PCH).
▶Memory Configuration	Submenu	Memory configuration parameters
▶GT - Power Management Control	Submenu	Processor Graphics Controller (GT) power management control options

11.5.2.1 DMI Configuration Submenu

Feature	Options	Description
DMI	No option	Displays the DMI bus characteristics.
DMI Vc1 Control	Enabled **Disabled**	Enable or disable DMI Vc1.
DMI Vcp Control	**Enabled** Disabled	Enable or disable DMI Vcp.
DMI Vcm Control	**Enabled** Disabled	Enable or disable DMI Vcm.
DMI Link ASPM Processor Side	**Disabled** L0s L1 L0sL1	Active State Power Management (ASPM) of the DMI link on the Processor side. DMI link is the main bus between the Processor and Platform Controller Hub (PCH).
DMI Extended Synch Control	Enabled **Disabled**	Enable or disable DMI extended synchronization.

Feature	Options	Description
DMI Gen 2	**Auto** Enabled Disabled	Enable or disable DMI Gen2.
DMI De-emphasis Control	**-6 dB** -3.5 dB	Configure the de-emphasis control on DMI.
DMI IOT	Enabled **Disabled**	Enable or disable DMI IOT.

11.5.2.2 Memory Configuration Submenu

Feature	Options	Description
Memory Frequency	No option	Displays the memory frequency.
Total Memory	No option	Displays the total amount of installed memory.
Memory Voltage	No option	Displays the memory voltage.
DIMM#0 (Bottom)	No option	Displays bottom memory socket DIMM information.
DIMM#2 (Top)	No option	Displays top memory socket DIMM information.
CAS Latency (tCL)	No option	Displays the CAS Latency (tCL).
CAS to RAS (tRCDmin)	No option	Displays the CAS to RAS (tRCDmin).
Row Precharge (tRPmin)	No option	Displays the Row Precharge (tRPmin).
Active to Precharge (tRASmin)	No option	Displays the Active to Precharge (tRASmin).
DIMM Profile	**Default DIMM Profile** Custom Profile XMP Profile 1 XMP Profile 2	Select the DIMM timing profile that should be used. XMP profiles cannot work on current modules and MUST not be selected. **CAUTION:** For congatec internal debugging only. DO NOT CHANGE.
▶Custom Profile Control	Submenu	Configure the custom DIMM profile options. **CAUTION:** For congatec internal debugging only. DO NOT CHANGE.
Memory Frequency Limiter	**Auto,** 1067,1333, 1600, 1867, 2133, 2400, 2667	Maximum memory frequency selections in [MHz] (Hidden if DIMM profile is set to 'Custom Profile').
DDR Reset Wait Time	0-3000000 **Default : 0**	The amount of time (in nano seconds) to wait for switch DDR voltage.
Max TOLUD	**Dynamic,** 1 GB, 1.25 GB, 1.5 GB, 1.75 GB, 2 GB, 2.25 GB, 2.5 GB, 2.75 GB, 3 GB, 3.25 GB	Maximum value of TOLUD Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

Feature	Options	Description
Enh Interleave Support	Disabled Enabled	Enable or disable Enhanced Interleave support.
RI Support	Disabled Enabled	Enable or disable Rank Interleave support. Note: RI and HORI can not be enabled at the same time.
DLL Weak Lock Support	Disabled Enabled	Enable or disable DLL weak lock support.
Mc Lock	Disabled Enabled	Enable or disable capacity to lock or not MC registers.
Ch Hash Support	Disabled Enabled	Enable or disable channel hash support. Note: Only if memory interleaved mode.
Ch Hash Mask	1-0x3FFF Default : 0x30CE	Set the bit(s) to be included in the XOR function. Note: Bit mask corresponds to bits[19:6].
Ch Hash Interleaved Bit	BIT06, BIT07, BIT08, BIT09	Select the bit to be used for channel interleaved mode. Note: BIT07 will interleave the channels at a 2 cacheline granularity, BIT08 at 4 and BIT09 at 8.
NMode Support	Auto 1N Mode 2N Mode	NMode support option
Memory Scrambler	Enabled Disabled	Enable or disable memory scrambler support.
RMT Crosser Support	Enabled Disabled	Enable or disable RMT crosser support.
MRC Fast Boot	Enabled Disabled	Enable or disable MRC fast boot.
DIMM Exit Mode	Auto Slow Exit Fast Exit	DIMM Exit Mode control
Power Down Mode	No Power Down APD PPD PPD-DLLoff APD-PPD Auto	Power Down Mode control Default is: Auto - when DIMM Exit Mode is set to Slow Exit and PPD - when DIMM Exit Mode is set to Fast Exit.
Memory Remap	Enabled Disabled	Enable or disable memory remap above 4G.
GDXC Support	Enabled Disabled	Enable or disable GDXC support.

11.5.2.3 GT - Power Management Control Submenu

Feature	Options	Description
Processor Graphics Controller Info	No option	Displays the Processor Graphics Controller Info.
RC6 (Render Standby)	Disabled Enabled	Check to enable render standby support.
GT Overclocking Support	Disabled Enabled	Enable or disable GT overclocking support.
GT Overclocking Frequency	0-255 Default : 22	Overclocked RP0 frequency (MLCClk) in multiples of 50 MHz.
GT Overclocking Voltage	0-255 Default : 0	Extra voltage needed above the original RP0 voltage. The unit is 1/256 volt.

11.6 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

11.6.1 Boot Settings Configuration

Feature	Options	Description
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. Note: The default OEM logo is a dark screen.
Setup Prompt Timeout	**1** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot (not recommended), 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. Note: Only works with an ATX type power supply.
AT Shutdown Mode	System Reboot **Hot S5**	Determines the behavior of an AT-powered system after a shutdown.

Feature	Options	Description
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	UEFI Standard **Type Based**	Set boot priority selection method.Select between device and type based boot priority lists. UEFI Standard: Determines boot priority by specific device selection. Devices must be present. Priority changes if devices are removed or added. Type Based: Determines boot priority by device type.
Boot Option Sorting Method	UEFI First Legacy First UEFI Before Legacy **Legacy Before UEFI**	Set boot option sorting method. UEFI First: Tries all UEFI boot options before first legacy boot option. Legacy First: Vice versa. UEFI Before Legacy: Tries UEFI boot option before legacy boot option for a selected device. Afterwards checks next device. Legacy Before UEFI: Vice versa.
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if 'UEFI Standard' priority list control is selected. If "Type Based" priority list control is enabled only 8 boot devices can be prioritized.)	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk USB CDROM Other USB Device Onboard SD Card Storage Onboard LAN External LAN Firmware-based UEFI Bootloader Other Device	This view is only available when in the default "Type Based" mode. When in "UEFI Standard" mode you will only see the devices that are currently connected to the system.
►CSM & Option ROM Control	Submenu	Opens submenu which controls the execution of UEFI and legacy option ROMs.
UEFI Fast Boot	**Disabled** Enabled	Enable or disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS / legacy boot options.
SATA Support	Last Boot HDD Only, All SATA Devices **HDD Only**	
VGA Support	Auto **UEFI Driver**	If set to Auto, the legacy video option ROM will be installed for legacy OS boot; boot logo will NOT be shown during POST. For UEFI OS boot the UEFI GOP driver will be installed.
USB Support	Disabled Full Init **Partial Init**	If set to Disabled, no USB device will be available before OS boot. If set to Partial Init, specific USB ports/ devices will NOT be available before OS boot. If set to Enabled, all USB devices will be available during POST and after OS boot.
PS/2 Device Support	Disabled **Enabled**	If set to Disabled, PS/2 devices will be skipped.
Network Stack Driver Support	**Disabled** Enabled	If set to Disabled, the UEFI network stack driver installation will be skipped.

Note

1. The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.

2. Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.

11.6.1.1 CSM & Option ROM Control Submenu

Feature	Options	Description
Launch CSM	Enabled Disabled	Controls the execution of the CSM module. Only disable for pure UEFI operating system support.
Boot Option Filter	UEFI and Legacy Legacy Only UEFI Only	Controls which devices / boot loaders the system should boot to.
PXE Option ROM Launch Policy	Do Not Launch UEFI ROM Only Legacy ROM Only Legacy ROM First UEFI ROM First	Controls the execution of UEFI and legacy PXE option ROMs.
Storage Option ROM Launch Policy	Do Not Launch UEFI ROM Only Legacy ROM Only Legacy ROM First UEFI ROM First	Controls the execution of UEFI and legacy mass storage device option ROMs.
Video Option ROM Launch Policy	Do Not Launch UEFI ROM Only Legacy ROM Only Legacy ROM First UEFI ROM First	Controls the execution of UEFI and legacy video option ROMs.
Other Option ROM Launch Policy	UEFI ROM Only Legacy ROM Only	Controls the execution of option ROMs for PCI / PCI Express devices other than network, mass storage or video.
GateA20 Active	Upon Request Always	Gate A20 control. Upon Request: Gate A20 can be disabled using BIOS services. Always: Do not allow disabling Gate A20 This option is useful when any runtime code is executed above 1MB.

Feature	Options	Description
Option ROM Messages	Force BIOS Keep Current	Set display mode for option ROMs.

11.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

11.7.1 Security Settings

Feature	Options	Description
BIOS Password	enter password	Specifies the BIOS and setup administrator password
BIOS Lock	Disabled **Enabled**	Enable or disable BIOS Lock Enable (BLE) and SMM BIOS Write Protect (SMM_BWP) bits. Once enabled, BIOS flash write accesses are only possible via dedicated BIOS SMM interfaces.
BIOS Update & Write Protection	**Disabled** Enabled	Enable or disable BIOS write protection. When enabled, the congatec flash software will require BIOS password for write and erase operations.

HDD Security Configuration	
List of all detected hard disks supporting the security feature set	Select device to open device security configuration submenu
►Secure Boot Menu	Submenu

11.7.1.1 BIOS Security Features

BIOS Password/ BIOS Write Protection

A BIOS password protects the BIOS setup program from unauthorized access. This ensures that end users cannot change the system configuration without authorization. With an assigned BIOS password, the BIOS prompts the user for a password on a setup entry. If the password entered is wrong, the BIOS setup program will not launch.

The congatec BIOS uses a SHA256 based encryption for the password, which is more secured than the original AMI encryption. The BIOS password is case sensitive with a minimum of 3 characters and a maximum of 20 characters. Once a BIOS password has been assigned, the BIOS activates the grayed out 'BIOS Update and Write Protection' option. If this option is set to 'enabled', only authorized users (users with the correct password) can update the BIOS.

To update the BIOS, use the congatec system utility cgutlcmd.exe with the following syntax:

```
CGUTLCMD BFLASH <BIOS file> /BP: <password> where <password> is the assigned BIOS password.
```

For more information about "Updating the BIOS" refer to the congatec system utility user's guide, which is called CGUTLm1x.pdf and can be found on the congatec GmbH website at www.congatec.com.

With the BIOS password protection and the BIOS update and write protection, the system configuration is completely secured. If the BIOS is password protected, you cannot change the configuration of an end application without the correct password.

Note

Use cgutlcmd.exe version 1.5.3 or later.

Built in BIOS recovery is disabled in the congatec BIOS firmware to prevent the BIOS from updating itself due to the user pressing a special key combination or a corrupt BIOS being detected. congatec considers such a recovery update a security risk because the BIOS internal update process bypasses the implemented BIOS security explained above.

Only the congatec utility interface to the SMI handler of the BIOS flash update is enabled. Other interfaces to the SMI handler are disabled to prevent non congatec tools from writing to the BIOS flash. As a result of this restriction, flash utilities supplied by AMI or Intel will not work .

UEFI Secure Boot

Secure Boot is a security standard defined in UEFI specification 2.3.1 that helps prevent malicious software applications and unauthorized operating systems from loading during system start up process. Without secure boot enabled (not supported or disabled), the computer simply hands over control to the bootloader without checking whether it is a trusted operating system or malware. With secure boot supported and enabled, the UEFI firmware starts the bootloader only if the bootloader's signature has maintained integrity and also if one of the following conditions is true:

- The bootloader was signed by a trusted authority that is registered in the UEFI database.
- The user has added the bootloader's digital signature to the UEFI database. The BIOS provides the key management setup sub-menu for this purpose.

Note

The congatec BIOS by default enables CSM (Compatibility Support Module) and disables secure boot because most of the industrial computers today boot in legacy (non-UEFI) mode. Since secure boot is only enabled when booting in native UEFI mode, you must therefore disable the CSM (compatibility support module) in the BIOS setup to enable Secure Boot.

A full description of secure boot is beyond the scope of this users guide. For more information about how secure boot leverages signature databases and keys, see the secure boot overview in the windows deployment options section of the Microsoft TechNet Library at http://technet.microsoft.com.

11.7.1.2 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to 'lock' and 'unlock' drives using the security password. A 'locked' drive will be detected by the system, but no data can be accessed. Accessing data on a 'locked' drive requires the proper password to 'unlock' the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within four attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

Note

If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

11.8 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen.

You can display a Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values of all the setup options.
► **Boot Override** List of all boot devices currently detected.	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to “Device Based”.

12 Additional BIOS Features

The BIOS setup description of the conga-TC87 can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative

12.1 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS is identified as BV87R1xx or BU87R1xx where:

- BV87 is the BIOS for modules with premium chipset
- BU87 is the BIOS for modules with mainstream chipset
- R is the identifier for a BIOS ROM file
- 1 is the so called feature number
- xx is the major and minor revision number.

The BV87 BIOS binary size is 16MB. The BU87 BIOS binary size is 8MB.

12.2 Updating the BIOS

BIOS updates are recommeded to correct platform issues or enhance the feature set of the module. The conga-TCG features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line [1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

12.3 Supported Flash Devices

The conga-TC87 supports the following flash device:

- Winbond W25Q128JVSIQ (8MB

The flash device listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.