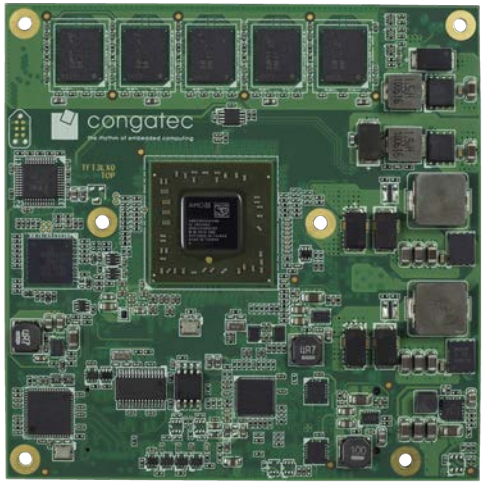

COM Express™ conga-TCG

Type 6 Compact Module based on AMD Embedded G-Series SoC

User's Guide

Revision 1.5

congatec

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2014-02-03	AEM	• Preliminary release
1.0	2015-03-05	AEM	• Added additional conga-TCG variants to "conga-TCG Options Information" in section 1 "Introduction" • Updated caution notes in sections 2.7 "Environmental Specifications" and 4 "Heatspreader" • Added the storage temperature range of industrial variants in section 2.7 "Environmental Specifications" • Updated section 6.6 "OEM BIOS Customization" • Added note about the configuration of fan_pwm pin as push-pull in section 7.3 "Thermal Management" and table 14 "Miscellaneous Signal Description" • Official release
1.1	2018-12-11	AEM	• Updated the information about handling electrostatic sensitive devices in preface section • Corrected the copyright date in the footer • Added note about the minimum storage requirement in section 2.2 "Supported Operating Systems" • Corrected the description of PWRBTN# signal in table 16 • Updated and reformatted section 2.5 "Power Consumption" • Updated section 3 "Block Diagram" • Updated sections 2.6 "Supply Voltage Battery Power", 2.7 "Environmental Specifications, 4 "Heatspreader" and 6 "Additional Features"
1.2	2020-08-14	AEM	• Corrected the product name in table 3 "Power Consumption Values" • Updated table 16 "Power and System Management Signal Descriptions" • Updated the link for the power supply implementation guidelines in section 5.1.12 "Power Control" • Updated section 4 "Cooling Solution" and added section 4.2 "CSP Dimensions" • Restructured sections 5 "Connector Rows" and 8 "Signal Descriptions and Pinout Tables" • Updated section 6 "Additional Features" • Added information about the congatec MLF file in section 11 "Additional BIOS Features" • Added section 11.1 "BIOS Versions" • Updated section 11.2 "Updating the BIOS" • Updated section 11.3 "Supported Flash Devices" • Deleted section 12 "Industry Specifications"
1.3	2021-04-19	AEM	• Updated table 2 "conga-TCG (commercial variants), table 3 "conga-TCG (industrial variants), table 4 "Feature Summary", table 9 "Display Combination" and table 18 "TMDS Signal Descriptions" • Updated section 3 "Block Diagram" and section 6.1.3 "Display Interfaces • Deleted section 5.1.3.1 "HDMI" and section 5.1.3.2 "Digital Visual Interface (DVI)" • Added note to table 18 "TMDS Signal Descriptions"
1.4	2021-07-31	AEM	• Added Software License Information • Changed congatec AG to congatec GmbH • Updated power supply implementation guidelines in section 5.1.15 "Power Control" • Updated section 6.7 "congatec Battery Management Interface"
1.5	2021-11-16	AEM	• Deleted HDMI references from section 2.1 "Feature List" and section 5.1.3 "Display Interfaces"

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-TCG. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide
COM Express™ Specification

The links to these documents can be found on the congatec GmbH website at www.congatec.com

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Note

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Terminology

Term	Description
cBC	congatec Board Controller
CGOS API	congatec Operating system Application Programming interface
DDI	Digital Display Interface
DVI	Digital Visual Interface
GB	Gigabyte
GHz	Gigahertz
HDA	High Definition Audio
I/F	Interface
KB	Kilobyte
KHz	Kilohertz
MB	Megabyte
Mbit	Megabit
MHz	Megahertz
N.C.	Not connected
N.A.	Not available
PCIe	PCI Express
SATA	Serial ATA
SoC	System on Chip
TBD	To be determined
TDP	Thermal Design Power

Contents

List of Tables

1 Introduction

1.1 COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available today. COM Express™ modules are available in following form factors:

- Mini 84 mm x 55 mm
- Compact 95 mm x 95 mm
- Basic 125 mm x 95 mm
- Extended 155 mm x 110 mm

Table 1 COM Express™ 2.1 Pinout Types

Types	Connector Rows	PCIe Lanes	PCI	IDE	SATA Ports	LAN ports	USB 2.0/ USB 3.0	Display Interfaces
Type 1	A-B	Up to 6		-	4	1	8 / 0	VGA, LVDS
Type 2	A-B C-D	Up to 22	32 bit	1	4	1	8 / 0	VGA, LVDS, PEG/SDVO
Type 3	A-B C-D	Up to 22	32 bit	-	4	3	8 / 0	VGA,LVDS, PEG/SDVO
Type 4	A-B C-D	Up to 32		1	4	1	8 / 0	VGA,LVDS, PEG/SDVO
Type 5	A-B C-D	Up to 32		-	4	3	8 / 0	VGA,LVDS, PEG/SDVO
Type 6	A-B C-D	Up to 24		-	4	1	8 / 4*	VGA,LVDS/eDP, PEG, 3x DDI
Type 10	A-B	Up to 4		-	2	1	8 / 2	LVDS/eDP, 1xDDI

** The SuperSpeed USB ports (USB 3.0) are not in addition to the USB 2.0 ports. Up to 4 of the USB 2.0 ports can support SuperSpeed USB*

The conga-TCG modules use the Type 6 pinout definition and comply with COM Express 2.1 specification. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are a legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 6 pinout provides the ability to offer PCI Express, Serial ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a

dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

1.2 Options Information

The conga-TCG is available in ten variants (eight commercial and two industrial). The table below shows the different configurations available.

Table 2 conga-TCG (commercial variants)

Part-No.	042000	042001	042002	042003	042004
SoC	AMD Embedded GX-420CA SoC	AMD Embedded GX-415GA SoC	AMD Embedded GX-217GA SoC	AMD Embedded GX-210HA SoC	AMD Embedded GX-420CA SoC
CPU Freq.	2.0 GHz Quad Core	1.5 GHz Quad Core	1.65 GHz Dual Core	1.0 GHz Dual Core	2.0 GHz Quad Core
L2 Cache	2 MB (Shared)	2 MB (Shared)	1 MB (Shared)	1 MB (Shared)	2 MB (Shared)
GPU Freq.	600 MHz	500 MHz	450 MHz	300 MHz	600 MHz
Graphic Engine	AMD Radeon™ HD 8400E	AMD Radeon™ HD 8330E	AMD Radeon™ HD 8280E	AMD Radeon™ HD 8210E	AMD Radeon™ HD 8400E
Onboard Memory	2 GB ECC DDR3L-1600	2 GB ECC DDR3L-1600	2 GB ECC DDR3L-1600	2 GB ECC DDR3L-1333	4 GB ECC DDR3L-1600
PCIe	4x	4x	4x	4x	4x
USB 3.0	2x	2x	2x	2x	2x
DDI	1x DP++	1x DP++	1x DP++	1x DP++	1x DP++
LVDS/eDP	LVDS	LVDS	LVDS	LVDS	LVDS
SoC TDP	25 W	15 W	15 W	9 W	25 W

Part-No.	042020	042021	042022
SoC	AMD Embedded GX-424CC SoC	AMD Embedded GX-412HC SoC	AMD Embedded GX-212JC SoC
CPU Freq.	2.4 GHz Quad Core	1.2/1.6 GHz Dual Core	1.2/1.4 GHz Dual Core
L2 Cache	2 MB (Shared)	1 MB (Shared)	2 MB (Shared)
GPU Freq.	497/800 MHz	300/400 MHz	300/350 MHz
Graphic Engine	AMD Radeon™ HD 8400E	AMD Radeon™ HD 8210E	AMD Radeon™ HD 8400E
Onboard Memory	4 GB ECC DDR3L-1600	4 GB ECC DDR3L-1333	2 GB ECC DDR3L-1300
PCIe	4x	4x	4x
USB 3.0	2x	2x	2x
DDI	1x DP++	1x DP++	1x DP++
LVDS/eDP	LVDS	LVDS	LVDS
SoC TDP	25 W	7 W	6 W

Table 3 conga-TCG (Industrial variants)

Part-No.	042010	042011
SoC	AMD Embedded GX-411GA SoC	AMD Embedded GX-209HA SoC
CPU Freq.	1.1 GHz Quad Core	1.0 GHz Dual Core
L2 Cache	2 MB (Shared)	1 MB (Shared)
GPU Freq.	300 MHz	225 MHz
Graphic Engine	AMD Radeon™ HD 8210E	AMD Radeon™ HD 8180E
Onboard Memory	2 GB ECC DDR3-1066	2 GB ECC DDR3-1066
PCIe	4x	4x
USB 3.0	2x	2x
DDI	1x DP++	1x DP++
LVDS/eDP	LVDS	LVDS
SoC TDP	15 W (Ext Temp)	9 W (Ext Temp)

2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 6 (Compact size 95 x 95 mm). Compliant with COM Express 2.1 specification.	
SoC	AMD Embedded G-Series SoC up to 25W TDP	
Memory	Up to 8GB ECC DDR3L-1600	
Chipset	Integrated in the SoC	
Audio	High Definition Audio (HDA) interface with support for multiple codecs	
Ethernet	Gigabit Ethernet via Intel® Ethernet Controller I210.	
Graphics Options	AMD Radeon™ HD 8000E Series Graphics with support for: - Video Compressing Engine (VCE 2.0) - Unified Video Decoder (UVD 4.2) - OpenGL 4.2, OpenCL™ 1.2, DirectX®11.2 - up to two independent displays	
	1x DP++ 1x VGA 1x LVDS 1x Optional eDP	NOTE: [1] *The conga-TCG does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.* [2] *Either eDP or LVDS signal is supported. Both signals are not supported together.*
Peripheral Interfaces	2x SATA® (up to 6 Gb/s) 4x PCI Express® Ports (5 Gb/s), supporting x1, x2 and x4 configurations 8x USB 2.0 (EHCI) 2x USB 3.0 (XHCI) SDIO interface (shared with GPIOs).	2x ExpressCard LPC Bus I²C Bus, Fast Mode, multimaster SM Bus
BIOS	AMI Aptio® V UEFI 2.x firmware; 8 MB serial flash memory with congatec Embedded BIOS features	
Power Management	ACPI compliant with battery support. Also supports Suspend to RAM (S3).	

Note

Some features are optional.

2.2 Supported Operating Systems

The conga-TCG supports the following operating systems.

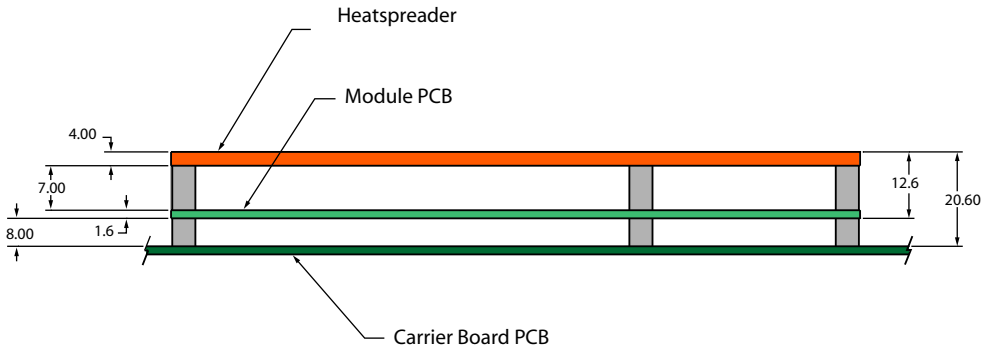
- Microsoft® Windows® 8
- Microsoft® Windows® 7
- Microsoft® Windows® Embedded Compact 7
- Microsoft® Windows® 7/8 Embedded Standard
- Linux

Note

The conga-TCG requires a minimum storage capacity of 16 GB (32-bit) or 20 GB (64-bit) for Windows 7/8 and WES7/8 installation. congatec will not offer support for systems that do not meet the minimum requirement.

2.3 Mechanical Dimensions

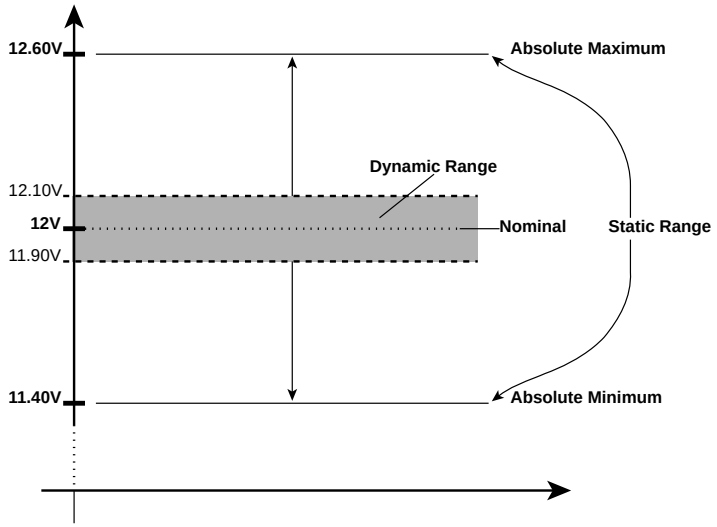
- 95.0 mm x 95.0 mm (3.74" x 3.74")
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5 mm (height) carrier board connector is used then approximate overall height is 18 mm. If the 8 mm (height) carrier board connector is used then approximate overall height is 21mm.



2.4 Supply Voltage Standard Power

- 12 V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-TCG COM
- modified congatec carrier board
- conga-TCG cooling solution
- Microsoft Windows 7 (64-bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool

Table 5 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle.	The CPU was stressed to its maximum frequency.
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency.
S0: Peak value	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.
S3	COM is powered by VCC_5V_SBY.	
S5	COM is powered by VCC_5V_SBY.	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Table 6 Power Consumption Values

The tables below provide additional information about the power consumption data for each of the conga-TCG variants offered. The values are recorded at various operating mode.

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64-bit)	CPU			Current (A)			
					Variant	Cores	Freq/Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S3
042000	2 x 2 GB	A.0	TFT3R002	Windows 7	AMD Embedded GX-420CA	4	2.00 / N.A	0.25	1.88	2.37	0.12
042001	2 x 2 GB	A.0	TFT3R002	Windows 7	AMD Embedded GX-415GA	4	1.50 / N.A	0.25	1.08	1.39	0.14
042002	2 GB	A.0	TFT3R003	Windows 7	AMD Embedded GX-217GA	2	1.65 / N.A	0.18	1.02	1.34	0.08
042003	2 GB	A.0	TFT3R003	Windows 7	AMD Embedded GX-210HA	2	1.00 / N.A	0.22	0.56	0.91	0.12
042010	2 GB	A.0	TFT3R002	Windows 7	AMD Embedded GX-411GA	4	1.10 / N.A	0.29	0.93	1.25	0.14
042011	2 GB	A.0	TFT3R002	Windows 7	AMD Embedded GX-209HA	2	1.00 / N.A	0.19	0.63	0.88	0.16

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

Supply power for S3 mode is 5V while all other measured modes are supplied with 12V power. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

2.6 Supply Voltage Battery Power

Table 7 CMOS Battery Power Consumption

RTC @	Voltage	Current
20°C	3V DC	3.3 µA

Note

1. *Do not use the CMOS battery power consumption value listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-TCG.*

2.7 Environmental Specifications

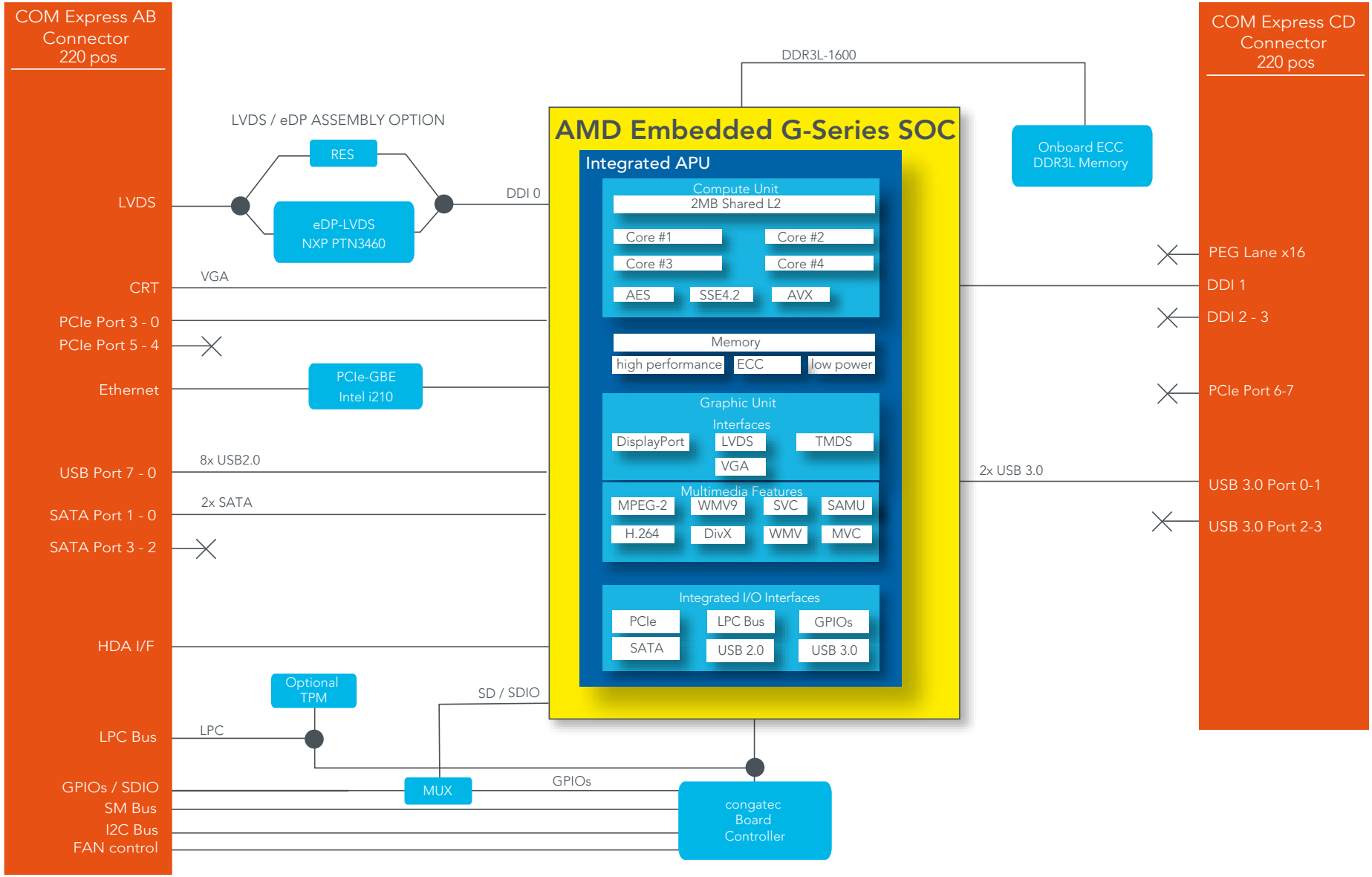
Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to 85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



4 Cooling Solution

congatec GmbH offers the following cooling solutions for the conga-TCG. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 8 Cooling Solution Variants

	Cooling Solution	Part No.	Description
1	HSP	042052	Standard heatspreader with M2.5 mm threaded standoffs
		042051	Standard heatspreader with 2.7 mm bore-hole standoffs
2	CSP	042054	Standard passive cooling solution with M2.5 mm threaded standoffs
		042053	Standard passive cooling solution with 2.7 mm bore-hole standoffs

Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*

2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification*

Caution

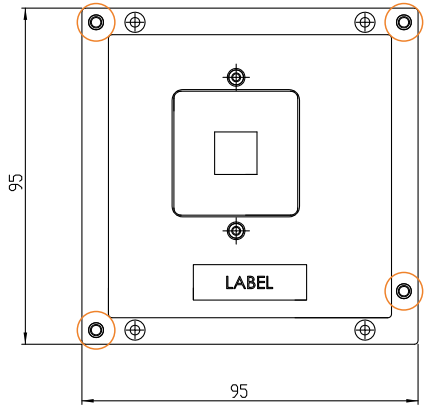
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

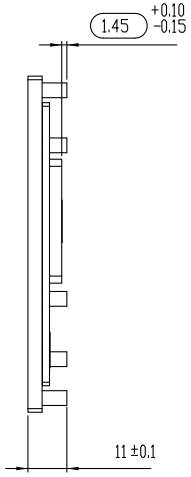
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

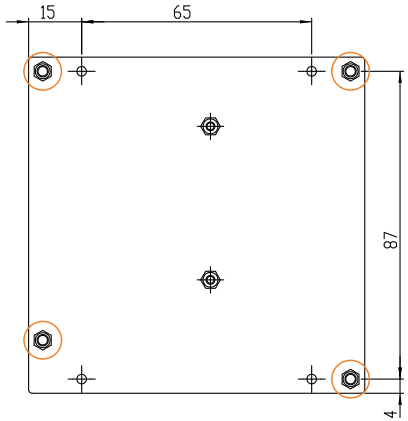
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

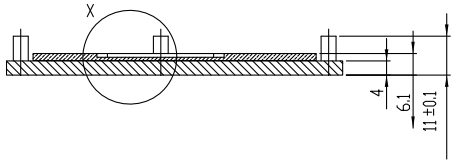
4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

4.1 HSP Dimensions

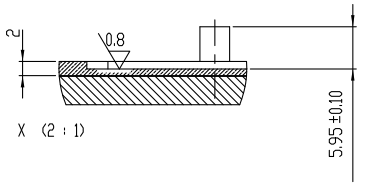


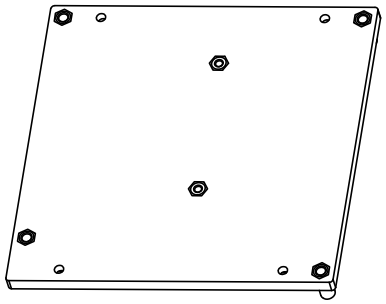


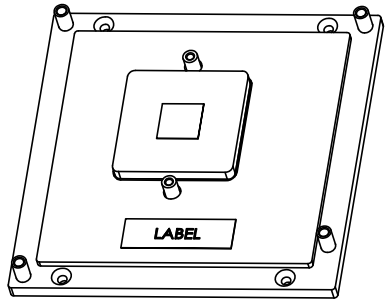




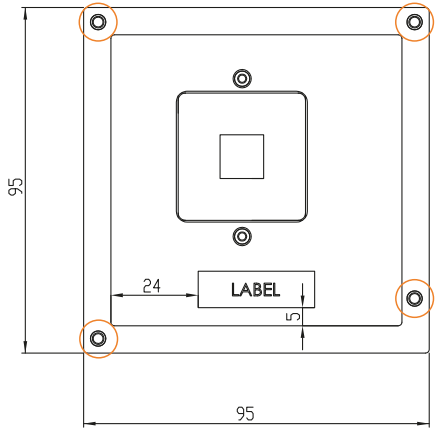
M2.5 x 10 mm
threaded standoff
for threaded version
or
ø2.7 x 10 mm
non-threaded standoff
for borehole version

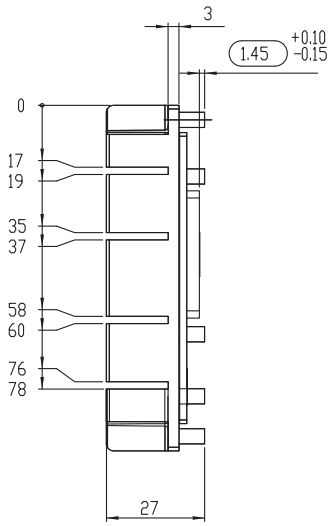


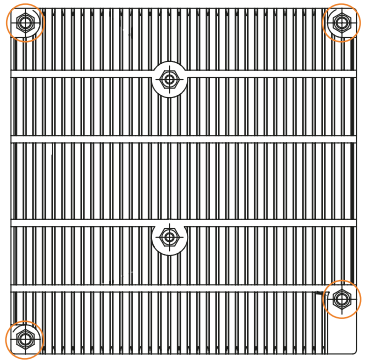


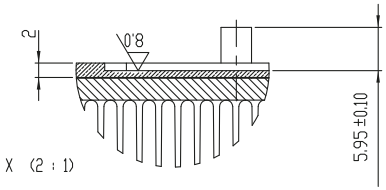


4.2 CSP Dimensions

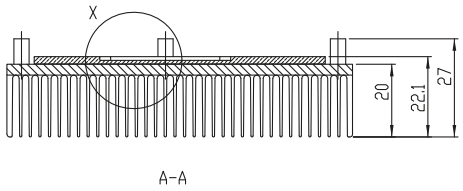




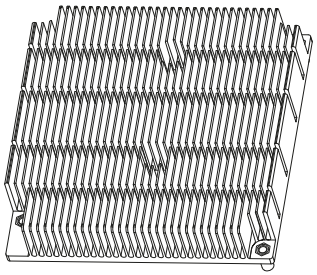


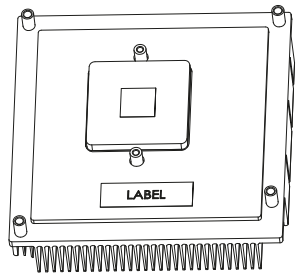


M2.5 x 10 mm
threaded standoff
for threaded version
or
ø2.7 x 10 mm
non-threaded standoff
for borehole version



A–A





5 Connector Rows

The conga-TCG is connected to the carrier board via two 220-pin connectors (COM Express Type 6 pinout). These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

5.1 Primary and Secondary Connector Rows A

The following subsystems can be found on the primary and secondary connector rows.

5.1.1 PCI Express™

The controller hub integrated in the AMD G-Series SoC provides four x1 general purpose PCI Express ports. The conga-TCG offers these four PCI Express™ ports externally on the A-B connector rows. These ports are PCI Express™ Gen. 2 compliant and can be configured as 4x1, 1x2 + 2x1, 2x2 or 1x4 links.

The PCIe interface is based on the PCI Express Specification 2.0 with Gen 1 and Gen 2 speeds.

5.1.2 PCI Express Graphics (PEG)

The conga-TCG does not support PCI Express Graphics.

5.1.3 Display Interface

The conga-TCG supports one Digital Display Interface on the C-D connector row. This interface supports:

- one DP++
- single- or dual-channel LVDS
- VGA
- up to two independent displays (combination of DP++, LVDS or VGA as shown in the table below)

Table 9 Display Combination

Display 1	Display 2	Display 1 Max. Resolution	Display 2 Max. Resolution
DP++ (DP/TMDS)	LVDS/eDP	DP: 2560x1600 @60Hz TMDS: 1920x1200 @60Hz	1920x1200 @60Hz
DP++ (DP/TMDS)	VGA	DP: 2560x1600 @60Hz TMDS: 1920x1200 @60Hz	2048x1536 @60Hz
LVDS	DP++ (DP/TMDS)	LVDS: 1920x1200 @60Hz	DP: 2560x1600 @60Hz TMDS: 1920x1200 @60Hz
LVDS	VGA	1920x1200 @60Hz	2048x1536 @60Hz
VGA	LVDS	2048x1536 @60Hz	1920x1200 @60Hz
VGA	DP++ (DP/TMDS)	2048x1536 @60Hz	DP: 2560x1600 @60Hz TMDS: 1920x1200 @60Hz

5.1.3.1 DisplayPort (DP)

The conga-TCG offers a dual-mode DisplayPort 1.2 interface on the DDI of the COM Express CD connector. The interface supports all mandatory features of the VESA DisplayPort Standard versions 1.2 including Multi-Stream Transport (MST) for monitor daisy-chaining, stereoscopic 3D frame transport, maximun bit rate of 5.4 Gbps and maximum display resolution of 2560x1600 at 60 Hz. Supported audio formats are linear PCM, Dolby Digital (AC-3), Dolby TrueHD, DTS, DTS-HD Master Audio and up to 8 channels.

The DP interface can be combined with LVDS/eDP or VGA interface to support two independent displays.

5.1.4 LVDS/eDP

The conga-TCG offers an LVDS interface on the A-B connector. The single/dual channel LVDS interface is provided by routing the onboard eDP to LVDS bridge device (NXP PTN3460) to one of the dedicated DisplayPort interfaces (DP0) of the G-Series SoC.

The eDP to LVDS bridge processes incoming DisplayPort stream and converts the DP protocol to LVDS, before transmitting the processed stream in LVDS format. The bridge supports single and dual channel signaling with color depths of 18 bits or 24 bits per pixel and pixel clock frequency up to 112 MHz.

Note

The conga-TCG can support eDP interface instead of the default LVDS interface by assembly option. The customized variant is available upon request but may require additional cost. For more information, contact congatec support team.

5.1.5 VGA

The conga-TCG supports one VGA interface on connector rows A-B. The interface supports a maximum resolution of 2048x1536 at a refresh rate of 60 Hz and 30 bpp. It also supports auto monitor detection and automatic power down for VGA DAC when a monitor is not attached.

5.1.6 SATA

The conga-TCG offers two SATA ports (SATA 0-1) on the A-B connector rows. These SATA ports are Gen 3 compliant, capable of up to 6.0 Gb/s transfer rate. Any of the ports can be configured to a lower transfer rate of 1.5 Gb/s for saving power.

The SATA controller supports two modes of operation - IDE and AHCI mode.

5.1.7 USB 2.0

The conga-TCG offers eight USB 2.0 via the OHCI and EHCI controllers. These controllers comply with USB 1.1 and 2.0 specifications. The USB ports are routed to connector rows A-B and each port is capable of supporting USB 1.1 and 2.0 compliant devices. For more information about how the USB host controllers are routed, see section 7.5.

Note

USB 2.0 ports 0 and 1 are connected to XHCI controller when USB 3.0 ports are enabled.

5.1.8 USB 3.0

The conga-TCG offers two RX and TX differential signal pairs on the COM Express C-D connector to support two USB 3.0 ports (USB 0 -1). Each USB 3.0 port requires corresponding USB 2.0 differential data pairs for USB 3.0 support.

The xHCI host controller provided by the SoC's controller hub controls these ports and allows data transfers of up to 5 Gb/s with SuperSpeed, highspeed, full-speed and low-speed traffic support. For more information about how the USB host controllers are routed, see section 7.5.

Note

USB 2.0 ports 0 and 1 are connected to XHCI controller when USB 3.0 ports are enabled.

5.1.9 Gigabit Ethernet

The conga-TCG offers Gigabit Ethernet with the integration of Intel i210 Ethernet Controller. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MDI0± to GBE0_MDI3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

Note

The GBE0_LINK# output is not active during a 10 Mb connection. It is only active during a 100 Mb or 1 Gb connection. This is a limitation of Ethernet Phy since it has only three LED outputs—ACT#, LINK100# and LINK1000#.

The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TCG module.

5.1.10 High Definition Audio (HDA)

The conga-TCG offers a HDA interface on the COM Express A-B connector rows. This interface supports the connection of external HD audio codecs over the HD audio link and is routed from the HD audio controller integrated in the controller hub. The HD audio controller supports up to four audio codecs and each codec has its own data input for the HD Audio interface

Note

COM Express modules support only up to three data inputs (HDA_SDIN[0:2]) as described in COM Express Specification 2.1.

The conga-TCG does not support AC'97 codecs.

5.1.11 LPC Bus

The conga-TCG offers the Low Pin Count (LPC) bus via the integrated controller hub. The LPC host bus controller supports one master DMA device. TPM version 1.1/1.2 devices are also supported. See section 9.1.1 for more information about the LPC Bus.

5.1.12 I²C Bus Fast Mode

The I²C bus is implemented through the congatec board controller and is accessed through the congatec CGOS driver and API. The controller provides a Fast Mode multi-master I²C Bus that has maximum I²C bandwidth.

5.1.13 ExpressCard™

The conga-TCG supports the implementation of two ExpressCards, which require the dedication of USB port or x1 PCI Express link for each ExpressCard used.

5.1.14 General Purpose Serial Interface

Two TTL compatible two wire ports are available on Type 6 COM Express modules. These pins are designated SER0_TX, SER0_RX, SER1_TX and SER1_RX. Data out of the module is on the _TX pins. Hardware handshaking and hardware flow control are not supported. The module asynchronous serial ports are intended for general purpose use and for use with debugging software that make use of the "console redirect" features available in many operating systems.

The conga-TCG offers two UART interfaces via the congatec Board Controller. The UART controllers integrated in the cBC support up to 1MBit/s and can operate in low-speed, full-speed and high-speed modes. The UART interfaces are routed to the A-B connector and require congatec driver to function.

Note

The UART interfaces do not support legacy COM port emulation.

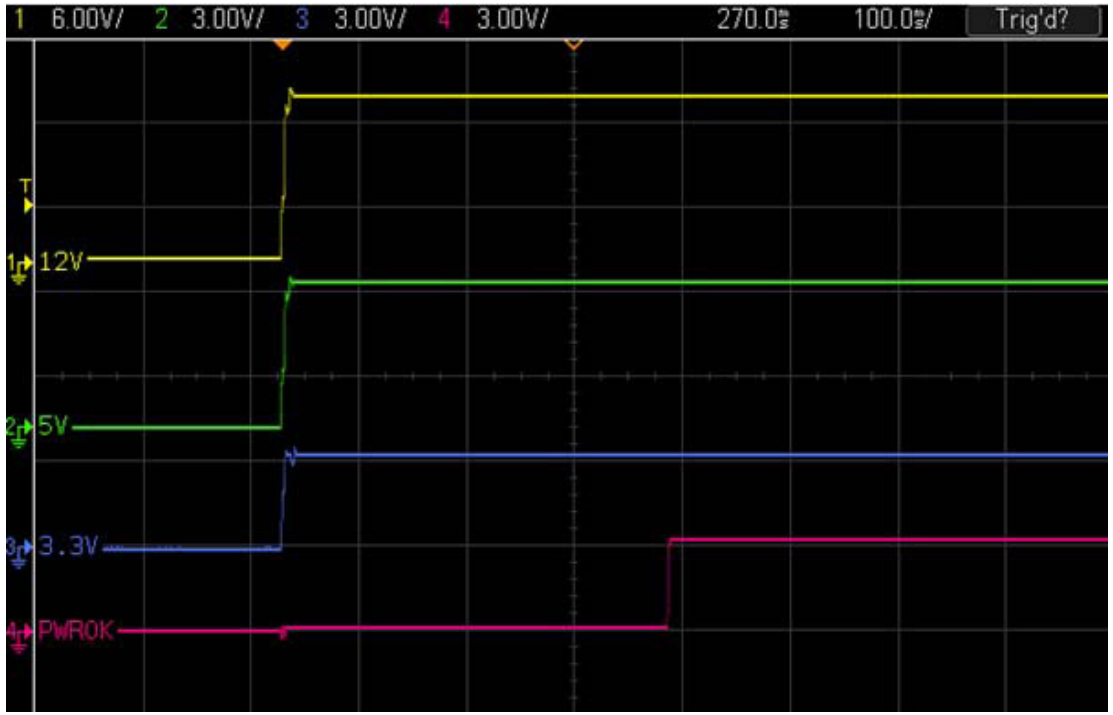
5.1.15 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. The PWR_OK is a 3.3V signal according to the COM Express Specification. The use of this input is optional.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. Although the PWR_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

A sample screenshot is shown below:



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the "power good" signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, it must be ensured that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-TCG module is capable of generating it's own power good through the use of an internal monitor on the +12V ± 5% input voltage and/or the internal power supplies. The conga-TCG also provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-TCG's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

The 12 volt input power is the sole operational power source for the conga-TCG. Other required voltages are generated internally on the module using onboard voltage regulators.

Note

When designing a power supply for a conga-TCG application, be aware that the system may malfunction when a 12V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.

The cause of this problem is that some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.

To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope, during the power supply qualication phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

5.1.16 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

6 Additional Features

6.1 congatec Board Controller (cBC)

The conga-TCG is equipped with Texas Instruments microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

6.2 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.3 Watchdog

The conga-TCG is equipped with a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, see the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

Note

The conga-TCG module does not support the watchdog NMI mode.

6.4 I²C Bus

The conga-TCG supports I²C bus. The I²C bus is accessed through the CGOS driver and API. It is multi-master capable and runs at fast mode.

6.5 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

6.6 OEM BIOS Customization

The conga-TCG is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

6.6.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.6.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.6.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.6.4 OEM BIOS Code/Data

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support verb tables for HDA codecs, PCI/PCIe OpROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.6.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.7 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-TCG BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface, contact your local sales representative.

6.8 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available on the congatec website.

6.9 Security Features

The conga-TCG offers an optional Trusted Platform Module (TPM 1.2).

6.10 Suspend to Ram

The Suspend to RAM feature is available on the conga-TCG.

7 conga Tech Notes

The conga-TCG has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

7.1 AMD Processor Features

7.1.1 AMD64 Technology

- AMD64 technology instruction-set extensions
- 64-bit integer registers, 48-bit virtual addresses, and 40-bit physical addresses
- Sixteen 64-bit integer registers
- Sixteen 128-bit SSE/SSE2/SSE3/SSE4a registers

For more information about AMD64 Technology, visit http://www.amd.com.

7.1.2 Power Management

- Multiple low-power states
- AMD AllDay™ power technology
- System Management Mode (SMM)
- ACPI-compliant, including support for processor performance states (P-states)
- Supports processor power states C0, C1, CC6, and PC6
- Supports sleep states including S0, S3, S4, and S5
- PCIe® core power gating
- PCIe speed power policy

For more information about AMD64 Technology, visit http://www.amd.com.

7.1.3 AMD Virtualization™ Technology

- SVM pause count capability
- SVM disable and lock
- Rapid virtualization indexing (nested paging)
- Improved world-switch speed

For more information about AMD64 Technology, visit http://www.amd.com.

Note

congatec supports RTS Hypervisor

7.2 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This enables the operating system to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-TCG ACPI thermal solution offers three different cooling policies:

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

Note

The congatec COM Express Type 6 and Type 10 modules use a Push-Pull output for the fan_pwm signal instead of the open drain output specified in the COM Express specification. Although this does not comply with the COM Express specification 2.0, the benefits are obvious. The Push-Pull output optimizes the power consumed by the fan_pwm signal without functional change.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points. If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.3 ACPI Suspend Modes and Resume Events

conga-TCG supports S3. For more information about S3 wake events see section 10.4.7 "ACPI Submenu".

Table 10 Wake Events

The table below lists the events that wake the system from S3

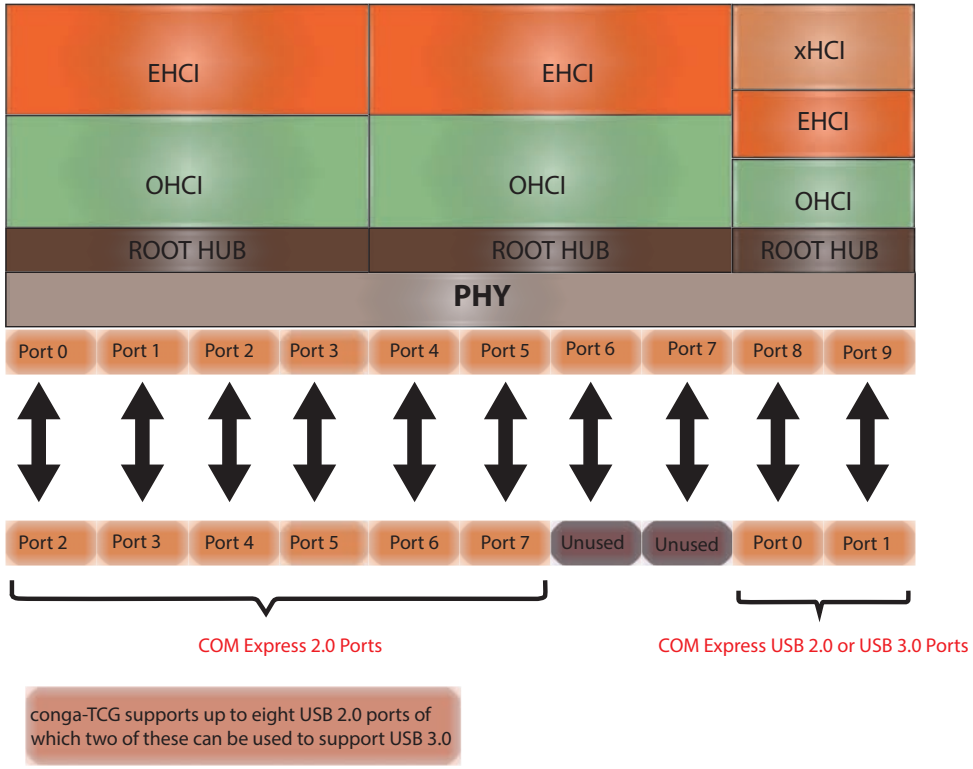
Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S3-S5.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
USB Mouse/Keyboard Event	When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event. USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program).
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

7.4 USB Host Controller

The conga-TCG offers up to eight USB 2.0 ports. Two of these ports (0 and 1) can be used together with the SuperSpeed signals on the CD connector to support USB 3.0. In general, the conga-TCG supports up to eight USB 2.0 or up to six USB 2.0 and two USB 3.0.

The integrated controller hub in the SoC supports these ports with one xHCI controller and three OHCI/EHCI controller pairs. The routing diagram is shown below:

Routing Diagram



CONTROLLER	COM EXPRESS
XHCI/EHCI/OHCI Port 8	USB0
	USB0_SS_TX
	USB0_SS_RX
XHCI/EHCI/OHCI Port 9	USB1
	USB1_SS_TX
	USB1_SS_RX
EHCI/OHCI Port 0	USB2
EHCI/OHCI Port 1	USB3
EHCI/OHCI Port 2	USB4
EHCI/OHCI Port 3	USB5
EHCI/OHCI Port 4	USB6
EHCI/OHCI Port 5	USB7
EHCI/OHCI Port 6	Unused
EHCI/OHCI Port 7	Unused

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type 6 connectors used for congatec GmbH modules. The pinout of the modules complies with COM Express Type 6 Rev. 2.1.

Table 3 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented on module.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Table 11 Signal Tables Terminology Descriptions

Term	Description
PU	Implemented pull-up resistor
PD	Implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Bi-directional signal 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
O 3.3V/12V	Output 3.3V/12V tolerant
I 3.3V/12V	Input 3.3V/12V tolerant
P	Power Input
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0
PEG	PCI Express Graphics
SATA	In compliance with Serial ATA specification, Revision 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

8.1 Connector Signal Descriptions

Table 12 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4- (*)	B56	PCIE_RX4- (*)
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# (*)	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4# (*)	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+ (*)	B22	SATA3_TX+(*)	A77	LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX-(*)	B23	SATA3_TX-(*)	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+ (*)	B25	SATA3_RX+ (*)	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX- (*)	B26	SATA3_RX- (*)	A81	LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA_BITCLK	B32	SPKR	A87	RSVD	B87	VCC_5V_SBY
A33	AC/HDA_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED
A35	THRMTRIP# (*)	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+ (*)	B52	PCIE_RX5+ (*)	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5- (*)	B53	PCIE_RX5- (*)	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+ (*)	B55	PCIE_RX4+ (*)	A110	GND (FIXED)	B110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-TCG.

Table 13 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1- (*)	D56	PEG_TX1- (*)
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+ (*)	D58	PEG_TX2+ (*)
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2- (*)	D59	PEG_TX2- (*)
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PEG_RX3+ (*)	D61	PEG_TX3+ (*)
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PEG_RX3- (*)	D62	PEG_TX3- (*)
C8	GND	D8	GND	C63	RSVD	D63	RSVD
C9	USB_SSRX2- (*)	D9	USB_SSTX2- (*)	C64	RSVD	D64	RSVD
C10	USB_SSRX2+ (*)	D10	USB_SSTX2+ (*)	C65	PEG_RX4+ (*)	D65	PEG_TX4+ (*)
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4- (*)	D66	PEG_TX4- (*)
C12	USB_SSRX3- (*)	D12	USB_SSTX3- (*)	C67	RSVD	D67	GND
C13	USB_SSRX3+ (*)	D13	USB_SSTX3+ (*)	C68	PEG_RX5+ (*)	D68	PEG_TX5+ (*)
C14	GND	D14	GND	C69	PEG_RX5- (*)	D69	PEG_TX5- (*)
C15	DDI1_PAIR6+ (*)	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	DDI1_PAIR6- (*)	D16	DDI1_CTRLDATA_AUX-	C71	PEG_RX6+ (*)	D71	PEG_TX6+ (*)
C17	RSVD	D17	RSVD	C72	PEG_RX6- (*)	D72	PEG_TX6- (*)
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	PCIE_RX6+ (*)	D19	PCIE_TX6+ (*)	C74	PEG_RX7+ (*)	D74	PEG_TX7+ (*)
C20	PCIE_RX6- (*)	D20	PCIE_TX6- (*)	C75	PEG_RX7- (*)	D75	PEG_TX7- (*)
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+ (*)	D22	PCIE_TX7+ (*)	C77	RSVD	D77	RSVD
C23	PCIE_RX7- (*)	D23	PCIE_TX7- (*)	C78	PEG_RX8+ (*)	D78	PEG_TX8+ (*)
C24	DDI1_HPD	D24	RSVD	C79	PEG_RX8- (*)	D79	PEG_TX8- (*)
C25	DDI1_PAIR4+ (*)	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	DDI1_PAIR4- (*)	D26	DDI1_PAIR0+	C81	PEG_RX9+ (*)	D81	PEG_TX9+ (*)
C27	RSVD	D27	DDI1_PAIR0-	C82	PEG_RX9- (*)	D82	PEG_TX9- (*)
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD
C29	DDI1_PAIR5+ (*)	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	DDI1_PAIR5- (*)	D30	DDI1_PAIR1-	C85	PEG_RX10+ (*)	D85	PEG_TX10+ (*)
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- (*)	D86	PEG_TX10- (*)
C32	DDI2_CTRLCLK_AUX+ (*)	D32	DDI1_PAIR2+	C87	GND	D87	GND
C33	DDI2_CTRLDATA_AUX- (*)	D33	DDI1_PAIR2-	C88	PEG_RX11+ (*)	D88	PEG_TX11+ (*)
C34	DDI2_DDC_AUX_SEL (*)	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11- (*)	D89	PEG_TX11- (*)
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+ (*)	D36	DDI1_PAIR3+	C91	PEG_RX12+ (*)	D91	PEG_TX12+ (*)
C37	DDI3_CTRLDATA_AUX- (*)	D37	DDI1_PAIR3-	C92	PEG_RX12- (*)	D92	PEG_TX12- (*)
C38	DDI3_DDC_AUX_SEL (*)	D38	RSVD	C93	GND	D93	GND

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C39	DDI3_PAIR0+ (*)	D39	DDI2_PAIR0+ (*)	C94	PEG_RX13+ (*)	D94	PEG_TX13+ (*)
C40	DDI3_PAIR0- (*)	D40	DDI2_PAIR0- (*)	C95	PEG_RX13- (*)	D95	PEG_TX13- (*)
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+ (*)	D42	DDI2_PAIR1+ (*)	C97	RVSD	D97	RSVD
C43	DDI3_PAIR1- (*)	D43	DDI2_PAIR1- (*)	C98	PEG_RX14+ (*)	D98	PEG_TX14+ (*)
C44	DDI3_HPD (*)	D44	DDI2_HPD (*)	C99	PEG_RX14- (*)	D99	PEG_TX14- (*)
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+ (*)	D46	DDI2_PAIR2+ (*)	C101	PEG_RX15+ (*)	D101	PEG_TX15+ (*)
C47	DDI3_PAIR2- (*)	D47	DDI2_PAIR2- (*)	C102	PEG_RX15- (*)	D102	PEG_TX15- (*)
C48	RSVD	D48	RSVD	C103	GND	D103	GND
C49	DDI3_PAIR3+ (*)	D49	DDI2_PAIR3+ (*)	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3- (*)	D50	DDI2_PAIR3- (*)	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+ (*)	D52	PEG_TX0+ (*)	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0- (*)	D53	PEG_TX0- (*)	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV# (*)	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+ (*)	D55	PEG_TX1+ (*)	C110	GND (FIXED)	D110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-TCG.

Table 14 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0. Not connected in variants with TDP < 9W.
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0. Not connected in variants with TDP < 9W.
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Not connected
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Not connected
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Not connected
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Not connected
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		Not connected
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		Not connected
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		Not connected
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		Not connected
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 15 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs.	I PCIE		Not connected.
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+	D52	PCI Express Graphics Transmit Output differential pairs.	O PCIE		Not connected.
PEG_TX0-	D53				
PEG_TX1+	D55				
PEG_TX1-	D56				
PEG_TX2+	D58				
PEG_TX2-	D59				
PEG_TX3+	D61				
PEG_TX3-	D62				
PEG_TX4+	D65				
PEG_TX4-	D66				
PEG_TX5+	D68				
PEG_TX5-	D69				
PEG_TX6+	D71				
PEG_TX6-	D72				
PEG_TX7+	D74				
PEG_TX7-	D75				
PEG_TX8+	D78				
PEG_TX8-	D79				
PEG_TX9+	D81				
PEG_TX9-	D82				
PEG_TX10+	D85				
PEG_TX10-	D86				
PEG_TX11+	D88				
PEG_TX11-	D89				
PEG_TX12+	D91				
PEG_TX12-	D92				
PEG_TX13+	D94				
PEG_TX13-	D95				
PEG_TX14+	D98				
PEG_TX14-	D99				
PEG_TX15+	D101				
PEG_TX15-	D102				
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I		Not connected.

Note

conga-TCG does not support PCI Express Graphics (PEG).

Table 16 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with SDVO1_RED+, DP1_LANE0+ and TMDS1_DATA2+. Multiplexed with SDVO1_RED-, DP1_LANE0- and TMDS1_DATA2-.	O PCIE		
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with SDVO1_GRN+, DP1_LANE1+ and TMDS1_DATA1+. Multiplexed with SDVO1_GRN-, DP1_LANE1- and TMDS1_DATA1-.	O PCIE		
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with SDVO1_BLU+, DP1_LANE2+ and TMDS1_DATA0+. Multiplexed with SDVO1_BLU-, DP1_LANE2- and TMDS1_DATA0-.	O PCIE		
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with SDVO1_CK+, DP1_LANE3+ and TMDS1_CLK+. Multiplexed with SDVO1_CK-, DP1_LANE3- and TMDS1_CLK-.	O PCIE		
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	Multiplexed with SDVO1_INT+. Multiplexed with SDVO1_INT-.			Not connected
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	Multiplexed with SDVO1_TVCLKIN+. Multiplexed with SDVO1_TVCLKIN-.			Not connected
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	Multiplexed with SDVO1_FLDSTALL+. Multiplexed with SDVO1_FLDSTALL-.			Not connected
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD.	I 3.3V	PD 100K	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with SDVO1_CTRLCLK, DP1_AUX+ and HMDI1_CTRLCLK. DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE OD 3.3V	PD100K	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with SDVO1_CTRLDATA, DP1_AUX- and HDMI1_CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE I/OD 3.3V	PU 100K 3.3V	
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+ and TMDS2_DATA2+. Multiplexed with DP2_LANE0- and TMDS2_DATA2-.	O PCIE		Not supported by default assembly variants.
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+ and TMDS2_DATA1+. Multiplexed with DP2_LANE1- and TMDS2_DATA1-.	O PCIE		Not supported by default assembly variants.
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+ and TMDS2_DATA0+. Multiplexed with DP2_LANE2- and TMDS2_DATA0-.	O PCIE		Not supported by default assembly variants.
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+ and TMDS2_CLK+. Multiplexed with DP2_LANE3- and TMDS2_CLK-.	O PCIE		Not supported by default assembly variants.
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD.	I 3.3V	PD 100K	Not supported by default assembly variants.
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+ and HDMI2_CTRLCLK. DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	I/O PCIE OD 3.3V	PD 100K	Not supported by default assembly variants.
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/OD 3.3V	PU 100K 3.3V	Not supported by default assembly variants.

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	Not supported by default assembly variants.
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+. Multiplexed with DP3_LANE0- and TMDS3_DATA2-.	O PCIE		Not connected
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+. Multiplexed with DP3_LANE1- and TMDS3_DATA1-.	O PCIE		Not connected
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+. Multiplexed with DP3_LANE2- and TMDS3_DATA0-.	O PCIE		Not connected
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+. Multiplexed with DP3_LANE3- and TMDS3_CLK-.	O PCIE		Not connected
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD.	I 3.3V	PD 100K	Not connected
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK. DP AUX+ function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high	I/O PCIE OD 3.3V	PD 100k	Not connected
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA. DP AUX- function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.	I/O PCIE I/OD 3.3V	PU 100k	Not connected
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	Not connected

Note

The conga-TCG supports one DDI interface on the COM Express CD connector. This interface supports only dual-mode DisplayPort 1.2 on the connector. To support TMDS, an external level shifter e.g PTN3360D should be implemented on the user's carrier board.

Table 17 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE3+ DP1_LANE3-	D36 D37	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
DP1_LANE2+ DP1_LANE2-	D32 D33	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
DP1_LANE1+ DP1_LANE1-	D29 D30	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		
DP1_LANE0+ DP1_LANE0-	D26 D27	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
DP1_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI1_HPD.	I 3.3V	PD 100K	
DP1_AUX+	D15	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100K	
DP1_AUX-	D16	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100K 3.3V	
DP2_LANE3+ DP2_LANE3-	D49 D50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		Not supported by default assembly variants.
DP2_LANE2+ DP2_LANE2-	D46 D47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		Not supported by default assembly variants.
DP2_LANE1+ DP2_LANE1-	D42 D43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		Not supported by default assembly variants.
DP2_LANE0+ DP2_LANE0-	D39 D40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR0+ and DDI1_PAIR0-	O PCIE		Not supported by default assembly variants.
DP2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI2_HPD.	I 3.3V	PD 100K	Not supported by default assembly variants.
DP2_AUX+	C32	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100K	Not supported by default assembly variants.
DP2_AUX-	C33	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100K 3.3V	Not supported by default assembly variants.
DP3_LANE3+ DP3_LANE3-	C49 C50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		Not connected

Signal	Pin #	Description	I/O	PU/PD	Comment
DP3_LANE2+ DP3_LANE2-	C46 C47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		Not connected
DP3_LANE1+ DP3_LANE1-	C42 C43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-.	O PCIE		Not connected
DP3_LANE0+ DP3_LANE0-	C39 C40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		Not connected
DP3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI3_HPD.	I 3.3V	PD 100K	Not connected
DP3_AUX+	C36	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	Not connected
DP3_AUX-	C37	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	Not connected

Note

The conga-TCG supports one DDI interface on the COM Express CD connector. This interface supports only dual-mode DisplayPort 1.2 on the connector. To support TMDS, an external level shifter e.g PTN3360D should be implemented on the user's carrier board.

Table 18 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS1_CLK + TMDS1_CLK -	D36 D37	TMDS Clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		Not supported
TMDS1_DATA0+ TMDS1_DATA0-	D32 D33	TMDS differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		Not supported
TMDS1_DATA1+ TMDS1_DATA1-	D29 D30	TMDS differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-..	O PCIE		Not supported
TMDS1_DATA2+ TMDS1_DATA2-	D26 D27	TMDS differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		Not supported
HDMI1_HPD	C24	TMDS Hot-plug detect. Multiplexed with DDI1_HPD.	I PCIE	PD 100K	Not supported
HDMI1_CTRLCLK	D15	TMDS I^2C Control Clock Multiplexed with DDI1_CTRLCLK_AUX+	OD 3.3V	PD 100K	Not supported
HDMI1_CTRLDATA	D16	TMDS I^2C Control Data Multiplexed with DDI1_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	Not supported
TMDS2_CLK + TMDS2_CLK -	D49 D50	TMDS Clock output differential pair.. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-.	O PCIE		Not Supported

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS2_DATA0+ TMDS2_DATA0-	D46 D47	TMDS differential pair. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-.	O PCIE		Not Supported
TMDS2_DATA1+ TMDS2_DATA1-	D42 D43	TMDS differential pair. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-.	O PCIE		Not Supported
TMDS2_DATA2+ TMDS2_DATA2-	D39 D40	TMDS differential pair. Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-..	O PCIE		Not Supported
HDMI2_HPD	D44	TMDS Hot-plug detect. Multiplexed with DDI2_HPD	I PCIE	PD 100K	Not Supported
HDMI2_CTRLCLK	C32	TMDS I²C Control Clock Multiplexed with DDI2_CTRLCLK_AUX+	OD 3.3V	PD 100K	Not Supported
HDM12_CTRLDATA	C33	TMDS I²C Control Data Multiplexed with DDI2_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	Not Supported
TMDS3_CLK + TMDS3_CLK -	C49 C50	TMDS Clock output differential pair.. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		Not Supported
TMDS3_DATA0+ TMDS3_DATA0-	C46 C47	TMDS differential pair. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		Not Supported
TMDS3_DATA1+ TMDS3_DATA1-	C42 C43	TMDS differential pair. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-..	O PCIE		Not Supported
TMDS3_DATA2+ TMDS3_DATA2-	C39 C40	TMDS differential pair. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		Not Supported
HDMI3_HPD	C44	TMDS Hot-plug detect. Multiplexed with DDI3_HPD.	I PCIE	PD 100K	Not Supported
HDMI3_CTRLCLK	C36	TMDS I²C Control Clock Multiplexed with DDI3_CTRLCLK_AUX+	OD 3.3V	PD 100K	Not Supported
HDMI3_CTRLDATA	C37	TMDS I²C Control Data Multiplexed with DDI3_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	Not Supported

Note

The conga-TCG supports one DDI interface (DP++) on the COM Express C-D connector. It does not natively support TMDS. A DP++ to TMDS converter (e.g PTN3360D) needs to be implemented.

Table 19 SDVO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDVO1_RED+ SDVO1_RED-	D26 D27	Serial Digital Video red output differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0- pair.	O PCIE		Not supported
SDVO1_GRN+ SDVO1_GRN-	D29 D30	Serial Digital Video green output differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		Not supported
SDVO1_BLU+ SDVO1_BLU-	D32 D33	Serial Digital Video blue output differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		Not supported
SDVO1_CK+ SDVO1_ CK-	D36 D37	Serial Digital Video clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		Not supported
SDVO1_INT+ SDVO1_INT-	C25 C26	Serial Digital Video Interrupt input differential pair. .Multiplexed with DDI1_PAIR4+ and DDI1_PAIR4-.	I PCIE		Not supported
SDVO1_TVCLKIN+ SDVO1_TVCLKIN-	C29 C30	Serial Digital Video TVOUT synchronization clock pair. Multiplexed with DDI1_PAIR5+ and DDI1_PAIR5-.	I PCIE		Not supported
SDVO1_FLDSTALL+ SDVO1_FLDSTALL-	C15 C16	Serial Digital Video Field Stall input differential pair. Multiplexed with DDI1_PAIR6+ and DDI1_PAIR6-.	I PCIE		Not supported
SDVO1_CTRLCLK	D15	SDVO I²C clock line - to set up SDVO peripherals. Multiplexed with DDI1_CTRLCLK_AUX+.	I/O OD 3.3V		Not supported
SDVO1_CTRLDATA	D16	SDVO I²C data line - to set up SDVO peripherals. Multiplexed with DDI1_CTRLDATA_AUX-.	I/O OD 3.3V		Not supported

Note

SDVO is not supported on the conga-TCG.

Table 20 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/OD	PU 4.7K 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/OD	PU 4.7K 3.3V	

Table 21 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10K	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10K	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	OD 3.3V	PU 2.2K 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/OD 3.3V	PU 2.2K 3.3V	

Table 22 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Not connected
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Not connected
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Not connected
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Not connected
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V		

Table 23 USB 2.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

Table 24 USB 3.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX0-	C3		I		
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX0-	D3		O		
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX1-	C6		I		
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX1-	D6		O		
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I		Not connected
USB_SSRX2-	C9		I		Not connected
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not connected
USB_SSTX2-	D9		O		Not connected
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I		Not connected
USB_SSRX3-	C12		I		Not connected
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not connected
USB_SSTX3-	D12		O		Not connected

Table 25 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/ PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		Twisted pair signals for external transformer.
			1000	100	10			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.				O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.				O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.				O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.						Not connected

Note

The GBE0_LINK# output is only active during a 100Mbit or 1Gbit connection, it is not active during a 10Mbit connection. The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TCG module.

Table 26 High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	High Definition Audio Reset: This signal is the master hardware reset to external codec(s).	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SYNC	A29	High Definition Audio Sync: This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_BITCLK	A32	High Definition Audio Bit Clock Output: This signal is a 24.000MHz serial data clock generated by the High Definition Audio controller.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SDOUT	A33	High Definition Audio Serial Data Out: This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for High Definition Audio.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SDIN[2:0]	B28-B30	High Definition Audio Serial Data In [0]: These signals are serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for High Definition Audio.	I 3.3VSB	PD 47K	AC'97 codecs are not supported.

Table 27 ExpressCard Support Pins Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request.	I 3.3VSB	PU 10k 3.3VSB	
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3V		

Table 28 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V	PU 47K 3.3V	
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V	PU 47K 3.3V	LPC_DRQ1# is not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/OD 3.3V	PU 47K 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		

Table 29 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10K 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB	PD 50K	
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or left as no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or left as no-connect

Table 30 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/OD 3.3VSB	PU 2.2K 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/OD 3.3VSB	PU 2.2K 3.3VSB	
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V	PD 10K	
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PD 10K	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O 3.3V/12V		Signal is driven to logic 1 only. External Pull down is required.
FAN_TACHIN	B102	Fan tachometer input.	I 3.3V/12V	PU 47K 3.3V	Requires a fan with two-pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 10K	Trusted Platform Module chip is optional.

Note

The congatec COM Express Type 6 and Type 10 modules use a Push-Pull output for the fan_pwm signal instead of the open drain output specified in the COM Express specification. Although this does not comply with the COM Express specification 2.0, the benefits are obvious. The Push-Pull output optimizes the power consumed by the fan_pwm signal without functional change.

Table 31 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3V		
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3V		
GPO2	B57	General purpose output pins. Shared with SD_WP. Input to COM Express, output from SD	O 3.3V / I 3.3V	SD mode: PU 47K 3.3V	
GPO3	B63	General purpose output pins. Shared with SD_CD. Input to COM Express, output from SD	O 3.3V / I 3.3V	SD mode: PU 47K 3.3V	
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3V	PU 10K 3.3V	

Table 32 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V	PU 10K 3.3V	
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		Not supported
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10K 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10K 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 10k 3.3V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10k 3.3V	Not supported
SMB_CK	B13	System Management Bus bidirectional clock line.	I/OD 3.3VSB	PU 2.2K 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line.	I/OD 3.3VSB	PU 2.2K 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3VSB	PU 10K 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3V/12V	PU 47K 3.3VSB	
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3V/12V	PU 47K 3.3VSB	

Table 33 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O 3.3V/12V		Signal is driven to logic 1 only. External PD is required.
SER1_TX	A101	General purpose serial port transmitter	O 3.3V/12V		Signal is driven to logic1 only. External PD is required.
SER0_RX	A99	General purpose serial port receiver	I 3.3V/12V	PU 47K 3.3V	
SER1_RX	A102	General purpose serial port receiver	I 3.3V/12V	PU 47K 3.3V	

Table 34 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# / TYPE1# / TYPE0# / X / X / X / Pinout Type 1 NC / NC / NC / Pinout Type 2 NC / NC / GND / Pinout Type 3 (no IDE) NC / GND / NC / Pinout Type 4 (no PCI) NC / GND / GND / Pinout Type 5 (no IDE, no PCI) GND / NC / NC / Pinout Type 6 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.	PDS	TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard. The conga-TCG is based on the COM Express Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.
TYPE10#	A97	Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed. TYPE10# NC – Pinout R2.0 PD – Pinout Type 10 pull down to ground with 4.7k resistor 12V – Pinout R1.0 This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7k resistor.	PDS	Not connected to indicate "Pinout R2.0".

Table 35 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109 C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110 C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

8.2 Boot Strap Signals

Table 36 Boot Strap Signal Descriptions

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V	PU 10K 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V	PU 10K 3.3V	
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V	PU 1k 3.3V	

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either COM Express™ internally implemented resistors or chipset internally implemented resistors that are located on the module.

No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM Express™ module to malfunction and/or cause irreparable damage to the module.

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-TCG module is functionally identical with a standard PC/AT.

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.1.1 LPC Bus

On the conga-TCG, the PCI Express Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Express Bus. Only specified I/O ranges are forwarded to the LPC Bus. In the congatec Embedded BIOS, the following I/O address ranges are sent to the LPC Bus:

2Eh-2Fh	4Eh-4Fh	60h, 64h
220h-227h	228h-22Fh	230h-233h
238h-23Fh	240h-253h	260h-273h
278h-27Fh	280h-293h	2E8h-2EFh
2F8h-2FFh	338h-33Fh	378h-37Fh
3BCh-3BFh	3E8h-3EFh	3F8h-3FFh
678h-67Fh	778h-77Fh	7BCh-7BFh
A00h-BFFh	E00h-FFFh	

Some of these ranges are not available for customer use if a Super I/O is present and enabled on the carrier board or on the module. The I/O range E38h to EBFh is always used by on module LPC devices.

If you need additional LPC Bus resources or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 37 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Root Complex
00h	01h	00h	Internal	Integrated Graphics Controller (VGA)
00h	01h	01h	Internal	TMDS / DisplayPort HDA Controller (for TMDS/DisplayPort integrated audio only)
00h	02h	00h	N.A.	Host Bridge
00h (see Note 1)	02h	01h	Internal	PCIExpress Root Bridge 0
00h (see Note 1)	02h	02h	Internal	PCIExpress Root Bridge 1
00h (see Note 1)	02h	03h	Internal	PCIExpress Root Bridge 2
00h (see Note 1)	02h	04h	Internal	PCIExpress Root Bridge 3
00h (see Note 1)	02h	05h	Internal	PCIExpress Root Bridge 4
00h	10h	00h	Internal	XHCI Host Controller
00h	11h	00h	Internal	Serial ATA Controller
00h	12h	00h	Internal	OHCI Host Controller 0
00h	12h	02h	Internal	EHCI Host Controller 0
00h	13h	00h	Internal	OHCI Host Controller 1
00h	13h	02h	Internal	EHCI Host Controller 1
00h	14h	00h	N.A.	SMBus Host Controller
00h	14h	02h	Internal	High Definition Audio Controller
00h	14h	03h	N.A.	PCI to LPC Bridge
00h	14h	07h	Internal	SD Controller
00h	16h	00h	Internal	OHCI Host Controller 2
00h	16h	02h	Internal	EHCI Host Controller 2
00h	18h	00h	N.A.	Chipset Configuration Registers
00h	18h	01h	N.A.	Chipset Configuration Registers
00h	18h	02h	N.A.	Chipset Configuration Registers
00h	18h	03h	N.A.	Chipset Configuration Registers
00h	18h	04h	N.A.	Chipset Configuration Registers
00h	18h	05h	N.A.	Chipset Configuration Registers
01h (see Note 2)	00h	00h	Internal	Onboard Gigabit LAN Controller
02h (see Note 2)	00h	00h	Internal	PCI Express Port 0
03h (see Note 2)	00h	00h	Internal	PCI Express Port 1
04h (see Note 2)	00h	00h	Internal	PCI Express Port 2
05h (see Note 2)	00h	00h	Internal	PCI Express Port 3

Note

1. *The PCI Express ports are visible only if the PCI Express port is set to "Enabled" in the BIOS setup program and a device is attached to the corresponding PCI Express port on the carrier board.*

2. *The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

9.3 PCI Interrupt Routing Map

Table 38 PCI Interrupt Routing Map

PIRQ	VGA	HDA (TMDS/DP)	XHCI0	OHCI0	EHCI 0	OHCI1	EHCI 1	OHCI2	EHCI 2	SM Bus	SATA (IDE)	HDA (Main)
A												20
B					17		17		17			
C			18	18		18		18				
D											19	
E	44											
F		45										
G												
H												

PIRQ	PCI-EX Root Bridge 0	PCI-EX Root Bridge 1	PCI-EX Root Bridge 2	PCI-EX Root Bridge 3	PCI-EX Root Bridge 4	LAN	PCI-EX Port 0	PCI-EX Port 1	PCI-EX Port 2	PCI-EX Port 3
A	24		32		40	24		32		40
B								33		41
C								34		42
D								35		43
E		28		36			28		36	
F							29		37	
G							30		38	
H							31		39	

Note

The given numbers specify the APIC interrupt numbers assigned to the respective devices.

9.4 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.5 SM Bus

System Management (SM) bus signals are connected to the AMD Chipset and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

10 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

10.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

10.1.1 Boot Selection Popup

Press the <F11> key during POST to access the Boot Selection Popup menu. A selection menu displays immediately after POST, allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

10.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar, left frame and right frame. The menu bar is shown below:

Main	Advanced	Chipset	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← →Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

10.3 Main Setup Screen

When you enter the BIOS setup, you will see the Main setup screen. The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time. You can always return to the Main setup screen by selecting the Main tab.

Feature	Options	Description
Main BIOS Version	no option	Displays the main BIOS version.
OEM BIOS Version	no option	Displays the additional OEM BIOS version.
Build Date	no option	Displays the date the BIOS was built
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
Running Time	no option	Displays the time the board is running [in hours max. 65535].
Memory Information	no option	
Total Memory	no option	Displays the total amount of installed memory.
System Date	Day of week, month/ day/year	Specifies the current system date. Note: The date is in month-day-year format.
System Time	Hour:Minute:Second	Specifies the current system time. Note: The time is in 24-hour format.

10.4 Advanced Setup

Select the advanced tab from the setup menu to enter the advanced BIOS setup screen. The menu is used for setting advanced features and only features described within this user's guide are listed.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Graphics				
	Watchdog				
	Hardware Health Monitoring				
	Module Serial Ports				
	PCI & PCI Express				
	RTC Wake				
	ACPI				
	Trusted Computing				
	CPU				
	SATA				
	SDIO				
	USB				
	SMART Settings				
	Super IO				
	Serial Port Console Redirection				
	UEFI Network Stack				
	Intel® I210 Gigabit Network Connection				
	PC Speaker Configuration				

10.4.1 Graphics Submenu

Feature	Options	Description
Primary Graphics Device	IGD **PCI/PCIe**	Select primary graphics adapter to be used during boot up. IGD: Internal Graphics Device PCI/PCIe: Try to use external PCI Express or PCI Graphics Device. If not present, IGD is used.
Integrated Graphics Device	**Auto** Disabled Manual Configuration	Deactivate IGD or select framebuffer configuration mode. In auto mode, the framebuffer size will be defined based on the amount of physical memory present.

Feature	Options	Description
IGD Framebuffer Size	32M 64M 128M **256M** 512M 1G	Only visible if IGD is set to manual configuration. Set fixed graphics framebuffer size for IGD. The graphics driver might allocate additional memory.
CRT Interface	Disabled **Enabled**	Enable or disable the CRT interface.
Digital Display Interface	Disabled **Auto Selection**	Configure the digital display interface. Display Port or HDMI/DVI is supported and automatically detected and configured.
LFP Interface	Disabled **Enabled**	Enable or disable the local flat panel (LFP) interface.
Always Try Auto Panel Detect	No **Yes**	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel . Only if no external EDID data set can be found, the data set selected under 'Local Flat Panel Type' will be used as fallback data set.
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x800 1x18 (01Eh) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.
Backlight Inverter Type	**None** PWM I2C	Select the type of backlight inverter used. PWM = Use module PWM output signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.
PWM Inverter Frequency (Hz)	**200**-40000	Only visible if Backlight Inverter Type is set to PWM. Set the PWM inverter frequency in Hertz.

Feature	Options	Description
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%**	Actual backlight value in percent of the maximum setting.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Setting	**No** Yes	Allow to invert backlight control values if required for the actual I2C type backlight hardware controller.
LVDS SSC	**Disabled**, 0.5%, 1.0%, 1.5%, 2.0%, 2.5%	Configure LVDS spread spectrum clock modulation depth. Using center spreading and a fixed modulation frequency of 32.9kHz

10.4.2 Watchdog Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog For User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One-time Trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to 'One-time Trigger' the watchdog will be disabled after the first trigger. If set to 'Single Event', every stage will be executed only once, then the watchdog will be disabled. If set to 'Repeated Event' the last stage will be executed repeatedly until a reset occurs.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.

Feature	Options	Description
Event 1	ACPI Event **Reset** Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event see note below.
Event 2	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

In ACPI mode, it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

10.4.3 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	no option	Displays the actual module CPU temperature in °C.
Board Temperature	no option	Displays the actual module board temperature in °C.
12V Standard	no option	Displays the actual voltage of the 12V standard power supply.
5V Standby	no option	Displays the actual voltage of the 5V standby power supply.
Input Current (12V Standard)	no option	Displays the module input current from 12V standard voltage.
CPU Fan Speed	no option	Displays the actual CPU Fan Speed in RPM.
Fan PWM Frequency Mode	Low Frequency, **High Frequency**	Select fan PWM base frequency mode. Low frequency: 11.0Hz-88.2Hz High frequency: 1kHz-63kHz
Fan PWM Frequency	11.0 Hz, 14.7 Hz, 22.1 Hz, 29.4 Hz, **35.3 Hz**, 44.1 Hz, 58.8 Hz, 88.2 Hz	Select fan PWM base frequency (11.0Hz-88.2Hz). (Only visible in low frequency mode)
Fan PWM Frequency (kHz)	1-63 default: **31**	Select fan PWM base frequency (1kHz-63kHz). (Only visible in high frequency mode)
Fan Speed Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%**	Boot up fan speed in percent of the maximum supported speed.

10.4.4 Module Serial Ports

Feature	Options	Description
Serial Port 0	**Disabled** Enabled	Enable or disable module serial port 0.
I/O Base Address	3F8h, 2F8h, 220h, 228h, 238h, 2E8h, 338h, **3E8h**	Set serial port base address.
Interrupt	None, IRQ3, IRQ4, IRQ5, IRQ6, **IRQ10**, IRQ11, IRQ14, IRQ15	Set serial port interrupt.
PNP ID	None PNP0501 **CGT0501**	Set serial port ACPI ID.

Feature	Options	Description
Baudrate	**2400**, 4800, 9600, 19200, 38400, 57600, 115200	Set serial port initial baudrate.
Serial Port 1	**Disabled** Enabled	Enable or disable module serial port 1.
I/O Base Address	3F8h, 2F8h, 220h, 228h, 238h, **2E8h**, 338h, 3E8h	Set serial port base address.
Interrupt	None, IRQ3, IRQ4, IRQ5, IRQ6, IRQ10, **IRQ11**, IRQ14, IRQ15	Set serial port interrupt.
PNP ID	None PNP0501 CGT0501 **CGT0502**	Set serial port ACPI ID.
Baudrate	**2400**, 4800, 9600, 19200, 38400, 57600, 115200	Set serial port initial baudrate.

10.4.5 PCI & PCI Express Submenu

Feature	Options	Description
PCI Settings		
PCI Latency Timer	**32**, 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate PERR#.
SERR# Generation	Disabled Enabled	Enable or disable PCI device to generate SERR#.
Generate EXCD0/1_PERST#	Disabled 1ms 5ms **10ms** 50ms 100ms 150ms 200ms 250ms	Select whether and how long the COM Express EXCD0_PERST# and EXCD1_PERST# pins should be driven low during POST.
» PCI Express Settings	submenu	PCI Express device and link settings.

Feature	Options	Description
» PCI Express Port Configuration	submenu	Configure PCI Express and PEG ports.
» PIRQ Routing & IRQ Reservation	submenu	Manual PIRQ routing and interrupt reservation for legacy devices.

10.4.5.1 PCI Express Settings Submenu

Feature	Options	Description
Relaxed Ordering	**Disabled** Enabled	Enable or disable PCI Express device relaxed ordering.
Extended Tag	**Disabled** Enabled	If enabled a device may use an 8-bit tag filed as a requester.
No Snoop	Disabled **Enabled**	Enable or disable PCI Express device 'No Snoop' option.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum payload of PCI Express devices or allow system BIOS to select the value.
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum read request size of PCI Express devices or allow system BIOS to select the value.
Extended Synch	**Disabled** Enabled	If enabled, the generation of extended PCI Express synchronization patterns is allowed.
Link Training Retry	Disabled 2 3 **5**	Defines numer of retry attempts software will take to retrain the link if the previous training attempt was unsuccessful.
Link Training Timeout (us)	10-10000 (**100**)	Defines number of microseconds software will wait before polling the link training bit in the link status register. Value ranges from 10us to 10000us.
Restore PCIE Registers	Enabled **Disabled**	On non-PCI Express aware operating systems some devices may not be re-initialized correctly after S3. Setting this node to Enabled restores PCI Express configuration on S3 resume. Warning: Enabling this may cause issues with other hardware after S3 resume.

Feature	Options	Description
PSPP Policy	Disabled **Performance** Balanced-High Balanced-Low Power Saving	Define PCI Express link speed selection policy.

10.4.5.2 PCI Express Port Configuration Submenu

Feature	Options	Description
Onboard LAN Controller	Disabled **Enabled**	Enable or disable the on module Ethernet controller.
PCI Express Port 0	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the 'Always Enable Port' support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
ASPM Support	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Configure PCI Express root port ASPM support.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 1	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the 'Always Enable Port' support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
ASPM Support	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Configure PCI Express root port ASPM support.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 2	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the 'Always Enable Port' support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
ASPM Support	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Configure PCI Express root port ASPM support.

Feature	Options	Description
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 3	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the 'Always Enable Port' support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
ASPM Support	**Disabled** L0s Entry L1 Entry L0s And L1 Entry	Configure PCI Express root port ASPM support.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.

10.4.5.3 PIRQ Routing & IRQ Reservation Submenu

Feature	Options	Description
PIRQA	**Auto**, IRQ3, IRQ4, IRQ10, IRQ11, IRQ14, IRQ15	Set interrupt for selected PIRQ. Please refer to the board's resource list for a detailed list of devices connected to the respective PIRQ. NOTE: These settings will only be effective while operating in PIC (non-IOAPIC) interrupt mode.
PIRQB	same as PIRQA	same as PIRQA
PIRQC	same as PIRQA	same as PIRQA
PIRQD	same as PIRQA	same as PIRQA
PIRQE	same as PIRQA	same as PIRQA
PIRQF	same as PIRQA	same as PIRQA
PIRQG	same as PIRQA	same as PIRQA
PIRQH	same as PIRQA	same as PIRQA
Reserve Legacy Interrupt 1	**None**, IRQ3, IRQ4, IRQ10, IRQ11, IRQ14, IRQ15	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.
Reserve Legacy Interrupt 2	same as Reserve Legacy Interrupt 1	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.

10.4.6 RTC Wake Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour		Specify wake up hour.
Wake up minute		Specify wake up minute.
Wake up second		Specify wake up second.

10.4.7 ACPI Submenu

Feature	Options	Description
Enable Hibernation	Disabled **Enabled**	Enable or disable system ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend.
Critical Trip Point	**Disabled**, 70, 80, 90, 95, 100, 105, 110, 115°C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Active Trip Point	**Disabled**, 20, 30, 40, 50, 60, 70, 80, 90, 95°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Trip Point	Disabled, 60, 70, 80, 90, 95°C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.
Lid Support	**Disabled** Enabled	Configure COM Express LID# signal to act as ACPI lid.
Sleep Button Support	**Disabled** Enabled	Configure COM Express SLEEP# signal to act as ACPI sleep button.

10.4.8 Trusted Computing Submenu

Feature	Options	Description
Security Device Support	**Disable** Enable	Enable or disable BIOS support for security device.
TPM State	**Disabled** Enabled	Enable or disable TPM chip. Note: System might restart several times during POST to acquire target state.

Feature	Options	Description
Pending operation	**None**, Enable Take Ownership, Disable Take Ownership, TPM Clear	Perform selected TPM chip operation. Note: System might restart several times during POST to perform selected operation.

10.4.9 CPU Submenu

Feature	Options	Description
AMD PowerNow! Support	Disabled **Enabled**	Enable or disable support for AMD PowerNow! technology. Allows operating systems to control CPU performance states.
Maximum Power Up P-State	**P-State 0** P-State 1 P-State 2 P-State 3 P-State 4 P-State 5 P-State 6 P-State 7	Select the maximum CPU performance state to be set at power up. Higher numbers mean lower performance. P-state 0 is the highest performance state.
Maximum OS P-State	**P-State 0** P-State 1 P-State 2 P-State 3 P-State 4 P-State 5 P-State 6 P-State 7	Select the maximum CPU performance state the operating system should support. Higher numbers mean lower performance. P-state 0 is the highest performance state.
NX Mode	Disabled **Enabled**	Enable or disable the 'no-execute' page protection function.
Virtualization Technology	Disabled **Enabled**	When enabled, a Virtual Machine Manager (VMM) can utilize the integrated hardware virtualization support.
C6 Support	**Disabled** Enabled	Enable or disable CPU C6 low power state support.
Core Performance Boost	Auto **Disabled**	Control usage of boosted P-States, i.e. P-States above the standard CPU P-State limit. Availability depends on CPU revision and type, actual usage on total CPU/GPU chip power consumption.
Core Leveling Support	**Automatic Mode**, Three cores per processor, Two cores per processor, One core per processor	Change/limit the number of active CPU cores.

10.4.10 SATA Submenu

Feature	Options	Description
SATA Controller	Disabled **Enabled**	Enable or disable the onboard SATA controller.
SATA Mode Selection	Native IDE **AHCI** Legacy IDE AHCI as ID 7804	Select onboard SATA controller mode.
SATA Gen2 Limit	**Disabled** Enabled	Limit all SATA ports to max. Gen2 speed.
SATA Port 0	**Enabled** Disabled	Enable or disable selected port.
Port Speed	**Auto** Gen1 Gen2	Select max. SATA speed generation for the selected port. Auto = up to Gen3
eSATA Support	**Disabled** Enabled	Enabled or disable eSATA and hotplug (only in AHCI mode) support.
SATA Port 1	**Enabled** Disabled	Enable or disable selected port.
Port Speed	**Auto** Gen1 Gen2	Select max. SATA speed generation for the selected port. Auto = up to Gen3
eSATA Support	**Disabled** Enabled	Enabled or disable eSATA and hotplug (only in AHCI mode) support.
SATA Port 0	no option	SATA drive 0 information.
SATA Port 1	no option	SATA drive 1 information.

10.4.11 SDIO Submenu

Feature	Options	Description
SDIO Access Mode	**Auto** DMA PIO	Select BIOS SD device access and boot mode. Auto = Access SD device in DMA mode if controller supports it, otherwise use PIO mode. DMA = Access SD device in DMA mode. PIO = Access SD device in PIO mode.
» SD Controller	submenu	Configure SD controller

10.4.11.1 SD Controller Submenu

Feature	Options	Description
SD Controller Mode	**Disabled**, Advanced DMA, DMA, PIO	Enable or disable the onboard SD controller and select its operating mode.
SD Clock Control	**50MHz/25MHz** 40MHz/20MHz 25MHz/12.5MHz	Select actual SD clocks for high and low speed transfer modes.
SD Speed Mode	Low Speed **High Speed**	Select SD transfer speed mode.
SD System Address Support	32Bit **64Bit**	Select 32bit or 64bit system address support for SD controller.
SD Host Controller Version	**SD 2.0** SD 3.0	Select SD host controller version.

10.4.12 USB Submenu

Feature	Options	Description
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
External USB Controller Support	Disabled **Enabled**	Enable or disable BIOS support for external USB controllers.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI OS driver.
EHCI Hand-off	**Disabled** Enabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable or disable USB mass storage BIOS support.
USB Transfer Timeout	1 sec 5sec 10 sec **20 sec**	Timeout value for legacy USB control, bulk and interrupt transfers.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device start unit command timeout.
Device Power-Up Delay Selection	**Auto** Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.

Feature	Options	Description
Device Power-Up Delay Value	**5** 1-40	Actual power-up delay value in seconds.
USB Mass Storage Device Name (Auto detected USB mass storage devices are listed here dynamically)	**Auto** Floppy Forced FDD Hard Disk CD-ROM	Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly. Select AUTO to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. Forced FDD allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. Hard Disk allows the device to be emulated as hard disk. CDROM assumes the CD.ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.
» USB Port & Controller Configuration	submenu	Configure USB ports and controllers.

10.4.12.1 USB Port & Controller Configuration Submenu

Feature	Options	Description
XHCI 0 (Port 0-1)	Disabled **Enabled**	Enable or disable the XHCI (USB 3.0) host controller.
EHCI 0 (Port 2-5)	Disabled **Enabled**	Enable or disable the EHCI (USB 2.0) host controller.
EHCI 1 (Port 6-7)	Disabled **Enabled**	Enable or disable the EHCI (USB 2.0) host controller.
EHCI 2 (Port 0-1)	Disabled **Enabled**	Enable or disable the EHCI (USB 2.0) host controller. Only visible if XHCI 0 is set to 'Disabled'
USB Port 0 (XHCI Mode) (USB Port 0)	Disabled **Enabled**	Enable or disable the respective USB port. Alternative port control if XHCI controller is disabled.
USB Port 1 (XHCI Mode) (USB Port 1)	Disabled **Enabled**	Enable or disable the respective USB port. Alternative port control if XHCI controller is disabled.
USB Port 2	Disabled **Enabled**	Enable or disable the respective USB port.
USB Port 3	Disabled **Enabled**	Enable or disable the respective USB port.
USB Port 4	Disabled **Enabled**	Enable or disable the respective USB port.
USB Port 5	Disabled **Enabled**	Enable or disable the respective USB port.

Feature	Options	Description
USB Port 6	Disabled **Enabled**	Enable or disable the respective USB port.
USB Port 7	Disabled **Enabled**	Enable or disable the respective USB port.
Overcurrent Protection	**Disabled** Enabled	Overcurrent protection on all USB ports.

10.4.13 SMART Settings Submenu

Feature	Options	Description
SMART Self Test	**Disabled** Enabled	Run SMART Self Test on all harddisks during POST.

10.4.14 Super I/O Submenu

Feature	Options	Description
SIO Clock	**24MHz** 48MHz	Select Super I/O base clock.
PS/2 Keyboard/Mouse Support	**Disabled** Enabled	Enable or disable PS/2 Keyboard/Mouse controller support.
Serial Port 0	Disabled **Enabled**	Enable or disable serial port 0.
Device Settings	IO=3F8h; IRQ=4;	Fixed configuration of serial port 0 if enabled.
Serial Port 1	Disabled **Enabled**	Enable or disable serial port 1.
Device Settings	IO=2F8h; IRQ=3;	Fixed configuration of serial port 1 if enabled.
Parallel Port	**Disabled** Enabled	Enable or disable parallel port.
Device Settings	IO=378h; IRQ=7;	Fixed configuration of the parallel port if enabled.
Device Mode	**Standard Parallel Mode** EPP Mode ECP Mode EPP Mode & ECP Mode	Set the parallel port mode.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

10.4.15 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
» Console Redirection Settings	submenu	Opens console redirection configuration sub menu.
COM1 Console Redirection	**Disabled** Enabled	Enable or disable serial port 1 console redirection.
» Console Redirection Settings	submenu	Opens console redirection configuration sub menu.

10.4.15.1 Console Redirection Settings Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.
Baudrate	9600, 19200, 38400, 57600, **115200**	Select baud rate.
Data Bits	7, **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.

Feature	Options	Description
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Enabled** Disabled	Select whether serial redirection should be continued after POST.

10.4.16 UEFI Network Stack Submenu

Feature	Options	Description
UEFI Network Stack	Disabled Enabled	Enable or disable the UEFI network stack.
IPv4 PXE Support	Disabled Enabled	Enable IPv4 PXE boot support. If disabled IPv4 PXE boot option will not be created.
IPv6 PXE Support	Disabled Enabled	Enable IPv6 PXE boot support. If disabled IPv6 PXE boot option will not be created.
PXE Boot Wait Time	**1** 0 - 5	Time in seconds waiting for ESC keypress to abort the PXE boot.

10.4.17 Intel® I210 Gigabit Network Connection Submenu

Feature	Options	Description
» NIC Configuration	submenu	Opens the NIC Configuration submenu.
Blink LEDs	0-15 Default : 0	The Ethernet activity LEDs will blink as many seconds as entered.
UEFI Driver	no option	Displays the UEFI Driver version.
Adapter PBA	no option	Displays the Adapter PBA.
Chip Type	no option	Displays the type of Ethernet chip.
PCI Device ID	no option	Displays the PCI Device ID of the Ethernet controller.
Bus:Device:Function	no option	Displays the PCI Bus:Device:Function number of the Ethernet controller.
Link Status	no option	Displays the Link Status.
MAC Address	no option	Displays the MAC Address.
Virtual MAC Address	no option	Displays the programmatically assignable MAC Address.

10.4.18 NIC Configuration Submenu

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake On LAN	Disabled **Enabled**	Enables the server to be powered on using an in-band magic packet.

10.4.19 PC Speaker Configuration Submenu

Feature	Options	Description
Debug Beeps	Disabled **Enabled**	Enable or disable general debug / status beep generation.
Input Device Debug Beeps	**Disabled** Enabled	Enable or disable input device debug beeps.
Output Device Debug Beeps	**Disabled** Enabled	Enable or disable output device debug beeps.
USB Driver Beeps	**Disabled** Enabled	Enable or disable USB driver beeps.

10.5 Chipset Setup

Select the Chipset tab from the setup menu to enter the Chipset setup screen.

10.5.1 Chipset Settings Configuration

Feature	Options	Description
HDMI/DP Audio Support	Disabled **Enabled**	Enable or disable HDMI/DisplayPort integrated audio support.
HDA Controller	**Auto** Disabled Enabled	Control activation of the High Definition Audio controller device. Disabled = HDA controller will be unconditionally disabled Enabled = HDA controller will be unconditionally enabled Auto = HDA controller will be enabled if HDA codec present, disabled otherwise.

Feature	Options	Description
Isolate SMBus Segments	Never During POST **Always**	Allows to isolate the off-module/external SMBus segment from the on-module SMBus segment. This can be a workaround for non specification conform external SMBus devices.
Adaptive S4 Control	**Disabled** Enabled	E.nable or disable adaptive S4 control
SB Clock Spread Spectrum	Disabled **Enabled**	Enable or disable clock spreading for I/O components like USB (3.0) and SATA.
SB Clock Spread Spectrum Option	-0.362%, **-0.375%**, -0.400%, -0.425%, -0,450%, -0.475%	I/O clock spreading value.
Native PCI Express Support	Disabled **Enabled**	Enable or disable native PCI Express OS support.
USB MSI Option	**Disabled** Enabled	Enable or disable MSI (Message Signaled Interrupt) support for USB controllers.
HD Audio MSI Option	**Disabled** Enabled	Enable or disable MSI (Message Signaled Interrupt) support for the HDA controller.
LPC MSI Option	**Disabled** Enabled	Enable or disable MSI (Message Signaled Interrupt) support for the LPC bridge.
PCIBridge MSI Option	**Disabled** Enabled	Enable or disable MSI (Message Signaled Interrupt) support for PCI/ PCIe bridges.
» Memory Configuration	Submenu	Opens the Memory Configuration submenu.

10.5.1.1 Memory Configuration Submenu

Feature	Options	Description
Memory Bus Clock	**Auto** 400MHz (DDR3-800) 533MHz (DDR3-1066) 667MHz (DDR3-1333) 800MHz (DDR3-1600)	Select or limit memory frequency.
Memory Hole Remapping	Disabled **Enabled**	Enable or disable memory hole remapping.
Bank Interleaving	**Disabled** Enabled	Enable or disable memory bank interleaving.
Memory Hole 15MB-16MB	**Disabled** Enabled	Create a memory hole in the range between 15MB and 16MB for some LPC/ISA expansion cards.

10.6 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.6.1 Boot Settings Configuration

Feature	Options	Description
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. Note: The default OEM logo is a dark screen.
Setup Prompt Timeout	**1** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot (not recommended), 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. Note: Only works with an ATX type power supply.
AT Shutdown Mode	System Reboot **Hot S5**	Determines the behavior of an AT-powered system after a shutdown.
Battery Support	Auto (Battery Manager), Battery-Only On I2C Bus, Battery-Only On SMBus	Battery system support selection. Select ' Battery-Only On I2C Bus' for battery-only systems using I2C bus and ' Battery-Only On SMBus' for battery-only systems using SMBus. Select 'Auto' for systems equipped with a real battery system manager (connected via I2C or SMBus).
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Option Sorting Method	UEFI First **Legacy First**	Set boot option sorting method. UEFI First: Tries all UEFI boot options before first legacy boot option. Legacy First: Tires all legacy boot options before first UEFI boot option.
Bootloader Type Priority	UEFI First **Legacy First**	Set the bootloader type that will be tried first. UEFI First: UEFI booloaders will be tried first. Legacy First: Legacy bootable devices will be tried first.

Feature	Options	Description
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if "UEFI Standard" priority list control is selected. If "Type Based" priority list control is enabled only 8 boot devices can be prioritized.)	Disabled SATA 0 Drive SATA 1 Drive USB Harddisk USB CDROM Other USB Device Onboard SD Card Storage Onboard LAN External LAN Firmware-based UEFI Bootloader Other Device	This view is only available when in the default "Type Based" mode. When in "UEFI Standard" mode, you will only see the devices that are currently connected to the system.
» CSM & Option ROM Control	submenu	Opens submenu which controls the execution of UEFI and legacy option ROMs.

UEFI Fast Boot	**Disabled** Enabled	Enable or disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS / legacy boot options.
SATA Support	**Last Boot HDD Only** All SATA Devices	Select which SATA device to be initialized in fast boot mode.
VGA Support	Auto **UEFI Driver**	If set to Auto, the legacy video option ROM will be installed for legacy OS boot; boot logo will NOT be shown during POST. For UEFI OS boot the UEFI GOP driver will be installed.
USB Support	Disabled **Full Init** Partial Init	If set to Disabled, no USB device will be available before OS boot. If set to Partial Init, specific USB ports/devices will NOT be available before OS boot. If set to Enabled, all USB devices will be available during POST and after OS boot.
PS/2 Device Support	Disabled **Enabled**	If set to Disabled, PS/2 devices will be skipped.
Network Stack Driver Support	**Disabled** Enabled	If set to Disabled, the UEFI network stack driver installation will be skipped.

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

10.6.1.1 CSM & Option ROM Control Submenu

Feature	Options	Description
Launch CSM	**Enabled** Disabled	Controls the execution of the CSM module. Only disable for pure UEFI operating system support.
Boot Option Filter	**UEFI and Legacy** Legacy Only UEFI Only	Controls which devices / boot loaders the system should boot to.
PXE Option ROM Launch Policy	**Do Not Launch** UEFI ROM Only Legacy ROM Only	Controls the execution of UEFI and legacy PXE option ROMs
Storage Option ROM Launch Policy	**Do Not Launch** UEFI ROM Only Legacy ROM Only	Controls the execution of UEFI and legacy mass storage device option ROMs
Video Option ROM Launch Policy	Do Not Launch UEFI ROM Only **Legacy ROM Only**	Controls the execution of UEFI and legacy video option ROMs
Other Option ROM Launch Policy	**UEFI ROM Only** Legacy ROM Only	Controls the execution of option ROMs for PCI / PCI Express devices other than network, mass storage or video.
GateA20 Active	**Upon Request** Always	Gate A20 control. Upon Request: Gate A20 can be disabled using BIOS services. Always: Do not allow disabling Gate A20 This option is useful when any runtime code is executed above 1MB.
Option ROM Messages	**Force BIOS** Keep Current	Set display mode for option ROMs.
INT19 Trap Response	**Immediate** Postponed	BIOS reaction on INT19 trapping by Option ROM Immediate: Execute the trap right away. Postponed: Execute the trap during legacy boot.

10.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

10.7.1 Security Settings

Feature	Options	Description
BIOS Password	enter password	Specifies the BIOS and setup administrator password.
BIOS Update & Write Protection	**Disabled** Enabled	Congatec flash software will require BIOS password to perform write or erase operations.
HDD Security Configuration		

Feature	Options	Description
List of all detected hard disks supporting the security feature set	Select device to open device security configuration submenu	
» Secure Boot Menu	submenu	

10.7.1.1 BIOS Security Features

BIOS Password/ BIOS Write Protection

A BIOS password protects the BIOS setup program from unauthorized access. This ensures that end users cannot change the system configuration without authorization. With an assigned BIOS password, the BIOS prompts the user for a password on a setup entry. If the password entered is wrong, the BIOS setup program will not launch.

The congatec BIOS uses a SHA256 based encryption for the password, which is more secured than the original AMI encryption. The BIOS password is case sensitive with a minimum of 3 characters and a maximum of 20 characters. Once a BIOS password has been assigned, the BIOS activates the grayed out 'BIOS Update and Write Protection' option. If this option is set to 'enabled', only authorized users (users with the correct password) can update the BIOS. To update the BIOS, use the congatec system utility cgutlcmd.exe with the following syntax:

```
CGUTLCMD BFLASH <BIOS file> /BP: <password> where <password> is the assigned BIOS password.
```

For more information about "Updating the BIOS" refer to the congatec system utility user's guide, which is called CGUTLm1x.pdf and can be found on the congatec GmbH website at www.congatec.com.

With the BIOS password protection and the BIOS update and write protection, the system configuration is completely secured. If the BIOS is password protected, you cannot change the configuration of an end application without the correct password.

Note

Use cgutlcmd.exe version 1.5.3 or later.

Built in BIOS recovery is disabled in the congatec BIOS firmware to prevent the BIOS from updating itself due to the user pressing a special key combination or a corrupt BIOS being detected. congatec considers such a recovery update a security risk because the BIOS internal update process bypasses the implemented BIOS security explained above.

Only the congatec utility interface to the SMI handler of the BIOS flash update is enabled. Other interfaces to the SMI handler are disabled to prevent non congatec tools from writing to the BIOS flash. As a result of this restriction, flash utilities supplied by AMI or Intel will not work .

UEFI Secure Boot

Secure Boot is a security standard defined in UEFI specification 2.3.1 that helps prevent malicious software applications and unauthorized operating systems from loading during system start up process. Without secure boot enabled (not supported or disabled), the computer simply hands over control to the bootloader without checking whether it is a trusted operating system or malware. With secure boot supported and enabled, the UEFI firmware starts the bootloader only if the bootloader's signature has maintained integrity and also if one of the following conditions is true:

- The bootloader was signed by a trusted authority that is registered in the UEFI database.
- The user has added the bootloader's digital signature to the UEFI database. The BIOS provides the key management setup sub-menu for this purpose.

Note

The congatec BIOS by default enables CSM (Compatibility Support Module) and disables secure boot because most of the industrial computers today boot in legacy (non-UEFI) mode. Since secure boot is only enabled when booting in native UEFI mode, you must therefore disable the CSM (compatibility support module) in the BIOS setup to enable Secure Boot.

A full description of secure boot is beyond the scope of this users guide. For more information about how secure boot leverages signature databases and keys, see the secure boot overview in the windows deployment options section of the Microsoft TechNet Library at http://technet.microsoft.com.

10.7.1.2 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to 'lock' and 'unlock' drives using the security password. A 'locked' drive will be detected by the system, but no data can be accessed. Accessing data on a 'locked' drive requires the proper password to 'unlock' the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within four attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

To ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

Note

If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

10.8 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen. You can display a Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
Boot Override	
List of all boot devices currently detected	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to “Device Based”.

11 Additional BIOS Features

The BIOS setup description of the conga-TCG can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative

11.1 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS is identified as TFT3R1xx or TFT4R1xx where:

- TFT3 / TFT4 is the project code
- R is the identifier for a BIOS ROM file
- 1 is the so called feature number
- xx is the major and minor revision number

The conga-TCG BIOS binary size is 8 MB.

11.2 Updating the BIOS

BIOS updates are recommeded to correct platform issues or enhance the feature set of the module. The conga-TCG features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line [1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

11.3 Supported Flash Devices

The conga-TCG supports the following flash devices:

- Winbond W25Q64JVSSIQ (8 MB)

The flash device listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.