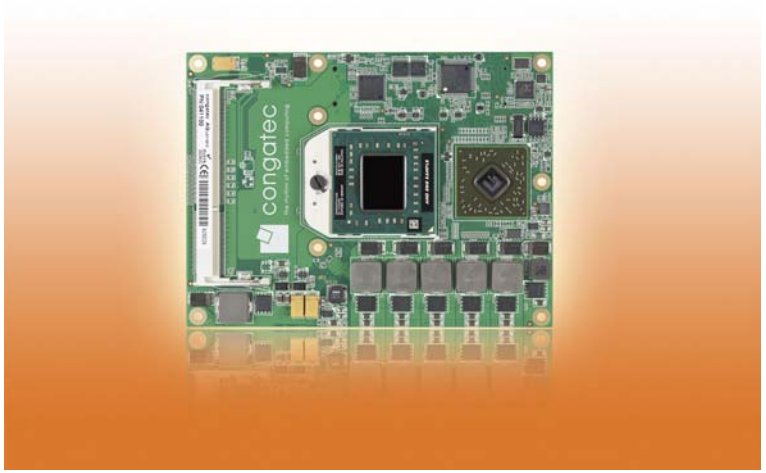

COM Express™ conga-TFS

AMD Embedded R-Series Processor with A70M Controller Hub

User's Guide

Revision 0.2 (Preliminary)

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2013.03.06	AEM	• Preliminary release
0.2	2013.05.16	AEM	• Added section 5 “Onboard Temperature Sensor”. • Replaced “FCH” with “Controller Hub” in the whole manual. • Updated section 11 “BIOS Setup Description”.

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-TFS. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide
COM Express™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

Disclaimer

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Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
KHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
T.O.M.	Top of memory = max. DRAM installed
HDA	High Definition Audio
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

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Contents

List of Tables

1 Introduction

COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). It's creation provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available today. COM Express™ modules are available in following form factors:

- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x 110mm

The COM Express™ specification 2.0 defines seven different pinout types.

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports
Type 1	A-B	Up to 6			1
Type 2	A-B C-D	Up to 22	32 bit	1	1
Type 3	A-B C-D	Up to 22	32 bit		3
Type 4	A-B C-D	Up to 32		1	1
Type 5	A-B C-D	Up to 32			3
Type 6	A-B C-D	Up to 24			1
Type 10	A-B	Up to 4			1

conga-TFS modules utilize the Type 6 pinout definition and are COM Express 2.1 Compliant. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are a legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 6 pinout provides the ability to offer PCI Express, Serial ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

conga-TFS Options Information

The conga-TFS is available in three variants. This user's guide describes these variants. The table below shows the different configurations available. Check the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

conga-TFS

Part-No.	041101	041102	041103
Processor	AMD Embedded R-464L 2.3/3.2 GHz Quad Core™	AMD Embedded R-460H 1.9/2.8 GHz Quad Core™	AMD Embedded R-272F 2.7/3.2 GHz Dual Core™
L2 Cache	2x2 MByte	2x2 MByte	1 MByte
PEG	Yes	Yes	Yes
SDVO	No	No	No
DisplayPort (DP)	Yes	Yes	Yes
HDMI/DVI	Yes	Yes	Yes
Processor TDP	35 W	35 W	35 W

2 Specifications

2.1 Feature List

Table 1 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 6 (Basic size 95 x 125mm). Compliant with COM Express 2.1 specification.
Processor	AMD Embedded R-464L 2.3/3.2 GHz (Nominal/Boost) Quad Core with 2x2-MByte L2Cache AMD Embedded R-460H 1.9/2.8 GHz (Nominal/Boost) Quad Core with 2x2-MByte L2 Cache AMD Embedded R-272F 2.7/3.2 GHz (Nominal/Boost) Dual Core with 1-MByte L2 Cache
Memory	2 sockets: SO-DIMM DDR3 up to 1600MT/s. Supports up to 16GB with two 8GB SO-DIMM modules. Sockets located top and bottom side of module.
Chipset	AMD A70M Controller Hub.
Audio	HDA (High Definition Audio)/digital audio interface with support for multiple codecs
Ethernet	Gigabit Ethernet: Realtek RTL8111GN Gbit Ethernet Lan Controller.
Graphics Options	AMD Radeon HD 7000G Series Graphics, Video Compressing Engine 1.0, dedicated hardware video decoder (UVD 3.2), OpenGL 4.2, OpenCL™ 1.1 and DirectX®11 support. conga-TFS supports up to three independent displays.

	• CRT Interface with resolutions up to 1920x1200 @ 60Hz. Supports auto monitor detection and automatic power down for VGA DAC, when there is no monitor attached.
	• Flat Panel Interface provided by connecting the Analogix ANX3110 DisplayPort converter to the APU's DisplayPort 0 supports:
	  • Single-channel LVDS interface: 1 x 18 bpp or 1 x 24 bpp.
	  • Dual-channel LVDS interface : 2 x 18 bpp or 2 x 24 bpp.
	  • VESA standard and JEDIA data mapping. Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3).
	  • Resolution up to 1920x1200 (WUXGA)
	• PCI Express® Graphics (PEG) x8 support.
	• 3x DDI (Digital Display Interface) with support for:
	  • 3x DisplayPort 1.2, multiplexed with HDMI/DVI ports. Supports hot plug detect.
	  • 1x HDMI 1.4a, multiplexed with DP/DVI ports. Supports hot plug detect.
	  • 2x Single Link DVI, multiplexed with DP/HDMI ports. Supports hot plug detect.

Peripheral Interfaces	• 4x Serial ATA® (6 Gb/s) with RAID 0/1 support. • 7 PCI Express® Lanes, supporting x1, x2 and x4 configurations. Supports full 5 Gb/s bandwidth in each direction per x1 link. • 8x USB 2.0 (EHCI) • SDIO interface (shared with GPIOs). • 4x USB 3.0 (XHCI) • 2x ExpressCard • LPC Bus • I²C Bus, Fast Mode, multimaster • SM Bus
BIOS	AMI Aptio® UEFI 2.x firmware; 4 MByte serial SPI with congatec Embedded BIOS features
Power Management	ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 11 of this user's guide to determine what options are available on your particular module.

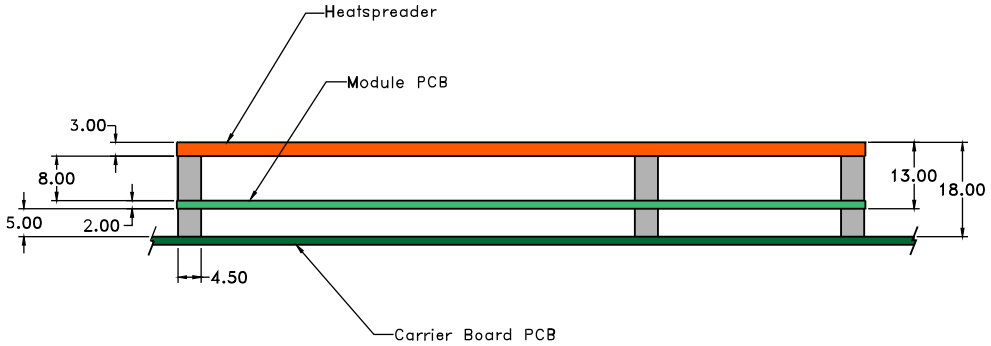
2.2 Supported Operating Systems

The conga-TFS supports the following operating systems.

- Microsoft® Windows® 8
- Microsoft® Windows® 7
- Microsoft® Windows® XP
- Microsoft® Windows® Embedded Standard
- Linux

2.3 Mechanical Dimensions

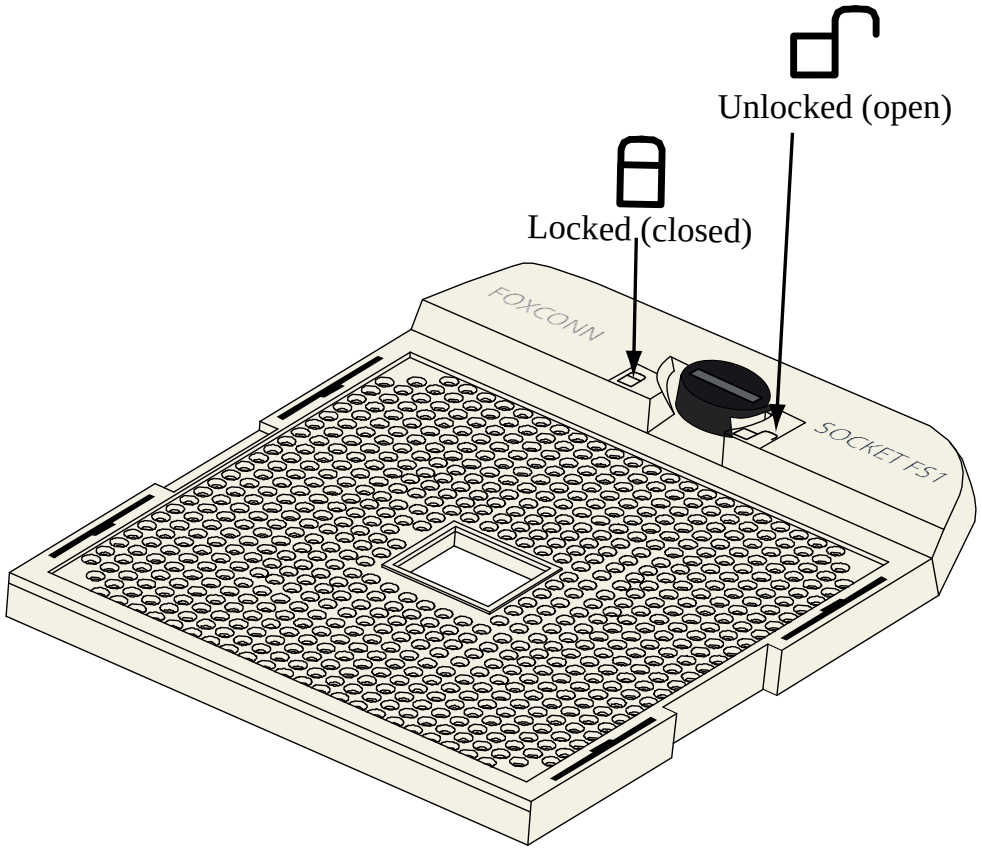
- 95.0 mm x 125.0 mm (3.74” x 4.92”)
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm.



2.4 Socketed Variant of conga-TFS

The conga-TFS is equipped with a µPGA zero insertion force (ZIF) socket. This socket has 722 contacts and mates with a µPGA package that has a maximum of 722 pins. The insertion and extraction forces are zero when the socket is not engaged (in the “open” position).

There are clear indicator marks located on the actuation mechanism that identify the lock (closed) and unlock (open) positions of the cover as well as the actuation direction (see picture below). These marks remain visible after the processor is inserted into the socket.



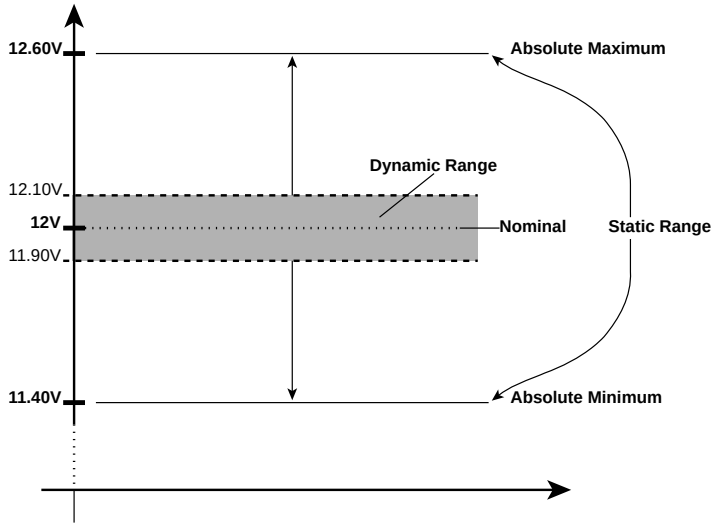
Electrostatic Sensitive Device

The conga-TFS is an electrostatic sensitive device. Do not handle the conga-TFS or processor, except at an electrostatic-free workstation. Failure to do so may cause damage to the module and/or processor and may void the manufacturer’s warranty.

2.5 Supply Voltage Standard Power

- 12V DC ± 5%

The dynamic range shall not exceed the static range.



2.5.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.5.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.6 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used for testing includes a conga-TFS module, conga-Cdebug carrier board, CRT monitor, SATA drive, and USB keyboard. The conga-Cdebug is modified so that the 12V input is only routed to the module and all other circuity on the carrier itself is powered by the 5V input. The SATA drive was powered externally by an ATX power supply so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. All recorded values were averaged over a 30 second time period. Cooling of the module was done by the module specific heatpipe heatspreader and a fan cooled heatsink to measure the power consumption under normal thermal conditions.

The conga-Cdebug originally does not provide 5V standby power. Therefore, an extra 5V_SB connection without any external loads was made. Using this setup, the power consumption of the module in S3 (Standby) mode was measured directly.

Each module was measured while running Windows 7 Professional 64Bit, PowerNow enabled, CPU Turbo Core enabled and Power Plan set to “Power Saver”. This setting ensures that core processors run in lowest frequency mode with minimal core voltage during desktop idle. Each module was tested while using two 1GB memory modules. Using different sizes of RAM, as well as one or two memory modules, will cause slight variances in the measured results.

To measure the worst case power consumption the cooling solution was removed and the CPU core temperature was allowed to run up to between 95° and 100°C while running 100% workload with the Power Plan set to “Balanced”. The peak current value was then recorded. This value should be taken into consideration when designing the system’s power supply to ensure that the power supply is sufficient during worst case scenarios.

Power consumption values were recorded during the following stages:

Windows 7 (64 bit)

- Desktop Idle (power plan = Power Saver)
- 100% CPU workload (see note below, power plan = Power Saver)
- 100% CPU workload at approximately 100°C peak power consumption (power plan = Balanced)
- Suspend to RAM. Supply power for S3 mode is 5V.

Note

A software tool was used to stress the CPU to Max Turbo Core Frequency.

Processor Information

In the following power tables there is some additional information about the processors. AMD describes the type of manufacturing process used for each processor. The following term is used:

nm=nanometer

The manufacturing process description is included in the power tables as shown below:

AMD R-464L 2.3 GHz Quad Core 2x2MB L2 Cache

32nm

For information about the manufacturing process visit AMD's website.

2.6.1 conga-TFS AMD Embedded R-464L 2.3/3.2 GHz Quad Core 2x2MB L2 Cache

conga-TFS Art. No. 041101	AMD Embedded R-464L 2.3/3.2 GHz Quad Core 2x2MB L2 Cache 32nm Layout Rev. TFSLA0 /BIOS Rev. TFSR000			
Turbo Frequency	3.2 GHz			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	TBD	TBD	TBD	TBD

2.6.2 conga-TFS AMD Embedded R-460H 1.9/2.8 GHz Quad Core 2x2MB L2 Cache

conga-TFS Art. No. 041102	AMD Embedded R-460H 1.9/2.8 GHz Quad Core 2x2MB L2 Cache 32nm Layout Rev. TFSLA0 /BIOS Rev. TFSR000			
Turbo Frequency	2.8 GHz			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	TBD	TBD	TBD	TBD

2.6.3 conga-TFS AMD Embedded R-272F 2.7/3.2 GHz Dual Core 1M L2 Cache

conga-TFS Art. No. 041103	AMD Embedded R-272F 2.7/3.2 GHz Dual Core 1MB L2 Cache 32nm Layout Rev. TFSLA0 /BIOS Rev. TFSR000			
Turbo Frequency	3.2 GHz			
Memory Size	2GB			
Operating System	Windows 7 (64 bit)			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	TBD	TBD	TBD	TBD

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Supply power for S3 mode is 5V while all other measured modes are supplied with 12V power. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

2.7 Supply Voltage Battery Power

- 2.0V-3.5V DC
- Typical 3V DC

2.7.1 CMOS Battery Power Consumption

RTC @ 20°C	Voltage	Current
Integrated in the AMD A70M Controller Hub	3V DC	0.5µA (4µA max)

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

2.8 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

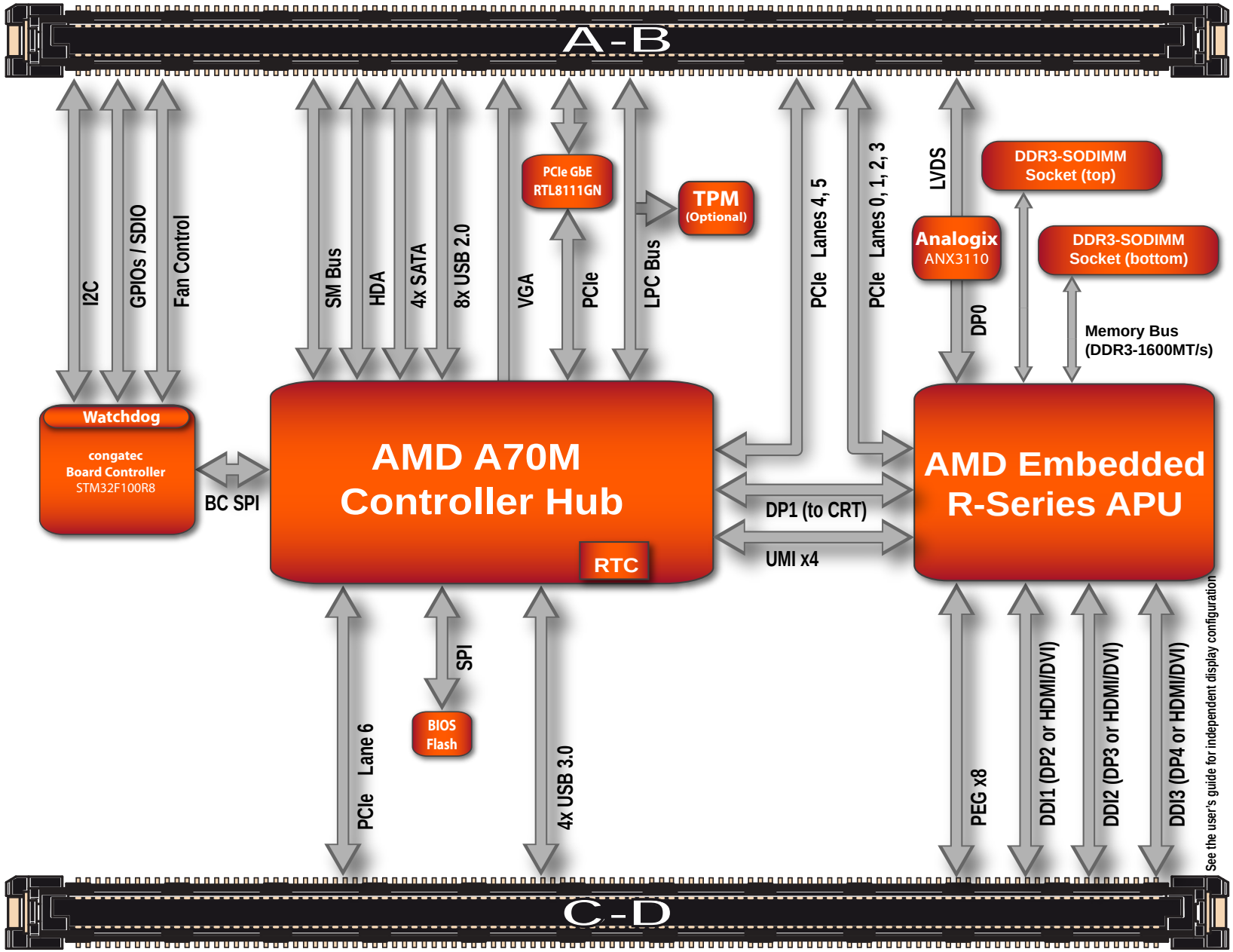
congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.

If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

For more information about operating a congatec module without heatspreader contact congatec technical support.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



4 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module and its aluminum plate is 1.6mm thick.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis thereby using the whole chassis as a heat dissipater.

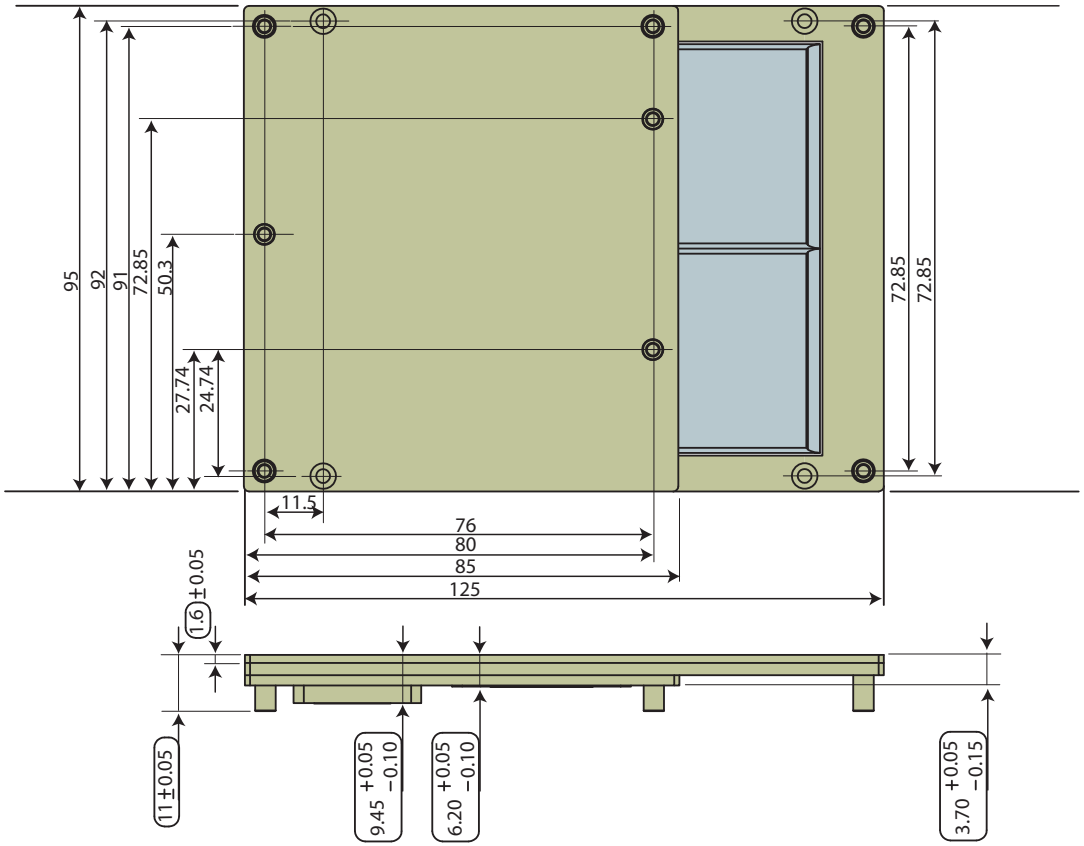
For additional information about the conga-TFS heatspreader, refer to section 4.1 of this document.

Caution

There are mounting holes on the heatspreader designed to attach the heatspreader to the module. These mounting holes must be used to ensure that all components that are required to make contact with heatspreader do so. Failure to utilize these mounting holes will result in improper contact between these components and heatspreader thereby reducing heat dissipation efficiency.

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

4.1 Heatspreader Dimensions



Note

All measurements are in millimeters. Maximum torque specification for heatspreader screws is 0.3 Nm. Mechanical system assembly mounting shall follow the valid DIN/IS0 specifications.

Caution

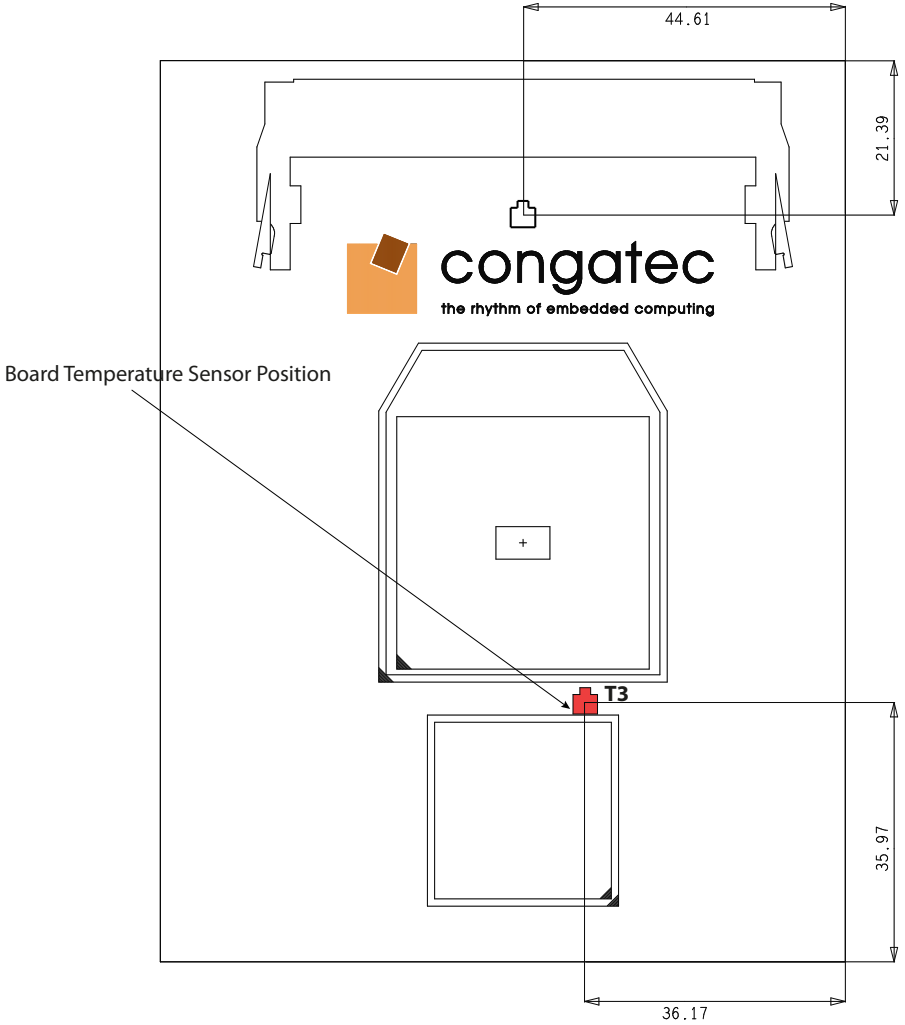
Exceeding the maximum torque specification for heatspreader screws may damage the module or/and the carrier board.

When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.

5 Onboard Temperature Sensor

Board Temperature Sensor:

Onboard the conga-TFS is a sensor that measures the temperature of the board. The board sensor is located at the top of the conga-TFS and is defined in CGOS API as CGOS_TEMP_BOARD. The sensor position is designated as T3 as shown below:

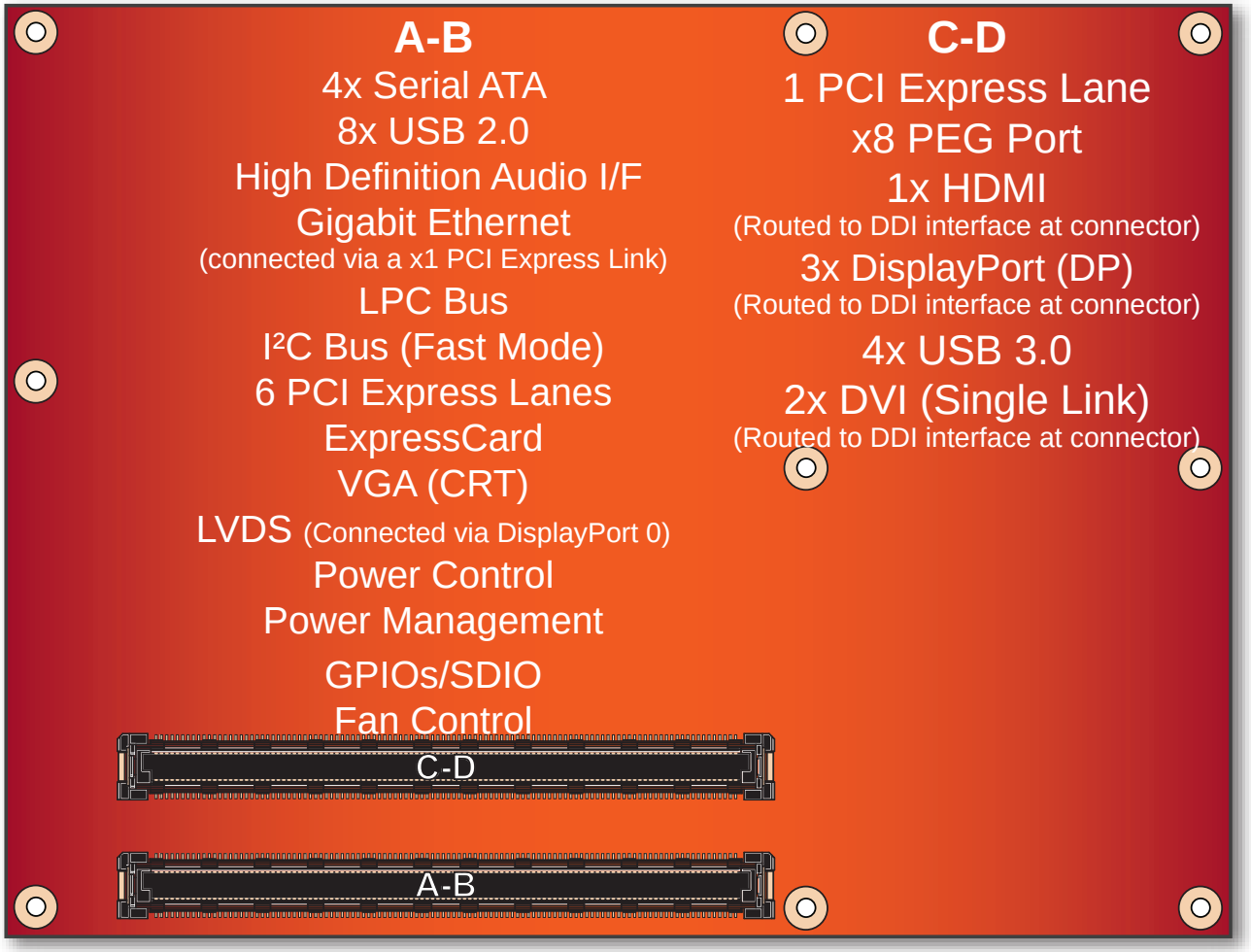


All dimensions in mm

6 Connector Subsystems Rows A, B, C, D

The conga-TFS is connected to the carrier board via two 220-pin connectors (COM Express Type 6 pinout) for a total of 440 pins connectivity. These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

In this view the connectors are seen “through” the module.



top view

6.1 Primary Connector Rows A and B

The following subsystems can be found on the primary connector rows A and B.

6.1.1 Serial ATA™ (SATA)

Six Serial ATA interfaces are provided via the AMD A70M Controller Hub . These six SATA ports are Gen 3 compliant, capable of up to 6.0 Gb/s transfer rate with RAID 0/1 support. Any of the six ports can be configured to a lower transfer rate of 3.0 Gb/s or 1.5 Gb/s for saving power. The SATA controller supports three modes of operation. These modes are IDE emulation, AHCI 1.3 and RAID.

The conga-TFS provides 4 SATA ports (SATA 0-3) externally, with hot plug detection and notification support.

6.1.2 USB 2.0

The conga-TFS offers four host controllers (two OHCI and EHCI respectively) provided by the AMD A70M Controller Hub for USB 2.0 support. These controllers comply with USB 1.1 and 2.0 specifications, offering a total of eight USB 2.0 ports on the conga-TFS. The USB ports are routed to connector rows A and B. Each port is capable of supporting USB 1.1 and 2.0 compliant devices. For more information about how the USB host controllers are routed, see section 8.6.

6.1.3 High Definition Audio (HDA) Interface

The conga-TFS provides an interface that supports the connection of external HD audio codecs over the HD audio link, via the AMD A70M Controller Hub audio controller. The HD audio controller consists of four independent output DMA engines and four independent input DMA engines. The controller supports up to four audio codecs and each codec has its own data input for the HD Audio interface.

Note

COM Express modules only support up to three data inputs (AC_SDIN[0:2]) as described in COM Express Specification 2.0.

The conga-TFS does not support AC'97 codecs.

6.1.4 Gigabit Ethernet

The conga-TFS offers Gigabit Ethernet with the integration of Realtek RTL8111GN Gigabit Ethernet Controller. This controller is implemented through the use of one PCI Express lane. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MDI0± to GBE0_MDI3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT

RJ45 connector with integrated or external isolation magnetics on the carrier board.

Note

The GBE0_LINK# output is only active during a 100Mbit or 1Gbit connection, it is not active during a 10Mbit connection. This is a limitation of Ethernet controller since it only has 3 LED outputs, ACT#, LINK100# and LINK1000#. The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TFS module.

6.1.5 LPC Bus

conga-TFS offers the Low Pin Count (LPC) bus via the AMD A70M Controller Hub. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific baseboard using this bus. Many devices are available for this cost-efficient, low-speed interface designed to support low bandwidth and legacy devices.

The LPC host bus controller supports two master DMA devices. TPM version 1.1/1.2 devices are also supported. See section 10.1.1 for more information about the LPC Bus.

6.1.6 I²C Bus Fast Mode

The I²C bus is implemented through the congatec board controller (STMicroelectronics STM32) and is accessed through the congatec CGOS driver and API. The controller provides a Fast Mode multi-master I²C Bus that has maximum I²C bandwidth.

6.1.7 PCI Express™

The AMD R-Series APU and the AMD A70M Controller Hub found on the conga-TFS provide a total of eight general purpose PCI Express lanes. One of the eight PCI Express lanes is utilized by the onboard Gigabit Ethernet interface. The conga-TFS offers the remaining seven PCI Express™ lanes externally on the AB and CD connector rows. These lanes are PCI Express™ Gen. 2 compliant.

Six PCI Express lanes (lanes 0-5) are available on the A,B connector row. Lanes 4 and 5 support only 2x1 links while lanes 0-3 support 1x4, 2x2, 1x2 + 2x1 and 4x1 links. These configurations are possible via the setup menu of the standard BIOS.

The PCI Express interface is based on the PCI Express Specification 2.0 with Gen 1 and Gen 2 speeds.

6.1.8 ExpressCard™

The conga-TFS supports the implementation of ExpressCards, which requires the dedication of one USB port or a x1 PCI Express link for each ExpressCard used.

6.1.9 VGA/CRT

The conga-TFS supports one VGA interface provided via the AMD A70M Controller Hub. The VGA translator provides VGA translation and supports a maximum resolution of 1920x1200 at a refresh rate of 60 Hz. It also provides auto monitor detection and automatic power-down for VGA DAC when there is no monitor attached.

6.1.10 LCD

The conga-TFS offers a dual channel LVDS interface. This interface is provided through the use of Analogix ANX3110 attached to one of the APU display channels (DP0). Analogix ANX3110 is a low-cost high quality DisplayPort to LVDS converter, offering up to 24 bits per pixel and single/dual channel LVDS output support.

6.1.11 General Purpose Serial Interface

Two TTL compatible two wire ports are available on Type 6 COM Express modules. These pins are designated SER0_TX, SER0_RX, SER1_TX and SER1_RX. Data out of the module is on the _TX pins. Hardware handshaking and hardware flow control are not supported. The module asynchronous serial ports are intended for general purpose use and for use with debugging software that make use of the “console redirect” features available in many operating systems.

Note

The General Purpose Serial Interface is not supported on the conga-TFS module.

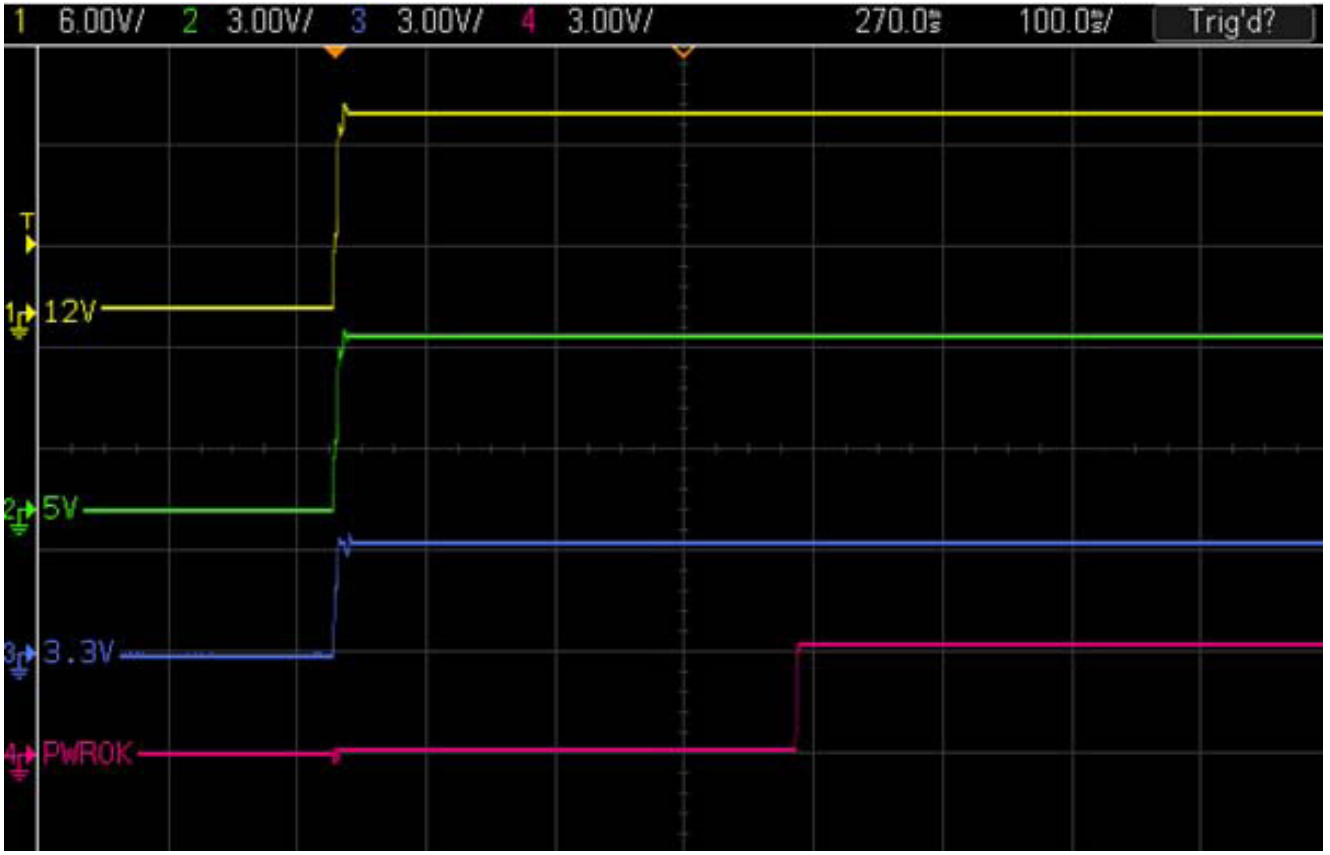
6.1.12 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. The PWR_OK is a 3.3V signal according to the COM Express Specification. The use of this input is optional.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. Although the PWR_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

A sample screenshot is shown below:



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the “power good” signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, it must be ensured that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-TFS module is capable of generating it’s own power good through the use of an internal monitor on the +12V ± 5% input voltage and/or the internal power supplies. The conga-TFS also provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-TFS’s pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

12 volt input power is the sole operational power source for the conga-TFS. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-TFS application:

- It has also been noticed that on some occasions, problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply

qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

6.1.13 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

6.2 Secondary Connector Rows C and D

The following subsystems can be found on the secondary connector rows C and D.

6.2.1 PCI Express™

The AMD R-Series APU and the AMD A70M Controller Hub found on the conga-TFS provide a total of eight general purpose PCI Express lanes. One of the eight PCI Express lanes is utilized by the onboard Gigabit Ethernet interface. The conga-TFS offers the remaining seven PCI Express™ lanes externally on the AB and CD connector rows.

One PCI Express lane (PCIe lane 6) is available on the CD connector row. This lane supports only x1 link and is PCI Express Specification 2.0 compliant, offering both Gen 1 and Gen 2 speeds.

6.2.2 PCI Express Graphics (PEG)

The conga-TFS supports x8 PCI Express Graphics only. The PEG interface is by default configured as a 1x8 link. The interface can be configured as a 2x4 link via the setup menu.

6.2.3 SDVO

SDVO is not supported on the conga-TFS.

6.2.4 HDMI/DVI

The AMD R-Series APU on the conga-TFS provides one port capable of full HDMI support. This HDMI port is supported on the conga-TFS and is multiplexed onto the Digital Display Interface (DDI) of the COM Express connector.

The HDMI interface can be combined with two DP ports or with DP and DVI ports to support three independent displays. Two independent HDMI ports may be enabled but only one port will support HDMI fully. The other will operate in DVI compatibility mode (without audio support).

6.2.5 DisplayPort (DP)

The conga-TFS offers three DP ports, each capable of supporting link-speeds of 1.62 Gbps and 2.7 Gbps on 1, 2 or 4 data lanes. The DP is multiplexed onto the Digital Display Interface of the COM Express connector. The DisplayPort specification is a VESA standard aimed at consolidating internal and external connection methods to reduce device complexity, supporting key cross industry applications and providing

performance scalability to enable the next generation of displays.

The supported DP combinations are:

- 3x DisplayPort
- 2x DisplayPort + 1x HDMI
- 2x DisplayPort + 1x DVI
- 1x DisplayPort + 1x DVI + 1x HDMI
- 1x DisplayPort + 2x DVI

Note

Two independent HDMI ports may be enabled but only one port will fully support HDMI. The other will operate in DVI compatibility mode (without audio support).

The combination of 1x HDMI and 2x DVI is not supported.

6.2.6 USB 3.0

The conga-TFS offers two xHCI host controllers provided by the AMD A70M Controller Hub. These controllers support up to four SuperSpeed USB 3.0 ports on the CD connector of the conga-TFS and allow data transfers up to 5 Gb/s. They also support SuperSpeed, high-speed, full-speed and low-speed traffic on the bus.

7 Additional Features

7.1 congatec Board Controller (cBC)

The conga-TFS is equipped with a STMicroelectronics STM32 microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

7.2 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

7.3 Graphic Output

The conga-TFS graphics are driven by AMD Radeon™ HD 7000G Series graphics engine, which is incorporated within the AMD R-Series APU found on the conga-TFS. This graphic engine supports DirectX®11 graphics with UVD 3.2, Video Compressing Engine 1.0, OpenGL 4.2, OpenCL™ 1.1.

7.4 Watchdog

The conga-TFS is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-TFS does not support external hardware triggering. For more information about the Watchdog feature see the BIOS setup description section 11.4.2 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

Note

The conga-TFS module does not support the watchdog NMI mode. COM Express type 6 modules do not support PCI bus and therefore the PCI_SERR# signal is not available. There is no way to drive an NMI to the processor without the presence of the PCI_SERR# PCI bus signal.

7.5 I²C Bus

The conga-TFS offers support for the frequently used I²C bus. The I2C bus is accessed through the CGOS driver and API. Thanks to the I²C host controller in the congatec board controller, the I²C bus is multi-master capable and runs at fast mode.

7.6 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behaviour of the system after an AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

7.7 Embedded BIOS

The conga-TFS is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. These are the most important embedded PC features:

7.7.1 CMOS Backup in Non Volatile Memory

A copy of the CMOS memory (SRAM) is stored in the BIOS flash device. This prevents the system from not booting up with the correct system configuration if the backup battery (RTC battery) has failed. Additionally, it provides the ability to create systems that do not require a CMOS backup battery.

7.7.2 OEM CMOS Default Settings and OEM BIOS Logo

This feature allows system designers to create and store their own CMOS default configuration and BIOS logo (splash screen) within the BIOS flash device. Customized BIOS development by congatec for these changes is no longer necessary because customers can easily do these changes by themselves using the congatec system utility CGUITL.

7.7.3 OEM BIOS Code

With the congatec embedded BIOS it is even possible for system designers to add their own code to the BIOS POST process. Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table, verb tables for HDA codecs, rare graphic modes and Super I/O controllers.

For more information about customizing the congatec embedded BIOS, refer to the congatec System Utility user’s guide, which is called

CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com or contact congatec technical support.

7.7.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-TFS BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

7.7.5 API Support (CGOS/EAPI)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

Other COM (Computer on Modules) vendors offer similar driver solutions for these kind of embedded PC features, which are by nature proprietary. All the API solutions that can be found on the market are not compatible to each other. As a result, writing application software that can run on more than one vendor's COM is not so easy. Customers have to change their application software when switching to another COM vendor. EAPI (Embedded Application Programming Interface) is a programming interface defined by the PICMG that addresses this problem. With this unified API it is now possible to run the same application on all vendor's COMs that offer EAPI driver support. Contact congatec technical support for more information about EAPI.

7.8 Security Features

The conga-TFS can be equipped optionally with a “Trusted Platform Module“ (TPM 1.2). The TPM 1.2 includes co-processors to calculate efficient hash and RSA algorithms with key lengths up to 2,048 bits, as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity and confidence levels.

7.9 Suspend to Ram

The Suspend to RAM feature is available on the conga-TFS.

8 conga Tech Notes

The conga-TFS has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

8.1 AHCI

The AMD A70M Controller Hub provides hardware support for Advanced Host Controller Interface (AHCI), a new programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

8.2 RAID

The industry-leading RAID capability provides high performance RAID 0/1 functionality on the 4 SATA ports of the conga-TFS. Software components include an Option ROM for pre-boot configuration and boot functionality, a Microsoft* Windows* compatible driver, and a user interface for configuration and management of the RAID capability of the AMD A70M Controller Hub.

8.3 AMD Processor Features

8.3.1 AMD64 Technology

- AMD64 technology instruction-set extensions
- 64-bit integer registers, 48-bit virtual addresses, and 40-bit physical addresses
- Sixteen 64-bit integer registers
- Sixteen 128-bit SSE/SSE2/SSE3/SSE4a registers

For more information about AMD64 Technology, visit http://www.amd.com.

8.3.2 Power Management

- Multiple low-power states
- AMD AllDay™ power technology
- System Management Mode (SMM)
- ACPI-compliant, including support for processor performance states (P-states)
- Supports processor power states C0, C1, C1E, C6, and CC6
- Supports sleep states including S0, S3, S4, and S5
- PCIe® core power gating
- PCIe speed power policy
- AMD Turbo CORE technology 3.0 with per core power gating

For more information about AMD64 Technology, visit http://www.amd.com.

8.3.3 AMD Virtualization™ Technology

- SVM pause count capability
- SVM disable and lock
- Rapid virtualization indexing (nested paging)
- Improved world-switch speed

For more information about AMD64 Technology, visit http://www.amd.com.

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

8.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-TFS ACPI thermal solution offers three different cooling policies:

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points. If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

8.5 ACPI Suspend Modes and Resume Events

conga-TFS supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 11.4.5 “ACPI Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Windows 7, Windows Vista, Linux, Windows XP and Windows 2K

This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S3-S5.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
USB Mouse/Keyboard Event	When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event. USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). Under Windows XP add following registry entries: Add this key: HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\usb Under this key add the following value: “USBBIOSx“=DWORD:00000000 *Note that Windows XP disables USB wakeup from S3, so this entry has to be added to re-enable it.* Configure USB keyboard/mouse to be able to wake up the system: In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check ‘Allow this device to bring the computer out of standby’. *Note: When the standby state is set to S3 in the ACPI setup menu, the power management tab for USB keyboard /mouse devices only becomes available after adding the above registry entry and rebooting to allow the registry changes to take affect.*
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

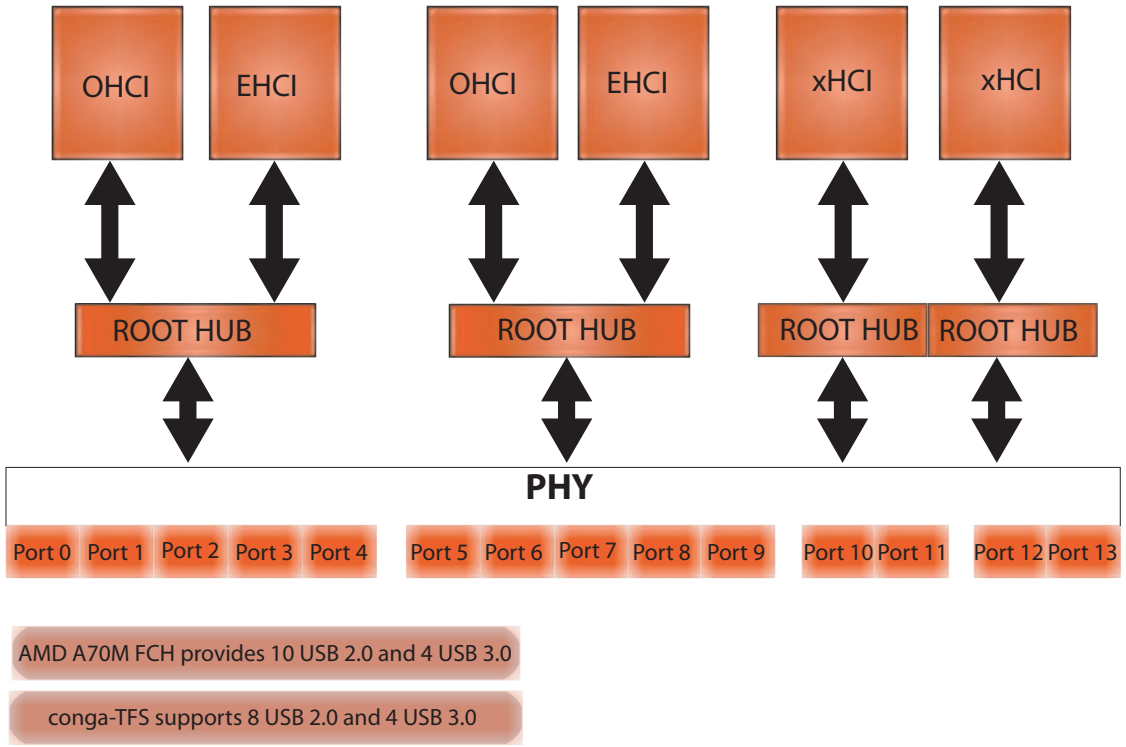
Note

The above list has been verified using a Windows XP SP3 ACPI enabled installation.

8.6 USB Host Controller

The AMD A70M Controller Hub provides two xHCI, two OHCI and two EHCI for the support of four USB 3.0 and ten USB 2.0 ports. The conga-TFS supports eight USB 2.0 via the OHCI and EHCI controllers, and four USB 3.0 via the xHCI controllers. The routing diagram is shown below:

Routing Diagram



9 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type 6 connectors used for congatec AG modules. The pinout of the modules complies with COM Express Type 6 Rev. 2.1.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.

Table 2 Signal Tables Terminology Descriptions

Term	Description
PU	Implemented pull-up resistor
PD	Implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0
PEG	PCI Express Graphics
SATA	In compliance with Serial ATA specification, Revision 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

9.1 A-B Connector Signal Descriptions

Table 3 High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	**High Definition Audio Reset:** This signal is the master hardware reset to external codec(s).	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SYNC	A29	**High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_BITCLK	A32	**High Definition Audio Bit Clock Output:** This signal is a 24.000MHz serial data clock generated by the High Definition Audio controller.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SDOUT	A33	**High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for High Definition Audio.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SDIN[2:0]	B28-B30	**High Definition Audio Serial Data In [0]:** These signals are serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for High Definition Audio.	I 3.3VSB	PD 50K	AC'97 codecs are not supported.

Table 4 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 / 100 / 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.			Not connected

Note

The GBE0_LINK# output is only active during a 100Mbit or 1Gbit connection, it is not active during a 10Mbit connection. This is a limitation of Ethernet controller since it only has 3 LED outputs, ACT#, LINK100# and LINK1000#. The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TFS module.

Table 5 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.0
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.0
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V		

Table 6 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0

PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 7 ExpressCard Support Pins Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request.	I 3.3VSB	PU 10k 3.3VSB	
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3V		

Table 8 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V	PU 10K 3.3V	
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V	PU 8.2K 3.3V	
LPC_SERIRQ	A50	LPC serial interrupt	I/OD 3.3V	PU 8.2K 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		

Table 9 USB 2.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

Table 10 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/OD	PU 4.7K 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/OD	PU 4.7K 3.3V	

Table 11 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10K	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10K	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	OD 3.3V	PU 2.2K 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/OD 3.3V	PU 2.2K 3.3V	

Table 12 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10K 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB	PD 10K	
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or left as no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or left as no-connect

Table 13 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/OD 3.3V	PU 2.2K 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/OD 3.3V	PU 2.2K 3.3VSB	
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.	O OD 3.3V	PU 10K 3.3V	
FAN_TACHIN	B102	Fan tachometer input.	I OD	PU 10K 3.3V	Requires a fan with two-pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 10K	Trusted Platform Module chip is optional.

Table 14 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3V		
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3V		
GPO2	B57	General purpose output pins. Shared with SD_WP. Input to COM Express, output from SD	O 3.3V	SD mode PU 8.2K 3.3V	
GPO3	B63	General purpose output pins. Shared with SD_CD. Input to COM Express, output from SD	O 3.3V	SD mode PU 8.2K 3.3V	
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3V	PU 40K 3.3V	
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3V	PU 40K 3.3V	
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3V	PU 40K 3.3V	
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3V	PU 40K 3.3V	

Table 15 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on rising edge.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V	PU 10K 3.3V	
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB	PU 10K 3.3VSB	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as “PS_ON”) may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		Not supported
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10K 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10K 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 10k 3.3V	

Signal	Pin #	Description	I/O	PU/PD	Comment
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10k 3.3V	
SMB_CK	B13	System Management Bus bidirectional clock line.	I/O 3.3VSB	PU 2.2K 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line.	I/O OD 3.3VSB	PU 2.2K 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3VSB	PU 10K 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch.	I 3.3V	PU 10K 3.3VSB	
SLEEP	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I 3.3V	PU 10K 3.3VSB	

Table 16 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O 3.3V		Not supported
SER1_TX	A101	General purpose serial port transmitter	O 3.3V		Not supported
SER0_RX	A99	General purpose serial port receiver	I 3.3V		Not supported
SER1_RX	A102	General purpose serial port receiver	I 3.3V		Not supported

Table 17 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

9.2 A-B Connector Pinout

Table 18 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+	B22	SATA3_TX+	A77	LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX-	B23	SATA3_TX-	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+	B25	SATA3_RX+	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX-	B26	SATA3_RX-	A81	LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA_BITCLK	B32	SPKR	A87	RSVD	B87	VCC_5V_SBY
A33	AC/HDA_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX (*)	B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX (*)	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX (*)	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX (*)	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga TFS.

9.3 C-D Connector Signal Descriptions

Table 19 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		Not supported

Table 20 USB 3.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX0-	C3		I		
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX0-	D3		O		
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX1-	C6		I		
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX1-	D6		O		
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX2-	C9		I		
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX2-	D9		O		
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX3-	C12		I		
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX3-	D12		O		

Table 21 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs.	I PCIE		PEG_RX8± - PEG_RX15± lanes are not supported.
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+	D52	PCI Express Graphics Transmit Output differential pairs.	O PCIE		PEG_TX8± - PEG_TX15± lanes are not supported.
PEG_TX0-	D53				
PEG_TX1+	D55				
PEG_TX1-	D56				
PEG_TX2+	D58				
PEG_TX2-	D59				
PEG_TX3+	D61				
PEG_TX3-	D62				
PEG_TX4+	D65				
PEG_TX4-	D66				
PEG_TX5+	D68				
PEG_TX5-	D69				
PEG_TX6+	D71				
PEG_TX6-	D72				
PEG_TX7+	D74				
PEG_TX7-	D75				
PEG_TX8+	D78				
PEG_TX8-	D79				
PEG_TX9+	D81				
PEG_TX9-	D82				
PEG_TX10+	D85				
PEG_TX10-	D86				
PEG_TX11+	D88				
PEG_TX11-	D89				
PEG_TX12+	D91				
PEG_TX12-	D92				
PEG_TX13+	D94				
PEG_TX13-	D95				
PEG_TX14+	D98				
PEG_TX14-	D99				
PEG_TX15+	D101				
PEG_TX15-	D102				
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I		Not supported.

Note

conga-TFS supports only x8 PCI Express Graphics (PEG).

Table 22 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with SDVO1_RED+, DP1_LANE0+ and TMDS1_DATA2+. Multiplexed with SDVO1_RED-, DP1_LANE0- and TMDS1_DATA2-.	O PCIE		
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with SDVO1_GRN+, DP1_LANE1+ and TMDS1_DATA1+. Multiplexed with SDVO1_GRN-, DP1_LANE1- and TMDS1_DATA1-.	O PCIE		
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with SDVO1_BLU+, DP1_LANE2+ and TMDS1_DATA0+. Multiplexed with SDVO1_BLU-, DP1_LANE2- and TMDS1_DATA0-.	O PCIE		
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with SDVO1_CK+, DP1_LANE3+ and TMDS1_CLK+. Multiplexed with SDVO1_CK-, DP1_LANE3- and TMDS1_CLK-.	O PCIE		
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	Multiplexed with SDVO1_INT+. Multiplexed with SDVO1_INT-.			Not supported
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	Multiplexed with SDVO1_TVCLKIN+. Multiplexed with SDVO1_TVCLKIN-.			Not supported
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	Multiplexed with SDVO1_FLDSTALL+. Multiplexed with SDVO1_FLDSTALL-.			Not supported
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD.	I 3.3V	PD 100K	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with SDVO1_CTRLCLK, DP1_AUX+ and HMDI1_CTRLCLK. DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE OD 3.3V	PD100K	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with SDVO1_CTRLDATA, DP1_AUX- and HDMI1_CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE I/OD 3.3V	PU 100K 3.3V	
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+ and TMDS2_DATA2+. Multiplexed with DP2_LANE0- and TMDS2_DATA2-.	O PCIE		
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+ and TMDS2_DATA1+. Multiplexed with DP2_LANE1- and TMDS2_DATA1-.	O PCIE		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+ and TMDS2_DATA0+. Multiplexed with DP2_LANE2- and TMDS2_DATA0-.	O PCIE		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+ and TMDS2_CLK+. Multiplexed with DP2_LANE3- and TMDS2_CLK-.	O PCIE		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD.	I 3.3V	PD 100K	
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+ and HDMI2_CTRLCLK. DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	I/O PCIE OD 3.3V	PD 100K	
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/OD 3.3V	PU 100K 3.3V	

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+. Multiplexed with DP3_LANE0- and TMDS3_DATA2-.	O PCIE		
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+. Multiplexed with DP3_LANE1- and TMDS3_DATA1-.	O PCIE		
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+. Multiplexed with DP3_LANE2- and TMDS3_DATA0-.	O PCIE		
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+. Multiplexed with DP3_LANE3- and TMDS3_CLK-.	O PCIE		
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD.	I 3.3V	PD 100K	
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK. DP AUX+ function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high	 I/O PCIE OD 3.3V	PD 100k	
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA. DP AUX- function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.	 I/O PCIE I/OD 3.3V	PU 100k	
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	

Note

The Digital Display Interface (DDI) signals are multiplexed with HDMI/DVI and DisplayPort (DP). The signals for these interfaces are routed to the DDI interface of the COM Express connector. Refer to the HDMI and DisplayPort signal description tables in this section for information about the signals routed to the DDI interface of the COM Express connector.

The conga-TFS provides three DDI interfaces that support three Display ports, one HDMI and two DVI. The supported combinations are:

3x Display Port, 2x Display Port + 1x HDMI, 2x Display Port + 1x DVI, 1x Display Port + 1x DVI + 1x HDMI, 1x Display Port + 2x DVI

The combination of HDMI + 2x DVI is not supported. Two independent HDMI ports may be enabled but only one port will fully support HDMI. The other will operate in DVI compatibility mode (without audio support).

Table 23 SDVO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDVO1_RED+ SDVO1_RED-	D26 D27	Serial Digital Video red output differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0- pair.	O PCIE		Not supported
SDVO1_GRN+ SDVO1_GRN-	D29 D30	Serial Digital Video green output differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		Not supported
SDVO1_BLU+ SDVO1_BLU-	D32 D33	Serial Digital Video blue output differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		Not supported
SDVO1_CK+ SDVO1_CK-	D36 D37	Serial Digital Video clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		Not supported
SDVO1_INT+ SDVO1_INT-	C25 C26	Serial Digital Video Interrupt input differential pair. .Multiplexed with DDI1_PAIR4+ and DDI1_PAIR4-.	I PCIE		Not supported
SDVO1_TVCLKIN+ SDVO1_TVCLKIN-	C29 C30	Serial Digital Video TVOUT synchronization clock pair. Multiplexed with DDI1_PAIR5+ and DDI1_PAIR5-.	I PCIE		Not supported
SDVO1_FLDSTALL+ SDVO1_FLDSTALL-	C15 C16	Serial Digital Video Field Stall input differential pair. Multiplexed with DDI1_PAIR6+ and DDI1_PAIR6-.	I PCIE		Not supported
SDVO1_CTRLCLK	D15	SDVO I²C clock line - to set up SDVO peripherals. Multiplexed with DDI1_CTRLCLK_AUX+.	I/O OD 3.3V		Not supported
SDVO1_CTRLDATA	D16	SDVO I²C data line - to set up SDVO peripherals. Multiplexed with DDI1_CTRLDATA_AUX-.	I/O OD 3.3V		Not supported

Note

SDVO is not supported on the conga-TFS.

Table 24 HDMI/DVI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS1_CLK + TMDS1_CLK -	D36 D37	HDMI/DVI TMDS Clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
TMDS1_DATA0+ TMDS1_DATA0-	D32 D33	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
TMDS1_DATA1+ TMDS1_DATA1-	D29 D30	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-..	O PCIE		
TMDS1_DATA2+ TMDS1_DATA2-	D26 D27	HDMI/DVI TMDS differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
HDMI1_HPD	C24	HDMI/DVI Hot-plug detect. Multiplexed with DDI1_HPD.	I PCIE	PD 100K	
HDMI1_CTRLCLK	D15	HDMI/DVI I²C Control Clock Multiplexed with DDI1_CTRLCLK_AUX+	OD 3.3V	PD 100K	2.2k to 3.3V Pull-up should be implemented on the carrier board.
HDMI1_CTRLDATA	D16	HDMI/DVI I²C Control Data Multiplexed with DDI1_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	2.2k to 3.3V Pull-up should be implemented on the carrier board.
TMDS2_CLK + TMDS2_CLK -	D49 D50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-.	O PCIE		
TMDS2_DATA0+ TMDS2_DATA0-	D46 D47	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-.	O PCIE		
TMDS2_DATA1+ TMDS2_DATA1-	D42 D43	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-.	O PCIE		
TMDS2_DATA2+ TMDS2_DATA2-	D39 D40	HDMI/DVI TMDS differential pair. Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-..	O PCIE		
HDMI2_HPD	D44	HDMI/DVI Hot-plug detect. Multiplexed with DDI2_HPD	I PCIE	PD 100K	
HDMI2_CTRLCLK	C32	HDMI/DVI I²C Control Clock Multiplexed with DDI2_CTRLCLK_AUX+	OD 3.3V	PD 100K	2.2k to 3.3V Pull-up should be implemented on the carrier board.
HDM12_CTRLDATA	C33	HDMI/DVI I²C Control Data Multiplexed with DDI2_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	2.2k to 3.3V Pull-up should be implemented on the carrier board.
TMDS3_CLK + TMDS3_CLK -	C49 C50	HDMI/DVI TMDS Clock output differential pair.. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		
TMDS3_DATA0+ TMDS3_DATA0-	C46 C47	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		
TMDS3_DATA1+ TMDS3_DATA1-	C42 C43	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-..	O PCIE		
TMDS3_DATA2+ TMDS3_DATA2-	C39 C40	HDMI/DVI TMDS differential pair. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		
HDMI3_HPD	C44	HDMI/DVI Hot-plug detect. Multiplexed with DDI3_HPD.	I PCIE	PD 100K	
HDMI3_CTRLCLK	C36	HDMI/DVI I²C Control Clock Multiplexed with DDI3_CTRLCLK_AUX+	OD 3.3V	PD 100K	2.2k to 3.3V Pull-up should be implemented on the carrier board.

Signal	Pin #	Description	I/O	PU/PD	Comment
HDMI3_CTRLDATA	C37	HDMI/DVI I²C Control Data Multiplexed with DDI3_CTRLDATA_AUX-	I/OD 3.3V	PU 100K 3.3V	2.2k to 3.3V Pull-up should be implemented on the carrier board.

Note

The conga-TFS supports a maximum of two activated TMDS outputs. Only one output can be used as HDMI.

Table 25 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE3+ DP1_LANE3-	D36 D37	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-.	O PCIE		
DP1_LANE2+ DP1_LANE2-	D32 D33	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-.	O PCIE		
DP1_LANE1+ DP1_LANE1-	D29 D30	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-.	O PCIE		
DP1_LANE0+ DP1_LANE0-	D26 D27	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-.	O PCIE		
DP1_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI1_HPD.	I 3.3V	PD 100K	
DP1_AUX+	D15	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100K	
DP1_AUX-	D16	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100K 3.3V	
DP2_LANE3+ DP2_LANE3-	D49 D50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		
DP2_LANE2+ DP2_LANE2-	D46 D47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		
DP2_LANE1+ DP2_LANE1-	D42 D43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		
DP2_LANE0+ DP2_LANE0-	D39 D40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI2_PAIR0+ and DDI1_PAIR0-	O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
DP2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI2_HPD.	I 3.3V	PD 100K	
DP2_AUX+	C32	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100K	
DP2_AUX-	C33	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100K 3.3V	
DP3_LANE3+ DP3_LANE3-	C49 C50	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-.	O PCIE		
DP3_LANE2+ DP3_LANE2-	C46 C47	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O PCIE		
DP3_LANE1+ DP3_LANE1-	C42 C43	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-.	O PCIE		
DP3_LANE0+ DP3_LANE0-	C39 C40	Uni-directional main link for the transport of isochronous streams and secondary data. Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-.	O PCIE		
DP3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI3_HPD.	I 3.3V	PD 100K	
DP3_AUX+	C36	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PD 100k	
DP3_AUX-	C37	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O PCIE	PU 100k 3.3V	

Table 26 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pinout Type 1 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 (no IDE) NC GND NC Pinout Type 4 (no PCI) NC GND GND Pinout Type 5 (no IDE, no PCI) GND NC NC Pinout Type 6 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.	PDS	TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard. The conga-TFS is based on the COM Express Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.
TYPE10#	A97	Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed. TYPE10# NC Pinout R2.0 PD Pinout Type 10 pull down to ground with 4.7k resistor 12V Pinout R1.0 This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7k resistor.	PDS	Not connected to indicate "Pinout R2.0".

Table 27 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

9.4 C-D Connector Pinout

Table 28 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1-	D56	PEG_TX1-
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+	D58	PEG_TX2+
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2-	D59	PEG_TX2-
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PEG_RX3+	D61	PEG_TX3+
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PEG_RX3-	D62	PEG_TX3-
C8	GND	D8	GND	C63	RSVD	D63	DDPC_CTRLCLK
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	RSVD	D64	DDPC_CTRLDATA
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	PEG_RX4+	D65	PEG_TX4+
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4-	D66	PEG_TX4-
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RSVD	D67	GND
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	PEG_RX5+	D68	PEG_TX5+
C14	GND	D14	GND	C69	PEG_RX5-	D69	PEG_TX5-
C15	DDI1_PAIR6+ (*)	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	DDI1_PAIR6- (*)	D16	DDI1_CTRLDATA_AUX-	C71	PEG_RX6+	D71	PEG_TX6+
C17	RSVD	D17	RSVD	C72	PEG_RX6-	D72	PEG_TX6-
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	PEG_RX7+	D74	PEG_TX7+
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	PEG_RX7-	D75	PEG_TX7-
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+ (*)	D22	PCIE_TX7+ (*)	C77	RSVD	D77	RSVD
C23	PCIE_RX7- (*)	D23	PCIE_TX7- (*)	C78	PEG_RX8+ (*)	D78	PEG_TX8+ (*)
C24	DDI1_HPD	D24	RSVD	C79	PEG_RX8- (*)	D79	PEG_TX8- (*)
C25	DDI1_PAIR4+ (*)	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	DDI1_PAIR4- (*)	D26	DDI1_PAIR0+	C81	PEG_RX9+ (*)	D81	PEG_TX9+ (*)
C27	RSVD	D27	DDI1_PAIR0-	C82	PEG_RX9- (*)	D82	PEG_TX9- (*)
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD
C29	DDI1_PAIR5+ (*)	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	DDI1_PAIR5- (*)	D30	DDI1_PAIR1-	C85	PEG_RX10+ (*)	D85	PEG_TX10+ (*)
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- (*)	D86	PEG_TX10- (*)
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-	C88	PEG_RX11+ (*)	D88	PEG_TX11+ (*)
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11- (*)	D89	PEG_TX11- (*)
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+	C91	PEG_RX12+ (*)	D91	PEG_TX12+ (*)
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-	C92	PEG_RX12- (*)	D92	PEG_TX12- (*)

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C38	DDI3_DDC_AUX_SEL	D38	RSVD	C93	GND	D93	GND
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+	C94	PEG_RX13+ (*)	D94	PEG_TX13+ (*)
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-	C95	PEG_RX13- (*)	D95	PEG_TX13- (*)
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+	C97	RVSD	D97	RSVD
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-	C98	PEG_RX14+ (*)	D98	PEG_TX14+ (*)
C44	DDI3_HPD	D44	DDI2_HPD	C99	PEG_RX14- (*)	D99	PEG_TX14- (*)
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+	C101	PEG_RX15+ (*)	D101	PEG_TX15+ (*)
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-	C102	PEG_RX15- (*)	D102	PEG_TX15- (*)
C48	RSVD	D48	RSVD	C103	GND	D103	GND
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+	D52	PEG_TX0+	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0-	D53	PEG_TX0-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV# (*)	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+	D55	PEG_TX1+	C110	GND (FIXED)	D110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-TFS.

10 System Resources

10.1 I/O Address Assignment

The I/O address assignment of the conga-TFS module is functionally identical with a standard PC/AT.

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

10.1.1 LPC Bus

On the conga-TFS, the PCI Express Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Bus not the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus. In the congatec Embedded BIOS, the following I/O address ranges are sent to the LPC Bus:

2Eh – 2Fh
4Eh – 4Fh
60h, 64h
2E8h – 2EFh
2F8h – 2FFh
378h – 37Fh
3E8h – 3EFh
3F8h – 3FFh
778h – 77Fh
A00h – BFFh

Parts of these ranges are not available if a Super I/O is used on the carrier board. If a Super I/O is not implemented on the carrier board, then these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

10.2 Interrupt Request (IRQ) Lines

Table 32 IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		IRQ3 via SERIRQ
4	Yes		IRQ4 via SERIRQ
5	Yes		IRQ5 via SERIRQ
6	Yes		IRQ6 via SERIRQ
7	Yes		IRQ7 via SERIRQ
8	No	Real-time Clock	Not applicable
9	No	SCI	Not applicable
10	Yes		IRQ10 via SERIRQ
11	Yes		IRQ11 via SERIRQ
12	Yes		IRQ12 via SERIRQ
13	No	Math processor	Not applicable
14	Note 1	IDE Controller 0 (IDE0) / Generic	IRQ14 via SERIRQ
15	Note 1	IDE Controller 1 (IDE0) / Generic	IRQ15 via SERIRQ

Note

1. If the SATA interface mode configuration in BIOS setup is not set to legacy IDE mode, the IRQ14 and IRQ15 are then available for LPC bus.

2. Interrupts to be used via SERIRQ have to be reserved in the BIOS setup to ensure that they are not assigned to any PCI Express device.

Table 33 IRQ Lines in APIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		IRQ3 via SERIRQ
4	Yes		IRQ4 via SERIRQ
5	Yes		IRQ5 via SERIRQ
6	Yes		IRQ6 via SERIRQ
7	Yes		IRQ7 via SERIRQ
8	No	Real-time Clock	Not applicable
9	No	SCI	Not applicable
10	Yes		IRQ10 via SERIRQ
11	Yes		IRQ11 via SERIRQ
12	Yes		IRQ12 via SERIRQ
13	No	Math processor	Not applicable
14	Note 1	IDE Controller 0 (IDE0) / Generic	IRQ14 via SERIRQ
15	Note 1	IDE Controller 1 (IDE1) / Generic	IRQ15 via SERIRQ
16	No		PIRQA, PCI Express Root Port 0/4, onboard Gigabit LAN Controller, PCI Express Port 0 (see Note 2), Main High Definition Audio Controller
17	No		PIRQB, PCI Express Root Port 1/5, PCI Express Port 1/4 (see Note 2), XHCI Host Controller 1, EHCI Host Controller 0, Integrated Graphics Controller
18	No		PIRQC, PCI Express Root Port 2/6, PCI Express Port 2/5 (see Note 2), XHCI Host Controller 0, OHCI Host Controller 0, HDMI / DisplayPort, HDA Controller (for HDMI/DisplayPort integrated audio only)
19	No		PIRQD, PCI Express Root Port 3/7, PCI Express Port 3/6 (see Note 2), Serial ATA Controller / IDE Controller
20	Yes		PIRQE
21	Yes		PIRQF
22	Yes		PIRQG
23	Yes		PIRQH

Note

1. If the SATA interface mode configuration in BIOS setup is not set to legacy IDE mode, then IRQ14 and 15 are free for LPC bus.

2. Interrupt used if a single function PCI Express device is connected to the respective PCI Express port.

3. Interrupts to be used via SERIRQ have to be reserved in the BIOS setup to ensure that they are not assigned to any PCI Express devices.

10.3 PCI Configuration Space Map

Table 34 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	01h	00h	Internal	Integrated Graphics Controller (VGA)
00h	01h	01h	Internal	HDMI/DisplayPort HDA Controller (for HDMI/DisplayPort integrated audio only)
00h (Note 1)	02h	00h	Internal	PCI Express Graphic (PEG) Port (x8)
00h (Note 1)	04h	00h	Internal	PCI Express Root Port 0
00h (Note 1)	05h	00h	Internal	PCI Express Root Port 1
00h (Note 1)	06h	00h	Internal	PCI Express Root Port 2
00h (Note 1)	07h	00h	Internal	PCI Express Root Port 3
00h	10h	00h	Internal	XHCI Host Controller 0
00h	10h	01h	Internal	XHCI Host Controller 1
00h	11h	00h	Internal	Serial ATA Controller / IDE Controller
00h	12h	00h	Internal	OHCI Host Controller 0
00h	12h	02h	Internal	EHCI Host Controller 0
00h	14h	00h	N.A	SMBus Host Controller
00h	14h	02h	Internal	High Definition Audio Controller
00h	14h	03h	N.A	PCI to LPC Bridge
00h	14h	04h	N.A	PCI to PCI Bridge
00h	15h	00h	Internal	PCI Express Root Port 4
00h (Note 1)	15h	01h	Internal	PCI Express Root Port 5
00h (Note 1)	15h	02h	Internal	PCI Express Root Port 6
00h (Note 1)	15h	03h	Internal	PCI Express Root Port 7
00h	18h	00h	N.A	Chipset Configuration Registers
00h	18h	01h	N.A	Chipset Configuration Registers
00h	18h	02h	N.A	Chipset Configuration Registers
00h	18h	03h	N.A	Chipset Configuration Registers
00h	18h	04h	N.A	Chipset Configuration Registers
00h	18h	05h	N.A	Chipset Configuration Registers
01h (Note 2)	00h	00h	Internal	PEG Port
02h (Note 2)	00h	00h	Internal	PCI Express Port 0
03h (Note 2)	00h	00h	Internal	PCI Express Port 1
04h (Note 2)	00h	00h	Internal	PCI Express Port 2
05h (Note 2)	00h	00h	Internal	PCI Express Port 3
07h (Note 2)	00h	00h	Internal	Onboard Gigabit LAN Controller
08h (Note 2)	00h	00h	Internal	PCI Express Port 4
09h (Note 2)	00h	00h	Internal	PCI Express Port 5
0Ah (Note 2)	00h	00h	Internal	PCI Express Port 6

Note

1. *The PCI Express ports are visible only if the PCI Express port is set to “Enabled” in the BIOS setup program and a device is attached to the corresponding PCI Express port on the carrier board.*

2. *The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

10.4 PCI Interrupt Routing Map

Table 35 PCI Interrupt Routing Map

PIRQ	APIC Mode IRQ	VGA	HDA (HDMI/DP)	XHCI0	XHCI1	OHCI0	EHCI 0	SM Bus	SATA (IDE)	HDA (Main)	PEG Root Port	PEG Port	LAN
A	16									x			x
B	17	x			x		x						
C	18		x	x		x					x	x	
D	19								x				
E	20												
F	21												
G	22												
H	23												

PIRQ	PCI-EX Root Port 0	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	PCI-EX Root Port 4	PCI-EX Root Port 5	PCI-EX Root Port 6	PCI-EX Root Port 7	PCI-EX Port 0	PCI-EX Port 1	PCI-EX Port 2	PCI-EX Port 3	PCI-EX Port 4	PCI-EX Port 5	PCI-EX Port 6
A	x				x				x [1]	x [4]	x [3]	x [2]	x [4]	x [3]	x [2]
B		x				x			x [2]	x [1]	x [4]	x [3]	x [1]	x [4]	x [3]
C			x				x		x [3]	x [2]	x [1]	x [4]	x [2]	x [1]	x [4]
D				x				x	x [4]	x [3]	x [2]	x [1]	x [3]	x [2]	x [1]
E															
F															
G															
H															

Note

[1] *Interrupt used by single function PCI Express devices (INTA).*

[2] *Interrupt used by multifunction PCI Express devices (INTB).*

[3] *Interrupt used by multifunction PCI Express devices (INTC).*

[4] *Interrupt used by multifunction PCI Express devices (INTD).*

10.5 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

10.6 SM Bus

The System Management (SM) bus signals are connected to the AMD A70M Controller Hub and is not intended to be used by off-board non-system management devices. For more information about this subject, contact congatec technical support.

11 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

11.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

11.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used, a selection will be displayed immediately after POST allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

11.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

Main	Advanced	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

11.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
Main BIOS Version	no option	Displays the main BIOS version.
OEM BIOS Version	no option	Displays the additional OEM BIOS version.
Build Date	no option	Displays the date the BIOS was built.
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
Running Time	no option	Displays the time the board is running [in hours max. 65535].
►Platform Information	submenu	Opens the platform information submenu.
System Date	Day of the week, month/day/year	Specifies the current system date *Note: The date is in month/day/year format.*
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24 hour format.*

11.3.1 Platform Information

The Platform Information submenu offers additional hardware and software information.

Feature	Options	Description
Processor Information	no option	Displays the processor ID string, supported speeds and microcode information.
Memory Information	no option	
Total Memory	no option	Displays the total amount of installed memory.
DIMM0 (Top)	no option	Displays the top memory socket DIMM information.
DIMM1 (Bottom)	no option	Displays the bottom memory socket DIMM information.

11.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features and only features described within this user's guide are listed.

Main	Advanced	Boot	Security	Save & Exit
	Graphics			
	Watchdog			
	Hardware Health Monitoring			
	PCI & PCI Express			
	RTC Wake			
	ACPI			
	CPU			
	Chipset			
	SATA			
	USB			
	Super IO			
	Serial Port Console Redirection			

11.4.1 Graphics Submenu

Feature	Options	Description
Primary Graphics Device	IGD **PCI/PCIe**	Select primary graphics adapter to be used during boot up. IGD: Internal Graphics Device. PCI/PCIe: Try to use external PCI Express or PCI Graphics Device. If not present, IGD is used.
Integrated Graphics Device	Auto Disabled Manual Configuration	Deactivate IGD or select frame buffer configuration mode. In auto mode, the frame buffer size will be defined based on the amount of physical memory present.
IGD Framebuffer size	32M 64M 128M **256M** 512M 1G 2G	Only visible if IGD is set to manual configuration. Set fixed graphics frame buffer size for IGD. The graphics driver might allocate additional memory.
CRT Interface	Disabled **Enabled**	Enable or disable the CRT interface.
Digital Display Interface 1	Disabled Display Port **HDMI/DVI**	Select the type of digital display interface that should be offered.
Digital Display Interface 2	Disabled Display Port **HDMI/DVI**	Select the type of digital display interface that should be offered.
Digital Display Interface 3	Disabled **Display Port** HDMI/DVI	Select the type of digital display interface that should be offered.
LFP Interface	Disabled **Enabled**	Enable or disable the local flat panel (LFP) interface.
Always Try Auto Panel Detect	**No** Yes	If set to ‘Yes’ the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel . Only if no external EDID data set can be found, the data set selected under ‘Local Flat Panel Type’ will be used as fallback data set.

Feature	Options	Description
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The numbers in bracket specify the congatec internal number of the respective panel data set. Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.
Backlight Inverter Type	None PWM **I2C**	Select the type of backlight inverter used. PWM = Use IGD PWM signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.
PWM Inverter Frequency (Hz)	**200**-40000	Only visible if backlight inverter type is set to PWM. Set the PWM inverter frequency in hertz.
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%**	Actual backlight value in percent of the maximum setting.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Setting	**No** Yes	Allow to invert backlight control values if required for the actual I2C type backlight hardware controller.

11.4.2 Watchdog Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One-time Trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to '*One time trigger'* the watchdog will be disabled after the first trigger. If set to *'Single event'*, every stage will be executed only once, then the watchdog will be disabled. If set to *'Repeated event'* the last stage will be executed repeatedly until a reset occurs.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event see note below.
Event 2	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Selects the timeout value for the first stage watchdog event.

Feature	Options	Description
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason, the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

Additionally, the conga-TFS module does not support the watchdog NMI mode. COM Express type 6 modules do not support the PCI bus and therefore the PCI_SERR# signal is not available. There is no way to drive a NMI to the processor without the presence of the PCI_SERR# PCI bus signal.

11.4.3 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	no option	Current CPU temperature
Board Temperature	no option	Current board temperature
12V Standard	no option	Current 12V input reading
5V Standby	no option	Current 5V standby input reading
CPU Fan Speed	no option	Current CPU fan speed reading

11.4.4 PCI and PCI Express Submenu

Feature	Options	Description
PCI Settings		
PCI Latency Timer	**32**, 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate SERR#.
Generate EXCD0/1_PERST#	Disabled 1ms 5ms **10ms** 50ms 100ms 150ms 200ms 250ms	Select whether and how long the COM Express EXCD0_PERST# and EXCD1_PERST# pins should be driven low during POST.
►PCI Express Settings	submenu	PCI Express device and link settings.
►PCI Express Gen 2 Settings	submenu	PCI Express generation 2 specific device and link settings.
►PCI Express Port Configuration	submenu	Configure PCI Express and PEG ports.
►PIRQ Routing & IRQ Reservation	submenu	Manual PIRQ routing and interrupt reservation for legacy devices.

11.4.4.1 PCI Express Settings Submenu

Feature	Options	Description
Relaxed Ordering	**Disabled** Enabled	Enable or disable PCI Express device relaxed ordering.
Extended Tag	**Disabled** Enabled	If enabled, a device may use an 8-bit tag filed as a requester.
No Snoop	Disabled **Enabled**	Enable or disable PCI Express device 'No Snoop' option.

Feature	Options	Description
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum payload of PCI Express devices or allow system BIOS to select the value.
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set maximum read request size of PCI Express devices or allow system BIOS to select the value.
Extended Synch	**Disabled** Enabled	If enabled, the generation of extended PCI Express synchronization patterns is allowed.
ASPM Support	Disabled Auto Force L0s	Set the ASPM level. Force L0s: Force all links to L0s state Auto: BIOS auto configuration Disabled: Disable ASPM on all links
Extended Synch	**Disabled** Enabled	If enabled, the generation of extended synchronization patterns is allowed.
Link Training Retry	Disabled 2 3 **5**	Defines numer of retry attempts software will take to retrain the link if the previous training attempt was unsuccessful.
Link Training Timeout (us)	10-10000 (**100**)	Defines number of microseconds software will wait before polling the link training bit in the link status register. Value ranges from 10us to 10000us.
Unpopulated Links	**Keep Link On** Disabled	In order to save power, software will disable unpopulated PCI Express links if this option is set to ‘Disabled’.
Restore PCIE Registers	Enabled **Disabled**	On non-PCI Express aware operating systems, some devices may not be re-initialized correctly after S3. Setting this node to Enabled restores PCI Express configuration on S3 resume. Warning: Enabling this may cause issues with other hardware after S3 resume.

11.4.4.2 PCI Express Gen2 Settings Submenu

Feature	Options	Description
Completion Timeout	**Default** Shorter Longer Disabled	Modify or disable the completion timeout value of devices that support this feature. Default: Use hardware default value (50us to 50ms) Shorter or Longer: Use shorter or longer timeouts Disabled: Disable completion timeout
ARI Forwarding	**Disabled** Enabled	If supported by hardware and set to 'Enabled', the downstream port disables its device number field 0 enforcement when turning a type1 configuration request into a type0 configuration request, thus permitting access to extended functions in an Alternative Routing-ID (ARI) device below the port.
AtomicOp Requester Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this function initiates AtomicOp requests if the bus master enable bit is set in the command register.
AtomicOp Egress Blocking	**Disabled** Enabled	If supported by hardware and set to 'Enabled', outbound AtomicOp requests via egress ports will be blocked.
IDO Request Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this permits ID-Based Ordering (IDO) for request packets.
IDO Completion Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this permits ID-Based Ordering (IDO) for completion packets.
LTR Mechanism Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this enables the Latency Tolerance Reporting (LTR) mechanism.
End-End TLP Prefix Blocking	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this function will block forwarding of TLPs containing End-End TLP prefixes.
Target Link Speed	**Auto** Force to 2.5 GT/s Force to 5.0 GT/s	If supported by hardware and set to 'Force to 2.5 GT/s' for downstream ports, this sets an upper limit on link operational speed by restricting the values advertised by the upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.
Clock Power Management	**Disabled** Enabled	If supported by hardware and set to 'Enabled', the device is permitted to use CLKREQ# signal for power management of the link clock in accordance to the protocol defined in appropriate form factor specification.
Compliance SOS	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this will force the Link Training and Status State Machine (LTSSM) to send SKP Ordered Sets between sequences when sending compliance pattern or modified compliance pattern.
Hardware Autonomous Width	**Enabled** Disabled	If supported by hardware and set to 'Disabled', this will disable the hardware's ability to change link width except width size reduction for the purpose of correcting unstable link operation.
Hardware Autonomous Speed	**Enabled** Disabled	If supported by hardware and set to 'Disabled', this will disable the hardware's ability to change link speed except speed rate reduction for the purpose of correcting unstable link operation.

11.4.4.3 PCI Express Port Configuration Submenu

Feature	Options	Description
PEG x8 Port	Disabled **Enabled**	Enable or disable PEG port. The conga-TFS PEG port only supports up to 8 lanes.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 0	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 1	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 2	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 3	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 4	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 5	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.
PCI Express Port 6	Disabled **Enabled**	Enable or disable PCI Express port. Note: Unless the hotplug support for this port is enabled as well, an unpopulated port will still be disabled if no PCI Express device is connected.
Always Enable Port	**Disabled** Enabled	Disabled: Disable the internal PCI Express interface device if no device detected on the port. Enabled: Enable the internal PCI Express interface device also if no device is detected on the port.

11.4.4.4 PIRQ Routing & IRQ Reservation Submenu

Feature	Options	Description
PIRQA	**Auto**, IRQ3, IRQ4, IRQ5, IRQ6, IRQ10, IRQ11, IRQ14, IRQ15	Set interrupt for selected PIRQ. Please refer to the board's resource list for a detailed list of devices connected to the respective PIRQ. NOTE: These settings will only be effective while operating in PIC (non-IOAPIC) interrupt mode.
PIRQB	same as PIRQA	same as PIRQA
PIRQC	same as PIRQA	same as PIRQA
PIRQD	same as PIRQA	same as PIRQA
PIRQE	same as PIRQA	same as PIRQA
PIRQF	same as PIRQA	same as PIRQA
PIRQG	same as PIRQA	same as PIRQA
PIRQH	same as PIRQA	same as PIRQA
Reserve Legacy Interrupt 1	**None**, IRQ3, IRQ4, IRQ5, IRQ6, IRQ10, IRQ11, IRQ14, IRQ15	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.
Reserve Legacy Interrupt 2	same as Reserve Legacy Interrupt 1	The interrupt reserved here will not be assigned to any PCI or PCI Express device and thus maybe available for some legacy bus device.

11.4.5 RTC Wake Submenu

Feature	Options	Description
Wake System AT Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour		Specify wake up hour.
Wake up minute		Specify wake up minute.
Wake up second		Specify wake up second.

11.4.6 ACPI Submenu

Feature	Options	Description
Hibernation Support	Disabled **Enabled**	Enable or disable system ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend.
Critical Trip Point	**Disabled,** 70, 80, 90, 95, 100, 105, 110, 115°C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Active Trip Point	**Disabled**, 20, 30, 40, 50, 60, 70, 80, 90, 95°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Trip Point	**Disabled**, 60, 70, 80, 90, 95°C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.
Lid Support	**Disabled** Enabled	Configure COM Express LID# signal to act as ACPI Lid.
Sleep Button Support	**Disabled** Enabled	Configure COM Express SLEEP# signal to act as ACPI sleep button.

11.4.7 CPU Submenu

Feature	Options	Description
AMD PowerNow! Support	Disabled **Enabled**	Enable or disable support for AMD PowerNow! technology. Allows operating systems to control CPU performance states.
Maximum Power Up P-State	**P-State 0** P-State 1 P-State 2 P-State 3 P-State 4 P-State 5	Select the maximum CPU performance state to be set at power up. Higher numbers mean lower performance. P-state 0 is the highest performance state.
Maximum OS P-State	**P-State 0** P-State 1 P-State 2 P-State 3 P-State 4 P-State 5	Select the maximum CPU performance state the operating system should support. Higher numbers mean lower performance. P-state 0 is the highest performance state.
NX Mode	Disabled **Enabled**	Enable or disable the 'no-execute' page protection function.
Virtualization Technology	Disabled **Enabled**	When enabled, a Virtual Machine Manager (VMM) can utilize the integrated hardware virtualization support.
Core Performance Boost	**Auto** Disabled	Control usage of boosted P-States, i.e. P-States above the standard CPU P-State limit. Availability depends on CPU revision and type, actual usage on total CPU/GPU chip power consumption.

Feature	Options	Description
C6 Support	**Disabled** Enabled	Enable or disable CPU C6 low power state support.

11.4.8 Chipset Submenu

Feature	Options	Description
Memory Bus Clock	**Auto** 400MHz (DDR3-800) 533MHz (DDR3-1066) 667MHz (DDR3-1333) 800MHz (DDR3-1600)	Select or limit memory frequency.
Bank Interleaving	Disabled **Enabled**	Enable or disable memory bank interleaving.
Channel Interleaving	Disabled **Enabled**	Enable or disable memory channel interleaving.
Memory Clear	**Disabled** Enabled	Select whether memory should be actively cleared during POST.
Onboard LAN Controller	Disabled **Enabled**	Enable or disable the onboard ethernet controller.
HDA Controller	**Auto** Disabled Enabled	Control activation of the High Definition Audio controller device. Disabled = HDA controller will be unconditionally disabled Enabled = HDA controller will be unconditionally enabled Auto = HDA controller will be enabled if HDA codec present, disabled otherwise.
HDMI/DP Audio Support	Disabled **Enabled**	Enable or disable HDMI/DisplayPort integrated audio support.
SD Controller Mode	Disabled DMA PIO	Enable or disable the onboard SD controller and select its operating mode.
SD Clock Control	**50MHz/25MHz** 40MHz/20MHz 25MHz/12.5MHz	Select actual SD clocks for high and low speed transfer modes.
SD Speed Mode	Low Speed **High Speed**	Select SD transfer speed mode.
SD System Address Support	32Bit **64Bit**	Select 32bit or 64bit system address support for SD controller.
USB 3.0 Spread Spectrum Clock	Disabled **Enabled**	Enable or disable clock spreading for USB 3.0

11.4.9 SATA Submenu

Feature	Options	Description
SATA Controller	Disabled **Enabled**	Enable or disable the onboard SATA controller.
SATA Mode Selection	Native IDE RAID **AHCI** Legacy IDE	Select onboard SATA controller mode.
SATA Port 0	**Enabled** Disabled	Enable or disable selected port.
Port Speed	**Auto** Gen1 Gen2	Select SATA speed generation for the selected port.
SATA Port 1	**Enabled** Disabled	Enable or disable selected port.
Port Speed	**Auto** Gen1 Gen2	Select SATA speed generation for the selected port.
SATA Port 2	**Enabled** Disabled	Enable or disable selected port.
Port Speed	**Auto** Gen1 Gen2	Select SATA speed generation for the selected port.
SATA Port 3	**Enabled** Disabled	Enable or disable selected port.
Port Speed	**Auto** Gen1 Gen2	Select SATA speed generation for the selected port.
SATA Port 0	no option	SATA drive 0 information.
SATA Port 1	no option	SATA drive 1 information.
SATA Port 2	no option	SATA drive 2 information.
SATA Port 3	no option	SATA drive 3 information.

11.4.10 USB Submenu

Feature	Options	Description
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
USB3.0 BIOS Support	**Enabled** Disabled	USB 3.0 operating mode support on USB ports 0-3 in BIOS run and pre-OS time. Enabled = USB ports are enabled to operate in USB 3.0 mode. Effective only when the XHCI controllers are enabled. Disabled = USB ports will operate in USB2.0 mode only.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI OS driver.
EHCI Hand-off	**Disabled** Enabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
USB Transfer Timeout	1 sec 5 sec 10 sec **20 sec**	Timeout value for legacy USB control, bulk and interrupt transfers.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device start unit command timeout.
Device Power -Up Delay Selection	**Auto** Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power-Up Delay Value	**5** 1-40	Actual power-up delay value in seconds.
USB Mass Storage Device Name (Auto detected USB mass storage devices are listed here dynamically)	**Auto** Floppy Forced FDD Hard Disk CD-ROM	Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. *Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.* Select *AUTO* to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. *Forced FDD* allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. *Hard disk* allows the device to be emulated as hard disk. *CDROM* assumes the CD-ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.
►USB Port & Controller Configuration	submenu	Configure USB ports and controllers.

11.4.10.1 USB Port & Controller Configuration Submenu

Feature	Options	Description
XHCI 0 (Port 0-1)	Disabled **Enabled**	Enable or disable the XHCI (USB 3.0) host controller.
XHCI 1 (Port 2-3)	Disabled **Enabled**	Enable or disable the XHCI (USB 3.0) host controller.
OHCI 0 (Port 4-7)	Disabled **Enabled**	Enable or disable the OHCI host controller.
EHCI 0 (Port 4-7)	Disabled **Enabled**	Enable or disable the EHCI (USB 2.0) host controller.
OHCI 2 (Port 0-3)	Disabled **Enabled**	Enable or disable the OHCI host controller.
EHCI 2 (Port 0-3)	Disabled **Enabled**	Enable or disable the EHCI (USB 2.0) host controller.
USB Port 0 (XHCI Mode) (USB Port 0)	Disabled **Enabled**	Enable or disable the respective USB port. Alternative port control if XHCI controller is disabled.
USB Port 1 (XHCI Mode) (USB Port 1)	Disabled **Enabled**	Enable or disable the respective USB port. Alternative port control if XHCI controller is disabled.
USB Port 2 (XHCI Mode) (USB Port 2)	Disabled **Enabled**	Enable or disable the respective USB port. Alternative port control if XHCI controller is disabled.
USB Port 3 (XHCI Mode) (USB Port 3)	Disabled **Enabled**	Enable or disable the respective USB port. Alternative port control if XHCI controller is disabled.
USB Port 4	Disabled **Enabled**	Enable or disable the respective USB port.
USB Port 5	Disabled **Enabled**	Enable or disable the respective USB port.
USB Port 6	Disabled **Enabled**	Enable or disable the respective USB port.
USB Port 7	Disabled **Enabled**	Enable or disable the respective USB port.

11.4.11 Super I/O Submenu

Feature	Options	Description
PS/2 Keyboard/Mouse Support	**Disabled** Enabled	Enable or disable PS/2 Keyboard/Mouse controller support.
Serial Port 0	Disabled **Enabled**	Enable or disable serial port 0.
Device Settings	*IO=3F8h; IRQ=4;*	*Fixed configuration of serial port 0 if enabled.*
Serial Port 1	Disabled **Enabled**	Enable or disable serial port 1.
Device Settings	*IO=2F8h; IRQ=3;*	*Fixed configuration of serial port 1 if enabled.*
Parallel Port	**Disabled** Enabled	Enable or disable parallel port.
Device Settings	*IO=378h; IRQ=7;*	*Fixed configuration of the parallel port if enabled.*
Device Mode	**Standard Parallel Mode** EPP Mode ECP Mode EPP Mode & ECP Mode	Set the parallel port mode.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

11.4.12 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
►Console Redirection Settings	submenu	Opens console redirection configuration sub menu.
COM1 Console Redirection	**Disabled** Enabled	Enable or disable serial port 1 console redirection.
►Console Redirection Settings	submenu	Opens console redirection configuration sub menu.

11.4.12.1 Console Redirection Settings Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.
Baud rate	9600, 19200, 38400, 57600, **115200**	Select baud rate.
Data Bits	7, **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Enabled** Disabled	Select whether serial redirection should be continued after POST.

11.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

11.5.1 Boot Settings Configuration

Feature	Options	Description
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. *Note: The default OEM logo is a dark screen.*
Setup Prompt Timeout	**1** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot (not recommended), 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The “Device Based” boot priority list allows you to select from a list of currently detected devices only. The “Type Based” boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the “Device Based” boot priority list might change dynamically in cases when devices are physically removed or added to the system. The “Type Based” boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if device based priority list control is selected. If “Type Based” priority list control is enabled only 8 boot devices can be prioritized.)	Disabled SATA 0 Drive SATA 1 Drive SATA 2 Drive SATA 3 Drive USB Floppy USB Hard disk USB CDROM Onboard LAN External LAN Other BEV Device	This view is only available when in the default “Type Based” mode. When in “Device Based” mode you will only see the devices that are currently connected to the system.
►CSM & Option ROM Control	submenu	Opens submenu which controls the execution of UEFI and legacy option ROMs.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. Note: *Only works with an ATX type power supply.*

Feature	Options	Description
AT Shutdown Mode	System Reboot **Hot S5**	Determines the behavior of an AT-powered system after a shutdown.
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
UEFI Fast Boot	**Disabled** Enabled	Enable or disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS / legacy boot options.
VGA Support	Auto **UEFI Driver**	If set to Auto, the legacy video option ROM will be installed for legacy OS boot; boot logo will NOT be shown during POST. For UEFI OS boot the UEFI GOP driver will be installed.
USB Support	Disabled **Full Init** Partial Init	If set to Disabled, no USB device will be available before OS boot. If set to Partial Init, specific USB ports/devices will NOT be available before OS boot. If set to Enabled, all USB devices will be available during POST and after OS boot.
PS/2 Device Support	Disabled **Enabled**	If set to Disabled, PS/2 devices will be skipped.
Network Stack Driver Support	**Disabled** Enabled	If set to Disabled, the UEFI network stack driver installation will be skipped.

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

11.5.1.1 CSM & Option ROM Control Submenu

Feature	Options	Description
Launch CSM	**Enabled** Disabled	Controls the execution of the CSM module. Only disable for pure UEFI operating system support.
Boot Option Filter	UEFI and Legacy **Legacy Only** UEFI Only	Controls which devices / boot loaders the system should boot to.
PXE Option ROM Launch Policy	**Do Not Launch** UEFI ROM Only Legacy ROM Only Legacy ROM First UEFI ROM First	Controls the execution of UEFI and legacy PXE option ROMs
Storage Option ROM Launch Policy	Do Not Launch UEFI ROM Only Legacy ROM Only **Legacy ROM First** UEFI ROM First	Controls the execution of UEFI and legacy mass storage device option ROMs
Video Option ROM Launch Policy	Do not Launch UEFI ROM Only **Legacy ROM Only** Legacy ROM First UEFI ROM First	Controls the execution of UEFI and legacy video option ROMs
Other Option ROM Launch Policy	**UEFI ROM Only** Legacy ROM Only	Controls the execution of option ROMs for PCI / PCI Express devices other than network, mass storage or video.
GateA20 Active	**Upon Request** Always	Gate A20 control. Upon Request: Gate A20 can be disabled using BIOS services. Always: Do not allow disabling Gate A20 This option is useful when any runtime code is executed above 1MB.
Option ROM Messages	**Force BIOS** Keep Current	Set display mode for option ROMs.
INT19 Trap Response	Immediate **Postponed**	BIOS reaction on INT19 trapping by Option ROM Immediate: Execute the trap right away. Postponed: Execute the trap during legacy boot.

11.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

11.6.1 Security Settings

Feature	Options	Description
Administrator Password	enter password	Specifies the setup administrator password.
HDD Security Configuration		
List of all detected hard disks supporting the security feature set	Select device to open device security configuration submenu	

11.6.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

11.6.3 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen.

You can display a Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
► **Boot Override** *List of all boot devices currently detected.*	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to “Device Based”.

12 Additional BIOS Features

The conga-TFS uses a congatec/AMI AptioEFI that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as TFS1R1xx where TFS1 is the project code, R is the identifier for a BIOS ROM file, 1 is the feature number and xx is the major and minor revision number.

The conga-TFS BIOS binary size is 4 MB.

12.1 Supported Flash Devices

The conga-TFS supports the following flash devices:

- Atmel AT25DF321-SU
- Greenliant Systems SST25VF032B-66-4I-S2AF
- Macronix MX25L3206EM2I-12G
- Winbond W25Q64CVSSIG

The flash devices listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.

12.2 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” refer to the user’s guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

12.3 BIOS Security Features

The BIOS provides a setup administrator password that limits access to the BIOS setup menu.

12.4 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to ‘lock’ and ‘unlock’ drives using the security password. A ‘locked’ drive will be detected by the system, but no data can be accessed. Accessing data on a ‘locked’ drive requires the proper password to ‘unlock’ the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within four attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

13 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.3	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0	http://www.serialata.org
PICMG® COM Express Module™ Base Specification	http://www.picmg.org/
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications