conga-TCA3

COM Express 2.1 Type 6 Compact Module with 3rd Generation Intel® Processors

User's Guide

Revision 1.9

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2014-01-09	AEM	• Preliminary release
0.2	2014-07-04	AEM	• Deleted the variant equipped with Intel Celeron N2920 (PN: 047306) from sections 1, 2.1 and 2.5 • Added industrial variant with PN: 047312 to conga-TCA3 Options Information in section 1 "Introduction" • Updated the notes in section 2.1 "Feature List" and section 6.1.2 "Low Voltage Memory". Added note in section 2.2 "Supported OS" • Updated caution notes in sections 2.7 “Environmental Specifications” and 4 “Heatspreader”. Updated section 7.3 "USB Port Mapping" • Deleted support for MIPI interfaces from the whole document
1.0	2014-09-23	AEM	• Added UART interface to the block diagram and to section 2.1 "Feature List" • Updated section 5.1.13 "General Purpose Serial Interface" • Deleted the conga-TCA3 PWR_OK input circuitry in section 5.1.14 "Power Control" because the circuitry is not implemented in conga-TCA3 • Added note about the configuration of fan_pwm pin as push-pull in section 6.1.3.3 “Fan Control” and table 14 “Miscellaneous Signal Description” • Updated section 7.1.1.1 "Intel Virtualization Technology" • Deleted the active cooling sub-section from section 7.1.1.3 “Thermal Management” because the BIOS does not support this feature • Added sections 9 "System Resources", 10 "BIOS Setup Description" and 11 "Additional BIOS Features" • Official release
1.1	2015-04-15	AEM	• Updated the note in section 2.2 "Supported Operating Systems" • Added note about Intel's HSIC errata (USB ports 4-7 reset) to sections 5.1.4 "USB 2.0" and 7.3 "USB Port Mapping"
1.2	2017-02-21	AEM	• Updated the notes in sections 2.1 "Feature List", 2.2 "Supported Operating Systems" and 6.1.2 "Low Voltage Memory (DDR3L)" • Updated section 2.7 "Environment Specifications" and added CSP dimensions to section 4 • Added note about UART limitations in section 5.1.13 " General Purpose Serial Interface (UART)" • Deleted the statement that the fan_pwm signal was configured as push-pull in section 6.1.3.3 “Fan Control” and table 14 “Miscellaneous Signal Description” • Deleted section 6.1.3.7 "Power Loss Control" because of duplication • Corrected the statement that PWRBTN# signal is active on rising edge in table 16 “Power and System Management Signal Descriptions” • Corrected the description of pins D63 and D64 in table 28 “Connector C-D Pinout" • Updated section 10 "BIOS Setup Description"
1.3	2018-12-07	AEM	• Updated the information about handling electrostatic sensitive devices in preface section • Updated the note in section 2.2 "Supported Operating Systems" • Added a note about optimal storage conditions to section 2.7 “Environmental Specifications” • Added note about the storage of congatec cooling solutions to section 4 “Cooling Solutions” • Changed the reference in the note in tables 30, 31 and 32 to section 8.4 • Updated section 10 "BIOS Setup Description"

1.4	2020-04-22	AEM	• Added note about the minimum pulse width required for proper button detection in table 23 “Power and System Management Signal Descriptions” • Updated section 4 "Cooling Solutions" • Added information about congatec MLF file to section 11 "Additional BIOS Features" • Updated sections 11.2 "Updating the BIOS" and 11.3 "Supported Flash Devices" • Deleted section 12 "Industry Specifications"
1.5	2020-08-07	AEM	• Updated section 7.1 "Intel SoC Features" • Restructured the whole document • Corrected typographical error in section 11 "Additional BIOS Features" • Removed the capacity of optional eMMC from the manual
1.6	2021-04-19	AEM	• Corrected the storage temperature for industrial variants in section 2.7 “Environmental Specifications” • Updated table 2 “conga-TCA3 (commercial variants)", table 3 “conga-TCA3 (industrial variants)", table 4 “Feature Summary”, table 9 “Display Combination” and table 17 “TMDS Signal Descriptions” • Updated section 3 “Block Diagram” and section 5.1.2 “Display Interfaces" • Deleted section 5.1.3 “HDMI” and section 5.1.4 “DVI” • Added note to table 17 “TMDS Signal Descriptions”
1.7	2021-07-31	AEM	• Added Software License Information • Changed congatec AG to congatec GmbH • Re-arranged section 6 "Additional Features" • Updated section 6.5 "congatec Battery Management Interface"
1.8	2021-11-16	AEM	• Deleted HDMI references from section 1.2 "Options Information", section 2.1 "Feature List", section 3 "Block Diagram and section 5.1.2 "Display Interfaces"
1.9	2023-11-30	AEM	• Updated the title page • Updated the RoHS statement • Added a note about optimal storage conditions to section 2.7 “Environmental Specifications” • Added note about the storage of congatec cooling solutions to section 4 “Cooling Solutions” • Updated section 6.3.4 "Power Loss Control"

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-TCA3. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide
COM Express™ Specification

The links to these documents can be found on the congatec GmbH website at www.congatec.com

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Caution

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Terminology

Term	Description
GB	Gigabyte
GHz	Gigahertz
kB	Kilobyte
MB	Megabyte
Mbit	Megabit
kHz	Kilohertz
MHz	Megahertz
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
DDC	Display Data Channel
SoC	System On Chip
LVDS	Low-Voltage Differential Signaling
Gbe	Gigabit Ethernet
eMMC	Embedded Multi-media Controller
HDA	High Definition Audio
cBC	congatec Board Controller
N.C	Not connected
N.A	Not available
TBD	To be determined

Contents

List of Tables

1 Introduction

1.1 COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express™ modules are available in following form factors:

- Mini 84 mm x 55 mm
- Compact 95 mm x 95 mm
- Basic 125 mm x 95 mm
- Extended 155 mm x110 mm

Table 1 COM Express™ 2.1 Pinout Types

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports	USB 2.0/ USB 3.0	Display Interfaces
Type 1	A-B	Up to 6			1	8 / 0	VGA, LVDS
Type 2	A-B C-D	Up to 22	32-bit	1	1	8 / 0	VGA, LVDS,PEG/SDVO
Type 3	A-B C-D	Up to 22	32-bit		3	8 / 0	VGA,LVDS,PEG/SDVO
Type 4	A-B C-D	Up to 32		1	1	8 / 0	VGA,LVDS,PEG/SDVO
Type 5	A-B C-D	Up to 32			3	8 / 0	VGA,LVDS,PEG/SDVO
Type 6	A-B C-D	Up to 24			1	8 / 4	VGA,LVDS,PEG, 3x DDI
Type 10	A-B	Up to 4			1	8 / 0	1x DDI

The conga-TCA3 modules use the Type 6 pinout definition and comply with COM Express 2.1 specification. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules provide most of the functional requirements for any application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 6 pinout provides the ability to offer PCI Express, Serial ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

1.2 Options Information

The conga-TCA3 is available in 10 variants (six commercial and four industrial).The table below shows the different configurations available.

Table 2 conga-TCA3 (commercial variants)

Part-No.	047302	047303	047305	047300	047301	047304
Processor	Intel® Atom™ E3826 (Dual Core, 1.46 GHz)	Intel® Atom™ E3825 (Dual Core, 1.33 GHz)	Intel® Celeron® J1900 (Quad Core, 2.0 GHz)	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3827 (Dual Core, 1.75 GHz)	Intel® Atom™ E3815 (Single Core, 1.46 GHz)
L2 Cache	1 MB	1 MB	2 MB	2 MB	1 MB	512kB
Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics
GFX Normal/Burst	533 / 667	533 / N.A	688 / 854	542 / 792	542 / 792	400 / N.A
LVDS	Single/Dual 18/24-bit	Single/Dual 18/24-bit	Single/Dual 18/24-bit	Single/Dual 18/24-bit	Single/Dual 18/24-bit	Single/Dual 18/24-bit
DDI	DP++	DP++	DP++	DP++	DP++	DP++
Memory (DDR3L)	1066 MT/s dual channel	1066 MT/s single channel	1333 MT/s dual channel	1333 MT/s dual channel	1333 MT/s dual channel	1066 MT/s single channel
Max. TDP / SDP	7 W	6 W	10 W	10 W	8 W	5 W

Table 3 conga-TCA3 (Industrial variants)

Part-No.	047310	047311	047312	047314
Processor	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3827 (Dual Core, 1.75 GHz)	Intel® Atom™ E3826 (Dual Core, 1.46 GHz)	Intel® Atom™ E3815 (Single Core, 1.46 GHz)
L2 Cache	2 MB	1 MB	1 MB	512kB
Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics
GFX Normal/Burst	542 / 792	542 / 792	533 / 667	400 / N.A
LVDS	Single/Dual 18/24-bit	Single/Dual 18/24-bit	Single/Dual 18/24-bit	Single/Dual 18/24-bit
DDI	DP++	DP++	DP++	DP++
Memory (DDR3L)	1333 MT/s dual channel	1333 MT/s dual channel	1066 MT/s dual channel	1066 MT/s single channel
Max. TDP	10 W	8 W	7 W	5 W

2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 6 Rev. 2.1 (Compact size 95 x 95 mm)	
Processor	3rd Generation Intel® Atom™ and Intel® Celeron® processors	
Memory	Single or dual channel memory interface (up to two memory sockets). Supports: - SO-DIMM non-ECC DDR3L modules - Data rates up to 1333 MT/s - Maximum 8 GB capacity **NOTE**: Variants equipped with Intel Atom E3815 and E3825 feature single channel memory interface and therefore support only one memory socket. For more information, see "Options Information" table on page 13.	
Chipset	Integrated in SoC	
Onboard Storage	Optional eMMC 4.5 onboard flash (optional for only Intel® Atom™ variants)	
Audio	High Definition Audio (HDA)/digital audio interface with support for multiple codecs.	
Ethernet	Gigabit Ethernet via the onboard Intel® I210 Gigabit Ethernet controller.	
Graphics Options	Intel® HD Graphics Gen. 7, full hardware acceleration for MPEG2, H.264, DirectX11, OCL 1.2, OGL 3.2, WMV9 and VC1. Dual simultaneous display support.	
	2x DP++ 1x LVDS 1x VGA Optional eDP interface	**NOTE**: *1 *The second DDI channel is only available if LVDS is disabled.* *2 *Variants with optional eDP interface do not support LVDS* *3 *The conga-TCA3 does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented*
Peripheral Interfaces	2x SATA® up to 3 Gb/s 5x PCI Express® Gen2 links up to 5.0 GT/s per lane 8x USB 2.0 (with up to 1x USB 3.0) 2x UART 1x SD/MMC	GPIOs muxed with SD card SPI Bus LPC Bus I²C Bus, multimaster
BIOS	AMI Aptio® V UEFI 2.x firmware; 8 MB serial SPI with congatec Embedded BIOS features (OEM Boot Logo, OEM Default Settings, LCD Control, Display Auto Detection, Backlight Control, Flash Update)	
Power Management	ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).	
congatec Board Controller	Multi Stage Watchdog, non-volatile User Data Storage, Manufacturing and Board Information, Board Statistics, BIOS Setup Data Backup, I²C bus (fast mode, 400 kHz, multi-master), Power Loss Control	

Note

The conga-TCA3 supports only DDR3L memory modules. The memory modules in the sockets must be symmetrical - that is, same raw cards and same memory sizes. Therefore, do not use different memory modules in the memory sockets. Doing so may cause system instability or memory errors. Also make sure the memory modules support the data transfer rate of the particular variant.

In addition, when using one memory socket, insert the memory module only in the first memory slot on the conga-TCA3 (top side). If the first memory slot is empty, the SoC will ignore the second memory socket (bottom side). When this happens, the conga-TCA3 will not turn on. See the Intel's Bay Trail datasheet for more information.

2.2 Supported Operating Systems

The conga-TCA3 supports the following operating systems

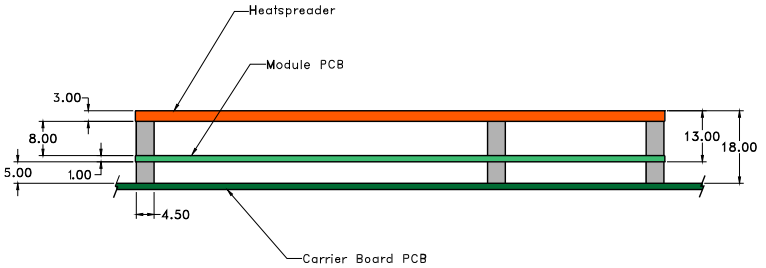
- Microsoft® Windows® 7, 8, 10 (64-bit)
- Microsoft® WES® 7/8
- Microsoft® WEC® 7/2013
- Linux (Timesys Fedora 18)

Note

The conga-TCA3 requires a minimum storage capacity of 16 GB (32-bit) or 20 GB (64-bit) for Windows 7/8/10 installation. congatec will not offer installation support for systems that do not meet the minimum requirement.

2.3 Mechanical Dimensions

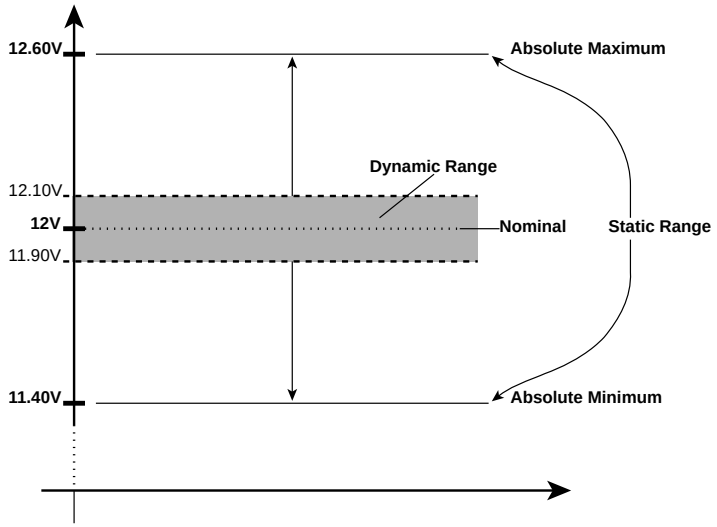
- 95.0 mm x 95.0 mm (3.75" x 3.75")
- Height approximately 18 or 21 mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18 mm. If the 8 mm (height) carrier board connector is used then approximate overall height is 21 mm.



2.4 Supply Voltage Standard Power

- 12V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Ampere)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- Input voltage +12 V
- conga-TCA3 COM
- modified congatec carrier board
- conga-TCA3 cooling solution
- Microsoft Windows 7 (64-bit)

Note

The CPU was stressed to its maximum workload.

Table 5 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	The CPU was stressed to its maximum frequency
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency
S0: Peak value	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	COM is powered by VCC_5V_SBY	
S5	COM is powered by VCC_5V_SBY	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Table 6 Power Consumption Values

The table below provides additional information about the conga-TCA3 power consumption. The values are recorded at various operating mode.

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64-bit)	CPU			Current (A)			
					Variant	Cores	Freq/Turbo (GHz)	S0:Min	S0:Max	S0: Peak	S3
047300 047310	2 x 2 GB	A.0	TA30R000	Windows 7	Intel® Atom™ E3845	4	1.91 / N.A	0.40	1.01	1.08	0.17
047301 047311	2 x 2 GB	A.0	TA30R000	Windows 7	Intel® Atom™ E3827	2	1.75 / N.A	0.39	0.81	0.84	0.17
047302	2 x 2 GB	A.0	TA30R000	Windows 7	Intel® Atom™ E3826	2	1.46 / N.A	0.38	0.75	0.75	0.17
047303	1 x 2 GB	A.0	TA30R000	Windows 7	Intel® Atom™ E3825	2	1.33 / N.A	0.36	0.63	0.65	0.17
047304 047314	1 x 2 GB	A.0	TA30R000	Windows 7	Intel® Atom™ E3815	1	1.46 / N.A	0.35	0.53	0.59	0.18
047305	1 x 2 GB	A.0	TA30R000	Windows 7	Intel® Celeron® J1900	4	2.00 / 2.42	0.40	1.33	1.33	0.18

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 7 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	N.A µA
20°C	3V DC	1.85 µA
70°C	3V DC	N.A µA

Note

1. *Do not use the CMOS battery power consumption value listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-TCA3.*

2.7 Environmental Specifications

Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to +85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

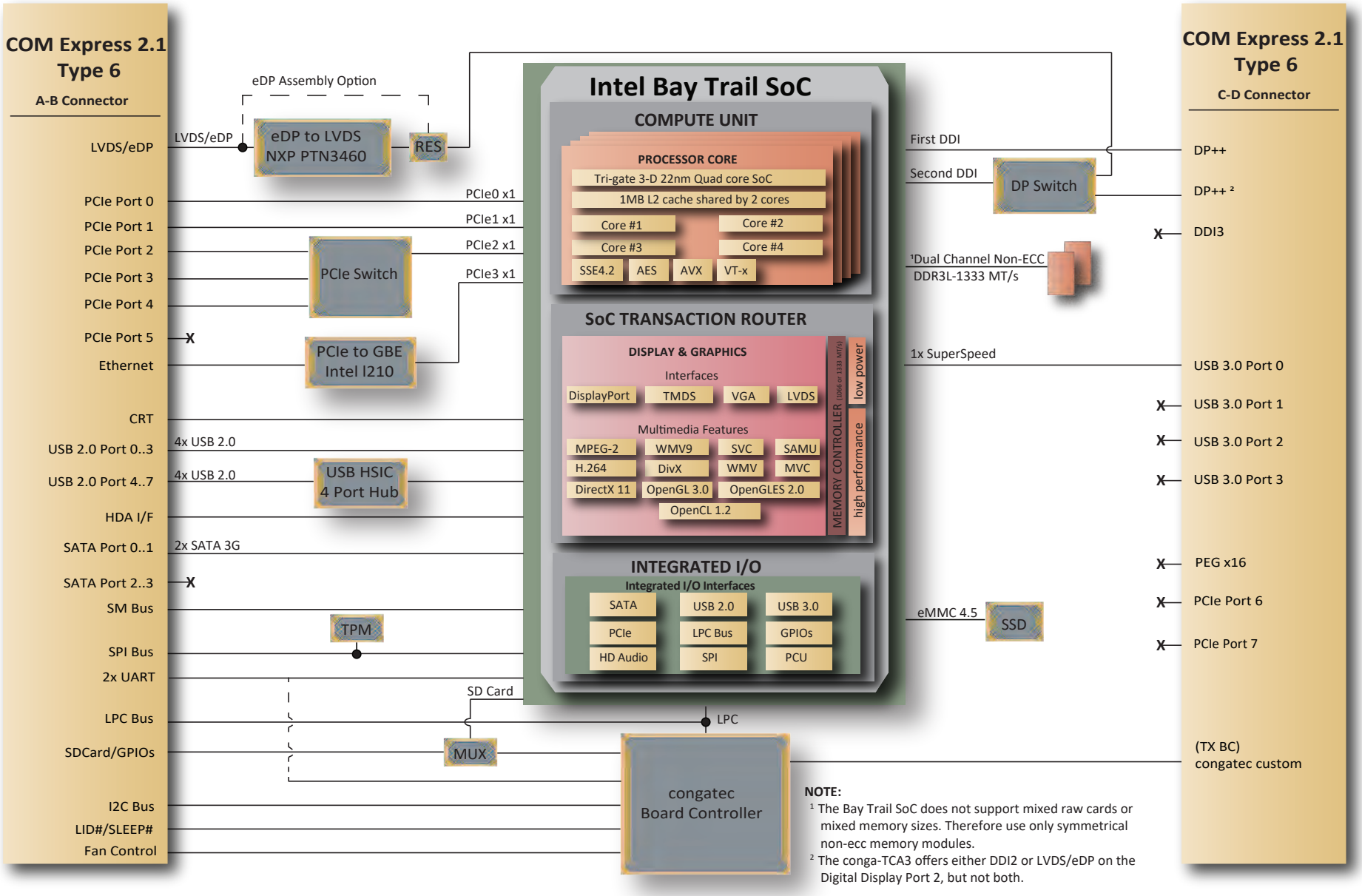
Humidity specifications are for non-condensing conditions.

Note

For long term storage of the conga-TCA3 (more than six months), keep the conga-TCA3 in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

We do not recommend storing the conga-TCA3 for more than five years under these conditions.

3 Block Diagram



NOTE:

[1] The Bay Trail SoC does not support mixed raw cards or mixed memory sizes. Therefore use only symmetrical non-ecc memory modules.

[2] The conga-TCA3 offers either DDI2 or LVDS/eDP on the Digital Display Port 2, but not both.

4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-TCA3. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 8 Cooling Solution Variants

	Cooling Solution	Part No.	Description
1	HSP	047350	Standard heatspreader with M2.5 mm threaded standoffs
		047351	Standard heatspreader with 2.7 mm bore-hole standoffs
2	CSP	047352	Standard passive cooling solution with M2.5 mm threaded standoffs
		047353	Standard passive cooling solution with 2.7 mm bore-hole standoffs

Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*

2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

3. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

Caution

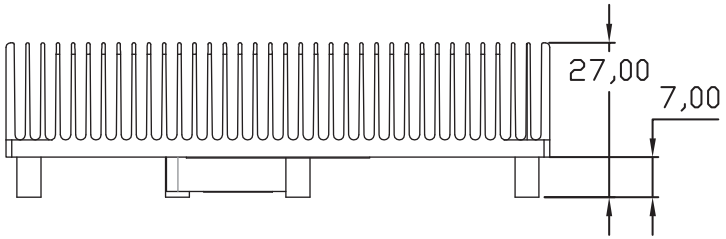
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

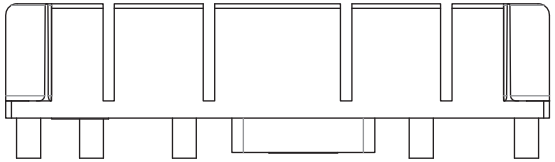
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

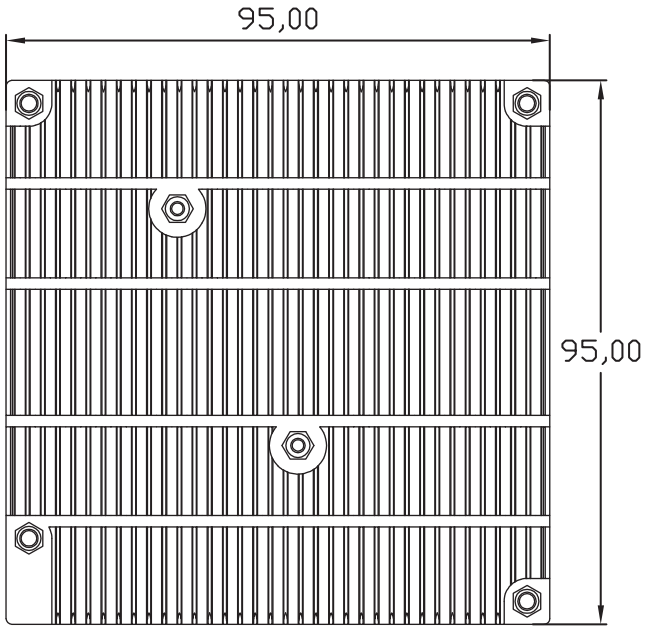
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

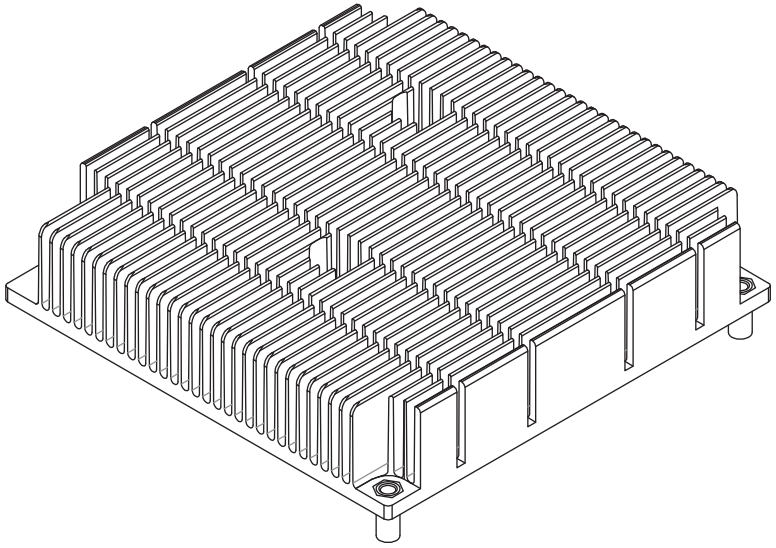
4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

4.1 CSP Dimensions

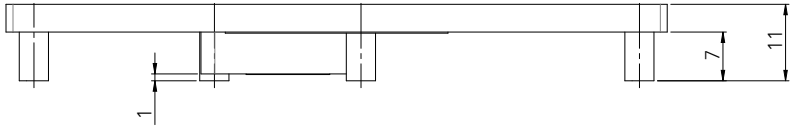


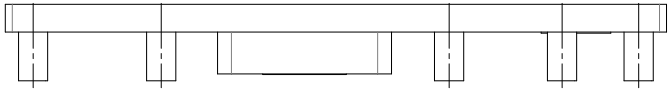


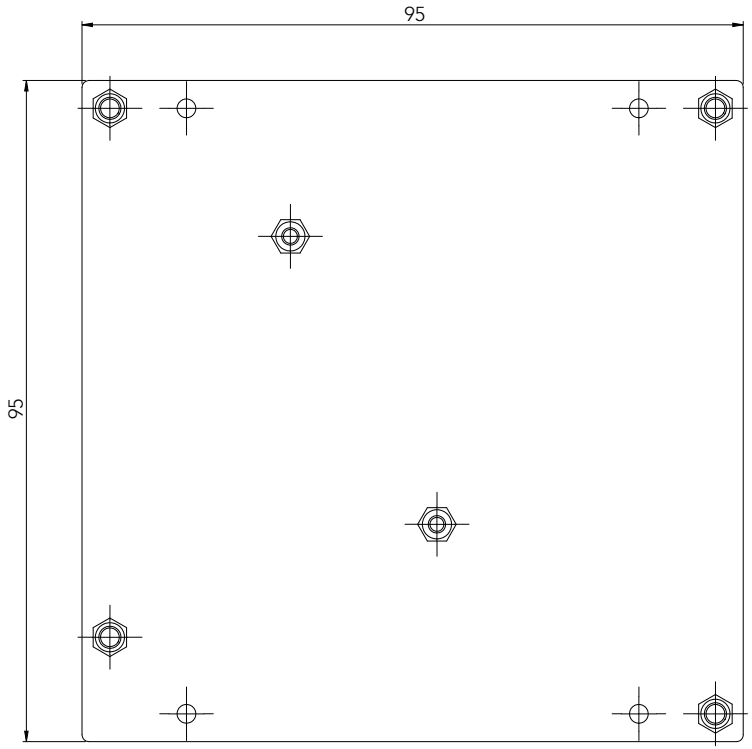


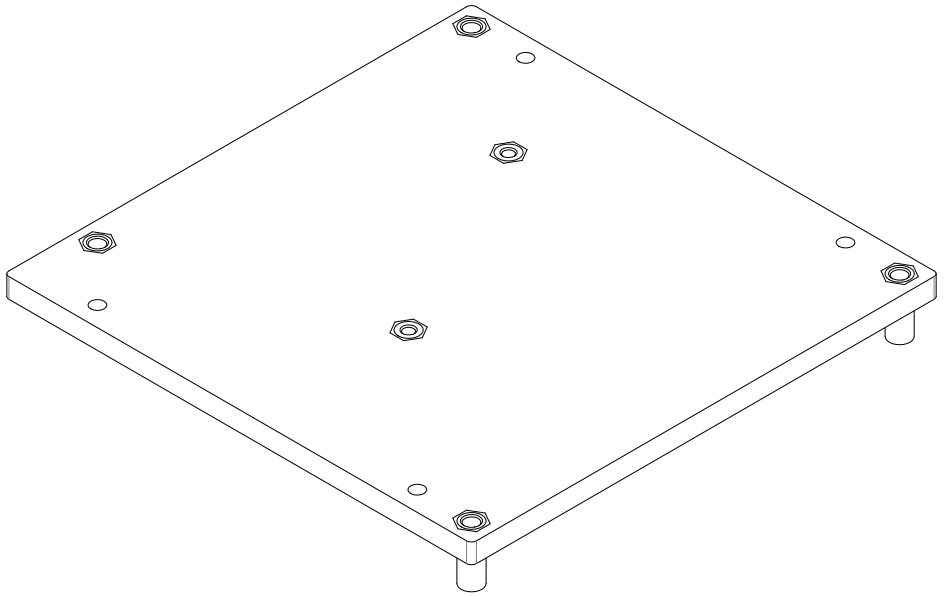


4.2 HSP Dimensions









5 Connector Rows

The conga-TCA3 is connected to the carrier board via two 220-pin connectors (COM Express Type 6 pinout). These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

5.1 Primary and Secondary Connector Rows

The following subsystems can be found on the primary and secondary connector rows.

5.1.1 PCI Express™

The conga-TCA3 offers five PCIe lanes on the A–B connector. The lanes support:

- up to 5 GTps (Gen 2) speed
- a 5 x1 link configuration
- a 3 x1 + 1 x2 link via a special/customized BIOS firmware
- PCI Express Specification 2.0

5.1.2 Display Interfaces

The conga-TCA3 supports the following:

- up to two DP++
- single- or dual-channel LVDS
- VGA
- up to two independent displays (display combination must be 2x DP++ or 1x DP++ plus 1x LVDS or 1x VGA)

Note

1. *The second DDI interface (DP++) is multiplexed with the LVDS interface and configurable via the BIOS setup menu.*
2. *The conga-TCA3 will support only one DP++ if LVDS is enabled in the BIOS setup menu.*

The table below shows the supported display combinations and resolutions.

Table 9 Display Combination

Display 1	Display 2	Display 1 (Max. Resolution)	Display 2 (Max. Resolution)
DP++	LVDS or Optional DP++	1920x1200 @60Hz (TMDS) 2560x1600 @60Hz (DP)	1920x1200 @60Hz (dual LVDS mode)
DP++	VGA	1920x1200 @60Hz (TMDS) 2560x1600 @60Hz (DP)	2560x1600 @60Hz
VGA	LVDS or Optional DP++	2560x1600 @60Hz	1920x1200 @60Hz (dual LVDS mode)

5.1.2.1 DisplayPort (DP)

The conga-TCA3 supports:

- up to two DP ports (dedicated DP port by default and optional DP port via the BIOS setup menu)
- VESA DisplayPort Standard 1.1a
- up to 2560x1600 resolutions at 60 Hz

Note

You can configure the optional (second) DP port only if LVDS is disabled in the BIOS setup menu.

5.1.2.2 LVDS

The conga-TCA3 offers a single/dual channel LVDS interface on the A–B connector rows. The interface is provided by routing the onboard PTN3460 to the SoC's second Digital Display Interface, via a DisplayPort switch. The conga-TCA3 can be configured in the BIOS to support either LVDS on the A–B connector or a second Digital Display Interface on the C-D connector.

The LVDS interface supports:

- single or dual channel LVDS (color depths of 18 bpp or 24 bpp)
- integrated flat panel interface with clock frequency up to 112 MHz
- VESA and OpenLDI LVDS color mappings
- automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3
- resolution up to 1920x1200 in dual LVDS bus mode

Note

The optional DDI interface (DDI2) will not function if LVDS is enabled in the BIOS setup menu.

5.1.3 VGA

The conga-TCA3 offers one VGA interface on the A–B connector rows. The VGA port provides RGB signal output as well as HSYNC and VSYNC signal, with dedicated DDC signal pair.

The analog VGA display interface has a RAM-based Digital-to-Analog Converter (RAMDAC). The 320 MHz RAMDAC integrated in the SoC supports resolution up to 2560 x 1600 at 60 Hz refresh rate.

5.1.4 Serial ATA™ (SATA)

The conga-TCA3 offers two SATA interfaces on the A–B connector. The interfaces support:

- independent DMA operation
- data transfer rates up to 3.0 Gb/s
- legacy and AHCI mode

5.1.5 USB 2.0

The conga-TCA3 offers eight USB 2.0 interfaces on connector rows A–B. Four of these ports are routed directly from the SoC to the A–B connector.The other four ports are routed to the A–B connector via a 4-port USB HSIC hub.

The EHCI host controller in the SoC supports these interfaces with high-speed, full-speed and low-speed USB signalling. The controller complies with USB standard 1.1 and 2.0. For more information about how the USB host controllers are routed, see section 7.3 "USB Port Mapping".

Note

According to an Intel Errata, the SoC's HSIC port 0 is reset and re-enumerated when a device is connected or disconnected from USB port 0 during runtime. For this reason, end users should not disconnect or connect any USB device to USB port 0 at runtime. Doing so may cause USB ports 4-7 (ports routed via USB 2.0 hub) to malfunction.

5.1.6 USB 3.0

The conga-TCA3 offers one USB SuperSpeed differential signal on the C–D connector. This interface is controlled by an xHCI host controller in the SoC. The host controller allows data transfers of up to 5 Gb/s and supports SuperSpeed, high-speed, full-speed and low-speed USB signalling. See section 7.3 "USB Port Mapping" for more information.

Note

The USB 3.0 port should be paired with USB 2.0 port 0 on the carrier board.

5.1.7 Gigabit Ethernet

The conga-TCA3 offers a Gigabit Ethernet interface on connector rows A–B via the onboard Intel® I210 Gigabit Ethernet controller. This controller is connected to the Intel® Bay Trail SoC through the fourth PCI Express lane.

5.1.8 HDA Interface

The conga-TCA3 provides an interface that supports the connection of HDA audio codecs.

5.1.9 UART

The conga-TCA3 offers two UART interfaces. The interfaces do not support hardware handshaking and flow control.

Note

The onboard UART cannot be used in combination with an external, SuperIO based UART. They are mutually exclusive. The first UART is implemented as a legacy compatible UART while the second is implemented as HSUART. The HSUART is not legacy compatible. Compared with a legacy UART, it is limited in its feature set and requires a dedicated driver.

5.1.10 ExpressCard™

The conga-TCA3 supports the implementation of ExpressCards, which requires the dedication of one USB port and a x1 PCI Express link for each ExpressCard used.

5.1.11 SD Card

The conga-TCA3 offers a 4-bit SD interface for SD/MMC cards on the A–B connector. The SD signals are multiplexed with GPIO signals and controlled by the congatec Board Controller. The SD card controller in the Storage Control Cluster of the SoC supports the SD interface with up to 832 Mb/s data rate, using four parallel data lines.

5.1.12 LPC Bus

The conga-TCA3 offers the LPC (Low Pin Count) bus on the A–B connector. For more information about the decoded LPC addresses, see section 9.1.1 "LPC Bus".

Note

The conga-TCA3 Atom variants operate at 33 MHz and the Celeron variants at 25 MHz.

5.1.13 I²C Bus

The I²C bus is implemented through the congatec board controller. It provides a fast-mode, multi-master I²C bus at maximum I²C bandwidth.

5.1.14 SPI

The conga-TCA5 supports SPI interface. This interface makes it possible to boot from an external SPI flash (alternative interface for the BIOS flash device).

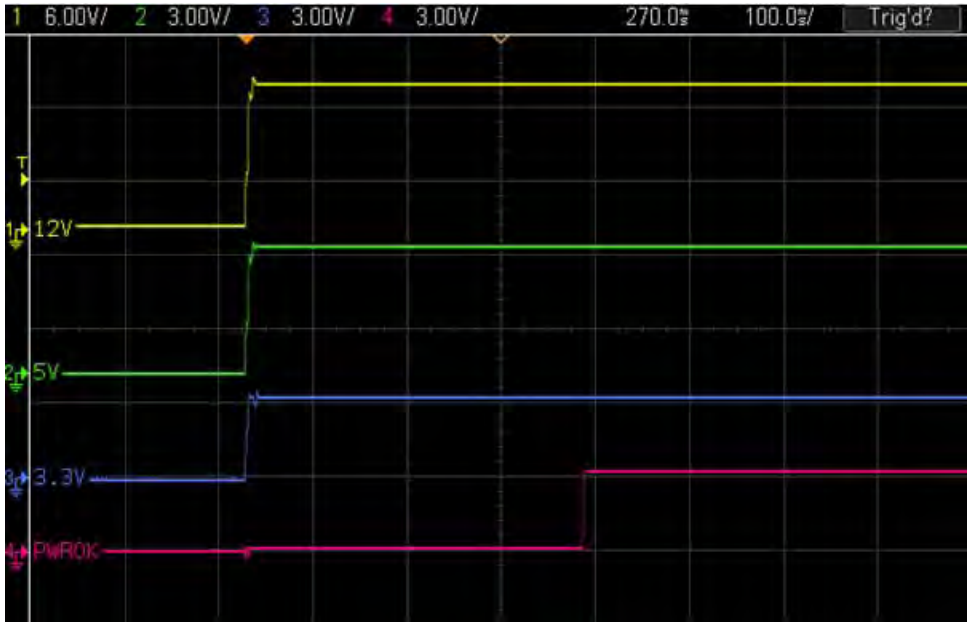
5.1.15 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100 ms) after all carrier board power rails are up, to ensure a stable system.

A sample screenshot is shown below.



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The conga-TCA3 provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-TCA3's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

The 12 volt input power is the sole operational power source for the conga-TCA3. Other required voltages are generated internally on the module using onboard voltage regulators.

Note

When designing a power supply for a conga-TCA3 application, be aware that the system may malfunction when a 12V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.

The cause of this problem is that some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.

To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope, during the power supply qualication phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

5.1.16 Power Management

ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).

6 Additional Features

6.1 Optional eMMC 4.5

The conga-TCA3 offers an optional eMMC 4.5 flash onboard the Intel Atom variants. Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology.

The performance of the newer eMMC may vary depending on the eMMC technology.

Note

1. *For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions."*

2. *The conga-TCA3 Celeron variants do not offer eMMC*

6.2 Low Voltage Memory (DDR3L)

The Bay Trail SoC on the conga-TCA3 offers a low voltage memory interface. The memory interface supports 1.35 volts and unbuffered DDR3L SO-DIMMs. By leveraging this feature set, the conga-TCA3 offers a system optimized for lowest possible power consumption.

Note

The conga-TCA3 supports only DDR3L memory modules. The memory modules in the sockets must be symmetrical - that is, same raw cards and same memory sizes. Therefore, do not use different memory modules in the memory sockets. Doing so may cause system instability or memory errors. Also make sure the memory modules support the data transfer rate of the particular variant.

In addition, when using one memory socket, insert the memory module only in the first memory slot on the conga-TCA3 (top side). If the first memory slot is empty, the SoC will ignore the second memory socket (bottom side). When this happens, the conga-TCA3 will not turn on. See the Intel's Bay Trail datasheet for more information.

6.3 congatec Board Controller (cBC)

The conga-TCA3 is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRBI microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

6.3.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.3.2 General Purpose Input/Output

The conga-TCA3 offers general purpose inputs and outputs for custom system design. These GPIOs are multiplexed with SD signals and are controlled by the cBC.

6.3.3 Fan Control

The conga-TCA3 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

1. *Use a 4-wire fan to generate the correct speed readout.*

2. *For the correct fan control implementation (FAN_PWMOUT, FAN_TACHIN), see the COM Express Design Guide.*

6.3.4 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The term “power loss” implies that all power sources, including the standby power are lost (G3 state). Once power loss (transition to G3) or shutdown (transition to S5) occurs, the board controller continuously monitors the standby power rail. If the standby voltage remains stable for 30 seconds, the cBC assumes the system was switched off properly. If the standby voltage is no longer detected within 30 seconds, the module considers this an AC power loss condition.

The power loss control feature has three different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to “ON”.*
2. *The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.*
3. *The 30 seconds monitoring cycle applies only to the “Last State” power loss control mode.*

6.3.4.1 Watchdog

The conga-TCA3 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-TCA3 does not support external hardware triggering.

For more information about the Watchdog feature, see section 10.4.1 "Watchdog Submenu" and also application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

Note

The conga-TCA3 module does not support the watchdog NMI mode. COM Express type 6 modules do not support the PCI bus and therefore the PCI_SERR# signal is not available. There is no way to drive an NMI to the processor without the presence of the PCI_SERR# PCI bus signal.

6.3.5 I²C Bus

The conga-TCA3 offers support for the frequently used I²C bus. Thanks to the I²C host controller in the cBC the I²C bus is multimaster capable and runs at fast mode.

6.4 OEM BIOS Customization

The conga-TCA3 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

6.4.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.4.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.4.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.4.4 OEM BIOS Code/Data

With the congatec embedded BIOS it is possible for system designers to add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table (OA2.0), Windows 8 OEM activation (OA3.0), verb tables for HDA codecs, PCI/PCIe opROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is only called when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.4.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.5 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for any additional modifications to the system BIOS.

In addition to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-TCA5 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface, contact your local sales representative.

6.6 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website.

6.7 Optional TPM

The conga-TCA3 can be equipped optionally with a "Trusted Platform Module" (TPM 1.2).

6.8 Suspend to Ram

The Suspend to RAM feature is available on the conga-TCA3.

7 conga Tech Notes

The conga-TCA3 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

7.1 Intel SoC Features

7.1.1 Intel Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel VT and is verified on all current congatec x86 hardware.

Note

congatec supports RTS Hypervisor.

7.1.2 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-TCA3 ACPI thermal solution offers two different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the “passive cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.2 ACPI Suspend Modes and Resume Events

The conga-TCA3 BIOS supports S3 (Suspend to RAM). The BIOS does not support S4 (Suspend to Disk) even though the following operating systems support it (S4_OS = Hibernate):

- Windows 7, Windows Vista, Linux

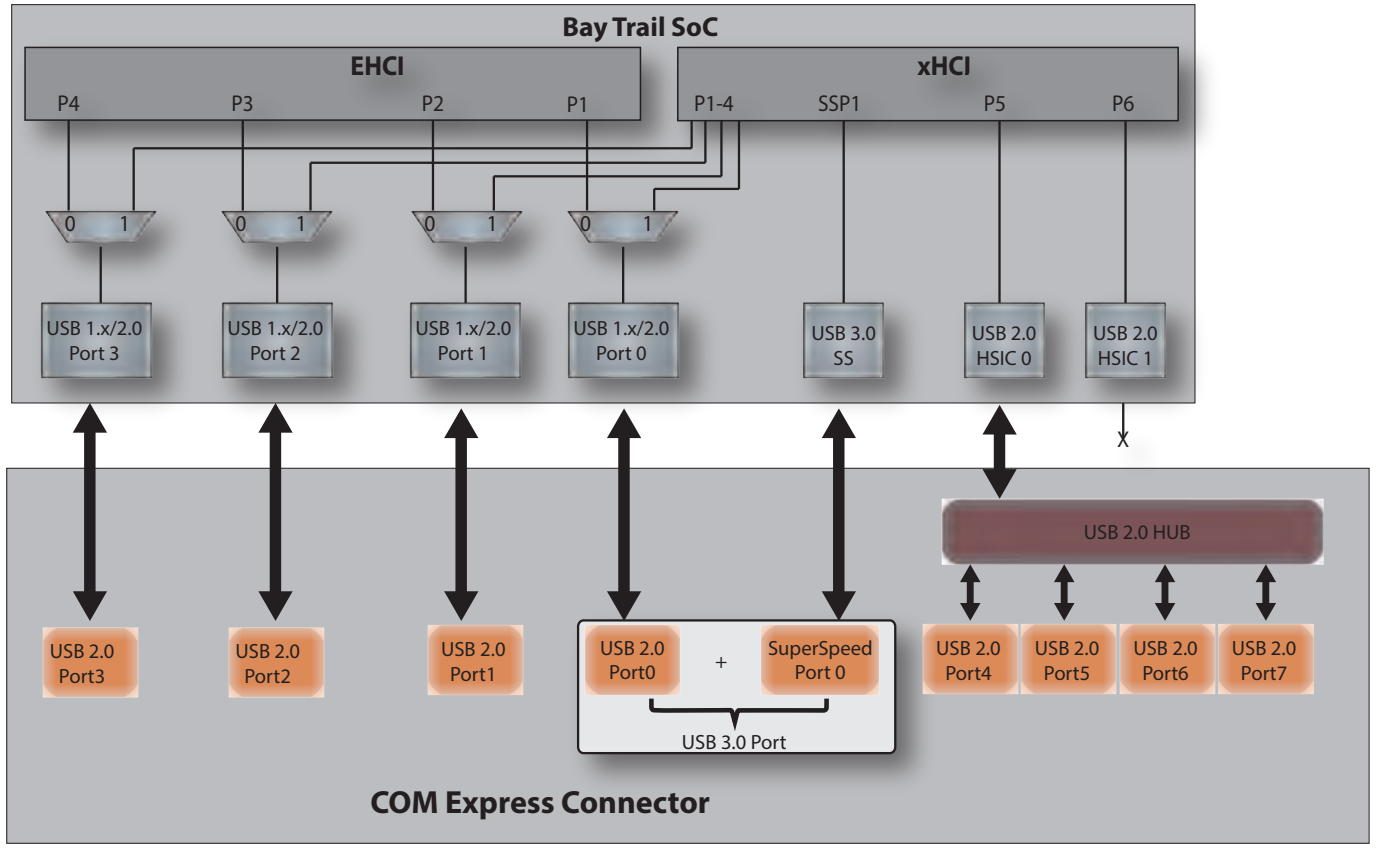
For more information about ACPI, see section 10.4.8 "ACPI Submenu".

Table 10 Wake Events

The table below lists the events that wake the system from S3.

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5
Onboard LAN Event	Device driver must be configured for Wake On LAN support
SMBALERT#	Wakes unconditionally from S3-S5
PCI Express WAKE#	Wakes unconditionally from S3-S5
WAKE#	Wakes unconditionally from S3
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu (only available in S5)
Watchdog Power Button Event	Wakes unconditionally from S3-S5

7.3 USB Port Mapping



NOTE:

Possible USB configurations are:

(*) Up to 8x USB 2.0
(*) Up to 7x USB 2.0 and 1x USB 3.0

Note

An Intel Errata states that the SoC's HSIC port 0 is reset and re-enumerated when a device is connected or disconnected from USB port 0 during runtime. Therefore, end users should not disconnect or connect any USB device to USB port 0 at runtime. Doing so may cause USB ports 4-7 (ports routed via USB 2.0 hub) to malfunction.

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type VI connectors used for congatec GmbH modules. The pinout of the modules complies with COM Express Type 6.0 Rev. 2.1.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 11 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
SATA	In compliance with Serial ATA specification, Revision 3.0
REF	Reference voltage output. May be sourced from a module power plane
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

8.1 Connector Signal Descriptions

Table 12 Connector A–B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+ (*)	B22	SATA3_TX+ (*)	A77	LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX- (*)	B23	SATA3_TX- (*)	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+ (*)	B25	SATA3_RX+ (*)	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX- (*)	B26	SATA3_RX- (*)	A81	LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2 (*)	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA_BITCLK	B32	SPKR	A87	RSVD	B87	VCC_5V_SBY
A33	AC/HDA_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98		B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+ (*)	B52	PCIE_RX5+ (*)	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5- (*)	B53	PCIE_RX5- (*)	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga TCA3.

Table 13 Connector C–D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1- (*)	D56	PEG_TX1- (*)
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+ (*)	D58	PEG_TX2+ (*)
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2- (*)	D59	PEG_TX2- (*)
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1- (*)	D6	USB_SSTX1- (*)	C61	PEG_RX3+ (*)	D61	PEG_TX3+ (*)
C7	USB_SSRX1+ (*)	D7	USB_SSTX1+ (*)	C62	PEG_RX3- (*)	D62	PEG_TX3- (*)
C8	GND	D8	GND	C63	RSVD	D63	RSVD
C9	USB_SSRX2- (*)	D9	USB_SSTX2- (*)	C64	RSVD	D64	RSVD
C10	USB_SSRX2+ (*)	D10	USB_SSTX2+ (*)	C65	PEG_RX4+ (*)	D65	PEG_TX4+ (*)
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4- (*)	D66	PEG_TX4- (*)
C12	USB_SSRX3- (*)	D12	USB_SSTX3- (*)	C67	RSVD	D67	GND
C13	USB_SSRX3+ (*)	D13	USB_SSTX3+ (*)	C68	PEG_RX5+ (*)	D68	PEG_TX5+ (*)
C14	GND	D14	GND	C69	PEG_RX5- (*)	D69	PEG_TX5- (*)
C15	DDI1_PAIR6+ (*)	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	DDI1_PAIR6- (*)	D16	DDI1_CTRLDATA_AUX-	C71	PEG_RX6+ (*)	D71	PEG_TX6+ (*)
C17	RSVD	D17	RSVD	C72	PEG_RX6- (*)	D72	PEG_TX6- (*)
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	PCIE_RX6+ (*)	D19	PCIE_TX6+ (*)	C74	PEG_RX7+ (*)	D74	PEG_TX7+ (*)
C20	PCIE_RX6- (*)	D20	PCIE_TX6- (*)	C75	PEG_RX7- (*)	D75	PEG_TX7- (*)
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+ (*)	D22	PCIE_TX7+ (*)	C77	RSVD	D77	RSVD
C23	PCIE_RX7- (*)	D23	PCIE_TX7- (*)	C78	PEG_RX8+ (*)	D78	PEG_TX8+ (*)
C24	DDI1_HPD	D24	RSVD	C79	PEG_RX8- (*)	D79	PEG_TX8- (*)
C25	DDI1_PAIR4+ (*)	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	DDI1_PAIR4- (*)	D26	DDI1_PAIR0+	C81	PEG_RX9+ (*)	D81	PEG_TX9+ (*)
C27	RSVD	D27	DDI1_PAIR0-	C82	PEG_RX9- (*)	D82	PEG_TX9- (*)
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD
C29	DDI1_PAIR5+ (*)	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	DDI1_PAIR5- (*)	D30	DDI1_PAIR1-	C85	PEG_RX10+ (*)	D85	PEG_TX10+ (*)
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- (*)	D86	PEG_TX10- (*)
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-	C88	PEG_RX11+ (*)	D88	PEG_TX11+ (*)
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11- (*)	D89	PEG_TX11- (*)
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+ (*)	D36	DDI1_PAIR3+	C91	PEG_RX12+ (*)	D91	PEG_TX12+ (*)
C37	DDI3_CTRLDATA_AUX- (*)	D37	DDI1_PAIR3-	C92	PEG_RX12- (*)	D92	PEG_TX12- (*)
C38	DDI3_DDC_AUX_SEL (*)	D38	RSVD	C93	GND	D93	GND
C39	DDI3_PAIR0+ (*)	D39	DDI2_PAIR0+	C94	PEG_RX13+ (*)	D94	PEG_TX13+ (*)
C40	DDI3_PAIR0- (*)	D40	DDI2_PAIR0-	C95	PEG_RX13- (*)	D95	PEG_TX13- (*)
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+ (*)	D42	DDI2_PAIR1+	C97	RVSD	D97	RSVD
C43	DDI3_PAIR1- (*)	D43	DDI2_PAIR1-	C98	PEG_RX14+ (*)	D98	PEG_TX14+ (*)
C44	DDI3_HPD (*)	D44	DDI2_HPD	C99	PEG_RX14- (*)	D99	PEG_TX14- (*)
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+ (*)	D46	DDI2_PAIR2+	C101	PEG_RX15+ (*)	D101	PEG_TX15+ (*)
C47	DDI3_PAIR2- (*)	D47	DDI2_PAIR2-	C102	PEG_RX15- (*)	D102	PEG_TX15- (*)
C48	RSVD	D48	RSVD	C103	GND	D103	GND
C49	DDI3_PAIR3+ (*)	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3- (*)	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+ (*)	D52	PEG_TX0+ (*)	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0- (*)	D53	PEG_TX0- (*)	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV#	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+ (*)	D55	PEG_TX1+ (*)	C110	GND (FIXED)	D110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-TCA3.

Table 14 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair	I PCIE		Not supported
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair	O PCIE		Not supported
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair	I PCIE		Not supported.
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair	O PCIE		Not supported.
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair	I PCIE		Not supported.
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair	O PCIE		Not supported.
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 15 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs. *Note: Can also be used as PCI Express Receive Input differential pairs 16 through 31 known as PCIE_RX[16-31] + and -.*	I PCIE		Not supported
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+ PEG_TX0- PEG_TX1+ PEG_TX1- PEG_TX2+ PEG_TX2- PEG_TX3+ PEG_TX3- PEG_TX4+ PEG_TX4- PEG_TX5+ PEG_TX5- PEG_TX6+ PEG_TX6- PEG_TX7+ PEG_TX7- PEG_TX8+ PEG_TX8- PEG_TX9+ PEG_TX9- PEG_TX10+ PEG_TX10- PEG_TX11+ PEG_TX11- PEG_TX12+ PEG_TX12- PEG_TX13+ PEG_TX13- PEG_TX14+ PEG_TX14- PEG_TX15+ PEG_TX15-	D52 D53 D55 D56 D58 D59 D61 D62 D65 D66 D68 D69 D71 D72 D74 D75 D78 D79 D81 D82 D85 D86 D88 D89 D91 D92 D94 D95 D98 D99 D101 D102	PCI Express Graphics Transmit Output differential pairs. *Note: Can also be used as PCI Express Transmit Output differential pairs 16 through 31 known as PCIE_TX[16-31] + and -*	O PCIE		Not supported
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order	I		Not supported

Note

The conga-TCA3 does not support PCI Express Graphics.

Table 16 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with SDVO1_RED+, DP1_LANE0+ and TMDS1_DATA2+ Multiplexed with SDVO1_RED-, DP1_LANE0- and TMDS1_DATA2-	O PCIE		Only TMDS/DP option, no SDVO
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with SDVO1_GRN+, DP1_LANE1+ and TMDS1_DATA1+ Multiplexed with SDVO1_GRN-, DP1_LANE1- and TMDS1_DATA1-	O PCIE		Only TMDS/DP option, no SDVO
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with SDVO1_BLU+, DP1_LANE2+ and TMDS1_DATA0+ Multiplexed with SDVO1_BLU-, DP1_LANE2- and TMDS1_DATA0-	O PCIE		Only TMDS/DP option, no SDVO
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with SDVO1_CK+, DP1_LANE3+ and TMDS1_CLK+ Multiplexed with SDVO1_CK-, DP1_LANE3- and TMDS1_CLK-	O PCIE		Only TMDS/DP option, no SDVO
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	Multiplexed with SDVO1_INT+ Multiplexed with SDVO1_INT-			Not supported due to missing SDVO support
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	Multiplexed with SDVO1_TVCLKIN+ Multiplexed with SDVO1_TVCLKIN-			Not supported due to missing SDVO support
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	Multiplexed with SDVO1_FLDSTALL+ Multiplexed with SDVO1_FLDSTALL-			Not supported due to missing SDVO support
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD	I 3.3V	PD 1M	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with SDVO1_CTRLCLK, DP1_AUX+ and HDMI1_CTRLCLK DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PD100k @ DP mode, PU 3.0k 3.3V @ HDMI/DVI mode	
DDI1_CTRLDATA_AUX-	D16	Multiplexed with SDVO1_CTRLDATA, DP1_AUX- and HDMI1_ CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PU 100k 3.3V@ DP mode, PU 3.0k 3.3V @ HDMI/DVI mode	Boot strap signal (see note below). Enable strap is already populated
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_ AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+ and TMDS2_DATA2+ Multiplexed with DP2_LANE0- and TMDS2_DATA2-	O PCIE		
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+ and TMDS2_DATA1+ Multiplexed with DP2_LANE1- and TMDS2_DATA1-	O PCIE		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+ and TMDS2_DATA0+ Multiplexed with DP2_LANE2- and TMDS2_DATA0-	O PCIE		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+ and TMDS2_CLK+ Multiplexed with DP2_LANE3- and TMDS2_CLK-	O PCIE		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD	I 3.3V	PD 1M	

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+ and HDMI2_CTRLCLK DP AUX+ function if DDI2_DDC_AUX_SEL is no connect HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PD100k @ DP mode, PU 3.0k 3.3V @ HDMI/DVI mode	
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA DP AUX- function if DDI2_DDC_AUX_SEL is no connect HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V	PU 100k 3.3V@ DP mode, PU 3.0k 3.3V @ HDMI/DVI mode	Boot strap signal (see note below). Enable strap is already populated
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_ AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V	PD 1M	
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+ Multiplexed with DP3_LANE0- and TMDS3_DATA2-	O PCIE		Not supported
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+ Multiplexed with DP3_LANE1- and TMDS3_DATA1-	O PCIE		Not supported
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+ Multiplexed with DP3_LANE2- and TMDS3_DATA0-	O PCIE		Not supported
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+ Multiplexed with DP3_LANE3- and TMDS3_CLK-	O PCIE		Not supported
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD	I 3.3V		Not supported
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK DP AUX+ function if DDI3_DDC_AUX_SEL is no connect HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V		Not supported
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA DP AUX- function if DDI3_DDC_AUX_SEL is no connect HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high	I/O PCIE I/O OD 3.3V		Not supported
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_ AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals	I 3.3V		Not supported

Note

1. *Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.2 "Boot Strap Signals".*

2. *The second DDI channel (DDI2) is only available if LVDS is not enabled. Refer to the TMDS and DisplayPort signal description tables in this section for information about the signals routed to the DDI interface of the COM Express connector.*

Table 17 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS1_CLK + TMDS1_CLK -	D36 D37	TMDS Clock output differential pair Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-	O PCIE		
TMDS1_DATA0+ TMDS1_DATA0-	D32 D33	TMDS differential pair Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-	O PCIE		
TMDS1_DATA1+ TMDS1_DATA1-	D29 D30	TMDS differential pair Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-	O PCIE		
TMDS1_DATA2+ TMDS1_DATA2-	D26 D27	TMDS differential pair Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-	O PCIE		
HDMI1_HPD	C24	TMDS Hot-plug detect Multiplexed with DDI1_HPD	I PCIE	PD 1M	
HDMI1_CTRLCLK	D15	TMDS I²C Control Clock Multiplexed with DDI1_CTRLCLK_AUX+	I/O OD 3.3V	PU 3.0k 3.3V	
HDMI1_CTRLDATA	D16	TMDS I²C Control Data Multiplexed with DDI1_CTRLDATA_AUX-	I/O OD 3.3V	PU 3.0k 3.3V	Boot strap signal (see note below). Enable strap is already populated
TMDS2_CLK + TMDS2_CLK -	D49 D50	TMDS Clock output differential pair Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		
TMDS2_DATA0+ TMDS2_DATA0-	D46 D47	TMDS differential pair Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		
TMDS2_DATA1+ TMDS2_DATA1-	D42 D43	TMDS differential pair Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		
TMDS2_DATA2+ TMDS2_DATA2-	D39 D40	TMDS differential pair Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-	O PCIE		
HDMI2_HPD	D44	TMDS Hot-plug detect Multiplexed with DDI2_HPD	I PCIE	PD 1M	
HDMI2_CTRLCLK	C32	TMDS I²C Control Clock Multiplexed with DDI2_CTRLCLK_AUX+	I/O OD 3.3V	PU 3.0k 3.3V	
HDM12_CTRLDATA	C33	TMDS I²C Control Data Multiplexed with DDI2_CTRLDATA_AUX-	I/O OD 3.3V	PU 3.0k 3.3V	Boot strap signal (see note below). Enable strap is already populated
TMDS3_CLK + TMDS3_CLK -	C49 C50	TMDS Clock output differential pair Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-	O PCIE		Not supported
TMDS3_DATA0+ TMDS3_DATA0-	C46 C47	TMDS differential pair Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-	O PCIE		Not supported
TMDS3_DATA1+ TMDS3_DATA1-	C42 C43	TMDS differential pair Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-	O PCIE		Not supported
TMDS3_DATA2+ TMDS3_DATA2-	C39 C40	TMDS differential pair Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-	O PCIE		Not supported

Signal	Pin #	Description	I/O	PU/PD	Comment
HDMI3_HPD	C44	TMDS Hot-plug detect Multiplexed with DDI3_HPD	I PCIE		Not supported
HDMI3_CTRLCLK	C36	TMDS I²C Control Clock Multiplexed with DDI3_CTRLCLK_AUX+	I/O OD 3.3V		Not supported
HDMI3_CTRLDATA	C37	TMDS I²C Control Data Multiplexed with DDI3_CTRLDATA_AUX-	I/O OD 3.3V		Not supported

Note

1. *Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.2 "Boot Strap Signals".*

2. *The second TMDS interface is only available if LVDS is disabled.*

3. *The conga-TCA3 does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.*

Table 18 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE3+ DP1_LANE3-	D36 D37	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-	O PCIE		
DP1_LANE2+ DP1_LANE2-	D32 D33	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-	O PCIE		
DP1_LANE1+ DP1_LANE1-	D29 D30	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-	O PCIE		
DP1_LANE0+ DP1_LANE0-	D26 D27	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-	O PCIE		
DP1_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI1_HPD	I 3.3V	PD 1M	
DP1_AUX+	D15	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O PCIE	PD 100k	
DP1_AUX-	D16	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O PCIE	PU 100k 3.3V	Boot strap signal (see note below). Enable strap is already populated
DP2_LANE3+ DP2_LANE3-	D49 D50	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O PCIE		
DP2_LANE2+ DP2_LANE2-	D46 D47	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
DP2_LANE1+ DP2_LANE1-	D42 D43	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O PCIE		
DP2_LANE0+ DP2_LANE0-	D39 D40	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI2_PAIR0+ and DDI1_PAIR0-	O PCIE		
DP2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI2_HPD	I 3.3V	PD 1M	
DP2_AUX+	C32	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O PCIE	PD 100k	
DP2_AUX-	C33	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O PCIE	PU 100k 3.3V	Boot strap signal (see note below). Enable strap is already populated
DP3_LANE3+ DP3_LANE3-	C49 C50	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-	O PCIE		Not supported
DP3_LANE2+ DP3_LANE2-	C46 C47	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-	O PCIE		Not supported
DP3_LANE1+ DP3_LANE1-	C42 C43	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-	O PCIE		Not supported
DP3_LANE0+ DP3_LANE0-	C39 C40	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-	O PCIE		Not supported
DP3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer Multiplexed with DDI3_HPD	I 3.3V		Not supported
DP3_AUX+	C36	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O PCIE		Not supported
DP3_AUX-	C37	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O PCIE		Not supported

Note

1. *Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.2 "Boot Strap Signals".*

2. *The second DP interface is only available if LVDS is not enabled.*

Table 19 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load	O Analog	PD 150R	Analog output
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load	O Analog	PD 150R	Analog output
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O OD 5V	PU 4k02 3.3V	
VGA_I2C_DAT	B96	DDC data line	I/O OD 5V	PU 4k02 3.3V	

Table 20 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10k	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10k	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control	O 3.3V	PU 2k0 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control	I/O 3.3V	PU 2k0 3.3V	

Note

The optional DP++ (DDI2) will not function if LVDS is enabled in the BIOS setup menu.

Table 21 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair	I SATA		Supports Serial ATA II specification, up to 3 Gb/s
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair	O SATA		Supports Serial ATA II specification, up to 3 Gb/s
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair	I SATA		Supports Serial ATA II specification, up to 3 Gb/s
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair	O SATA		Supports Serial ATA II specification, up to 3 Gb/s
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair	I SATA		Not supported
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair	O SATA		Not supported
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair	I SATA		Not supported
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair	O SATA		Not supported
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low	I/O 3.3v	PU 4.99k 3.3V	

Table 22 USB 2.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low	I 3.3VSB	PU 4.99k 3.3VSB	Do not pull this line high on the carrier board
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low	I 3.3VSB	PU 4.99k 3.3VSB	Do not pull this line high on the carrier board
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board

Table 23 USB 3.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSRX0-	C3		I		
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSTX0-	D3		O		
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported
USB_SSRX1-	C6		I		Not supported
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported
USB_SSTX1-	D6		O		Not supported
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported
USB_SSRX2-	C9		I		Not supported
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported
USB_SSTX2-	D9		O		Not supported
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I		Not supported
USB_SSRX3-	C12		I		Not supported
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not supported
USB_SSTX3-	D12		O		Not supported

Table 24 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		Twisted pair signals for external transformer
			1000	100	10			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				O 3.3VSB		

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low	O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low	O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.			Not connected

Table 25 Intel® High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	**Intel® High Definition Audio Reset:** This signal is the master hardware reset to external codec(s)	O 3.3V		AC'97 codecs are not supported
AC/HDA_SYNC	A29	**Intel® High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number	O 3.3V		AC'97 codecs are not supported
AC/HDA_BITCLK	A32	**Intel® High Definition Audio Bit Clock Output:** This signal is a 24.000MHz serial data clock generated by the Intel® High Definition Audio controller	O 3.3V		AC'97 codecs are not supported
AC/HDA_SDOUT	A33	**Intel® High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio	O 3.3V		AC'97 codecs are not supported
AC/HDA_SDIN[1:0]	B29-B30	**Intel® High Definition Audio Serial Data In [1:0]:** These signals are serial TDM data inputs from the two codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio	I 3.3V	100k PD	AC'97 codecs are not supported AC/HDA_SDIN2 is not supported

Table 26 ExpressCard Support Pins Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE#	A49	ExpressCard 0 capable card request	I 3.3V	PU 10k 3.3V	
EXCD0_PERST#	A48	ExpressCard 0 Reset	O 3.3V	PU 10k 3.3V	
EXCD1_CPPE#	B48	ExpressCard 1 capable card request	I 3.3V	PU 10k 3.3V	
EXCD1_PERST#	B47	ExpressCard 1 Reset	O 3.3V	PU 10k 3.3V	

Table 27 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V		Not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3V		
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		33 MHz with Bay Trail-I SoC (Intel Atom series) 25 MHz with Bay Trail-M/D SoC (Intel Celeron series)

Table 28 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 69k8 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only	+ 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device	I 3.3VSB	PU 10k 3.3VSB	Carrier shall pull to GND or leave no-connect
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device	I 3.3VSB	PU 10k 3.3VSB	Carrier shall pull to GND or leave no-connect

Table 29 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O 3.3V	PU 2k0 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O 3.3V	PU 2k0 3.3VSB	
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V	PU 4k99 3.3V	
WDT	B27	Output indicating that a watchdog time-out event has occurred	O 3.3V	PD 10k	
FAN_PWMOUT [1,2]	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM	O OD 3.3V		

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_TACHIN [1,2]	B102	Fan tachometer input	I OD	PU 10k 3.3V	Requires a fan with two pulse output
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM	I 3.3V		Trusted Platform Module chip is optional

Note

1. *For fan control implementation, see the COM Express Design Guide*
2. *Protected on the module by a series schotty diode. Therefore, pull-down resistor is required on the carrier board for proper logic level.*

Table 30 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins Shared with SD_CLK. Output from COM Express, input to SD	O 3.3V		
GPO1	B54	General purpose output pins Shared with SD_CMD. Output from COM Express, input to SD	O 3.3V		
GPO2	B57	General purpose output pins Shared with SD_WP. Output from COM Express, input to SD	O 3.3V		
GPO3	B63	General purpose output pins Shared with SD_CD. Output from COM Express, input to SD	O 3.3V		
GPI0	A54	General purpose input pins. Pulled high internally on the module Shared with SD_DATA0. Bidirectional signal	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode
GPI2	A67	General purpose input pins. Pulled high internally on the module Shared with SD_DATA2. Bidirectional signal	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode
GPI3	A85	General purpose input pins. Pulled high internally on the module Shared with SD_DATA3. Bidirectional signal	I 3.3V	PU 10K 3.3V	Pull-up only active in GPIO mode

Table 31 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low. Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good	I 3.3V		Set by resistor divider to accept 3.3V
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices	O 3.3VSB	PU 10k 3.3VSB	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON#") may be used to enable the non-standby power on a typical ATX power supply	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state	O 3.3VSB		Not supported by chipset. Shorted with SUS_S4#
WAKE0#	B66	PCI Express wake up signal	I 3.3VSB	PU 4.99k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity	I 3.3VSB	PU 4.99k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event	I 3.3VSB	PU 4.99k 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation	I 3.3V	PU 10k 3.3V	
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown	O 3.3V	PU 10k 3.3V	
SMB_CK	B13	System Management Bus bidirectional clock line	I/O 3.3VSB	PU 4.99k 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line	I/O OD 3.3VSB	PU 4.99k 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system	I 3.3VSB	PU 10k 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch. Note: For proper detection, assert a pulse width of at least 16 ms.	I OD 3.3V	PU 10k 3.3VSB	

Signal	Pin #	Description	I/O	PU/PD	Comment
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again. Note: For proper detection, assert a pulse width of at least 16 ms.	I OD 3.3V	PU 10k 3.3VSB	

Table 32 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX [1]	A98	General purpose serial port transmitter	O 3.3V		
SER1_TX [1]	A101	General purpose serial port transmitter	O 3.3V		
SER0_RX [1]	A99	General purpose serial port receiver	I 3.3V	43.2k 3.3V	
SER1_RX [1]	A102	General purpose serial port receiver	I 3.3V	43.2k 3.3V	

Note

1. *Pins are protected on the module by a series schotty diode. Therefore, pull-down resistor is required on the carrier board for proper logic level.*

Table 33 Module Type Definition Signal Description

Signal	Pin #	Description				I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X).				PDS	TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard. The conga-TCA3 is based on the COM Express Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.
		TYPE2#	TYPE1#	TYPE0#			
		X NC NC NC NC GND	X NC NC GND GND NC	X NC GND NC GND NC	Pinout Type 1 Pinout Type 2 Pinout Type 3 (no IDE) Pinout Type 4 (no PCI) Pinout Type 5 (no IDE, no PCI) Pinout Type 6 (no IDE, no PCI)		
		The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.					

Signal	Pin #	Description		I/O	Comment
TYPE10#	A97	Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed.		PDS	Not connected to indicate "Pinout R2.0"
		TYPE10#			
		NC PD 12V	Pinout R2.0 Pinout Type 10 pull down to ground with 4.7k resistor Pinout R1.0		
		This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7k resistor.			

Table 34 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109 C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110 C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

8.2 Boot Strap Signals

Table 35 Boot Strap Signal Descriptions

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
DDI1_CTRLDATA_AUX- DP1_AUX- HDMI_CTRLDATA	D16	Multiplexed with DP1_AUX- and HDMI1_CTRLDATA. DP AUX- function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3V	PU100k 3.3V	DDI1_CTRLDATA_AUX- is a boot strap signal (see caution statement below).
DDI2_CTRLDATA_AUX- DP2_AUX- HDM2_CTRLDATA	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA. DP AUX- function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE I/O OD 3.3V	PU100k 3.3V	DDI2_CTRLDATA_AUX- is a boot strap signal (see caution statement below).

Caution

1. *The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either COM Express™ internally implemented resistors or chipset internally implemented resistors that are located on the module.*

2. *No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM Express™ module to malfunction and/or cause irreparable damage to the module.*

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-TCA3 module is functionally identical with a standard PC/AT. The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.1.1 LPC Bus

On the conga-TCA3, the Platform Controller Hub (PCH) acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCH and the LPC Bus. Some fixed I/O space ranges seen by the processor are:

Device	IO Address
8259 Master	20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39h, 3Ch-3Dh
8254s	40h-43h, 50h-53h
Ps2 Control	60h, 64h
NMI Controller	61h, 63h, 65h, 67h
RTC	70h-77h
Port 80h	80h-83h
Init Register	92h
8259 Master	A0h- A1h, A4h-A5h, A8h-A9h, Ach-ADh, B0h-B1h, B4h-B5h, B8h-B9h, Bch-BDh, 4D0h-4D1h
PCU UART	3F8h-3FFh
Reset Control	CF9h
Active Power Management	B2h-B3h

Some of these ranges are used by a Super I/O if implemented on the carrier board or are occupied by the COM Express on-module UARTs if these are enabled in the setup. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 36 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	SoC Transaction Router
00h	02h	00h	Graphics and Display
00h	12h	00h	SD Port
00h	13h	00h	SATA
00h	14h	00h	XHCI USB
00h	17h	01h	eMMC 4.5 Port
00h	1Ah	00h	Trusted Execution Engine
00h	1Bh	00h	HD Audio
00h	1Ch	00h	PCI Express Root Port 0
00h	1Ch	01h	PCI Express Root Port 1
00h	1Ch	02h	PCI Express Root Port 2
00h	1Ch	03h	PCI Express Root Port 3
00h	1Dh	00h	EHCI USB
00h	1Fh	00h	LPC: Bridge to Intel Legacy Port
00h	1Fh	03h	SMBus Port
03h	00h	00h	PLX PE8605 PCI Express Bridge
04h	01h	00h	PLX PCI Express Port 0
04h	02h	00h	PLX PCI Express Port 1
04h	03h	00h	PLX PCI Express Port 2
08h	00h	00h	Intel® I210 Ethernet Network

Note

1. *The PCI Express Ports are visible only if they are set to "Enabled" in the BIOS setup program and a device attached to the corresponding PCI Express port on the carrier board.*

2. *The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on the actual configuration of the hardware.*

9.3 PCI Interrupt Routing Map

Table 37 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line [1]	APIC Mode IRQ	Graphic	SD Card	SATA	XHCI	eMMC 4.5 Port	TXE	HD Audio	PCI-EX Root Port 0	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	EHCI USB	SMBus Port	I210 Ethernet Network
A	INTA	16	x	x	x	x	x	x	x	x				x		x [3]
B	INTB	17									x				x	x [4]
C	INTC	18										x				x [5]
D	INTD	19											x			x [2]
E		20														
F		21														
G		22														
H		23														

Note

[1] *These interrupt lines are virtual (message based).*

[2] *Interrupt used by single function PCI Express devices (INTA).*

[3] *Interrupt used by multifunction PCI Express devices (INTB).*

[4] *Interrupt used by multifunction PCI Express devices (INTC).*

[5] *Interrupt used by multifunction PCI Express devices (INTD).*

9.4 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.5 SMBus

System Management (SM) bus signals are connected to the Intel® Baytrail SoC and the SMBus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

10 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

10.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <ESC> key during POST.

10.1.1 Boot Selection Popup

Press the <F11> key during POST to access the Boot Selection Popup menu. A selection menu displays immediately after POST, allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

10.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar, left frame and right frame. The menu bar is shown below:

Main	Advanced	Chipset	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

10.3 Main Setup Screen

When you first enter the BIOS setup, you will see the main setup screen. The main setup screen reports BIOS, processor, memory and board information and is for configuring the system date and time. You can always return to the main setup screen by selecting the 'Main' tab.

Feature	Options	Description
Main BIOS Version	No option	Displays the main BIOS version.
OEM BIOS Version	No option	Displays the additional OEM BIOS version.
Build Date	No option	Displays the date the BIOS was built.
Product Revision	No option	Displays the hardware revision of the board.
Serial Number	No option	Displays the serial number of the board.
BC Firmware Revision	No option	Displays the firmware revision of the congatec board controller.
MAC Address	No option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	No option	Displays the number of boot-ups (maximum 16777215).
Microcode Patch	No option	Displays the microcode patch loaded for the onboard CPU.
Baytrail SoC	No option	Displays B3 Stepping.
Total Memory	No option	Total amount of low voltage DDR3 present on the system.
System Date	Day of week, month/day/year	Specifies the current system date. **Note:** *The date is in month/day/year format.*
System Time	Hour:Minute:Second	Specifies the current system time. **Note:** *The time is in 24 hour format.*

10.4 Advanced Setup

Select the advanced tab from the setup menu to enter the advanced BIOS setup screen. The menu is used for setting advanced features and only features described within this user's guide are listed.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Watchdog				
	Graphics				
	Hardware Health Monitoring				
	Trusted Computing				
	RTC Wake				
	Module Serial Ports				
	Reserve Legacy Interrupt				
	ACPI				
	Super IO				
	Intel(R) Smart Connect Technology				
	Serial Port Console Redirection				
	CPU Configuration				
	PPM Configuration				
	Thermal Configuration				
	IDE Configuration				
	Miscellaneous Configuration				
	SCC Configuration				
	PCI Subsystem Settings				
	Network Stack				
	CSM Configuration				
	SDIO				
	USB				
	Platform Trust Technology				
	Security Configuration				
	Intel® I210 Gigabit Network				
	Driver Health				

10.4.1 Watchdog Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Set the timeout value for the POST watchdog. The watchdog is only active during the system POST and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup of the boot selection menu or while waiting for the setup password.
Runtime Watchdog	**Disabled** One-time Trigger Single Event Repeated Event	Select the operating mode of the runtime watchdog: 'One-time Trigger' - Disables watchdog after the first trigger. 'Single Event' - Executes every stage once before the watchdog is disabled. 'Repeated Event' - Executes the last stage repeatedly until reset. **Note:** This watchdog will be initialized just before the operating system starts booting.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	The runtime watchdog is delayed for the selected time. **Note:** Use this feature to ensure that the operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Select the type of event that is generated when timeout 1 is reached.
Event 2	**Disabled** ACPI Event Reset Power Button	Select the type of event that is generated when timeout 2 is reached.
Event 3	**Disabled** ACPI Event Reset Power Button	Select the type of event that is generated when timeout 3 is reached.

Feature	Options	Description
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Select the timeout value for the first stage watchdog event.
Timeout 2	See above	Select the timeout value for the second stage watchdog event.
Timeout 3	See above	Select the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. This feature performs a critical but orderly operating system shutdown or restart.

Note

In ACPI mode, it is not possible for a 'Watchdog ACPI Event' handler to directly restart or shutdown the operating system. For this reason, the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the operating systemto shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

Additionally, the conga-TCA3 module does not support the watchdog NMI mode. COM Express type 6 modules do not support the PCI bus and therefore the PCI_SERR# signal is not available. There is no way to drive a NMI to the processor without the presence of the PCI_SERR# PCI bus signal.

10.4.2 Graphics Submenu

Feature	Options	Description
Boot Display Device	VBIOS Default	
CRT	**Enabled** Disabled	Enable or disable the CRT video interface.
Active LFP	No LVDS **LVDS**	Set 'Active LFP' configuration.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes', BIOS uses the EDID™ data set in an external EEPROM to configure the LFP. In case it cannot be found, the data set selected under 'Local Flat Panel Type' is used.
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 2x24 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose 'Auto' to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID™ data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. **Note:** Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.
Backlight Inverter Type	None **PWM** I2C	Select the type of backlight inverter: 'PWM' - IGD PWM signal. 'I2C' - I2C backlight inverter device connected to the video I²C bus.
Digital Display Interface 1 (DDI1)	Disabled **DisplayPort** HDMI/DVI Auto	Select the output type of the DDI.
Digital Display Interface 2 (DDI2)	Disabled **DisplayPort** HDMI/DVI Auto	Select the output type of DDI2. **Note:** This Interface is configurable if 'Active LFP' is set to 'No LVDS'. The DDI2 and LFP interface is shared.
PWM Inverter Frequency (Hz)	**200** - 40000	Set the PWM inverter frequency in Hz. **Note:** This feaute is only visible if the 'Backlight Inverter Type' is set to 'PWM'.

Feature	Options	Description
PWM Inverter Polarity	**Normal** Inverted	Set the PWM inverter polarity. **Note:** This feature is only visible if 'Backlight Inverter Type' is set to 'PWM'.
Backlight Setting	0% 10% 25% 40% 50% 60% 75% 90% **100%**	Select the backlight value in percentage of the maximum setting.
Force LVDS Backlight	**No** Yes	If set to 'Yes', the board controller activates the backlight enable signal independently from the SoC-backlight signal.
Inhibit Backlight	**No** Permanent Until End Of POST	Select whether the backlight enable signal should be activated when the panel is activated, remain inhibited until the end of BIOS POST, or remain inhibited permanently.
Backlight Delay	**No Delay** 100ms Delay 250ms Delay 500ms Delay 1s Delay	Set a delay to adjust the LVDS panel timings. The congatec board controller will add the delay to the backlight signal coming from the SoC according this setup node. **Note:** Try this feature if your panel is flickering.
LVDS SSC	**Disabled** 0.5% 1.0% 1.5% 2.0% 2.5%	Select the LVDS spread-spectrum clock modulation depth. **Note:** This feature performs center spreading with a fixed modulation frequency of 32.9kHz.

10.4.3 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	No option	Displays the CPU temperature in °C.
Board Temperature	No option	Displays the board temperature in °C.
12V Standard	No option	Displays the actual 12V standard voltage.
5Volts Standby	No option	Displays the actual 5V standby voltage.
Input Current (12V Standard)	No option	Displays the actual input current of 12V standard power plane.

Feature	Options	Description
CPU Fan Speed	No option	Displays the CPU fan speed in RPM.
Fan PWM Frequency Mode	Low Frequency **High Frequency**	Select the fan PWM base frequency mode: 'Low Frequency' - 11.0 to 88.2Hz. 'High Frequency' - 1k to 63kHz.
Fan PWM Frequency (kHz)	1 - 63	Select the fan PWM base frequency. Default: 31

10.4.4 Hardware Health Monitoring Submenu

Feature	Options	Description
Security Device Support	**Disabled** Enabled	Enable or disable TPM support. **Note:** Restart your system for the change to take effect.
User Confirmation	Disabled **Enabled**	Enable or disable user confirmation requests for certain transactions.
TPM State	**Disabled** Enabled	Enable or disable TPM chip. **Note:** The system may restart several times during POST to acquire the target state.
Pending operation	**None** Enable Take Ownership Disable Take Ownership TPM Clear	Select TPM chip operation. **Note:** The system may restart several times during POST to perform the selected operation.

10.4.5 RTC Wake Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable this feature to wake the system from S5 using the RTC alarm.
Wake up hour		Specify the wake up hour. For example: Enter "3" for 3am and "15" for 3pm.
Wake up minute		Specify the wake up minute.
Wake up second		Specify the wake up second.

10.4.6 Module Serial Ports Submenu

Feature	Options	Description
Serial Port 0	**Disabled** Enabled	Enable or disable the module's serial port 0.
Serial Port 1	**Disabled** Enabled	Enable or disable the module's serial port 1.

10.4.7 Reserve Legacy Interrupt Submenu

Feature	Options	Description
Reserve Legacy Interrupt 1/2/3	**None** IRQ3 IRQ4 IRQ5 IRQ6 IRQ10 IRQ11 IRQ14 IRQ15	Use this feature to reserve the interrupt for a legacy bus device. **Note:** The selected interrupt will not be assigned to a PCI/PCIe device.

10.4.8 ACPI Submenu

Feature	Options	Description
Enable ACPI Auto Configuration	**Disabled** Enabled	Enable or disable BIOS ACPI auto configuration.
Enable Hibernation	Disabled **Enabled**	Enable or disable the system's ability to hibernate (OS S4 sleep state). **Note:** If you want to use this feature, ensure that the operating system supports it.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state for ACPI system sleep/suspend.
Lock Legacy Resources	**Disabled** Enabled	Enable this feature to lock legacy resources.
LID Support	Disabled **Enabled**	If this feature is enabled, COM Express LID# signal acts as ACPI lid.
Sleep Button Support	Disabled **Enabled**	If this feature is enabled, COM Express SLEEP# signal acts as ACPI sleep button.

10.4.9 SIO Submenu

Feature	Options	Description
AMI SIO Driver Version	No option	
▶Serial Port 1	No option	Opens 'Serial Port 1' submenu.
▶Serial Port 2	No option	Opens 'Serial Port 2' submenu.
▶Parallel Port	No option	Opens 'Parallel Port' submenu.
▶PS2 Controller (KB&MS)	No option	Opens 'PS2 Controller' submenu.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

10.4.10 Serial Port 1 Submenu

Feature	Options	Description
Use this Device	Enable **Disable**	Enable or disable logical device.
Logical Device Settings	No option	Displays logical device settings.
Possible	**Use Automatic Settings** IO=3F8; IRQ=3,4,5,7,9,10,11,12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11,12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11,12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11,12; DMA;	Select the configuration for serial port 1.

10.4.11 Serial Port 2 Submenu

Feature	Options	Description
Use this Device	Enable **Disable**	Enable or disable logical device.
Logical Device Settings	No option	Displays logical device settings.
Possible	**Use Automatic Settings** IO=3F8; IRQ=3,4,5,7,9,10,11,12; DMA IO=2F8; IRQ=3,4,5,7,9,10,11,12; DMA IO=3F8; IRQ=3,4,5,7,9,10,11,12; DMA IO=3E8; IRQ=3,4,5,7,9,10,11,12; DMA	Select the configuration for serial port 2.

10.4.12 Parallel Port Submenu

Feature	Options	Description
Use this Device	Enable **Disable**	Enable or disable logical device.
Logical Device Settings	No option	Displays logical device settings.
Possible	**Use Automatic Settings** IO=3F8; IRQ=3,4,5,7,9,10,11,12; DMA IO=2F8; IRQ=3,4,5,7,9,10,11,12; DMA IO=3F8; IRQ=3,4,5,7,9,10,11,12; DMA IO=3E8; IRQ=3,4,5,7,9,10,11,12; DMA	Select configuration for parallel port.

10.4.13 PS2 Controller (KB&MS) Submenu

Feature	Options	Description
Use this Device	Enable **Disable**	Enable or disable logical device.
Logical Device Settings	No option	Displays logical device settings.
Possible	**Use Automatic Settings** IO=60h; IO=64h; IRQ=1	Select configuration for PS2.

10.4.14 Intel® Smart Connect Technology Submenu

Feature	Options	Description
ISCT Support	**Disabled** Enabled	Enable or disable Intel® Smart Connection Support (ISCT). **Note:** If this setup node is set to disabled, all the other nodes will be invisible.
ISCT Notification Control	Disabled **Enabled**	Enable or disable ISCT notification control.
ISCT WLAN Power Control	Disabled **Enabled**	Enable or disable ISCT WLAN power control.
ISCT WWAN Power Control	Disabled **Enabled**	Enable or disable ISCT WWAN power control
ISCT Sleep Duration Value Format	**Duration in Seconds**	Set the ISCT sleep duration in seconds.
ISCT RF Kill Switch Type	Software **Hardware**	Set the ISCT RF kill switch type.
ISCT RTC Timer Support	**Disabled** Enabled	Enable or disable ISCT RTC timer.

10.4.15 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable redirection for serial port 0.
►Console Redirection Settings	Submenu	Opens console redirection configuration submenu.
Serial Port for Out-of-Band Management / EMS Console Redirection	**Disabled** Enabled	Enable or disable serial port for out-of-band management / Windows Emergency Management Services (EMS).
►Console Redirection Settings	Submenu	Opens console redirection configuration submenu.

Note

The 'Serial Port Console Redirection' can be only enabled if an external Super I/O offering UARTs has been implemented on the carrier board.

10.4.15.1 Console Redirection Settings COM0 Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Set the terminal type.
Baudrate	9600 19200 38400 57600 **115200**	Set baud rate.
Data Bits	7 **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Set parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Set flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable or disable the VT-UTF8 combination key support for ANSI/VT100 terminals.

Feature	Options	Description
Recorder Mode	**Disabled** Enabled	Enable this feature to only send text output over the terminal. **Note:** This feature is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enable or disable extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Select the number of rows and columns for the legacy operating system redirection.
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select the function key and keypad for Putty.

10.4.15.2 Console Redirection Settings Out-of-Band Management Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ **VT-UTF8** ANSI	Set the terminal type.
Bits Per Second	9600 19200 38400 57600 **115200**	Set the baud rate.
Data Bits	**8**	Set the number of data bits.
Parity	None	
Stop Bits	**1**	Set the number of stop bits.

10.4.16 CPU Configuration Submenu

Feature	Options	Description
▶Socket 0 CPU Information	Submenu	Opens the socket specific CPU information.
▶CPU Thermal Configuration	Submenu	Opens the CPU thermal configuration options.
CPU Speed	No option	Displays the CPU clock frequency.
64-bit	No option	Displays whether 64-bit is supported.

Feature	Options	Description
Limit CPUID Maximum	**Disabled** Enabled	If set to 'Enabled', the processor limits the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. If set to 'Disabled', the processor returns the actual maximum CPUID input value of the processor when queried. **Note:** Limiting the CPUID input value might be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Execute Disable Bit	Disabled **Enabled**	If set to 'Enabled', this feature helps to prevent certain classes of malicious buffer overflow attacks. **Note:** If you want to use this feature, ensure that your operating system supports it.
Hardware Prefetcher	Disabled **Enabled**	Enable or disable the Mid Level Cache (MLC) streamer prefetcher.
Adjacent Cache Line Prefetch	Disabled **Enabled**	Enable or disable prefetching of adjacent cache lines.
Intel Virtualization Technology	Disabled **Enabled**	Enable or disable support for the Intel® virtualization technology.
Power Technology	Disable **Energy Efficient** Custom	Configure the power technology schema for the CPU.

10.4.16.1 Socket 0 CPU Information Submenu

Feature	Options	Description
CPU Name	No option	Displays the socket specific CPU name.
CPU Signature	No option	Displays the CPU signature number.
Microcode Patch	No option	Displays the CPU microcode patch number.
Max. CPU Speed	No option	Displays the maximum CPU clock frequency.
Min. CPU Speed	No option	Displays the minimum CPU clock frequency.
Processor Cores	No option	Displays the number of CPU core on socket CPU.
Intel HT Technology	No option	Displays the Intel® HT Technology support information.
Intel VT-x Technology	No option	Displays the Intel® VT-x Technology support information.
L1 Data Cache	No option	Displays the socket L1 data cache information.
L1 Code Cache	No option	Displays the socket L1 code cache information.
L2 Cache	No option	Displays the socket L2 data cache information.
L3 Cache	No option	Displays the socket L3 data cache information.

10.4.16.2 CPU Thermal Configuration Submenu

Feature	Options	Description
DTS	Enabled **Disabled**	Enable or disable the CPU Digital Thermal Sensor (DTS). The DTS is used on ACPI functions to read the CPU temperature from MSR.

10.4.17 PPM Configuration Submenu

Feature	Options	Description
EIST	Disabled **Enabled**	Enable or disable Enhanced Intel® SpeedStep Technology (EIST).
CPU C state Report	Disabled **Enabled**	Enable or disable CPU state report to the operating system.
Enhanced CPU C-state	Disabled **Enabled**	Enable or disable enhanced CPU C states.
Max CPU C state	C7 C6 **C1**	Set the maximum CPU C state supported by the CPU.
SOix	**Disabled** Enabled	Enable or disable CPU SOix state support.

10.4.18 Thermal Configuration

Feature	Options	Description
Critical Trip Point	**110 C** 105 C 100 C 95 C 90 C 87 C 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Select the temperature for the ACPI critical trip point. **Note:** The operating system will shut down when the CPU reaches the selected temperature.

Feature	Options	Description
Passive Trip Point	110 C 105 C 100 C 95 C **90 C** 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Select the temperature for the ACPI passive trip point. **Note:** The operating system will throttle the CPU when the selected temperature is reached.

Note

The conga-TCA3 does not support active trip point.

10.4.19 IDE Configuration Submenu

Feature	Options	Description
Serial-ATA (SATA)	**Enabled** Disabled	Enable or disable the onboard SATA controller.
SATA Test Mode	Enabled **Disabled**	Enable this feature for verification measurements only.
SATA Speed Support	Gen1 **Gen2**	Displays the maximum SATA speed supported by the controller.
SATA ODD Port	Port 0 ODD Port 1 ODD **No ODD**	Select which SATA port is ODD.
SATA Mode	IDE Mode **AHCI Mode**	Select the SATA port mode.
Serial-ATA Port 0	**Enabled** Disabled	Enable or disable the SATA port 0.
SATA Port 0 Hot Plug	**Disabled** Enabled	Enable this feature if you need hot plug support at SATA port 0. **Note:** This feature is not available in native IDE mode.
Serial-ATA Port 1	**Enabled** Disabled	Enable or disable the SATA port 1.

Feature	Options	Description
SATA Port 1 Hot Plug	**Disabled** Enabled	Enable this feature if you need hot plug support at SATA port 1. **Note:** This feature is not available in native IDE mode.
SATA Port 0 Information	No Option	Displays information of device detected at SATA port 0.
SATA Port 1 Information	No Option	Displays information of device detected at SATA port 1.

10.4.20 Miscellaneous Configuration Submenu

Feature	Options	Description
High Precision Timer	**Enabled** Disabled	Enable or disable the high precision event timer.
Boot Timer with HPET Timer	Enabled **Disabled**	Enable this feature to allow boot timer calculation with the high precision event timer.
PCI Express Dynamic Clock Gating	Enabled **Disabled**	Enable or disable dynamic clock gating.

10.4.21 SCC Configuration Submenu

Feature	Options	Description
SCC Device Mode	ACPI Mode **PCI Mode**	Select the storage control cluster working mode.
SCC eMMC Support	Enable eMMC 4.5 Support Enable eMMC 4.41 Support **eMMC AUTO MODE** Disable	Configure SCC eMMC support mode.
SCC 4.5 DDR50 eMMC Support	**Enabled** Disabled	Enable or disable DDR50 eMMC support.
SCC 4.5 HS200 eMMC Support	Enabled **Disabled**	Enable or disable HS200 eMMC support.
eMMC Secure Erase	Enabled **Disabled**	Enable or disable eMMC secure erase support.
SCC SD Card Support	**Enabled** Disabled	Enable or disable storage control cluster SD card support.
SDR25 Support for SD Card	**Enabled** Disabled	Enable or disable SDR25 support for SD card.
DDR50 Support for SD Card	Enabled **Disabled**	Enable or disable DDR50 support for SD card.

10.4.22 PCI Subsystem Settings Submenu

Feature	Options	Description
PCI Settings		
PCI Latency Timer	**32** 64 96 128 160 192 224 248 PCI Bus Clocks	Select the value to be programmed into the PCI latency timer register.
PCI-X Latency Timer	32 **64** 96 128 160 192 224 248 PCI Bus Clocks	Select the value to be programmed into the PCI latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate SERR#.
Above 4G Decoding	**Disabled** Enabled	Enable or disable 64-bit capable devices to be decoded in Above 4G address space. **Note:** If you want to use this feature, ensure that the system supports 64-bit PCI decoding.
SR-IOV Support	**Disabled** Enabled	Enable or disable Single Root IO Virtualization (SR-IOV) support.
▶PCI Express Settings	Submenu	Opens the 'PCI Express Settings' submenu.
▶PCI Express GEN 2 Settings	Submenu	Opens the 'PCI Express Generation 2 Settings' submenu.

10.4.23 PCI Express Settings

Feature	Options	Description
Relaxed Ordering	**Disabled** Enabled	Enable or disable 'Relaxed Ordering' for the PCIe device.
Extended Tag	**Disabled** Enabled	Enable this feature to use 8-bit tag field as a requester.
No Snoop	Disabled **Enabled**	Enable or disable 'No Snoop' for the PCIe device.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 1096 Bytes	Select the maximum payload for the PCIe device manually or set to 'Auto'.
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 1096 Bytes	Select the maximum read request size for the PCIe device or set to 'Auto'.
ASPM Support	**Disabled** Auto Force L0s	Select the ASPM Level: 'Disabled' - Disables ASPM. 'Auto' - BIOS auto configure. 'Force L0s' - Forces all links to L0s state.
Extended Synch	**Disabled** Enabled	Enable this feature to allow the generation of extended synchronization patterns.
Link Training Retry	Disabled 2 3 **5**	Select the number of retry attempts by the software to retrain the link.
Link Training Timeout (uS)	10 - 10000	Enter duration in microseconds for the software to wait before polling 'Link Training' bit in the link status register. Default: 1000
Unpopulated Links	**Keep Link ON** Disabled	Set to 'Disabled' to disable unpopulated PCIe links.
Restore PCIE Registers	Enabled **Disabled**	If the non-PCI aware operating system does not properly reinitiliaze devices after S3, enable this feature to restore PCIe device configurations on S3 resume. **Note:** This feature may cause issues with other hardware after S3 resume.

10.4.24 PCI Express GEN 2 Settings

Feature	Options	Description
Completion Timeout	**Default** Shorter Longer Disabled	Select the completion timeout value: 'Default' - 50us to 50ms. 'Shorter' - Software will use shorter timeout ranges. 'Longer' - Software will use longer timeout ranges.
ARI Forwarding	**Disabled** Enabled	If set to 'Enabled', the downstream port disables it's traditional device number field when turning a type 1 configuration request into a type 0 configuration request, permitting access to extended functions in an ARI device immediately below the port.
AtomicOp Requester Enable	**Disabled** Enabled	If set to 'Enabled', this feature initiates AtomicOp requests only if bus master enable bit is in the command register set.
AtomicOp Egress Blocking	**Disabled** Enabled	If set to 'Enabled', outbound AtomicOp requests via egress ports will be blocked.
IDO Request Enable	**Disabled** Enabled	If set to 'Enabled', this feature permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated.
IDO Completion Enable	**Disabled** Enabled	If set to 'Enabled', this feature permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated.
LTR Mechanism Enable	**Disabled** Enabled	Enable or disable the Latency Tolerance Reporting (LTR) mechanism.
End-End TLP Prefix Blocking	**Disabled** Enabled	If set to 'Enabled', this function will block forwarding of TLPs containing End-End TLP prefixes.
Target Link Speed	**Auto** Force to 2.5 GT/s Force to 5.0 GT/s	Select the target link speed: 'Auto' - Uses HW initialized data. 'Force to X.X GT/s' - Sets an upper limit on link operational speed by restricting the values advertised by the upstream component in its training sequences.
Clock Power Management	**Disabled** Enabled	If set to 'Enabled', the device is permitted to use CLKREQ# signal for power management of link clock in accordance to protocol as defined in appropriate form factor specification.
Compliance SOS	**Disabled** Enabled	If set to 'Enabled', this feature forces LTSSM to send SKP ordered sets between sequences when sending a compliance pattern or a modified compliance pattern.
Hardware Autonomous Width	Enabled **Disabled**	If set to 'Disabled', this feature disables the hardware´s ability to change link width, except for the purpose of correcting unstable link operation.
Hardware Autonomous Speed	Enabled **Disabled**	If set to 'Disabled', this feature disables the hardware´s ability to change link speed, except speed rate reduction for the purpose of correcting unstable link operation.

Note

Ensure that the hardware supports the feature(s) described in this table if you want to use them. Features listed in this table but not supported by the hardware cannot be used.

10.4.25 Network Stack

Feature	Options	Description
Network Stack	Enabled **Disabled**	Enable or disable the UEFI network stack.
Ipv4 PXE Support	Enabled **Disabled**	If disabled, IPV6 PXE boot option will not be created.
Ipv6 PXE Support	Enabled **Disabled**	If disabled, IPV6 PXE boot option will not be created.
PXE boot wait time	0 - 5	Select wait time to press ESC and abort the PXE boot.

10.4.26 CSM Submenu

Feature	Options	Description
Launch CSM	**Enabled** Disabled	Enable or disable the compatibility support module.
CSM16 Module Version	No option	Display the CSM module version number.
Gate A20 Active	**Upon Request** Always	Configure legacy Gate A behavior.
Option ROM Messages	**Force BIOS** Keep Current	Enable or disable option ROM message.
INT19 Trap Response	**Immediate** Postponed	Select the BIOS reaction on INT19 trapping by option ROM: 'Immediate' - Executes the trap immediately. 'Postpone' - Executes the trap during legacy boot.
Boot Option Filter	UEFI and Legacy **Legacy Only** UEFI Only	Control which devices and boot loaders the system should boot to.
Network	Do not launch **UEFI only** Legacy only	Control the execution of UEFI and legacy network option ROMs.
Storage	Do not launch **UEFI only** Legacy only	Control the execution of UEFI and legacy storage option ROMs.
Video	Do not launch UEFI only **Legacy only**	Control the execution of UEFI and legacy video option ROMs
Other PCI Devices	**UEFI only** Legacy only	Control the execution of UEFI and legacy option ROMs for PCI devices different to network, video and storage.

10.4.27 SDIO Submenu

Feature	Options	Description
SDIO Access Mode	**Auto** DMA PIO	Control the SDIO access mode to the device.

10.4.28 USB Submenu

Feature	Options	Description
USB Module Version	No option	Displays the version of the USB module.
USB Devices	No option	Displays the detected USB devices.
xHCI Hand-off	**Enabled** Disabled	This feature can be used as a workaround for operating systems without xHCI hand-off support. **Note:** If this feature is enabled, the xHCI ownership change should be claimed by the xHCI operating system driver.
EHCI Hand-off	**Disabled** Enabled	This feature can be used as a workaround for operating systems without EHCI hand-off support. **Note:** If this feature is enabled, the EHCI ownership change should be claimed by the EHCI operating system driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable or disable mass storage driver support.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	Set the USB legacy mass storage device start unit command timeout.
USB Transfer Timeout	1 sec 5 sec 10 sec **20 sec**	Set the timeout value for control, bulk, and interrupt transfers.
Device Power-Up Delay Selection	**Auto** Manual	Select whether the delay time for a USB device to report itself properly to the host controller should be set automatically or manually. If set to 'Auto', the delay is 100ms for a root port or the value is derived from the hub descriptor for a hub port.
Device Power-Up Delay Value	0 - 40	Set power-up delay value in seconds. Default: 5

10.4.29 Platform Trust Technology

Feature	Options	Description
fTPM	**Disable** Enable	Enable or disable trusted platform module support.

10.4.30 Security Configuration

Feature	Options	Description
TXE	**Enabled** Disabled	Enable or disable trusted execution engine.
TXE HMRFPO	Enable **Disable**	Enable or disable Host ME Region Flash Protection Overwrite (HMRFPO).
TXE Firmware Update	**Enabled** Disabled	Enable or disable firmware update.
TXE EOP Message	**Enabled** Disabled	Enable or disable TXE End of Post (EOP) message.
TXE Unconfiguration Perform	No option	Execute a TXE unconfiguration command
Intel® Anti-Theft Technology Configuration	No option	
Intel® AT	Enable **Disable**	Enable or disable Anti-Theft (AT) technology.
Intel® AT Platform PBA	Enable **Disable**	Enable or disable AT platform Pre-Boot Authentication (PBA).
Intel® AT Suspend Mode	Enable **Disable**	Enable or disable AT suspend mode.

10.4.31 Intel® Ethernet Connection I210 Submenu

Feature	Options	Description
► NIC Configuration	Submenu	Opens the NIC Configuration submenu.
Blink LEDs	**0** - 15	Set the number of seconds for the Ethernet LEDs to blink.
UEFI Driver	No option	Displays the UEFI driver version.
Adapter PBA	No option	Displays the adapter PBA.
Chip Type	No option	Displays the type of the chip in which the Ethernet controller is integrated.
PCI Device ID	No option	Displays the PCI device ID of the Ethernet controller.
Bus:Device:Function	No option	Displays the PCI Bus:Device:Function number of the Ethernet controller.
Link Status	No option	Displays the link status.
MAC Address	No option	Displays the MAC address.

10.4.31.1 NIC Configuration Submenu

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Select the port speed for the selected boot protocol.
Wake on LAN	Disabled **Enabled**	Enable or disable the Wake on LAN (WOL) feature

10.4.32 Driver Health Submenu

Feature	Options	Description
▶Intel® PRO/1000	No option	Displays health status of the drivers/controllers connected to the system.

10.5 Chipset Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.5.1 North Bridge Submenu

Feature	Options	Description
Memory Information		
Total Memory	No option	Displays total amount of memory detected by the system
Memory Slot 0	No option	Displays memory detected by the system on slot 0.
Memory Slot 1	No option	Displays memory detected by the system on slot 1
Max TOLUD	**Dynamic** 2 GB 2.25 GB 2.5 GB 2.75 GB 3 GB	Select the maximum Top of Low Usable DRAM (TOLUD).
Aperture Size	128MB, **256MB**, 512MB	Set the aperture size.
PAVC	Enable **Disable**	Enable or disable Protected Audio Video Control (PAVC).

10.5.2 South Bridge Submenu

Feature	Options	Description
▶ Azalia HD Audio	Submenu	Opens the Azalia HD Audio submenu.
▶ USB	Submenu	Opens the USB submenu.
▶ PCI Express Configuration	Submenu	Opens the PCIe configuration submenu.
High Precision Timer	**Enabled** Disabled	Enable or disable high precision event timer.
Serial IRQ	**Quiet** Continuous	Configure IRQ serial mode.
CLKRUN# Logic	Enable **Disable**	Enable the CLKRUN# logic to stop the LPC clocks when possible. Requires Serial IRQ Mode to be set to Quiet as well
Global SMI Lock	**Enabled** Disabled	Enable or disable SMI lock.
BIOS Read/Write Protection	Enable **Disable**	Enable BIOS SPI region read/write protection.
Generate EXCD0/1_PERST#	Disabled 1ms, 5ms, **10ms**, 50ms, 100ms, 150ms, 200ms, 250ms	The COM Express EXCD0_PERST# and EXCD1_PERST# pins are driven low during POST for the set duration.
Isolate SMBus Segments	Never During POST **Always**	This feature allows to isolate the off-module/external SMBus segment from the on-module SMBus segment. **Note:** This feature can be a workaround for non-spec conform external SMBus devices.

10.5.2.1 Azalia HD Audio

Feature	Options	Description
LPE Audio Support	**Disable** LPE Audio PCI Mode LPE Audio ACPI Mode	Enable or disable LPE audio support.
Audio Controller	**Enabled** Disabled	Enable or disable audio controller.
Azalia Vci Enable	**Enabled** Disabled	Enable or disable Azalia Vci.
Azalia Docking Support Enable	Enable **Disable**	Enable or disable Azalia docking support.
Azalia PME Enable	**Enabled** Disabled	Enable or disable Azalia PME support.

Feature	Options	Description
Azalia HDMI Codec	**Enabled** Disabled	Enable or disable Azalia HDMI codec.
HDMI Port B	**Enabled** Disabled	Enable or disable HDMI port B audio.
HDMI Port C	Enable **Disable**	Enable or disable HDMI port C audio.

10.5.2.2 USB Submenu

Feature	Options	Description
USB OTG Support	**Disabled** Enabled	Enable or disable USB OTG support.
USB VBUS	**On** Off	Set 'On' for host mode and 'Off' for OTG device mode.
xHCI Mode	Enable Disable Auto **Smart Auto**	Select mode for all USB ports (0-3): 'Enabled' - USB ports will function in USB 3.0 mode but require driver on the operating system. USB ports will not function in pre-operating system time if USB 3.0 support in BIOS is disabled (see the USB 3.0 support in BIOS item). 'Disabled' - USB ports will function in USB 2.0 mode only and routed to the EHCI1 controller. 'Auto' - USB ports will initially function in USB 2.0 mode but the operating system driver can switch to USB 3.0. 'Smart Auto' - Identical to 'Auto', except the BIOS will take over the operating system driver setting after each restart.
USB2 Link Power Management	Disabled **Enabled**	Enable or disable USB2 Link Power Management (LPM).
USB 2.0 (EHCI) Support	**Disabled** Enabled	Enable or disable USB 2.0 EHCI functions.
USB Per Port Control	Disabled **Enabled**	Select whether each USB Port (0-3) can be enabled and disabled individually.
USB Port 0	Disabled **Enabled**	Enable or disable USB port 0.
USB Port 1	Disabled **Enabled**	Enable or disable USB port 1.
USB Port 2	Disabled **Enabled**	Enable or disable USB port 2.
USB Port 3	Disabled **Enabled**	Enable or disable USB port 3.

Note

The USB ports originating from the HSIC hub behave differently from the EHCI USB 2.0 ports. For this reason, it is necessary to set the 'xHCI mode' correctly. See the congatec technical note 'CTN-20140702-001' for more information on the configuration that suits your requirements.

10.5.2.3 PCI Express Configuration Submenu

Feature	Options	Description
PCIe noncompliance Card	**Not Supported** Supported	Select whether to support PCIe 1.0 cards. **Note:** If set to 'Supported', the speed of all PCIe ports defaults to Gen 1.
PCI Express Port 0	Disabled **Enabled**	Enable or disable PCIe port 0.
Speed	**Auto** Gen 2 Gen 1	Select PCIe speed on port 0.
PCI Express Port 1	Disabled **Enabled**	Enable or disable PCIe port 1.
Speed	**Auto** Gen 2 Gen 1	Select PCIe speed on port 1.
PCI Express Port 2	Disabled **Enabled**	Enable or disable PCIe port 2.
Speed	**Auto** Gen 2 Gen 1	Select PCIe speed on port 2.
PCI Express Port 3	Disabled **Enabled**	Enable or disable PCIe port 3.
Speed	**Auto** Gen 2 Gen 1	Select PCIe speed on port 3.

10.6 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.6.1 Boot Settings Configuration

Feature	Options	Description
Setup Prompt Timeout	0 - 65535	Set number of seconds to wait for setup activation key. Default: 1 **Note:** 0 is not recommended. 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Quiet Boot	**Disabled** Enabled	'Disabled' - Displays normal POST diagnostic messages. 'Enabled' - Displays OEM logo instead of POST messages. **Note:** The default OEM logo is a dark screen.
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists: 'Device Based' - Select boot priority from a list of currently detected devices. 'Type Based' - Select boot priority from a list of device types even if they are not connected yet.
Power Loss Control	**Remain Off** Turn On Last State	Select the mode of operation if an AC power loss occurs: 'Remain Off' - Keeps the power off until the power button is pressed. 'Turn On' - Restores power to the computer. 'Last State' - Restores the previous power state before power loss occurred. **Note:** If you want to use this feature, chose an ATX type power supply.
AT Shutdown Mode	System Reboot **Hot S5**	Select the behavior of an AT-powered system after a shutdown.
Battery Support	**Auto (Battery Manager)** Battery-Only On I2C Bus Battery-Only On I2C Bus	Select the battery system support bus.
System Off Mode	**G3/Mech Off** S5/Soft Off	Select the system state after a shutdown if a battery system is connected.
Fast Boot	**Disabled** Enabled	Enable to boot with a minimum set of devices. **Note:** This feature has no effect on BBS / legacy boot options.

Note

The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. The standby voltage is continuously monitored after the system is turned off. If the standby voltage is not detected within 30 seconds, this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, it is assumed that the system was switched off properly.

Inexpensive ATX power supplies often have problems with short AC power sags. The system turns off but might not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually, a AC power off/on cycle is necessary to recover from this situation.

10.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

10.7.1 Security Settings

Feature	Options	Description
Administrator Password	Enter password	Enter the setup administrator password.
HDD Security Configuration		
List of all detected hard disks supporting the security feature set		Select the device to open the device security configuration submenu.

10.7.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

10.8 Save & Exit Menu

Select the Save & Exit tab from the setup menu with the <Arrow> keys to enter the Save & Exit setup screen.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset, if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
Boot Override	
List of all boot devices currently detected	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to “Device Based”.

11 Additional BIOS Features

The BIOS setup description of the conga-TCA3 can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

11.1 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-TCA3 is identified as TA31R1xx or TA32R1xx, where:

- TA31 is the BIOS for modules with Baytrail Single Channel Memory SoC
- TA32 is the BIOS for modules with Baytail Dual Channel Memory SoC
- R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number

The TA31 and TA32 BIOS binary size is 8 MB.

11.2 Updating the BIOS

BIOS updates are recommeded to correct platform issues or enhance the feature set of the module. The conga-TCA3 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

11.2.1 Update from External Flash

For instructions on how to update the BIOS from external flash, refer to the AN7_External_BIOS_Update.pdf application note on the congatec website at http://www.congatec.com.

11.3 Supported Flash Devices

The conga-TCA3 supports the following flash device:

- Winbond W25Q64JVSSIQ (8 MB)

The flash device listed above can be used on the carrier board for external BIOS support.