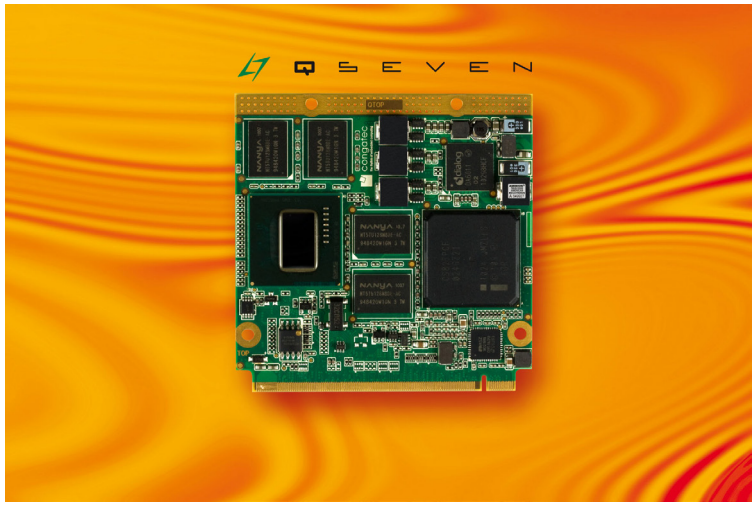

Qseven® conga-QA6

Intel® Atom™ processor E6xx/E6xxT series with an Intel® Platform Controller Hub EG20T

User's Guide

Revision 1.4

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2010.12.22	GDA	• Preliminary release
0.2	2010.12.28	GDA	• Updated information about HDMI support in section 4.13 "HDMI* and table 15 "HDMI Signal Descriptions."
0.3	2011.01.10	GDA	• Corrected the information in the pinout table and PCI Express Signal Descriptions table for pins 161-164 and 179-182.
0.4	2011.02.01	GDA	• Updated section 9 "BIOS Setup Description."
0.5	2011.12.20	GDA	• Updated USB port configuration to reflect hardware revisions A.0 and later. Added additional information to section 5 "Additional Features". • Updated section 9 "BIOS Setup Description."
1.0	2012.06.14	GDA	• Official release. • Added information about the use of conga-QA6 heatspreaders to sections 1.7 "Environment Specifications" and 3.0 "Heatspreader." • Added note to section 4.4 "Serial ATA (SATA)" about AHCI support only. • Added section 6.5 "Important Information". • Updated section 9 "BIOS Setup Description."
1.1	2012.07.13	GDA	• Updated section 9 "BIOS Setup Description."
1.2	2012.11.06	GDA	• Changed maximum torque rating for heatspreader screws in section 3.1 "Heatspreader Dimensions" and added a caution statement. Added comment about LPC_CLK signal to "LPC Signal Descriptions" table. • Updated the PU/PD column of the USB_ID signal in table 9 "USB Signal Description".
1.3	2013.07.10	AEM	• Added section 1 "Introduction". Moved COM Express™ Concept and Options Information to section 1 "Introduction". • Corrected the PCIE_WAKE# Pull-up (PU) value from 1k 3.3VSB to 10k 3.3VSB in table 5 "PCIE Signal Description". • Deleted the RTC alarm option and the option to use USB Mouse/Keyboard Event as Wake event in section 7.3 "ACPI Suspend Modes and Resume Events" because these options are not supported in the BIOS. • Updated section 9 "BIOS Setup Description".
1.4	2017.02.17	BEU	• Corrected WVGA resolution to 800x480. • Updated template and variants.
1.5	2018.06.25	BEU	• Updated "Electrostatic Sensitive Device" information on page 3 • Updated new cooling solution design in section 4.1 "Heatspreader Dimension" and 4.2 "Heatspreader Exploded View". • Updated the USB_ID signal settings in table 9 "USB Signal Description".

Preface

This user's guide provides information about the components, features, connector and BIOS Setup menus available on the conga-QA6. It is one of three documents that should be referred to when designing a Qseven® application. The other reference documents that should be used include the following:

Qseven® Design Guide
Qseven® Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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Electrostatic Sensitive Device

All electronic parts described in this user's guide are electrostatic sensitive devices. Therefore, they are shipped enclosed in static shielding bags in addition to secondary packaging. Do not remove the device from the static shielding bag, nor handle it, except at an electrostatic-free workstation. The secondary packaging should not be permitted in an ESD protected area (EPA).

Additionally, do not ship or store electronic devices near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
DDC	Display Data Channel
SoC	System On Chip
LVDS	Low-Voltage Differential Signaling
Gbe	Gigabit Ethernet
eMMC	Embedded Multi-media Controller
MLC	Multi-level Cell
SLC	Single-level Cell
HDA	High Definition Audio
cBC	congatec Board Controller
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

Contents

List of Tables

1 Introduction

Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector. The pinout remains the same regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The Qseven® evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose what are suitable for their application. Qseven® applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no need to redesign the carrier board.

This document describes the features available on the Qseven® evaluation carrier board. Additionally, the schematics for the Qseven® evaluation carrier board can be found on the congatec website.

conga-QA6 Options Information

The conga-QA6 is currently available in several different variants. This user's guide describes the available features these different variants offer. Below you will find an order table showing the base configuration modules that are currently offered by congatec AG. For more information about the additional conga-QA6 variants offered by congatec, contact your local congatec sales representative or visit the congatec website at www.congatec.com.

Table 1 conga-QA6 Commercial Variants

Part-No.	015033	015030	015031	015032
Processor	Intel® Atom™ E680 1.6 GHz	Intel® Atom™ E660 1.3 GHz	Intel® Atom™ E640 1.0 GHz	Intel® Atom™ E620 0.6 GHz
L2 Cache	512kB	512kB	512kB	512kB
Onboard Memory up to 2GB	1GB DDR2 (800 MT/s)	1GB DDR2 (800 MT/s)	1GB DDR2 (667 MT/s)	1GB DDR2 (667 MT/s)
External PCI Express Lane(s)	3	3	3	3
Gigabit Ethernet	Yes	Yes	Yes	Yes
Onboard Solid-State Drive (SSD)	No	No	No	No
CAN Bus	Yes	Yes	Yes	Yes
CPU TDP	3.9 W	3.6 W	3.6 W	2.7 W

Part-No.	015042	015046	015047
Processor	Intel® Atom™ E680 1.6GHz	Intel® Atom™ E680 1.6GHz	Intel® Atom™ E640 1.0GHz
L2 Cache	512kB	512kB	512kB
Onboard Memory up to 2GB	2GB DDR2 (800 MT/s)	1GB DDR2 (533 MT/s)	1GB DDR2 (533 MT/s)
External PCI Express Lane(s)	3	3	3
Gigabit Ethernet	Yes	Yes	Yes
Onboard Solid-State Drive (SSD)	No	8GB MLC	4GB MLC
CAN Bus	Yes	Yes	Yes
CPU TDP	4.5 W	4.5 W	3.6 W

Table 2 conga-QA6 Industrial Variants

Part-No.	015038	015035	015036	015039
Processor	Intel® Atom™ E680T 1.6 GHz	Intel® Atom™ E660T 1.3 GHz	Intel® Atom™ E640T 1.0 GHz	Intel® Atom™ E640T 1.0GHz
L2 Cache	512kB	512kB	512kB	512kB
Onboard Memory	1GB DDR2 (800 MT/s)	1GB DDR2 (800 MT/s)	1GB DDR2 (667 MT/s)	1GB DDR2 (800 MT/s)
External PCI Express Lane(s)	3	3	3	3
Gigabit Ethernet	Yes	Yes	Yes	Yes
Onboard Solid-State Drive (SSD)	No	No	No	2GB SLC
CAN Bus	Yes	Yes	Yes	Yes
CPU TDP	3.9 W	3.6 W	3.6 W	3.6 W

Part-No.	015041	015037
Processor	Intel® Atom™ E680T 1.6GHz	Intel® Atom™ E620T 600 MHz
L2 Cache	512kB	512kB
Onboard Memory	2GB DDR2 (800 MT/s)	1GB DDR2 (667 MT/s)
External PCI Express Lane(s)	3	3
Gigabit Ethernet	Yes	Yes
Onboard Solid-State Drive (SSD)	No	No
CAN Bus	Yes	Yes
CPU TDP	4.5 W	2.7 W

2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	Based on Qseven® form factor specification revision 1.20	
Processor	Intel® Atom™ E680 1.6 GHz with 512kB L2 cache Intel® Atom™ E660 1.3 GHz with 512kB L2 cache Intel® Atom™ E640 1.0 GHz with 512kB L2 cache Intel® Atom™ E620 600 MHz with 512kB L2 cache Intel® Atom™ E680T 1.6 GHz with 512kB L2 cache (industrial grade processor) Intel® Atom™ E660T 1.3 GHz with 512kB L2 cache (industrial grade processor) Intel® Atom™ E640T 1.0 GHz with 512kB L2 cache (industrial grade processor) Intel® Atom™ E620T 600 MHz with 512kB L2 cache (industrial grade processor)	
Memory	Onboard DDR 2 up to 2GB	
Chipset	Intel® Platform Controller Hub (PCH) EG20T	
Audio	HDA (High Definition Audio)/digital audio interface with support for multiple codecs	
Ethernet	Gigabit Ethernet, Micrel KSZ9021RN (commercial temp) or KSZ9021RNI (industrial temp) and Phy	
Graphics Options	Integrated 3D graphics engine. Dual independent display support.	
	• Flat panel Interface (integrated) 80 MHz LVDS Transmitter Supports 1x18 and 1x24 bit TFT configurations. Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3) Resolutions 640x480 up to 1280x768. • AUX Output 1 x Intel compliant SDVO port (serial DVO). Resolutions up to 1280x1024 @ 85 Hz. Supports external DVI, TV and LVDS transmitters	• Video Decode Acceleration: MPEG2 MPEG4 H.264 WMV9/VC1
Peripheral Interfaces	• 2x Serial ATA® Gen 2 (SATA port 1 not available if SSD option is used) • 1x SDIO • 3 PCI Express Lanes (revision 1.1 (2.5Gbps) compliant) • 8x USB 2.0 host ports	• SPI Bus • CAN Bus • LPC Bus • I²C Bus, Fast Mode (400 kHz) multimaster
Onboard Storage	Optionally equipped with a Solid State Drive (SSD) up to 32 GByte in capacity	
BIOS	AMI Aptio® UEFI 2.x firmware, 4MByte serial SPI with congatec Embedded BIOS features	
Power Mgmt.	ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).	

Note

Some of the features mentioned in the above Feature Summary are optional and require customized articles. Check the part number of your module and compare it to the option information list on page 12 to determine what options are available on your particular module. For more information, contact congatec support.

2.2 Supported Operating Systems

The conga-QA6 supports the following operating systems.

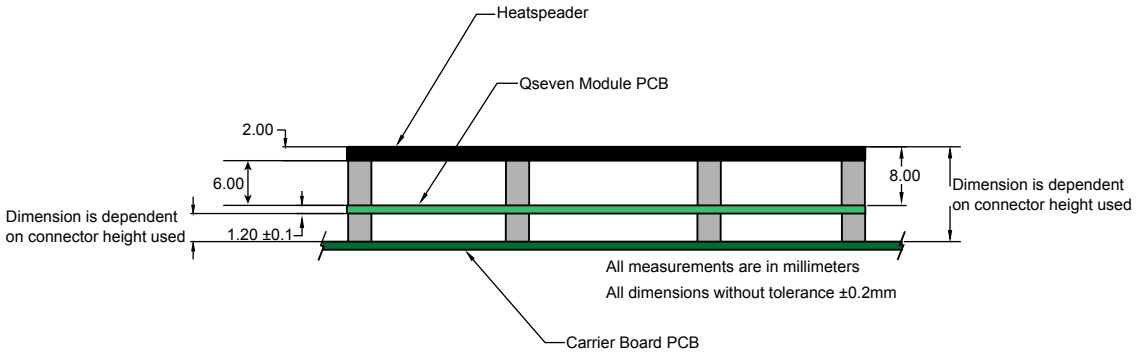
- Microsoft® Windows® 7
- Microsoft® Windows® Embedded Standard 7
- Microsoft® Windows® Embedded Compact 7
- Microsoft® Windows® CE 6.0
- Microsoft® Windows® XP
- Microsoft® Windows® XP Embedded
- Linux

Note

DOS is not officially supported by the Intel® Queensbay platform (E6xx series processors and EG20T Platform Controller Hub (PCH)). As a result of this it's possible that some legacy DOS based applications will not function properly when used in conjunction with the conga-QA6. This limitation is due to the EG20T PCH architecture, which is not designed for legacy applications.

2.3 Mechanical Dimensions

- 70.0 mm x 70.0 mm @ (2 ¾" x 2 ¾")
- The Qseven™ module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.

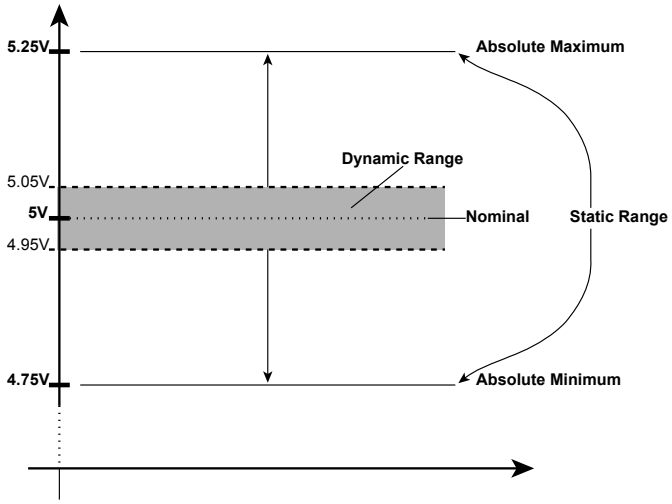


Rear View of Qseven Module

2.4 Supply Voltage Standard Power

- 5V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Table 4 Power Limits

Characteristics			Min.	Typ.	Max.	Units	Comment
5V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV_{PP}	0-20MHz
	Current						
5V_SB	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple				± 50	mV_{PP}	

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-QA6
- modified congatec carrier board
- conga-QA6 cooling solution
- Microsoft Windows 7 (32 bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool

Table 5 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle.	The CPU was stressed to its maximum frequency.
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency.
S0: Peak value	Highest current spike during the measurement of “S0: Maximum value”. This state shows the peak value during runtime	Consider this value when designing the system’s power supply to ensure that sufficient power is supplied during worst case scenarios.
S3	COM is powered by VCC_5V_SBY.	
S5	COM is powered by VCC_5V_SBY.	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Table 6 Power Consumption Values

The tables below provide additional information about the power consumption data for each of the conga-QA6 variants offered. The values are recorded at various operating mode.

Part No.	Memory Size	BIOS Rev.	OS (32 bit)	CPU			Current (Amp.)			
				Variant	Cores	Freq/Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S3
015033	1GB	QTOPR002	Windows 7	Intel® Atom™ E680	1	1.6 GHz	1.04	1.81	1.92	0.12
015030	1GB	QTOPR002	Windows 7	Intel® Atom™ E660	1	1.3 GHz	1.06	1.54	1.76	0.14
015031	1GB	QTOPR002	Windows 7	Intel® Atom™ E640	1	1.0 GHz	1.12	1.51	1.70	0.14
015032	1GB	QTOPR002	Windows 7	Intel® Atom™ E620	1	0.6 GHz	0.96	1.09	1.24	0.12

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 7 CMOS Battery Power Consumption

RTC @	Voltage	Current
20°C	3V DC	2.26 µA

Note

There is a limitation with the Intel® Platform Controller Hub EG20T and the RTC. The RTC leakage current is extremely high. This means the RTC battery within a system featuring this chipset will be depleted after as little as 8 months.

congatec solves this RTC current leakage problem by using the onboard board controller found on the conga-QA6. When the conga-QA6 is powered off, the EG20T RTC is disconnected and the onboard board controller's RTC is used. When the conga-QA6 is restarted, the BIOS overwrites the EG20T system clock with the correct one provided by the congatec board controller.

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider also the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec AG website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-MA5.*

2.7 Environmental Specifications

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface. Humidity specifications are for non-condensing conditions.

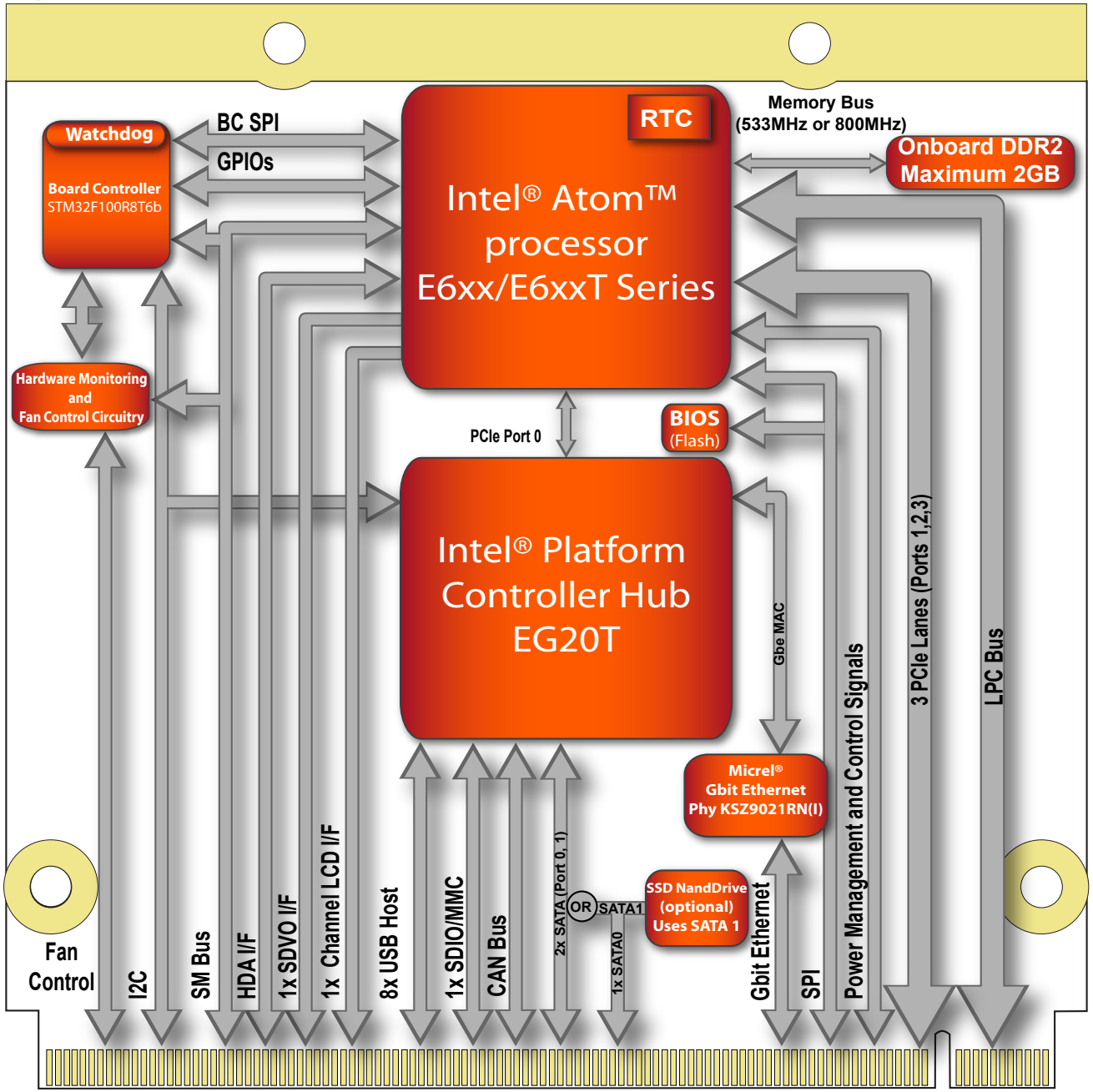
Temperature (commercial variants)	Operation:	0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation:	-40° to 85°C	Storage: -45° to +85°C
Humidity	Operation:	10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



4 Cooling Solutions

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module and its aluminum plate is 2mm thick.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis thereby using the whole chassis as a heat dissipater.

Caution

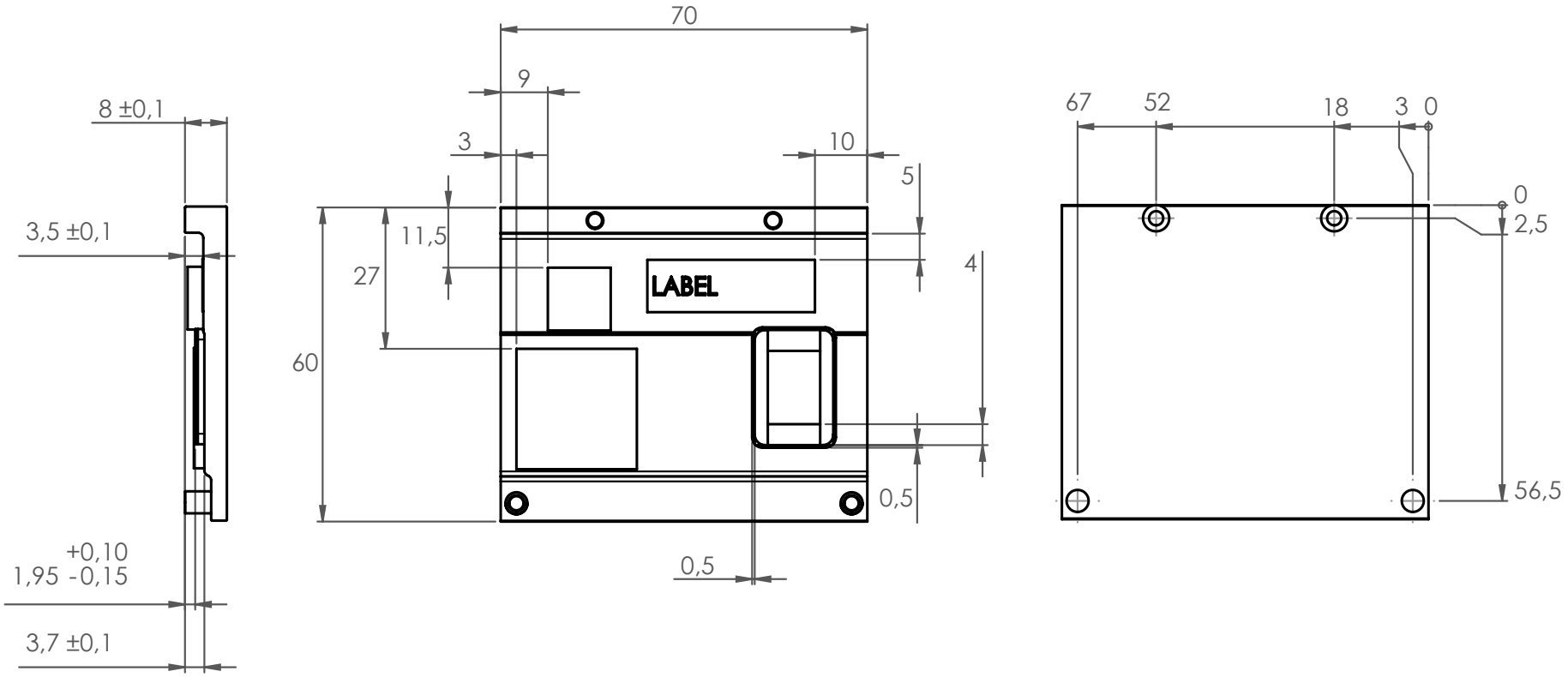
congatec Qseven® heaspreaders have been specifically designed for use within commercial temperature ranges (0° to 60°C) only. When using industrial temperature variants of the conga-QA6 in industrial temperature ranges (-40° to 85°C), use of the conga-QA6 heatspreaders is not recommended by congatec and furthermore its use is at the risk of the end user. It is the responsibility of the end user to design an optimized thermal solution that meets the needs of their application within the industrial environmental conditions it is required to operate in.

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

Only heatspreaders that feature micro pins that secure the thermal stacks should be used for applications that require the heatspreader to be mounted vertically. It cannot be guaranteed that the thermal stacks will not move if a heatspreader that does not have the micro pin feature is used in vertically mounted applications.

Additionally, the gap pad material used on all heatspreaders contains silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.

4.1 Heatspreader Dimensions



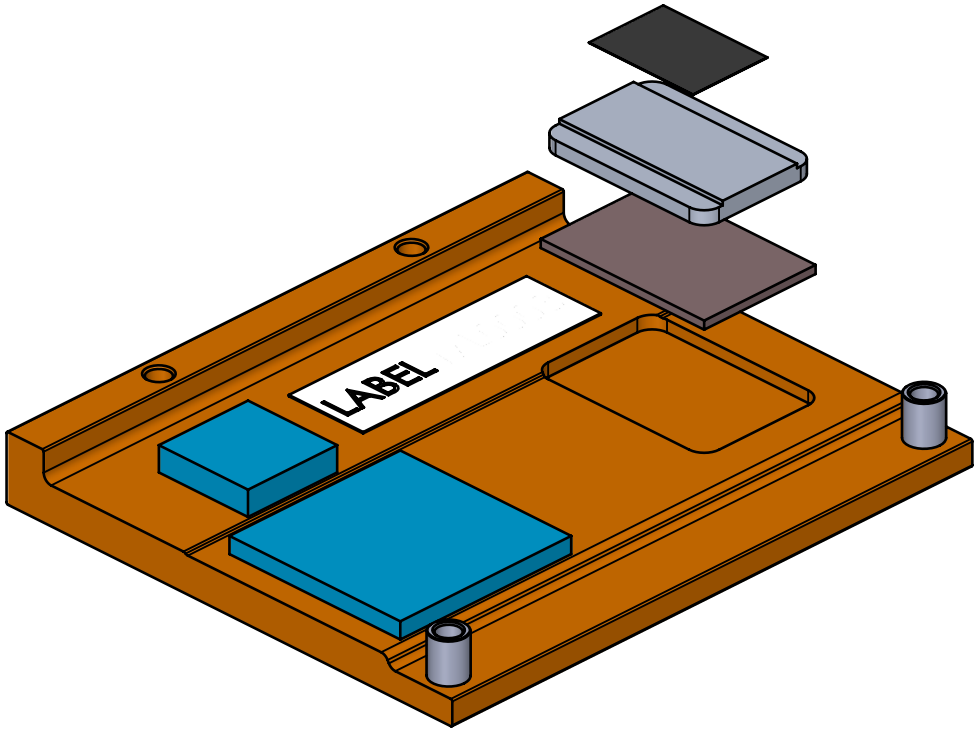
Note

All measurements are in millimeters. Torque specification for heatspreader screws is 0.3 Nm. Mechanical system assembly mounting shall follow the valid DIN/IS0 specifications. The cooling strip found on the conga-QA is connected directly to the ground plane when mounted in the conga-QEVAL evaluation carrier board. For more information about connecting the conga-QA's PCB cooling plate to the carrier board ground plane refer to the Qseven Design Guide.

Caution

When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.

4.2 Heatspreader Exploded View

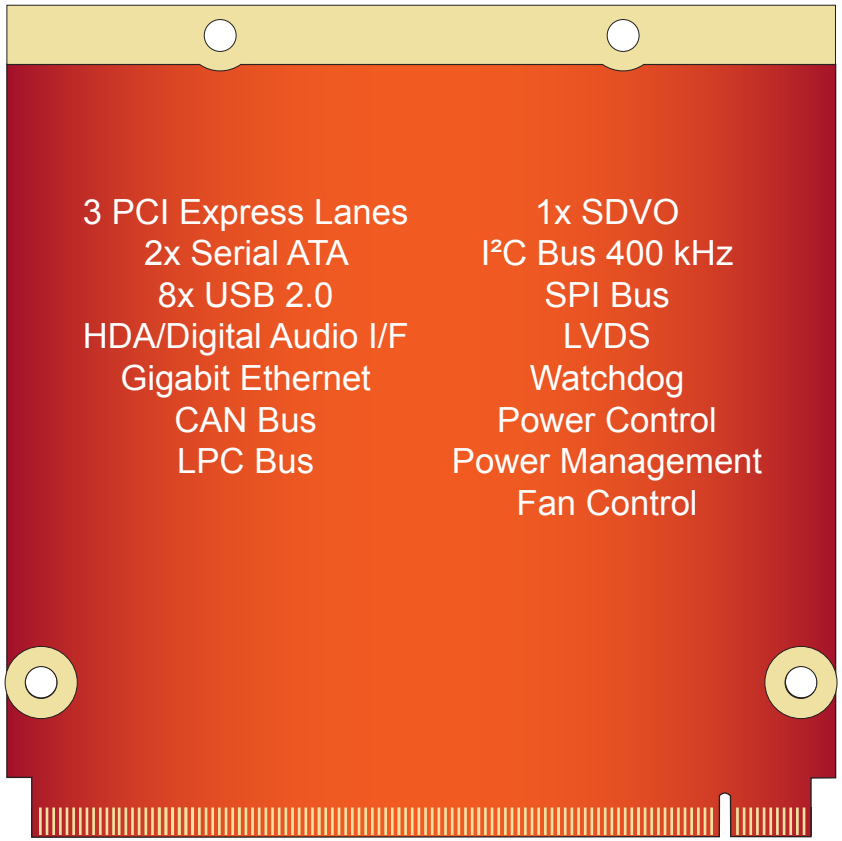


Note

Torque specification for heatspreader screws is 0.3 Nm.

5 Connector Subsystems

The conga-QA6 is based on the Qseven® standard and therefore has 115 edge fingers on the top and bottom side of the module that mate with the 230-pin card-edge MXM connector located on the carrier board. This connector provides the ability to interface the available signals of the conga-QA6 with the carrier board peripherals.



5.1 PCI Express™

The Intel® Atom. processor E6xx/E6xxT series supports 4 PCI Express Lanes. PCI Express lane 0 of the CPU connects the processor to the Intel® Platform Controller Hub EG20T on the conga-QA6. The remaining 3 PCI Express lanes are available externally on the MXM connector as PCIe channel 0, 1 and 2 on the carrier board and can be configured to support PCI Express edge cards or ExpressCards. The PCI Express interface supports PCI Express Specification 1.0a. For more information about which channels are available on the MXM connector refer to the conga-QA6 pinout table in section 8 "Signal Descriptions and Pinout Tables." Only x1 PCI Express link configurations possible.

5.2 ExpressCard™

The conga-QA6 supports the implementation of one ExpressCard. This requires the dedication of one USB port and one PCI Express lane. Refer to section 8, "Signal Descriptions and Pinout Tables" for information about which ExpressCard port is supported.

5.3 Gigabit Ethernet

The Intel® Platform Controller Hub EG20T provides the conga-QA6 with a Gigabit Ethernet Media Access Controller (GbE MAC) that is connected to a Micrel KSZ9021RN(I) Phy. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

Note

For conga-QA6 rev C.x and earlier, congatec AG reccommends not to connect the center-taps of the magnetics to either each other or to CTREF pin.

5.4 Serial ATA™ (SATA)

Two Serial ATA (SATA) connections are provided by a SATA controller integrated in the Intel® Platform Controller Hub EG20T found on the conga-QA6. Supports SATA 1.5-Gbps Gerneration 1 and 3-Gbps Generation 2 speeds. Compliant with Serial ATA specification 2.6 and Advanced Host Controller Interface (AHCI) specification revision 1.1. The optional SSD feature utilizes SATA port 1 and therefore only SATA port 0 is available externally when the module is equipped with the onboard SSD feature.

Note

The conga-QA6 SATA interface supports AHCI mode only. Legacy parallel ATA emulation is not supported.

5.5 USB 2.0

The conga-QA6 offers a USB 2.0 host controller provided by the Intel® Platform Controller Hub EG20T. This controller complies with USB standard 1.1 and 2.0 and provides a total of 8 USB ports via the card-edge MXM connector. All ports are capable of supporting USB 1.1 and 2.0 compliant devices.

5.6 SDIO/MMC

SDIO stands for Secure Digital Input Output. Devices that support SDIO can use small devices such as SD-Card or MMC-Card flash memories. The Intel® Platform Controller Hub EG20T found on the conga-QA6 provides a SDIO/MMC expansion port used to communicate with a variety of SDIO and MMC devices. This port is available externally and supports SDIO Revision 1.1 and MMC Revision 4.1 and is backward compatible with previous interface specifications.

Note

Only DOS and Linux (Ubuntu, Xandros) boot support for SDIO/MMC devices is available.

5.7 High Definition Audio (HDA)

The conga-QA6 provides an interface that supports the connection of HDA audio codecs.

5.8 LCD

The Intel® Atom™ processor E6xx/E6xxT series, found on the conga-QA6, offers an integrated single channel 80MHz LVDS interface that is internally connected to Display Pipe A. It supports the connection of 1x18 or 1x24 bit data mapping up to a resolution of 1280x768@60Hz. For more information about the supported resolutions, see table 2 below.

5.9 SDVO

conga-QA6 provides one SDVO port via Display Pipe B of the Intel® Atom™ processor E6xx/E6xxT series. The SDVO port can support a variety of display types (VGA, LVDS, DVI, TV-Out, etc.) by an external SDVO device. This single channel 160MHz SDVO interface supports resolutions up to 1920x1080@60Hz and 1280x1024@85Hz. For more information see the table below.

Table 8 Display Resolutions

Resolution	Refresh	Pixel Clock Freq	SDVO Support	LVDS Support	
640x480	50 Hz	19.75 MHz	Y	Y	
640x480	60 Hz	23.75 MHz	Y	Y	
848x480	50 Hz	26 MHz	Y	Y	
848x480RB	60 Hz	29.75 MHz	Y	Y	
640x480	75 Hz	30.75 MHz	Y	Y	
800x600	50 Hz	30.75 MHz	Y	Y	
848x480	60 Hz	31.5 MHz	Y	Y	
640x480	85 Hz	35 MHz	Y	Y	
800x600RB	60 Hz	35.5 MHz	Y	Y	
800x600	60 Hz	38.25 MHz	Y	Y	
848x480	75 Hz	41 MHz	Y	Y	
848x480	85 Hz	46.75 MHz	Y	Y	
800x600	75 Hz	49 MHz	Y	Y	
1024x768	50 Hz	52 MHz	Y	Y	
1024x768RB	60 Hz	56 MHz	Y	Y	
800x600	85 Hz	56.75 MHz	Y	Y	
1024x768	60 Hz	63.5 MHz	Y	Y	
1280x768	50 Hz	65.25 MHz	Y	Y	
1280x768RB	60 Hz	68.25 MHz	Y	Y	
1280x768	60 Hz	79.5 MHz	Y	Y	Max LVDS interface support
1400x1050	60 Hz	121.75 MHz	Y		
1280x960	75 Hz	130 MHz	Y		
1600x1200RB	60 Hz	130.25 MHz	Y		
1600x1200	50 Hz	131.5 MHz	Y		
1920x1080RB	60 Hz	138.5 MHz	Y		
1280x1024	75 Hz	138.75 MHz	Y		
1920x1080	50 Hz	141.5 MHz	Y		
1280x960	85 Hz	148.25 MHz	Y		
1400x1050	75 Hz	156 MHz	Y		
1280x1024	85 Hz	159.5 MHz	Y		Max SDVO interface support

5.10 DisplayPort

DisplayPort is an open, industry standard digital display interface, that has been developed within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

Note

The conga-QA6 does not offer a DisplayPort interface.

5.11 HDMI

High-Definition Multimedia Interface (HDMI) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video.

Note

The conga-QA6 does not offer a HDMI interface.

5.12 LPC

conga-QA6 offers the LPC (Low Pin Count) bus through the use of the Intel® Atom™ processor E6xx/E6xxT series. There are already many devices available for this Intel® defined bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals and functionality. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific carrier board using this bus. Only certain devices such as Super I/O or TPM 1.2 chips can be implemented on the carrier board.

5.13 SPI

A SPI interface that supports booting from an external SPI flash is available on the conga-QA6. This interface is provided by the Intel® Atom™ processor E6xx/E6xxT series and only supports the connection of an external SPI flash to enable external boot capabilities.

5.14 CAN Bus

The conga-QA6 supports CAN bus. The CAN controller performs communication in accordance with the BOSCH CAN Protocol Version 2.0B Active1 (standard format and extended format). The bit rate can be programmed to a maximum of 1Mbit/s, based on the technology used. To connect the CAN controller module to the CAN bus, it is necessary to add transceiver hardware. A complete description of the CAN controller registers and functionality is beyond the scope of this user's guide. Refer to chapter 13.0 of the Intel Platform Controller Hub E20GT datasheet for additional information about this interface.

5.15 Power Control

PWGIN

PWGIN (pin 26) can be connected to an external power good circuit or it may also be utilized as a manual reset input. In order to use PWGIN as a manual reset the pin must be grounded through the use of a momentary-contact push-button switch. When external circuitry asserts this signal, it's necessary that an open-drain driver drives this signal causing it to be held low for a minimum of 15ms to initiate a reset. Using this input is optional. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies, the conga-QA6 module is capable of generating its own power-on good.

The conga-QA6 provides support for controlling ATX-style power supplies. In order to do this the power supply must provide a constant source of VCC_5V_SB power. When using an AT power supply (5V only) then the conga-QA6's pins SUS_S3 and PWRBTN# should be left unconnected. VCC_5V_SB can also be left unconnected but it is recommended to connect it to the 5V input power rail.

SUS_S3#

The SUS_S3# (pin 18) signal is an active-low output that can be used to turn on the main 5V rail of the power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 20) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-QA6. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-QA6 application:

- It has also been noticed that on some occasions problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush-current on the conga-QA6 VCC_5V_SB power rail can go up as high as 2.3A for a maximum of 100µS. Sufficient decoupling capacitance must be implemented to ensure proper power-up sequencing.

The maximum peak-current on the conga-QA6 VCC (5V) power rail can be as high as 3.0A. This requires that the power supply be properly dimensioned.

Note

For more information about power control event signals refer to the Qseven® specification.

5.16 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3). No support for legacy APM.

5.17 I²C Bus

The I²C bus is implemented through the use of STMicroelectronics STM32F100R8 microcontroller. It provides a multi-master I²C Bus that has maximum I²C bandwidth.

5.18 Watchdog

The conga-QA6 is equipped with a multi stage watchdog solution that can be triggered by software or external hardware. For more information about the Watchdog feature see the BIOS setup description of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

5.19 Fan Control

conga-QA6 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) Output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system fan's RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason a two pulse per revolution fan, or similar hardware solution, is recommended.

Note

A four wire fan must be used to generate the correct speed readout.

6 Additional Features

6.1 congatec Board Controller (cGB)

The conga-QA6 is equipped with an STMicroelectronics STM32F100R8 microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

6.2 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.3 Watchdog

The conga-QA6 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-QA6 does not support external hardware triggering. For more information about the Watchdog feature see the BIOS setup description section 10.5.2 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

6.4 I²C Bus

The conga-QA6 offers support for the frequently used I²C bus. Thanks to the I²C host controller in the cBC the I²C bus is multimaster capable and runs at speeds up to 400kHz (fast mode).

6.5 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behaviour of the system after a AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

6.6 Embedded BIOS

The conga-QA6 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. These are the most important embedded PC features:

6.6.1 CMOS Backup in Non Volatile Memory

A copy of the CMOS memory (SRAM) is stored in the BIOS flash device. This prevents the system from not booting up with the correct system configuration if the backup battery (RTC battery) has failed. Additionally, it provides the ability to create systems that do not require a CMOS backup battery.

6.6.2 OEM CMOS Default Settings and OEM BIOS Logo

This feature allows system designers to create and store their own CMOS default configuration and BIOS logo (splash screen) within the BIOS flash device. Customized BIOS development by congatec for these changes is no longer necessary because customers can easily do these changes by themselves using the congatec system utility CGUITL.

6.6.3 OEM BIOS Code

With the congatec embedded BIOS it is even possible for system designers to add their own code to the BIOS POST process. Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table, verb tables for HDA codecs, rare graphic modes and Super I/O controllers.

For more information about customizing the congatec embedded BIOS refer to the congatec System Utility user's guide, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com or contact congatec technical support.

6.6.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-QA6 BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM²C User's Guide

6.6.5 API Support (CGOS/EAPI)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux and QNX. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

Other COM (Computer on Modules) vendors offer similar driver solutions for these kind of embedded PC features, which are by nature proprietary. All the API solutions that can be found on the market are not compatible to each other. As a result, writing application software that can run on more than one vendor's COM is not so easy. Customers have to change their application software when switching to another COM vendor. EAPI (Embedded Application Programming Interface) is a programming interface defined by the PICMG that addresses this problem. With this unified API it is now possible to run the same application on all vendor's COMs that offer EAPI driver support. Contact congatec technical support for more information about EAPI.

6.7 Suspend to Ram

The Suspend to RAM feature is available on the conga-QA6.

6.8 Onboard Solid State Disk

A solid-state drive (SSD) is a data storage device that uses solid-state memory to store persistent data. A SSD is a hard disk drive without the traditional moving parts, thus easily replacing traditional hard drives in most applications. The conga-QA6 can be optionally equipped with a SSD up to 32 GByte in capacity. Due to the nature of NAND Flash technology there is a limitation of maximum write cycles related to each storage cell.

According to the manufacturer datasheet, an endurance of 10 million (for commercial MLC technology) or 100 million (for industrial SLC technology) write cycles is specified. Unlimited write cycles IS NOT specified. Since an advanced NAND memory management technology firmware is implemented in the SSD drive, it will balance the wear on erased blocks with an advanced wear-leveling algorithm, which provides a maximum of 10 million (or 100 million depending of the type of SSD used) product write cycles.

In most applications this will be an acceptable and secure solution but it must be mentioned that the device lifetime will be affected mainly by the following parameters:

1. Operation time and used OS: If a 24/7 application is running under a write-intensive OS (such as Windows XP etc.) without EWF (Enhanced Write Filter), the amount of guaranteed write-cycles may be reached before the defined MTBF of the complete system.

2. The ratio between used and unused SSD capacity will also affect the lifetime. Since the wear-leveling algorithm uses access statistics for balancing the wears on the blocks, the SSD endurance will increase or decrease according to the amount of used and unused SSD space.

3. Given the information in parameters 1 and 2, if the SSD application is a 24/7 continuously running OS equipped SSD drive, with frequent write accesses and there is not enough free capacity available for wear leveling, the SSD endurance will decrease accordingly. For this reason it's necessary to avoid a configuration that will result in not enough free capacity being available for wear leveling and therefore it is required that an EWF mechanism is used thereby limiting the write-cycles in order to maintain sufficient free disk space. Failure to use a EWF mechanism will void the warranty of the SSD drive.

Note

For more information about the SSD drive's capability refer to the manufacturers datasheet.

7 conga Tech Notes

The conga-QA6 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

7.1 Intel® Processor Features

7.1.1 Thermal Monitor and Catastrophic Thermal Protection

Intel® Atom™ processor E6xx/E6xxT series have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature, that the Intel® Thermal Monitor uses to activate the TCC, cannot be configured by the user nor is it software visible.

The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel® Speedstep transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.

Note

The maximum operating temperature for Intel® Atom™ processor E6xx/E6xxT series is 100°C.

Two modes are supported by the Thermal Monitor to activate the TCC. They are called Automatic and On-Demand. No additional hardware, software, or handling routines are necessary when using Automatic Mode.

Note

To ensure that the TCC is active for only short periods of time thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Atom™ processor E6xx/E6xxT series respective datasheet can provide more information about this subject.

7.1.2 Processor Performance Control

Intel® Atom™ processor E6xx/E6xxT series run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it's not being fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that your power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

7.1.3 Intel® Virtualization Technology

Virtualization solutions enhanced by Intel® VT will allow Atom™ processor E6xx/E6xxT series to run multiple operating systems and applications in independent partitions. When using virtualization capabilities, one computer system can function as multiple "virtual" systems. With processor and I/O enhancements to Intel®'s various platforms, Intel® Virtualization Technology can improve the performance and robustness of today's software-only virtual machine solutions.

Intel® VT is a multi-generational series of extensions to Intel® processor and platform architecture that provides a new hardware foundation for virtualization, establishing a common infrastructure for all classes of Intel® based systems. The broad availability of Intel® VT makes it possible to create entirely new applications for virtualization in servers, clients as well as embedded systems thus providing new ways to improve system reliability, manageability, security, and real-time quality of service.

The success of any new hardware architecture is highly dependent on the system software that puts its new features to use. In the case of virtualization technology, that support comes from the virtual machine monitor (VMM), a layer of software that controls the underlying physical platform resources sharing them between multiple "guest" operating systems. Intel® VT is already incorporated into most commercial and open-source VMMs including those from VMware, Microsoft, XenSource, Parallels, Virtual Iron, Jaluna and TenAsys.

You can find more information about Intel Virtualization Technology at: http://developer.intel.com/technology/virtualization/index.htm

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

7.2 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-QA6 ACPI thermal solution offers three different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point, the processor clock is throttled according to the formula below.

$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

- ΔP is the performance delta

- T_t is the target temperature = critical trip point
- The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants. These constants are set to fixed values for the conga-QA6:
- TC1= 1
- TC2= 5
- TSP= 5 seconds

See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.3 ACPI Suspend Modes and Resume Events

conga-QA6 supports the S3 (STR= Suspend to RAM) power state. For more information about S3 wake events see section 10.5.7 "ACPI Configuration Submenu". S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by some operating systems (S4_OS= Hibernate). Check with the operating system vendor to determine if S4 (Suspend to Disk) is supported.

This table lists the "Wake Events" that resume the system from S3 unless otherwise stated in the "Conditions/Remarks" column:

Table 9 Wake Events resuming system from S3

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3 and S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support. Featured must be enabled in BIOS setup.
PCI Express WAKE#	Wakes unconditionally from S3.
Watchdog Power Button Event	Wakes unconditionally from S3 and S5.

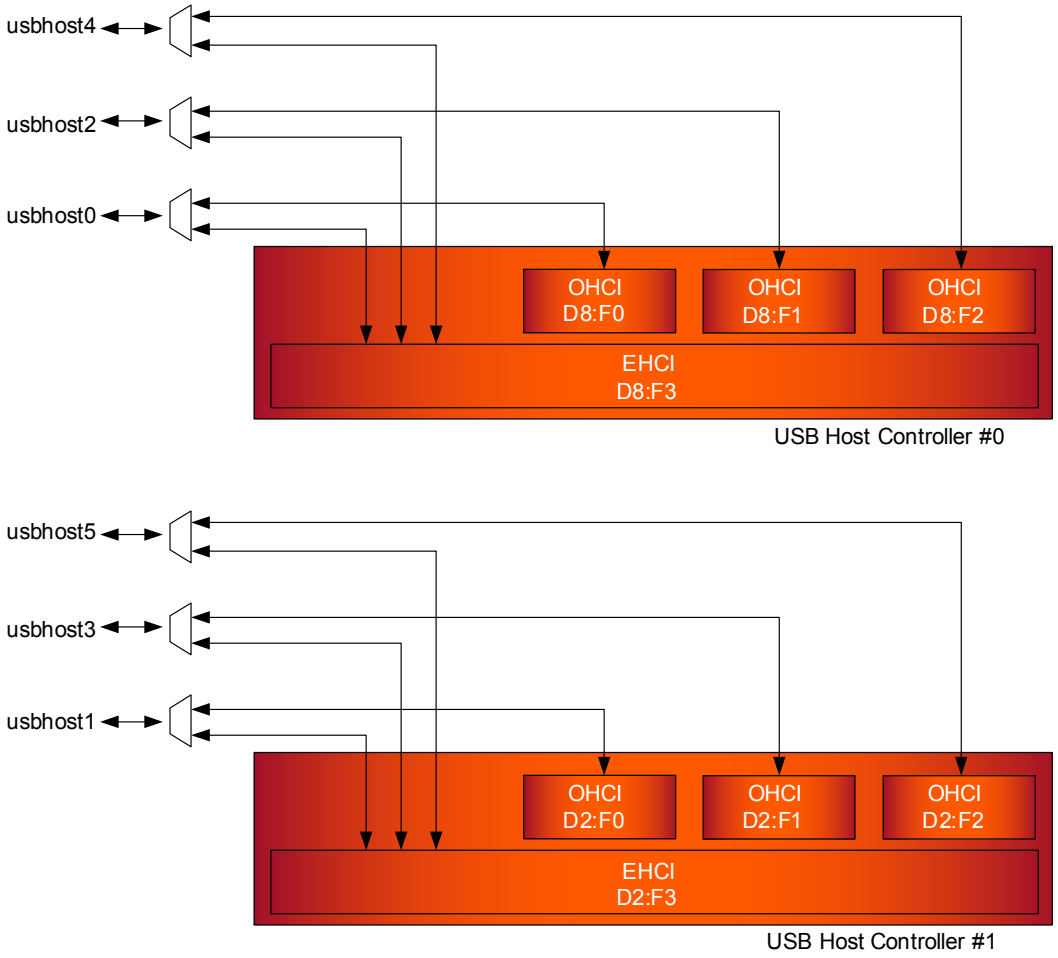
Note

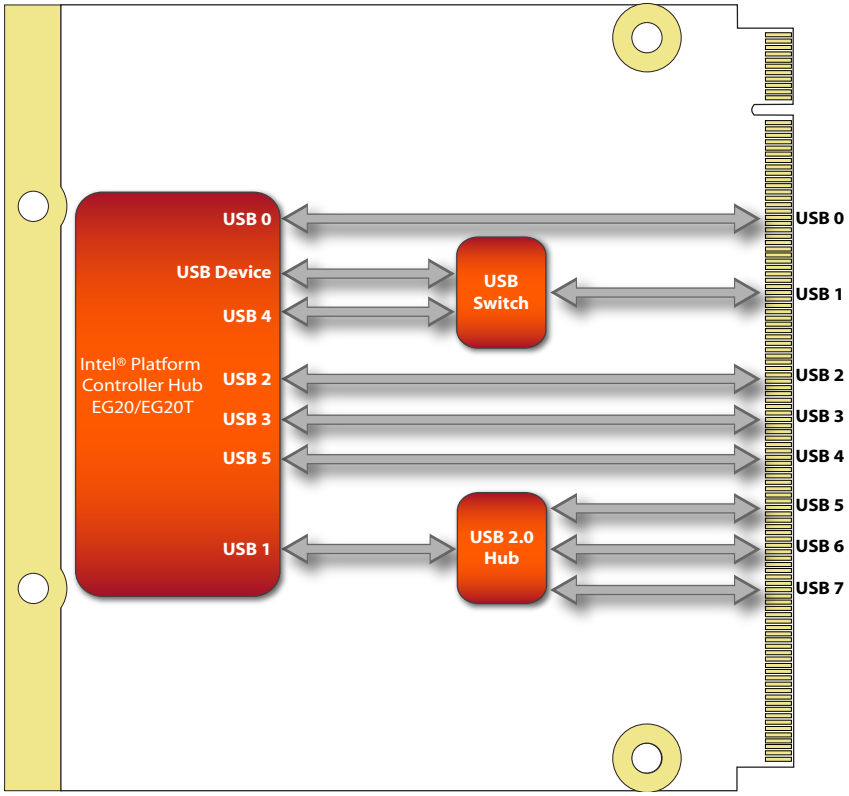
The above list has been verified using a Windows XP SP3 ACPI enabled installation.

7.4 USB Port Connections

The 6 USB ports are shared between 2 EHCI host controllers. Ports 0-5 are capable of supporting USB 1.1 and 2.0 compliant devices. congatec has implemented a USB 2.0 hub on the conga-QA6 that provides two additional ports for a total of 8. See conga-QA6 USB Routing Diagram on the following page.

Routing Diagram





7.5 Important Information

There are certain limitations associated with the Intel platform featured on the conga-QA6 as well as the module itself. These limitation are documented in a conga-QA6 Fact Sheet. For information about the conga-QA6 Fact Sheet contact your local congatec representative.

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on Qseven® module's edge fingers.

Table 3 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a Qseven® module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Not all the signals described in this section are available on all conga-QA6 variants. Use the article number of the module and refer to the options table on page 8 to determine the options available on the module.

Table 10 Signal Tables Terminology Descriptions

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PP	Push Pull
I/O	Bi-directional Input/Output Pin
P	Power Input
NA	Not applicable
NC	Not Connected
PCIE	PCI Express differential pair signals. In compliance with the PCI Express Base Specification 1.0a.
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet Specification.
USB	Universal Serial Bus differential pair signals. In compliance with the Universal Serial Bus Specification 2.0
SATA	Serial Advanced Technology Attachment differential pair signals. In compliance with the Serial ATA High Speed Serialized AT Attachment Specification 1.0a.
SPI	Serial Peripheral Interface bus is a synchronous serial data link that operates in full duplex mode.
CAN	Controller Area Network bus is a vehicle bus standard that allows microcontrollers and devices to communicate with each other within a vehicle without a host computer.
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

Table 11 Edge Finger Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Power Ground	2	GND	Power Ground
3	GBE_MDI3-	Gigabit Ethernet MDI3-	4	GBE_MDI2-	Gigabit Ethernet MDI2-
5	GBE_MDI3+	Gigabit Ethernet MDI3+	6	GBE_MDI2+	Gigabit Ethernet MDI2+
7	GBE_LINK100#	100 Mbps link speed	8	GBE_LINK1000#	1000 Mbps link speed
9	GBE_MDI1-	Gigabit Ethernet MDI1-	10	GBE_MDI0-	Gigabit Ethernet MDI0-
11	GBE_MDI1+	Gigabit Ethernet MDI1+	12	GBE_MDI0+	Gigabit Ethernet MDI0+
13	GBE_LINK#	Gigabit Ethernet Link indicator	14	GBE_ACT#	Gigabit Ethernet Activity indicator
15	GBE_CTREF (*)	Reference voltage for GBE	16	SUS_S5#	S5 (Soft OFF) – shutdown state
17	WAKE#	External system wake event	18	SUS_S3#	S3 (Suspend to RAM) – SLP
19	SUS_STAT#	Suspend status	20	PWRBTN#	Power button
21	SLP_BTN#	Sleep button	22	LID_BTN#	LID button
23	GND	Power Ground	24	GND	Power Ground
25	GND	Power Ground	26	PWGIN	Power good input
27	BATLOW#	Battery low input	28	RSTBTN#	Reset button input
29	SATA0_TX+	Serial ATA Channel 0 TX+	30	SATA1_TX+(*)	Serial ATA Channel 1 TX+
31	SATA0_TX-	Serial ATA Channel 0 TX-	32	SATA1_TX- (*)	Serial ATA Channel 1 TX-
33	SATA_ACT#	Serial ATA Activity	34	GND	Power Ground
35	SATA0_RX+	Serial ATA Channel 0 RX+	36	SATA1_RX+ (*)	Serial ATA Channel 1 RX+
37	SATA0_RX-	Serial ATA Channel 0 RX-	38	SATA1_RX- (*)	Serial ATA Channel 1 RX-
39	GND	Power Ground	40	GND	Power Ground
41	BIOS_DISABLE# /BOOT_ALT#	BIOS Module disable Boot Alternative Enable	42	SDIO_CLK	SDIO Clock Output
43	SDIO_CD#	SDIO Card Detect	44	SDIO_LED	SDIO LED
45	SDIO_CMD	SDIO Command/Response	46	SDIO_WP	SDIO Write Protect
47	SDIO_PWR#	SDIO Power Enable	48	SDIO_DAT1	SDIO Data Line 1
49	SDIO_DAT0	SDIO Data Line 0	50	SDIO_DAT3	SDIO Data Line 3
51	SDIO_DAT2	SDIO Data Line 2	52	SDIO_DAT5	SDIO Data Line 5
53	SDIO_DAT4	SDIO Data Line 4	54	SDIO_DAT7	SDIO Data Line 7
55	SDIO_DAT6	SDIO Data Line 6	56	RESERVED	
57	GND	Power Ground	58	GND	Power Ground
59	HDA_SYNC	HD Audio/AC'97 Synchronization	60	SMB_CLK	SMBus Clock line
61	HDA_RST#	HD Audio/AC'97 Codec Reset	62	SMB_DAT	SMBus Data line
63	HDA_BITCLK	HD Audio/AC'97 Serial Bit Clock	64	SMB_ALERT#	SMBus Alert input
65	HDA_SDI	HD Audio/AC'97 Serial Data In	66	I2C_CLK	I2C Bus Clock
67	HDA_SDO	HD Audio/AC'97 Serial Data Out	68	I2C_DAT	I2C Bus Data
69	THRM#	Thermal Alarm active low	70	WDTRIG#	Watchdog trigger signal
71	THRMTRIP#	Thermal Trip indicates an overheating condition	72	WDOUT	Watchdog event indicator
73	GND	Power Ground	74	GND	Power Ground

Pin	Signal	Description	Pin	Signal	Description
75	USB_P7-	USB Port 7 Differential Pair-	76	USB_P6-	USB Port 6 Differential Pair-
77	USB_P7+	USB Port 7 Differential Pair+	78	USB_P6+	USB Port 6 Differential Pair+
79	USB_6_7_OC#	Over current detect input 6/7 USB	80	USB_4_5_OC#	Over current detect input 4/5 USB
81	USB_P5-	USB Port 5 Differential Pair-	82	USB_P4-	USB Port 4 Differential Pair-
83	USB_P5+	USB Port 5 Differential Pair+	84	USB_P4+	USB Port 4 Differential Pair+
85	USB_2_3_OC#	Over current detect input 2/3 USB	86	USB_0_1_OC#	Over current detect input 0/1 USB
87	USB_P3-	USB Port 3 Differential Pair-	88	USB_P2-	USB Port 2 Differential Pair-
89	USB_P3+	USB Port 3 Differential Pair+	90	USB_P2+	USB Port 2 Differential Pair+
91	USB_CC	USB Client present detect pin	92	USB_ID	USB ID pin
93	USB_P1-	USB Port 1 Differential Pair-	94	USB_P0-	USB Port 0 Differential Pair-
95	USB_P1+	USB Port 1 Differential Pair+	96	USB_P0+	USB Port 0 Differential Pair+
97	GND	Power Ground	98	GND	Power Ground
99	LVDS_A0+	LVDS Primary channel 0+	100	LVDS_B0+ (*)	LVDS Secondary channel 0+
101	LVDS_A0-	LVDS Primary channel 0-	102	LVDS_B0- (*)	LVDS Secondary channel 0-
103	LVDS_A1+	LVDS Primary channel 1+	104	LVDS_B1+ (*)	LVDS Secondary channel 1+
105	LVDS_A1-	LVDS Primary channel 1-	106	LVDS_B1- (*)	LVDS Secondary channel 1-
107	LVDS_A2+	LVDS Primary channel 2+	108	LVDS_B2+ (*)	LVDS Secondary channel 2+
109	LVDS_A2-	LVDS Primary channel 2-	110	LVDS_B2- (*)	LVDS Secondary channel 2-
111	LVDS_PPEN	LVDS Power enable	112	LVDS_BLEN	LVDS Backlight enable
113	LVDS_A3+	LVDS Primary channel 3+	114	LVDS_B3+ (*)	LVDS Secondary channel 3+
115	LVDS_A3-	LVDS Primary channel 3-	116	LVDS_B3- (*)	LVDS Secondary channel 3-
117	GND	Power Ground	118	GND	Power Ground
119	LVDS_A_CLK+	LVDS Primary channel CLK+	120	LVDS_B_CLK+ (*)	LVDS Secondary channel CLK+
121	LVDS_A_CLK-	LVDS Primary channel CLK-	122	LVDS_B_CLK- (*)	LVDS Secondary channel CLK-
123	LVDS_BLT_CTRL /GP_PWM_OUT0	PWM Backlight brightness General Purpose PWM Output	124	RESERVED	
125	LVDS_DID_DAT /GP_I2C_DAT	DDC Display ID Data line General Purpose I2C Data line	126	LVDS_BLC_DAT (*)	SSC clock chip data line
127	LVDS_DID_CLK /GP_I2C_CLK	DDC Display ID Clock line General Purpose I2C Clock line	128	LVDS_BLC_CLK (*)	SSC clock chip clock line
129	CAN0_TX	CAN TX Output for CAN Bus Channel 0	130	CAN0_RX	CAN RX Input for CAN Bus Channel 0
131	SDVO_BCLK+	SDVO Clock line+	132	SDVO_INT+	SDVO Interrupt line+
133	SDVO_BCLK-	SDVO Clock line-	134	SDVO_INT-	SDVO Interrupt line-
135	GND	Power Ground	136	GND	Power Ground
137	SDVO_GREEN+	SDVO Green line+	138	SDVO_FLDSTALL+	SDVO Field stall line+
139	SDVO_GREEN-	SDVO Green line-	140	SDVO_FLDSTALL-	SDVO Field stall line-
141	GND	Power Ground	142	GND	Power Ground
143	SDVO_BLUE+	SDVO Blue line+	144	SDVO_TVCLKIN+	SDVO TV-Out line+
145	SDVO_BLUE-	SDVO Blue line-	146	SDVO_TVCLKIN-	SDVO TV-Out line-
147	GND	Power Ground	148	GND	Power Ground
149	SDVO_RED+	SDVO Red line+	150	SDVO_CTRL_DAT	I2C based control clock for SDVO

Pin	Signal	Description	Pin	Signal	Description
151	SDVO_RED-	SDVO Red line-	152	SDVO_CTRL_CLK	I2C based control data for SDVO
153	HDMI_HPD# (*)	Hot plug detection for HDMI	154	DP_HPD# (*)	Hot plug detection for Display port
155	PCIE_CLK_REF+	PCI Express Reference Clock+	156	PCIE_WAKE#	PCI Express Wake event
157	PCIE_CLK_REF-	PCI Express Reference Clock-	158	PCIE_RST#	Reset Signal for external devices
159	GND	Power Ground	160	GND	Power Ground
161	PCIE3_TX+ (*)	PCI Express Channel 3 Output+	162	PCIE3_RX+ (*)	PCI Express Channel 3 Input+
163	PCIE3_TX- (*)	PCI Express Channel 3 Output-	164	PCIE3_RX- (*)	PCI Express Channel 3 Input-
165	GND	Power Ground	166	GND	Power Ground
167	PCIE2_TX+	PCI Express Channel 2 Output+	168	PCIE2_RX+	PCI Express Channel 2 Input+
169	PCIE2_TX-	PCI Express Channel 2 Output-	170	PCIE2_RX-	PCI Express Channel 2 Input-
171	EXCD0_PERST#	Express Card slot#0 reset	172	EXCD1_PERST# (*)	Express Card slot#1 reset
173	PCIE1_TX+	PCI Express Channel 1 Output+	174	PCIE1_RX+	PCI Express Channel 1 Input+
175	PCIE1_TX-	PCI Express Channel 1 Output-	176	PCIE1_RX-	PCI Express Channel 1 Input-
177	EXCD0_CPPE#	Express Card slot#0 Capable/Req	178	EXCD1_CPPE# (*)	Express Card slot#0 Capable/Req
179	PCIE0_TX+	PCI Express Channel 0 Output+	180	PCIE0_RX+	PCI Express Channel 0 Input+
181	PCIE0_TX-	PCI Express Channel 0 Output-	182	PCIE0_RX-	PCI Express Channel 0 Input-
183	GND	Power Ground	184	GND	Power Ground
185	LPC_AD0	LPC Interface Address/Data 0	186	LPC_AD1	LPC Interface Address/Data 1
187	LPC_AD2	LPC Interface Address/Data 0	188	LPC_AD3	LPC Interface Address/Data 3
189	LPC_CLK	LPC Interface Clock	190	LPC_FRAME#	LPC frame indicator
191	SERIRQ	Serialized interrupt	192	LPC_LDRQ# (*)	LPC DMA request
193	VCC_RTC	3V backup cell input	194	SPKR /GP_PWM_OUT2	Output for audio enunciator General Purpose PWM Output
195	FAN_TACHOIN /GP_TIMER_IN	Fan tachometer input General Purpose Timer In	196	FAN_PWMOUT /GP_PWM_OUT1	Fan speed control (PWM) General Purpose PWM Output
197	GND	Power Ground	198	GND	Power Ground
199	SPI_MOSI	SPI Master serial output/Slave serial input	200	SPI_CS0#	SPI Chip Select 0 Output
201	SPI_MISO	SPI Master serial input/Slave serial output signal	202	SPI_CS1# (*)	SPI Chip Select 1 Output
203	SPI_SCK	SPI Clock Output	204	MFG_NC4	Do not connect on carrier board
205	VCC_5V_SB	+5VDC,Standby ±5%	206	VCC_5V_SB	+5VDC Standby ±5%
207	MFG_NC0	Do not connect on carrier board	208	MFG_NC2	Do not connect on carrier board
209	MFG_NC1	Do not connect on carrier board	210	MFG_NC3	Do not connect on carrier board
211	VCC	Power supply +5VDC ±5%	212	VCC	Power supply +5VDC ±5%
213	VCC	Power supply +5VDC ±5%	214	VCC	Power supply +5VDC ±5%
215	VCC	Power supply +5VDC ±5%	216	VCC	Power supply +5VDC ±5%
217	VCC	Power supply +5VDC ±5%	218	VCC	Power supply +5VDC ±5%
219	VCC	Power supply +5VDC ±5%	220	VCC	Power supply +5VDC ±5%
221	VCC	Power supply +5VDC ±5%	222	VCC	Power supply +5VDC ±5%
223	VCC	Power supply +5VDC ±5%	224	VCC	Power supply +5VDC ±5%
225	VCC	Power supply +5VDC ±5%	226	VCC	Power supply +5VDC ±5%

Pin	Signal	Description	Pin	Signal	Description
227	VCC	Power supply +5VDC ±5%	228	VCC	Power supply +5VDC ±5%
229	VCC	Power supply +5VDC ±5%	230	VCC	Power supply +5VDC ±5%

Note

The signals in the previous table marked with an asterisk symbol (*) are not supported on the conga-QA6.

Table 12 PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.0a.
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.0a.
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.0a.
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.0a.
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.0a.
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.0a.
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	I PCIE		Not available externally. Used to connect EG20T PCH Supports PCI Express Base Specification, Revision 1.0a.
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Not available externally. Used to connect EG20T PCH Supports PCI Express Base Specification, Revision 1.0a.
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock for Lanes 0 to 3.	O PCIE		
PCIE_WAKE#	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I 3.3VSB	PU 10k 3.3VSB	
PCIE_RST#	158	Reset Signal for external devices.	O 3.3V		

Table 13 ExpressCard Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE#	177	ExpressCard slot #0 capable card request.	I 3.3V	PU 10k 3.3V	
EXCD0_PERST#	171	ExpressCard slot #0 reset.	O 3.3V	PU 10k 3.3V	
EXCD1_CPPE#	178	ExpressCard slot #1 capable card request.	I 3.3V		Not supported
EXCD1_PERST#	172	ExpressCard slot #1 reset.	O 3.3V		Not supported

Table 14 Ethernet Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GBE_MDI0+ GBE_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI1+ GBE_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI2+ GBE_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI3+ GBE_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_CTREF	15	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		Not Supported
GBE_LINK#	13	Ethernet controller 0 link indicator, active low.	O 2.5VSB	PD 1k	GBE0_LINK# is a bootstrap signal (see note below)
GBE_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 2.5VSB	PU 4k99 2,5VSB	Not Supported. Internally connected to GBE_ACT#. GBE0_LINK100# is a bootstrap signal (see note below)
GBE_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 2.5VSB	PD 1k	Not Supported. Internally connected to GBE_LINK# GBE0_LINK1000# is a bootstrap signal (see note below)
GBE_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 2.5VSB	PU 4k99 2,5VSB	GBE0_ACT# is a bootstrap signal (see note below)

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module.

For more information refer to section 8.1 of this user's guide.

Table 15 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	O 3.3V		

Note

Serial ATA channel 1 is not available externally if the conga-QA6 is equipped with the onboard SSD option.

Table 16 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_P0+ USB_P0-	96 94	Universal Serial Bus Port 0 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P1+ USB_P1-	95 93	Universal Serial Bus Port 1 differential pair. If USB_ID is LOW = USB Host If USB_ID is tied HIGH (default) = USB device (Client)	I/O		If USB_ID is LOW = USB 2.0 compliant Host. Backwards compatible to USB 1.1 If USB_ID is HIGH (default) = USB 2.0 Client. Backwards compatible to USB 1.1
USB_P2+ USB_P2-	90 88	Universal Serial Bus Port 2 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P3+ USB_P3-	89 87	Universal Serial Bus Port 3 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P4+ USB_P4-	84 82	Universal Serial Bus Port 4 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P5+ USB_P5-	83 81	Universal Serial Bus Port 5 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P6+ USB_P6-	78 76	Universal Serial Bus Port 6 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P7+ USB_P7-	77 75	Universal Serial Bus Port 7 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	86	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	I 3.3VSB	PU 10k 3.3VSB	
USB_2_3_OC#	85	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	I 3.3VSB	PU 10k 3.3VSB	

USB_4_5_OC#	80	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	I 3.3VSB	PU 10k 3.3VSB	
USB_6_7_OC#	79	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	I 3.3VSB	PU 10k 3.3VSB	
USB_ID	92	USB ID pin. Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the BIOS will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.	I 3.3VSB	PD 1k	
USB_CC#	91	USB Client Connect pin. If USB Port 1 is configured for client mode then an externally connected USB host should set this signal to high-active in order to properly make the connection with the module's internal USB client controller. If the external USB host is disconnected, this signal should be set to low-active in order to inform the USB client controller that the external host has been disconnected. A level shifter/protection circuitry should be implemented on the carrier board for this signal.	I 3.3V	PU 10k 3.3V	

Table 17 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	43	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I/O 3.3V	PU 10k 3.3V	
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	O 3.3V		
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O 3.3V OD/PP	PU 10k 3.3V	
SDIO_LED	44	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	O 3.3V		
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I/O 3.3V	PU 10k 3.3V	
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/ MMC card device.	O 3.3V	PU 10k 3.3V	
SDIO_DAT0 SDIO_DAT1 SDIO_DAT2 SDIO_DAT3 SDIO_DAT4 SDIO_DAT5 SDIO_DAT6 SDIO_DAT7	49 48 51 50 53 52 55 54	SDIO Data lines. These signals operate in push-pull mode.	I/O 3.3V PP	PU 10k 3.3V	

Table 18 HDA/AC'97 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST#	61	HD Audio/AC'97 Codec Reset.	O 3.3V		
HDA_SYNC	59	Serial Bus Synchronization.	O 3.3V		
HDA_BITCLK	63	HD Audio/AC'97 24 MHz Serial Bit Clock from Codec.	O 3.3V		
HDA_SDO	67	HD Audio/AC'97 Serial Data Output to Codec.	O 3.3V		
HDA_SDI	65	HD Audio/AC'97 Serial Data Input from Codec.	I 3.3V		

Note

The High Definition Audio interface found on the conga-QA6 complies with Intel® High Definition Audio Specification 1.0.

Table 19 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_PPEN	111	Controls panel power enable.	O 3.3V		
LVDS_BLEN	112	Controls panel Backlight enable.	O 3.3V		
LVDS_BLT_CTRL /GP_PWM_OUT0	123	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
LVDS_A0+ LVDS_A0-	99 101	LVDS primary channel differential pair 0.	O LVDS		
LVDS_A1+ LVDS_A1-	103 105	LVDS primary channel differential pair 1.	O LVDS		
LVDS_A2+ LVDS_A2-	107 109	LVDS primary channel differential pair 2.	O LVDS		
LVDS_A3+ LVDS_A3-	113 115	LVDS primary channel differential pair 3.	O LVDS		
LVDS_A_CLK+ LVDS_A_CLK-	119 121	LVDS primary channel differential pair clock lines.	O LVDS		
LVDS_B0+ LVDS_B0-	100 102	LVDS secondary channel differential pair 0.	O LVDS		Not supported
LVDS_B1+ LVDS_B1-	104 106	LVDS secondary channel differential pair 1.	O LVDS		Not supported
LVDS_B2+ LVDS_B2-	108 110	LVDS secondary channel differential pair 2.	O LVDS		Not supported
LVDS_B3+ LVDS_B3-	114 116	LVDS secondary channel differential pair 3.	O LVDS		Not supported
LVDS_B_CLK+ LVDS_B_CLK-	120 122	LVDS secondary channel differential pair clock lines.	O LVDS		Not supported

LVDS_DID_CLK /GP_I2C_CLK	127	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used, it can be used as General Purpose I²C bus clock line.	I/O 3.3V OD	PU 10k 3.3V	
LVDS_DID_DAT /GP_I2C_DAT	125	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used, it can be used as General Purpose I²C bus data line.	I/O 3.3V OD	PU 10k 3.3V	
LVDS_BLC_CLK	128	Control clock signal for external SSC clock chip.	I/O 3.3V OD	PU 4k7 3.3V	Not supported
LVDS_BLC_DAT	126	Control data signal for external SSC clock chip.	I/O 3.3V OD	PU 10k 3.3V	Not supported

Table 20 SDVO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDVO_BCLK+ SDVO_BCLK-	131 133	SDVO differential pair clock lines.	O PCIE		
SDVO_INT+ SDVO_INT-	132 134	SDVO differential pair interrupt input lines.	I PCIE		
SDVO_GREEN+ SDVO_GREEN-	137 139	SDVO differential pair green data lines.	O PCIE		
SDVO_BLUE+ SDVO_BLUE-	143 145	SDVO differential pair blue data lines.	O PCIE		
SDVO_RED+ SDVO_RED-	149 151	SDVO differential pair red data lines.	O PCIE		
SDVO_FLDSTALL+ SDVO_FLDSTALL-	138 140	SDVO differential pair field stall lines.	I PCIE		
SDVO_TVCLKIN+ SDVO_TVCLKIN-	144 146	SDVO differential pair TV-Out synchronization clock lines.	I PCIE		
SDVO_CTRL_CLK	152	I²C based control signal (clock) for SDVO device. *Note: If the control bus from the SDVO device has a different signaling voltage, then a level shifting device will be required on the carrier board to properly translate the voltage level for this signal.*	I/O 3.3V OD	PU 100k 3.3V	
SDVO_CTRL_DAT	150	I²C based control signal (data) for SDVO device. *Note: If the control bus from the SDVO device has a different signaling voltage, then a level shifting device will be required on the carrier board to properly translate the voltage level for this signal.*	I/O 3.3V OD	PU 100k 3.3V	

Note

The SDVO interface signals are shared with the signals for the DisplayPort interface and/or the TMDS interface. The conga-QA6 does not support the DisplayPort/TMDS interface.

Table 21 DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP_LANE3+ DP_LANE3-	131 133	DisplayPort differential pair lines lane 3.	O PCIE		Shared with SDVO_BCLK+ and SDVO_BCLK- DisplayPort interface not supported
DP_LANE2+ DP_LANE2-	143 145	DisplayPort differential pair lines lane 2.	O PCIE		Shared with SDVO_BLUE+ and SDVO_BLUE- DisplayPort interface not supported
DP_LANE1+ DP_LANE1-	137 139	DisplayPort differential pair lines lane 1.	O PCIE		Shared with SDVO_GREEN+ and SDVO_GREEN- DisplayPort interface not supported
DP_LANE0+ DP_LANE0-	149 151	DisplayPort differential pair lines lane 0.	O PCIE		Shared with SDVO_RED+ and SDVO_RED- DisplayPort interface not supported
DP_AUX+ DP_AUX-	138 140	Auxiliary channel used for link management and device control. Differential pair lines.	I/O PCIE		Shared with SDVO_FLDSTALL+ and SDVO_FLDSTALL- DisplayPort interface not supported
DP_HPD#	154	Hot plug detection signal that serves as an interrupt request.	NC		DisplayPort interface not supported

Note

The DisplayPort interface signals are shared with the signals for the SDVO interface and/or the TMDS interface. DisplayPort interface is not supported on the conga-QA6.

Table 22 HDMI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS_CLK+ TMDS_CLK-	131 133	TMDS differential pair clock lines.	O TMDS		Shared with SDVO_BCLK+ and SDVO_BCLK- HDMI interface not supported
TMDS_LANE0+ TMDS_LANE0-	143 145	TMDS differential pair lines lane 0.	O TMDS		Shared with SDVO_BLUE+ and SDVO_BLUE- HDMI interface not supported
TMDS_LANE1+ TMDS_LANE1-	137 139	TMDS differential pair lines lane 1.	O TMDS		Shared with SDVO_GREEN+ and SDVO_GREEN- HDMI interface not supported
TMDS_LANE2+ TMDS_LANE2-	149 151	TMDS differential pair lines lane 2.	O TMDS		Shared with SDVO_RED+ and SDVO_RED- HDMI interface not supported
HDMI_CTRL_CLK	152	DDC based control signal (clock) for HDMI device.	I/O 3.3V OD		Shared with SDVO_CTRL_CLK HDMI interface not supported
HDMI_CTRL_DAT	150	DDC based control signal (data) for HDMI device.	I/O 3.3V OD		Shared with SDVO_CTRL_DAT HDMI interface not supported
HDMI_HPD#	153	Hot plug detection signal that serves as an interrupt request.	I 3.3V		HDMI interface not supported

Note

The TMDS interface signals are shared with the signals for the SDVO interface and/or the DisplayPort interface. HDMI interface is not supported on the conga-QA6.

Table 23 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	185 186 187 188	Multiplexed Command, Address and Data.	I/O 3.3V		
LPC_FRAME#	190	LPC frame indicates the start of a new cycle or the termination of a broken cycle.	O 3.3V		
LPC_LDRQ#	192	LPC DMA request.	I 3.3V		Not Supported
LPC_CLK	189	LPC clock.	O 3.3V		The LPC clock output operates at 1/4th of FSB frequency. By default, the LPC clock is only active when LPC bus transfers occur. Because of this behavior, LPC clock must be routed directly to the bus device; they cannot go through a clock buffer or other circuit that could delay the signal going to the end device.
SERIRQ	191	Serialized Interrupt.	I/O 3.3V	PU 10k 3.3V	

Table 24 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_MOSI	199	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	O 3.3V		
SPI_MISO	201	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	I 3.3V		
SPI_SCK	203	SPI clock output.	O 3.3V		
SPI_CS0#	200	SPI chip select 0 output.	O 3.3V		
SPI_CS1#	202	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	O 3.3V		Not Supported

Table 25 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	129	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	O 3.3V		
CAN0_RX	130	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	I 3.3V	PU 10k 3.3V	

Table 26 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	211-230	Power Supply +5VDC ±5%.	P		
VCC_5V_SB	205-206	Standby Power Supply +5VDC ±5%.	P		
VCC_RTC	193	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V).	P		
GND	1, 2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198	Power Ground.	P		

Table 27 Power Control Signal Descriptions

Signal	Pin #	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	26	High active input for the Qseven® module indicates that power from the power supply is ready.	I 5V	PU 10k 5V	
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge.	I 3.3VSB OD	PU 10k 3.3VSB	

Table 28 Power Management Signal Descriptions

Signal	Pin #	Description of Power Management signals	I/O	PU/PD	Comment
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module.	I 3.3V	PU 10k 3.3V	
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	I 3.3VSB	PU 10k 3.3VSB	
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	I 3.3VSB	PU 10k 3.3VSB	
SUS_STAT#	19	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3VSB		
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	O 3.3VSB		
SUS_S5#	16	S5 State: This signal indicates S4 or S5 (Soft Off) state.	O 3.3VSB		
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	I 3.3VSB	PU 10k 3.3VSB	
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again.	I 3.3VSB	PU 10k 3.3VSB	

Table 29 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	I 3.3V	PU 10k 3.3V	
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	O 3.3V		
I2C_CLK	66	Clock line of I²C bus.	I/O 3.3V OD	PU 4k99 3.3V	
I2C_DAT	68	Data line of I²C bus.	I/O 3.3V OD	PU 4k99 3.3V	
SMB_CLK	60	Clock line of System Management Bus.	I/O 3.3VSB OD	PU 10k 3.3VSB	
SMB_DAT	62	Data line of System Management Bus.	I/O 3.3VSB OD	PU 10k 3.3VSB	
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	I/O 3.3VSB OD	PU 10k 3.3V	
SPKR /GP_PWM_OUT2	194	Primary functionality is output for audio enunciator, the “speaker” in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
BIOS_DISABLE# /BOOT_ALT#	41	Module BIOS disable input signal. Pull low to disable module’s on-board BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a bootloader.	I 3.3V	PU 10k 3.3V	

Table 30 Manufacturing Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
MFG_NC0	207	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC1	209	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	Optional UART TxD
MFG_NC2	208	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	
MFG_NC3	210	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	NA	NA	Optional UART RxD
MFG_NC4	204	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes.	NA	NA	
RSVD	124	Do not connect.	NA	NA	

Note

The MFG_NC0..4 pins are reserved for manufacturing and debugging purposes. It's recommended to route the signals to a connector on the carrier board.

The carrier board must not drive the MFG_NC-pins or have pull-up or pull-down resistors implemented for these signals. MFG_NC0...4 are defined to have a voltage level of 3.3V. It must be ensured that the carrier board has the correct voltage levels for JTAG/UART signals originating from the module. For this reason, a level shifting device may be required on the carrier board to guarantee that these voltage levels are correct in order to prevent damage to the module.

More information about implementing a carrier board multiplexer can be found in the Qseven® Design Guide.

Table 31 Thermal Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I 3.3V	PU 10k 3.3V	
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off).	O 3.3VSB		

Table 32 Fan Control Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT /GP_PWM_OUT1	196	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V OC	PU 10k 3.3V	
FAN_TACHOIN /GP_TIMER_IN	195	Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.	I 3.3V		

8.1 Bootstrap Signals

Table 33 Bootstrap Signal Descriptions

Signal	Pin #	Description of Bootstrap Signal	I/O	PU/PD	Comment
GBE_LINK#	13	Ethernet controller 0 link indicator, active low.	O 2.5VSB	PD 1k	GBE0_LINK# is a bootstrap signal (see note below)
GBE_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 2.5VSB	PU 4k99 2,5VSB	Not Supported. Internally connected to GBE_ACT#. GBE0_LINK100# is a bootstrap signal (see note below)
GBE_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 2.5VSB	PD 1k	Not Supported. Internally connected to GBE_LINK# GBE0_LINK1000# is a bootstrap signal (see note below)
GBE_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 2.5VSB	PU 4k99 2,5VSB	GBE0_ACT# is a bootstrap signal (see note below)

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either Qseven® internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the Qseven® module to malfunction and/or cause irreparable damage to the module.

Additionally, if it is necessary to have link and activity LEDs connected to GBE_LINK# and GBE_ACT# on the carrier board, then buffers must be used since without a buffer the strapping becomes active and the PHY will be programmed to a wrong address.

9 System Resources

9.1 Interrupt Request (IRQ) Lines

Table 34 IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Can be used for
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		LPC bus via SERIRQ or PCIe bus via MSI
4	Yes		LPC bus via SERIRQ or PCIe bus via MSI
5	Yes		LPC bus via SERIRQ or PCIe bus via MSI
6	Yes		LPC bus via SERIRQ or PCIe bus via MSI
7	Yes		LPC bus via SERIRQ or PCIe bus via MSI
8	No	Real-time Clock	Not applicable
9	Note	SCI / Generic	LPC bus via SERIRQ or PCIe bus via MSI
10	Yes		LPC bus via SERIRQ or PCIe bus via MSI
11	Yes		LPC bus via SERIRQ or PCIe bus via MSI
12	Yes		LPC bus via SERIRQ or PCIe bus via MSI
13	No	Math coprocessor	Not applicable
14	Yes		LPC bus via SERIRQ or PCIe bus via MSI
15	Yes		LPC bus via SERIRQ or PCIe bus via MSI

MSI = Message Signal Interrupt (used by PCIe)

In PIC mode, the PCI bus interrupt lines can be routed to any free IRQ.

Note

In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCIe interrupt line.

Table 35 IRQ Lines in APIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		LPC bus via SERIRQ
4	Yes		LPC bus via SERIRQ
5	Yes		LPC bus via SERIRQ
6	Yes		LPC bus via SERIRQ
7	Yes		LPC bus via SERIRQ
8	No	Real-time Clock	Not applicable
9	Yes	Generic	LPC bus via SERIRQ, option for SCI
10	Yes		LPC bus via SERIRQ
11	Yes		LPC bus via SERIRQ
12	No		LPC bus via SERIRQ (Exclusively)
13	No	Math processor	Not applicable
14	Yes		LPC bus via SERIRQ
15	Yes		LPC bus via SERIRQ
16	Yes		Integrated graphics device, HDA controller, PCIe Bridge 0, PCIe Port 1 Slot, PCIe Port 2 Slot, PCIe Port 3 Slot, PCIe Root Port 0, PCIe Root Port 1, PCIe Root Port 2, PCIe Root Port 3
17	Yes		PCIe Bridge 0, PCIe Port 1 Slot, PCIe Port 2 Slot, PCIe Port 3 Slot
18	Yes		PCIe Bridge 0, PCIe Port 1 Slot, PCIe Port 2 Slot, PCIe Port 3 Slot
19	Yes		PCIe Bridge 0, PCIe Port 1 Slot, PCIe Port 2 Slot, PCIe Port 3 Slot
20	No		
21	No		
22	No		
23	No		

9.2 PCI Configuration Space

Table 36 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	01h	00h		Device ID4114h
00h	02h	00h	Internal	IGD (Integrated graphics device)
00h	03h	00h	Internal	SDVO Unit Display
00h	17h	00h	Internal	PCIe Port 0
00h	18h	00h	Internal	PCIe Port 1
00h	19h	00h	Internal	PCIe Port 2
00h	1Ah	00h	Internal	PCIe Port 3
00h	1Bh	00h	Internal	Intel High Definition Audio
00h	1Fh	00h	Internal	LPC Interface
01h	00h	00h	Internal	PCI Express Bridge
02h	00h	00h	Internal	Packet Hub Control
02h	00h	01h	Internal	Gigabit Ethernet MAC
02h	00h	02h	Internal	GPIO
02h	02h	00h	Internal	USB 2.0 OHCI Host 1
02h	02h	01h	Internal	USB 2.0 OHCI Host 1
02h	02h	02h	Internal	USB 2.0 OHCI Host 1
02h	02h	03h	Internal	USB 2.0 OHCI Host 1
02h	02h	04h	Internal	USB Device
02h	04h	00h	Internal	SDIO0
02h	04h	01h	Internal	SDIO1
02h	06h	00h	Internal	AHCI SATA Controller
02h	08h	00h	Internal	USB 2.0 OHCI Host 2
02h	08h	01h	Internal	USB 2.0 OHCI Host 2
02h	08h	02h	Internal	USB 2.0 OHCI Host 2
02h	08h	03h	Internal	USB 2.0 OHCI Host 2
02h	0Ah	00h	Internal	Shared DMA
02h	0Ah	01h	Internal	UART 0
02h	0Ah	02h	Internal	UART 1
02h	0Ah	03h	Internal	UART 2
02h	0Ah	04h	Internal	UART 3
02h	0Ch	00h	Internal	Shared DMA
02h	0Ch	01h	Internal	SPI
02h	0Ch	02h	Internal	I2C
02h	0Ch	03h	Internal	CAN
02h	0Ch	04h	Internal	IEEE1588

9.3 PCI Interrupt Routing

Table 37 PCI Interrupt Routing Map

PIRQ	PCIe BUS INT Line	APIC Mode IRQ	IGD	SDVO	HDA	PCIe Bridge 0	PCIe Bridge 1	PCIe Bridge 2	PCIe Bridge 3	PCIe Root Port 0	PCIe Root Port 1	PCIe Root Port 2	PCIe Root Port 3
A	INTA	16	x	x	x	x [2]	x [3]	x [4]	x [5]	x	x	x	x
B	INTB	17				x [3]	x [4]	x [5]	x [2]				
C	INTC	18				x [4]	x [5]	x [2]	x [3]				
D	INTD	19				x [5]	x [2]	x [3]	x [4]				
E		20											
F		21											
G		22											
H		23											

Note

[2] *Interrupt used by single function PCI Express devices (INTA).*

[3] *Interrupt used by multifunction PCI Express devices (INTB).*

[4] *Interrupt used by multifunction PCI Express devices (INTC).*

[5] *Interrupt used by multifunction PCI Express devices (INTD).*

10 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

10.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> key during POST.

10.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used a message will be displayed during POST stating that the "Boot Selection Popup menu has been selected" and the menu itself will be displayed immediately after POST thereby allowing the operator to choose the boot device to be used.

10.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

Main	Advanced	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display general help screen.
F2	Load previous values.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

10.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
BIOS ID	no option	Displays the BIOS ID.
OEM BIOS Version	no option	Displays the OEM BIOS ID.
Build Date	no option	Displays the date when the BIOS was built.
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
MAC Address	no option	Displays the MAC address of the board.
Running Time	no option	Displays the time the board is running [in hours max. 65535].
MRC Version	no option	Displays the MRC version number.
System Memory	no option	Displays the total amount of system memory.
Platform Information	submenu	Opens the platform information submenu.
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24-hour format.*
System Date	Day of week, month/day/year	Specifies the current system date. *Note: The date is in month-day-year format.*

10.4 Platform Information submenu

Feature	Options	Description
Processor Version	no option	Displays the silicon revision of the processor.
IGD VBIOS	no option	Displays the video BIOS version ID.
PUNIT Build Date	no option	Displays the PUNIT build date.
PUNIT Build Time	no option	Displays the PUNIT build time

10.5 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Power	Exit
	Graphic Configuration				
	Watchdog Configuration				
	PCI Subsystem Settings				
	ACPI Configuration				
	CPU Configuration				
	Chipset Configuration				
	AHCI SATA Configuration				
	SDIO Configuration				
	USB Configuration				
	Super IO Configuration				
	Serial Port Console Redirection				

10.5.1 Graphics Configuration Submenu

Feature	Options	Description
Primary Display	**Auto** IGD PEG	This option allows you to select the primary video device among internal graphic driver, external card or auto configuration.
Internal VGA Mode Select	Enabled, 4MB **Enabled, 8MB** Enabled, 16MB Enabled, 32MB Enabled, 64MB	This option allows you to disable the internal VGA controller or enable it with 1MB, 4MB, 8MB, 16MB, 32MB or 64MB initial frame buffer size.
MSAC Mode Select	Enabled 128MB **Enabled 256MB** Enabled 512MB	Determines the size of the graphics memory aperture.
IGD – Boot Type	**No option**	VBIOS default configuration
Boot Display Device	**Integrated SDVO** Integrated LVDS	Select the display device used for booting up.
Flat Panel Scaling	**Auto** Forced Disabled	Defines the flat panel scaling mode.
Flat Panel Type	Auto VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) **WVGA 800x480 1x24 (01Bh)** SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 1x18 (008h) Customized EDID 1 Customized EDID 2 Customized EDID 3	Select a predefined LFP type or choose "auto" to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.*
DPST Control	**VBIOS-Default** DPST Disabled DPST Enabled L1 DPST Enabled L2 DPST Enabled L3 DPST Enabled L4 DPST Enabled L5	Determines whether the VBIOS default controls the Display Power Save Technology or the setup configures the desired level.
Backlight Inverter Type	**None** PWM I2C	Select the type of backlight inverter used. PWM = Use IGD PWM signal.
PWM Inverter Frequency	200 - 40000	Select PWM inverter frequency. Default 20300.
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100**%	Actual backlight value in percent of the maximum setting.

Feature	Options	Description
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently. Hidden if "Backlight Inverter Type" is "None".
Invert Backlight Setting	**No** Yes	Allow to invert backlight control values if required for the actual backlight hardware controller. Hidden if "Backlight Inverter Type" is "None".

10.5.2 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset..
Stop Watchdog For User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One time trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to 'One time trigger' the watchdog will be disabled after the first trigger. If set to 'Single event', every stage will be executed only once, then the watchdog will be disabled. If set to 'Repeated event' the last stage will be executed repeatedly until a reset occurs.
Delay	see Post Watchdog	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	NMI ACPI Event **Reset** Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event see note below.
Event 2	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.

Feature	Options	Description
Timeout 1	0.5sec 1sec 2sec 5sec 10sec **30sec** 1min 2min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

10.5.3 PCI Subsystem Settings Submenu

Feature	Options	Description
PCI BUS Driver Version	**no option**	Displays the PCI Bus driver version ID number
PCI ROM Priority	**[EFI Compatible ROM]** Legacy ROM	In case of multiple Option ROMS, specifies what Option ROM is to be launched.
Launch PXE OpROM	**Disabled** Enabled	Allows the launching of PXE Option ROMS
Launch Storage OpROM	Disabled **Enabled**	Allows the launching of Storage Option ROMS
PCI Express Ports Configuration	submenu	Opens the platform information submenu.
PCI Latency Timer	32, 64, 96, ... 248	Specifies the PCI latency using bus clock units.
VGA Palette Snoop	**Disabled** Enabled	Enables or Disables VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enables or Disables PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enables or Disables PCI device to generate SERR#.
Relaxed Ordering	**Disabled** Enabled	Enables or Disables PCI Express device Relaxed Ordering.
Reserved Interrupt 1	**None** IRQ3 IRQ4 IRQ6 IRQ7 IRQ10 IRQ11 IRQ14 IRQ15	Reserves additional IRQ for custom purposes.

Feature	Options	Description
Reserved Interrupt 2	**None** IRQ3 IRQ4 IRQ6 IRQ7 IRQ10 IRQ11 IRQ14 IRQ15	Reserves additional IRQ for custom purposes.
PIRQ Routing	submenu	
Extended Tag	**Disabled** Enabled	Allows device to use 8-bit tag field as a requester.
No Snoop	**Disabled** Enabled	Enables or Disables PCI Express Device no snoop option.
Maximum Payload	**Auto**, 128, 256, 512, 1024, 2048, 4096	Sets the maximum payload value on bytes or allows the system BIOS to select the value.
Maximum Read Request	**Auto**, 128, 256, 512, 1024, 2048, 4096	Sets the maximum read request value on bytes or allows the system BIOS to select the value.
Automatic ASPM	**Disabled** Enabled	Enables or disables ASPM on reported capabilities and known issues.
Extended Synch	**Disabled** Enabled	Enables or disables the generation of extended synchronization patterns.

10.5.4 PCI Express Ports 1-4 Configuration Submenu

Feature	Options	Description
PCI Express Root Port 0..3	Disabled **Enabled**	Controls the PCI Express Root port.

10.5.5 PIRQ Routing Submenu

Feature	Options	Description
PIRQA...H	**Auto** IRQ3 IRQ4 IRQ6 IRQ7 IRQ10 IRQ11 IRQ14 IRQ15	Sets Interrupt for selected PIRQ. Refer to the board's Resource List for a detailed description of devices connected to the respective PIRQ. This setup node is only effective while operating in PIC (non IOAPIC) interrupt mode.

10.5.6 PCI to PCI Bridge Submenu

Feature	Options	Description
Extra Bus Reserved	**0**-7	Extra bus reserved for bridges behind the PCI root bridge. Range 0 to 7

10.5.7 ACPI Configuration Submenu

Feature	Options	Description
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or disables BIOS ACPI auto configuration
Enable Hibernation	**Disabled** Enabled	Enables or disables system ability to hibernate (OS/S4 Sleep State).
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend.
Sleep Button	Disabled **Enabled**	Allows the sleep button to drive the system to (or wake from) sleep state. This sleep state is defined by the OS.
Lid Function	Disabled **Enabled**	Allows the system's lid signal to drive the system to (or to wake from) sleep state. This sleep state is defined by the OS.
Critical Trip Point	70, 80, 90, 95, 100, 105, 110, 115, 120, **125**°C, Disabled	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Active Trip Point	Disabled, 30, 40, 50, **60**, 70, 80, 90, 95, 100°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Trip Point	Disabled, 30, 40, 50, 60, 70, 80, 90, **95**, 100°C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.

Note

In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

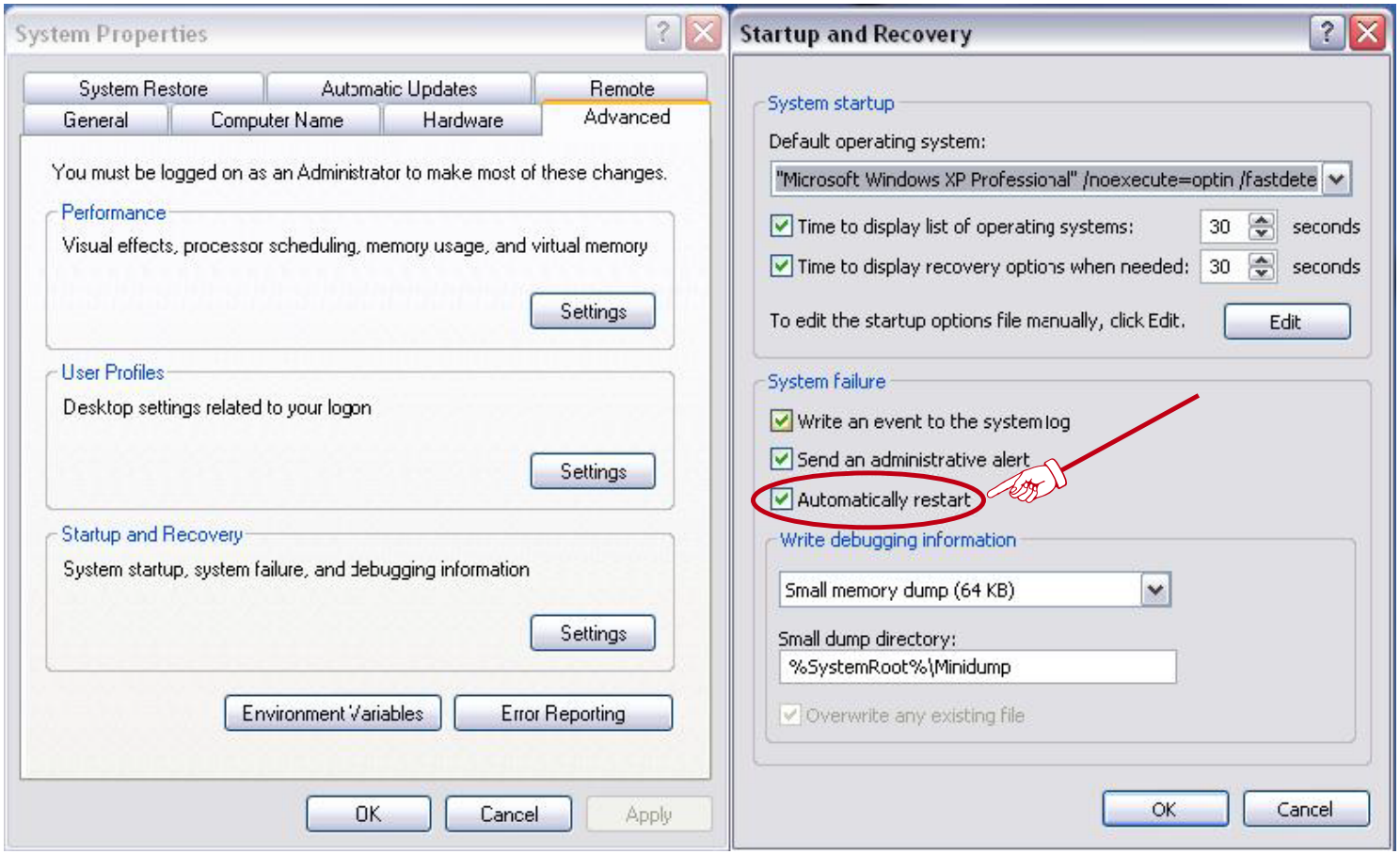
For Restart: An ACPI fatal error is reported to the OS.

It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP/2000 there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very

brief blue-screen the system will restart.

You can enable this setting buy going to the "System Properties" dialog box and choosing the "Advanced" tab. Once there choose the "Settings" button for the "Startup and Recovery" section. This will open the "Startup and Recovery" dialog box. In this dialog box under "System failure" there are three check boxes that define what Windows will do when a fatal error has been detected. In order to ensure that the system restarts after a 'Watchdog ACPI Event" that is set to 'Restart', you must make sure that the check box for the selection "Automatically restart" has been checked. If this option is not selected then Windows will remain at a blue-screen after a 'Watchdog ACPI Event" that has been configured for 'Restart' has been generated. Below is a Windows screen-shot showing the proper configuration.

Win XP/2000 Watchdog ACPI Event restart configuration



10.5.8 CPU Configuration Submenu

Feature	Options	Description
CPU Information	no option	Describes the CPU/Processor main parameters.
Intel(R) SpeedStep(tm)	Disabled **Enabled**	Disabled: CPU speed is set to maximum and cannot be altered by the operating system. Enabled: CPU speed is controlled by the operating system.
Hyperthreading	Disabled **Enabled**	Enables or disables Intel Hyperthreading Technology for being used by the OS.
Execute Disable Bit	Disabled **Enabled**	Enable or disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled, certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting OS.
Limit CPUID Maximum	**Disabled** Enabled	When enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When disabled, the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Intel Virtualization Technology	**Disabled** Enabled	When enabled, a VMM can utilize the additional hardware capabilities provided by the Vanderpool Technology.
C-States	**Disabled** Enabled	Enable support for supported standard CPU idle states.
C-State POPUP	**Enabled** Disabled	Enables or disables C-State POPUP.
Enhanced C-1	**Disabled** Enabled	Enables or disables the Enhanced C1 State.
Enhanced C-2	**Disabled** Enabled	Enables or disables the Enhanced C2 State.
Enhanced C-3	**Disabled** Enabled	Enables or disables the Enhanced C3 State.
Enhanced C-4	**Disabled** Enabled	Enables or disables the Enhanced C4 State.

10.5.9 Chipset Configuration Submenu

Feature	Options	Description
Audio Controller	Auto Enabled **Disabled**	Controls activation of the HDA controller device. Disabled = HDA controller will be unconditionally disabled Enabled = HDA controller will be unconditionally enabled Auto = HDA Controller will be enabled if HDA codec present, disabled otherwise.
Azalia PME Enable	Disabled **Enabled**	Enables or disables the Azalia PME (Power Management Events)
Azalia Vci Enable	Disabled **Enabled**	Enables or disables the Azalia Vci
SMBUS Controller	**Disabled** Enabled	Enables disables the SMBUS Controller
Network Settings	submenu	EG20T MAC Device configuration.
EG20T Ethernet PHY	**Enabled** Disabled during S5 Disabled during S3/S5 Disabled Always	Configures the Chip Power State of Ethernet PHY. Disable S5 and Disable S3/S5 set the PHY on Power off mode saving energy during the system ACPI Power States S3 or S5. Enable/Disabled always configures Power On/ Power off for all the ACPI states.
High Precision Timer	Disabled **Enabled**	Enable or disable the high precision event timer (HPET). This timer can be used for precise multimedia or real time application timing. Special software support is required.

Note

The BIOS does not initialize the HDA codec. The codecs remain in default mode and must be initialized by its respective device driver.

10.5.9.1 Network Settings Submenu

Feature	Options	Description
Network Stack	**Disabled** Enabled	Enable/Disable the Network Stack for PXE and UEFI.
Wake on LAN	Disabled **Enabled**	Enables/Disables WOL.
WOL Mode	**Wake Up Frame** Magic packet	Selects WOL Mode. Hidden if Wake on LAN is disabled.
WOL Speed	**10 Mbps** 100Mbps 1000Mbps	Selects WOL Speed. Hidden if Wake on LAN is disabled.

10.5.10 AHCI SATA Configuration

Feature	Options	Description
PORT 0	Disabled **Enabled**	This node enables or disables the Set Transfer mode programming for SATA port 0
PORT 1	Disabled **Enabled**	This node enables or disables the Set Transfer mode programming for SATA port 1

10.5.11 SDIO Configuration Submenu

Feature	Options	Description
SDIO Access Mode	**Auto** DMA PIO	Configures the access to the SD devices. With Auto, the controller determines the SD access method.

10.5.12 USB Configuration Submenu

Feature	Options	Description
USB Device List	no option	List of the USB devices connected to the system updated dynamically.
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
EHCI Hand-off	Disabled **Enabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device Start Unit command timeout.
Controller Timeout	1 sec 5 sec 10 sec **20 sec**	Timeout value for legacy USB control, bulk and interrupt transfers.
USB Mass Storage Device Name ***(Auto detected USB mass storage devices are listed here dynamically)***	**Auto** Floppy Forced FDD Hard Disk CD-ROM	Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. *Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.* ***Select AUTO to let the BIOS auto detect the current formatted media.*** If Floppy is selected then the device will be emulated as a floppy drive. Forced FDD allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. Hard Disk allows the device to be emulated as hard disk. CDROM assumes the CD-ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

10.5.13 Super I/O Configuration Submenu

Feature	Options	Description
Super IO Chip	**no option**	Displays Winbond SIO ID.
Serial Port 0 Configuration	submenu	Opens the Serial Port 0 Configuration submenu.
Serial Port 1 Configuration	submenu	Opens the Serial Port 1 Configuration submenu.
Wake on Ring	Disabled **Enabled**	Enables or disables SIO wake.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

10.5.13.1 Serial Port 0/1 Configuration Submenu

Feature	Options	Description
Serial Port 0	Disabled **Enabled**	Enable or disable serial port 0.
Device Settings	IO=3F8h; IRQ=4;	Fixed configuration of serial port 0 if enabled.
Change Settings	[Auto] [IO=3F8; IRQ=4] [IO=3F8 IRQ=3,4,5,6,7, 8, 9,10,11,12] [IO=2F8 IRQ=3,4,5,6,7, 8, 9,10,11,12] [IO=3E8 IRQ=3,4,5,6,7, 8, 9,10,11,12] [IO=2E8 IRQ=3,4,5,6,7, 8, 9,10,11,12]	Selects the IO port address and Interrupt for the SIO Port
Device Mode	**Normal** High Speed	Changes the serial port mode

10.5.14 Serial Port Console Redirection

Feature	Options	Description
COM0/COM1	no option	
Console Redirection	**Disabled** Enabled	Allows the Console Redirection Settings note selection
Console Redirection Settings	submenu	Opens the Serial Port 1/Port2 Console Redirection submenu. Only selectable when console redirection is enabled
Serial Port for Out-of-Band Management/ Windows EMS	no option	Serial Port for Out-of-Band Management/ Windows Emergency Management Services (EMS)
Console Redirection	**Disabled** Enabled	Allows the Serial redirection for Windows EMS
Out-of-Band Mgmt Port	**COM0** COM1 COM4	Defines the Serial Pot used for the Windows EMS
Terminal Type	VT100 VT100+ **VT-UTF8** ANSI	This note defines the Terminal Type used for the connection.

10.5.14.1 Console Redirection Settings

Feature	Options	Description
Console Redirection Setting	no option	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	**8** 7	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals. Software flow control uses start/stop ASCII chars, which slows down the data flow and can be problematic if binary data is being sent.
Recorder Mode	**Disabled** Enabled	On this mode enabled only text will be send. This is to capture Terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Legacy OS Redirection Resolution.

10.6 etup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.6.1 Boot Settings Configuration Submenu

Feature	Options	Description
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. *Note: The default OEM logo is a dark screen.*
Fast Boot	**Disabled** Enabled	Enables or disables UEFI fast boot with initialization of a minimal set of devices required to launch the active boot option.
Setup Prompt Timeout	**1** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot, 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. *Note: Only works with an ATX type power supply.*
AT Shutdown Mode	**System Reboot** Hot S5	Determines the system's behavior, when shutting down the system working on AT Mode. The system can reboot or stay on a Hot S5 power state. When the system is ATX powered this setup node has no effect.
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The "Device Based" boot priority list allows you to select from a list of currently detected devices only. The "Type Based" boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the "Device Based" boot priority list might change dynamically in cases when devices are physically removed or added to the system. The "Type Based" boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device (Up to 10 boot devices can be prioritized if device based priority list control is selected. If "Type Based" priority list control is enabled only 8 boot devices can be prioritized.)	Disabled SATA 0 Drive SATA 1 Drive Primary Master Secondary Master USB Floppy USB Harddisk USB CDROM Onboard LAN External LAN Other BEV Device	This view is only available when in the default "Type Based" mode. When in "Device Based" mode you will only see the devices that are currently connected to the system.
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
CSM16 Module Version	no option	Displays the CSM16 Version ID
GateA20 Active	**Upon Request** Always	Gate A20 control. Upon Request = Gate A20 can be disabled using BIOS services. Always = Do not allow disabling Gate A20.
Option ROM Messages	Force BIOS **Keep Current**	Set display mode for option ROMs.

Feature	Options	Description
Interrupt 19 Capture	**Disabled** Enabled	Defines whether option ROMs may trap the INT19h legacy boot vector.

10.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

10.7.1 Security Settings

Feature	Options	Description
Setup Administrator Password	Enter password	Specifies the setup administrator password.

10.8 Save & Exit

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen. You can display the Save & Exit screen option by highlighting it using the ← Arrow → Keys.

10.8.1 Save & Exit Menu

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	*Save changes and reset the system.*
Discard Changes and Reset	Reset the system without saving any changes.
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.

11 Additional BIOS Features

The conga-QA6 uses a congatec/AMI AptioEFI that is stored in an onboard SPI Flash chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as QTOPR1xx, where QTOP is the congatec internal BIOS project name for conga-QA6, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

11.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

11.2 BIOS Security Features

The BIOS provides a setup administrator password that limits access to the BIOS setup menu.

12 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Table 38 Industry Specifications

Specification	Link
Qseven® Specification	http://www.qseven-standard.org/
Qseven® Design Guide	http://www.qseven-standard.org/
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications