Qseven™ conga-QA

Intel® Atom™ ZX5xx series processors with an Intel® System Controller Hub US15W

User's Guide

Revision 1.1

Revision History

Revision	Date (dd.mm.yy)	Author	Changes
0.1	28.05.09	GDA	Preliminary release
0.2	10.06.09	GDA	Added “System Resources” section and updated “BIOS Setup Description” section.
1.0	19.06.09	GDA	Official release
1.1	08.04.10	GDA	Added “Inrush and Maximum Current Peaks on VCC_5V_SB and VCC” information to section 4.15. Corrected signal names in Table 3. Changed naming convention of pins Table 3 in compliance with Qseven specification. Added pin number column to tables in section 7 “Signal Descriptions and Pinout Tables.” Updated section 8 “System Resources” and section 9 “BIOS Setup Description.”

Preface

This user's guide provides information about the components, features, connector and BIOS Setup menus available on the conga-QA. It is one of three documents that should be referred to when designing a Qseven™ application. The other reference documents that should be used include the following:

Qseven™ Design Guide
Qseven™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
PCI Express (PCIe)	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4 or x16 link.
ExpressCard	A PCMCIA standard built on the latest USB 2.0 and PCI Express buses.
PCI Express Mini Card	PCI Express Mini Card add-in card is a small size unique form factor optimized for mobile computing platforms.
MMCplus	MMCplus was defined for first time in MMC System Specification v4.0. MMCplus is backward compatible with MMC. MMCplus has 13 pins.
SDIO card	SDIO (Secure Digital Input Output) is a non-volatile memory card format developed for use in portable devices.
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial-interface standard for hard disks
HDA	High Definition Audio
S/PDIF	S/PDIF (Sony/Philips Digital Interconnect Format) specifies a Data Link Layer protocol and choice of Physical Layer specifications for carrying digital audio signals between devices and stereo components.
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
LPC	Low Pin-Count: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy device support into a single IC.
I²C Bus	Inter-Integrated Circuit Bus: is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system.
SM Bus	System Management Bus: is a popular derivative of the I²C-bus.
GBE	Gigabit Ethernet
LVDS	Low-Voltage Differential Signaling
SDVO	Serial Digital Video Out is a proprietary technology introduced by Intel® to add additional video signaling interfaces to a system.
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

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- AMIBIOS8_HDD_Security.pdf
- AMIBIOS8-Flash-Recovery-Whitepaper.pdf
- AMIBIOS8_SerialRedirection.pdf
- AMIBIOS8 Setup User's Guide

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Qseven™ Concept

The Qseven™ concept is an off-the-shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven™ modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector. The pinout remains the same regardless of the vendor. The Qseven™ module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven™ module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The Qseven™ evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven™ I/O interfaces available and then choose what are suitable for their application. Qseven™ applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven™ modules. Simply unplug one module and replace it with another, no need to redesign the carrier board.

This document describes the features available on the Qseven evaluation carrier board. Additionally, the schematics for the Qseven™ evaluation carrier board can be found on the congatec website.

Certification

congatec AG is certified to DIN EN ISO 9001:2000 standard.

Technical Support

congatec AG technicians and engineers are committed to providing the best possible technical support for our customers so that our products can be easily used and implemented. We request that you first visit our website at www.congatec.com for the latest documentation, utilities and drivers, which have been made available to assist you. If you still require assistance after visiting our website then contact our technical support department by email at support@congatec.com

Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

conga-QA Options Information

The conga-QA is currently available in several different variants. This user's guide describes all of the available features these different variants offer. Below you will find an order table showing the base configuration modules that are currently offered by congatec AG. For more information about the additional conga-QA variants offered by congatec, contact your local congatec sales representative or visit the congatec website at www.congatec.com.

Part-No.	015001	015002
Processor	Intel® Atom™ Z510 1.1GHz	Intel® Atom™ Z530 1.6GHz
L2 Cache	512kB	512kB
Hyper-Threading Technology	No	Yes
Onboard Memory	1GB DDR2 (400 MT/s)	1GB DDR2 (533 MT/s)
External PCI Express Link(s)	1	1
Gigabit Ethernet	Yes	Yes
Onboard Solid-State Drive (SSD)	2GB	2GB
SATA	Yes	Yes
FSB	400MHz	533MHz
CPU TDP	2 W	2.3 W

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1 Specifications

1.1 Feature List

Table 1 Feature Summary

Form Factor	Based on Qseven™ form factor specification
Processor	Intel® Atom™ Z510 1.1GHz with 512kB L2 cache Intel® Atom™ Z530 1.6GHz with 512kB L2 cache with Hyper-Threading Technology
Memory	Onboard DDR 2 up to 1 GB
Chipset	Intel® System Controller Hub US15W
Audio	HDA (High Definition Audio)/digital audio interface with support for multiple codecs
Ethernet	Gigabit Ethernet, Realtek 8111 (uses one x1 PCI Express Link)
Graphics Options	Intel® Graphics Media Accelerator 500 (Intel® GMA 500), up to 8MB frame buffer supporting DirectX 9.0E and Open GL 2.0. Dual independent display support. • Flat panel Interface (integrated) 112MHz LVDS Transmitter Supports 1x18 and 1x24 bit TFT configurations. Supports both conventional (FPDI) and non-conventional (LDI) color mappings. Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3) Resolutions 640x480 up to 1366x768. • AUX Output 1 x Intel compliant SDVO port (serial DVO). Resolutions up to 1280x1024. Supports external DVI, TV and LVDS transmitters • Video Decode Acceleration: MPEG2 MPEG4 H.264 WMV9/VC1
Peripheral Interfaces	• 1x Serial ATA® (Provided by a PATA to SATA bridge) • 1x SDIO • 1x x1 PCI Express Link • 8x USB 2.0 (8 host ports, or 7 hosts + 1 client) • LPC Bus • I²C Bus, Fast Mode (400 kHz) multimaster
Onboard Storage	Optionally equipped with a Solid State Drive (SSD) up to 4 GByte in capacity
BIOS	Based on AMIBIOS8® 1 MByte Flash BIOS with congatec Embedded BIOS features
Power Management	ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 9 of this user's guide to determine what options are available on your particular module.

1.2 Supported Operating Systems

The conga-QA supports the following operating systems.

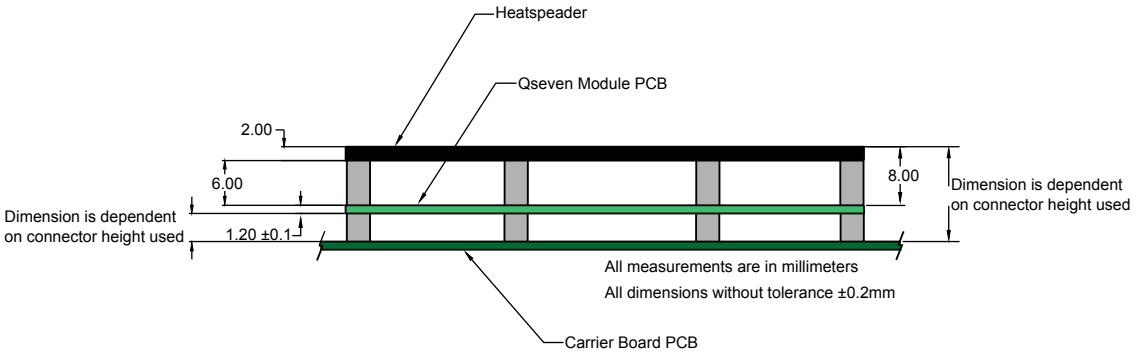
- Microsoft® Windows® 7
- Microsoft® Windows® XP
- Microsoft® Windows® XP Embedded
- Microsoft® Windows® CE 6.0
- Linux
- QNX

Note

DOS is not officially supported by the Intel® Menlow platform (Z5xx series processors and US15W System Controller Hub (SCH)). As a result of this it's possible that some legacy DOS based applications will not function properly when used in conjunction with the conga-QA. This limitation is due to the US15W SCH architecture, which is not designed for legacy applications.

1.3 Mechanical Dimensions

- 70.0 mm x 70.0 mm @ (2 ¾" x 2 ¾")
- The Qseven™ module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.

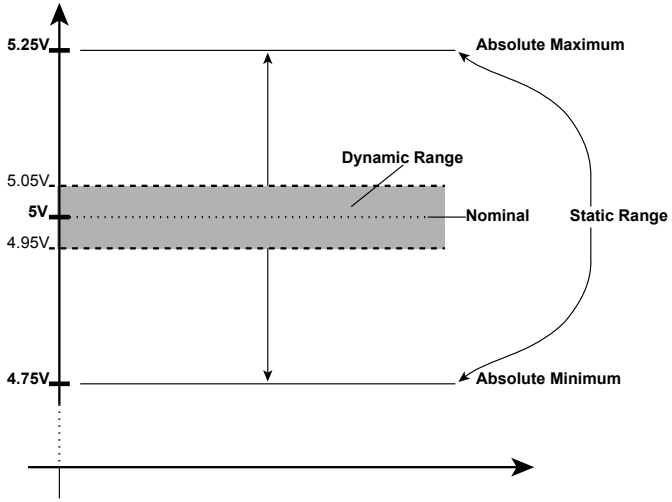


Rear View of Qseven Module

1.4 Supply Voltage Standard Power

- 5V DC ± 5%

The dynamic range shall not exceed the static range.



1.4.1 Electrical Characteristics

Characteristics			Min.	Typ.	Max.	Units	Comment
5V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV_{PP}	0-20MHz
	Current						
5V_SB	Voltage	± 5%	4.75	5.00	4.75	Vdc	
	Ripple				± 50	mV_{PP}	

1.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum rise time of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

Note

For information about the input power sequencing of the Qseven module refer to the Qseven specification.

1.5 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used includes a conga-QA module, conga-QEVAL, SATA drive, and USB keyboard. The SATA drive was powered externally by an ATX power supply so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. The module was first inserted into the conga-QEVAL, which was powered by a Direct Current (DC) power supply set to output 12V (the conga-QEVAL converts the input power to 5V). The current consumption value displayed by the DC power supply's readout is the value that is recorded as the power consumption measurement for Desktop Idle, 100% Workload and Standby modes. The power consumption of the conga-QEVAL (without module attached) was measured and this value was later subtracted from the overall power consumption value measured when the module and all peripherals were connected. All recorded values are approximate.

S3 mode was measured using the conga-QEVAL powered by an ATX power supply with a multimeter attached to the 5V Standby power line. The 5V Standby power consumption of the conga-QEVAL (without module attached) and all peripherals connected was first measured and the resulting value was later subtracted from the overall S3 power consumption value measured when the module was attached. All S3 recorded values are approximate.

Each module was measured while running Windows XP Professional with SP3 (service pack 3) and the "Power Scheme" was set to "Portable/ Laptop". This setting ensures that the Intel® Atom™ processors run in LFM (lowest frequency mode) with minimal core voltage during desktop idle. Power consumption values were recorded during the following stages:

Windows XP Professional SP2

- Desktop Idle (600MHz for the Intel® Atom™ Z510 and 800MHz for the Intel® Atom™ Z530)
- 100% CPU workload (see note below)
- Suspend to RAM (requires setup node "Suspend Mode" in BIOS to be configured to S3 STR (suspend to RAM)). Supply power for S3 mode is 5V.

Note

A software tool was used to stress the CPU to 100% workload.

Processor Information

In the following power tables there is some additional information about the processors. Intel® describes the type of manufacturing process used for each processor. The following term is used:

nm=nanometer

The manufacturing process description is included in the power tables. See example below. For information about the manufacturing process visit Intel®'s website.

Intel® Atom™ Z530 1.60GHz 512kB L2 cache
45nm

1.5.1 Intel® Atom™ Z510 1.1GHz 512kB L2 cache

With 1GB onboard memory and 2GB onboard SSD

conga-QA/510-1G Art. No. 015001	Intel® Atom™ Z510 1.1GHz 512kB L2 cache 45nm Layout Rev. QMENLA0 /BIOS Rev. QMENR005		
Memory Size	1GB onboard		
Operating System	Windows XP Professional SP3		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	0.7 A/3.5 W	0.9 A/4.5 W	0.06 A/0.3 W

1.5.2 Intel® Atom™ Z530 1.6GHz 512kB L2 cache

With 1GB onboard memory and 2GB onboard SSD

conga-QA/530-1G Art. No. 015002	Intel® Atom™ Z530 1.6GHz 512kB L2 cache 45nm Layout Rev. QMENLA0 /BIOS Rev. QMENR005		
Memory Size	1GB onboard		
Operating System	Windows XP Professional SP3		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	0.8 A/4.0 W	1.2 A/6.0 W	0.06 A/0.3 W

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

1.6 Supply Voltage Battery Power

- 2.0V-3.6V DC
- Typical 3V DC

1.6.1 CMOS Battery Power Consumption

RTC @ 20ºC	Voltage	Current
Integrated in the Intel® System Controller Hub US15W	3V DC	3.3 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

1.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

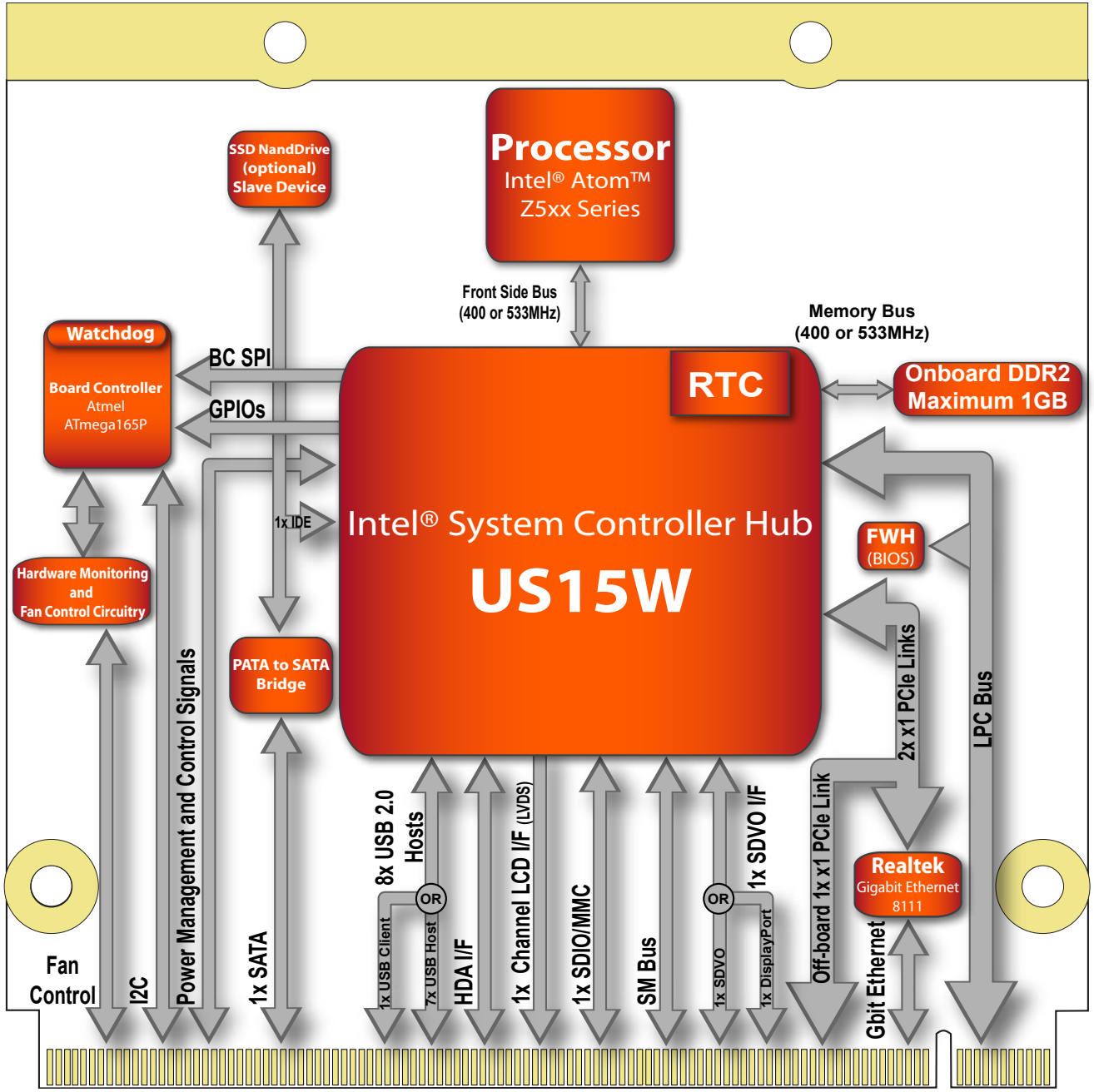
congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.

If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

For more information about operating a congatec module without heatspreader contact congatec technical support.

Humidity specifications are for non-condensing conditions.

2 Block Diagram



3 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module. It is a 2mm thick aluminum plate.

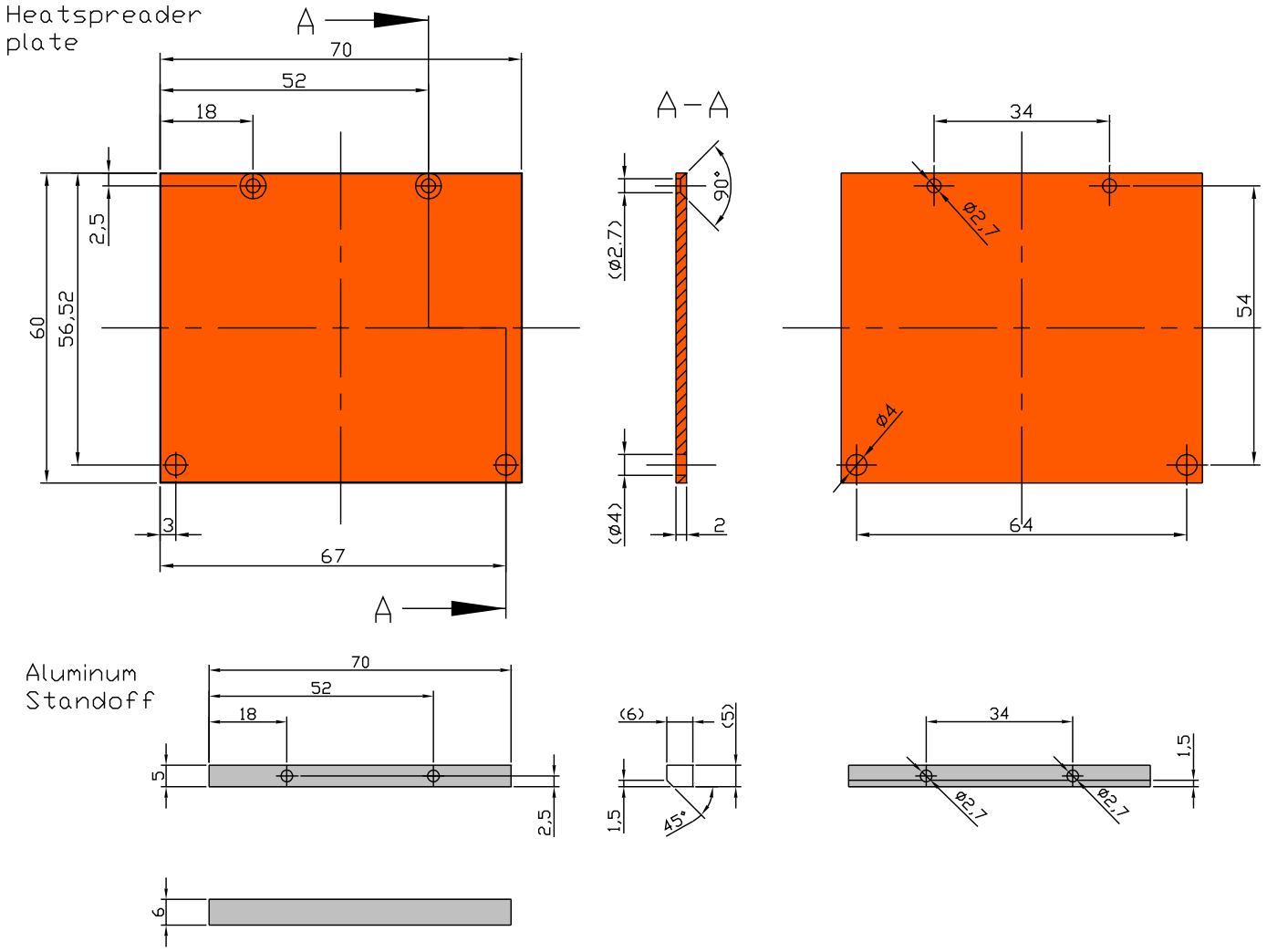
The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

Caution

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

3.1 Heatspreader and Aluminum Standoff Dimensions

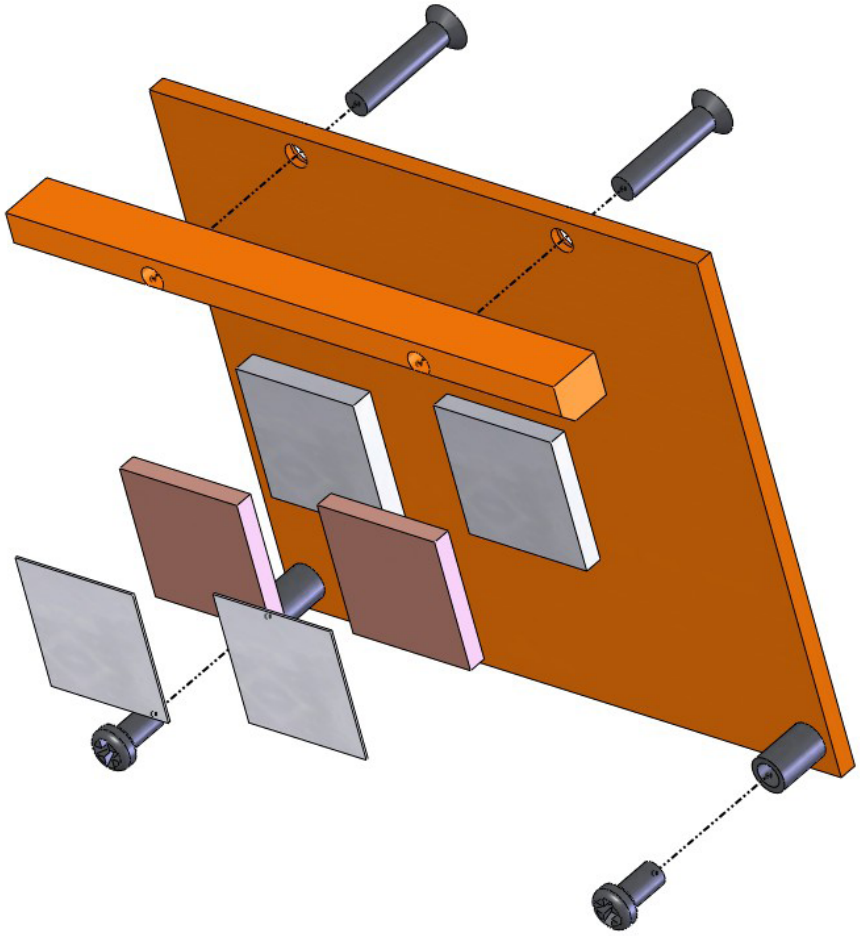


Note

All measurements are in millimeters. Torque specification for heatspreader screws is 0.5 Nm.

The cooling strip found on the conga-QA is connected directly to the ground plane when mounted in the conga-QEVAL evaluation carrier board. For more information about connecting the conga-QA's PCB cooling plate to the carrier board ground plane refer to the Qseven Design Guide.

3.2 Heatspreader and Aluminum Standoff Exploded View

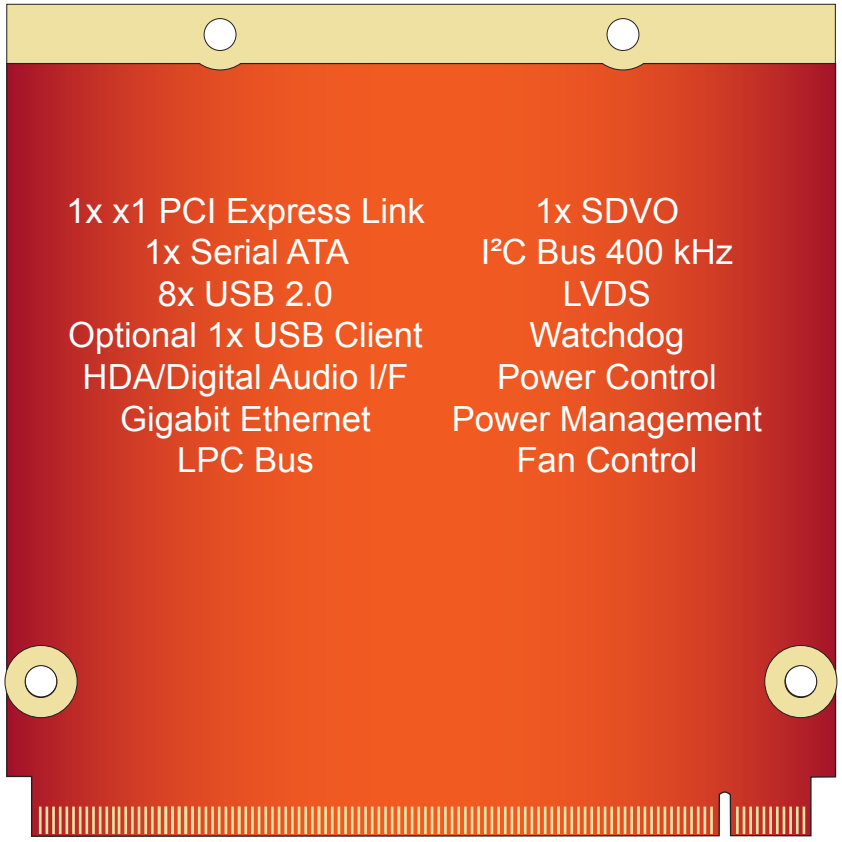


Note

Torque specification for heatspreader screws is 0.5 Nm.

4 Connector Subsystems

The conga-QA is based on the Qseven standard and therefore has 115 edge fingers on the top and bottom side of the module that mate with the 230-pin card-edge MXM connector located on the carrier board. This connector provides the ability to interface the available signals of the conga-QA with the carrier board peripherals.



Note

Not all the interfaces described above are available on all conga-QA variants. Use the article number of the module and refer to the options table on page 9 to determine the options available on the module.

4.1 PCI Express™

The conga-QA offers 2x x1 PCI Express links via the Intel® System Controller Hub US15W. One of these links is used for the onboard Gigabit Ethernet controller. One link is made available externally via the MXM connector on the carrier board and can be configured to support PCI Express edge cards or ExpressCards. The PCI Express interface is based on the PCI Express Specification 1.1.

Note

Not all variants of the conga-QA offer PCI Express links externally. Use the article number of the module and refer to the options table on page 9 to determine the options available on the module.

4.2 ExpressCard™

The conga-QA variants that provide PCI Express links at the connector can support the implementation of one ExpressCard, which requires the dedication of one USB port and one PCI Express link. Refer to section 7, “Signal Descriptions and Pinout Tables” for information about which ExpressCard port is supported.

Note

Not all variants of the conga-QA offer PCI Express links externally.

4.3 Gigabit Ethernet

The conga-QA is equipped with a Realtek 8111 Gigabit Ethernet Controller. This controller is implemented through the use of the second x1 PCI Express link found on the Intel® System Controller Hub US15W. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

Note

Not all variants of the conga-QA are equipped with a Gigabit Ethernet controller.

4.4 Serial ATA™ (SATA)

One Serial ATA (SATA) connection is provided by an IDE to Serial ATA bridge located on the conga-QA. The SATA device attached to this interface operates as a ‘Master’ device.

Note

Multiword DMA is not supported on the SATA interface. Not all variants of the conga-QA are equipped with a SATA interface.

4.5 USB 2.0

The conga-QA offers 3 UHCI USB host controllers and one EHCI USB host controller provided by the Intel® System Controller Hub US15W. These controllers comply with USB standard 1.1 and 2.0 and offer a total of 8 USB ports via card-edge MXM connector. Ports 0-5 are capable of supporting USB 1.1 and 2.0 compliant devices. Ports 6 and 7 are not multiplexed onto a UHCI controller, so they are only capable of high-speed operation and therefore only support the connection of USB 2.0 compliant devices. Additionally, the Intel® System Controller Hub US15W features a Universal Serial Bus 2.0 client controller. The USB client is configured to run on USB port 1. If the USB client controller is enabled then there are 7 host ports + 1 client port versus 8 host ports available on the conga-QA. For more information about the USB Client Controller and how the USB host controllers are routed see section 6.5 of this document.

4.6 SDIO/MMC

SDIO stands for Secure Digital Input Output. Devices that support SDIO can use small devices such as SD-Card or MMC-Card flash memories. The Intel® System Controller Hub US15W found on the conga-QA provides a SDIO/MMC expansion port used to communicate with a variety of SDIO and MMC devices. This port is available externally and supports SDIO Revision 1.1 and MMC Revision 4.0 and is backward-compatible with previous interface specifications.

Note

Only DOS and Linux (Ubuntu, Xandros) boot support for SDIO/MMC devices is available.

4.7 High Definition Audio (HDA)

The conga-QA provides an interface that supports the connection of HDA audio codecs.

4.8 Graphics Output (VGA/CRT)

The conga-QA does not provide a VGA/CRT output.

4.9 LCD

The Intel® System Controller Hub US15W, found on the conga-QA, offers an integrated single channel LVDS interface that is internally connected to Display Pipe B. It supports the connection of 1x18 or 1x24 Bit TFT configurations.

4.10 SDVO

conga-QA provides one SDVO port via Display Pipe A of the Intel® System Controller Hub US15W. The SDVO port can support a variety of display types (VGA, LVDS, DVI, TV-Out, etc.) by an external SDVO device.

4.11 TV-Out

The conga-QA does not offer a dedicated TV-Out interface. TV-Out can be made available via the SDVO interface offered by the conga-QA.

4.12 DisplayPort

DisplayPort is an open, industry standard digital display interface, that has been developed within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

The conga-QA does not offer a DisplayPort interface.

4.13 HDMI

High-Definition Multimedia Interface (HDMI) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video.

The conga-QA does not offer a HDMI interface.

4.14 LPC

conga-QA offers the LPC (Low Pin Count) bus through the use of the Intel® System Controller Hub US15W. There are already many devices available for this Intel® defined bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific carrier board using this bus.

4.15 Power Control

PWGIN

PWGIN (pin 26) can be connected to an external power good circuit or it may also be utilized as a manual reset input. In order to use PWGIN as a manual reset the pin must be grounded through the use of a momentary-contact push-button switch. When external circuitry asserts this signal, it's necessary that an open-drain driver drives this signal causing it to be held low for a minimum of 15ms to initiate a reset. Using this input is optional. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies, the conga-QA module is capable of generating its own power-on reset.

The conga-QA provides support for controlling ATX-style power supplies. In order to do this the power supply must provide a constant source of 5V power. When not using an ATX power supply then the conga-QA's pins SUS_S3, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#

The SUS_S3# (pin 18) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 20) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-QA. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-QA application:

- It has also been noticed that on some occasions problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush-current on the conga-QA VCC_5V_SB power rail can go up as high as 2.3A for a maximum of 100µS. Sufficient decoupling capacitance must be implemented to ensure proper power-up sequencing.

The maximum peak-current on the conga-QA VCC (5V) power rail can be as high as 3.0A. This requires that the power supply be properly dimensioned.

Note

For more information about power control event signals refer to the Qseven specification.

4.16 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

4.17 I²C Bus 400kHz

The I²C bus is implemented through the use of ATMEL ATmega165P microcontroller. It provides a Fast Mode (400kHz max.) multi-master I²C Bus that has maximum I²C bandwidth.

4.18 Watchdog

The conga-QA is equipped with a multi stage watchdog solution that can be triggered by software or external hardware. For more information about the Watchdog feature see the BIOS setup description section 9.4.11 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

4.19 Fan Control

conga-QA has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) Output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system fan's RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason a two pulse per revolution fan, or similar hardware solution, is recommended.

5 Additional Features

5.1 Onboard Microcontroller

The conga-QA is equipped with an ATMEL Atmega165P microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

5.2 Onboard Solid State Disk

A solid-state drive (SSD) is a data storage device that uses solid-state memory to store persistent data. A SSD is a hard disk drive without the traditional moving parts, thus easily replacing traditional hard drives in most applications. The conga-QA can be optionally equipped with a SSD up to 8 GByte in capacity. The SSD operates as a 'Slave' device. Due to the nature of NAND Flash technology there is a limitation of maximum write cycles related to each storage cell. According to the manufacturer datasheet an endurance of 10 million (for commercial MLC technology) or 100 million (for industrial SLC technology) write cycles is specified. Unlimited write cycles IS NOT specified. Since an advanced NAND memory management technology firmware is implemented in the SSD drive, it will balance the wear on erased blocks with an advanced wear-leveling algorithm, which provides a maximum of 10 million (or 100 million depending of the type of SSD used) product write cycles. In most applications this will be an acceptable and secure solution but it must be mentioned that the device lifetime will be affected mainly by the following parameters:

1. Operation time and used OS: If a 24/7 application is running under a write-intensive OS (such as Windows XP etc...) without EWF (Enhanced Write Filter), the amount of guaranteed write-cycles may be reached before the defined MTBF of the complete system.

2. The ratio between used and unused SSD capacity will also affect the lifetime. Since the wear-leveling algorithm uses access statistics for balancing the wears on the blocks, the SSD endurance will increase or decrease according to the amount of used and unused SSD space.

3. Given the information in parameters 1 and 2, if the SSD application is a 24/7 continuously running OS equipped SSD drive, with frequent write accesses and there is not enough free capacity available for wear leveling, the SSD endurance will decrease accordingly. For this reason it's necessary to avoid a configuration that will result in not enough free capacity being available for wear leveling and therefore it is required that an EWF mechanism is used thereby limiting the write-cycles in order to maintain sufficient free disk space. Failure to use a EWF mechanism will void the warranty of the SSD drive.

Note

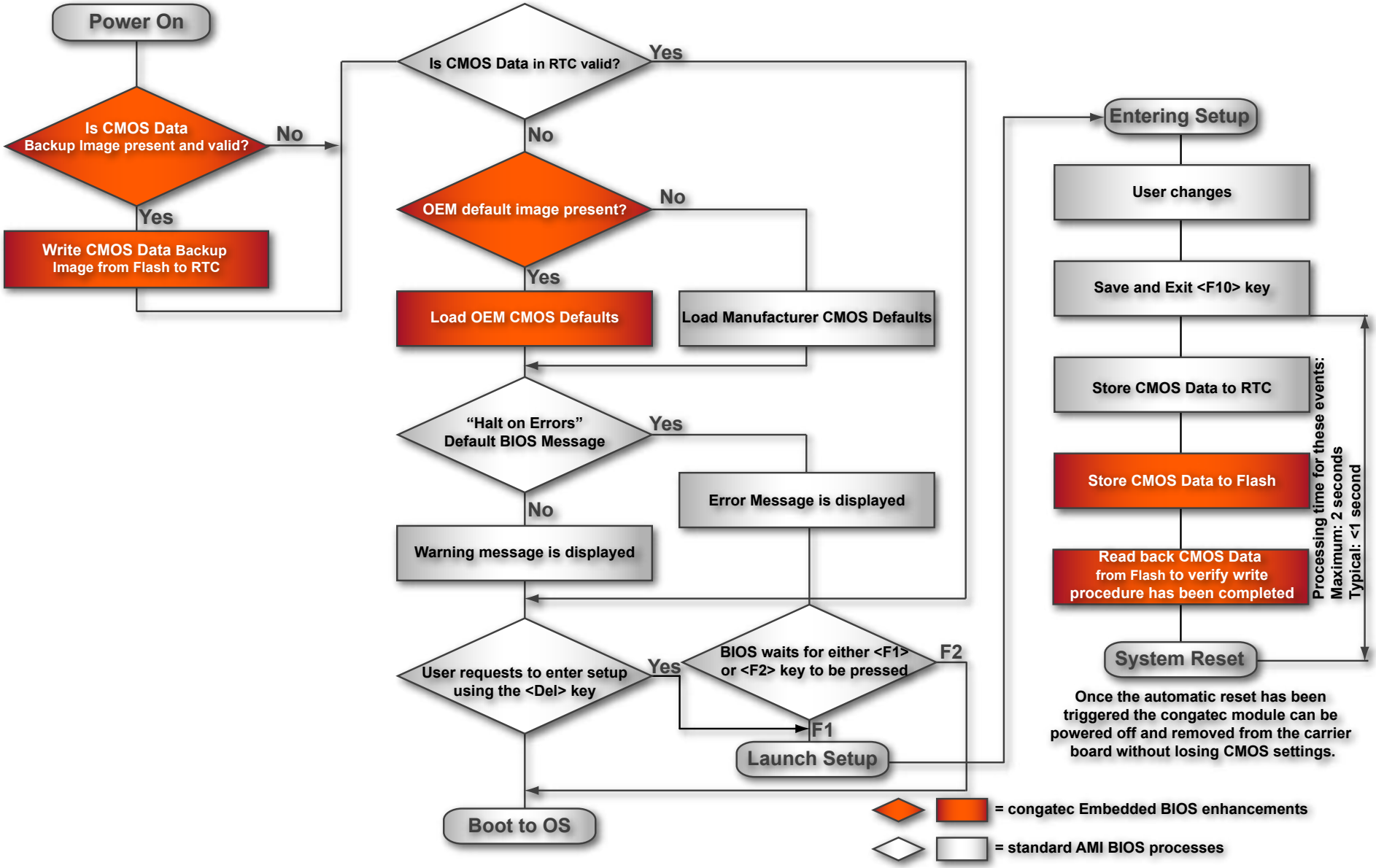
conga-QA variants that are equipped with the optional solid-state drive use SST NANDrive. For more information about this device refer to the manufactures datasheet.

5.3 Embedded BIOS

The conga-QA is equipped with congatec Embedded BIOS and has the following features:

- ACPI Power Management
- ACPI Battery Support
- Supports Customer Specific CMOS Defaults
- Multistage Watchdog
- User Data Storage
- Manufacturing Data and Board Information
- OEM Splash Screen
- Flat Panel Auto Detection and Backlight Control
- BIOS Setup Data Backup (see section 5.3.1)
- Fast Mode I²C Bus

5.3.1 Simplified Overview of BIOS Setup Data Backup



The above diagram provides an overview of how the BIOS Setup Data is backed up on congatec modules. OEM default values mentioned above refer to customer specific CMOS settings created using the congatec System Utility tool.

Once the BIOS Setup Program has been entered and the settings have been changed, the user saves the settings and exits the BIOS Setup Program using the F10 key feature. After the F10 function has been evoked, the CMOS Data is stored in a dedicated non-volatile CMOS Data Backup area located in the BIOS Flash Memory chip as well as RTC. The CMOS Data is written to and read back from the CMOS Data Backup area and verified. Once verified the F10 Save and Exit function continues to perform some minor processing tasks and finally reaches an automatic reset point, which instructs the module to reboot. After the Automatic Reset has been triggered the congatec module can be powered off and if need be removed from the baseboard without losing the new CMOS settings.

5.4 Suspend to RAM

The Suspend to RAM feature is available on the conga-QA.

5.5 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-QA BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide

6 conga Tech Notes

The conga-QA has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

6.1 Comparison of I/O APIC to 8259 PIC Interrupt mode

I/O APIC (Advanced Programmable Interrupt controller) mode deals with interrupts differently than the 8259 PIC.

The method of interrupt transmission used by APIC mode is implemented by transmitting interrupts through the system bus and they are handled without the requirement of the processor to perform an interrupt acknowledge cycle.

Another difference between I/O APIC and 8259 PIC is the way the interrupt numbers are prioritized. Unlike the 8259 PIC, the I/O APIC interrupt priority is independent of the actual interrupt number.

A major advantage of the I/O APIC found in the chipset of the conga-QA is that it's able to provide more interrupts, a total of 24 to be exact. It must be mentioned that the APIC is not supported by all operating systems. In order to utilize the APIC mode it must be enabled in the BIOS setup program before the installation of the OS and it only functions in ACPI mode. You can find more information about APIC in the IA-32 Intel Architecture Software Developer's Manual, Volume 3 in chapter 8.

Note

You must ensure that your operating system supports APIC mode in order to use it.

6.2 Intel® Processor Features

6.2.1 Thermal Monitor and Catastrophic Thermal Protection

Intel® Atom™ Z5xx series processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature, that the Intel® Thermal Monitor uses to activate the TCC, cannot be configured by the user nor is it software visible.

The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel® Speedstep transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.

Note

The maximum operating temperature for Intel® Atom™ Z5xx series processors is 100°C.

Two modes are supported by the Thermal Monitor to activate the TCC. They are called Automatic and On-Demand. No additional hardware, software, or handling routines are necessary when using Automatic Mode.

Note

To ensure that the TCC is active for only short periods of time thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Atom™ Z5xx series processor's respective datasheet can provide more information about this subject.

6.2.2 Processor Performance Control

Intel® Atom™ Z5xx series processors run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it's not being fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting found in the control panel option applet.

Note

If the "Home/Office" or "Always On" power scheme is selected when using Windows operating systems then the processor will always run at the highest performance state. For more information about this subject see chapter 8 of the ACPI Specification Revision 2.0c, which can be found at www.acpi.info . Also visit Microsoft's website and search for the document called "Windows Native Processor Performance Control".

6.2.3 Intel® Virtualization Technology

Virtualization solutions enhanced by Intel® VT will allow Intel® Atom™ Z5xx series processors, that feature 2 Thread Support, to run multiple operating systems and applications in independent partitions. When using virtualization capabilities, one computer system can function as multiple “virtual” systems. With processor and I/O enhancements to Intel®’s various platforms, Intel® Virtualization Technology can improve the performance and robustness of today’s software-only virtual machine solutions.

Intel® VT is a multi-generational series of extensions to Intel® processor and platform architecture that provides a new hardware foundation for virtualization, establishing a common infrastructure for all classes of Intel® based systems. The broad availability of Intel® VT makes it possible to create entirely new applications for virtualization in servers, clients as well as embedded systems thus providing new ways to improve system reliability, manageability, security, and real-time quality of service.

The success of any new hardware architecture is highly dependent on the system software that puts its new features to use. In the case of virtualization technology, that support comes from the virtual machine monitor (VMM), a layer of software that controls the underlying physical platform resources sharing them between multiple “guest” operating systems. Intel® VT is already incorporated into most commercial and open-source VMMs including those from VMware, Microsoft, XenSource, Parallels, Virtual Iron, Jaluna and TenAsys.

You can find more information about Intel Virtualization Technology at: http://developer.intel.com/technology/virtualization/index.htm

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

6.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system’s thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-QA ACPI thermal solution offers three different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the “passive cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the “active cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the “critical trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled according to the formula below.

$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

- *ΔP is the performance delta*
- *T_t is the target temperature = critical trip point*
- *The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants. These constants are set to fixed values for the conga-QA:*
- *TC1= 1*
- *TC2= 5*
- *TSP= 5 seconds*

See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

6.4 ACPI Suspend Modes and Resume Events

conga-QA supports the S3 (STR= Suspend to RAM) power state. For more information about S3 wake events see section 9.4.1 “ACPI Configuration Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by some operating systems (S4_OS= Hibernate). Check with the operating system vendor to determine if S4 (Suspend to Disk) is supported.

This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3 and S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event. USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu. Under Windows XP add following registry entries: Add this key: HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\usb Under this key add the following value: “USBBIOSx“=DWORD:00000000 *Note that Windows XP disables USB wakeup from S3, so this entry has to be added to re-enable it.* Configure USB keyboard/mouse to be able to wake up the system: In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check ‘Allow this device to bring the computer out of standby’. *Note: When the standby state is set to S3 in the ACPI setup menu, the power management tab for USB keyboard /mouse devices only becomes available after adding the above registry entry and rebooting to allow the registry changes to take affect.*
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu.
Watchdog Power Button Event	Wakes unconditionally from S3 and S5.

Note

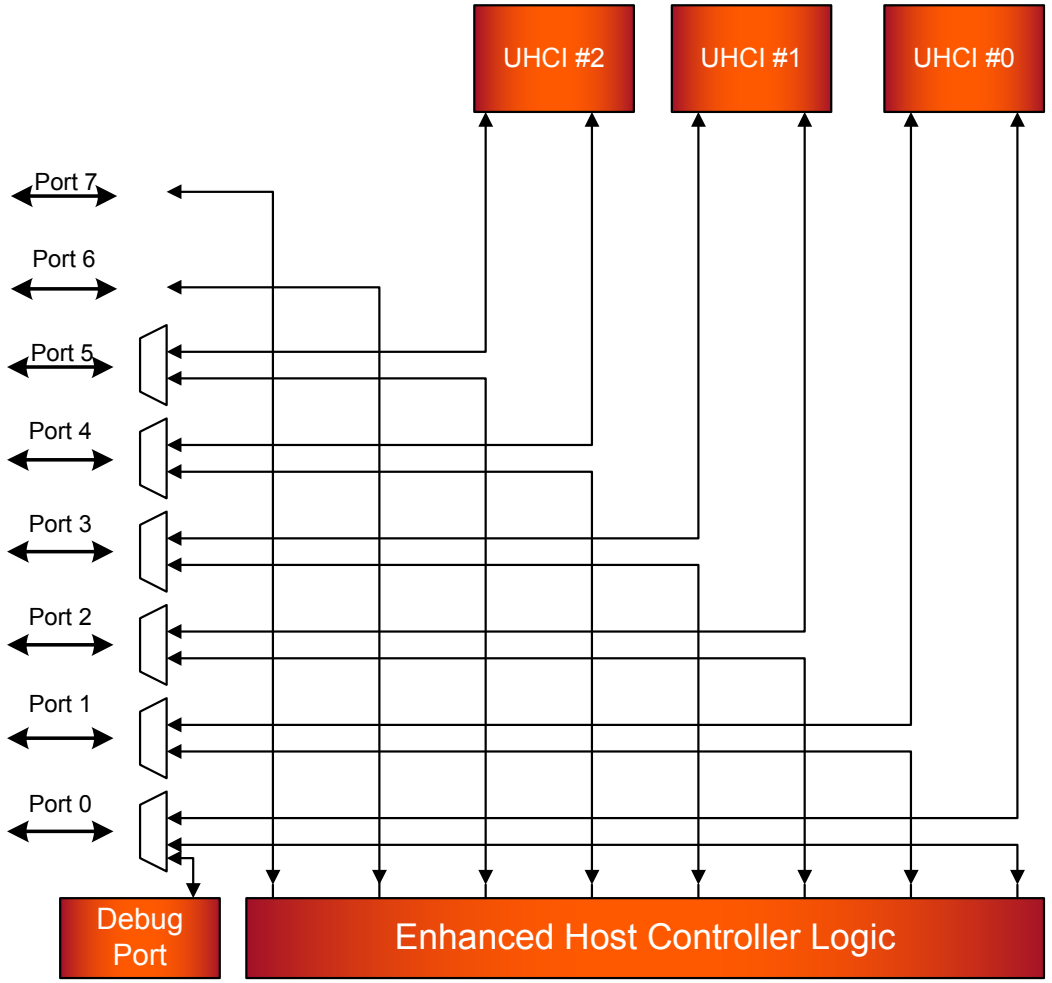
The above list has been verified using a Windows XP SP2 ACPI enabled installation.

6.5 USB Port Connections

The 8 USB ports are shared between an EHCI host controller and the 3 UHCI host controllers.

Within the EHC functionality there is a port-routing logic that executes the mixing between the two different types of host controllers (EHCI and UHCI). This means that when a USB device is connected the routing logic determines who owns the port. If the device is not USB 2.0 compliant, or if the software drivers for EHCI support are not installed, then the UHCI controller owns the ports. Ports 0-5 are capable of supporting USB 1.1 and 2.0 compliant devices. Ports 6 and 7 are not multiplexed onto a UHCI controller, so they are only capable of high-speed operation and therefore only support the connection of USB 2.0 compliant devices.

Routing Diagram



6.5.1 USB Client Controller

The Intel US15W system controller hub located on the conga-QA features a Universal Serial Bus 2.0 client controller that is configured to run on USB port 2. This means that if the USB client controller is enabled then 7 of the 8 available USB ports are host ports and 1 is a client port. This USB client controller allows the conga-QA to connect to other computer systems that utilize a USB Host interface. Once connected, the conga-QA has the ability to perform tasks supported by common USB devices. This can include, but is not limited to, such functionality as data transfer and network access.

This USB client implementation is designed to achieve maximum flexibility while maintaining hardware simplicity. Most of the behavior above the DMA and USB protocol layer is the responsibility of software. This includes Transaction level formatting, handling USB Descriptors and the implementation of defined Device Classes.

For information about USB Client software installation on the conga-QA refer to the document “USBC_ReleaseNotes.pdf” found in the USB Client driver packet located in the conga-QA driver section at www.congatec.com.

Detailed information about the USB Client Controller is beyond the scope of this document. For more information refer to the Intel® System Controller Hub US15W datasheet.

Note

The US15W system controller hub USB client Port 2 is routed to USB Port 1 on the conga-QA.

7 Signal Descriptions and Pinout Tables

The following section describes the signals found on Qseven™ module's edge fingers.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a Qseven™ module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Not all the signals described in this section are available on all conga-QA variants. Use the article number of the module and refer to the options table on page 9 to determine the options available on the module.

Table 2 Signal Tables Terminology Descriptions

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PP	Push Pull
I/O	Bi-directional Input/Output Pin
P	Power Input
NC	Not Connected
PCIE	PCI Express differential pair signals. In compliance with the PCI Express Base Specification 1.1.
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet Specification.
USB	Universal Serial Bus differential pair signals. In compliance with the Universal Serial Bus Specification 2.0
SATA	Serial Advanced Technology Attachment differential pair signals. In compliance with the Serial ATA High Speed Serialized AT Attachment Specification 1.0a.
SPI	Serial Peripheral Interface bus is a synchronous serial data link that operates in full duplex mode.
CAN	Controller Area Network bus is a vehicle bus standard that allows microcontrollers and devices to communicate with each other within a vehicle without a host computer.
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

Table 3 Edge Finger Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Power Ground	2	GND	Power Ground
3	GBE_MDI3-	Gigabit Ethernet MDI3-	4	GBE_MDI2-	Gigabit Ethernet MDI2-
5	GBE_MDI3+	Gigabit Ethernet MDI3+	6	GBE_MDI2+	Gigabit Ethernet MDI2+
7	GBE_LINK100#	100 Mbps link speed	8	GBE_LINK1000#	1000 Mbps link speed
9	GBE_MDI1-	Gigabit Ethernet MDI1-	10	GBE_MDI0-	Gigabit Ethernet MDI0-
11	GBE_MDI1+	Gigabit Ethernet MDI1+	12	GBE_MDI0+	Gigabit Ethernet MDI0+
13	GBE_LINK#	Gigabit Ethernet Link indicator	14	GBE_ACT#	Gigabit Ethernet Activity indicator
15	GBE_CTREF (*)	Reference voltage for GBE	16	SUS_S5#	S5 (Soft OFF) – shutdown state
17	WAKE#	External system wake event	18	SUS_S3#	S3 (Suspend to RAM) – SLP
19	SUS_STAT#	Suspend status	20	PWRBTN#	Power button
21	SLP_BTN#	Sleep button	22	LID_BTN#	LID button
23	GND	Power Ground	24	GND	Power Ground
25	GND	Power Ground	26	PWGIN	Power good input
27	BATLOW#	Battery low input	28	RSTBTN#	Reset button input
29	SATA0_TX+	Serial ATA Channel 0 TX+	30	SATA1_TX+(*)	Serial ATA Channel 1 TX+
31	SATA0_TX-	Serial ATA Channel 0 TX-	32	SATA1_TX- (*)	Serial ATA Channel 1 TX-
33	SATA_ACT#	Serial ATA Activity	34	GND	Power Ground
35	SATA0_RX+	Serial ATA Channel 0 RX+	36	SATA1_RX+ (*)	Serial ATA Channel 1 RX+
37	SATA0_RX-	Serial ATA Channel 0 RX-	38	SATA1_RX- (*)	Serial ATA Channel 1 RX-
39	GND	Power Ground	40	GND	Power Ground
41	BIOS_DISABLE# /BOOT_ALT#	BIOS Module disable Boot Alternative Enable	42	SDIO_CLK	SDIO Clock Output
43	SDIO_CD#	SDIO Card Detect	44	SDIO_LED	SDIO LED
45	SDIO_CMD	SDIO Command/Response	46	SDIO_WP	SDIO Write Protect
47	SDIO_PWR#	SDIO Power Enable	48	SDIO_DAT1	SDIO Data Line 1
49	SDIO_DAT0	SDIO Data Line 0	50	SDIO_DAT3	SDIO Data Line 3
51	SDIO_DAT2	SDIO Data Line 2	52	SDIO_DAT5	SDIO Data Line 5
53	SDIO_DAT4	SDIO Data Line 4	54	SDIO_DAT7	SDIO Data Line 7
55	SDIO_DAT6	SDIO Data Line 6	56	RESERVED	
57	GND	Power Ground	58	GND	Power Ground
59	HDA_SYNC	HD Audio/AC'97 Synchronization	60	SMB_CLK	SMBus Clock line
61	HDA_RST#	HD Audio/AC'97 Codec Reset	62	SMB_DAT	SMBus Data line
63	HDA_BITCLK	HD Audio/AC'97 Serial Bit Clock	64	SMB_ALERT#	SMBus Alert input
65	HDA_SDI	HD Audio/AC'97 Serial Data In	66	I2C_CLK	I2C Bus Clock
67	HDA_SDO	HD Audio/AC'97 Serial Data Out	68	I2C_DAT	I2C Bus Data
69	THRM#	Thermal Alarm active low	70	WDTRIG#	Watchdog trigger signal
71	THRMTRIP# (*)	Thermal Trip indicates an overheating condition	72	WDOUT	Watchdog event indicator
73	GND	Power Ground	74	GND	Power Ground
75	USB_P7-	USB Port 7 Differential Pair-	76	USB_6P-	USB Port 6 Differential Pair-

Pin	Signal	Description	Pin	Signal	Description
77	USB_P7+	USB Port 7 Differential Pair+	78	USB_6P+	USB Port 6 Differential Pair+
79	USB_6_7_OC#	Over current detect input 6/7 USB	80	USB_4_5_OC#	Over current detect input 4/5 USB
81	USB_5P-	USB Port 5 Differential Pair-	82	USB_4P-	USB Port 4 Differential Pair-
83	USB_5P+	USB Port 5 Differential Pair+	84	USB_4P+	USB Port 4 Differential Pair+
85	USB_2_3_OC#	Over current detect input 2/3 USB	86	USB_0_1_OC#	Over current detect input 0/1 USB
87	USB_3P-	USB Port 3 Differential Pair-	88	USB_2P-	USB Port 2 Differential Pair-
89	USB_3P+	USB Port 3 Differential Pair+	90	USB_2P+	USB Port 2 Differential Pair+
91	USB_CC	USB Client present detect pin	92	USB_ID	USB ID pin
93	USB_1P-	USB Port 1 Differential Pair-	94	USB_0P-	USB Port 0 Differential Pair-
95	USB_1P+	USB Port 1 Differential Pair+	96	USB_0P+	USB Port 0 Differential Pair+
97	GND	Power Ground	98	GND	Power Ground
99	LVDS_A0+	LVDS Primary channel 0+	100	LVDS_B0+ (*)	LVDS Secondary channel 0+
101	LVDS_A0-	LVDS Primary channel 0-	102	LVDS_B0- (*)	LVDS Secondary channel 0-
103	LVDS_A1+	LVDS Primary channel 1+	104	LVDS_B1+ (*)	LVDS Secondary channel 1+
105	LVDS_A1-	LVDS Primary channel 1-	106	LVDS_B1- (*)	LVDS Secondary channel 1-
107	LVDS_A2+	LVDS Primary channel 2+	108	LVDS_B2+ (*)	LVDS Secondary channel 2+
109	LVDS_A2-	LVDS Primary channel 2-	110	LVDS_B2- (*)	LVDS Secondary channel 2-
111	LVDS_PPEN	LVDS Power enable	112	LVDS_BLEN	LVDS Backlight enable
113	LVDS_A3+	LVDS Primary channel 3+	114	LVDS_B3+ (*)	LVDS Secondary channel 3+
115	LVDS_A3-	LVDS Primary channel 3-	116	LVDS_B3- (*)	LVDS Secondary channel 3-
117	GND	Power Ground	118	GND	Power Ground
119	LVDS_A_CLK+	LVDS Primary channel CLK+	120	LVDS_B_CLK+ (*)	LVDS Secondary channel CLK+
121	LVDS_A_CLK-	LVDS Primary channel CLK-	122	LVDS_B_CLK- (*)	LVDS Secondary channel CLK-
123	LVDS_BLT_CTRL /GP_PWM_OUT0	PWM Backlight brightness General Purpose PWM Output	124	RESERVED	
125	LVDS_DID_DAT /GP_I2C_DAT	DDC Display ID Data line General Purpose I2C Data line	126	LVDS_BLC_DAT	SSC clock chip data line
127	LVDS_DID_CLK //GP_I2C_CLK	DDC Display ID Clock line General Purpose I2C Clock line	128	LVDS_BLC_CLK	SSC clock chip clock line
129	CAN0_TX (*)	CAN TX Output for CAN Bus Channel 0	130	CAN0_RX (*)	CAN RX Input for CAN Bus Channel 0
131	SDVO_BCLK+	SDVO Clock line+	132	SDVO_INT+	SDVO Interrupt line+
133	SDVO_BCLK-	SDVO Clock line-	134	SDVO_INT-	SDVO Interrupt line-
135	GND	Power Ground	136	GND	Power Ground
137	SDVO_GREEN+	SDVO Green line+	138	SDVO_FLDINSTALL+	SDVO Field stall line+
139	SDVO_GREEN-	SDVO Green line-	140	SDVO_FLDINSTALL-	SDVO Field stall line-
141	GND	Power Ground	142	GND	Power Ground
143	SDVO_BLUE+	SDVO Blue line+	144	SDVO_TVCLKIN+	SDVO TV-Out line+
145	SDVO_BLUE-	SDVO Blue line-	146	SDVO_TVCLKIN-	SDVO TV-Out line-
147	GND	Power Ground	148	GND	Power Ground
149	SDVO_RED+	SDVO Red line+	150	SDVO_CTRL_DAT	I2C based control clock for SDVO
151	SDVO_RED-	SDVO Red line-	152	SDVO_CTRL_CLK	I2C based control data for SDVO

Pin	Signal	Description	Pin	Signal	Description
153	HDMI_HPD# (*)	Hot plug detection for HDMI	154	DP_HPD# (*)	Hot plug detection for Display port
155	PCIE_CLK_REF+	PCI Express Reference Clock+	156	PCIE_WAKE#	PCI Express Wake event
157	PCIE_CLK_REF-	PCI Express Reference Clock-	158	PCIE_RST#	Reset Signal for external devices
159	GND	Power Ground	160	GND	Power Ground
161	PCIE3_TX+ (*)	PCI Express Channel 3 Output+	162	PCIE3_RX+ (*)	PCI Express Channel 3 Input+
163	PCIE3_TX- (*)	PCI Express Channel 3 Output-	164	PCIE3_RX- (*)	PCI Express Channel 3 Input-
165	GND	Power Ground	166	GND	Power Ground
167	PCIE2_TX+ (*)	PCI Express Channel 2 Output+	168	PCIE2_RX+ (*)	PCI Express Channel 2 Input+
169	PCIE2_TX- (*)	PCI Express Channel 2 Output-	170	PCIE2_RX- (*)	PCI Express Channel 2 Input-
171	EXCD0_PERST#	Express Card slot#0 reset	172	EXCD1_PERST# (*)	Express Card slot#1 reset
173	PCIE1_TX+	PCI Express Channel 1 Output+	174	PCIE1_RX+	PCI Express Channel 1 Input+
175	PCIE1_TX-	PCI Express Channel 1 Output-	176	PCIE1_RX-	PCI Express Channel 1 Input-
177	EXCD0_CPPE#	Express Card slot#0 Capable/Req	178	EXCD1_CPPE# (*)	Express Card slot#0 Capable/Req
179	PCIE0_TX+	PCI Express Channel 0 Output+	180	PCIE0_RX+	PCI Express Channel 0 Input+
181	PCIE0_TX-	PCI Express Channel 0 Output-	182	PCIE0_RX-	PCI Express Channel 0 Input-
183	GND	Power Ground	184	GND	Power Ground
185	LPC_AD0	LPC Interface Address/Data 0	186	LPC_AD1	LPC Interface Address/Data 1
187	LPC_AD2	LPC Interface Address/Data 0	188	LPC_AD3	LPC Interface Address/Data 3
189	LPC_CLK	LPC Interface Clock	190	LPC_FRAME#	LPC frame indicator
191	SERIRQ	Serialized interrupt	192	LPC_LDRQ# (*)	LPC DMA request
193	VCC_RTC	3V backup cell input	194	SPKR /GP_PWM_OUT2	Output for audio enunciator General Purpose PWM Output
195	FAN_TACHOIN /GP_TIMER_IN	Fan tachometer input General Purpose Timer In	196	FAN_PWMOUT /GP_PWM_OUT1	Fan speed control (PWM) General Purpose PWM Output
197	GND	Power Ground	198	GND	Power Ground
199	SPI_MOSI (*)	SPI Master serial output/Slave serial input	200	SPI_CS0 (*)	SPI Chip Select 0 Output
201	SPI_MISO (*)	SPI Master serial input/Slave serial output signal	202	SPI_CS1 (*)	SPI Chip Select 1 Output
203	SPI_SCK (*)	SPI Clock Output	204	MFG_NC4	Do not connect on carrier board
205	VCC_5V_SB	+5VDC,Standby ±5%	206	VCC_5V_SB	+5VDC Standby ±5%
207	MFG_NC0	Do not connect on carrier board	208	MFG_NC2	Do not connect on carrier board
209	MFG_NC1	Do not connect on carrier board	210	MFG_NC3	Do not connect on carrier board
211	VCC	Power supply +5VDC ±5%	212	VCC	Power supply +5VDC ±5%
213	VCC	Power supply +5VDC ±5%	214	VCC	Power supply +5VDC ±5%
215	VCC	Power supply +5VDC ±5%	216	VCC	Power supply +5VDC ±5%
217	VCC	Power supply +5VDC ±5%	218	VCC	Power supply +5VDC ±5%
219	VCC	Power supply +5VDC ±5%	220	VCC	Power supply +5VDC ±5%
221	VCC	Power supply +5VDC ±5%	222	VCC	Power supply +5VDC ±5%
223	VCC	Power supply +5VDC ±5%	224	VCC	Power supply +5VDC ±5%
225	VCC	Power supply +5VDC ±5%	226	VCC	Power supply +5VDC ±5%
227	VCC	Power supply +5VDC ±5%	228	VCC	Power supply +5VDC ±5%
229	VCC	Power supply +5VDC ±5%	230	VCC	Power supply +5VDC ±5%

Note

The signals in the previous table marked with an asterisk symbol (*) are not supported on the conga-QA.

Table 4 PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1.
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1.
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1.
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1.
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	I PCIE		Not supported
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Not supported
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	I PCIE		Not supported
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Not supported
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock for Lanes 0 to 3.	O PCIE		
PCIE_WAKE#	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I 3.3VSB	PU 1k 3.3VSB	
PCIE_RST#	158	Reset Signal for external devices.	O 3.3V		

Table 5 ExpressCard Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE#	177	ExpressCard slot #0 capable card request.	I 3.3V	PU 10k 3.3V	
EXCD0_PERST#	171	ExpressCard slot #0 reset.	O 3.3V	PU 10k 3.3V	
EXCD1_CPPE#	178	ExpressCard slot #1 capable card request.	I 3.3V		Not supported
EXCD1_PERST#	172	ExpressCard slot #1 reset.	O 3.3V		Not supported

Table 6 Ethernet Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GBE_MDI0+ GBE_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI1+ GBE_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI2+ GBE_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_MDI3+ GBE_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Analog		Twisted pair signals for external transformer.
GBE_CTREF	15	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		Not Supported
GBE_LINK#	13	Ethernet controller 0 link indicator, active low.	O 3.3V PP		
GBE_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3V PP		
GBE_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3V PP		
GBE_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 3.3V PP		

Table 7 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	I SATA		Not supported
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Not supported
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	O 3.3V		

Table 8 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_P0+ USB_P0-	96 94	Universal Serial Bus Port 0 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P1+ USB_P1-	95 93	Universal Serial Bus Port 1 differential pair. This port may be optionally used as USB client port.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P2+ USB_P2-	90 88	Universal Serial Bus Port 2 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P3+ USB_P3-	89 87	Universal Serial Bus Port 3 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P4+ USB_P4-	84 82	Universal Serial Bus Port 4 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P5+ USB_P5-	83 81	Universal Serial Bus Port 5 differential pair.	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_P6+ USB_P6-	78 76	Universal Serial Bus Port 6 differential pair.	I/O		USB 2.0 compliant. USB 2.0 compliant only. NOT backwards compatible to USB 1.1
USB_P7+ USB_P7-	77 75	Universal Serial Bus Port 7 differential pair.	I/O		USB 2.0 compliant. USB 2.0 compliant only. NOT backwards compatible to USB 1.1
USB_0_1_OC#	86	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	I 3.3VSB	PU 10k 3.3VSB	
USB_2_3_OC#	85	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	I 3.3VSB	PU 10k 3.3VSB	
USB_4_5_OC#	80	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	I 3.3VSB	PU 10k 3.3VSB	
USB_6_7_OC#	79	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	I 3.3VSB	PU 10k 3.3VSB	
USB_ID	92	USB ID pin. Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the BIOS will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.	I 3.3VSB	PU 10k 3.3VSB	
USB_CC#	91	USB Client Connect pin. If USB Port 1 is configured for client mode then an externally connected USB host should set this signal to high-active in order to properly make the connection with the module's internal USB client controller. If the external USB host is disconnected, this signal should be set to low-active in order to inform the USB client controller that the external host has been disconnected. A level shifter/protection circuitry should be implemented on the carrier board for this signal.	I 3.3V	PU 10k 3.3V	

Table 9 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	43	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I/O 3.3V	PU 10k 3.3V	
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	O 3.3V		
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O 3.3V OD/PP	PU 10k 3.3V	
SDIO_LED	44	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	O 3.3V		
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I/O 3.3V		
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/ MMC card device.	O 3.3V		
SDIO_DAT0 SDIO_DAT1 SDIO_DAT2 SDIO_DAT3 SDIO_DAT4 SDIO_DAT5 SDIO_DAT6 SDIO_DAT7	49 48 51 50 53 52 55 54	SDIO Data lines. These signals operate in push-pull mode.	I/O 3.3V PP		

Table 10 HDA/AC'97 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST#	61	HD Audio/AC'97 Codec Reset.	O 3.3V		
HDA_SYNC	59	Serial Bus Synchronization.	O 3.3V		
HDA_BITCLK	63	HD Audio/AC'97 24 MHz Serial Bit Clock from Codec.	O 3.3V		
HDA_SDO	67	HD Audio/AC'97 Serial Data Output to Codec.	O 3.3V		
HDA_SDI	65	HD Audio/AC'97 Serial Data Input from Codec.	I 3.3V		

Note

The High Definition Audio interface found on the Qseven module complies with Intel® High Definition Audio Specification 1.0 and Audio Codec '97 Component Specification, Version 2.3 (AC '97).

Table 11 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_PPEN	111	Controls panel power enable.	O 3.3V		
LVDS_BLEN	112	Controls panel Backlight enable.	O 3.3V		
LVDS_BLT_CTRL /GP_PWM_OUT0	123	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
LVDS_A0+ LVDS_A0-	99 101	LVDS primary channel differential pair 0.	O LVDS		
LVDS_A1+ LVDS_A1-	103 105	LVDS primary channel differential pair 1.	O LVDS		
LVDS_A2+ LVDS_A2-	107 109	LVDS primary channel differential pair 2.	O LVDS		
LVDS_A3+ LVDS_A3-	113 115	LVDS primary channel differential pair 3.	O LVDS		
LVDS_A_CLK+ LVDS_A_CLK-	119 121	LVDS primary channel differential pair clock lines.	O LVDS		
LVDS_B0+ LVDS_B0-	100 102	LVDS secondary channel differential pair 0.	O LVDS		Not supported
LVDS_B1+ LVDS_B1-	104 106	LVDS secondary channel differential pair 1.	O LVDS		Not supported
LVDS_B2+ LVDS_B2-	108 110	LVDS secondary channel differential pair 2.	O LVDS		Not supported
LVDS_B3+ LVDS_B3-	114 116	LVDS secondary channel differential pair 3.	O LVDS		Not supported
LVDS_B_CLK+ LVDS_B_CLK-	120 122	LVDS secondary channel differential pair clock lines.	O LVDS		Not supported
LVDS_DID_CLK /GP_I2C_CLK	127	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus clock line.	I/O 3.3V OD	PU 10k 3.3V	
LVDS_DID_DAT /GP_I2C_DAT	125	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus data line.	I/O 3.3V OD	PU 10k 3.3V	
LVDS_BLC_CLK	128	Control clock signal for external SSC clock chip.	I/O 3.3V OD	PU 4k7 3.3V	
LVDS_BLC_DAT	126	Control data signal for external SSC clock chip.	I/O 3.3V OD	PU 10k 3.3V	

Table 12 SDVO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDVO_BCLK+ SDVO_BCLK-	131 133	SDVO differential pair clock lines.	O PCIE		
SDVO_INT+ SDVO_INT-	132 134	SDVO differential pair interrupt input lines.	I PCIE		
SDVO_GREEN+ SDVO_GREEN-	137 139	SDVO differential pair green data lines.	O PCIE		
SDVO_BLUE+ SDVO_BLUE-	143 145	SDVO differential pair blue data lines.	O PCIE		
SDVO_RED+ SDVO_RED-	149 151	SDVO differential pair red data lines.	O PCIE		
SDVO_FLDSTALL+ SDVO_FLDSTALL-	138 140	SDVO differential pair field stall lines.	I PCIE		
SDVO_TVCLKIN+ SDVO_TVCLKIN-	144 146	SDVO differential pair TV-Out synchronization clock lines.	I PCIE		
SDVO_CTRL_CLK	152	I²C based control signal (clock) for SDVO device.	I/O 3.3V OD	PU 100k 3.3V	
SDVO_CTRL_DAT	150	I²C based control signal (data) for SDVO device.	I/O 3.3V OD	PU 100k 3.3V	

Note

The SDVO interface signals are shared with the signals for the DisplayPort interface and/or the TMDS interface. The conga-QA does not support the DisplayPort interface and/or the TMDS interface

Table 13 DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP_LANE3+ DP_LANE3-	131 133	DisplayPort differential pair lines lane 3.	O PCIE		Shared with SDVO_BCLK+ and SDVO_BCLK- DisplayPort interface not supported
DP_LANE2+ DP_LANE2-	143 145	DisplayPort differential pair lines lane 2.	O PCIE		Shared with SDVO_BLUE+ and SDVO_BLUE- DisplayPort interface not supported
DP_LANE1+ DP_LANE1-	137 139	DisplayPort differential pair lines lane 1.	O PCIE		Shared with SDVO_GREEN+ and SDVO_GREEN- DisplayPort interface not supported
DP_LANE0+ DP_LANE0-	149 151	DisplayPort differential pair lines lane 0.	O PCIE		Shared with SDVO_RED+ and SDVO_RED- DisplayPort interface not supported
DP_AUX+ DP_AUX-	138 140	Auxiliary channel used for link management and device control. Differential pair lines.	I/O PCIE		Shared with SDVO_FLDSTALL+ and SDVO_FLDSTALL- DisplayPort interface not supported
DP_HPD#	154	Hot plug detection signal that serves as an interrupt request.	NC		DisplayPort interface not supported

Note

The DisplayPort interface signals are shared with the signals for the SDVO interface and/or the TMDS interface. DisplayPort interface is not supported on the conga-QA.

Table 14 HDMI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS_CLK+ TMDS_CLK-	131 133	TMDS differential pair clock lines.	O TMDS		Shared with SDVO_BCLK+ and SDVO_BCLK- HDMI interface not supported
TMDS_LANE0+ TMDS_LANE0-	143 145	TMDS differential pair lines lane 0.	O TMDS		Shared with SDVO_BLUE+ and SDVO_BLUE- HDMI interface not supported
TMDS_LANE1+ TMDS_LANE1-	137 139	TMDS differential pair lines lane 1.	O TMDS		Shared with SDVO_GREEN+ and SDVO_GREEN- HDMI interface not supported
TMDS_LANE2+ TMDS_LANE2-	149 151	TMDS differential pair lines lane 2.	O TMDS		Shared with SDVO_RED+ and SDVO_RED- HDMI interface not supported
HDMI_CTRL_CLK	152	DDC based control signal (clock) for HDMI device.	I/O 3.3V OD		Shared with SDVO_CTRL_CLK HDMI interface not supported
HDMI_CTRL_DAT	150	DDC based control signal (data) for HDMI device.	I/O 3.3V OD		Shared with SDVO_CTRL_DAT HDMI interface not supported
HDMI_HPD#	153	Hot plug detection signal that serves as an interrupt request.	NC		HDMI interface not supported

Note

The TMDS interface signals are shared with the signals for the SDVO interface and/or the DisplayPort interface. HDMI interface is not supported on the conga-QA.

Table 15 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	185 186 187 188	Multiplexed Command, Address and Data.	I/O 3.3V	PU 20k 3.3V	
LPC_FRAME#	190	LPC frame indicates the start of a new cycle or the termination of a broken cycle.	O 3.3V		
LPC_LDRQ#	192	LPC DMA request.	I 3.3V		Not Supported
LPC_CLK	189	LPC clock.	O 3.3V		
SERIRQ	191	Serialized Interrupt.	I/O 3.3V	PU 8k2 3.3V	

Table 16 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_MOSI	199	Master serial output/Slave serial input signal. SPI serial output data from Qseven module to the SPI device.	O 3.3V		Not Supported
SPI_MISO	201	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven module.	I 3.3V		Not Supported
SPI_SCK	203	SPI clock output.	O 3.3V		Not Supported
SPI_CS0	200	SPI chip select 0 output.	O 3.3V		Not Supported
SPI_CS1	202	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	O 3.3V		Not Supported

Table 17 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	129	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven module's CAN bus it is necessary to add transceiver hardware to the carrier board.	O 3.3V		Not Supported
CAN0_RX	130	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven module's CAN bus it is necessary to add transceiver hardware to the carrier board.	I 3.3V		Not Supported

Table 18 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	211-230	Power Supply +5VDC ±5%.	P		
VCC_5V_SB	205-206	Standby Power Supply +5VDC ±5%.	P		
VCC_RTC	193	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V).	P		
GND	1, 2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198	Power Ground.	P		

Table 19 Power Control Signal Descriptions

Signal	Pin #	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	26	High active input for the Qseven™ module indicates that power from the power supply is ready.	I 5V	PU 10k 5V	
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge.	I 3.3VSB OD	PU 10k 3.3VSB	

Table 20 Power Management Signal Descriptions

Signal	Pin #	Description of Power Management signals	I/O	PU/PD	Comment
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven module.	I 3.3V	PU 100k 3.3V	
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	I 3.3VSB	PU 10k 3.3VSB	
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	I 3.3VSB	PU 10k 3.3VSB	
SUS_STAT#	19	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3VSB	PU 10k 3.3VSB	
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	O 3.3VSB	PU 10k 3.3VSB	
SUS_S5#	16	S5 State: This signal indicates S4 or S5 (Soft Off) state.	O 3.3VSB	PU 10k 3.3VSB	
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	I 3.3VSB	PU 10k 3.3VSB	
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again.	I 3.3VSB	PU 10k 3.3VSB	

Table 21 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven module on the falling edge of a low active pulse.	I 3.3V	PU 10k 3.3V	
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	O 3.3V		
I2C_CLK	66	Clock line of I²C bus.	I/O 3.3V OD	PU 4k7 3.3V	
I2C_DAT	68	Data line of I²C bus.	I/O 3.3V OD	PU 4k7 3.3V	
SMB_CLK	60	Clock line of System Management Bus.	I/O 3.3VSB OD	PU 2k2 3.3VSB	
SMB_DAT	62	Data line of System Management Bus.	I/O 3.3VSB OD	PU 2k2 3.3VSB	
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	I/O 3.3VSB OD	PU 10k 3.3VSB	
SPKR /GP_PWM_OUT2	194	Primary functionality is output for audio enunciator, the “speaker” in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V		
BIOS_DISABLE# /BOOT_ALT#	41	Module BIOS disable input signal. Pull low to disable module’s on-board BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a bootloader.	I 3.3V	PU 10k 3.3V	
MFG_NC0 MFG_NC1 MFG_NC2 MFG_NC3 MFG_NC4	207 209 208 210 204	Do not connect on the carrier board. These pins are reserved for manufacturing purposes. May be used as JTAG signals, for example for boundary scan purposes during production.	n.a.		
RSVD	124, 129, 130, 199, 200, 201, 202, 203	Do not connect.	NC		

Table 22 Thermal Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I 3.3V	PU 10k 3.3V	
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off).	O 3.3VSB		Not supported. Do not connect.

Table 23 Fan Control Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT /GP_PWM_OUT1	196	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O 3.3V OC		
FAN_TACHOIN /GP_TIMER_IN	195	Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.	I 3.3V		

8 System Resources

8.1 System Memory Map

Table 24 Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(TOM- FB) – TOM	N.A.	1, 4 or 8MB	VGA frame buffer *
(TOM – FB – TSEG) – (TOM - FB)	N.A.	1MB	TSEG**
(TOM - FB – TSEG – BIOS) - (TOM – FB – TSEG)	N.A.	448kB or 192kB	Used by BIOS firmware with ACPI enabled respectively disabled**
1024kB – (TOM - FB – TSEG – BIOS)	100000 – N.A	N.A.	Extended memory
869kB – 1024kB	E0000 - FFFFF	128kB	Runtime BIOS
832kB – 869kB	D0000 - DFFFF	64kB	Upper memory
640kB – 832kB	A0000 - CFFFF	192kB	Video memory and BIOS
639kB – 640kB	9FC00 - 9FFFF	1kB	EBDA=Extended BIOS Data Area
0 – 639kB	00000 - 9FC00	512kB	Conventional memory

Note

T.O.M. = Top of memory = max. DRAM installed

FB = VGA frame buffer

TSEG = Designated as internally used by system BIOS for SMI handling.

** VGA frame buffer can be reduced to 1MB in setup.*

*** Only if ACPI Aware OS is set to YES in setup.*

8.2 I/O Address Assignment

The I/O address assignment of the conga-QA module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

Table 25 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
0100 - 010F	16 bytes	No	congatec System Control
01F0 - 01F7	8 bytes	No	Primary IDE channels
03B0 – 03DF	16 bytes	No	Video system
03F6	1 byte	No	Primary IDE channel command port
03F7	1 byte	No	Primary IDE channel status port
0400 – 04BF	192 bytes	No	Motherboard resources
04D0 – 04D1	2 bytes	No	Motherboard resources
0900 – 09FF	256 bytes	No	Motherboard resources
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
0D00 – FFFF		See note	PCI / PCI Express bus

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

8.3 Interrupt Request (IRQ) Lines

Table 26 IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Can be used for
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		LPC bus via SERIRQ or PCIe bus via MSI
4	Yes		LPC bus via SERIRQ or PCIe bus via MSI
5	Yes		LPC bus via SERIRQ or PCIe bus via MSI
6	Yes		LPC bus via SERIRQ or PCIe bus via MSI
7	Yes		LPC bus via SERIRQ or PCIe bus via MSI
8	No	Real-time Clock	Not applicable
9	Note 2	SCI / Generic	LPC bus via SERIRQ or PCIe bus via MSI
10	Yes		LPC bus via SERIRQ or PCIe bus via MSI
11	Yes		LPC bus via SERIRQ or PCIe bus via MSI
12	Yes		LPC bus via SERIRQ or PCIe bus via MSI
13	No	Math coprocessor	Not applicable
14	Note 1	IDE Controller 0 (IDE0) / Generic	LPC bus via SERIRQ or PCIe bus via MSI
15	Yes		LPC bus via SERIRQ or PCIe bus via MSI

MSI = Message Signal Interrupt (used by PCIe)

In PIC mode, the PCI bus interrupt lines can be routed to any free IRQ.

Note

1. *If the ATA/IDE controller is set to disabled, IRQ14 is free for PCI/LPC bus.*
2. *In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCIe interrupt line.*

Table 27 IRQ Lines in APIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		LPC bus via SERIRQ
4	Yes		LPC bus via SERIRQ
5	Yes		LPC bus via SERIRQ
6	Yes		LPC bus via SERIRQ
7	Yes		LPC bus via SERIRQ
8	No	Real-time Clock	Not applicable
9	Note 2	Generic	LPC bus via SERIRQ, option for SCI
10	Yes		LPC bus via SERIRQ
11	Yes		LPC bus via SERIRQ
12	No		LPC bus via SERIRQ (Exclusively)
13	No	Math processor	Not applicable
14	Note 1	IDE Controller 0 (IDE0) / Generic	LPC bus via SERIRQ
15	Yes		LPC bus via SERIRQ
16	Yes		Integrated graphics device, PCI Express Root Port 1, PCIe slot 1
17	Yes		PCI Express Root Port 2, PCIe slot 2 or onboard Gigabit LAN Controller
18	Yes		USB Client controller, SDIO Ports
19	Yes		HDA Controller
20	Note 2		UHCI Host Controller 0, option for SCI
21	No		UHCI Host Controller 1
22	No		UHCI Host Controller 2
23	No		EHCI Host Controller

Note

1. If the ATA/IDE controller is set to disabled in BIOS setup, IRQ14 is avialable via SERIRQ.

2. In ACPI and APIC mode, IRQ9 or IRQ 20 is used for the SCI (System Control Interrupt).

8.4 PCI Configuration Space

Table 28 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	02h	00h	Internal	IGD (Integrated graphics device)
00h	1Ah	00h	Internal	USB 2.0
00h	1Bh	00h	Internal	Intel High Definition Audio Controller
00h (see Note)	1Ch	00h	Internal	PCI Express Root Port 1
00h (see Note)	1Ch	01h	Internal	PCI Express Root Port 2
00h	1Dh	00h	Internal	UHCI Host Controller 0
00h	1Dh	01h	Internal	UHCI Host Controller 1
00h	1Dh	02h	Internal	UHCI Host Controller 2
00h	1Dh	07h	Internal	EHCI Host Controller
00h	1Eh	00h	Internal	SDIO/MMC Port 0 (Not routed)
00h	1Eh	01h	Internal	SDIO/MMC Port 1 (Not routed)
00h	1Eh	02h	Internal	SDIO/MMC Port 2
00h	1Fh	00h	N.A.	LPC Interface
00h	1Fh	01h	Internal	Parallel ATA Controller
01h (see Note)	00h	00h	Internal	PCIe slot 1
02h (see Note)	00h	00h	Internal	Onboard Gigabit LAN Controller

Note

The given bus numbers only apply to a conga-QA supporting Gigabit Ethernet with both PCI Express Ports being enabled in the BIOS setup. When using carrier boards with a PCIe packet switch at PCIe slot 1, the bus number of the onboard Gigabit Ethernet controller is increased by the number of PCI bridges within the switch.

8.5 PCI Interrupt Routing

Table 29 PCI Interrupt Routing Map

PIRQ	PCIe BUS INT Line	APIC Mode IRQ	IGD	HDA	UHCI 0	UHCI 1	UHCI 2	EHCI	USB 2.0 Client	LAN	SATA	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Slot1	PCI-EX Slot2	SDIO0	SDIO1	SDIO2
A	INTA	16	x	x								x		x [2]	x [5]			
B	INTB	17								x			x	x [3]	x [2]			
C	INTC	18							x					x [4]	x [3]	x	x	x
D	INTD	19									x			x [5]	x [4]			
E		20			x													
F		21				x												
G		22					x											
H		23						x										

Note

[2] *Interrupt used by single function PCI Express devices (INTA).*

[3] *Interrupt used by multifunction PCI Express devices (INTB).*

[4] *Interrupt used by multifunction PCI Express devices (INTC).*

[5] *Interrupt used by multifunction PCI Express devices (INTD).*

8.6 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

8.7 SM Bus

System Management (SM) bus signals are connected to the Intel® I/O System Controller Hub US15W and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

9 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

Note

The BIOS Setup Program described in the following section depicts the BIOS that will be used for mass production conga-QA modules and does not necessarily describe the BIOS Setup Program found on early engineering samples currently being shipped.

9.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> key during POST.

9.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used a message will be displayed during POST stating that the “Boot Selection Popup menu has been selected” and the menu itself will be displayed immediately after POST thereby allowing the operator to choose the boot device to be used.

9.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

Main	Advanced	Boot	Security	Power	Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2/F3	Change Colors of setup screen.
F7	Discard Changes.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

9.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24-hour format.*
System Date	Day of week, month/day/year	Specifies the current system date. *Note: The date is in month-day-year format.*
BIOS ID	no option	Displays the BIOS ID.
Processor	no option	Displays the processor type.
CPU Frequency	no option	Displays CPU frequency.
System Memory	no option	Displays the total amount of system memory.
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
Running Time	no option	Displays the time the board is running [in hours max. 65535].

9.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Power	Exit
	ACPI Configuration				
	PCI Configuration				
	Graphics Configuration				
	CPU Configuration				
	Chipset Configuration				
	I/O Interface Configuration				
	IDE Configuration				
	USB Configuration				
	Keyboard/Mouse Configuration				
	Remote Access Configuration				
	Hardware Health Configuration				
	Watchdog Configuration				
	SDIO Configuration				

9.4.1 ACPI Configuration Submenu

Feature	Options	Description
ACPI Aware O/S	No **Yes**	Set this value to allow the system to utilize the Intel ACPI (Advanced Configuration and Power Interface). Set to *NO* for non ACPI aware operating system like DOS and Windows NT. Set to *YES* if your OS complies with the ACPI specification (e.g. Windows 2000, XP)
ACPI Version Features	ACPI v1.0 **ACPI v2.0** ACPI v3.0	ACPI version supported by the BIOS ACPI code and tables.
System Off Mode	**G3/Mech Off** S5/Soft Off	Select the actual power down mode when the system performs a shutdown with a congatec battery system connected. *Note: This node is only visible when the system is connected to a congatec battery system.*
ACPI APIC support	**Enabled** Disabled	Set to enable to include the APIC support table to ACPI.
Suspend mode	**S3 (STR)**	Select the state used for ACPI system suspend. *Note: Only S3 is supported.*
Repost Video on S3 Resume	No Yes	Determines whether to invoke VGA BIOS post on S3 resume (required by some OS to re-initialize graphics).
USB Device Wakeup From S3/S4	**Disabled** Enabled	Enable or disable USB device wakeup from S3 and S4 state.
Active Cooling Trip Point	**Disabled** 50, 60, 70, 80, 90°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Cooling Trip Point	Disabled 50, 60, 70, 80, **90**°C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.
Critical Trip Point	80, 85, 90, 95, 100, **105**, 110°C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Watchdog ACPI Event	**Shutdown** Restart	Select the event that is initiated by the watchdog ACPI event. When the watchdog times out a critical but orderly OS shutdown or restart can be performed (see note below).
LID Device	Disable **Enable**	Enable using the LID Button functionality when it is present in the system.
Sleep Button Device	Disable **Enable**	Enable using the sleep button to go or resume S3 when it is present on the system.

Note

In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

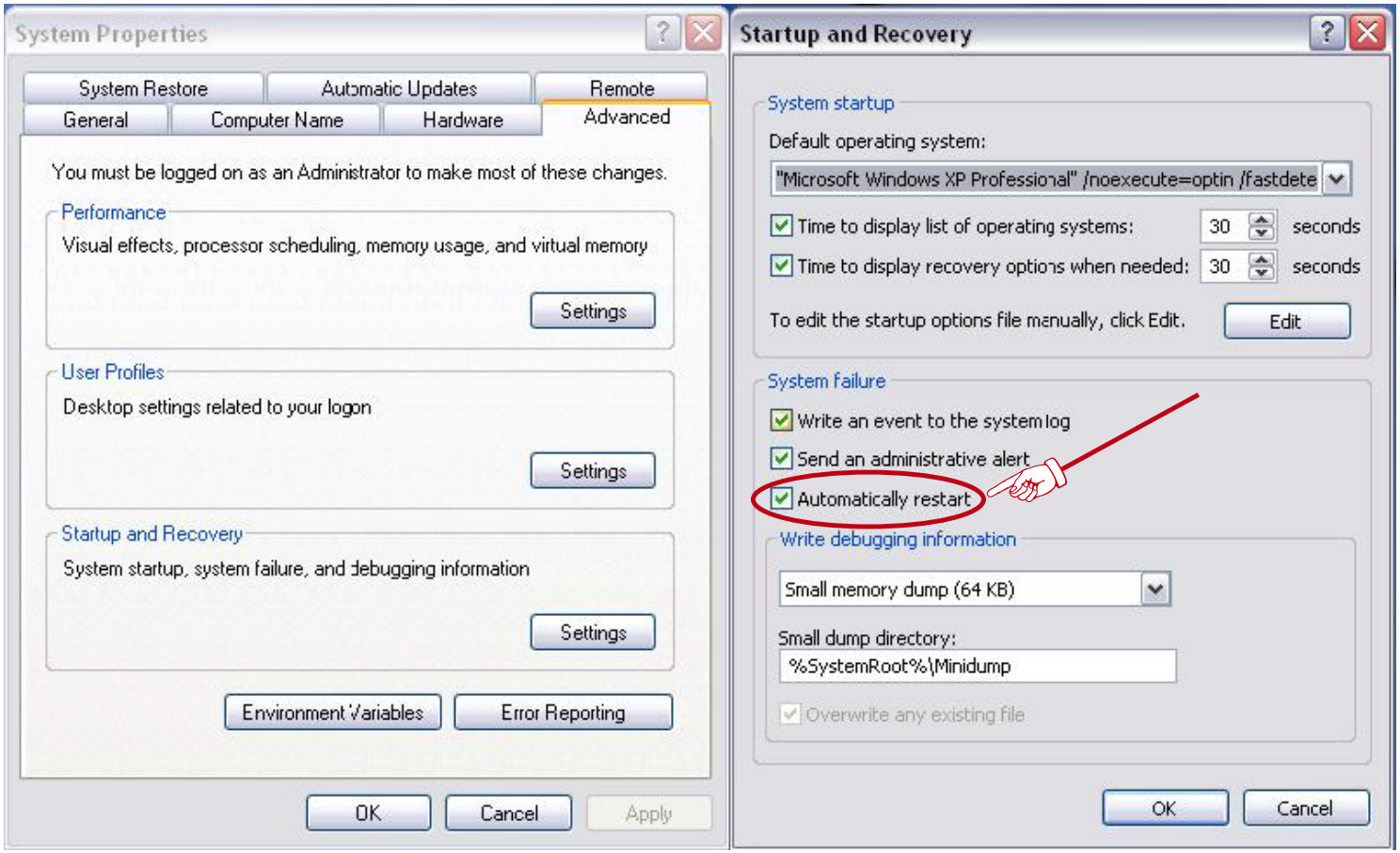
For Restart: An ACPI fatal error is reported to the OS.

It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP/2000 there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very

brief blue-screen the system will restart.

You can enable this setting buy going to the "System Properties" dialog box and choosing the "Advanced" tab. Once there choose the "Settings" button for the "Startup and Recovery" section. This will open the "Startup and Recovery" dialog box. In this dialog box under "System failure" there are three check boxes that define what Windows will do when a fatal error has been detected. In order to ensure that the system restarts after a 'Watchdog ACPI Event" that is set to 'Restart', you must make sure that the check box for the selection "Automatically restart" has been checked. If this option is not selected then Windows will remain at a blue-screen after a 'Watchdog ACPI Event" that has been configured for 'Restart' has been generated. Below is a Windows screen-shot showing the proper configuration.

Win XP/2000 Watchdog ACPI Event restart configuration



9.4.2 PCI Configuration Submenu

Feature	Options	Description
Plug & Play O/S	**No** Yes	Specifies if manual configuration is desired. Set to *NO* for operating systems that do not meet the Plug and Play specification. In this case the BIOS configures all devices in the system. Select *YES* to let the operating system configure PnP devices that are not required for booting.
PCI Latency Timer	32, **64**, 96, ... 248	This option allows you to adjust the latency timer of all devices on the PCI bus.
Allocate IRQ to PCI VGA	**Yes** No	Allow or restrict the BIOS from giving the VGA controller an IRQ resource.
►PCI IRQ Resource Exclusion	sub menu	Opens PCI IRQ Resource Exclusion sub menu.
►PCI Interrupt Routing	sub menu	Opens PCI Interrupt Routing sub menu.

9.4.2.1 PCI IRQ Resource Exclusion Submenu

Feature	Options	Description
IRQ xx	**Available** Reserved	Allow or restrict the BIOS from giving IRQ resource to PCI/PNP devices. *Note: Assigned IRQ resources are shaded and listed as 'Allocated'.*

9.4.2.2 PCI Interrupt Routing Submenu

Feature	Options	Description
PIRQ xx (devices)	**Auto,** 3, 4, .., 14, 15	Select fixed IRQ for PCI interrupt line or set to AUTO to let the BIOS and operating system route an IRQ. *Note: Only those IRQs that are free are listed.*
1st Exclusive PCI IRQ	**None**, [IRQs assigned manually above]	The selected IRQ will only be assigned to the PIRQ line it has been set to manually. PIRQs set to AUTO will not be assigned this IRQ.
2nd Exclusive PCI IRQ	**None**, [IRQs assigned manually above]	The selected IRQ will only be assigned to the PIRQ line it has been set to manually. PIRQs set to AUTO will not be assigned this IRQ.

9.4.3 Graphics Configuration Submenu

Feature	Options	Description
Primary Video Device	**PCIe/IGD** IGD	Select primary video adapter to be used during boot up. IGD: Internal Graphics Device PCIe: PCI Express Graphics Device
Internal VGA Mode Select	Disabled Enabled, 1MB **Enabled, 4MB** Enabled, 8MB	This option allows you to disable the internal VGA controller or enable it with 1MB, 4MB or 8MB initial frame buffer size.
Graphics Aperture Size	128MB **256MB**	Determines the size of the graphics memory aperture.
Boot Display Device	**Auto** Intergrated LVDS External DVI/HDMI External TV External CRT External LVDS	Select the display device(s) used for boot up. External display devices are connected to the SDVO interface. External TV is only visible when this mode is selected for the 3rd supported SDVO type.
Local Flat Panel Scaling	**Auto** Forced Scaling Disabled	Select whether and how to scale the actual video mode resolution to the local flat panel resolution.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM. If set to 'No' (Default) the BIOS uses the panel type defined in the Local Flat Panel Type node.
Local Flat Panel Type	**Auto** VGA 1x18 (002h) VGA 1x18 (013h) WVGA 1x18 (01Bh) SVGA 1x18 (01Ah) XGA 1x18 (006h) XGA 1x24 (008h) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.* VGA = 640x480 WVGA = 800x480 SVGA = 800x600 XGA = 1024x768
3rd Supported SDVO Type	Disabled TV LVDS **DVI-I**	Select the device type supported by the SDVO Interface. *Note: Analog CRT and DVI codecs are supported by default..*

Feature	Options	Description
SDVO Flat Panel Type	VGA 1x18 (002h) VGA 1x18 (013h) **WVGA 1x18 (01Bh)** SVGA 1x18 (01Ah) XGA 1x18 (006h) XGA 2x18 (007h) XGA 1x24 (008h) XGA 2x24 (012h) SXGA 2x24 (018h) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select the predefined LFP type for the external LVDS. Only visible if the 3rd supported SDVO Type is set to LVDS.
TV Standard	**VBIOS-Default** NTSC PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3	Select TV standard that should be supported. TV connection type is automatically detected by the Video BIOS.
TV Sub-Type	(Options depend on selected TV standard)	Select sub-type for selected TV standard.
Backlight Control	**Auto**, 0%, 25%, 50%, 75%, 100%	Select local flat panel backlight control value. If set to Auto, the BIOS tries to read the backlight brightness value from the EPI data set.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Control	**No** Yes	Allow the inversion of backlight control values if required by the actual backlight hardware controller.
PWM Backlight Control	**Disabled** Enabled	Enable/Disable backlight PWM output of COM Express.
PWM Inverter Frequency (Hz)	**200**-40000	Allow the user to introduce an integer value in the range of 200 to 40000 corresponding to the PWM Inverter frequency. The default value is 200. This setup node is only visible when PWM Backlight Control is set to Enable.

9.4.4 CPU Configuration Submenu

Feature	Options	Description
Processor Info Block	No option	Displays the processor manufacturer, brand, frequency, and cache sizes.
Max CPUID Value Limit	**Disabled** Enabled	When **enabled**, the processor will limit the maximum CPUID input value to **03h** when queried, even if the processor supports a higher CPUID input value. When **disabled**, the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Intel® Virtualization Technology	**Enabled**	Support for Intel® Virtualization Technology. This setup node is only available and visible for the 1.6Ghz frequency modules. It is always enabled.
Execute Disable Bit	Disabled **Enabled**	Enable or disable the hardware support for data execution prevention.
Hyper Threading Technology	Disabled **Enabled**	Enable Hyper Threading Technology for operating systems that are optimized for it. Only available and visible for the 1.6Ghz frequency modules.
Intel SpeedStep tech.	**Enabled** Disabled	Enabled: CPU speed is controlled by the operating system. Disabled: No SpeedStep, default CPU speed.
Boot CPU Speed On AC	**Maximum** Minimum	Determines the default CPU Frequency.
Intel C-State tech	Disabled **Enabled**	Enables the processor C-State support when in IDLE mode.
Enhanced C-States	Disabled **Enabled**	Processor IDLE is set to enhanced C-states.

9.4.5 Chipset Configuration Submenu

Feature	Options	Description
Serial IRQ Mode	**Continuos** Quiet	Selects the Serial IRQ mode.
APIC ACPI SCI IRQ	**Disabled** Enabled	If set to Disabled IRQ9 is used for the SCI. If set to Enabled IRQ20 is used for the SCI.
PCIE Port 0	**Auto** Enabled Disabled	Enable or disable PCI Express port.
PCIE Port 1	**Auto** Enabled Disabled	Enable or disable PCI Express port.
PCIe Base Spec Compliance	**Disabled** Enabled	Enable or disable PCI Express Compliance feature.
Active State Power Management	**Disabled** Enabled	Enable or disable PCI Express L0s and L1 link power states.
US15W Silicon Revision	D.2	Chipset revision
Atom Silicon Revision	C.0	Processor revision
CMC Lo-Module and Hi-Module Revision:	0D2.026x 0D2.018x	CMC Binary version number. Might change with future BIOS revisions.

9.4.6 I/O Interface Configuration Submenu

Feature	Options	Description
SDIO/MMC Controller	Enabled **Disabled**	N/A
HDA Controller	Enabled **Disabled**	When set to Enabled, the HDA will be enabled no matter if a codec is present or not.
►SIO Winbond W83627 Configuration	sub menu	Opens submenu. *Note: This setup node is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.*
►SIO SMSC SCH3114 Configuration	sub menu	Opens submenu. *Note: This setup node is only available if an external SMSC SCH3114 Super I/O has been implemented on the carrier board.*

Note

The BIOS does not initialize the HDA codec. The codec remains in default mode and must be initialized by the codec's driver.

9.4.6.1 SIO Winbond W83627 Configuration

Feature	Options	Description
Serial Port 1/2 Configuration	**Disabled** 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Specifies the I/O base address and IRQ of serial port 1/2.
Parallel Port Address	**Disabled** 378 278 3BC	Specifies the I/O base address used by the parallel port.
Parallel Port Mode	**Normal** Bi-directional ECP EPP ECP&EPP	Specifies the parallel port mode.
EPP Version	**1.9** 1.7	Specifies the EPP version.
Parallel Port DMA	DMA0 DMA1 **DMA3**	Specifies the DMA channel for parallel port in ECP mode.
Parallel Port IRQ	None IRQ5 **IRQ7**	Specifies the interrupt for the parallel port.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

9.4.6.2 SIO SMSC SCH3114 Configuration

Feature	Options	Description
Serial Port 1/2/3/4 Address	**Disabled** 3F8 2F8 3E8 2E8	Specifies the I/O base address of serial port 1/2/3/4.
Serial Port 1/2/3/4 IRQ	3 4 10 11	Specifies the interrupt of serial port 1/2/3/4.
Serial Port 2 Mode	**Normal** IrDA ASK IR	Select serial port 2 mode.
IR Duplex Mode	**Full Duplex** Half Duplex	Serial port 2 infrared duplex mode.
Receiver Polarity	**High** Low	Serial port 2 infrared receiver polarity.
Xmitter Polarity	High **Low**	Serial port 2 infrared transmitter polarity.

Note

This setup menu is only available if an external SMSC SCH3114 Super I/O has been implemented on the carrier board.

9.4.7 IDE Configuration Submenu

Feature	Options	Description
IDE Controller	Disabled **Enabled**	Enables/Disables the integrated parallel ATA controller.
►Primary IDE Master	sub menu	Reports type of connected IDE device.
►Primary IDE Slave	sub menu	Reports type of connected IDE device.
Hard Disk Write Protect	**Disabled** Enabled	If enabled, protects the hard drive from being erased. Disabled allows the hard drive to be used normally. Read, write and erase functions can be performed to the disk.
IDE Detect Time Out (s)	0, 5, 10, ... 30, **35**	Set this option to stop the BIOS from searching for IDE devices within the specified number of seconds. Basically, this allows you to fine-tune the settings to allow for faster boot times. Adjust this setting until a suitable timing can be found that will allow for all IDE disk drives that are attached to be detected.

9.4.7.1 Primary/Secondary IDE Master/Slave Submenu

Feature	Options	Description
Device	Hard Disk ATAPI CDROM	Displays the type of drive detected. The 'grayed-out' items below are the IDE disk drive parameters taken from the firmware of the IDE disk
Vendor	no option	Manufacturer of the device.
Size	no option	Total size of the device.
LBA Mode	supported not supported	Shows whether the device supports Logical Block Addressing.
Block Mode	number of sectors	Block mode boosts IDE performance by increasing the amount of data transferred. Only 512 byte of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 kB per interrupt.
PIO Mode	0, 1, 2, 3, 4	IDE PIO mode programs timing cycles between the IDE drive and the programmable IDE controller. If PIO mode increases, the cycle time decreases.
Async DMA	no option	This indicates the highest Asynchronous DMA Mode that is supported.
Ultra DMA	no option	This indicates the highest Synchronous DMA Mode that is supported.
S.M.A.R.T	no option	Self-Monitoring Analysis and Reporting Technology protocol used by IDE drives of some manufacturers to predict drive failures.
Type	Not Installed **Auto** CD/DVD ARMD	Sets the type of device that the BIOS attempts to boot from after the POST has completed. *Not Installed* prevents the BIOS from searching for an IDE disk. *Auto* allows the BIOS to auto detect the IDE disk drive type. *CD/DVD* specifies that an IDE CD/DVD drive is attached. The BIOS will not attempt to search for other types of IDE disk drives. *ARMD* specifies an ATAPI Removable Media Device. This includes, but is not limited to ZIP and LS-120.
LBA/Large Mode	Disabled **Auto**	Set to *AUTO* to let the BIOS auto detect LBA mode control. Set to Disabled to prevent the BIOS from using LBA mode.
Block (Multi-Sector Transfer)	Disabled **Auto**	Set to *AUTO* to let the BIOS auto detect device support for multi sector transfer. The data transfer to and from the device will occur multiple (the number of sectors, see above) sectors at a time. Set to Disabled to prevent the BIOS from using block mode. The data transfer to and from the device will occur one sector at a time.
PIO Mode	**Auto** 0, 1, 2, 3, 4	Set to *AUTO* to let the BIOS auto detect the supported PIO mode.
DMA Mode	**Auto** Disabled UDMA0, 1, 2, 3, 4, 5, 6	Set to *AUTO* to let the BIOS auto detect the supported DMA mode. UDMA = Ultra DMA
S.M.A.R.T	**Auto** Disabled Enabled	Set to *AUTO* to let the BIOS auto detect hard disk drive support. Set to *Disabled* to prevent the BIOS from using SMART feature. Set to *Enabled* to allow the BIOS to use SMART feature on supported hard disk drives.
32Bit Data Transfer	Disabled **Enabled**	Enable/Disable 32-bit data transfers on supported hard disk drives.
ARMD Emulation Type	**Auto** Floppy Hard disk drive	ARMD is a device that uses removable media, such as the LS120, MO (Magneto-optical), or Iomega Zip drives. If you want to boot from media on ARMD, it is required that you emulate boot up from a floppy or hard disk drive. This is essentially necessary when trying to boot to DOS. You can select the type of emulation used if you are booting such a device.

9.4.8 USB Configuration Submenu

Feature	Options	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports **6 USB Ports**	Disable US15W USB host controllers. Enable UHCI host controller 0. Enable UHCI host controller 0 + 1. Enable UHCI host controller 0 + 1 + 2.
USB 2.0 Controller	**Enabled** Disabled	Enable the US15W USB 2.0 (EHCI) host controller.
USB Client Controller	**Enabled** Disabled Auto	conga-QA offers USB client support on USB port 2. See section 6.5.1 “USB Client Controller” of this document for more details. The ‘Auto’ option configures the Port according to the jumper position on the conga-QEVAL evaluation board.
Legacy USB Support	Disabled **Enabled** Auto	Legacy USB Support refers to the USB keyboard, USB mouse and USB mass storage device support. If this option is *Disabled*, any attached USB device will not become available until a USB compatible operating system is booted. However, legacy support for USB keyboard will be present during POST. When this option is *Enabled*, those USB devices can control the system even when there is no USB driver loaded. *AUTO* disables legacy support if no USB devices are connected.
USB Keyboard Legacy Support	Disabled **Enabled**	Enable/Disable USB keyboard legacy support. *Note: This option has to be used with caution. If the system is equipped with USB keyboard only, then the user cannot enter setup to enable the option back.*
USB Mouse Legacy Support	**Disabled** Enabled	Enable/Disable USB mouse legacy support.
USB Storage Device Support	Disabled **Enabled**	Enable/Disable USB mass storage device support.
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configures the USB 2.0 host controller in HiSpeed (480Mbps) or Full Speed (12Mbps).
BIOS EHCI Hand-Off	**Disabled** Enabled	Enable workaround for OSes without EHCI hand-off support.
USB Beep Message	Disabled **Enabled**	Enable/Disable the beep during USB device enumeration.
USB Stick Default Emulation	Auto **Hard Disk**	Select default USB stick emulation type. Auto selects floppy or hard disk emulation based on the storage size of the USB stick, but the emulation type can be manually re-configured for each device using the Mass Storage Device Configuration sub menu.
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds the legacy USB support BIOS routine waits for the USB mass storage device after the start unit command.
►USB Mass Storage Device Configuration	sub menu	Opens sub menu.

9.4.8.1 USB Mass Storage Device Configuration Submenu

Feature	Options	Description
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	Every USB MSD that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. *Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.* Select *AUTO* to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. *Forced FDD* allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. *Hard Disk* allows the device to be emulated as hard disk. *CDROM* assumes the CD.ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

9.4.9 Keyboard/Mouse Configuration Submenu

Feature	Options	Description
Bootup Num-Lock	Off **On**	Specifies the power-on state of the Num-lock feature on the numeric keypad of the keyboard.
Typematic Rate	Slow **Fast**	Specifies the rate at which the computer repeats a key that is held down. *Slow* sets a rate of under 8 times per second. *Fast* sets a rate of over 20 times per second.
Port 64 Reset Function	**Disabled** Enabled	Allows the use of the legacy Port 64 reset command by software emulation.
PS/2 Mouse Support	Enable **Disable**	Allows the use of the PS/2 mouse legacy software emulation.

9.4.10 Remote Access Configuration Submenu

Feature	Options	Description
Remote Access	**Disabled** Enabled	Enable/Disable the BIOS remote access feature. *Note: If the systems serial ports are disabled in the 'I/O Interface Configuration' submenu, then Serial Redirection is disabled and 'Remote Access Configuration' menu is unavailable to the users.*
Serial Port Number	**COM1** COM2	Select the serial port you want to use for console redirection. *Note: Only enabled serial ports are presented as an option.*
Serial Port Mode	**115200 8,n,1** 57600 8,n,1 19200 8,n,1	Select the baud rate (transmitted bits per second) you want the serial port to use for console redirection. *Note: The terminal program used with Serial Redirection must be set to use exact the same set of communication parameters.*
Flow Control	**None** Hardware Software	Select the flow control for Serial Redirection.
Redirection After BIOS POST	Disabled Boot Loader **Always**	With *Disabled* Serial Redirection functionality is disabled at the end of BIOS POST. If set to *Always*, all resources and interrupts associated with Serial Redirection are protected and not released to DOS. This option lets Serial Redirection permanently reside at base memory which allows the DOS console to be redirected. *Note, that graphics output (VGA, SVGA, etc) from DOS programs is not redirected!* If set to *Boot loader*, Serial Redirection is active during the OS boot loader process. This allows boot status messages to be redirected, but Serial Redirection will terminate when the OS loads.
Terminal Type	**ANSI** VT100 VT-UTF8	Select the target terminal type. Escape sequences representing keystrokes are sent to the remote terminal based on these settings.
VT-UTF8 Combination Key Support	Disabled **Enabled**	This option enables VT-UFT8 combination key support for ANSI/ VT100 terminals.
Sredir Memory Display Delay	**No Delay** Delay 1 Sec Delay 2 Sec Delay 4 Sec	Set the delay in seconds to display memory information if serial redirection is enabled.
Serial Port BIOS Update	**Disabled** Enabled	Enable or disable the serial port BIOS update feature. Disabling saves boot time.

Note

Setup node is only available for BIOS Rev. QMENR113 or later and also requires an external Super I/O be implemented on the carrier board.

9.4.11 Hardware Monitoring Submenu

Feature	Options	Description
H/W Health Function	Disabled **Enabled**	Enable hardware health monitoring device and display the readings.
Board Temperature	No option	Current board temperature
CPU Temperature	No option	Current processor die temperature
CPU Fan Speed	No option	Current CPU FAN speed

9.4.12 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset..
Stop Watchdog For User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the Popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One time trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to '*One time trigger'* the watchdog will be disabled after the first trigger. If set to *'Single event'*, every stage will be executed only once, then the watchdog will be disabled. If set to *'Repeated event'* the last stage will be executed repeatedly until a reset occurs.
Delay	see Post Watchdog	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	**ACPI Event** Reset Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about *ACPI Event* see section 9.4.1 of this user's guide.
Event 2	**Disabled** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	0.5sec 1sec 2sec 5sec **10sec** 30sec 1min 2min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.

9.4.13 SDIO Configuration Submenu

Feature	Options	Description
SDIO Devices Enabled	None	List of SDIO devices detected by the system
Data Access Mode	**Auto** DMA PIO	Selects the access mode to the SD device. Auto defines the access mode as DMA if the controller supports it. Select DMA to access the device in Direct Memory Access mode (DMA). Select PIO to access the device in Programmed Input Output mode (PIO).
SD Card Default Emulation	Auto **Floppy**	Select the emulation type implemented by the BIOS. The SDIO card is emulated by default as a floppy drive. When using other emulation types selecting Auto appear new configuration possibilities.

Note

This submenu is only visible if the SDIO controller is enabled. The SDIO controller setup node is located in the 'I/O Interface Configuration Submenu'.

9.4.13.1 SDIO Mass Storage Device Configuration Submenu

Feature	Options	Description
Devices	None	Identification name of the SDIO card.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk	Every SDIO MSD that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. *Note: The device's formatted type and the emulation type provided by the BIOS must match in order for the device to boot properly.* Select AUTO to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. Forced FDD allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. Hard Disk allows the device to be emulated as hard disk.

9.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen. In the upper part of the screen the Boot setup allows you to prioritize the available boot devices. The lower part of this setup screen shows options related to the BIOS boot.

9.5.1 Boot Device Priority

Feature	Options	Description
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The “Device Based” boot priority list allows you to select from a list of currently detected devices only. The “Type Based” boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the “Device Based” boot priority list might change dynamically in cases when devices are physically removed or added to the system. The “Type Based” boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if device based priority list control is selected. If “Type Based” priority list control is enabled only 8 boot devices can be prioritized.)	Disabled Primary Master Primary Slave Secondary Master Secondary Slave Legacy Floppy USB Floppy USB Hard disk USB CDROM USB Removable Dev. Onboard LAN External LAN PCI Mass Storage PCI SCSI Card Any PCI BEV Device Onboard PCI SATA Third Master Third Slave PCI RAID Local BEV ROM Fourth Master Fourth Slave SDIO Floppy SDIO Hard disk	This view is only available when in the default “Type Based” mode. When in “Device Based” mode you will only see the devices that are currently connected to the system. The default boot priority is *Removables 1st, ATAPI CDROM 2nd, Hard Disk 3rd, BEV 4th* (BEV = Boot Entry Vector, e.g. Network or SCSI Option-ROMs).

9.5.2 Boot Settings Configuration

Feature	Options	Description
Quick Boot	Disabled **Enabled**	If *Enabled*, some POST tasks will be skipped to speed-up the BIOS boot process.
Quiet Boot	**Disabled** Enabled	*Disabled* displays normal POST diagnostic messages. *Enabled* displays OEM logo instead of POST messages. *Note: The default OEM logo is a dark screen.*
Boot Display	**Clear** Maintain	Controls the end of POST boot display handling, if Quiet Boot is enabled. If set to *Maintain* the BIOS will maintain the current display contents and graphics video mode used for POST display. If set to *Clear* the BIOS will clear the screen and switch to VGA text mode at end of POST.
Automatic Boot List Retry	**Disabled** Enabled	
Add-On ROM Display Mode	Force BIOS **Keep current**	Set display mode for Option ROM.
Halt On Error	**Disabled** Enabled	Determines whether the BIOS halts and displays an error message if an error occurs. If set to *Enabled* the BIOS waits for user input.
Hit 'DEL' Message Display	Disabled **Enabled**	Allows/Prevents the BIOS to display the '*Hit Del to enter Setup'* message.
Interrupt 19 Capture	**Disabled** Enabled	Allows/Prevents the option ROMs (such as network controllers) from trapping the boot strap interrupt 19.
PXE Boot to LAN	**Disabled** Enabled	Disable/Enable PXE boot to LAN *Note: When set to 'Enabled', the system has to be rebooted in order for the Intel Boot Agent device to be available in the Boot Device Menu. Only visible for variants with onboard Gigabit Ethernet controller.*
Power Loss Control (see note below)	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. *Remain Off* keeps the power off until the power button is pressed. *Turn On* restores power to the computer. *Last State* restores the previous power state before power loss occurred. *Note: Only works with an ATX type power supply.*

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

3. *Unlike other module designs available in the embedded market, a CMOS battery is not required by congatec modules to support the 'Power Loss Control' feature.*

9.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

9.6.1 Security Settings

Feature	Options	Description
Supervisor Password	Installed Not Installed	Reports if there is a supervisor password set.
User Password	Installed Not Installed	Reports if there is a user password set.
Change Supervisor Password	Enter password	Specifies the supervisor password.
User Access Level	No Access View Only Limited **Full Access**	Sets BIOS setup utility access rights for user level.
Boot Selection Popup Menu Access	**Anybody** Setup User Setup Supervisor No Access	Select who can access the boot selection popup menu when setup passwords are installed.
Change User Password	Enter password	Specifies the user password.
Password Check	**Setup** Always	Setup: Check password while invoking setup Always: Check password also on each boot.
Boot Sector Virus Protection	**Disabled** Enabled	Select *Enabled* to enable boot sector protection. The BIOS displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. If enabled, the following appears when a write is attempted to the boot sector. You may have to type N several times to prevent the boot sector write. *Boot Sector Write!* *Possible VIRUS: Continue (Y/N)?* The following appears after any attempt to format any cylinder, head or sector of any hard disk drive via the BIOS INT13 hard disk drive service: *Format!!!* *Possible VIRUS: Continue (Y/N)?*
BIOS Update & Write Protection	**Disabled** Enabled	Only visible if a supervisor password is installed. If enabled the BIOS update and modification utilities will ask for the supervisor password before allowing any write accesses to the BIOS flash ROM chip.
HDD Security Freeze Lock	**Enable** Disable	If enable, the Security Freeze Lock command will be issued during POST. This will prevent anybody from setting or changing a harddisk password after POST.

9.7 Exit Menu

Select the Exit tab from the setup menu to enter the Exit setup screen.

You can display an Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup and reboot so the new system configuration parameters can take effect.
Discard Changes and Exit	Exit setup without saving any changes made in the BIOS setup program.
Discard Changes	Discard changes without exiting setup. The option values presented when the computer was turned on are used.
Load CMOS Defaults	Load the CMOS defaults of all the setup options.

10 Additional BIOS Features

The conga-QA uses a congatec/AMIBIOS that is stored in an onboard Flash ROM chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as QMENR1xx, where QMEN is the congatec internal project name, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

10.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” refer to the user’s guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

10.2 BIOS Recovery

The “BIOS recovery” scenario is recommended for situations when the normal flash update fails and the user can no longer boot back to an OS to restore the system. The code that handles BIOS recovery resides in a section of the flash referred to as “boot block”.

For more information about “BIOS Recovery” refer to application note AN6_BIOS_Recovery.pdf, which can be found on the congatec AG website at www.congatec.com.

10.2.1 BIOS Recovery via Storage Devices

In order to make a BIOS recovery from an IDE CD-ROM (ISO9660), USB floppy or USB CD-ROM, the BIOS file must be copied into the root directory of the storage device and renamed *AMIBOOT.ROM*.

For more information about “BIOS Recovery via Storage Devices” refer to application note AN6_BIOS_Recovery.pdf, which can be found on the congatec AG website at www.congatec.com.

10.3 Serial Port and Console Redirection

Serial Redirection allows video and keyboard redirection via a standard RS-232 serial port. For more information about “Serial Port and Console Redirection” refer to application note AN2_Remote_Control.pdf, which can be found on the congatec AG website at www.congatec.com.

Note

The above mentioned feature is only applicable if an external Super I/O has been implemented on the carrier board.

10.4 BIOS Security Features

The BIOS provides both a supervisor and user password. If you use both passwords, the supervisor password must be set first. The system can be configured so that all users must enter a password every time the system boots or when setup is executed.

The two passwords activate two different levels of security. If you select password support you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed.

The supervisor password (supervisor mode) gives unrestricted access to view and change all the setup options. The user password (user mode) gives restricted access to view and change setup options.

If only the supervisor password is set, pressing <Enter> at the password prompt of the BIOS setup program allows the user restricted access to setup.

Setting the password check to ‘Always’ restricts who can boot the system. The password prompt will be displayed before the system attempts to load the operating system. If only the supervisor password is set, pressing <Enter> at the prompt allows the user to boot the system.

11 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Qseven Specification	http://www.qseven-standard.org/
Qseven Design Guide	http://www.qseven-standard.org/
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
PICMG® COM Express Module™ Base Specification	http://www.picmg.org/
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications