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the rhythm of embedded computing

Qseven® conga-QEVAL

Detailed description of the congatec Qseven® evaluation carrier board

User's Guide

Revision 1.2

Revision History

Revision	Date (dd.mm.yy)	Author	Changes
1.0	23.03.09	GDA	Official release
1.1	08.09.09	GDA	Removed description for socket CN44. SD/MMC PLUS is not supported on the conga-QEVAL. Added note about USB Client connector in section 4.2.5.
1.2	18.11.11	GDA	Corrected section 4.2.11, Qseven® modules do not support the PEG interface. Updated document throughout for conga-QEVAL hardware revision B.x.

Preface

This user's guide provides information about the components, features and connectors available on the conga-QEVAL Qseven® evaluation carrier board.

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Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Lead-Free Designs (RoHS)

All congatec AG products are created from lead-free components and are completely RoHS compliant.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Connector Type

Describes the connector that must be used with the Qseven® evaluation carrier board, not the connector found on the Qseven® evaluation carrier board.

Link to connector layout diagram

This link icon is located in the top left corner of each page. It provides a direct link to the connector layout diagram on page 8 of this document.

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Terminology

Term	Description
PCI Express (PCIe)	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4 or x16 link.
ExpressCard	A PCMCIA standard built on the latest USB 2.0 and PCI Express buses.
PCI Express Mini Card	PCI Express Mini Card add-in card is a small size unique form factor optimized for mobile computing platforms.
MMCplus	MMCplus was defined for first time in MMC System Specification v4.0. MMCplus is backward compatible with MMC. MMCplus has 13 pins.
SDIO card	SDIO (Secure Digital Input Output) is a non-volatile memory card format developed for use in portable devices.
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial-interface standard for hard disks
HDA	High Definition Audio
S/PDIF	S/PDIF (Sony/Philips Digital Interconnect Format) specifies a Data Link Layer protocol and choice of Physical Layer specifications for carrying digital audio signals between devices and stereo components.
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
LPC	Low Pin-Count: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy device support into a single IC.
I²C Bus	Inter-Integrated Circuit Bus: is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system.
SM Bus	System Management Bus: is a popular derivative of the I²C-bus.
CAN	Controller Area Network
SPI	Serial Peripheral Interface
GBE	Gigabit Ethernet
LVDS	Low-Voltage Differential Signaling
SDVO	Serial Digital Video Out is a proprietary technology introduced by Intel® to add additional video signaling interfaces to a system.
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

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Electrostatic Sensitive Device

All electronic parts described in this user's guide are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a carrier board or module except at an electrostatic-free workstation. Additionally, do not ship or store electronic devices near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging.

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Contents

1 Introduction

1.1 Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector and the pinout remains the same regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

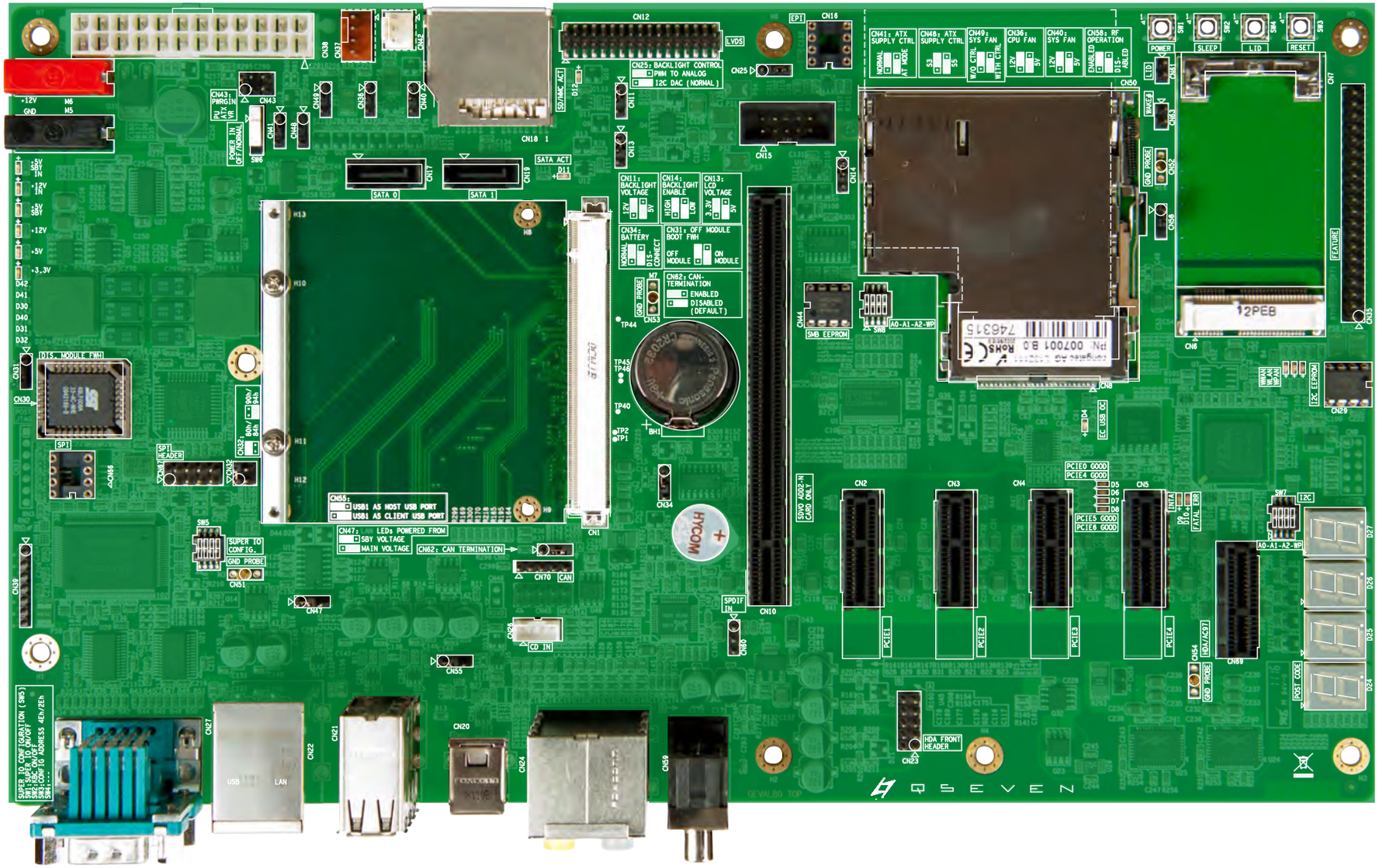
Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The Qseven® evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose what are suitable for their application. Qseven® applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no need to redesign the carrier board.

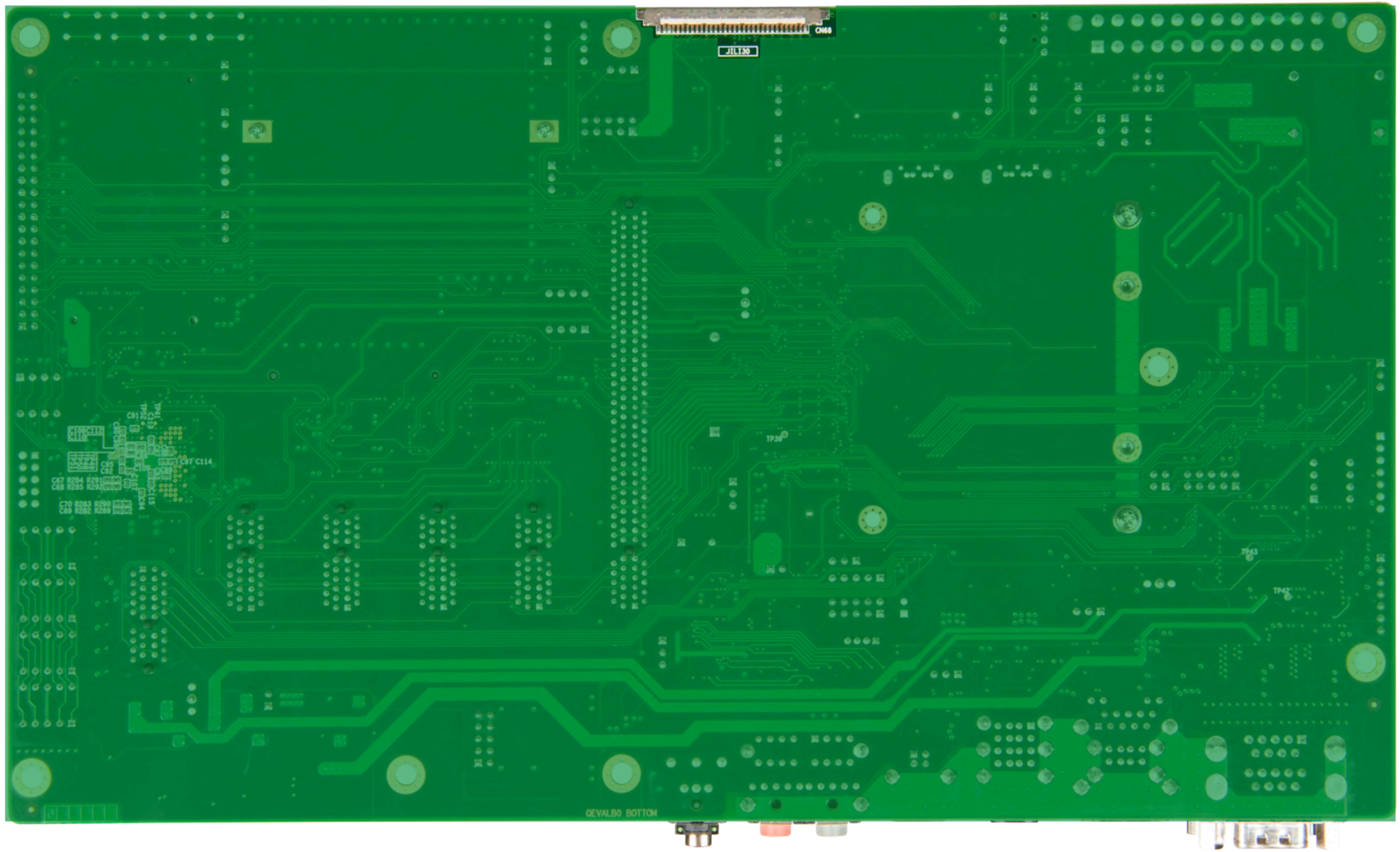
This document describes the features available on the Qseven® evaluation carrier board. Additionally, the schematics for the Qseven® evaluation carrier board can be found on the congatec website.

2 Connector Layout

The connector layout picture below shows each connector and its name designator. Jumpers and their respective Pin 1 are also shown. Select the Adobe 'Zoom-In-Tool' and zoom in on a given component to see its designator. Hover over the component and the 'Zoom-In-Tool' will change indicating there is a link. Click on the link to navigate to the area in the document where the component is described. Use the mouse icon in the top left hand corner of the destination page to return to the connector layout picture.



Connector Layout Bottom Side



3 Specifications

3.1 Mechanical Dimensions

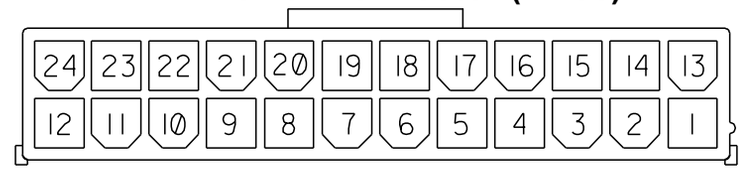
- 293.4mm x 171.5mm
- Height approximately 37mm

3.2 Power Supply

The conga-QEVAL can be used with standard ATX (Connector CN38) power supplies. The 3.3V, 5V and -5V power outputs of the ATX power supply are not used.

The following table lists the pinout for connector CN38.

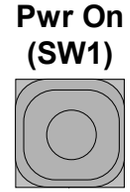
ATX Power Connector (CN38)

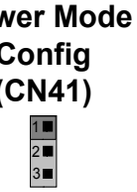


Pin	Signal	Description	Pin	Signal	Description
1	+3.3V	Power Supply +3.3VDC	13	+3.3V	Power Supply +3.3VDC
2	+3.3V	Power Supply +3.3VDC	14	-12V	Power Supply -12VDC
3	GND	Power Ground	15	GND	Power Ground
4	+5V	Power Supply +5VDC	16	PS_ON#	Power Supply On (active low). Short this pin to GND to switch power supply ON, disconnect from GND to switch OFF.
5	GND	Power Ground	17	GND	Power Ground
6	+5V	Power Supply +5VDC	18	GND	Power Ground
7	GND	Power Ground	19	GND	Power Ground
8	PWR_OK	Power Ok: A status signal generated by the power supply to notify the computer that the DC operating voltages are within the ranges required for proper computer operation.	20	-5V	Power Supply -5VDC
9	5V_SB	Standby Power Supply +5VDC	21	+5V	Power Supply +5VDC
10	+12V	Power Supply +12DC	22	+5V	Power Supply +5VDC
11	+12V	Power Supply +12DC	23	+5V	Power Supply +5VDC
12	+3.3V	Power Supply +3.3VDC	24	GND	Power Ground

When using an ATX power supply, the Qseven® module will start after the power-on button SW1 is pressed. The ATX power supply can also be used in AT mode. In this case the module will start after the power switch on the power supply is turned on. The power supply mode can be configured using jumper CN41.

Jumper CN41	Configuration
1 - 2	ATX Power supply (default)
2 - 3	ATX Power supply runs in AT mode



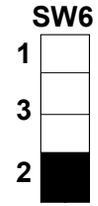


Connector Type

CN41 : 2.54mm grid jumper.

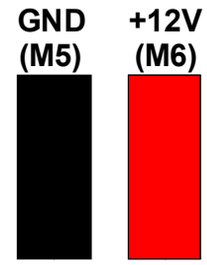
The input voltage can be disconnected from power sources through the use of switch SW6.

SW6	Configuration
ON (1 - 3)	Input power voltage is ON (default)
OFF (2 - 3)	Input power voltage is forced off



The conga-QEVAL can also be used with +12VDC power supply (connector M5 and M6). The +3.3V and +5V used by some devices on the conga-QEVAL are generated onboard from the +12V power supply.

Connector	Configuration
M5	Ground
M6	+12VDC ±5%



Connector Type

4mm diameter plug

3.2.1 PWR_OK Signal

The Qseven® specification defines the signal PWRGIN, which is a HIGH active input from the main power supply to the module and indicates whether the power is good. Jumper CN43 on the conga-QEVAL provides the ability to choose different settings for this signal.

Jumper CN43	Configuration
1 - 2	PWGIN generated by Pull-up resistor. (default)
3 - 4	PWGIN generated by ATX power source.
5 - 6	PWGIN generated by DC/DC converter.

PWGIN Config. (CN43)

Connector Type

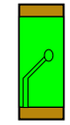
CN43: 2.54mm grid jumper.

3.2.2 Power Status LEDs D30-D32 and D40-D42

The six green status LEDs D30-D32 and D40-D42 indicate different power states of the conga-QEVAL. Refer to the following table for detailed information.

LEDs D30-D32 and D40-D42	Power state
All Off	No power applied.
D30	+5V Standby power is present.
D31	+5V is present.
D32	+3.3V is present
D40	+12V is present
D41	+12V_IN is present
D42	+5V_SBY_IN is present

D30-D32
D40-D42



3.2.3 Power-up Control

The native system Power-up support of Qseven® modules uses the *'SUS_S3#'* signal to control the *'PS_ON#'* signal, which is used to switch the ATX power supply on or off. When using the *SUS_S3#'* signal the Qseven® module is capable of supporting Suspend to RAM (S3).

When the system goes to Suspend to RAM (S3) or Soft Off (S5), the *'SUS_S3#'* signal is asserted by the chipset of the module. Through the use of an inverter, the low active *'PS_ON#'* signal goes high and switches off the ATX power supply. Vice versa, if the system resides in a power-down system state, any system wake-up event invokes the chipset of the module to deassert the *'SUS_S3#'* signal. This results in a system transition to Full-On (S0).

The way Suspend to RAM is implemented on a Qseven® module may differ depending on the module manufacturer. For this reason, it is recommended that a hardware jumper be implemented on the carrier board in order to provide the ability to choose if the *'PS_ON#'* signal should be controlled either by the *'SUS_S3#'* signal or '*SUS_S5#'* signal. On the conga-QEVAL this is accomplished through the use of jumper CN48.

Jumper CN48	Configuration
1 - 2	ATX Power supply controlled via S3# (default)
2 - 3	ATX Power supply controlled via S5#

Control signal Config (CN48)

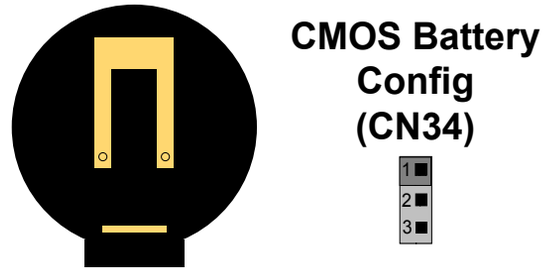
Connector Type

CN48 : 2.54mm grid jumper.

3.3 CMOS Battery

The conga-QEVAL includes a battery that supplies the RTC and CMOS memory of the Qseven® module. The battery needs to provide 3V of power. The specified battery type is CR2032. It is possible to disconnect the CMOS battery using jumper CN34.

Jumper CN34	Configuration
1 - 2	Normal operation, battery connected (default)
2 - 3	Battery disconnected



Connector Type

CN34 : 2.54mm grid jumper.

Warning

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

To fulfill the requirements of the EN60950, the conga-QEVAL incorporates two current-limiting devices (resistor and diode) in the battery power supply path.

3.4 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

The above operating temperatures must be strictly adhered to at all times.

Humidity specifications are for non-condensing conditions.

4 Connector Description

4.1 Connector CN1 Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Power Ground	2	GND	Power Ground
3	GBE_MDI3-	Gigabit Ethernet MDI3-	4	GBE_MDI2-	Gigabit Ethernet MDI2-
5	GBE_MDI3+	Gigabit Ethernet MDI3+	6	GBE_MDI2+	Gigabit Ethernet MDI2+
7	GBE_LINK100#	100 Mbps link speed	8	GBE_LINK1000#	1000 Mbps link speed
9	GBE_MDI1-	Gigabit Ethernet MDI1-	10	GBE_MDI0-	Gigabit Ethernet MDI0-
11	GBE_MDI1+	Gigabit Ethernet MDI1+	12	GBE_MDI0+	Gigabit Ethernet MDI0+
13	GBE_LINK#	Gigabit Ethernet Link indicator	14	GBE_ACT#	Gigabit Ethernet Activity indicator
15	GBE_CTREF	Reference voltage for GBE	16	SUS_S5#	S5 (Soft OFF) – shutdown state
17	WAKE#	External system wake event	18	SUS_S3#	S3 (Suspend to RAM) – SLP
19	SUS_STAT#	Suspend status	20	PWRBTN#	Power button
21	SLP_BTN#	Sleep button	22	LID_BTN#	LID button
23	GND	Power Ground	24	GND	Power Ground
25	GND	Power Ground	26	PWGIN	Power good input
27	BATLOW#	Battery low input	28	RSTBTN#	Reset button input
29	SATA0_TX+	Serial ATA Channel 0 TX+	30	SATA1_TX+	Serial ATA Channel 1 TX+
31	SATA0_TX-	Serial ATA Channel 0 TX-	32	SATA1_TX-	Serial ATA Channel 1 TX-
33	SATA_ACT#	Serial ATA Activity	34	GND	Power Ground
35	SATA0_RX+	Serial ATA Channel 0 RX+	36	SATA1_RX+	Serial ATA Channel 1 RX+
37	SATA0_RX-	Serial ATA Channel 0 RX-	38	SATA1_RX-	Serial ATA Channel 1 RX-
39	GND	Power Ground	40	GND	Power Ground
41	BIOS_DISABLE# /BOOT_ALT#	BIOS Module disable Boot Alternative Enable	42	SDIO_CLK	SDIO Clock Output
43	SDIO_CD#	SDIO Card Detect	44	SDIO_LED	SDIO LED
45	SDIO_CMD	SDIO Command/Response	46	SDIO_WP	SDIO Write Protect
47	SDIO_PWR#	SDIO Power Enable	48	SDIO_DAT1	SDIO Data Line 1
49	SDIO_DAT0	SDIO Data Line 0	50	SDIO_DAT3	SDIO Data Line 3
51	SDIO_DAT2	SDIO Data Line 2	52	SDIO_DAT5	SDIO Data Line 5
53	SDIO_DAT4	SDIO Data Line 4	54	SDIO_DAT7	SDIO Data Line 7
55	SDIO_DAT6	SDIO Data Line 6	56	RESERVED	
57	GND	Power Ground	58	GND	Power Ground
59	HDA_SYNC	HD Audio/AC'97 Synchronization	60	SMB_CLK	SMBus Clock line
61	HDA_RST#	HD Audio/AC'97 Codec Reset	62	SMB_DAT	SMBus Data line
63	HDA_BITCLK	HD Audio/AC'97 Serial Bit Clock	64	SMB_ALERT#	SMBus Alert input
65	HDA_SDI	HD Audio/AC'97 Serial Data In	66	I2C_CLK	I2C Bus Clock
67	HDA_SDO	HD Audio/AC'97 Serial Data Out	68	I2C_DAT	I2C Bus Data

Pin	Signal	Description	Pin	Signal	Description
69	THRM#	Thermal Alarm active low	70	WDTRIG#	Watchdog trigger signal
71	THRMTRIP#	Thermal Trip indicates an overheating condition	72	WDOUT	Watchdog event indicator
73	GND	Power Ground	74	GND	Power Ground
75	USB_P7-	USB Port 7 Differential Pair-	76	USB_P6-	USB Port 6 Differential Pair-
77	USB_P7+	USB Port 7 Differential Pair+	78	USB_P6+	USB Port 6 Differential Pair+
79	USB_6_7_OC#	Over current detect input 6/7 USB	80	USB_4_5_OC#	Over current detect input 4/5 USB
81	USB_P5-	USB Port 5 Differential Pair-	82	USB_P4-	USB Port 4 Differential Pair-
83	USB_P5+	USB Port 5 Differential Pair+	84	USB_P4+	USB Port 4 Differential Pair+
85	USB_2_3_OC#	Over current detect input 2/3 USB	86	USB_0_1_OC#	Over current detect input 0/1 USB
87	USB_P3-	USB Port 3 Differential Pair-	88	USB_P2-	USB Port 2 Differential Pair-
89	USB_P3+	USB Port 3 Differential Pair+	90	USB_P2+	USB Port 2 Differential Pair+
91	USB_CC	USB Client present detect pin	92	USB_ID	USB ID pin
93	USB_P1-	USB Port 1 Differential Pair-	94	USB_P0-	USB Port 0 Differential Pair-
95	USB_P1+	USB Port 1 Differential Pair+	96	USB_P0+	USB Port 0 Differential Pair+
97	GND	Power Ground	98	GND	Power Ground
99	LVDS_A0+	LVDS Primary channel 0+	100	LVDS_B0+	LVDS Secondary channel 0+
101	LVDS_A0-	LVDS Primary channel 0-	102	LVDS_B0-	LVDS Secondary channel 0-
103	LVDS_A1+	LVDS Primary channel 1+	104	LVDS_B1+	LVDS Secondary channel 1+
105	LVDS_A1-	LVDS Primary channel 1-	106	LVDS_B1-	LVDS Secondary channel 1-
107	LVDS_A2+	LVDS Primary channel 2+	108	LVDS_B2+	LVDS Secondary channel 2+
109	LVDS_A2-	LVDS Primary channel 2-	110	LVDS_B2-	LVDS Secondary channel 2-
111	LVDS_PPEN	LVDS Power enable	112	LVDS_BLEN	LVDS Backlight enable
113	LVDS_A3+	LVDS Primary channel 3+	114	LVDS_B3+	LVDS Secondary channel 3+
115	LVDS_A3-	LVDS Primary channel 3-	116	LVDS_B3-	LVDS Secondary channel 3-
117	GND	Power Ground	118	GND	Power Ground
119	LVDS_A_CLK+	LVDS Primary channel CLK+	120	LVDS_B_CLK+	LVDS Secondary channel CLK+
121	LVDS_A_CLK-	LVDS Primary channel CLK-	122	LVDS_B_CLK-	LVDS Secondary channel CLK-
123	LVDS_BLT_CTRL /GP_PWM_OUT0	PWM Backlight brightness General Purpose PWM Output	124	RESERVED	
125	LVDS_DID_DAT /GP_I2C_DAT	DDC Display ID Data line General Purpose I2C Data line	126	LVDS_BLC_DAT	SSC clock chip data line
127	LVDS_DID_CLK //GP_I2C_CLK	DDC Display ID Clock line General Purpose I2C Clock line	128	LVDS_BLC_CLK	SSC clock chip clock line
129	CAN0_TX	CAN TX Output for CAN Bus Channel 0	130	CAN0_RX	CAN RX Input for CAN Bus Channel 0
131	SDVO_BCLK+	SDVO Clock line+	132	SDVO_INT+	SDVO Interrupt line+
133	SDVO_BCLK-	SDVO Clock line-	134	SDVO_INT-	SDVO Interrupt line-
135	GND	Power Ground	136	GND	Power Ground
137	SDVO_GREEN+	SDVO Green line+	138	SDVO_FLDINSTALL+	SDVO Field stall line+
139	SDVO_GREEN-	SDVO Green line-	140	SDVO_FLDINSTALL-	SDVO Field stall line-
141	GND	Power Ground	142	GND	Power Ground
143	SDVO_BLUE+	SDVO Blue line+	144	SDVO_TVCLKIN+	SDVO TV-Out line+

Pin	Signal	Description	Pin	Signal	Description
145	SDVO_BLUE-	SDVO Blue line-	146	SDVO_TVCLKIN-	SDVO TV-Out line-
147	GND	Power Ground	148	GND	Power Ground
149	SDVO_RED+	SDVO Red line+	150	SDVO_CTRL_DAT	I2C based control clock for SDVO
151	SDVO_RED-	SDVO Red line-	152	SDVO_CTRL_CLK	I2C based control data for SDVO
153	HDMI_HPD#	Hot plug detection for HDMI	154	DP_HPD#	Hot plug detection for Display port
155	PCIE_CLK_REF+	PCI Express Reference Clock+	156	PCIE_WAKE#	PCI Express Wake event
157	PCIE_CLK_REF-	PCI Express Reference Clock-	158	PCIE_RST#	Reset Signal for external devices
159	GND	Power Ground	160	GND	Power Ground
161	PCIE3_TX+	PCI Express Channel 3 Output+	162	PCIE3_RX+	PCI Express Channel 3 Input+
163	PCIE3_TX-	PCI Express Channel 3 Output-	164	PCIE3_RX-	PCI Express Channel 3 Input-
165	GND	Power Ground	166	GND	Power Ground
167	PCIE2_TX+	PCI Express Channel 2 Output+	168	PCIE2_RX+	PCI Express Channel 2 Input+
169	PCIE2_TX-	PCI Express Channel 2 Output-	170	PCIE2_RX-	PCI Express Channel 2 Input-
171	EXCD0_PERST#	Express Card slot#0 reset	172	EXCD1_PERST#	Express Card slot#1 reset
173	PCIE1_TX+	PCI Express Channel 1 Output+	174	PCIE1_RX+	PCI Express Channel 1 Input+
175	PCIE1_TX-	PCI Express Channel 1 Output-	176	PCIE1_RX-	PCI Express Channel 1 Input-
177	EXCD0_CPPE#	Express Card slot#0 Capable/Req	178	EXCD1_CPPE#	Express Card slot#0 Capable/Req
179	PCIE0_TX+	PCI Express Channel 0 Output+	180	PCIE0_RX+	PCI Express Channel 0 Input+
181	PCIE0_TX-	PCI Express Channel 0 Output-	182	PCIE0_RX-	PCI Express Channel 0 Input-
183	GND	Power Ground	184	GND	Power Ground
185	LPC_AD0	LPC Interface Address/Data 0	186	LPC_AD1	LPC Interface Address/Data 1
187	LPC_AD2	LPC Interface Address/Data 0	188	LPC_AD3	LPC Interface Address/Data 3
189	LPC_CLK	LPC Interface Clock	190	LPC_FRAME#	LPC frame indicator
191	SERIRQ	Serialized interrupt	192	LPC_LDRQ#	LPC DMA request
193	VCC_RTC	3V backup cell input	194	SPKR /GP_PWM_OUT2	Output for audio enunciator General Purpose PWM Output
195	FAN_TACHOIN /GP_TIMER_IN	Fan tachometer input General Purpose Timer In	196	FAN_PWMOUT /GP_PWM_OUT1	Fan speed control (PWM) General Purpose PWM Output
197	GND	Power Ground	198	GND	Power Ground
199	SPI_MOSI	SPI Master serial output/Slave serial input	200	SPI_CS0	SPI Chip Select 0 Output
201	SPI_MISO	SPI Master serial input/Slave serial output signal	202	SPI_CS1	SPI Chip Select 1 Output
203	SPI_SCK	SPI Clock Output	204	MFG_NC4	Do not connect on carrier board
205	VCC_5V_SB	+5VDC,Standby ±5%	206	VCC_5V_SB	+5VDC Standby ±5%
207	MFG_NC0	Do not connect on carrier board	208	MFG_NC2	Do not connect on carrier board
209	MFG_NC1	Do not connect on carrier board	210	MFG_NC3	Do not connect on carrier board
211	VCC	Power supply +5VDC ±5%	212	VCC	Power supply +5VDC ±5%
213	VCC	Power supply +5VDC ±5%	214	VCC	Power supply +5VDC ±5%
215	VCC	Power supply +5VDC ±5%	216	VCC	Power supply +5VDC ±5%
217	VCC	Power supply +5VDC ±5%	218	VCC	Power supply +5VDC ±5%
219	VCC	Power supply +5VDC ±5%	220	VCC	Power supply +5VDC ±5%
221	VCC	Power supply +5VDC ±5%	222	VCC	Power supply +5VDC ±5%

Pin	Signal	Description	Pin	Signal	Description
223	VCC	Power supply +5VDC ±5%	224	VCC	Power supply +5VDC ±5%
225	VCC	Power supply +5VDC ±5%	226	VCC	Power supply +5VDC ±5%
227	VCC	Power supply +5VDC ±5%	228	VCC	Power supply +5VDC ±5%
229	VCC	Power supply +5VDC ±5%	230	VCC	Power supply +5VDC ±5%

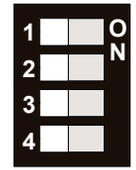
4.2 Subsystems of conga-QEVAL

4.2.1 SMBus

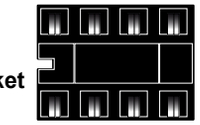
The System Management Bus (SMBus) signals are available in different locations on the conga-QEVAL including the feature connector (CN35) described in section 5.10 of this document. Additionally, the conga-QEVAL includes a socket for a SMBus EEPROM (CN44) that can be used for test purposes during the system development. This 8 pin DIP socket can be used with different 2-wire serial EEPROMS. The address inputs (A0-A2) and write protect (WP) pin of SMBus EEPROM can be configured using SW8 dip switch. When ON / OFF is configured, the pin is set to LOW / HIGH level. Default setting is LOW level on all pins.

Dips	Signal
1 ON/OFF	A0 set to LOW/HIGH
2 ON/OFF	A1 set to LOW/HIGH
3 ON/OFF	A2 set to LOW/HIGH
4 ON/OFF	WP set to LOW/HIGH

SW8



CN44
EEPROM Socket

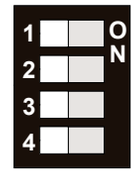


4.2.2 I²C Bus

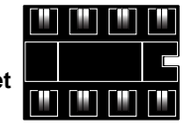
The I²C signals are available in different locations on the conga-QEVAL including the feature connector (CN35) described in section 5.10 of this document. Additionally, the conga-QEVAL includes a socket for an I²C EEPROM (CN29) that can be used for test purposes during the system development. This 8 pin DIP socket can be used with different 2-wire serial EEPROMS (for example 24C04 / 08 / 16 ...) and can be accessed easily by using the I²C control commands implemented in the Qseven® EASI API driver. Refer to the Qseven® module's user's guide and the EASI programmers guide for details. The address inputs (A0-A2) and write protect (WP) pin of I²C EEPROM can be configured using SW7 dip switch. When ON / OFF is configured, the pin is set to LOW / HIGH level. Default setting is LOW level on all pins.

Dips	Signal
1 ON/OFF	A0 set to LOW/HIGH
2 ON/OFF	A1 set to LOW/HIGH
3 ON/OFF	A2 set to LOW/HIGH
4 ON/OFF	WP set to LOW/HIGH

SW7



CN29
EEPROM Socket



4.2.3 SPI Bus

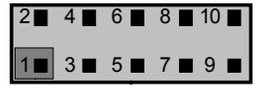
The conga-QEVAL provides a connection to the Serial Peripheral Interface (SPI) Bus via connector CN67 and also an 8 pin EEPROM socket for SPI EEPROM is available on the carrier board. The 8 pin DIP socket (connector CN66) can be used for SPI EEPROM (for example AT25010 / 020 / 040 ...). The write protect (WP#) and hold (HOLD#) pins are internally pulled up and allows normal read/write operations.

The chip select (CS#) signal on the SPI EEPROM socket is connected to the Qseven® module's SPI_CS0# signal and is active only if BOOT_ALT# is selected (see connector CN31).

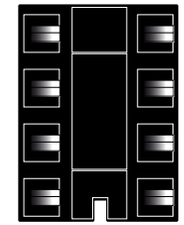
SPI connector CN67

Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
3	SPI_MOSI	4	SPI_CS0#
5	SPI_MISO	6	SPI_CS1#
7	SPI_SCK	8	N.C.
9	GND	10	GND

SPI Header (CN67)



CN66
EEPROM Socket



Connector Type

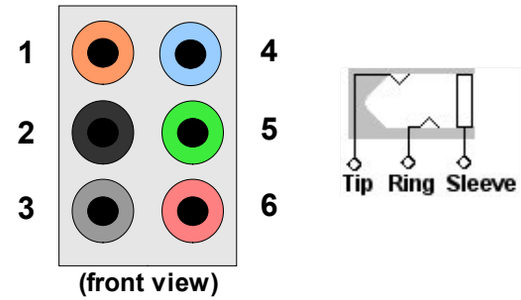
CN67: 10 pin, 2 row 2.54mm grid female.

4.2.4 HDA Audio

The conga-QEVAL has an HDA (High Definition Audio) codec (Realtek ALC888) mounted on it. The 7.1 channel audio output interface of this codec is available on the connector described below. The drivers for this codec can be found on the congatec website at www.congatec.com in the 'Drivers' section under 'conga-QEVAL'.

Stereo Jack 1	Signal	Stereo Jack 4	Signal
Tip	Center	Tip	Line Input Left
Ring	LFE	Ring	Line Input Right
Sleeve	Analog Ground	Sleeve	Analog Ground
Stereo Jack 2	**Signal**	**Stereo Jack 5**	**Signal**
Tip	Surround Left	Tip	Line Output Left
Ring	Surround Right	Ring	Line Output Right
Sleeve	Analog Ground	Sleeve	Analog Ground
Stereo Jack 3	**Signal**	**Stereo Jack 6**	**Stereo Mode**
Tip	Side Surround Left	Tip	Microphone Input Left
Ring	Side Surround Right	Ring	Microphone Input Right
Sleeve	Analog Ground	Sleeve	Analog Ground

Audio (CN24)



(front view)

Connector Type

CN24: 6 dedicated 3.5mm audio jacks (7.1 channel).

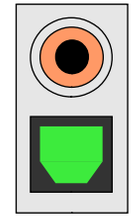
S/PDIF IN connector CN60

Pin	Signal
1	+5V Power supply
2	S/PDIF Input
3	Ground

S/PDIF IN (CN60)

S/PDIF Out connector CN59 (S/PDIF OUT is available via RCA or optical connector).

S/PDIF OUT (CN59)



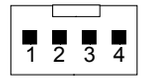
Connector Type

CN60 3 pin, 2.54mm grid female, CN59 RCA and optical audio.

CD IN connector CN26

Pin	Signal
1	CD Input Left
2	Analog Ground
3	Analog Ground
4	CD Input Right

CD-IN CN26



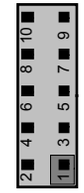
Connector Type

CN26 4 pin, 2.54mm grid female.

HDA Front Header connector CN23

Pin	Signal	Pin	Signal
1	Microphone 2 Input Left	2	Analog Ground
3	Microphone 2 Input Right	4	HDA_PRESENCE#
5	Line 2 Output Right	6	Microphone 2 Sense
7	Analog Ground	8	N.C.
9	Line 2 Output Left	10	Line 2 Sense

HDA Front Header (CN23)



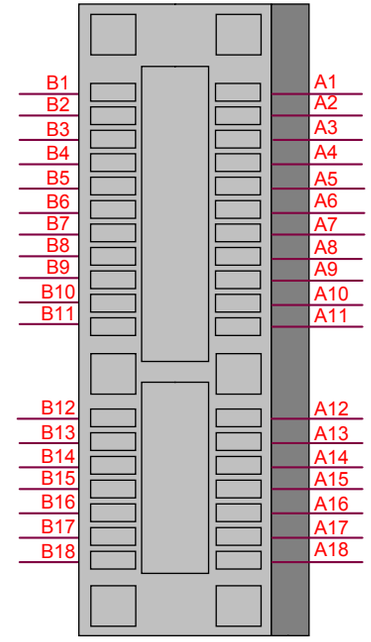
Connector Type

CN23 10 pin, 2 row 2.54mm grid female.

The conga-QEVAL also provides the HDA interface on a edge card connector (CN69) for additional AC'97 or HDA codec support.

Pin	Signal	Pin	Signal
B1	+12V	A1	PRSNT1#
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	N.C.	A5	HDA_BCLK
B6	N.C.	A6	HDA_SDOUT
B7	GND	A7	HDA_SDIN
B8	+3.3V	A8	HDA_SYNC
B9	HDA_RST#	A9	+3.3V
B10	+3.3V AUX	A10	+3.3V
B11	N.C.	A11	N.C.
Key			
B12	SPKR	A12	GND
B13	GND	A13	N.C.
B14	N.C.	A14	N.C.
B15	N.C.	A15	GND
B16	GND	A16	N.C.
B17	PRSNT2#	A17	N.C.
B18	GND	A18	GND

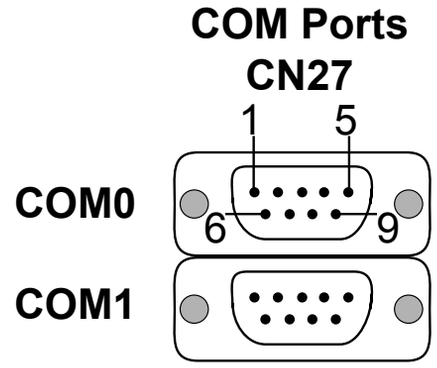
HDA Edge Card Connector (CN69)



4.2.5 LPC Super I/O Device

The conga-QEVAL utilizes a Super I/O controller that provides additional interfaces such as two serial ports via connector CN27. The Winbond W83627DHG controller is connected to the LPC Bus of the Qseven® module. Serial ports COM0 and COM1 follow the RS232 standard.

Pin	COM0	COM1
1	DCD#	DCD#
2	RXD	RXD
3	TXD	TXD
4	DTR#	DTR#
5	GND	GND
6	DSR	DSR
7	RTS#	RTS#
8	CTS#	CTS#
9	RI#	RI#

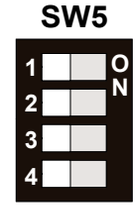


Connector Type

CN27 2x 9 pin D-SUB female.

The Super I/O controller can be configured using the SW5 dip switch. SW5 can be used to either disable the Super I/O or configure its base address. The following table describes the settings for SW5.

Dips	Configuration
1 ON/OFF	Super I/O Enabled/Disabled (ON=default)
2 ON/OFF	KBC Enabled/Disabled
3 ON/OFF	Super I/O configured for address 4Eh/2Eh
4	N.C.



PS2 mouse or keyboard can be connected to the KBC interface of the Super I/O controller via connector CN39.

Pin	Signal
1	Keyboard Data
2	N.C.
3	Mouse Data
4	GND
5	+5V power supply
6	Keyboard Clock
7	Mouse Clock

KBC (CN39)

Connector Type

CN39 7 pin, 2.54mm grid female.

4.2.6 LPC Firmware Hub

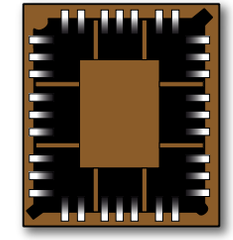
The conga-QEVAL offers the possibility to boot the Qseven® CPU module from an external firmware hub. This can be very useful when a customized BIOS must be evaluated.

The evaluation carrier board includes one 32-lead PLCC socket for one LPC firmware hub (socket CN30). With jumper CN31, the user can configure whether the Qseven® module should boot from its onboard BIOS or from a BIOS located in the external firmware hub. The yellow LED D23 is lit when the Qseven® module boots from the external firmware hub.

Jumper CN31	Configuration
1 - 2	Qseven® module boots from external FWH (CN30)
2 - 3	Qseven® module boots from onboard FWH (default)

Boot Config (CN31)

CN30
PLCC Socket



D23

Connector Type

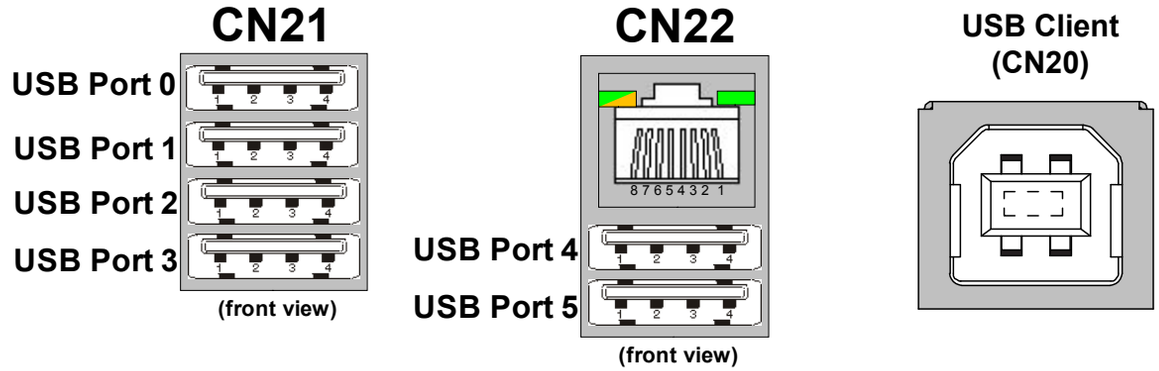
CN31: 2.54mm grid jumper.

4.2.7 Universal Serial Bus (USB)

The conga-QEVAL provides 6 USB ports (USB Ports 0-5) via connectors CN21 and CN22. USB Ports 4 and 5 found on connector CN22 are supplied by suspend power and can be used to test “wake-up via USB” functionality. Connector CN20 (USB B type) can be used for USB client connection. CN20 utilizes USB Port 1.

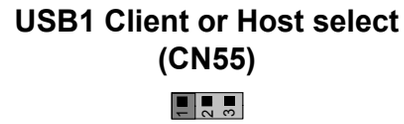
USB connector pinout

Pin	Signal
1	+5V
2	DATA-
3	DATA+
4	GND



USB port 1 can be configured as either Client or Host through the use of jumper CN55. USB port 1 Host is available on CN21 and Client on CN20.

Jumper CN55	Configuration
1 - 2	USB port 1 as Host (default)
2 - 3	USB port 1 as Client



Connector Type

CN55: 2.54mm grid jumper.

Note

If USB Client connector CN20 is enabled within the Qseven® module’s BIOS setup program, then the USB Port 1 connector (CN21) is not available.

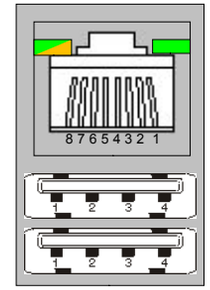
4.2.8 Ethernet 10/100/1000

The conga-QEVAL provides a LAN interface via connector CN22. The following tables describe the pinout and configuration possibilities.

RJ45 socket pinout

Pin	Signal	Pin	Signal
1	Bidirectional pair A+	2	Bidirectional pair A-
3	Bidirectional pair B+	4	Bidirectional pair C+
5	Bidirectional pair C-	6	Bidirectional pair B-
7	Bidirectional pair D+	8	Bidirectional pair D+

CN22



(front view)

RJ45 Socket LED descriptions

LED Left Side	Description
Off	10 Mbps link speed
Green	100 Mbps link speed
Orange	1000 Mbps link speed

LED Right Side	Description
Off	No link
Steady On	Link established, no activity detected
Blinking	Link established, activity detected

Jumper CN47 provides the ability to select the power source for the LAN controller.

Jumper CN47	Description
1 - 2	LAN controller is powered from standby voltage (default)
2 - 3	LAN controller is powered from main voltage

LAN Power Source Config (CN47)

Connector Type

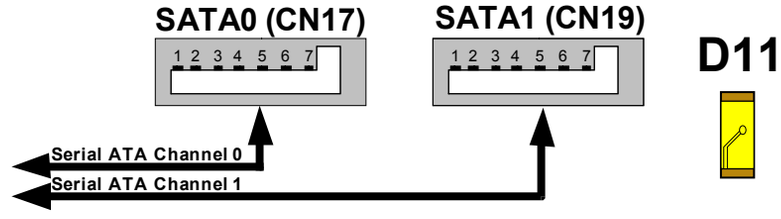
8 pin RJ45 plug

CN47: 2.54mm grid jumper

4.2.9 Serial ATA™

The conga-QEVAL provides two SATA drive connectors, CN17 and CN19. The yellow LED D11 indicates when there is activity on either of the SATA interfaces. The following table describes the pinout of the SATA connectors.

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND



4.2.10 LVDS Flat Panel Interface

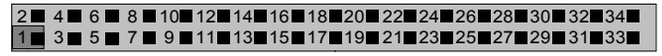
The conga-QEVAL provides two different connectors for LVDS. LVDS output is available on connectors CN12 and CN68 (CN68 is located on the bottom side of the conga-QEVAL).

Pin	LVDS Output	Description	Pin	LVDS Output	Description
1	LVDS_DID_DAT	DisplayID DDC data line used for LVDS flat panel detection.	2	LVDS_DID_CLK	DisplayID DDC clock line used for LVDS flat panel detection.
3	N.C.		4	N.C.	
5	GND	Power Ground	6	LVDS_A0-	LVDS Channel A differential pairs
7	LVDS_A0+	LVDS Channel A differential pairs	8	LVDS_PPEN	Controls panel power enable
9	LVDS_A1-	LVDS Channel A differential pairs	10	LVDS_A1+	LVDS Channel A differential pairs
11	LVDS_BLEN	Controls backlight enable. (see jumper CN14)	12	LVDS_A2+	LVDS Channel A differential pairs
13	LVDS_A2-	LVDS Channel A differential pairs	14	N.C.	
15	LVDS_A_CLK-	LVDS Channel A differential clock	16	LVDS_A_CLK+	LVDS Channel A differential clock
17	N.C.		18	LVDS_A3+	LVDS Channel A differential pairs
19	LVDS_A3-	LVDS Channel A differential pairs	20	GND	
21	LVDS_B0-	LVDS Channel B differential pairs	22	LVDS_B0+	LVDS Channel B differential pairs
23	GND	Power Ground	24	LVDS_B1-	LVDS Channel B differential pairs
25	LVDS_B1+	LVDS Channel B differential pairs	26	GND	Power Ground
27	LVDS_B2-	LVDS Channel B differential pairs	28	LVDS_B2+	LVDS Channel B differential pairs
29	GND	Power Ground	30	LVDS_B_CLK+	LVDS Channel B differential clock
31	LVDS_B_CLK-	LVDS Channel B differential clock	32	N.C.	
33	LVDS_B3+	LVDS Channel B differential pairs	34	LVDS_B3-	LVDS Channel B differential pairs

Connector Type

CN12: 34 pin, 2 row 2mm grid female.

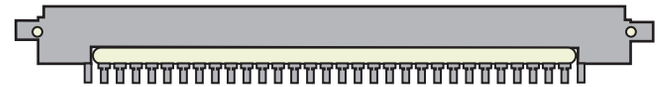
LVDS (CN12)



LVDS output is available on connector CN68 (signal descriptions can be found in the table on the previous page).

Pin	LVDS Output	Pin	LVDS Output
1	GND	17	LVDS_B1+
2	LVDS_A0-	18	GND
3	LVDS_A0+	19	LVDS_B2-
4	LVDS_A1-	20	LVDS_B2+
5	LVDS_A1+	21	LVDS_B_CLK-
6	LVDS_A2-	22	LVDS_B_CLK+
7	LVDS_A2+	23	LVDS_B3-
8	GND	24	LVDS_B3+
9	LVDS_A_CLK-	25	GND
10	LVDS_A_CLK+	26	LVDS_DID_DAT
11	LVDS_A3-	27	LVDS_PPEN
12	LVDS_A3+	28	LVDS_DID_CLK
13	LVDS_B0-	29	VDD_LCD (2A Fuse)
14	LVDS_B0+	30	VDD_LCD (2A Fuse)
15	GND	31	VDD_LCD (2A Fuse)
16	LVDS_B1-	32	GND

LVDS Connector (CN68)



Connector Type

CN68: JAE FI-X30SSL-HF, 32 pin, single row, 1mm pitch spacing (compatible with JILI30).

The polarity of the backlight enable signal LVDS_BLEN from the Qseven® module can be set up using configuration jumper CN14.

Jumper CN14	Configuration
1 - 2	Backlight enable HIGH active (default)
2 - 3	Backlight enable LOW active

Backlight Polarity Config (CN14)

Connector Type

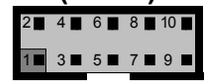
CN14: 2.54mm grid jumper.

4.2.10.1 Flat Panel and Backlight Power Supply

The power supply for flat panels and their backlight inverter is available on connector CN15. Panel and backlight voltage can be selected using jumpers CN13 and CN11. Analog backlight control (BL_CTRL_AN) can be set by jumper CN25. The table below describes the pinout for connector CN15. The flat panel and backlight power supply connection can be seen on the following page.

Pin	Signal	Pin	Signal
1	VDD_LCD (2A Fuse)	2	VDD_BL (0.75A Fuse)
3	+5V (2A Fuse)	4	+12V (0.75A Fuse)
5	LVDS_PPEN	6	LVDS_BLEN
7	BL_CTRL_AN	8	BL_CTRL
9	GND	10	GND

LCD Power (CN15)



Connector Type

CN15: 10 pin, 2 row 2.54 mm grid female.

Jumper CN13	Configuration
1 - 2	Backlight by PWM to Analog
2 - 3	Backlight by I2C DAC (default)

Backlight Control (CN25)

Jumper CN13	Configuration
1 - 2	+3.3VDC LCD Voltage
2 - 3	+5VDC LCD Voltage (default)

LCD Power Config (CN13)

Jumper CN11	Configuration
1 - 2	+12VDC Backlight Voltage (default)
2 - 3	+5VDC Backlight Voltage

Backlight Power Config (CN11)

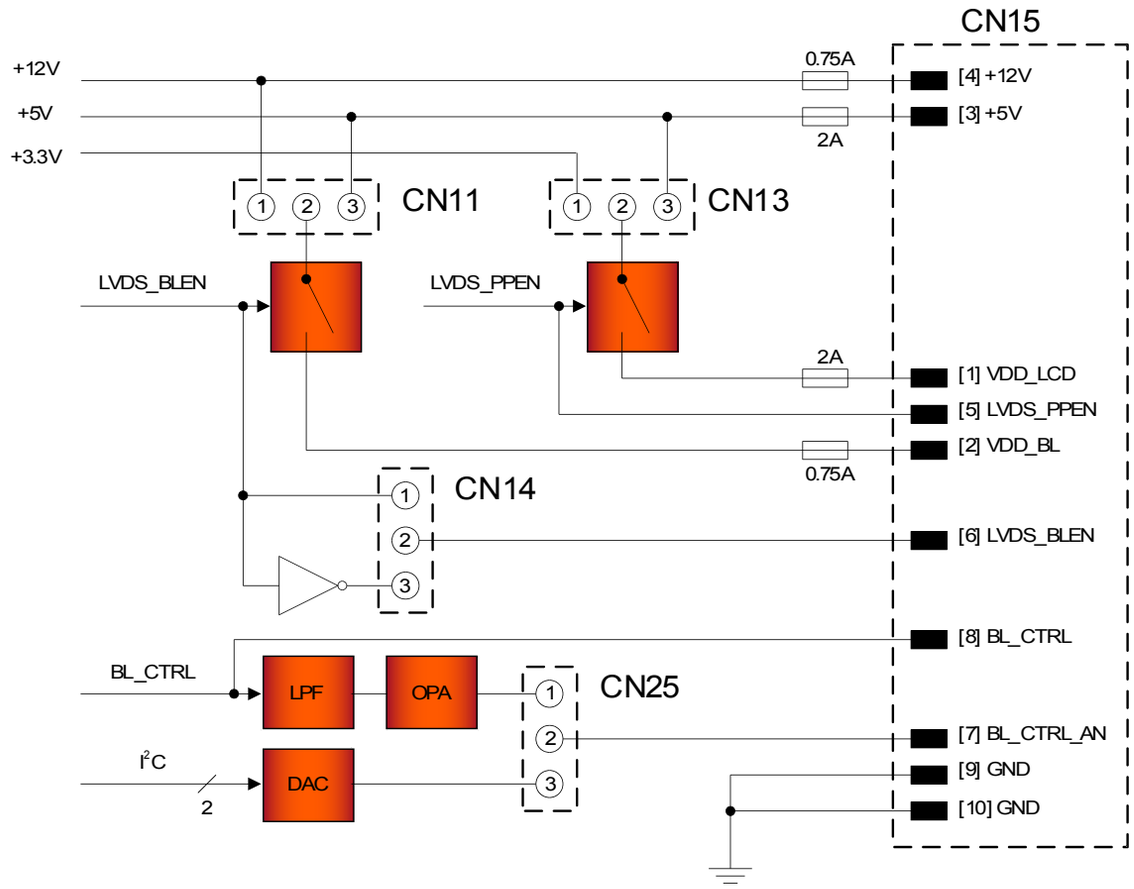
Connector Type

CN11 and CN13 and CN25 2.54mm grid jumpers.

4.2.10.2 Flat Panel and Backlight Power Supply Connection

The following diagram shows a typical connection possibility for powering panel/backlight by either the VDD_LCD/VDD_BL signals or by using LVDS_PPEN/LVDS_BLEN for external power switches.

- Signals 1-10 correspond to signals 1-10 found on the CN15 connector.
- CN11, CN13, CN14 and CN25 represent jumpers CN11, CN13, CN14 and CN25 found on the conga-QEVAL.
- The conga-QEVAL carrier board is equipped with a Maxim MAX5362 device referred to in the diagram below as “DAC”.
- LPF represent Low Pass Filter (RC circuit) and OPA is Operational Amplifier.



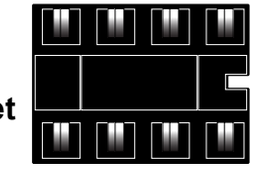
4.2.10.3 Flat Panel Configuration Data

The flat panel configuration data (EPI extended EDID™ 1.3 file) for most common displays is included in the congatec Qseven® CPU module's system BIOS. The customer also has the possibility to use a customized EPI extended EDID™ 1.3 file that can be stored in a serial EEPROM located on the conga-QEVAL (DIL 8 socket CN16).

Note

Supported EEPROMs: 24C02, 24C04 and 24C16 at address A0h.

CN16
EEPROM Socket

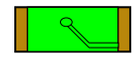


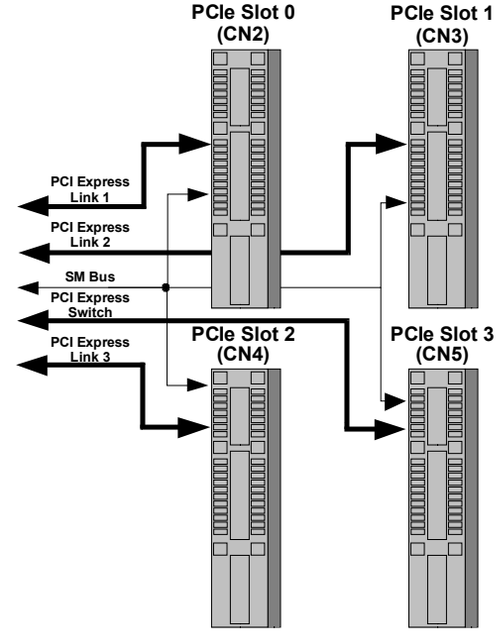
4.2.11 PCI Express x1 Connectors

The Qseven® module is capable of supporting up to 4 x1 PCI Express links. The conga-QEVAL utilizes a PCIe switch (connected to PCI Express Link 0) in order to provide three x1. One link is connected to the PCI Express Mini Card socket and one to the ExpressCard socket. The remaining link is connected to PCI Express Slot 3 (CN5). The table and diagram below describe the routing of the PCI Express links. The table on the following page describes the pinout of each PCI Express slot..

PCIe Link	Originates from	Connected to	Green Status LEDs
0	Qseven® module	PCIe Switch	D5 PCIe link 0 Present
1	Qseven® module	PCIe Slot 0 - CN2	
2	Qseven® module	PCIe Slot 1 - CN3	
3	Qseven® module	PCIe Slot 2 - CN4	
4	PCIe Switch	PCIe Slot 3 - CN5	D6 PCIe link 4 Present
5	PCIe Switch	PCI Express Mini Card - CN6	D7 PCIe link 5 Present
6	PCIe Switch	PCI ExpressCard - CN8	D8 PCIe link 6 Present

D5-D8





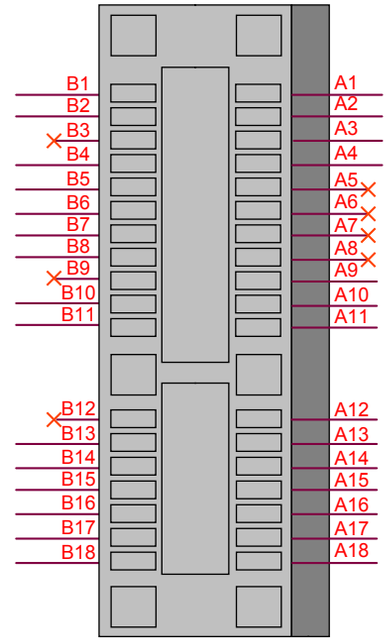
Note

The JTAG Interface is not available on the 4 PCI Express slots 0 to 3.

PCI Express Slot 0/Link 1 Connector CN2				PCI Express Slot 1/Link 2 Connector CN3			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B1	+12V	A1	PRSNT#1_S0	B1	+12V	A1	PRSNT#1_S1
B2	+12V	A2	+12V	B2	+12V	A2	+12V
B3	N.C.	A3	+12V	B3	N.C.	A3	+12V
B4	GND	A4	GND	B4	GND	A4	GND
B5	SMB_CLK	A5	N.C.	B5	SMB_CLK	A5	N.C.
B6	SMB_DAT	A6	N.C.	B6	SMB_DAT	A6	N.C.
B7	GND	A7	N.C.	B7	GND	A7	N.C.
B8	+3.3V	A8	N.C.	B8	+3.3V	A8	N.C.
B9	N.C.	A9	+3.3V	B9	N.C.	A9	+3.3V
B10	+3.3V Standby	A10	+3.3V	B10	+3.3V Standby	A10	+3.3V
B11	WAKE0#	A11	PCIE_RST#	B11	WAKE0#	A11	PCIE_RST#
B12	N.C.	A12	GND	B12	N.C.	A12	GND
B13	GND	A13	PCIE1_CLK+	B13	GND	A13	PCIE2_CLK+
B14	PCIE1_TX+	A14	PCIE1_CLK-	B14	PCIE2_TX+	A14	PCIE2_CLK-
B15	PCIE1_TX-	A15	GND	B15	PCIE2_TX-	A15	GND
B16	GND	A16	PCIE1_RX+	B16	GND	A16	PCIE2_RX+
B17	PRSNT#2_S0	A17	PCIE1_RX-	B17	PRSNT#2_S1	A17	PCIE2_RX-
B18	GND	A18	GND	B18	GND	A18	GND

PCI Express Slot 2/Link 3 Connector CN4				PCI Express Slot 3/Link 4 Connector CN5 (PCIe switch			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B1	+12V	A1	PRSNT#1_S2	B1	+12V	A1	PRSNT#1_S3
B2	+12V	A2	+12V	B2	+12V	A2	+12V
B3	N.C.	A3	+12V	B3	N.C.	A3	+12V
B4	GND	A4	GND	B4	GND	A4	GND
B5	SMB_CLK	A5	N.C.	B5	SMB_CLK	A5	N.C.
B6	SMB_DAT	A6	N.C.	B6	SMB_DAT	A6	N.C.
B7	GND	A7	N.C.	B7	GND	A7	N.C.
B8	+3.3V	A8	N.C.	B8	+3.3V	A8	N.C.
B9	N.C.	A9	+3.3V	B9	N.C.	A9	+3.3V
B10	+3.3V Standby	A10	+3.3V	B10	+3.3V Standby	A10	+3.3V
B11	WAKE0#	A11	PCIE_RST#	B11	WAKE0#	A11	PCIE_RST#
B12	N.C.	A12	GND	B12	N.C.	A12	GND
B13	GND	A13	PCIE3_CLK+	B13	GND	A13	PCIE4_CLK+
B14	PCIE3_TX+	A14	PCIE3_CLK-	B14	PCIE4_TX+	A14	PCIE4_CLK-
B15	PCIE3_TX-	A15	GND	B15	PCIE4_TX-	A15	GND
B16	GND	A16	PCIE3_RX+	B16	GND	A16	PCIE4_RX+
B17	PRSNT#2_S2	A17	PCIE3_RX-	B17	PRSNT#2_S3	A17	PCIE4_RX-
B18	GND	A18	GND	B18	GND	A18	GND

x1 PCI Express Connector



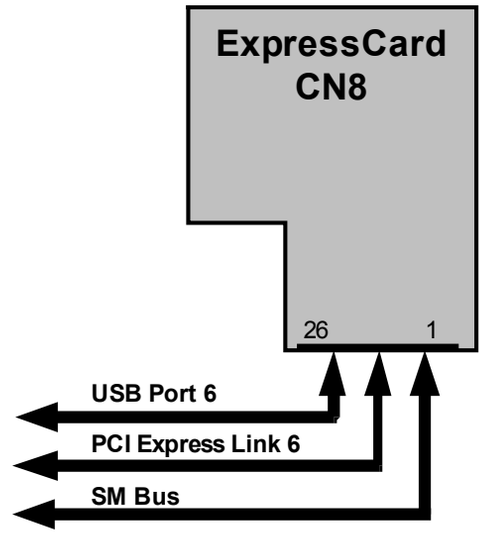
4.2.12 ExpressCard and PCI Express Mini Card

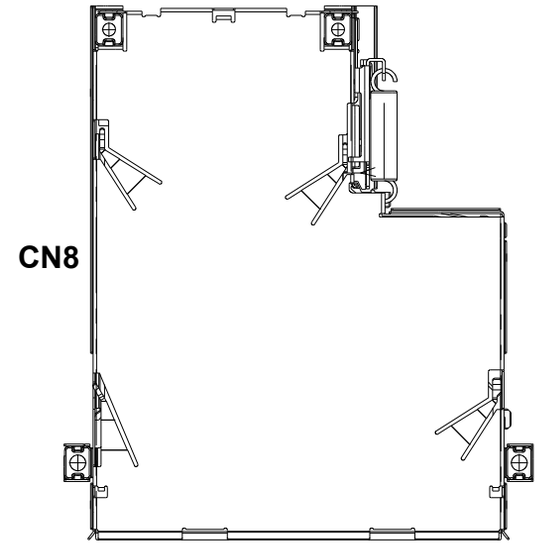
4.2.12.1 ExpressCard

The conga-QEVAL is equipped with a ExpressCard slot (connector CN8). ExpressCard is a small, modular add-in card designed to replace common PCMCIA and PC Cards. It takes advantage of the scalable, high-bandwidth serial PCI Express and USB 2.0 interfaces to provide much higher data rates. More information about the ExpressCard Standard can be found at http://www.expresscard.org.

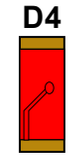
The following table lists the default pinout of the ExpressCard slot. It utilizes USB port 6 and PCI Express link 6.

Pin	Signal	Pin	Signal
1	GND	14	+3.3V
2	USB_P6-	15	+3.3V
3	USB_P6+	16	CLKREQ#
4	CPUSB#	17	EXCD0_CPPE#
5	RSVD	18	PCIE6_CLKC-
6	RSVD	19	PCIE6_CLKC+
7	SMBCLK	20	GND
8	SMBDATA	21	PCIE6_RX-
9	+1.5V	22	PCIE6_RX+
10	+1.5V	23	GND
11	PCIE_WAKE#	24	PCIE6_TX-
12	+3.3V Standby	25	PCIE6_TX+
13	EXCD0_PERST#	26	GND





LED D4 is a red LED that indicates an ‘Overcurrent Event’ has occurred in the ExpressCard slot.



Note

The ExpressCard socket uses USB Port 6. On some Qseven® modules this port is USB 2.0 compliant only, it is not backwards compatible to USB 1.1 and therefore does not support the connection of USB 1.1 devices.

4.2.12.2 PCI Express Mini Card

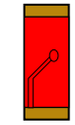
The conga-QEVAL is equipped with a PCI Express Mini Card socket. PCI Express Mini Card is a unique small size form factor optimized for mobile computing platforms equipped with communication applications such as wireless LAN. The small footprint connector can be implemented on carrier board designs providing the ability to insert different removable PCI Express Mini Cards. Using this approach gives the flexibility to mount an upgradable, standardized PCI Express Mini Card device to the carrier board without additional expenditure of a redesign. The PCI Express Mini Card utilizes USB port 7 and PCI Express link 5. The following table lists the default pinout of the PCI Express Mini Card.

Pin	Signal	Pin	Signal
1	PCIE_WAKE#	2	+3.3V
3	N.C.	4	GND
5	N.C.	6	+1.5V
7	CLKREQ#	8	N.C.
9	GND	10	N.C.
11	PCIE5_CLK-	12	N.C.
13	PCIE5_CLK+	14	N.C.
15	GND	16	N.C.
17	N.C.	18	GND
19	N.C.	20	W_DISABLE#
21	GND	22	PCIE_RST#
23	PCIE5_RX-	24	+3.3V Standby
25	PCIE5_RX+	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PCIE5_TX-	32	SMB_DATA
33	PCIE5_TX+	34	GND
35	GND	36	USB_P7-
37	RSVD	38	USB_P7+
39	RSVD	40	GND
41	RSVD	42	LED_WWAN#
43	RSVD	44	LED_WLAN#
45	N.C.	46	LED_WPAN#
47	N.C.	48	+1.5V
49	N.C.	50	GND
51	N.C.	52	+3.3V

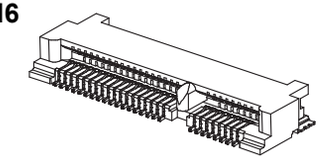
The PCI Mini Card socket has three different red LEDs to indicate the presence of certain area network types. They are as follows:

LED	Indicates
D1	WWAN Wireless Wide Area Network
D2	WLAN Wireless Local Area Network
D3	WPAN Wireless Personal Area Network

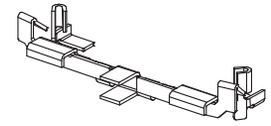
D1-D3



CN6



CN7



Note

The ExpressCard socket uses USB Port 7. This port is USB 2.0 compliant only, it is not backwards compatible to USB 1.1 and therefore does not support the connection of USB 1.1 devices.

Jumper CN58 provides the ability to enable/disable WiFi radio on the PCI Express Mini card.

Jumper CN58	Configuration
1 - 2	WiFi Radio is Enabled (default)
2 - 3	WiFi Radio is Disabled

WiFi Radio Enable/Disable (CN58)

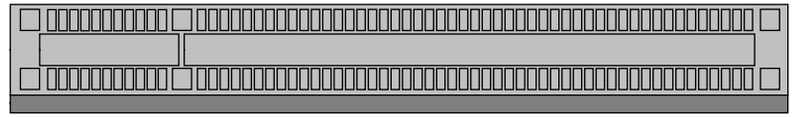
Connector Type

CN58: 3 pin 2.54mm grid jumper.

4.2.13 ADD2 Slot

The ADD2 is available on connector CN10. ADD2 is second generation of Advance Digital Display interface, provides video signaling (such as VGA, DVI, TV outputs) via a PCI Express slot. Video input for ADD2-N card is taken directly from Qseven® module (SDVO signals, see connector CN1). If module provides different video output on these pins (DisplayPort/HDMI/DVI) then the appropriate ADD2 video card has to be used.

(CN10)

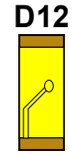


Note

The conga-QEVAL supports ADD2-N cards only in the PEG slot. The conga-QEVAL does not support ADD2-R cards.

4.2.14 SDIO Interface

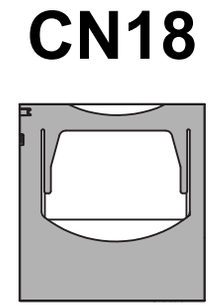
The Qseven® module's SDIO interface is used on the conga-QEVAL to provide a SD/miniSD/MMC/MMC PLUS card socket. Yellow LED D12 indicates activity on the SDIO interface.



4.2.14.1 SD/MMC Card Socket

The conga-QEVAL provides one SD/MMC socket (CN18). The following table lists the pinout of socket CN18.

Pin	Signal	Pin	Signal
1	SDIO_WP	9	+3.3V
2	SDIO_CD	10	GND
3	SDIO Data Line 1	11	SDIO Data Line 5
4	SDIO Data Line 0	12	SDIO_CMD
5	SDIO Data Line 7	13	SDIO Data Line 4
6	GND	14	SDIO Data Line 3
7	SDIO Data Line 6	15	SDIO Data Line 2
8	SDIO CLK		



4.2.15 CAN Bus

The conga-QEVAL provides a Controller Area Network bus interface via a 5 pin header (CN70). CAN bus originates from Qseven® module and the bus is connected to CN70 through CAN transceiver SN65HVD232. Jumper CN62 enables or disables CAN bus termination.

Pin	Signal
1	+12V
2	CAN Low
3	GND
4	CAN High
5	N.C.

CAN (CN70)

Jumper CN62	Configuration
1 - 2	CAN termination Enabled
2 - 3	CAN termination Disabled (default)

CAN Termination (CN62)

Connector Type

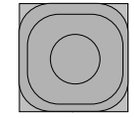
CN70: 5 pin 2.54mm grid female, CN62: 2.54mm grid jumper.

5 Additional Features

5.1 Power Button

The Qseven® module will perform a power up sequence when this button is pressed. The power button is connected to the Qseven® module's PWRBTN# signal.

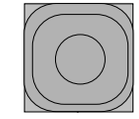
Pwr On (SW1)



5.2 Sleep Button

The Qseven® module will enter a sleep state when this button is pressed. The sleep button is connected to the Qseven® module's SLP_BTN# signal.

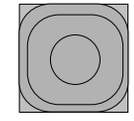
Sleep (SW2)



5.3 Reset Button

The Qseven® module and all connected components will perform a hard reset when this button is pressed. The reset button is connected to the Qseven® module's RSTBTN# signal.

LID (SW4)

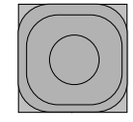


5.4 LID Button

Pressing the LID button creates a low active signal used by the ACPI operating system to detect a LID switch and to bring the system into either a sleep state or to wake it up again. The LID button is connected to the Qseven® module's LID_BTN# signal.

External LID switch can be connected to connector CN61.

Reset (SW3)



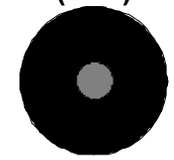
Connector Type

CN61: 2 pin 2.54mm grid female.

LID (CN61)

5.5 PC Speaker

Speaker (U23)

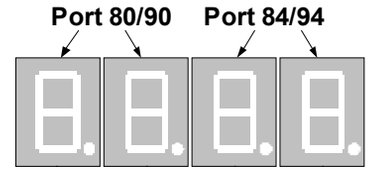


The board-mounted speaker provides audible error code (beep code) information during POST. The speaker is connected to the Qseven® module's SPEAKER signal.

5.6 Debug Display

During the POST (Power On Self Test), the BIOS generates diagnostic progress codes (POST-codes) to different I/O ports (usually port 80h). If the POST fails, execution stops and the last POST code generated is left at the respective port. This code is useful for determining the point where an error occurred.

The conga-QEVAL decodes these ports and displays their contents on 4 seven-segment displays (D24 to D27).



A list of the POST codes and associated POST test and initialization routines for the BIOS used on congatec Qseven® modules is available at: http://www.congatec.com.

Jumper CN32	Configuration
1 - 2	Port 80h and port 84h output (default)
3 - 4	Port 90h and port 94h output

Debug Display Config (CN32)

Connector Type

CN32 4 pin 2 row 2.54mm grid jumper.

5.7 Internal Use Only Connectors

Connectors CN9, CN33, CN45, CN46, CN56 and CN57 are designated for internal use only and therefore are not available.

Connector Type

CN33 7 pin 2.54mm grid jumper.

CN9, CN45 10 pin 2 row 2.54mm grid jumpers.

CN46 , CN56, CN57 2 pin 2 row 2.54mm grid jumpers.

5.8 Ground Probes

The conga-QEVAL provides 4 ground probes (CN51 to CN54) that are connected to Ground Potential. These test points make it easier to connect oscilloscope probes and/or multimeter lines to GND when performing measurements on the Qseven® module.

Ground Probe
CN51-CN54

5.9 Fan Connector and Power Configuration

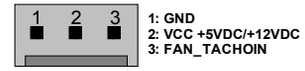
The conga-QEVAL provides the ability to connect 5V or 12V cooling fans for the CPU module and system. Connector CN37 is for the CPU module's fan and connector CN42 is for the system's fan. The following tables describe the pinouts and jumper configuration possibilities.

CN37 CPU FAN Pin	Signal
1	GND
2	VCC +5VDC/+12VDC
3	FAN_TACHOIN
4	FAN_CTRL

CN42 SYS FAN Pin	Signal
1	GND
2	VCC +5VDC/+12VDC
3	FAN_TACHOIN

CPU Fan (CN37)

SYS Fan (CN42)



Connector Type

CN37: 4 pin 2.54mm grid female fan connector, CN42: 3 pin 2.54mm grid female fan connector.

Note

The FAN_TACHOIN signal, that originates from the Qseven® module and is connected to pin 3 on connector CN37 and CN42 of the conga-QEVAL, must receive two pulses per revolution in order to produce an accurate reading and therefore a two pulse per revolution fan is recommended.

VCC on CN42 is controlled by the Fan PWM control signal, which originates from the Qseven® module.

Jumper CN36	Configuration
1 - 2	4pin FAN +12VDC (default)
2 - 3	4pin FAN +5VDC

Jumper CN40	Configuration
1 - 2	3pin FAN +12VDC (default)
2 - 3	3pin FAN +5VDC

Jumper CN49	Configuration
1 - 2	3pin FAN w/o control (default)
2 - 3	3pin FAN with control

CN36
CN40
CN49

Connector Type

CN36, CN40 and CN49: 2.54mm grid jumper.

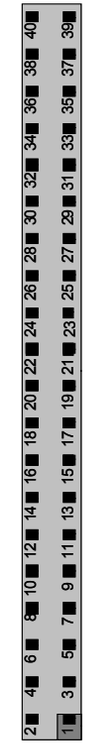
Note

The FAN_TACHOIN signal, that originates from the Qseven® module and is connected to pin 3 on connector CN37 and CN42 of the conga-QEVAL, must receive two pulses per revolution in order to produce an accurate reading and therefore a two pulse per revolution fan is recommended.

5.10 Feature Connector

Pin	Signal	Description	Pin	Signal	Description
1	+5V (750 mA fuse)		2	5V_SB (750 mA fuse)	
3	HDD LED		4	Hard Disk Activity	Shows activity on hard disk interface
5	I2C_DAT	General purpose I²C port data I/O line.	6	SMB_CLK	System Management Bus bidirectional clock line.
7	I2C_CLK	General purpose I²C port clock output.	8	SMB_DAT	System Management Bus bidirectional data line.
9	N.C.		10	N.C.	
11	N.C.		12	N.C.	
13	PS_ON#	Power Supply On (active low).	14	N.C.	
15	SUS_S3#	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	16	N.C.	
17	GND	Power Ground	18	GND	Power Ground
19	THRMTRIP#	Active low output indicating that the CPU has entered thermal shutdown.	20	SMB_ALERT#	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.
21	N.C.		22	N.C.	
23	SUS_STAT#	Suspend Status: indicates that the system will be entering a low power state soon.	24	N.C.	
25	N.C.		26	SUS_S5#	S5 State: This signal indicates S4 or S5 (Soft Off) state.
27	WDTRIG#		28	THRM#	Input from off-module temp sensor indicating an over-temp situation.
29	N.C.		30	N.C.	
31	BATLOW#	Indicates that external battery is low.	32	WAKE#	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.
33	N.C.		34	N.C.	
35	N.C.		36	RSTBTN#	Reset Button Input. Active low input. This input may be driven active low by an external circuitry to reset the Qseven® module.
37	GND	Power Ground	38	GND	Power Ground
39	PWBTN#	Power Button: Low active power button input. This signal is triggered on the falling edge.	40	PWGIN	High active input for the Qseven® module indicates that power from the power supply is ready.

Feature (CN35)



Connector Type

40 pin, 2 row 2.54mm grid female.

5.11 External System Wake Event

The external system wake event (WAKE#) signal can be found on the feature connector CN35. If the Qseven® module does not support the WAKE# signal then CN63 can be jumpered to connect the Qseven® module's PCIE_WAKE# to WAKE#.

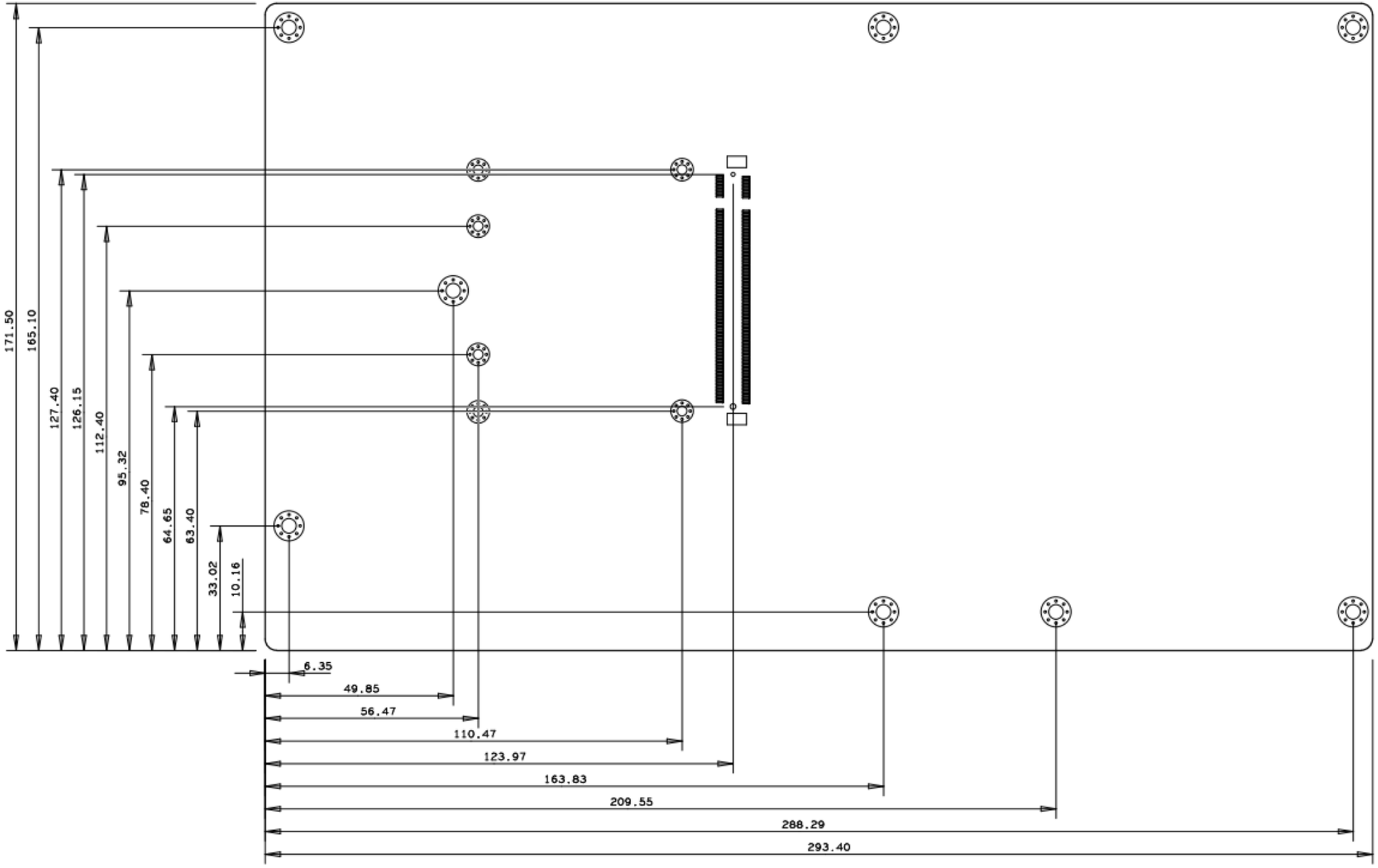
Pin	Signal
1	WAKE#
2	PCIE_WAKE#

CN63

Connector Type

CN63: 2.54mm grid jumper.

6 conga-QEVAL Mechanical Drawing



7 Industry Specifications

The list below provides links to industry specifications that should be used as reference material when designing a Qseven® carrier board.

Specification	Link
Qseven® Specification	http://www.qseven-standard.org/
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
ExpressCard Standard Release 1.0	http://www.expresscard.org/
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
MMC Multimedia Card Association	http://www.mmca.org
SD Card Association	http://www.sdcard.org
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
High Definition Audio Specification, Rev. 1.0	http://www.intel.com/standards/hdaudio/
LVDS Owner's Manual	http://www.national.com
Extended Display Identification Data Standard Version 1.3 (EDID™)	http://www.vesa.org
Enhanced Display Data Channel Specification Version 1.1 (DDC)	http://www.vesa.org
IEEE standard 802.3ab 1000BASE T Ethernet	http://www.ieee.org/portal/site
Advanced Configuration and Power Interface Specification Rev. 3.0a	http://www.acpi.info/