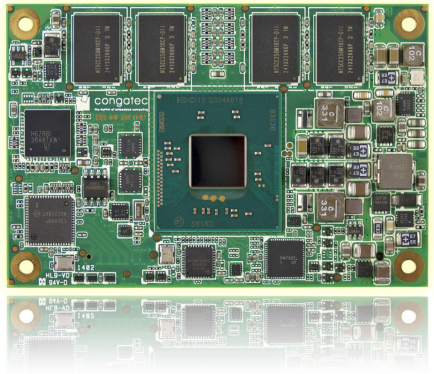
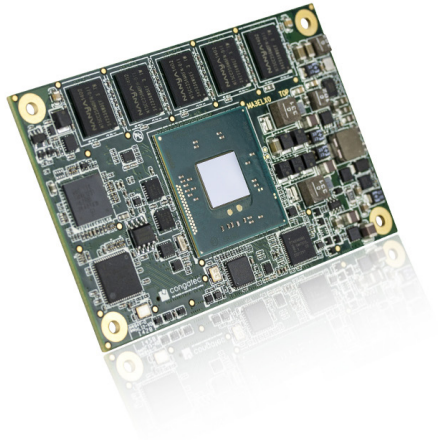


COM Express™ conga-MA3/MA3E

COM Express Type 10 Mini Module Based On 3rd Generation Intel® Atom™ and Intel® Celeron® Soc



User's Guide

Revision 1.5

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2014.07.02	AEM	• Preliminary release
0.2	2014.08.08	AEM	• Added UART interface to section 2.1 "Feature List". Updated section 2.4.1 and added section 2.4.2 "Rise time" • Updated section 5.1.7 "Digital Display Interface" with LVDS single channel resolution. • Added note about eMMC and SD drivers in sections 5.1.9 "SD Card" and 6.1.1 "eMMC 4.5" • Added section 5.1.10 "General Purpose Serial Interface (UART)"
1.0	2015.08.21	AEM	• Added additional variant (PN: 047007) to table 2 "Options Information Table" • Added additional note to section 2.2 "Supported Operating Systems" • Updated section 2.5 "Power Consumption" • Updated section 3 "Block Diagram" • Deleted the note in table 5 "Gigabit Ethernet Signal Descriptions" about the GBE0_LINK# not being active during a 10Mbit connection because the Intel Atom/Celeron SoCs on the conga-MA3/MA3E do not have this limitation • Updated section 6.5 "ECC Memory Support" • Added note about the configuration of fan_pwm pin as push-pull in section 6.1.2.4 “Fan Control” and table 18 “Miscellaneous Signal Description” • Official release
1.1	2015.09.11	AEM	• Updated conga-MA3 and conga-MA3E variants in conga-MA3/conga-MA3E Options Information sections • Updated section 2.1 "Feature List" • Updated section 2.5 "Power Consumption" • Added RTC power consumption values, measured at temperatures -10°C, 20°C and 70°C in section 2.6.1 • Updated section 3 "Block Diagram", section 5 "Connector Subsystems Rows A, B" and section 6 "Additional Features" • Added note about signals that should be routed as short as possible to several sections
1.2	2017.06.21	BEU	• Added note about UART limitations in section 5.1.10 "General Purpose Serial Interface (UART)" • Updated section 2.5 "Power Consumption" • Changed note in 6.1.2.4 "Fan Control" • Updated section 10 "BIOS Setup Description" • Updated section 11 "Additional BIOS Features"
1.3	2020.08.06	BEU	• Updated information about handling electrostatic sensitive devices in the preface section • Added power consumption values for PN: 047407 to table 6 • Removed maximum supported capacity of optional eMMC from section 2.1 "Feature List" and 6.1.1 "eMMC 4.5" • Updated section 4 "Cooling Solutions" • Updated reference to power supply design guide in section 5.1.14 "Power Control" • Added note about pulse width to several signals in table 26 • Corrected SDIO_WP pin number in table 30 "SDIO Signal Descriptions" • Added section 11.2 "Supported Flash Devices" • Removed section 12 "Industry Specifications"
1.4	2021.02.19	BEU	• Corrected the storage temperature for industrial variants in section 2.7 "Environmental Specifications"
1.5	2021.04.15	BEU	• Updated display interfaces in table 1, 2, 3, 4, 5, 20, 22 and section 3 "Block Diagam", 5 "Connector Subsystems Rows A, B", 5.1.7 "Digital Display Interface", 5.1.7.1 "DisplayPort (DP)" • Removed sections 5.1.7.1 "HDMI", 5.1.7.2 "DVI", 12 "Industry Specifications"

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-MA3/MA3E. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents are COM Express™ Design Guide and COM Express™ Specification.

The links to these documents can be found on the congatec AG website at www.congatec.com

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The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
DDC	Display Data Channel
SoC	System On Chip
LVDS	Low-Voltage Differential Signaling
Gbe	Gigabit Ethernet
eMMC	Embedded Multi-media Controller
MLC	Multi-level Cell
SLC	Single-level Cell
HDA	High Definition Audio
cBC	congatec Board Controller
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

Contents

List of Tables

1 Introduction

COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express™ modules are available in following form factors:

- Mini 84mm x 55mm
- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x110mm

The COM Express™ specification 2.0 defines seven different pinout types.

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports
Type 1	A-B	Up to 6			1
Type 2	A-B C-D	Up to 22	32 bit	1	1
Type 3	A-B C-D	Up to 22	32 bit		3
Type 4	A-B C-D	Up to 32		1	1
Type 5	A-B C-D	Up to 32			3
Type 6	A-B C-D	Up to 24			1
Type 10	A-B	Up to 4			1

conga-MA3/MA3E modules use the Type 10 pinout definition. They are equipped with single 220-pin high performance connector that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 10 pinout provides the ability to offer PCI Express, Serial ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

conga-MA3 Options Information

The conga-MA3 is available in eleven variants (six commercial and five industrial variants). The tables below show the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Table 1 conga-MA3 Commercial Variants

Part-No.	047400	047401	047402	047404	047406	047407
Processor	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3827 (Dual Core, 1.75 GHz)	Intel® Atom™ E3826 (Dual Core, 1.46 GHz)	Intel® Atom™ E3815 (Single Core, 1.46 GHz)	Intel® Celeron® N2930 (Quad Core,1.83/2.16 GHz)	Intel® Celeron® N2807 (Dual Core,1.58/2.16 GHz)
L2 Cache	2 MB	1 MB	1 MB	512 kB	2 MB	1 MB
Onboard Memory	4GB DDR3L-1333 dual channel	2GB DDR3L-1333 dual channel	2GB DDR3L-1066 dual channel	2GB DDR3L-1066 single channel	2GB DDR3L-1333 dual channel	2GB DDR3L-1333 single channel
ECC Memory Support	No	No	No	No	No	No
Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics
GFX Base/Burst	542 / 792	542 / 792	533 / 667	400 / 400	313 / 854	313 / 750
LVDS	Single 18 or 24 bpp	Single 18 or 24 bpp	Single 18 or 24 bpp	Single 18 or 24 bpp	Single 18 or 24 bpp	Single 18 or 24 bpp
DDI	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)
eMMC (SLC/MLC)	8 GB (MLC)	4 GB (MLC)	4 GB (MLC)	N/A	N/A	N/A
SD Card	Yes	Yes	Yes	Yes	Yes	Yes
Max. TDP / SDP	10 W / N/A	8 W / N/A	7 W / N/A	5 W / N/A	7.5 W / 4.5 W	4.3 W / 2.5 W

Table 2 conga-MA3 Industrial Variants

Part-No.	047410	047411	047413	047414	047415
Processor	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3827 (Dual Core, 1.75 GHz)	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3815 (Single Core, 1.46 GHz)	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)
L2 Cache	2 MB	1 MB	2 MB	512kB	2 MB
Onboard Memory	4GB DDR3L-1333 dual channel	2GB DDR3L-1333 dual channel	2GB DDR3L-1333 dual channel	2GB DDR3L-1066 single channel	4GB DDR3L-1333 dual channel
ECC Memory Support	No	No	No	No	No
Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics	Intel® HD Graphics
GFX Base/Burst	542 / 792	542 / 792	542 / 792	400 / 400	542 / 792
LVDS	Single 18 or 24 bpp	Single 18 or 24 bpp	Single 18 or 24 bpp	Single 18 or 24 bpp	Single 18 or 24 bpp
DDI	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)	DP++ (DP/HDMI™/DVI)
eMMC (SLC/MLC)	8 GB (MLC)	4 GB (MLC)	4 GB (MLC)	N/A	2 GB (SLC)
SD Card	Yes	Yes	Yes	Yes	Yes
Max. TDP / SDP	10 W / N/A	8 W / N/A	10 W / N/A	5 W / N/A	10 W / N.A

conga-MA3E Options Information

The conga-MA3E is available in three variants (one commercial and two industrial). The table below shows the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Table 3 conga-MA3E Commercial Variants

Part-No.	048400
Processor	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)
L2 Cache	2 MB
Onboard Memory	4GB DDR3L-1333 single channel
ECC Memory Support	Yes
Graphics	Intel® HD Graphics
GFX Base/Burst	542 / 792
LVDS	Single 18 or 24 bpp
DDI	DisplayPort 1.1
eMMC (SLC/MLC)	8 GB (MLC)
SD Card	Yes
Max. TDP / SDP	10 W / N/A

Table 4 conga-MA3E Industrial Variants

Part-No.	048410	048411
Processor	Intel® Atom™ E3845 (Quad Core, 1.91 GHz)	Intel® Atom™ E3827 (Dual Core, 1.75 GHz)
L2 Cache	2 MB	1 MB
Onboard Memory	4GB DDR3L-1333 single channel	2GB DDR3L-1333 single channel
ECC Memory Support	Yes	Yes
Graphics	Intel® HD Graphics	Intel® HD Graphics
GFX Base/Burst	542 / 792	542 / 792
LVDS	Single 18 or 24 bpp	Single 18 or 24 bpp
DDI	DisplayPort 1.1	DisplayPort 1.1
eMMC (SLC/MLC)	8 GB (MLC)	4 GB (MLC)
SD Card	Yes	Yes
Max. TDP / SDP	10 W / N/A	8 W / N/A

2 Specifications

2.1 Feature List

Table 5 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 10 Rev. 2.1 (mini size 84 x 55 mm)	
Processor	Intel® Atom™ E3845 /E3827 / E3826 / E3815 Intel® Celeron N2930 / N2807	
Memory	**conga-MA3:** Up to 4 GB single channel or up to 8 GB dual channel non-ECC DDR3L onboard memory interface with data rates up to 1333 MT/s. Variants equipped with Intel Atom E3815 or Intel Celeron N2807 feature single channel memory interface. For more information, see Options Information tables on page 11. **conga-MA3E:** Single channel ECC DDR3L onboard memory interface with up to 8 GB and data rates of 1333 MT/s. For more information, see conga-MA3E Options Information table on page 12.	
Chipset	Integrated in SoC	
Onboard Storage	eMMC 4.5 onboard flash with optional storage capacity (assembly option)	
Audio	High Definition Audio (HDA)/digital audio interface with support for multiple codecs.	
Ethernet	Gigabit Ethernet via the onboard Intel® I210 Gigabit Ethernet controller.	
Graphics Options	Intel® HD Graphics Gen. 7, full hardware acceleration for MPEG2, H.264, DirectX11, OCL 1.2, OGL 3.2, WMV9 and VC1. Dual simultaneous display support	
	1x DDI1 supports the following via eDP to LVDS bridge IC: - Single-channel LVDS interface: 1 x 18 bpp or 1 x 24 bpp. - VESA LVDS color mappings - Automatic Panel Detection via Embedded Panel Interface based on VESA EDID™ 1.3. - Resolution up to 1400x1050 @ 60 Hz in single channel LVDS mode. Optional eDP interface (assembly option) **NOTE**: Either eDP or LVDS signals supported, not both signal types simultaneously	1x DDI0 with support for DP++ (DP/HDMI™/DVI) **NOTE**: The conga-MA3/MA3E does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.
Peripheral Interfaces	2x Serial ATA® up to 3Gb/s Up to 4x PCI Express® Gen2 links with up to 5.0 GT/s per lane 6x USB 2.0 1x USB 3.0 1x SD/MMC	2x UART GPIOs muxed with SD card SPI Bus LPC Bus I²C Bus, multimaster
BIOS	AMI Aptio® UEFI 2.x firmware; 8 MByte serial SPI with congatec Embedded BIOS features (OEM Logo, OEM CMOS Defaults, LCD Control, Display Auto Detection, Backlight Control, Flash Update)	
Power Mgmt.	ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).	
congatec Board Controller	Multi Stage Watchdog, non-volatile User Data Storage, Manufacturing and Board Information, Board Statistics, BIOS Setup Data Backup, I²C bus (fast mode, 400 kHz, multi-master), Power Loss Control	

Note

Some of the features mentioned in the above Feature Summary are optional and requires customized article. Check the part number of your module and compare it to the option information list on page 11 to determine what options are available on your particular module. For more information, contact congatec support.

2.2 Supported Operating Systems

The conga-MA3/MA3E supports the following operating systems

- Microsoft® Windows® 7
- Microsoft® Windows® 8
- Microsoft® Windows® Embedded Standard 7
- Microsoft® Windows® Embedded Standard 8
- Microsoft® Windows® Embedded Compact 7
- Linus (Timesys Fedora 18)

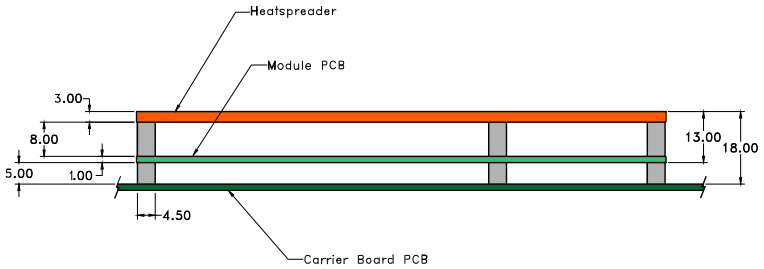
Note

The eMMC and SD drivers for Win7/WES7 are currently not provided by Intel.

For the installation of Windows 7/8 and WES7/8, congatec AG requires a minimum storage capacity of 16 GB. congatec will not offer installation support for systems with less than 16 GB storage space.

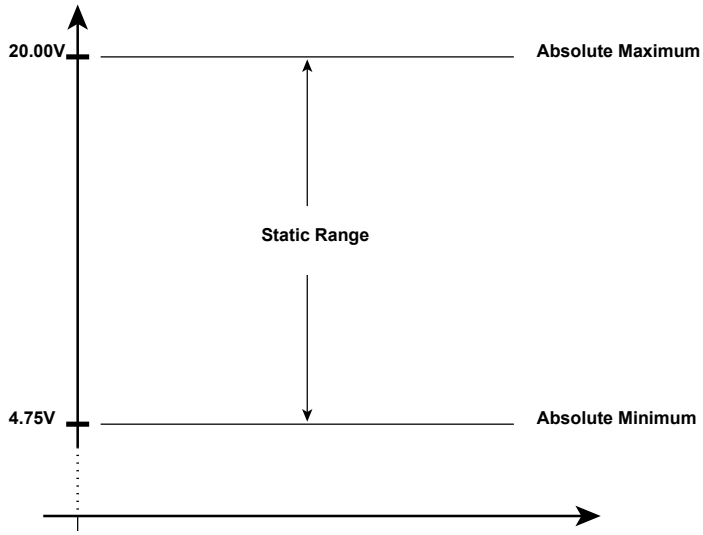
2.3 Mechanical Dimensions

- 84.0 mm x 55.0 mm
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm



2.4 Supply Voltage Standard Power

- 4.75V - 20V (Wide input range)



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 10 (single connector, 220 pins).

Power Rail	Module Pin Current Capability (A)	Nominal Input (V)	Input Range (V)	Derated Input (V)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (W)	Assumed Conversion Efficiency	Max. Load Power (W)
Wide Input	6		4.75-20.0	4.75	+/- 100	28	85%	23.8
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 95% of nominal within 0.1 ms to 20 ms (0.1 ms ≤ Rise Time ≤ 20 ms). Each DC input voltage must rise from 10% to 90% of its nominal voltage in a smooth, continous ramp and the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-MA3/MA3E COM
- modified congatec carrier board
- conga-MA3/MA3E cooling solution
- Microsoft Windows 7 (64 bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle.	The CPU was stressed to its maximum frequency.
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency.
S0: Peak value	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.
S3	COM is powered by VCC_5V_SBY.	
S5	COM is powered by VCC_5V_SBY.	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

The tables below provide additional information about the power consumption data for each of the conga-MA3/MA3E variants offered. The values are recorded at various operating modes.

Table 6 Power Consumption Values

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (A) at 12V (S0) or 5V (S3)			
					Variant	Cores	Freq / Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S3
047400 047413 047410 047415 048400 048410	2 GB or 4 GB	X.0	MA32R010	Windows 7	Intel® Atom™ E3845	4	1.91 GHz	0.30	0.98	1.15	0.08
047401 047411 048411	2 GB	X.0	MA31R0xx	Windows 7	Intel® Atom™ E3827	2	1.75 GHz	0.29	0.79	0.90	0.08
047402	2 GB	X.0	MA31R0xx	Windows 7	Intel® Atom™ E3826	2	1.46 GHz	0.29	0.67	0.71	0.08
047404 047414	2 GB	X.0	MA32R010	Windows 7	Intel® Atom™ E3815	1	1.46 GHz	0.21	0.38	0.40	0.08
047406	2 GB	X.1	MA32R010	Windows 7	Intel® Celeron® N2930	4	1.83 GHz / 2.16 GHz	0.33	1.02	1.25	0.08
047407	2 GB	B.1	MC31R128	Windows 7	Intel® Celeron® N2807	2	1.58 GHz / 2.16 GHz	0.22	0.54	0.67	0.05

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 7 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	1.30 µA
20°C	3V DC	1.57 µA
70°C	3V DC	2.57 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider also the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec AG website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the* conga-MA3/MA3E.

2.7 Environmental Specifications

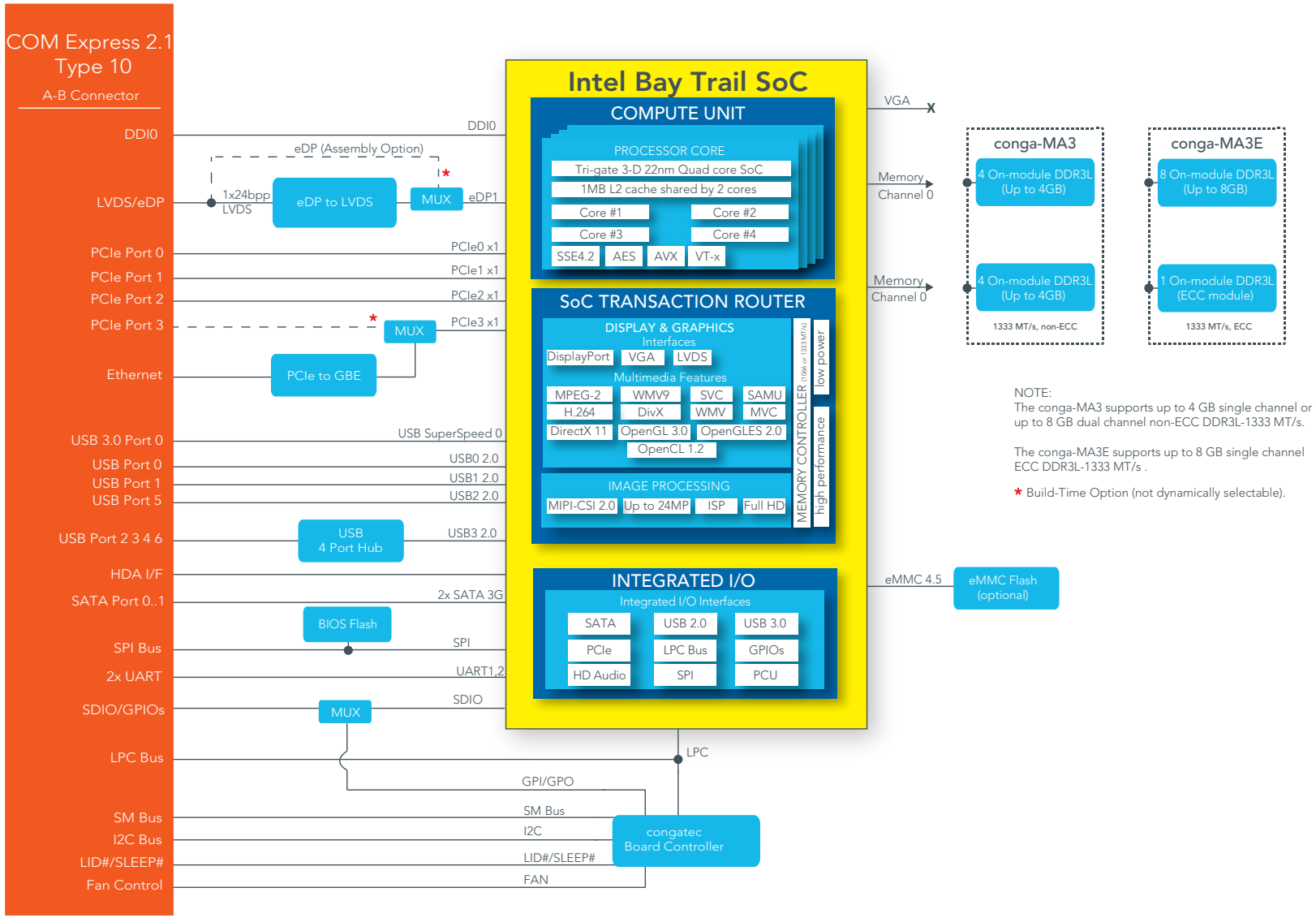
Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to +85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



NOTE:
The conga-MA3 supports up to 4 GB single channel or up to 8 GB dual channel non-ECC DDR3L-1333 MT/s.

The conga-MA3E supports up to 8 GB single channel ECC DDR3L-1333 MT/s .

* Build-Time Option (not dynamically selectable).

4 Cooling Solutions

congatec AG offers the following cooling solutions for conga-MA3/MA3E. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 8 Cooling Solution Variants

Cooling Solution	Part No	Description
HSP	047450	Standard heatspreader for COM Express Type 10 modules conga-MA3 and MA3E. All standoffs are M2.5 thread.
	047451	Standard heatspreader for COM Express Type 10 modules conga-MA3 and MA3E. All standoffs are 2.7mm bore hole.
CSP	047452	Standard passive cooling solution for COM Express Type 10 modules conga-MA3 and MA3E with fins. All standoffs are M2.5mm thread.
	047453	Standard passive cooling solution for COM Express Type 10 modules conga-MA3 and MA3E with fins. All standoffs are 2.7mm bore hole.

Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*

2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

Caution

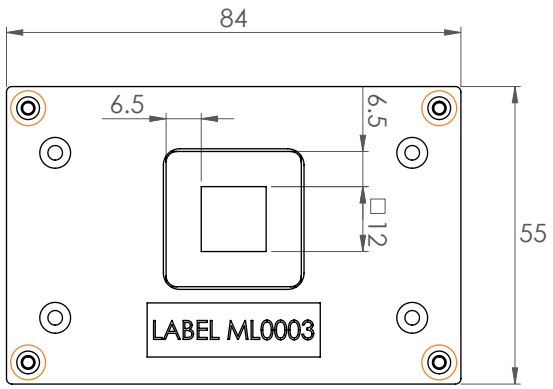
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

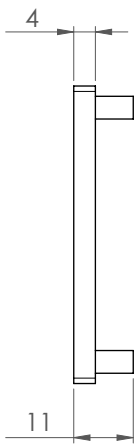
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

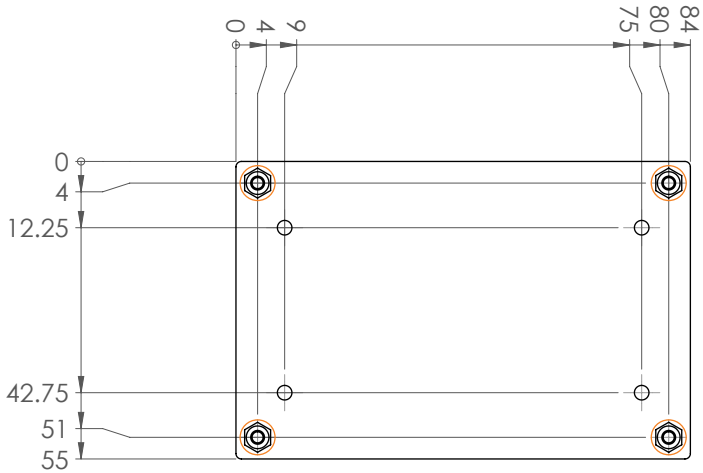
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

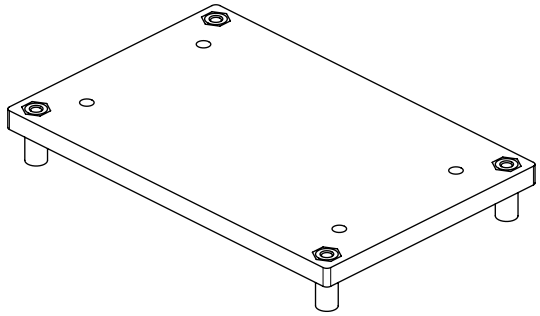
4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

4.1 Heatspreader Dimensions

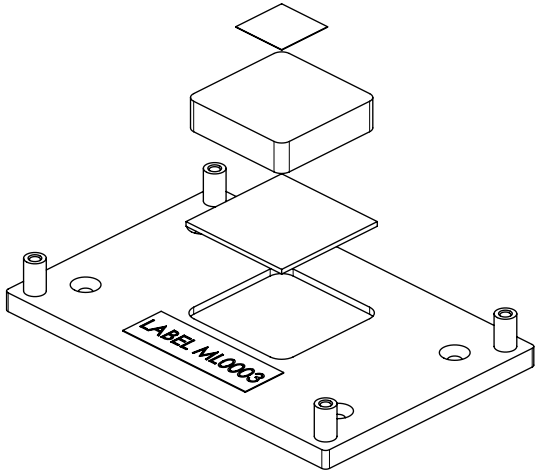




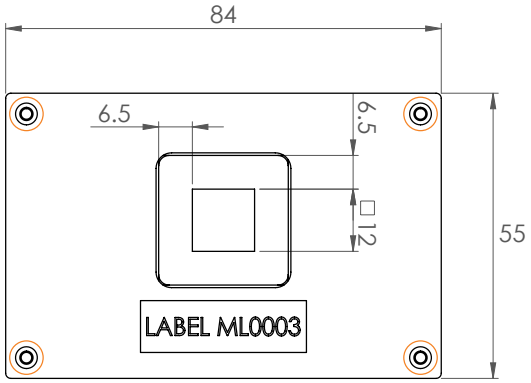


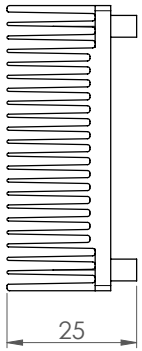


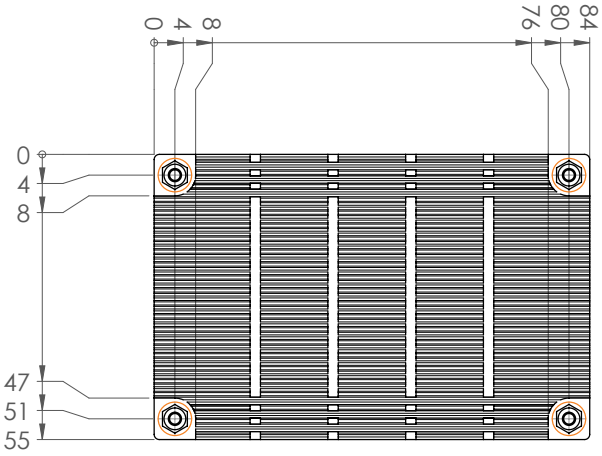
M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version

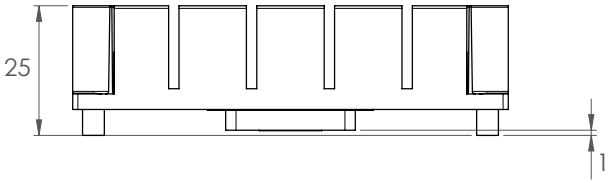


4.2 CSP Dimensions

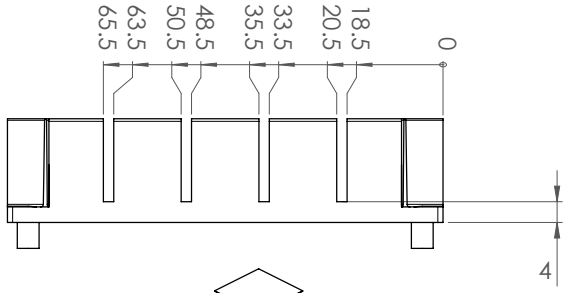


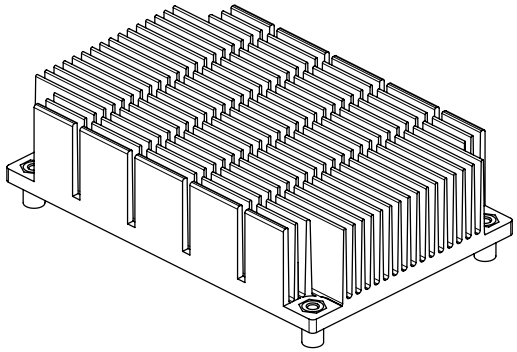


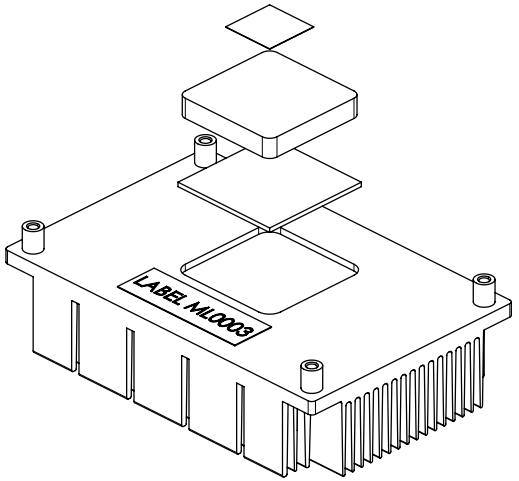




M2.5 x 8 mm
threaded standoff
for threaded version
or
ø2.7 x 10 mm
non-threaded standoff
for borehole version

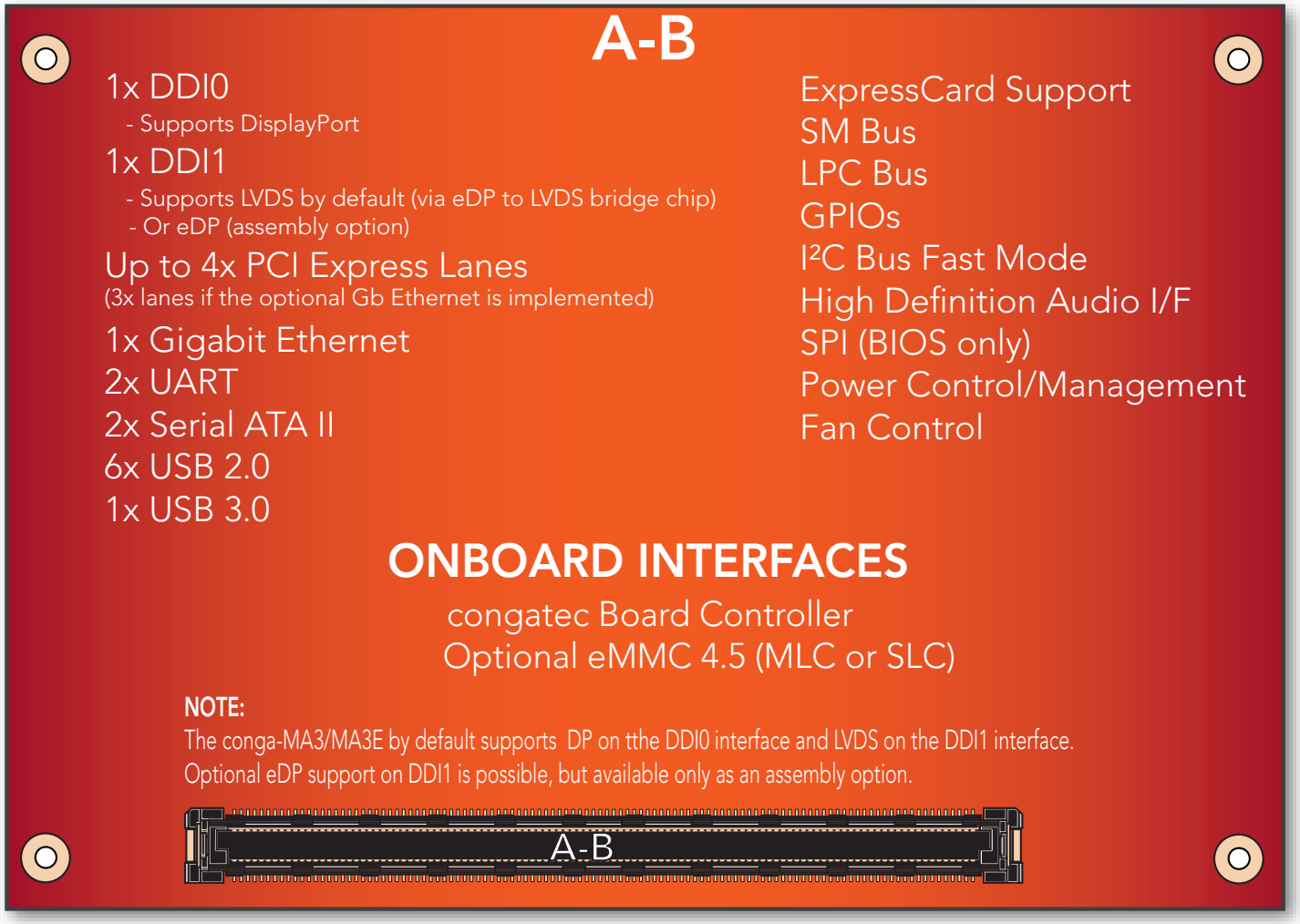






5 Connector Subsystems Rows A, B

The conga-MA3/MA3E is connected to the carrier board via a 220-pin connector (COM Express Type 10 pinout). This connector is broken down into two rows (rows A and B).



top view

5.1 Connector Rows A and B

The following subsystems can be found on conga-MA3/MA3E COM Express connector rows A and B.

5.1.1 PCI Express™

The conga-MA3/MA3E by default offers up to 3 PCI Express externally on the connector (PCIe 0-2). It can also offer up to 4 PCI Express on the connector if the fourth PCI express lane (PCIe 3) is not used for Gigabit Ethernet controller. This option is only available as an assembly option.

The default configuration for the lanes on the COM Express connector is 3 x1. A 1 x2 + 1 x1 configuration is also possible but requires special/customized BIOS. The configuration for the assembly option (4 PCI Express lanes) is 4 x1. A 2 x2, 1 x4 or 1 x2 + 2 x1 configuration is also possible but requires special/customized BIOS.

The PCI Express interface is based on the PCI Express Specification 2.0 with Gen 1 (2.5Gb/s) and Gen 2 (5 Gb/s) speed. For more information refer to the conga-MA3 pinout table in section 8 “Signal Descriptions and Pinout Tables” and table 14 "PCI Express Signal Descriptions".

5.1.2 Gigabit Ethernet

The conga-MA3/MA3E offers a Gigabit Ethernet interface on the COM Express connector via the onboard Intel® I210 Gigabit Ethernet controller. This controller is connected to the Intel® Bay Trail SoC through the fourth PCI Express lane.

The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

5.1.3 Serial ATA™ (SATA)

The conga-MA3/MA3E offers two SATA interfaces on the COM Express connector via a SATA host controller integrated in the Intel® Bay Trail SoC. The controller supports independent DMA operation and data transfer rates of 1.5 Gb/s and 3.0 Gb/s. It also supports two modes of operation - a legacy mode and AHCI mode. Software that uses legacy mode will not have AHCI capabilities.

For more information, refer to section 10 “BIOS Setup Description”.

5.1.4 Universal Serial Bus

The conga-MA3/MA3E offers 7 USB ports (one USB 3.0 and six USB 2.0). Three of these ports (USB 0, USB1, & USB5) are routed directly from the SoC to the COM Express connector. The other four (USB2, USB3, USB4, & USB6) are routed to the connector via a 4-port USB hub.

5.1.4.1 USB 2.0

The conga-MA3/MA3E offers 6 USB 2.0 interfaces on the COM Express connector. The EHCI host controller in the SoC supports these interfaces with high-speed, full-speed and low-speed USB signalling. The controller complies with USB standard 1.1 and 2.0. For more information about how the USB host controllers are routed, see section 7.3 "USB Port Mapping".

Note

Only USB 2.0 port 1 can be used as a debug port.

5.1.4.2 USB 3.0

The conga-MA3/MA3E offers one set of USB 3.0 Super Speed (SS) signals on the COM Express connector. These SS signals can be used with USB0, USB1 or USB5 to create a USB 3.0 port.

The USB 3.0 port is controlled by an xHCI host controller in the SoC. The host controller allows data transfers of up to 5 Gb/s and supports SuperSpeed, high-speed, full-speed and low-speed USB signalling. See section 7.3 for more information about USB port mapping.

Note

BIOS defaults the Super Speed signals to USB0. Custom BIOS is needed to connect the Super Speed signals to USB1 or USB5.

5.1.5 ExpressCard™

The conga-MA3/MA3E supports the implementation of ExpressCards, which requires the dedication of one USB port and a x1 PCI Express link for each ExpressCard used.

5.1.6 High Definition Audio (HDA) Interface

The conga-MA3/MA3E provides an interface that supports the connection of HDA audio codecs.

5.1.7 Digital Display Interface

The conga-MA3/MA3E offers two Digital Display Interfaces (DDI0 & DDI1) on the COM Express connector:

- DDI0 supports DisplayPort 1.1
- DDI1 supports LVDS by default.

Optionally, DDI1 can support eDP instead (assembly option).

The supported display combinations are shown below:

Table 9 Display Combination

Display 1	Display 2	Display 1 Max. Resolution	Display 2 Max. Resolution
DDI0 (DP++)	DDI1 (LVDS/eDP)	2560x1600 @60Hz (DP)	1400x1050 @60Hz (single channel LVDS)
DDI1 (LVDS/eDP)	DDI0 (DP++)	1400x1050 @60Hz (single channel LVDS)	2560x1600 @60Hz (DP)

5.1.7.1 DisplayPort (DP)

DisplayPort (DP) is an open, industry standard digital display interface, that has been developed within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

5.1.7.2 LVDS

The conga-MA3/MA3E offers a 24bpp single channel LVDS interface on the COM Express connector. The interface is provided by routing the onboard PTN3460 to the SoC's second Digital Display Interface (DDI1).

The PTN3460 processes incoming DisplayPort stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format. It supports the single channel signalling on the conga-MA3/MA3E with color depths of 18 bits or 24 bits per pixel and pixel clock frequency up to 112 MHz.

5.1.8 SD Card

The conga-MA3/MA3E offers a 4-bit SD interface for SD/MMC cards on the COM Express connector. The SD signals are multiplexed with GPIO signals and controlled by the congatec board controller. The SD card controller in the Storage Control Cluster of the SoC supports the SD interface with up to 832 Mb/s data rate using 4 parallel data lines.

Note

The SD driver for Win7/WES7 does not currently support all SD cards.

5.1.9 General Purpose Serial Interface (UART)

The conga-MA3/MA3E offers two UART interfaces. The pins are designated SER0_TX, SER0_RX, SER1_TX and SER1_RX. Data out of the module is on the _TX pins. Hardware handshaking and hardware flow control are not supported. See table 23 "General Purpose Serial Interface Signal Descriptions" for the signal description.

Note

The onboard UART cannot be used in combination with an external, SuperIO based UART. They are mutually exclusive. The first UART is implemented as a legacy compatible UART while the second is implemented as HSUART. The HSUART is not legacy compatible. Compared with a legacy UART, it is limited in its feature set and requires a dedicated driver.

5.1.10 LPC Bus

The conga-MA3/MA3E offers the LPC (Low Pin Count) bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals and functionality. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific carrier board using this bus. Only certain devices such as Super I/O or TPM chips can be implemented on the carrier board. See section 9.1.1 for more information about the LPC Bus

Note

The Atom variants operate at a frequency of 33 MHz while the Celeron variants operate at 25 MHz.

5.1.11 SPI

An SPI interface that supports booting from an external SPI flash is available on the conga-MA3/MA3E via the Intel® Bay Trail SoC . The interface is implemented on the conga-MA3/MA3E as an alternative interface for the BIOS flash device. An SPI flash device can be used as a replacement for the firmware hub.

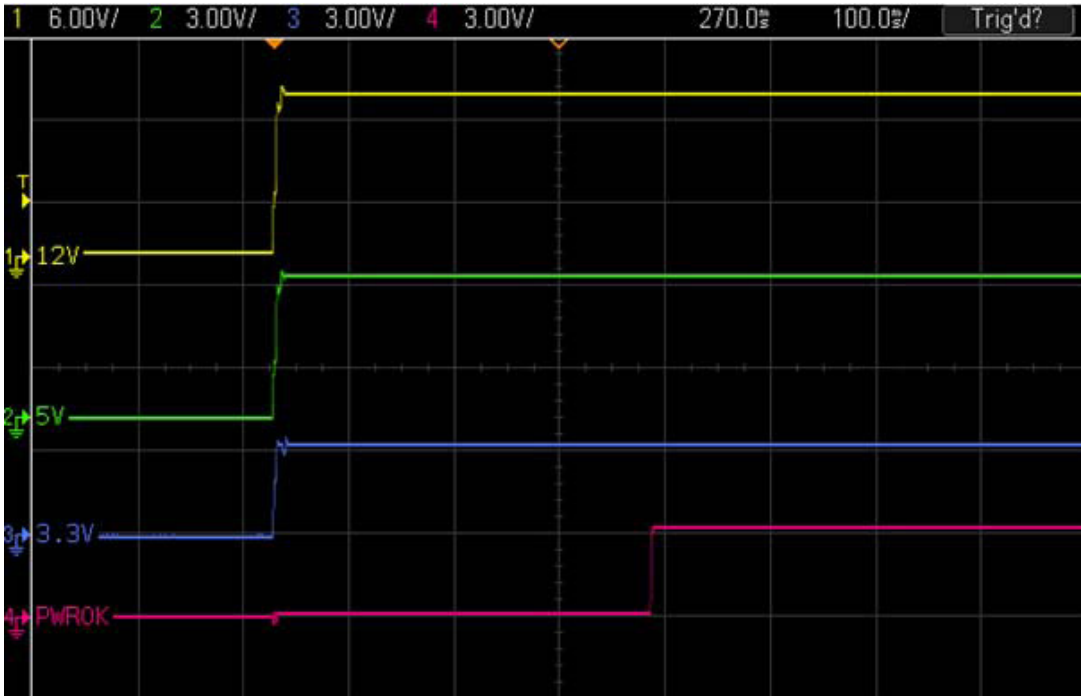
5.1.12 I²C Bus

The I²C bus is implemented through the congatec board controller. It provides a fast mode multi-master I²C bus.

5.1.13 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. See screenshot below.



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.
It is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the "power good" signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, you must make sure that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-MA3/MA3E provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-MA3/MA3E's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the COM Express connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the COM Express connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

Input power of 4.75 - 20 volt is the sole operational power source for the conga-MA3/MA3E. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-MA3/MA3E application:

- It has also been noticed that on some occasions, problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com..

5.1.14 Power Management

ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).

6 Additional Features

6.1 Onboard Interfaces

6.1.1 eMMC 4.5

The conga-MA3/MA3E offers an optional eMMC 4.5 flash (MLC/SLC) onboard. Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology. The performance of the newer eMMC may vary depending on the eMMC technology.

Note

The eMMC drivers for Win7/WES7 are currently not provided by Intel.

For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions.

6.1.2 congatec Board Controller (cBC)

The conga-MA3/MA3E is equipped with a Texas Instruments Tiva™ TM4E1231H6ZRBI microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

6.1.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.1.2.2 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

6.1.2.3 Watchdog

The conga-MA3/MA3E is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the watchdog; therefore, the conga-MA3/MA3E does not support external hardware triggering.

For more information about the Watchdog feature, see the BIOS setup description section 10.4.1 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

6.1.2.4 Fan Control

The conga-MA3/MA3E has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

A four wire fan must be used to generate the correct speed readout.

For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express Design Guide.

6.1.2.5 General Purpose Input/Output

The conga-MA3/MA3E offers general purpose inputs and outputs for custom system design. These GPIOs are multiplexed with SD signals and are controlled by the cBC.

6.1.2.6 I²C Bus

The conga-MA3/MA3E offers support for the frequently used I²C bus. Thanks to the I²C host controller in the cBC the I²C bus is multimaster capable and runs at fast mode.

6.1.3 Embedded BIOS

The conga-MA3/MA3E is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. These are the most important embedded PC features:

6.1.3.1 CMOS Backup in Non Volatile Memory

A copy of the CMOS memory (SRAM) is stored in the BIOS flash device. This prevents the system from not booting up with the correct system configuration if the backup battery (RTC battery) has failed. Additionally, it provides the ability to create systems that do not require a CMOS backup battery.

6.1.3.2 OEM CMOS Default Settings and OEM BIOS Logo

This feature allows system designers to create and store their own CMOS default configuration and BIOS logo (splash screen) within the BIOS flash device. Customized BIOS development by congatec for these changes is no longer necessary because customers can easily do these changes by themselves using the congatec system utility CGUTIL.

6.1.3.3 OEM BIOS Code

With the congatec embedded BIOS it is even possible for system designers to add their own code to the BIOS POST process. Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table, verb tables for HDA codecs, rare graphic modes and Super I/O controllers.

For more information about customizing the congatec embedded BIOS refer to the congatec System Utility user's guide, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com or contact congatec technical support.

6.1.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-MA3/MA3E BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^3 User's Guide

6.2 API Support (CGOS/EAPI)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

Other COM (Computer on Modules) vendors offer similar driver solutions for these kind of embedded PC features, which are by nature proprietary. All the API solutions that can be found on the market are not compatible to each other. As a result, writing application software that can run on more than one vendor's COM is not so easy. Customers have to change their application software when switching to another COM vendor. EAPI (Embedded Application Programming Interface) is a programming interface defined by the PICMG that addresses this problem. With this unified API, it is now possible to run the same application on all vendor's COMs that offer EAPI driver support. Contact congatec technical support for more information about EAPI.

6.3 Security Features

The conga-MA3/MA3E does not have an onboard TPM chip. It however supports carrier board mounted TPM, connected via the LPC bus.

6.4 Suspend to Ram

The Suspend to RAM feature is available on the conga-MA3/MA3E.

6.5 ECC Memory Support

Error-Correcting Code (ECC) memory is a memory system that tests for and corrects errors automatically, very often without the operating system being aware of it, let alone the user. As data are written into memory, ECC circuitry generates checksums from the binary sequences in the bytes and stores them in an additional seven bits of memory for 32-bit data paths or eight bits for 64-bit paths. When data are retrieved from memory, the checksum is recomputed to determine if any of the data bits have been corrupted.

Note

The conga-MA3 does not support ECC memory. Only the conga-MA3E supports ECC memory. The ECC memory can detect and correct single bit errors. It can detect but not correct double bit errors.

7 conga Tech Notes

The conga-MA3/MA3E has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help the user to better understand the information found in the system resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Description section.

7.1 Intel Bay Trail SoC Features

7.1.1 Processor Core

The Intel Bay Trail Soc features Single, Dual or Quad Out-of-Order Execution processor cores. The cores are sub-divided into dual-core modules with each module sharing a 1 MB L2 cache (512 KB per core). Some of the features supported by the core are:

- Intel 64 architecture
- Intel Streaming SIMD Extensions 4.1 and 4.2
- Support for Intel VT-x
- Thermal management support vial Intel Thermal Monitor
- Uses Power Aware Interrupt Routing
- Uses 22 nm process technology

Note

Intel Hyper-Threading technology is not supported (four cores execute four threads)

7.1.1.1 Intel Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel® VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

7.1.1.2 AHCI

The Intel Bay Trail SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

Legacy Mode

When operating in legacy mode, the SATA controllers need two legacy IRQs (14 and 15) and are unable to share these IRQs with other devices. This is because the SATA controllers emulate the primary and secondary legacy IDE controllers.

Native Mode

Native mode allows the SATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources. This means they can be configured anywhere within the system. When either SATA controller 1 or 2 runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system. Setting "Native IDE" mode in the BIOS setup program will automatically enable Native mode. See section 10.4.14 for more information about this.

Running in native mode frees up interrupt resources (IRQs 14 and 15) and decreases the chance that there may be a shortage of interrupts when installing devices.

Note

If your operating system supports native mode then congatec AG recommends you enable it.

7.1.1.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-MA3/MA3E ACPI thermal solution currently offers two different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.2 ACPI Suspend Modes and Resume Events

conga-MA3/MA3E supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 10.4.8 "ACPI Configuration Submenu".

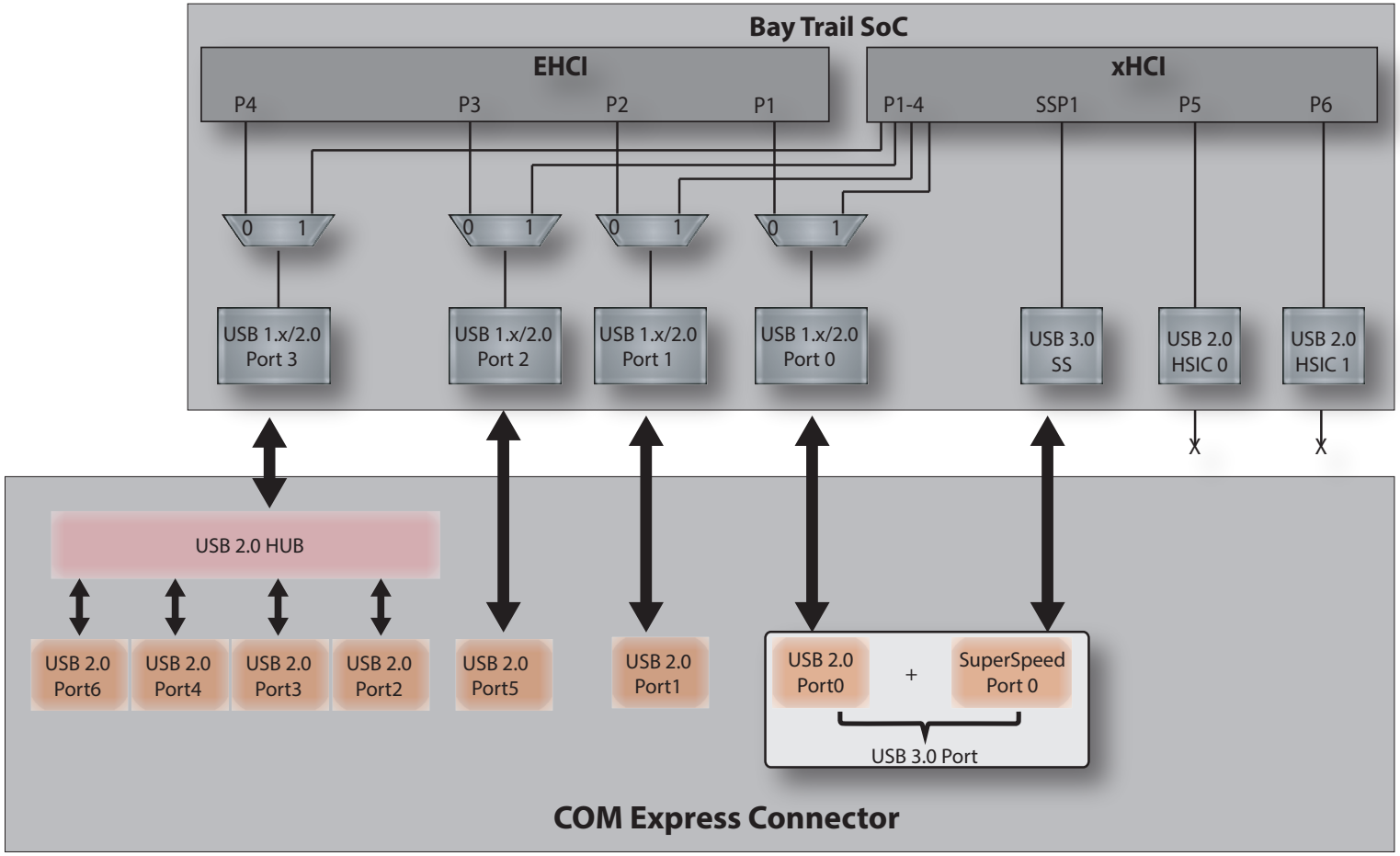
S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Windows 7, Windows Vista, Windows XP and Linux

This table lists the "Wake Events" that resume the system from S3 unless otherwise stated in the "Conditions/Remarks" column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

7.3 USB Port Mapping



8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type 10 connectors used for congatec AG modules. The pinout of the modules complies with COM Express Type 10 Rev. 2.1.

The table below describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 10 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V
I/O 5V	Bi-directional signal 5V
I 3.3V	Input 3.3V
I 5V	Input 5V
I/O 3.3VSB	Input 3.3V active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

8.1 COM Express Connector Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND(FIXED)	B1	GND(FIXED)	A56	RSVD	B56	RSVD
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND(FIXED)	B60	GND(FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0# (*)	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# (*)	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND(FIXED)	B11	GND(FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1# (**)
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND(FIXED)	B70	GND(FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	eDP_TX2+/LVDS_A0+	B71	DDI0_PAIR0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	eDP_TX2-/LVDS_A0-	B72	DDI0_PAIR0-
A18	SUS_S4#	B18	SUS_STAT#	A73	eDP_TX1+/LVDS_A1+	B73	DDI0_PAIR1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	eDP_TX1-/LVDS_A1-	B74	DDI0_PAIR1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	eDP_TX0+/LVDS_A2+	B75	DDI0_PAIR2+
A21	GND(FIXED)	B21	GND(FIXED)	A76	eDP_TX0-/LVDS_A2-	B76	DDI0_PAIR2-
A22	USB_SSRX0-	B22	USB_SSTX0-	A77	eDP/LVDS_VDD_EN	B77	DDI0_PAIR4+ (*)
A23	USB_SSRX0+	B23	USB_SSTX0+	A78	LVDS_A3+	B78	DDI0_PAIR4- (*)
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP/LVDS_BKLT_EN
A25	USB_SSRX1- (*)	B25	USB_SSTX1- (*)	A80	GND(FIXED)	B80	GND(FIXED)
A26	USB_SSRX1+ (*)	B26	USB_SSTX1+ (*)	A81	eDP_TX3+/LVDS_A_CK+	B81	DDI0_PAIR3+
A27	BATLOW#	B27	WDT	A82	eDP_TX3-/LVDS_A_CK-	B82	DDI0_PAIR3-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2 (*)	A83	eDP_AUX+/LVDS_I2C_CK	B83	eDP/LVDS_BKLT_CTRL
A29	AC/HDA_SYNC (**)	B29	AC/HDA_SDIN1 (*)	A84	eDP_AUX-/LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0 (**)	A85	GPI3	B85	VCC_5V_SBY
A31	GND(FIXED)	B31	GND(FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA_BITCLK (**)	B32	SPKR	A87	eDP_HPD	B87	VCC_5V_SBY
A33	AC/HDA_SDOUT (**)	B33	I2C_CK	A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE_CLK_REF-	B89	DD0_HPD
A35	THRMTRIP#	B35	THRM#	A90	GND(FIXED)	B90	GND(FIXED)
A36	USB6-	B36	USB7- (*)	A91	SPI_POWER	B91	DDI0_PAIR5+ (*)
A37	USB6+	B37	USB7+ (*)	A92	SPI_MISO (**)	B92	DDI0_PAIR5- (*)
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	DDI0_PAIR6+ (*)

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A39	USB4-	B39	USB5-	A94	SPI_CLK (**)	B94	DDI0_PAIR6- (*)
A40	USB4+	B40	USB5+	A95	SPI_MOSI (**)	B95	DDI0_DDC_AUX_SEL
A41	GND(FIXED)	B41	GND(FIXED)	A96	TPM_PP (*)	B96	RSVD
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS# (**)
A43	USB2+	B43	USB3+	A98	SER0_TX (**)	B98	DDI0_CTRLCLK_AUX+
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX (**)	B99	DDI0_CTRLDATA_AUX-
A45	USB0-	B45	USB1-	A100	GND(FIXED)	B100	GND(FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX (**)	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX (**)	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ (**)	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND(FIXED)	B51	GND(FIXED)	A106	VCC_12V	B106	VCC_12V
A52	RSVD	B52	RSVD	A107	VCC_12V	B107	VCC_12V
A53	RSVD	B53	RSVD	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	RSVD	B55	RSVD	A110	GND(FIXED)	B110	GND(FIXED)

Note

The signals marked with asterisk (*) are not supported or connected on the conga-MA3/MA3E.

On Intel Bay Trail SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the COM Express Specification. To comply with the COM Express Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

8.2 COM Express Connector Signal Descriptions

Table 11 High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	High Definition Audio Reset: This signal is the master hardware reset to external codec(s).	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SYNC (**)	A29	High Definition Audio Sync: This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_BITCLK (**)	A32	High Definition Audio Bit Clock Output: This signal is a 24.000MHz serial data clock generated by the Intel® High Definition Audio controller.	O 3.3V		AC'97 codecs are not supported.
AC/HDA_SDOUT (**)	A33	High Definition Audio Serial Data Out: This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3V	PU 1K 3.3VSB	AC'97 codecs are not supported.
AC/HDA_SDIN[2:0] (**)	B28-B30	High Definition Audio Serial Data In [0]: These signals are serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	I/O 3.3V	PD 100K	AC'97 codecs are not supported. HDA_SDIN[2:1] are not connected.

Note

On Intel Bay Trail SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the COM Express Specification. To comply with the COM Express Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

Table 12 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		Twisted pair signals for external transformer.
			1000	100	10			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.				O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.				O 3.3VSB		

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.			Not connected

Table 13 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6

Table 14 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 15 ExpressCard Support Pins Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request.	I 3.3V	PU 10k 3.3V	
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3V	PU 10k 3.3V	

Table 16 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB Port 0 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Default port to form Native USB 3.0 port
USB1+ USB1-	B46 B45	USB Port 1 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Native USB port. Only this port can be used as debug port.
USB2+ USB2-	A43 A42	USB Port 2 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Routed via on-module USB hub.
USB3+ USB3-	B43 B42	USB Port 3 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Routed via on-module USB hub.
USB4+ USB4-	A40 A39	USB Port 4 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Routed via on-module USB hub.
USB5+ USB5-	B40 B39	USB Port 5 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Native USB port
USB6+ USB6-	A37 A36	USB Port 6 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1 Routed via on-module USB hub.
USB7+ USB7-	B37 B36	USB Port 7 differential data pairs	I/O		Not connected
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_SSTX0+ USB_SSTX0-	B23 B22	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O PCIe		

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSTX1+ USB_SSTX1-	B26 B25	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O PCIe		Not connected.
USB_SSRX0+ USB_SSRX0-	A23 A22	Additional receive signal differential pairs for the SuperSpeed USB data path.	I PCIe		
USB_SSRX1+ USB_SSRX1-	A26 A25	Additional receive signal differential pairs for the SuperSpeed USB data path.	I PCIe		Not connected.

Table 17 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ eDP_TX2+	A71	LVDS Channel A differential pair 0 Embedded Display Port channel 0 differential pair 2	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A0- eDP_TX2-	A72	LVDS Channel A differential pair 0 Embedded Display Port channel 0 differential pair 2	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A1+ eDP_TX1+	A73	LVDS Channel A differential pair 1 Embedded Display Port channel 0 differential pair 1	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A1- eDP_TX1-	A74	LVDS Channel A differential pair 1 Embedded Display Port channel 0 differential pair 1	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A2+ eDP_TX0+	A75	LVDS Channel A differential pair 2 Embedded Display Port channel 0 differential pair 0	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A2- eDP_TX0-	A76	LVDS Channel A differential pair 2 Embedded Display Port channel 0 differential pair 0	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A3+	A78	LVDS Channel A differential pair 3			
LVDS_A3-	A79	LVDS Channel A differential pair 3			
LVDS_A_CK+ eDP_TX3+	A81	LVDS Channel A differential clock Embedded Display Port channel 0 differential pair 3	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_A_CK- eDP_TX3-	A82	LVDS Channel A differential clock Embedded Display Port channel 0 differential pair 3	O LVDS O eDP		LVDS (default) Build-time option: eDP
LVDS_VDD_EN eDP_VDD_EN	A77	Panel power enable	O 3.3V	PD 10k	LVDS (default) Build-time option: eDP
LVDS_BKLT_EN eDP_BKLT_EN	B79	Panel backlight enable	O 3.3V	PD 10k	LVDS (default) Build-time option: eDP
LVDS_BKLT_CTRL eDP_BKLT_CTRL	B83	Panel backlight brightness control	O 3.3V		LVDS (default) Build-time option: eDP
LVDS_I2C_CK eDP_AUX+	A83	DDC lines used for flat panel detection and control. Embedded Display Port AUX channel pair	O 3.3V	PU 2k2 3.3V	LVDS (default) Build-time option: eDP
LVDS_I2C_DAT eDP_AUX-	A84	DDC lines used for flat panel detection and control. Embedded Display Port AUX channel pair	I/O 3.3V	PU 2k2 3.3V	LVDS (default) Build-time option: eDP

Table 18 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V		Not connected
LPC_SERIRQ (**)	A50	LPC serial interrupt	I/O OD 3.3V		
LPC_CLK	B10	LPC clock output - 33MHz for Bay Trail-I. 25MHz for Bay Trail-M and D	O 3.3V		

Note

On Intel Bay Trail SoC, the signal marked with asterisks (**) has different voltage level from the level defined in the COM Express Specification. To comply with the COM Express Specification, the signal is routed through bidirectional level shifter on the module.

Bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route this signal as short as possible.

Table 19 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS# (**)	B97	Chip select for carrier board SPI.	O 3.3VSB		Carrier shall pull to SPI_POWER when external SPI provided but not used.
SPI_MISO (**)	A92	Master Input Slave Output: SPI output data from carrier board SPI device to module.	I 3.3VSB		
SPI_MOSI (**)	A95	Master Output Slave Input: SPI output data from module to carrier board SPI.	O 3.3VSB		
SPI_CLK (**)	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	+ 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or leave no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. Ground to select external SPI device. Pull high or leave no-connect to select on-module BIOS flash	I 3.3VSB	PU 10K 3.3VSB	Carrier shall pull to GND or leave no-connect

Note

On Intel Bay Trail SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the COM Express Specification. To comply with the COM Express Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

Table 20 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI0_PAIR0+ DDI0_PAIR0-	B71 B72	Digital Display Interface 0 Pair 0 differential pairs	O		Only TMDS/DP option, no SDVO
DDI0_PAIR1+ DDI0_PAIR1-	B73 B74	Digital Display Interface 0 Pair 1 differential pairs	O		Only TMDS/DP option, no SDVO
DDI0_PAIR2+ DDI0_PAIR2-	B75 B76	Digital Display Interface 0 Pair 2 differential pairs	O		Only TMDS/DP option, no SDVO
DDI0_PAIR3+ DDI0_PAIR3-	B81 B82	Digital Display Interface 0 Pair 3 differential pairs	O		Only TMDS/DP option, no SDVO
DDI0_HPD	B89	Digital Display Interface Hot Plug Detect	I 3.3V	PD 1M	
DDI0_CTRLCLK_AUX+	B98	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect.	I/O	PD100k @ DP mode	
		TMDS I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O OD 3.3V	PU 5k 3.3V @ TMDS mode	
DDI0_CTRLDATA_AUX-	B99	DP AUX- function if DDI1_DDC_AUX_SEL is no connect.	I/O	PU 100k 3.3V@ DP mode	
		TMDS I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O OD 3.3V	PU 5k 3.3V @ TMDS mode	
DDI0_DDC_AUX_SEL	B95	Selects the function of DDI0_CTRLCLK_AUX+ and DDI0_CTRLDATA_ AUX-. This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3V	PD 1M	

Table 21 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP0_LANE0+ DP0_LANE0-	B71 B72	Uni-directional main link for the transport of isochronous streams and secondary data.	O		
DP0_LANE1+ DP0_LANE1-	B73 B74	Uni-directional main link for the transport of isochronous streams and secondary data.	O		
DP0_LANE2+ DP0_LANE2-	B75 B76	Uni-directional main link for the transport of isochronous streams and secondary data. .	O		
DP0_LANE3+ DP0_LANE3-	B81 B82	Uni-directional main link for the transport of isochronous streams and secondary data.	O		
DP0_HPD	B89	Detection of Hot Plug / Unplug and notification of the link layer.	I 3.3V	PD 1M	

Signal	Pin #	Description	I/O	PU/PD	Comment
DP0_AUX+	B98	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O	PD 100k	
DP0_AUX-	B99	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O	PU 100k 3.3V	

Table 22 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS0_DATA2+ TMDS0_DATA2-	B71 B72	TMDS lane 2 differential pair.	O		
TMDS0_DATA1+ TMDS0_DATA1-	B73 B74	TMDS lane 1 differential pair.	O		
TMDS0_DATA0+ TMDS0_DATA0-	B75 B76	TMDS lane 0 differential pair.	O		
TMDS0_CLK + TMDS0_CLK -	B81 B82	TMDS Clock output differential pair.	O		
HDMI0_HPD	B89	TMDS Hot-plug detect.	I	PD 1M	
HDMI0_CTRLCLK	B98	TMDS I²C Control Clock	I/O OD 3.3V	PU 5k 3.3V	
HDMI0_CTRLDATA	B99	TMDS I²C Control Data	I/O OD 3.3V	PU 5k 3.3V	

Note

The conga-MA3/MA3E does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented.

Table 23 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX (**)	A98	General purpose serial port transmitter	O 3.3V	PU 5K 3.3V	12 volt tolerant
SER1_TX (**)	A101	General purpose serial port transmitter	O 3.3V	PU 5K 3.3V	12 volt tolerant
SER0_RX (**)	A99	General purpose serial port receiver	I 3.3V	PU 5K 3.3V	12 volt tolerant
SER1_RX (**)	A102	General purpose serial port receiver	I 3.3V	PU 5K 3.3V	12 volt tolerant

Note

On Intel Bay Trail SoC, the signals marked with asterisks (**) have voltage levels that are different from the levels defined in the COM Express Specification. To comply with the COM Express Specification, the signals are routed through bidirectional level shifters on the module.

The bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route these signals as short as possible.

Table 24 I2C Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I2C port clock output	I/O OD 3.3V	PU 2.2K 3.3VSB	
I2C_DAT	B34	General purpose I2C port data I/O line	I/O OD 3.3V	PU 2.2K 3.3VSB	

Table 25 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PD 10K	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V		
FAN_TACHIN	B102	Fan tachometer input.	I OD	PU 10K 3.3V	Requires a fan with a two pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. This feature is not implemented on the conga-MA3/MA3E	I 3.3V		Not connected

Note

The congatec COM Express Type 6 and Type 10 modules use a Push-Pull output for the fan_pwm signal instead of the open drain output specified in the COM Express specification. Although this does not comply with the COM Express specification 2.0, the benefits are obvious. The Push-Pull output optimizes the power consumed by the fan_pwm signal without functional change.

Table 26 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a main power input (VIN) that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V		
SUS_STAT#	B18	Suspend Status: Indicates the system will enter a low power state soon. Used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3VSB		Same signal as SUS_S5#
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		Same signal as SUS_S4#
WAKE0#	B66	PCI Express wake up request signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1# (**)	B67	General purpose wake up signal. May be used to implement a wake-up request from an external device.	I 3.3VSB	PU 100k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low.	I 3.3VSB	PU 10k 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I OD 3.3V	PU 10k 3.3VSB	
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again. **Note:** For proper detection, assert a pulse width of at least 16 ms.	I OD 3.3V	PU 10k 3.3VSB	

Note

On Intel Bay Trail SoC, the signal marked with asterisks (**) has different voltage level from the level defined in the COM Express Specification. To comply with the COM Express Specification, the signal is routed through bidirectional level shifter on the module.

Bidirectional level shifters by nature have limited driving strenght. congatec therefore recommends that you route this signal as short as possible.

Table 27 Thermal Protection Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over temperature situation	I 3.3V	PU 10k 3.3V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown	O 3.3V	PU 10k 3.3V	

Table 28 SM Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line	I/O OD 3.3VSB	PU 10k 3.3VSB	
SMB_DAT	B14	System Management Bus bidirectional data line	I/O OD 3.3VSB	PU 10k 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert - Active low input can be used to generate an SMI# (System Management Interrupt)	I 3.3VSB	PU 10k 3.3VSB	

Table 29 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3V	PU 10K 3.3V	
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3V	PU 10K 3.3V	
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3V		
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3V		
GPO2	B57	General purpose output pins. Shared with SD_WP. Output from COM Express, input to SD	O 3.3V		
GPO3	B63	General purpose output pins. Shared with SD_CD. Output from COM Express, input to SD	O 3.3V		

Table 30 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	B63	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. Maps to GPO3; used as an input when used for SD card support	I 3.3V		
SDIO_CLK	A93	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz. Maps to GPO0.	O 3.3V		

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CMD	B54	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Maps to GPO1	O 3.3V		
SDIO_WP	B57	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. Maps to GPO2; used as an input when used for SD card support	I 3.3V		
SDIO_DAT0	A54	SDIO Data line. Operates in push-pull mode and maps to GPI0	IO 3.3V		
SDIO_DAT1	A63	SDIO Data line. Operates in push-pull mode and maps to GPI1	IO 3.3V		
SDIO_DAT2	A67	SDIO Data line. Operates in push-pull mode and maps to GPI2	IO 3.3V		
SDIO_DAT3	A85	SDIO Data line. Operates in push-pull mode and maps to GPI3	IO 3.3V		

Table 31 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE10#	A97	Indicates to the carrier board that a Type 10 module is installed.	PDS	This pin is pulled to ground through a 47K resistor.

Table 32 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: 4.75V to 20V. All available VCC_12V pins on the connector(s) shall be used.	P		The conga-MA3/MA3E is a Type 10 mini module and as such supports a wide power supply range between 4.75 and 20V
VCC_5V_SBY	B84-B87	Standby power input: +5V nominal. If VCC5V_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real time clock circuit-power input: +3V nominal	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110 B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

Table 33 CAN Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CAN0_TX	A101	Controller Area Network TX output for CAN Bus channel 0. This pin is shared with SER1_TX	O 3.3V		Not supported
CAN0_RX	A102	Controller Area Network RX input for CAN Bus channel 0. This pin is shared with SER1_RX	I 3.3V		Not supported

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-MA3 and conga-MA3E modules are functionally identical with a standard PC/AT.

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.1.1 LPC Bus

On the conga-MA3 and conga-MA3E, the Platform Controller Hub (PCH) acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCH and the LPC Bus. Some fixed I/O space ranges seen by the processor:

Table 34 Fixed I/O Space Addresses

Device	IO Address
8259 Master	20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39h, 3Ch-3Dh,
8254s	40h-43h, 50h-53h
PS2 Control	60h, 64h,
NMI Controller	61h, 63h, 65h, 67h
RTC	70h-77h
Port 80h	80h-83h
Init Register	92h
8259 Slave	A0h- A1h, A4h-A5h, A8h-A9h, ACh-ADh, B0h-B1h, B4h-B5h, B8h-B9h, BCh-BDh, 4D0h-4D1h
PCU UART	3F8h-3FFh
Reset Control	CF9h
Active Power Management	B2h-B3h

Some of these ranges may be used by a Super I/O on the carrier board, or are occupied by the COM Express module UARTs if these are enabled in setup. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 35 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	SoC Transaction Router
00h	02h	00h	Graphics & Display
00h	012h	00h	SD Port
00h	013h	00h	SATA
00h	014h	00h	XHCI USB
00h	017h	00h	EMMC 4.5 Port
00h	01Ah	00h	Trusted Execution Engine
00h	01Bh	00h	HD Audio
00h	01Ch	00h	PCI Express Root Port 1
00h	01Ch	01h	PCI Express Root Port 2
00h	01Ch	02h	PCI Express Root Port 3
00h	01Ch	03h	PCI Express Root Port 4
00h	01Dh	00h	EHCI USB
00h	1Fh	00h	LPC
00h	1Fh	03h	SMBUS
04h	00h	00h	Intel I210 Ethernet

Note

1. *The PCI Express Ports are visible only if they are set to "Enabled" in the BIOS setup program and a device attached to the corresponding PCI Express port on the carrier board.*

2. *The above table represents a case when a single function PCI Express device is connected to all possible slots on the carrier board. The given bus numbers will change based on the actual configuration of the hardware.*

9.3 PCI Interrupt Routing Map

Table 36 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line [1]	APIC Mode IRQ	Graphics	SD Port	SATA	XHCI	eMMC 4.5	TXE	HD Audio	PCIe Root Port 1	PCIe Root Port 2	PCIe Root Port 3	PCIe Root Port 4	EHCI	SMBUS	I210 Ethernet
A	INTA	16	x							x						
B	INTB	17									x					
C	INTC	18		x								x			x	
D	INTD	19			x								x			x
E		20				x										
F		21						x								
G		22							x							
H		23					x							x		

Note

[1] *These interrupt lines are virtual (message based).*

9.4 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.5 SM Bus

System Management (SM) bus signals are connected to the Intel Baytrail SoC, and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject please contact congatec technical support.

10 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

10.1 Entering the BIOS Setup Program

The BIOS setup program can be accessed by pressing the <DEL> or <ESC> key during POST.

10.1.1 Boot Selection Popup

Press the <F11> key during POST to access the Boot Selection Popup menu. A selection menu displays immediately after POST, allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

10.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar, left frame and right frame. The menu bar is shown below:

Main	Advanced	Chipset	Security	Boot	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

Note

Entries in the option column that are displayed in bold indicate BIOS default values.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

10.3 Main Setup Screen

When you first enter the BIOS setup, you will see the main setup screen. The main setup screen reports BIOS, processor, memory and board information and is for configuring the system date and time. You can always return to the main setup screen by selecting the 'Main' tab.

Feature	Options	Description
Main BIOS Version	No option	Displays the main BIOS version.
OEM BIOS Version	No option	Displays the additional OEM BIOS version.
Build Date	No option	Displays the date the BIOS was built.
Product Revision	No option	Displays the hardware revision of the board.
Serial Number	No option	Displays the serial number of the board.
BC Firmware Rev.	No option	Displays the firmware revision of the congatec board controller.
MAC Address	No option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	No option	Displays the number of boot-ups. (max. 16777215).
Microcode Patch	No option	Displays the Microcode Patch loaded for the onboard CPU.
Baytrail SoC	No option	B3 Stepping.
Total Memory	No option	Total amount of Low Voltage DDR3 present on the system.
System Date	Day of week, month/day/year	Specifies the current system date. *Note: The date is in month-day-year format.*
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24 hour format.*

10.4 Advanced Setup

Select the advanced tab from the setup menu to enter the advanced BIOS setup screen. The menu is used for setting advanced features.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Watchdog				
	Graphics				
	Hardware Health Monitoring				
	Trusted Computing				
	RTC Wake				
	Module Serial Ports				
	Reserve Legacy Interrupt				
	ACPI				
	Super IO				
	Intel(R) Smart Connect Technology				
	Serial Port Console Redirection				
	CPU Configuration				
	PPM Configuration				
	Thermal Configuration				
	IDE Configuration				
	Miscellaneous Configuration				
	SCC Configuration				
	PCI Subsystem Settings				
	Network Stack				
	CSM Configuration				
	SDIO				
	USB				
	Platform Trust Technology				
	Security Configuration				
	Intel(R) I210 Gigabit Network				
	Driver Health				

10.4.1 Watchdog Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Sets the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Stop Watchdog for User Interaction	No **Yes**	Sets whether the POST watchdog should be stopped during the popup of the boot selection menu, or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One-time Trigger Single Event Repeated Event	Sets the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to 'One-time Trigger', the watchdog will be disabled after the first trigger. If set to 'Single Event', every stage will be executed only once, then the watchdog will be disabled. If set to 'Repeated Event', the last stage will be executed repeatedly until a reset occurs.
Delay	**Disabled** 10sec 30sec 1min 2min 5min 10min 30min	Sets the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	ACPI Event **Reset** Power Button	Sets the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event, see note below.
Event 2	**Disabled** ACPI Event Reset Power Button	Sets the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** ACPI Event Reset Power Button	Sets the type of event that will be generated when timeout 3 is reached.

Feature	Options	Description
Timeout 1	1sec 2sec 5sec 10sec **30sec** 1min 2min 5min 10min 30min	Sets the timeout value for the first stage watchdog event.
Timeout 2	see above	Sets the timeout value for the second stage watchdog event.
Timeout 3	see above	Sets the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Sets the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

In ACPI mode, it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

10.4.2 Graphics Submenu

Feature	Options	Description
Boot Display Device	VBIOS Default	
CRT	**Enable** Disable	Enable CRT Video Interface.
Active LFP	No LVDS **LVDS**	Sets the active local flat panel configuration.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel. If no external EDID data set is found, the data set selected under 'Local Flat Panel Type' will then be used as a fallback data set.
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) HD 1920x1080 2x24 (01Dh) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Sets a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.
Backlight Inverter Type	None **PWM** I2C	Sets the type of backlight inverter used. PWM = Use IGD PWM signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.
Digital Display Interface 1 (DDI1)	Disabled DisplayPort **HDMI™/DVI** Auto	Select the output type of the Digital Display Interface 1.
PWM Inverter Frequency (Hz)	**200** - 40000	Set the PWM inverter frequency in Hz. Only visible if 'Backlight Inverter Type' is set to 'PWM'.
PWM Inverter Polarity	**Normal** Inverted	Sets PWM inverter polarity. Only visible if 'Backlight Inverter Type' is set to 'PWM' .

Feature	Options	Description
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, **75%**, 90%, 100%	Actual backlight value in percent of the maximum setting.
Force LVDS Backlight	**No** Yes	Board Controller forces Backlight Enable Signal unconditionally, independently from SoC Backlight Signal.
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Backlight Delay	**No Delay** 100ms Delay 250ms Delay 500ms Delay 1s Delay	congatec Board Controller will add a delay on the Backlight signal coming from the SoC according this setup node. This delay is intended to adjust some LVDS Panel Timings.
LVDS SSC	**Disabled** 0.5% 1.0% 1.5% 2.0% 2.5%	Configure LVDS Spread Spectrum Clock Modulation depth. It performs a center spreading and a fixed modulation frequency of 32.9kHz.

10.4.3 Hardware Health Monitoring Submenu

Feature	Options	Description
CPU Temperature	No option	Displays the actual CPU temperature in °C.
Board Temperature	No option	Displays the actual board temperature in °C.
DC Input Voltage	No option	Displays the actual voltage of the 12V standard supply.
5V Standby	No option	Displays the actual voltage of the 5V standby supply.
CPU Fan Speed	No option	Displays the actual CPU Fan Speed in RPM.
Fan PWM Frequency Mode	Low Frequency **High Frequency**	Sets the fan PWM base frequency mode: - 11.0-88.2Hz for Low Frequency - 1k-63kHz for High Frequency
Fan PWM Frequency (kHz)	1 – 63	Sets the fan PWM base frequency (1-63kHz). Default: 31kHz

10.4.4 Trusted Computing Submenu

Feature	Options	Description
Security Device Support	**Disabled** Enabled	Enable or disable TPM support. System reset is required after change.
User Confirmation	**Disabled** Enabled	Enable or disable user confirmation requests for certain transactions.
TPM State	**Disabled** Enabled	Enable or disable TPM chip. Note: System might restart several times during POST to acquire target state.
Pending operation	**None,** Enable Take Ownership, Disable Take Ownership, TPM Clear	Perform selected TPM chip operation. Note: System might restart several times during POST to perform selected operation.

10.4.5 RTC Wake Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour		Specify wake up hour (0 - 23). For example, enter “3” for 3am and “15” for 3pm.
Wake up minute		Specify wake up minute.
Wake up second		Specify wake up second.

10.4.6 Module Serial Ports Submenu

Feature	Options	Description
Serial Port 0	**Disabled** Enabled	Enable or disable module serial port 0.
Serial Port 1	**Disabled** Enabled	Enable or disable module serial port 1.

10.4.7 Reserve Legacy Interrupt Submenu

Feature	Options	Description
Reserve Legacy Interrupt 1/2/3	**None** IRQ3 IRQ4 IRQ5 IRQ6 IRQ10 IRQ11 IRQ14 IRQ15	The interrupt will not be assigned to any PCI or PCI Express device and thus may be available for a legay bus device.

10.4.8 ACPI Submenu

Feature	Options	Description
Enable ACPI Auto Configuration	**Disabled** Enabled	Enable or disable BIOS ACPI Auto Configuration
Enable Hibernation	Disabled **Enabled**	Enable or disable system's ability to hibernate (operating system S4 sleep state). This option may not be effective with some operating systems.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Sets the state used for ACPI system sleep/suspend.
Lock Legacy Resources	**Disabled** Enabled	Enable or disable lock of legacy resources.
LID Support	Disabled **Enabled**	Configure COM Express LID# signal to act as ACPI lid
Sleep Button Support	Disabled **Enabled**	Configure COM Express SLEEP# signal to act as ACPI sleep button.

10.4.9 SIO Submenu

Feature	Options	Description
AMI SIO Driver Version		
▶Serial Port 1	No option	Serial Port 1 Submenu
▶Serial Port 2	No option	Serial Port 2 Submenu
▶Parallel Port	No option	Parallel Port Submenu

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

10.4.9.1 Serial Port 1 Submenu

Feature	Options	Description
Serial Port	**Enable** Disable	Enable or disable Serial Port (COM).
Change Settings	**Auto** IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11, 12; DMA;	Select optimal settings for Super IO device.

10.4.9.2 Serial Port 2 Submenu

Feature	Options	Description
Serial Port	**Enable** Disable	Enable or disable Serial Port (COM).
Possible	**Use Automatic Settings** IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=2F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3F8; IRQ=3,4,5,7,9,10,11, 12; DMA; IO=3E8; IRQ=3,4,5,7,9,10,11, 12; DMA;	Serial Port 2 configuration options.
Device Mode	**Standard Serial Port Mode** IrDA Active pulse 1.6 uS IrDA Active pulse 3/16 bit time ASKIR Mode	Change the Serial Port mode.

10.4.9.3 Parallel Port Submenu

Feature	Options	Description
Parallel Port	Enabled **Disabled**	Enable or disable Parallel Port (LPT/LPTE).

10.4.10 Intel(R) Smart Connect Technology Submenu

Feature	Options	Description
ISCT Support	**Disabled** Enabled	Enable or disable Intel(R) Smart Connection Support. When this setup node is set as Disabled, all the other Nodes are not visible.
ISCT Notification Control	Disabled **Enabled**	Enable or disable ISCT Notification Control.
ISCT WLAN Power Control	Disabled **Enabled**	Enable or disable ISCT WLAN Power Control.
ISCT WWAN Power Control	Disabled **Enabled**	Enable or disable ISCT WWAN Power Control
ISCT Sleep Duration Value Format	**Duration in Seconds**	ISCT Sleep Duration in seconds.
ISCT RF Kill Switch Type	Software **Hardware**	Select Software or Hardware ISCT RF Kill Switch Type
ISCT RTC Timer Support	**Disabled** Enabled	Enable ISCT RTC Timer

10.4.11 Serial Port Console Redirection Submenu

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
▶Console Redirection Settings (COM0)	Submenu	Opens console redirection configuration submenu.
COM1 Console Redirection	**Disabled** Enabled	Enable or disable serial port 1 console redirection.
▶Console Redirection Settings (COM1)	Submenu	Opens console redirection configuration submenu.
Serial Port for Out-of-Band Management / EMS Console Redirection	**Disabled** Enabled	Enable or disable Serial Port for Out-of-Band Management / Windows Emergency Management Services.
▶Console Redirection Settings	Submenu	Opens console redirection configuration sub menu.

10.4.11.1 Console Redirection Settings COM 0 Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Sets terminal type.
Baudrate	9600, 19200, 38400, 57600, **115200**	Sets baud rate.
Data Bits	7, **8**	Sets number of data bits.
Parity	**None** Even Odd Mark Space	Sets parity.
Stop Bits	**1** 2	Sets number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Sets flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enable or disable extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Sets Function Key and Key Pad on Putty.

10.4.11.2 Console Redirection Settings COM 1 Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Sets terminal type.
Baudrate	9600, 19200, 38400, 57600, **115200**	Sets baud rate.
Data Bits	7, **8**	Sets number of data bits.
Parity	**None** Even Odd Mark Space	Sets parity.
Stop Bits	**1** 2	Sets number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Sets flow control.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enable or disable extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Sets Function Key and Key Pad on Putty.

10.4.11.3 Console Redirection Settings Out-of-Band Management Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ **VT-UTF8** ANSI	Sets terminal type.
Bits Per Second	9600, 19200, 38400, 57600, **115200**	Sets baud rate.
Data Bits	**8**	Set number of data bits.
Parity	**None**	Select parity.
Stop Bits	**1**	Set number of stop bits.

10.4.12 CPU Configuration Submenu

Feature	Options	Description
▶Socket 0 CPU Information	Submenu	Socket specific CPU information
▶CPU Thermal Configuration	Submenu	CPU thermal configuration options
CPU Speed	No option	CPU clock frequency
64-bit	No option	64-bit support information.
Limit CPUID Maximum	**Disabled** Enabled	When enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When disabled, the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Execute Disable Bit	Disabled **Enabled**	Enable or disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled, certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting OS.
Hardware Prefetcher	Disabled **Enabled**	Enable or disable the Mid Level Cache (MLC) streamer prefetcher.
Adjacent Cache Line Prefetch	Disabled **Enabled**	Enable or disable prefetching of adjacent cache lines.
Intel Virtualization Technology	Disabled **Enabled**	Enable or disable support for the Intel virtualization technology.
Power Technology	Disable **Energy Efficient** Custom	Configure the power technology schema for the CPU

10.4.12.1 Socket 0 CPU Information Submenu

Feature	Options	Description
CPU Name	No option	Displays socket specific CPU name
CPU Signature	No option	Displays CPU signature number
Microcode Patch	No option	Displays the CPU microcode patch number
Max. CPU Speed	No option	Displays the maximum CPU clock frequency
Min. CPU Speed	No option	Displays the minimum CPU clock frequency
Processor Cores	No option	Displays the number of CPU Core on Socket CPU
Intel HT Technology	No option	Displays the Intel HT Technology support information.
Intel VT-x Technology	No option	Displays the Intel VT-x Technology support information
L1 Data Cache	No option	Displays the Socket L1 data cache information
L1 Code Cache	No option	Displays the Socket L1 code cache information
L2 Cache	No option	Displays the Socket L2 cache information
L3 Cache	No option	Displays the Socket L3 cache information

10.4.12.2 CPU Thermal Configuration

Feature	Options	Description
DTS	Enabled **Disabled**	Enable or Disable CPU Digital Thermal Sensor (DTS). DTS is used on ACPI functions to read the CPU temperature. This value is read from MSR.

10.4.13 PPM Configuration

Feature	Options	Description
CPU C state Report	Disabled **Enabled**	Enable/Disable CPU state Report to Operating System.
Max CPU C state	C7 C6 **C1**	Maximal CPU C state supported by the CPU
SOix	**Disabled** Enabled	Enable/Disable CPU SOix state support

10.4.14 Thermal Configuration

Feature	Options	Description
Critical Trip Point	110 C **105 C** 100 C 95 C 90 C 87 C 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Temperature of the ACPI critical Trip Point in which the OS will shut the system off.
Passive Trip Point	110 C 105 C 100 C 95 C **90 C** 85 C 79 C 71 C 63 C 55 C 47 C 39 C 31 C 23 C 15 C	Temperature of the ACPI passive Trip Point in which the OS will begin throttling the processor.

Feature	Options	Description
Active Trip Point High	110 C 105 C 100 C 95 C 90 C 85 C **79 C** 71 C 63 C 55 C 47 C 39 C 31 C	This value controls the temperature of the ACPI active Trip Point – the point in which the OS will enable the active cooling device at maximum capacity. DST must be enable on the CPU Submenu to make effective this Node.
Active Trip Point Low	110 C 105 C 100 C 95 C 90 C 85 C 79 C **71 C** 63 C 55 C 47 C 39 C 31 C 23 C 15 C	This value controls the temperature of the ACPI active Trip Point – the point in which the OS will enable the active cooling device at maximum capacity. DST must be enable on the CPU Submenu to make effective this Node.

10.4.15 IDE Configuration Submenu

Feature	Options	Description
Serial-ATA (SATA)	**Enabled** Disabled	Enable or disable the onboard SATA controller.
SATA Test Mode	Enabled **Disabled**	Should be set to Disabled. Test Mode is used just for verification measurements.
SATA Speed Support	Gen1 **Gen2**	Indicates the maximum speed the SATA controller can support.
SATA ODD Port	Port 0 ODD Port 1 ODD **No ODD**	Configure which SATA Port is ODD.

Feature	Options	Description
SATA Mode	IDE Mode **AHCI Mode**	Configure SATA Port Mode
mSATA Interface	mSATA mPCIe **Auto**	Configures the physical interface to support mSATA or mPCIE.
Serial-ATA Port 0	**Enabled** Disabled	Enable or disable the SATA Port 0.
SATA Port 0 Hot Plug	**Disabled** Enabled	Sets hot plug support for SATA Port 0. Not possible in Native IDE mode.
Serial-ATA Port 1	**Enabled** Disabled	Enable or disable the SATA Port 1.
SATA Port 1 Hot Plug	**Disabled** Enabled	Sets hot plug support for SATA Port 1. Not possible in Native IDE mode.
SATA Port 0 Information	No Option	Displays Information of device detected on SATA Port 0.
SATA Port 1 Information	No Option	Displays Information of device detected on SATA Port 1.

10.4.16 Miscellaneous

Feature	Options	Description
High Precision Timer	**Enabled** Disabled	Enable or disable the high precision event timer.
Boot Timer with HPET Timer	Enabled **Disabled**	Allow boot timer calculation with the high precision event timer.
PCI Express Dynamic Clock Gating	Enabled **Disabled**	Enable dynamic clock gating.

10.4.17 SCC Configuration Submenu

Feature	Options	Description
SCC Device Mode	ACPI Mode **PCI Mode**	Configure the Storage Control Cluster working mode.
SCC eMMC Support	Enable eMMC 4.5 Support Enable eMMC 4.41 Support **eMMC AUTO MODE** Disable	Enable SCC eMMC support and configure eMMC mode.
SCC 4.5 DDR50 eMMC Support	**Enabled** Disabled	Enable DDR50 eMMC support.
SCC 4.5 HS200 eMMC Support	Enabled **Disabled**	Enable HS200 eMMC support.
eMMC Secure Erase	Enabled **Disabled**	Enable eMMC secure erase support.
SCC SD Card Support	**Enabled** Disabled	Enable storage control cluster SD Card support.
SDR25 Support for SD Card	**Enabled** Disabled	Enable SDR25 Support for SD Card.
DDR50 Support for SD Card	Enabled **Disabled**	Enable DDR50 Support for SD Card.
MIPI Camera Support	**Disabled** Enabled for Windows Enabled for Linux	Enable or Disable support for ISP device, MIPI CSI interface and dedicated camera I2C bus. ISP can either be a part of IGD device (for Windows) or a separate device (for Linux).

10.4.18 PCI Subsystem Settings Submenu

Feature	Options	Description
PCI Latency Timer	**32**, 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
PCI-X Latency Timer	32, **64**, 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
VGA Palette Snoop	**Disabled** Enabled	Enable or disable VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enable or disable PCI device to generate SERR#.

Feature	Options	Description
Above 4G Decoding	**Disabled** Enabled	Enable or disable 64-bit capable devices to be decoded in above 4G address space (Only if system supports 64-bit PCI decoding).
SR-IOV Support	**Disabled** Enabled	If the System has a SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.
▶PCI Express Settings	Submenu	Opens the PCI Express Settings submenu
▶PCI Express GEN 2 Settings	Submenu	Opens the PCI Express Generation 2 Settings submenu. Not displayed on IC97.

10.4.18.1 PCI Express Settings

Feature	Options	Description
Relaxed Ordering	**Disabled** Enabled	Enables or Disables PCI Express Device Relaxed Ordering.
Extended Tag	**Disabled** Enabled	If Enabled allows Device to use 8-bit Tag field as a requester.
No Snoop	**Enabled** Disabled	Enables or Disables PCI Express Device No Snoop option.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 1096 Bytes	Set Maximum Payload of PCI Express Device or allow System BIOS to select the Value.
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 1096 Bytes	Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.
ASPM Support	**Disabled** Auto Force L0s	Set the ASPM Level: Force L0s – Force all links to L0s State. Auto – BIOS auto configure. Disable – Disables ASPM
Extended Synch	**Disabled** Enabled	If Enabled allows generation of Extended Synchronization patterns.
Link Training Retry	Disabled 2 3 **5**	Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

Feature	Options	Description
Link Training Timeout (uS)	10 - 10000	Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status Register. Value range from 10 to 10000 uS. Default: '1000'.
Unpopulated Links	**Keep Link ON** Disabled	In order to save power, software will disable unpopulated PCI Express links if this option set to 'Disable Link'.
Restore PCIE Registers	Enabled **Disabled**	On non-PCI Express aware OS's (Pre Windows Vista) some devices may not be correctly reinitialized after S3. Enabling this restores PCI Express device configurations on S3 resume. Warning: Enabling this may cause issues with other hardware after S3 resume.

10.4.18.2 PCI Express GEN 2 Settings

Feature	Options	Description
Completion Timeout	**Default** Shorter Longer Disabled	In device Functions that support Completion Timeout programmability, allows system software to modify the Completion Timeout value. 'Default' 50us to 50ms. If 'Shorter' is selected, software will use shorter timeout ranges supported by hardware. If 'Longer' is selected, software will use longer timeout ranges.
ARI Forwarding	**Disabled** Enabled	Set to 'Enabled', the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type1 Configuration Request into a Type0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
AtomicOp Requester Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this function initiates AtomicOp Requests only if Bus Master Enable bit is in the Command Register Set.
AtomicOp Egress Blocking	**Disabled** Enabled	If supported by hardware and set to 'Enabled', outbound AtomicOp Requests via Egress Ports will be blocked.
IDO Request Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated.
IDO Completion Enable	**Disabled** Enabled	If supported by hardware and set to 'Enable', this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated.
LTR Mechanism Enable	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this enables the Latency Tolerance Reporting (LTR) Mechanism.
End-End TLP Prefix Blocking	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this function will block forwarding of TLPs containing End-End TLP Prefixes.
Target Link Speed	**Auto** Force to 2.5 GT/s Force to 5.0 GT/s	If supported by hardware and set to 'Force to 2.5 GT/s' for Downstream Ports, this sets an upper limit an Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.
Clock Power Management	**Disabled** Enabled	If supported by hardware and set to 'Enabled', the device is permitted to use CLKREQ# signal for power management of Link clock in accordance to protocol defined in appropriate form factor specification.
Compliance SOS	**Disabled** Enabled	If supported by hardware and set to 'Enabled', this will force LTSSM to send SKP Ordered Sets between sequences when sending Compliance Pattern or Modified Compliance Pattern.

Feature	Options	Description
Hardware Autonomous Width	Enabled **Disabled**	If supported by hardware and set to 'Disabled', this will disable the hardware´s ability to change link width except for the purpose of correcting unstable link operation.
Hardware Autonomous Speed	Enabled **Disabled**	If supported by hardware and set to 'Disabled', this will disable the hardware´s ability to change link speed except speed rate reduction for the purpose of correcting unstable link operation.

10.4.19 Network Stack

Feature	Options	Description
Network Stack	Enabled **Disabled**	Enable or disable the UEFI network stack.
Ipv4 PXE Support	Enabled **Disabled**	Enable Ipv4 PXE boot support. If disabled IPV6 PXE boot option will not be created.
Ipv6 PXE Support	Enabled **Disabled**	Enable Ipv4 PXE boot support. If disabled IPV6 PXE boot option will not be created.
PXE Boot Wait Time	**0**-5	Wait time to press ESC to abort PXE Boot

10.4.20 CSM Submenu

Feature	Options	Description
Launch CSM	**Enabled** Disabled	Enable the Compatibility Support Module.
CSM16 Module Version	No option	Display CSM Module Version number.
Gate A20 Active	**Upon Request** Always	Configure legacy Gate A behavior.
Option ROM Messages	**Force BIOS** Keep Current	Enable Option ROM message
Boot Option Filter	UEFI and Legacy **Legacy Only** UEFI Only	Controls which devices / boot loaders the system should boot to.
Network	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and legacy Network option ROMs.
Storage	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and legacy Storage option ROMs.

Feature	Options	Description
Video	Do not launch UEFI only **Legacy only**	Controls the execution of UEFI and legacy Video option ROMs
Other PCI Devices	Do not launch **UEFI only** Legacy only	Controls the execution of UEFI and legacy option ROMs for any other PCI device different to Network, Video and Storage.

10.4.21 SDIO Submenu

Feature	Options	Description
SDIO Access Mode	**Auto** DMA PIO	Controls the SDIO Access mode to the device.

10.4.22 USB Submenu

Feature	Options	Description
USB Module Version	No option	
USB Devices	No option	Displays the detected USB devices.
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
xHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without xHCI hand-off support. The xHCI ownership change should be claimed by xHCI OS driver. Not displayed on BS/BP77.
EHCI Hand-off	**Disabled** Enabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI OS driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable Mass Storage Driver Support.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device start unit command timeout.
Device Power -Up Delay Selection	**Auto** Manual	Define maximum time a USB device might need before it properly reports itself to the host controller. Auto selects a default value which is 100ms for a root port or derived from the hub descriptor for a hub port.
Device Power -Up Delay in Seconds	1-40	Actual power-up delay value in seconds. Default: 5

10.4.23 Platform Trust Technology

Feature	Options	Description
fTPM	**Disable** Enable	Enable Trusted Platform Module support.

10.4.24 Security Configuration

Feature	Options	Description
TXE	**Enabled** Disabled	Enable Trusted Execution Engine.
TXE HMRFPO	Enable **Disable**	Enable Host ME Region Flash Protection Overwrite.
TXE Firmware Update	**Enabled** Disabled	Enable Firmware update.
TXE EOP Message	**Enabled** Disabled	Enable TXE End of Post Message.
TXE Unconfiguration Perform	No option	Execute a TXE unconfiguration command
Intel(R) Anti-Theft Technology Configuration	No option	
Intel(R) AT	Enable **Disable**	Enable Anti-Theft technology.
Intel(R) AT Platform PBA	Enable **Disable**	Enable Anti-Theft Platform Pre-boot Authentication.
Intel(R) AT Suspend Mode	Enable **Disable**	Enable Anti-Theft Suspend Mode.

10.4.25 Intel(R) Ethernet Connection I210 Submenu

At this submenu additionally to its title the MAC address is displayed at the end of the title.

Feature	Options	Description
► NIC Configuration	Submenu	Opens the NIC Configuration submenu.
Blink LEDs	**0**-15	The Ethernet LEDs will blink so many seconds long as entered.
UEFI Driver	No option	Displays the UEFI Driver version.
Adapter PBA	No option	Displays the Adapter PBA.

Feature	Options	Description
Chip Type	No option	Displays the type of the Chip in which the Ethernet controller is integrated.
PCI Device ID	No option	Displays the PCI Device ID of the Ethernet controller.
Bus:Device:Function	No option	Displays the PCI Bus:Device:Function number of the Ethernet controller.
Link Status	No option	Displays the Link Status.
MAC Address	No option	Displays the MAC Address.

10.4.25.1 NIC Configuration Submenu

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake on LAN	Disabled **Enabled**	Enables Wake on LAN (WOL) feature

10.4.26 Driver Health Submenu

Feature	Options	Description
▶Intel(R) PRO/1000	No option	Provides health status for the drivers/controllers connected to the system

10.4.26.1 Intel(R) PRO/1000 Submenu

Feature	Options	Description
Controller	No option	Provides health status for the drivers/controllers connected to the system

10.5 Chipset Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.5.1 North Bridge Submenu

Feature	Options	Description
Total Memory	No option	Total amount of memory detected by the system
Memory Slot 0	No option	Memory detected by the system on Slot 0
Memory Slot 1	No option	Memory detected by the system on Slot 1
Max TOLUD	**Dynamic** 2 GB 2.25 GB 2.5 GB 2.75 GB 3 GB	Maximum value for top of addressable memory below the 4GB marker.
Aperture Size	128 MB **256 MB** 512 MB	Sets the amount of ram that will be assigned for internal graphics use.
PAVC	Enable **Disable**	Enable or disable Protected Audio Video Control mode.

10.5.2 South Bridge Submenu

Feature	Options	Description
▶ Azalia HD Audio	Submenu	Azalia HD Audio Submenu.
▶ USB	Submenu	USB Submenu.
▶ PCI Express Configuration	Submenu	PCI Express Configuration Submenu.
High Precision Timer	**Enabled** Disabled	Enable High Precision Event Timer.
Serial IRQ	**Quiet** Continuous	Configure IRQ Serial Mode
CLKRUN# Logic	Enable **Disable**	Enable the CLKRUN# logic to stop the LPC clocks when possible. Requires Serial IRQ Mode to be set to Quiet as well.
Global SMI Lock	**Enabled** Disabled	Enable or Disable SMI Lock
BIOS Read/Write Protection	Enabled **Disabled**	Enable BIOS SPI Region read/write protection.
Isolate SMBus Segments	Never During POST **Always**	Allows to isolate the off-module/external SMBus segment from the on-module SMBus segment. This can be a workaround for non spec conform external SMBus devices.

10.5.2.1 Azalia HD Audio

Feature	Options	Description
LPE Audio Support	**Disable** LPE Audio PCI Mode LPE Audio ACPI Mode	Enable LPE Audio Support.
Audio Controller	**Enabled** Disabled	Enable Audio Controller.
Azalia Vci Enable	**Enabled** Disabled	Enable Azalia Vci.
Azalia Docking Support Enable	Enabled **Disabled**	Enable Azalia Docking support.
Azalia PME Enable	**Enabled** Disabled	Enable Azalia PME support.
Azalia HDMI™ Codec	**Enabled** Disabled	Enable Azalia HDMI™ Codec
HDMI™ Port B	**Enabled** Disabled	Enable HDMI™ Port B Audio.
HDMI™ Port C	Enabled **Disabled**	Enable HDMI™ Port C Audio.

10.5.2.2 USB Submenu

Feature	Options	Description
USB OTG Support	**Disabled** Enabled	Enable USB OTG support.
USB VBUS	**On** Off	VBUS should be On in Host Mode and it should be Off in OTG device Mode.
XHCI Mode	Enabled Disabled Auto **Smart Auto**	USB3.0 mode support on USB0, USB1, USB2 and USB3 ports. Enabled: USB ports will function correctly in BIOS but the ports on which the USB3.0 mode is enabled (see USB0 port USB3.0 item) will not function at all under OS if the USB3.0 OS driver is not installed. USB ports will not function in pre-OS time if USB3.0 Support in BIOS is disabled (see the USB3.0 Support in BIOS item). Disabled – USB ports will function in USB2.0 mode only. No USB3.0 OS driver required. The USB ports will be routed to EHCI1 controller. Auto: USB ports are initially set to operate in USB2.0 Mode and the USB3.0 OS driver (if available) will switch them to USB3.0 mode. If USB3.0 OS driver is not available, the ports will function correctly but will operate in USB2.0 mode. Smart Auto: The BIOS will store the USB mode set by the OS and at next boot the BIOS will set this previously used mode. At G3 boot (first boot after mechanical disconnection of the power supply) the USB ports will function identically as in Auto mode. This mode is not available when 'Disabled' is selected at USB3.0 Support in BIOS item.

Feature	Options	Description
USB2 Link Power Management	Disabled **Enabled**	Enable USB2 Link Power Management
USB 2.0(EHCI) Support	**Disabled** Enabled	Control USB EHCI (USB 2.0) functions.
USB Per Port Control	Disabled **Enabled**	Control each of the USB ports (0-3).
USB Port 0	Disabled **Enabled**	Enable Port 0
USB Port 1	Disabled **Enabled**	Enable Port 1
USB Port 2	Disabled **Enabled**	Enable Port 2
USB Port 3	Disabled **Enabled**	Enable Port 3

10.5.2.3 PCI Express Configuration Submenu

Feature	Options	Description
PCIe noncompliance Card	**Not Supported** Supported	Enable PCIe 1.0 Device Support
PCI Express Port 0	Disabled **Enabled**	Enable PCIe Port 0.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 0 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 1	Disabled **Enabled**	Enable PCIe Port 1.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 1 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 2	Disabled **Enabled**	Enable PCIe Port 2.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 2 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.
PCI Express Port 3	Disabled **Enabled**	Enable PCIe Port 3.
Speed	**Auto** Gen 2 Gen 1	Configure PCIe Port 3 Speed. This feature is visible only if PCIe noncompliance card option is set to "Not Supported". If the option is set to "supported", then the speed defaults to Gen 1.

10.6 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.6.1 Boot Settings Configuration

Feature	Options	Description
Setup Prompt Timeout	**1** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot (not recommended), 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Quiet Boot	**Disabled** Enabled	Disable displays normal POST diagnostic messages. Enable displays OEM logo instead of POST messages. Note: The default OEM logo is a dark screen.
Enter Setup If No Boot Device	No **Yes**	Select whether the setup menu should be started if no boot device is connected.
Enable Popup Boot Menu	No **Yes**	Sets whether the popup boot menu can be started via the F11 key.
Boot Priority Selection	Device Based **Type Based**	Sets between device and type based boot priority lists. The "Device Based" boot priority list allows you to select from a list of currently detected devices only. The "Type Based" boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the "Device Based" boot priority list might change dynamically in cases when devices are physically removed or added to the system. The "Type Based" boot menu is static and can only be changed by the user.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. Note: Only works with an ATX type power supply.
AT Shutdown Mode	System Reboot **Hot S5**	Determines the behavior of an AT-powered system after a shutdown.
Battery Support	**Auto (Battery Manager)** Battery-Only on I2C Bus Battery-Only on SMBus	Select the Battery System Support Bus.It can be I2C, SMBus or Auto.
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
Fast Boot	**Disabled** Enabled	Enable or disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS / legacy boot options.

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

10.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

10.7.1 Security Settings

Feature	Options	Description
Administrator Password	Enter password	Specifies the setup administrator password.
HDD Security Configuration		
List of all detected hard disks supporting the security feature set	Select device to open device security configuration submenu	

10.7.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

10.8 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen. You can display a Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Options	
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.
Boot Override	
List of all boot devices currently detected	Select device to leave setup menu and boot from the selected device. Only visible and active if Boot Priority Selection setup node is set to “Device Based”.

11 Additional BIOS Features

The conga-MA3/MA3E uses a congatec/AMI AptioEFI that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility (version 1.5.0 and later), which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as MA31R1xx, MA32R1xx, MC31R1xx or MC32R1xx, where:

- MA31 BIOS is for Modules with Baytrail Atom Single Channel Memory SoC,
- MA32 BIOS is for Modules with Baytrail Atom Dual Channel Memory SoC,
- MC31 BIOS is for Modules with Baytrail Celeron Single Channel Memory SoC
- MC32 BIOS is for Modules with Baytrail Celeron Dual Channel Memory SoC
- MA3E BIOS is for Modules with Baytrail Atom and ECC Memory
- R is the identifier for a BIOS ROM file
- 1 is the so called feature number
- xx is the major and minor revision number.

11.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

11.2 Supported Flash Devices

The conga-MA3/MA3E supports the following flash device:

- Winbond W25Q64JVSSIQ (8 MB)

The flash devices listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note "AN7_External_BIOS_Update.pdf" on the congatec website at www.congatec.com.

11.3 BIOS Security Features

The BIOS provides a setup administrator password that limits access to the BIOS setup menu.

11.4 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to 'lock' and 'unlock' drives using the security password. A 'locked' drive will be detected by the system, but no data can be accessed. Accessing data on a 'locked' drive requires the proper password to 'unlock' the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within four attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.