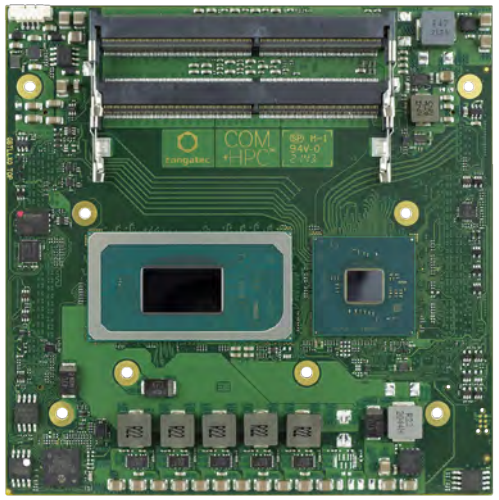

conga-HPC/cTLH

COM-HPC 1.10 Client Size B Module with 11th Generation Intel® Processors

User's Guide

Revision 1.00

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.01	2023-01-10	AEM	• Preliminary release
0.02	2023-07-26	AEM	• Renamed the title of the document • Updated the RoHS statement • Updated section 2.2 "Supported Operating Systems" • Corrected the temperature range of the CPU Tjunction in tables 2 "Commercial Variants" and 3 "Industrial Variants" • Updated section 3 "Block Diagram" • Added table 14 "I²C Address" • Added PCIe routing illustration to section 6.1.3 "PCIe Link Configuration" • Corrected the typographical error in section 11.4 "Supported Flash Devices" • Updated section 11.4 "Supported Flash Devices" • Updated section 7.1.10 "Enhanced Soft-Off State"
0.03	2023-11-30	AEM	• Added a note about optimal storage conditions to section 2.7 "Environmental Specifications" • Added note about the storage of congatec cooling solutions to section 4 "Cooling Solutions" • Added note about the PCIe width lenght for lanes 16 - 23 to section 6.1.3 "PCIe Link Configuration" • Updated the PCIe Link Configuration diagram in section 6.1.3 "PCIe Link Configuration" • Updated section 7.1.8 "Power Loss Control"
1.00	2024-04-08	AEM	• Updated section 1.1 "COM-HPC® Concept" • Added power consumption values to the tables in section 2.5 "Power Consumption" • Updated section 7.1 "congatec Board Controller (cBC)" • Updated section 10 "System Resources" • Official release

Preface

This user's guide provides information about the components, features, connectors and system resources available on the conga-HPC/cTLH. It is one of three documents that should be referred to when designing a COM-HPC® application. The other reference documents that should be used include the following:

- COM-HPC® Module Base Specification
- COM-HPC® Carrier Design Guide

These documents are available on the PICMG website at **www.picmg.org**. Additionally, check the restricted area of the congatec website at **www.congatec.com** and the website of the respective silicon vendor for relevant documents (Erratum, PCN, Sighting Reports and others).

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Note

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Terminology

Term	Description
CSA	Active Cooling Solution
CSP	Passive Cooling Solution
cTDP	Configurable TDP
DDI	Digital Display Interface
DTR	Dynamic Temperature Range
eDP	Embedded DisplayPort
GB	Gigabyte
GHz	Gigahertz
HDA	High Definition Audio
HSP	Heatspreader
kB	Kilobyte
kHz	Kilohertz
Mb	Megabit
MB	Megabyte
MHz	Megahertz
N.C	Not connected
N.A	Not available
PCH	Platform Controller Hub
PCIe	PCI Express
PEG	PCI Express Graphics
SATA	Serial ATA
TBD	To be determined
TDP	Thermal Design Power
TPM	Trusted Platform Module

Contents

List of Tables

1 Introduction

1.1 COM-HPC® Concept

COM-HPC® is an open standard defined specifically for high performance Computer-on-Modules (COMs) for embedded systems. The defined module types are client module with fixed input voltage, client module with variable input voltage and server module with fixed input voltage.

The COM-HPC® modules are available in the following form factors:

- Mini 95 mm x 70 mm
- Size A 95 mm x 120 mm
- Size B 120 mm x 120 mm
- Size C 160 mm x 120 mm
- Side D 160 mm x 160 mm
- Side E 200 mm x 160 mm

Table 1 COM-HPC® Interface Summary

Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
Ethernet	NBASE-T	1 / 2	1 / 2	1 / 1	
	KR/KX	N.A	0 / 2	2 / 8	
	SGMII	0 /2	N.A	N.A	
Storage	SATA	0 / 2	0 / 2	0 / 2	Pin is shared with PCIe on mini module
PCIe	Lane 0-47	1 / 16	4 / 48	8 / 48	Two PCIe reference clock output pairs required on mini module
	Lane 48-63	N.A	N.A	0 / 16	
	BMC	N.A	0 / 1	1 / 1	
USB	USB 2.0 Ports 0-7	6 / 8	4 / 8	4 / 8	Ports 0-5 (mini module) or ports 0-3 (server/client module) are used for USB 3.2 and USB4 if implemented.
	USB 3.2 Gen 1 or Gen 2	0 / 5	0 / 4	0 / 2	Requires one SuperSpeed Tx pair and one Rx pair per port
	USB 3.2 Gen 2x2	0 / 4	0 / 4	0 / 2	Requires two SuperSpeed Tx pairs and two Rx pairs per port
	USB4	0 / 4	0 / 4	0 / 2	USB4 ports use USB 3.2 Gen 2x2 ports

Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
SPI	eSPI	0 / 1	0 / 1	0 / 1	
	Boot SPI	1 / 1	1 / 1	1 / 1	
	General Purpose SPI	1 / 1	1 / 1	1 / 1	
BIOS Select	-	1 / 1	1 / 1	1/1	
Display	DDI	0 / 2	1 / 3	N.A	Additional display outputs may be available on the USB4 interface. On mini module, DDI pins are shared with USB4.
	eDP	0 / 1	0 / 1	N.A	
MIPI	DSI	0 / 1	0 / 1	N.A	
	CSI	N.A [1]	0 / 2	N.A	[1] Optional FFC connectors for MIPI-CSI on the mini module.
Audio	SoundWire	0 / 2	0 / 2	N.A	I2S pins may be used for one HDA port or two additional SoundWire ports for a total of up to four SoundWire ports.
	I2S	0 / 1	0 / 1	N.A	
Other Serial Ports	I2C	2 / 3	2 / 2	2 / 2	I2C0 and I2C1 for client and server modules. The mini module supports a third I2C port (I2C2/MDIO (for SGMII PHY setup).
	SMBus	1 / 1	1 / 1	1 / 1	
	IPMB	N.A	0 / 1	0 / 1	
	UART	0 / 2	0 / 2	1 / 2	
GPIO	-		12 / 12	12 / 12	
Miscellaneous	Watchdog Timer	0 / 1	0 / 1	0 / 1	
	Fan (PWM and tachometer)	1 / 1	1 / 1	1 / 1	
FuSa	FuSa set of signals	0 / 1	0 / 1	0 / 1	
Power Rails	VCC	12 / 12	28 / 28	28 / 28	
	VCC_5V-SBY	N.A	0 / 2	0 / 2	The mini module does not have 5V standby pins.
	VCC_RTC	1 / 1	1 / 1	1 / 1	
	GND	All	All	All	All available GND pins shall be used.
Connector	J1	1 / 1	1 / 1	1 / 1	
	J2	N.A	0 / 1	1 / 1	

1.2 Options Information

The conga-HPC/cTLH is currently available in 10 variants (seven commercial and three industrial). The table below shows the different configurations available.

Table 2 Commercial Variants

Part-No.		050800	050801	050802	050803
Processor		Intel® Core™ i7-11850HE 2.6 GHz, 8 Core™	Intel® Core™ i5-11500HE 2.6 GHz, 6 Core™	Intel® Core™ i3-11100HE 2.4 GHz, 4 Core™	Intel® Celeron® 6600HE 2.6 GHz, 2 Core™
Intel® Smart Cache		24 MB	12 MB	8 MB	8 MB
Max. Turbo Frequency		4.7 GHz	4.5 GHz	4.4 GHz	N.A
Chipset		QM580E	QM580E	HM570E	HM570E
Processor Graphics		Intel® UHD Graphics (32 EU)	Intel® UHD Graphics (32 EU)	Intel® UHD Graphics (16 EU)	Intel® UHD Graphics (16 EU)
GFX Base/Max. Dynamic Freq.		0.35/1.35 GHz	0.35/1.35 GHz	0.35/1.25 GHz	0.35/1.10 GHz
DDR4 Memory (ECC or non-ECC)		3200 MTps Dual Channel Non-ECC	3200 MTps Dual Channel Non-ECC	3200 MTps Dual Channel Non-ECC	3200 MTps Dual Channel Non-ECC
PCIe Lanes	Gen 3	20 lanes	20 lanes	16 lanes	16 lanes
	Gen 4	20 lanes	20 lanes	20 lanes	20 lanes
Ethernet Controller		Intel® I226-LM	Intel® I226-LM	Intel® I226-V	Intel® I226-V
Intel® TSN/TCC		TSN	TSN	N.A	N.A
CPU Use Condition [1]		Embedded	Embedded	Embedded	Embedded
CPU Tjunction	Min.	0°C	0°C	0°C	0°C
	Max.	100°C	100°C	100°C	100°C
DTR (Cold to Hot Transition) [2]		T_{Boot} + 70°C	T_{Boot} + 70°C	T_{Boot} + 70°C	T_{Boot} + 70°C
DTR (Hot to Cold Transition) [2]		T_{Boot} - 70°C	T_{Boot} - 70°C	T_{Boot} - 70°C	T_{Boot} - 70°C
Processor TDP (cTDP down)		45 (35) W	45 (35) W	45 (35) W	35 W
Compatible Carrier Board		conga-HPC/EVAL-Client carrier board for COM-HPC® client modules			

Note

1. *Intel SoC use conditions. For more information, see Intel documentation.*

2. *T_{Boot} is the boot temperature. If the Tjunction is not within the DTR range, you must reboot the system. See Intel documentation for more information.*

Part-No.		050813	050814	050815
Processor		Intel® Xeon® W-11865MLE 1.5 GHz, 8 Core™	Intel® Xeon® W-11555MLE 1.9 GHz, 6 Core™	Intel® Xeon® W-11155MLE 1.8 GHz, 4 Core™
Intel® Smart Cache		24 MB	12 MB	8 MB
Max. Turbo Frequency		4.5 GHz	4.4 GHz	3.1 GHz
Chipset		RM590E	RM590E	RM590E
Processor Graphics		Intel® UHD Graphics (32 EU)	Intel® UHD Graphics (32 EU)	Intel® UHD Graphics (16 EU)
GFX Base/Max. Dynamic Freq.		0.35/1.35 GHz	0.35/1.35 GHz	0.35/1.25 GHz
DDR4 Memory (ECC or non-ECC)		3200 MTps Dual Channel ECC or non-ECC	3200 MTps Dual Channel ECC or non-ECC	3200 MTps Dual Channel ECC or non-ECC
PCIe Lanes	Gen 3	20 lanes	20 lanes	20 lanes
	Gen 4	20 lanes	20 lanes	20 lanes
Ethernet Controller		Intel® I226-IT	Intel® I226-IT	Intel® I226-IT
Intel® TSN/TCC		TSN/TCC	TSN/TCC	TSN/TCC
Processor TDP (cTDP down)		25 W	25 W	25 W
CPU Use Condition [1]		Industrial (Commercial Temperature)	Industrial (Commercial Temperature)	Industrial (Commercial Temperature)
CPU Tjunction	Min.	0°C	0°C	0°C
	Max.	100°C	100°C	100°C
DTR (Cold to Hot Transition) [2]		T_{Boot} + 70°C	T_{Boot} + 70°C	T_{Boot} + 70°C
DTR (Hot to Cold Transition) [2]		T_{Boot} - 70°C	T_{Boot} - 70°C	T_{Boot} - 70°C
Compatible Carrier Board		conga-HPC/EVAL-Client carrier board for COM-HPC® client modules		

Note

1. *Intel SoC use conditions. For more information, see Intel documentation.*

2. *T_{Boot} is the boot temperature. If the Tjunction is not within the DTR range, you must reboot the system. See Intel documentation for more information.*

Table 3 Industrial Variants

Part-No.		050810	050811	050812
Processor		Intel® Xeon® W-11865MRE 2.6 GHz, 8 Core™	Intel® Xeon® W-11555MRE 2.6 GHz, 6 Core™	Intel® Xeon® W-11155MRE 2.4 GHz, 4 Core™
Intel® Smart Cache		24 MB	12 MB	8 MB
Max. Turbo Frequency		4.7 GHz	4.5 GHz	4.4 GHz
Chipset		RM590E	RM590E	RM590E
Processor Graphics		Intel® UHD Graphics (32 EU)	Intel® UHD Graphics (32 EU)	Intel® UHD Graphics (16 EU)
GFX Base/Max. Dynamic Freq.		0.35/1.35 GHz	0.35/1.35 GHz	0.35/1.25 GHz
DDR4 Memory (ECC or non-ECC)		3200 MTps dual channel ECC or non-ECC	3200 MTps dual channel ECC or non-ECC	3200 MTps dual channel ECC or non-ECC
PCIe Lanes	Gen 3	20 lanes	20 lanes	20 lanes
	Gen 4	20 lanes	20 lanes	20 lanes
Ethernet Controller		Intel® I226-IT	Intel® I226-IT	Intel® I226-IT
Intel® TSN/TCC		TSN/TCC	TSN/TCC	TSN/TCC
Processor TDP (cTDP down)		45 (35) W	45 (35) W	45 (35) W
CPU Use Condition [1]		Industrial (Extended Temperature)	Industrial (Extended Temperature)	Industrial (Extended Temperature)
CPU Tjunction	Min.	-40°C	-40°C	-40°C
	Max.	100°C	100°C	100°C
DTR (Cold to Hot Transition) [2]		T_{Boot} + 110°C	T_{Boot} + 110°C	T_{Boot} + 110°C
DTR (Hot to Cold Transition) [2]		T_{Boot} - 110°C	T_{Boot} - 110°C	T_{Boot} - 110°C
Compatible Carrier Board		conga-HPC/EVAL-Client carrier board for COM-HPC® client modules		

Note

1. *Intel SoC use conditions. For more information, see Intel documentation.*

2. *T_{Boot} is the boot temperature. If the Tjunction is not within the DTR range, you must reboot the system. See Intel documentation for more information.*

2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	COM-HPC® size B (120 x 120 mm) client connector pinout	
Processor	11th Generation Intel® Core i7,i5,i3, Celeron and Xeon H-processors	
Memory	Up to four memory sockets (located on the top and bottom side of the conga-HPC/cTLH). Supports - SO-DIMM ECC [1] or non-ECC DDR4 modules [2] - Data rates up to 3200 MT/s - Maximum 128 GB capacity (32 GB each)	
Chipset	Intel® 500 Series Chipset QM580E, HM570E [3] and RM590E PCH	
Audio	1 x I2S or HDA 2x Soundwire	
Ethernet	2x Intel® i226-LM/V/IT 2.5 GbE controller with support for TSN	
Graphics Options	Intel® Iris® Xᵉ (Gen. 12). Supports: - API (DirectX 12, Direct3D 12, Direct3D 2015, OpenGL 4.5, OpenCL 2.2) - Intel® QuickSync & Clear Video Technology HD (hardware accelerated video decode/encode/processing/transcode) - Up to four independent displays (see table 11 "Display Combination and Resolution")	
	3x DP++ 1x eDP Resolutions up to 4x4k @ 60 Hz	**NOTE**: *For TMDS support, a DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented on the carrier board.*
Peripheral Interfaces	1x MIPI-CSI-2 x4 lane 20x PCIe Gen. 3 lanes 20x PCIe Gen 4 lanes (1x PEG x16 and 1x PCIe x4) 8x USB [4] with up to: - 2x USB 4 - 2x USB 3.2 Gen 2x2 - 8x USB 2.0	2x SATA® 6 Gbps (with RAID 0/1/5/10 support) 2x UART (16C550 compatible) 12x GPIOs eSPI I²C (fast mode, multi-master) SMBus SPI
BIOS	AMI Aptio® V UEFI 2.6 firmware 32 MB serial SPI flash with congatec Embedded BIOS features	
Power Management	ACPI 5.0a compliant with battery support. S5e mode (see section 7.1.6 "Enhanced Soft-Off State") Deep Sx and Suspend to RAM (S3) Configurable TDP	
congatec Board Controller	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, hardware monitoring, fan control, I²C bus, power loss control	
Security	Discrete SPI Trusted Platform Module (Infineon SLB9670_VQ2.0); AES Instructions	

Note

1. *Only variants that feature the Intel RM590E support ECC memory.*
2. *See section 8.6 "SO-DIMM Population Rules"for a list of memory population rules.*
3. *Variants with Intel HM570E chipset do not support Intel VPro/AMT Technology.*
4. *The number of USB 2.0 ports available depends on how many USB 3.2/USB 4 ports you implement.*

2.2 Supported Operating Systems

The conga-HPC/cTLH supports the following operating systems.

- Microsoft® Windows® 10 (64-bit)
- Microsoft® Windows® 10 IoT Enterprise (64-bit)
- Linux (Ubuntu 20.04.1 LTS, kernel 5.15 or newer)
- Yocto
- Real Time Systems Hypervisor

Note

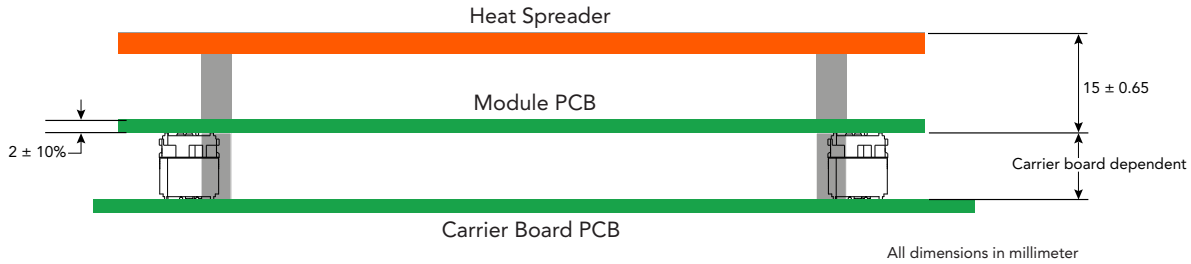
1. *The conga-HPC/cTLH supports only native UEFI Operating Systems. Legacy Operating Systems which require CSM (Compatibility Suppport Module) as part of the UEFI firmware are not supported anymore.*
2. *For Windows 10 installation, we recommend a minimum storage capacity of 20 GB. congatec will not offer technical support for systems with less than 20 GB storage space.*
3. *To support Intel i226 Ethernet controller in Linux by default, you need kernel 5.15 or newer.*

2.3 Mechanical Dimensions

The conga-HPC/cTLH has the following dimensions:

- length of 120 mm
- width of 120 mm

The overall height of the heatspreader is shown below:



2.4 Supply Voltage Standard Power

- 8.0 V – 20 V DC

2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for the conga-HPC/cTLH (COM-HPC client module with wide range input voltage).

Table 5 Overview of Type 6 Limitations

Power Rail	Module Pin Current Capability 20% Derated (A)	Input Range (V)	Min. Input (V)	Max. Module Input Power at Min. Input Voltage (W)	Assumed Conversion Efficiency (%)	Max. Module Load Power at Min. Input Voltage (W)
VCC	28 * 1.12 = 31.4	8 - 20	8	251	85	213
VCC_5V_SBY	1.12	4.75 - 5.25	4.75	5.32	100	5.32
VCC_RTC	1.12	2.00 - 3.30	2.30			

2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal within a timeframe of 0.1 ms to 20 ms. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-HPC/cTLH COM
- modified congatec carrier board
- conga-HPC/cTLH cooling solution
- Microsoft Windows 10 (64 bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool

Table 6 Measurement Description

The power consumption values were recorded during the following system states :

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	COM is powered by VCC_5V_SBY	
S5	COM is powered by VCC_5V_SBY	
S5e	COM is powered by VCC_5V_SBY	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement*

Table 7 Power Consumption Values (Nominal and TDP Down)

The table below provide additional information about the conga-HPC/cTLH power consumption. The values were recorded at various operating mode.

Nominal TDP (25/35/45 W TDP)

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (Ampere)					
					Variant	Cores	Freq. /Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5	S5e
050800	3 x 32 GB	A.3	GQTLR731	Windows 10	Intel® Core™ i7-11850HE	8	2.6 / 4.7	1.14	8.49	10.13	0.26	0.26	0.001
050801	3 x 16 GB	A.3	GQTLR731	Windows 10	Intel® Core™ i5-11500HE	6	2.6 / 4.5	0.99	7.95	8.90	0.28	0.21	0.001
050802	3 x 8 GB	A.3	GHTLR731	Windows 10	Intel® Core™ i3-11100HE	4	2.4 / 4.4	0.89	4.84	6.15	0.24	0.21	0.001
050803	3 x 8 GB	A.1	GHTLR731	Windows 10	Intel® Celeron® 6600HE	2	2.6 / N.A	1.01	2.15	2.44	0.30	0.21	0.001
050810	3 x 16 GB	A.3	GQTLR731	Windows 10	Intel® Xeon® W-11865MRE	8	2.6 / 4.7	1.06	8.56	10.81	0.28	0.21	0.001
050811	3 x 16 GB	A.1	GQTLR731	Windows 10	Intel® Xeon® W-11555MRE	6	2.6 / 4.5	1.07	5.97	7.09	0.28	0.21	0.001
050812	3 x 16 GB	A.3	GHTLR731	Windows 10	Intel® Xeon® W-11155MRE	4	2.4 / 4.4	0.87	3.51	4.84	0.26	0.21	0.001
050813	3 x 8 GB	A.3	GQTLR731	Windows 10	Intel® Xeon® W-11865MLE	8	1.5 / 4.5	0.84	8.77	11.86	0.24	0.21	0.001
050814	3 x 16 GB	A.3	GHTLR731	Windows 10	Intel® Xeon® W-11555MLE	6	1.9 / 4.4	0.98	6.06	8.42	0.27	0.21	0.001
050815	3 x 8 GB	A.3	GQTLR731	Windows 10	Intel® Xeon® W-11155MLE	4	1.8 / 3.1	0.91	2.80	3.35	0.24	0.21	0.001

TDP Down (35 W TDP)

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (Ampere)					
					Variant	Cores	Freq. /Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5	S5e
050800	3 x 32 GB	A.3	GQTLR731	Windows 10	Intel® Core™ i7-11850HE	8	2.6 / 4.7	1.14	8.29	9.57	0.26	0.26	0.001
050801	3 x 16 GB	A.3	GQTLR731	Windows 10	Intel® Core™ i5-11500HE	6	2.6 / 4.5	0.99	7.94	9.04	0.28	0.21	0.001
050802	3 x 8 GB	A.3	GHTLR731	Windows 10	Intel® Core™ i3-11100HE	4	2.4 / 4.4	0.89	5.01	6.01	0.24	0.21	0.001
050803	3 x 8 GB	A.1	GHTLR731	Windows 10	Intel® Celeron® 6600HE	2	2.6 / N.A	N.A	N.A	N.A	N.A	N.A	N.A
050810	3 x 16 GB	A.3	GQTLR731	Windows 10	Intel® Xeon® W-11865MRE	8	2.6 / 4.7	1.06	8.62	10.19	0.29	0.21	0.001
050811	3 x 16 GB	A.1	GQTLR731	Windows 10	Intel® Xeon® W-11555MRE	6	2.6 / 4.5	1.05	5.77	6.92	0.29	0.21	0.001
050812	3 x 16 GB	A.3	GHTLR731	Windows 10	Intel® Xeon® W-11155MRE	4	2.4 / 4.4	0.88	3.49	4.37	0.26	0.21	0.001
050813	3 x 8 GB	A.3	GQTLR731	Windows 10	Intel® Xeon® W-11865MLE	8	1.5 / 4.5	N.A	N.A	N.A	N.A	N.A	N.A
050814	3 x 16 GB	A.3	GHTLR731	Windows 10	Intel® Xeon® W-11555MLE	6	1.9 / 4.4	N.A	N.A	N.A	N.A	N.A	N.A
050815	3 x 8 GB	A.3	GQTLR731	Windows 10	Intel® Xeon® W-11155MLE	4	1.8 / 3.1	N.A	N.A	N.A	N.A	N.A	N.A

2.6 Supply Voltage Battery Power

Table 8 CMOS Battery Power Consumption (Commercial Variants)

RTC @	Voltage	Current
-10°C	3V DC	1.61 µA
20°C	3V DC	1.82 µA
70°C	3V DC	2.28 µA

Table 9 CMOS Battery Power Consumption (Industrial Variants)

RTC @	Voltage	Current
-50°C	3V DC	1.73 µA
20°C	3V DC	1.92 µA
95°C	3V DC	4.09 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-HPC/cTLH.*

2.7 Environmental Specifications

Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to 80°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to 85°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

1. *The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.*
2. *Humidity specifications are for non-condensing conditions.*
3. *Disable Turbo mode for industrial use condition.*

2.8 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

2.8.1 Module

For long-term storage of the conga-HPC/cTLH (more than six months), keep the conga-HPC/cTLH in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

Note

We do not recommend storing the conga-HPC/cTLH for more than five years under these conditions.

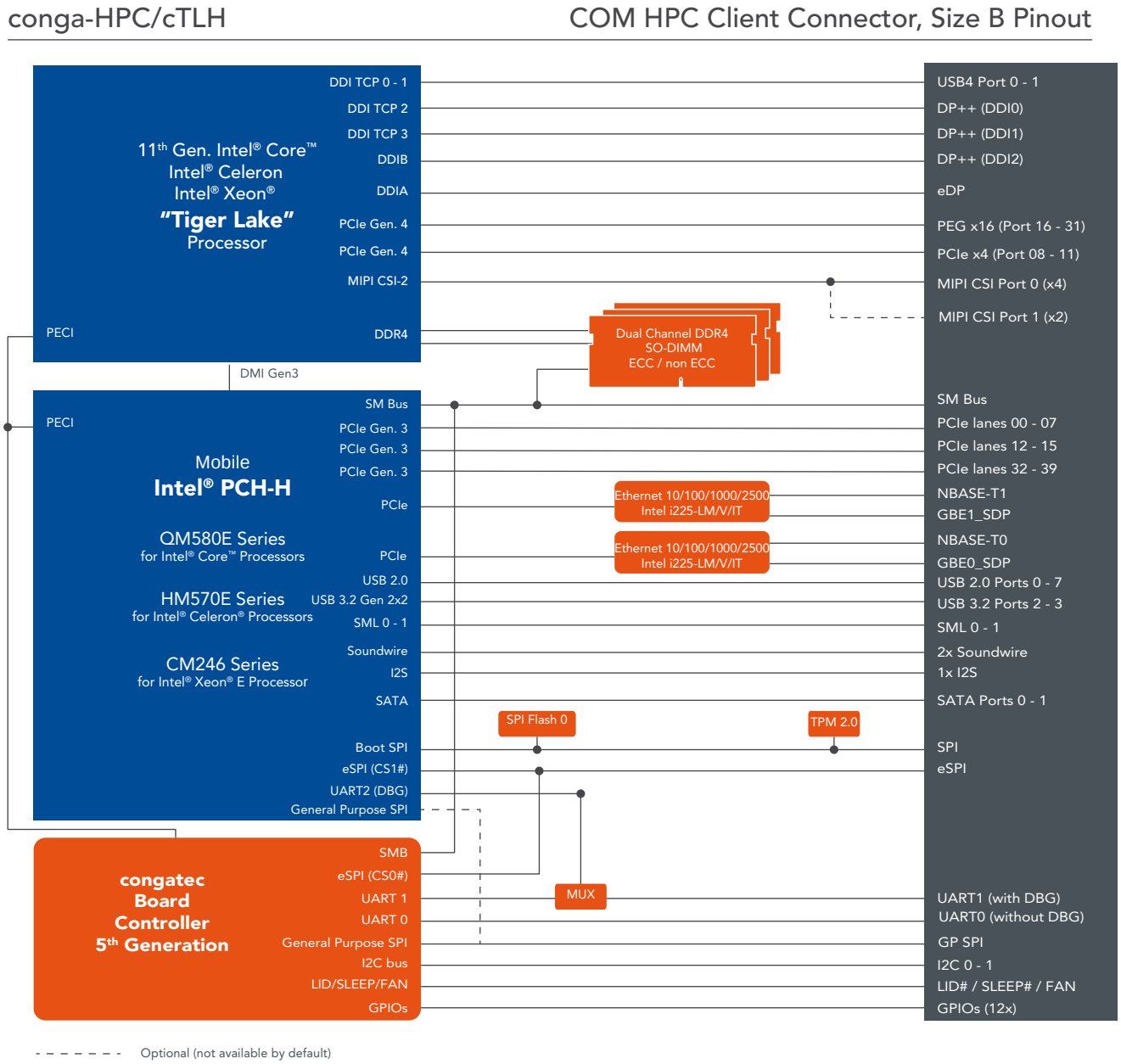
2.8.2 Cooling Solution

The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. For optimal cooling performance, do not store the heatspreaders/cooling solutions at temperatures below -20°C.

Note

1. *For temperatures between -10°C and -20°C, preheat the heatpipes before operation. Optionally, fill the heatpipes with acetone.*
2. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

3 Block Diagram



4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-HPC/cTLH. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 10 Cooling Solution Variants

	Cooling Solution	Part No	Description
1	CSA	050850	Active cooling solution with 2.7 mm bore-hole standoffs
		050851	Active cooling with M2.5 mm threaded standoffs
2	CSP	050852	Passive cooling solution with 2.7 mm bore-hole standoffs
		050853	Passive cooling solution with M2.5 mm threaded standoffs
3	HSP	050854	Heatspreader with 2.7 mm bore-hole standoffs
		050855	Heatspreader with M2.5 mm threaded standoffs

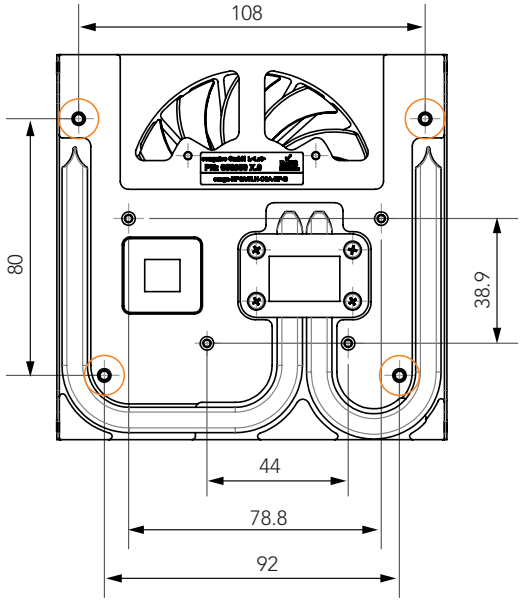
Note

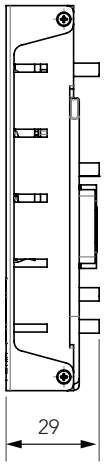
1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

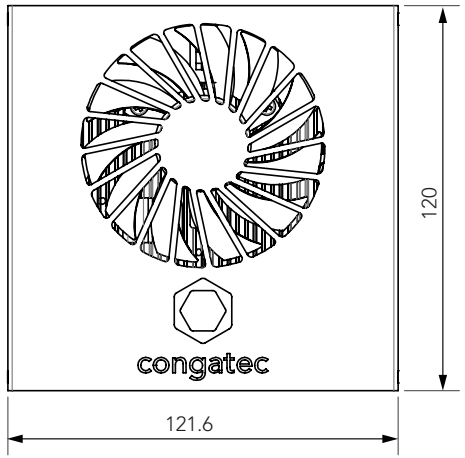
Caution

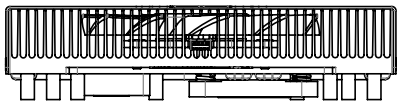
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. If your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

4.1 CSA Dimensions

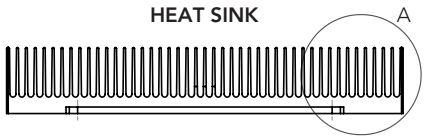


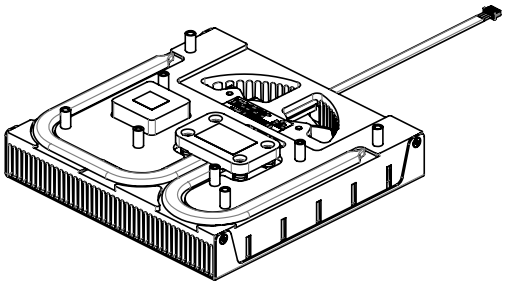


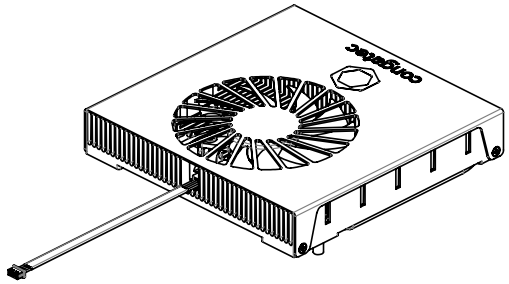


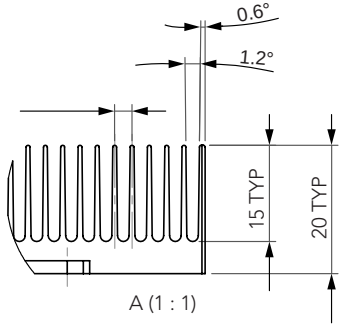


M2.5 threaded standoff
for threaded version
or
ø2.7 non-threaded standoff
for borehole version

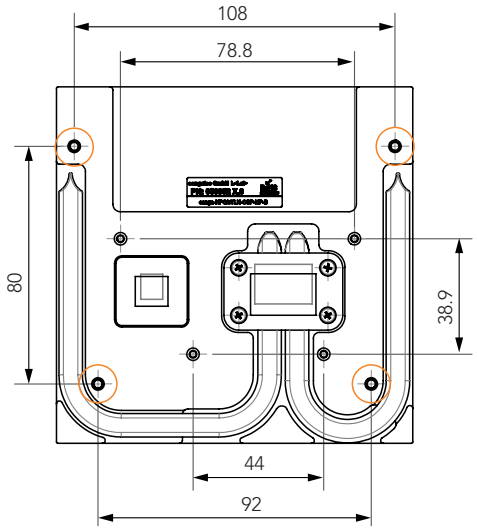


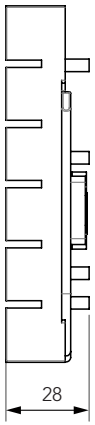


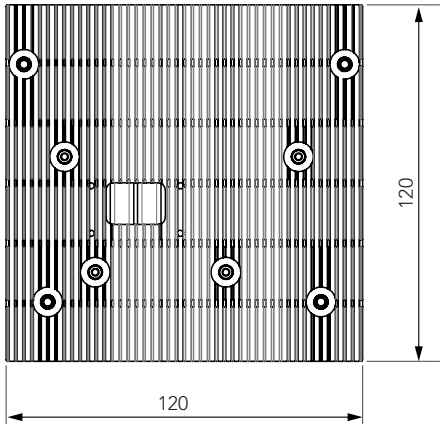


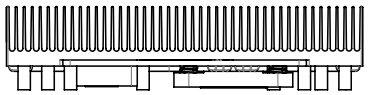


4.2 CSP Dimensions

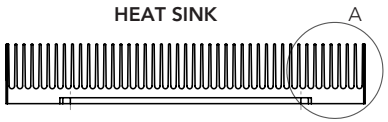


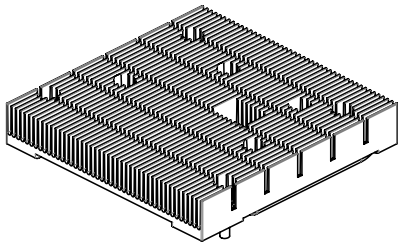


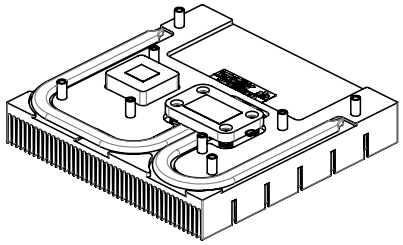


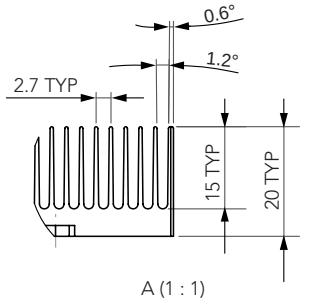


M2.5 threaded standoff
for threaded version
or
ø2.7 non-threaded standoff
for borehole version



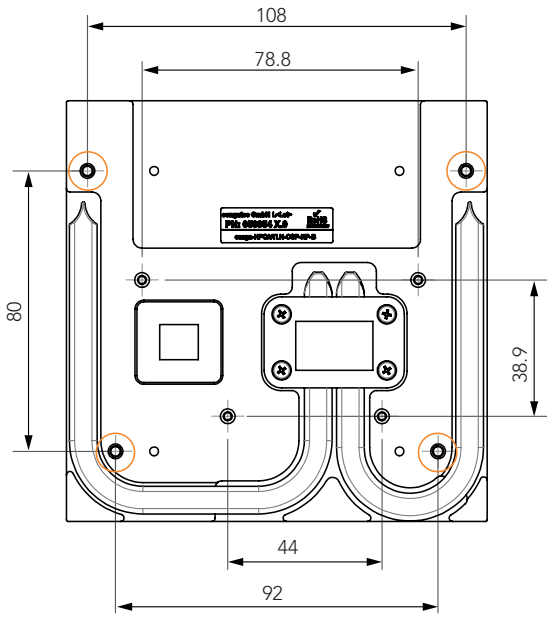


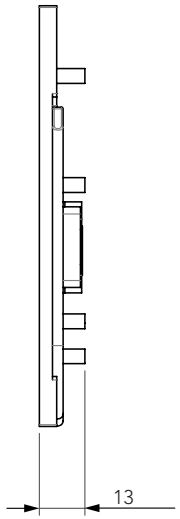


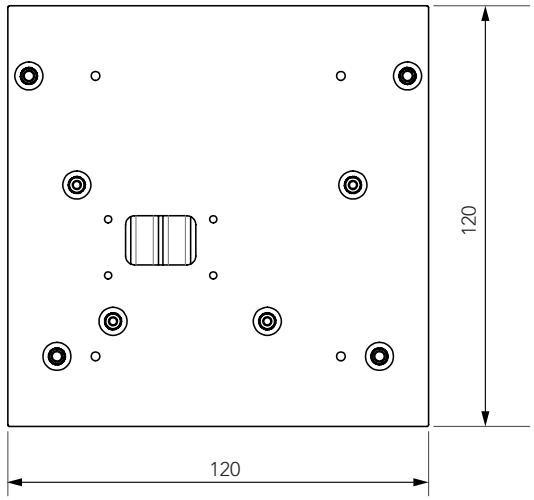


A (1 : 1)

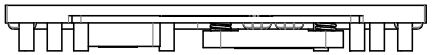
4.3 HSP Dimensions

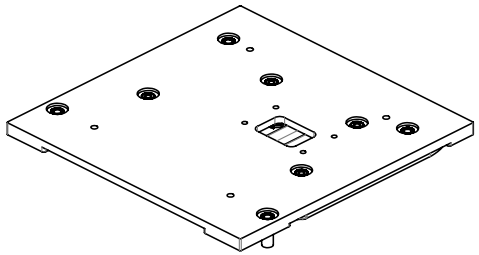


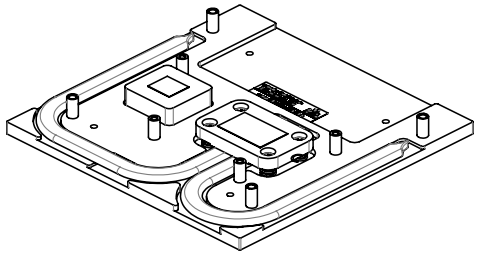




M2.5 threaded standoff
for threaded version
or
ø2.7 non-threaded standoff
for borehole version



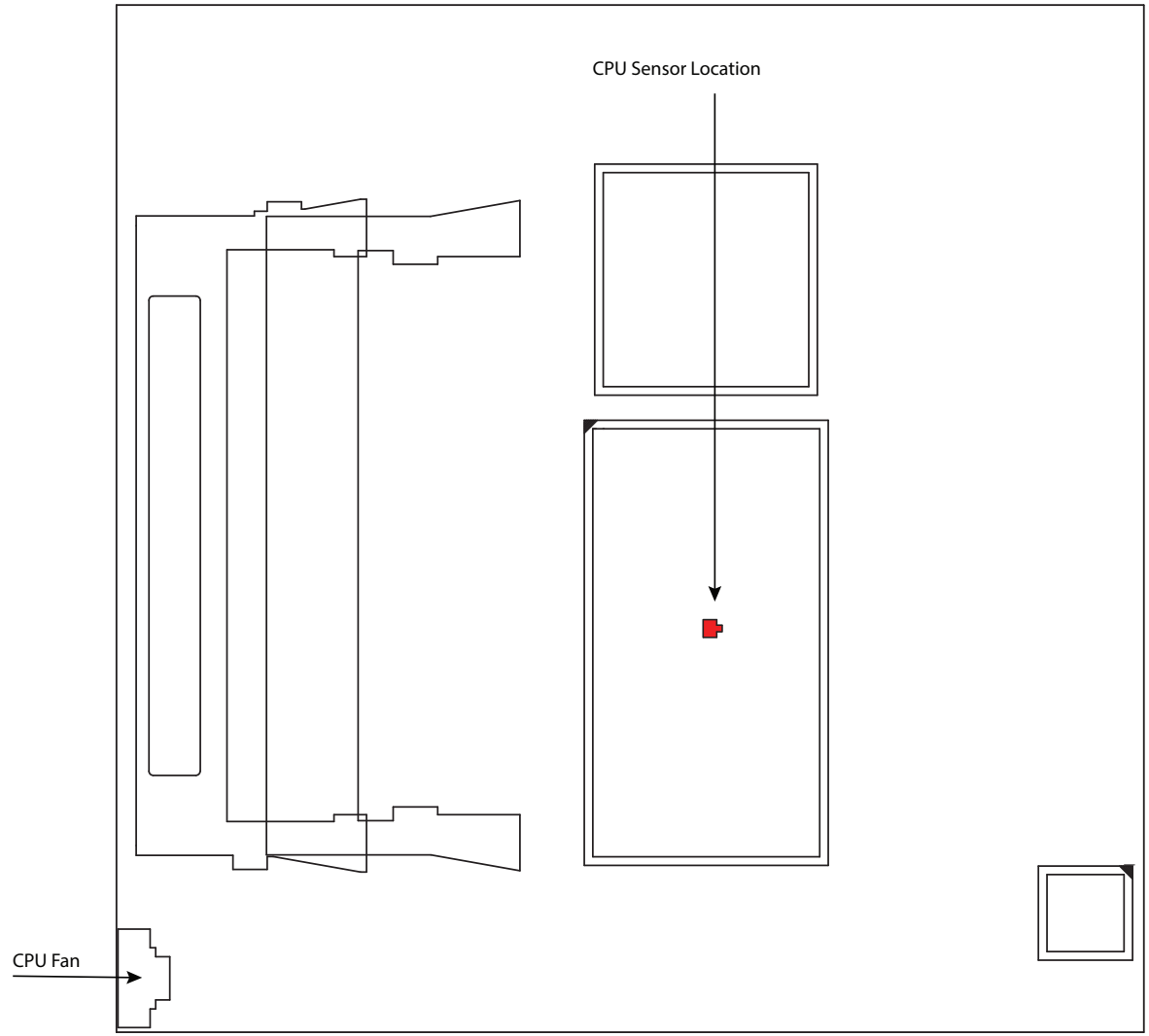




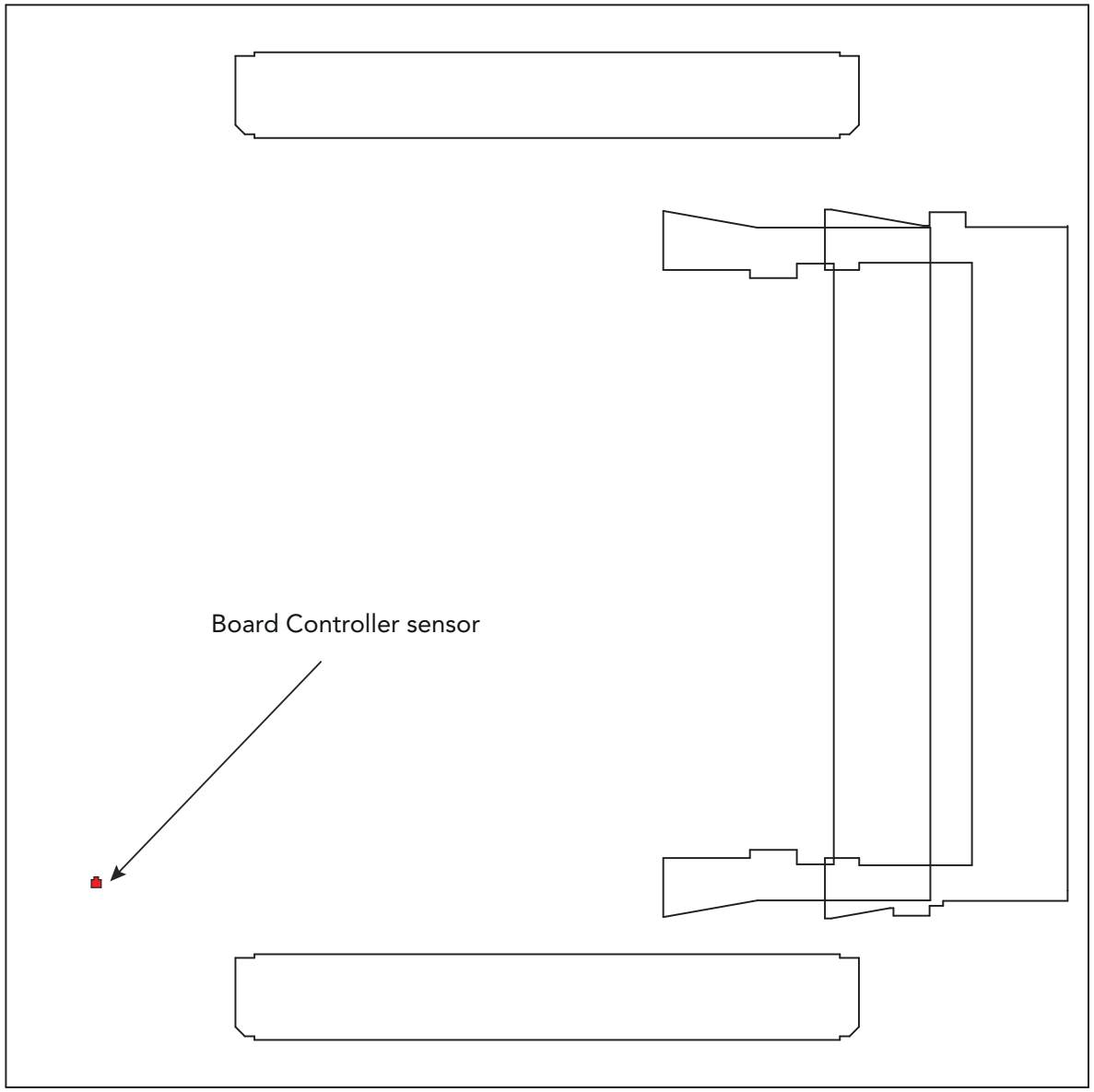
5 Onboard Temperature Sensors

The conga-HPC/cTLH features one sensors on the top-side of the module and one sensor on the bottom-side of the module.

5.1 Top-Side Sensor



5.2 Bottom-Side Sensor:



6 Connector Rows

The conga-HPC/cTLH is connected to the carrier board via two 400-pin connectors (COM-HPC® module pinout). These connectors are broken down into eight rows. The primary connector J1 consists of rows A, B, C, and D. The secondary connector J2 consists of rows E, F, G, and H. The following subsystems can be found on these connector rows.

6.1 PCI Express (PCIe)

The conga-HPC/cTLH offers the following PCIe lanes:

- up to 20 PCIe Gen 3 lanes via the chipset
- up to 20 PCIe Gen 4 lanes via the SoC

6.1.1 PCIe Gen 3

The conga-HPC/cTLH offers up to 20 PCIe Gen 3 lanes via the chipset. The PCIe interface supports:

- up to 8 GTps (Gen 3) speed
- a x1 link configuration by default
- a x2 or x4 link configuration via a customized BIOS firmware
- lane polarity inversion

Note

1. *Variants with HM570E chipset feature up to 16 PCIe Gen 3 lanes (PCIe 00–07, PCIe 12–15 and PCIe 36–39).*
2. *Maximum of 16 devices can be enabled.*

6.1.2 PCIe Gen 4

The conga-HPC/cTLH offers a 16-lane PCIe Gen 4 port (PEG x16) and a 4-lane PCIe Gen 4 port (PCIe x4) via the SoC. The PCIe ports support:

- PCI Express Specification 4.0, with up to 16 GT/s
- a x4 minimum link width
- graphics or non-graphics PCIe devices
- lane reversal

Note

1. *The PCIe x4 port does not support bifurcation.*
2. *You can configure PCIe x16 port for multiple devices at narrower widths.*
3. *The Gen 4 lanes can not be linked together with PCIe Gen 3 lanes.*

6.1.3 PCIe Link Configuration

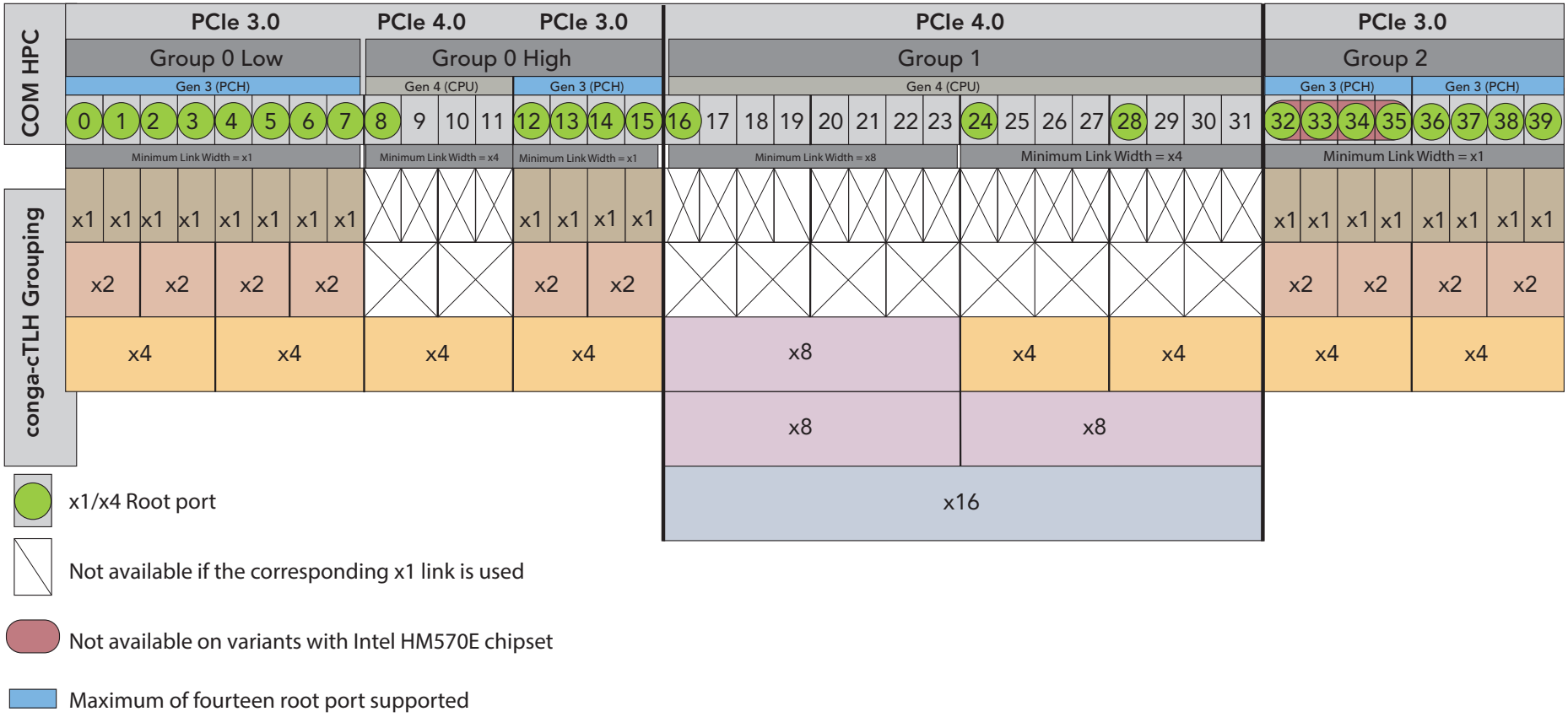
The possible link configurations are listed in the table below.

Table 11 PCIe Link

PCIe Lane	PCIe Generation	Link Configuration		COM-HPC® Grouping	Source	Comment
		Default	Optional			
PCIe 00 - 03	Gen 3	x1	x2, x4	Group 0 Low	Chipset	
PCIe 04 - 07	Gen 3	x1	x2, x4		Chipset	
PCIe 08 - 11	Gen 4	x4	-	Group 0 High	CPU	
PCIe 12 - 15	Gen 3	x1	x2, x4		Chipset	
PCIe 16 - 31	Gen 4	x16	x8, x4	Group 1	CPU	PEG port
PCIe 32 - 35	Gen 3	x1	x2, x4	Group 2	Chipset	Not available on variants with Intel HM570E chipset
PCIe 36 - 39	Gen 3	x1	x2, x4	Group 2	Chipset	

Note

PCIe lanes 16 -23 support only x8 configuration. These lanes do not support narrow width configuration.



6.2 NBASE-T Ethernet

The conga-HPC/cTLH offers two 2.5 Gigabit Ethernet interfaces via two onboard Intel® i226-LM/V/IT controllers. The interfaces supports:

- full-duplex operation at 10/100/1000/2500 Mbps
- half-duplex operation at 10/100 Mbps
- Audio Video Bridging
- Time Sensitive Networking [1]

Note

1. *Not supported in Windows Operating Systems*

6.3 Display

The conga-HPC/cTLH offers four dedicated display interfaces:

- three DP++
- an eDP

The table below shows the supported display combinations and resolutions.

Table 12 Display Combination and Resolution

Display 1 (DDI1)		Display 2 (DDI2)		Display 3 (DDI3)		Display 4	
Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution
DP++	4096x2304 @ 60 Hz, 36 bpp	DP++	4096x2304 @ 60 Hz, 36 bpp	DP++	4096x2304 @ 60 Hz, 36 bpp	eDP	4096x2304 @ 60 Hz, 24 bpp

Note

A single DP/eDP display supports maximum resolution of 5120x3200 @ 60 Hz.

6.3.1 DP++

The conga-HPC/cTLH offers three DP++ interfaces. Each interface supports:

- VESA DisplayPort Standard 1.2
- data rate of 1.62 GT/s, 2.97 GT/s and 5.4 GT/s on 1, 2 or 4 data lanes
- up to 4096x2304 resolutions at 60 Hz
- Various audio formats

6.3.2 eDP

The conga-HPC/cTLH offers an eDP interface. This interface supports:

- eDP 1.4 specification
- Spread-Spectrum Clocking
- eDP display authentication

Note

The eDP interface does not support HDCP.

6.4 MIPI-CSI2

The conga-HPC/cTLH offers a x4 MIPI-CSI2 interface by default. Optionally, the conga-HPC/cTLH can support up to two x2 MIPI-CSI2 interfaces.

Table 13 MIPI-CSI2 Options

Port/Signal	Configuration	
	Default	Assembly Option
Port A Clock	x4	x2
Port B Lane 0		
Port B Lane 1		
Port B Clock		x2
Port B Lane 2 / Port A Lane 1		
Port B Lane 3 / Port A Lane 2		

6.5 SATA

The conga-HPC/cTLH offers two SATA interfaces (SATA 0-1) on J1 connector. The interfaces support:

- independent DMA operation
- SATA specification 3.2
- data transfer rates up to 6.0 Gb/s
- AHCI mode using memory space and RAID mode
- Hot-plug detect

Note

The interfaces do not support IDE legacy mode using I/O space.

6.6 USB

The conga-HPC/cTLH offers up to:

- eight USB 2.0
- two USB 3.2 Gen 2x2
- two USB 4.0

Note

For each USB 3.2 Gen 2x2 or USB 4 port, you need one USB 2.0 port with corresponding USB 3.2/USB 4 SuperSpeed signals. Therefore, the available USB 2.0 port depends on how many USB 3.2/USB 4 ports you implement.

6.6.1 USB 2.0

The conga-HPC/cTLH offers up to eight USB 2.0 interfaces. The interfaces support:

- USB 2.0 specification
- High-Speed, Full-Speed and Low-Speed USB signaling
- data transfers of up to 480 Mbps (High-Speed mode)

6.6.2 USB 3.2

The conga-HPC/cTLH offers two USB 3.2 Gen 2x2 interfaces. The interfaces support:

- USB 3.2 specification
- wake up from S1-S4 sleep states (each wake up capable port must include USB 3.2 and USB 2.0 signaling)
- data transfers of up to 20 Gbps for USB 3.2 Gen 2x2 port (requires two differential signals and USB-C connector)
- SuperSpeed USB 20 Gbps, SuperSpeed USB 10 Gbps, SuperSpeed USB 5 Gbps, High-Speed, Full-Speed and Low-Speed traffic
- USB dual role
- USB debug port on all USB 3.2 capable ports

Note

For each USB 3.2 Gen 2x2 port, you need one USB 2.0 port with corresponding USB 3.2 SuperSpeed signals. Therefore, the available USB 2.0 ports depend on the number of USB 3.2 ports implemented.

6.6.3 USB 4.0

The conga-HPC/cTLH offers two USB 4.0 ports. These ports support:

- DisplayPort 1.4 specification
- USB-C specification
- data rate of up to 40 Gbps (requires two differential signals and USB-C connector)
- power saving when USB-C is disconnected
- wake capability on each host port
- USB dual role

Note

For each USB 4 port, you need one USB 2.0 port with corresponding USB 4 SuperSpeed signals. Therefore, the available USB 2.0 port depends on the number of USB 4 ports implemented.

6.7 Audio

The conga-HPC/cTLH offers two MIPI Soundwire audio, one Inter IC Sound (I2S) audio and one High Definition audio.

Note

The Soundwire and I2S are not verified because the Intel driver is currently not available. For verified audio interface, we recommend to use the High Definition audio.

6.8 General Purpose SPI

The conga-HPC/cTLH offers a general purpose SPI interface via the congatec Board Controller. Optionally, the conga-HPC/cTLH can route the general purpose SPI interface via the Intel® PCH (assembly option).

The interface offers up to two chip select pins.

6.9 eSPI

The conga-HPC/cTLH offers an eSPI interface for general purpose carrier board devices such as Super I/O, FPGAs, CPLDs and so on. The interface offers one chip select pin for carrier board device.

Unlike the LPC interface, the eSPI interface runs from a 1.8 V supply.

6.10 Boot SPI

The conga-HPC/cTLH offers a Boot SPI interface for carrier-based SPI BIOS flash device. The congatec onboard flash device (Winbond W25R256JVEIQ (256 Mb)) and TPM device are also connected to the Boot SPI interface.

The boot select configuration pins to select the carrier board flash device are described in section 6.11 “BIOS Flash Selection”.

Note

1. *The power supply to the carrier board SPI (VCC_BOOT_SPI) is 3.3 V.*
2. *The onboard SPI flash is disabled when the carrier board SPI flash is enabled.*

6.11 BIOS Flash Selection

The boot select pins BSEL0-BSEL2 are configured to load the firmware BIOS from the conga-HPC/cTLH by default. Optionally, you can configure these pins to load the boot firmware from the carrier board flash as described in the table below.

Table 14 BIOS Select Options

BSEL2	BSEL1	BSEL0	Boot Option
1	1	1	Boot from module SPI flash (default)
1	1	0	Boot from carrier board SPI flash

6.12 I²C

The conga-HPC/cTLH offers two I²C interfaces (I2C0 and I2C1) via the congatec Board Controller. The I²C bus is multi-master capable and can run at fast mode. However, the I²C bus is configured by default to run in standard mode (100 Kbps).

Table 15 Reserved I²C Address

8-bit Device Address	7-bit Device Address	Device	Description
0xAE	0x57	Carrier board EEPROM	Recommended for carrier board EEPROM
0x14	0x0A	congatec Board Controller	Reserved for battery management
0x16	0x0B	congatec Board Controller	Reserved for battery management

Note

You need the congatec CGOS driver and API to access the I²C interface.

6.13 SMBus

The conga-HPC/cTLH offers the System Management Bus (SMBus) via the congatec Board Controller by default. Optionally, you can route the SMBus signals from the SoC instead by configuring the routing in the BIOS setup menu.

The SMBus is not intended to be used by off-board non-system management devices. For more information about this subject, contact congatec technical support.

Table 16 Reserved SMBus Address

Onboard SMB Device	Address
Memory SPD	A0h - A6h
Memory thermal sensors	30h - 36h
Fan voltage controller	6Bh

Note

Make sure the address space of the carrier board SMBus devices does not overlap the address space of the module devices. For more information, refer to the COM-HPC® Module Base Specification and Carrier Design Guide.

6.14 GPIOs

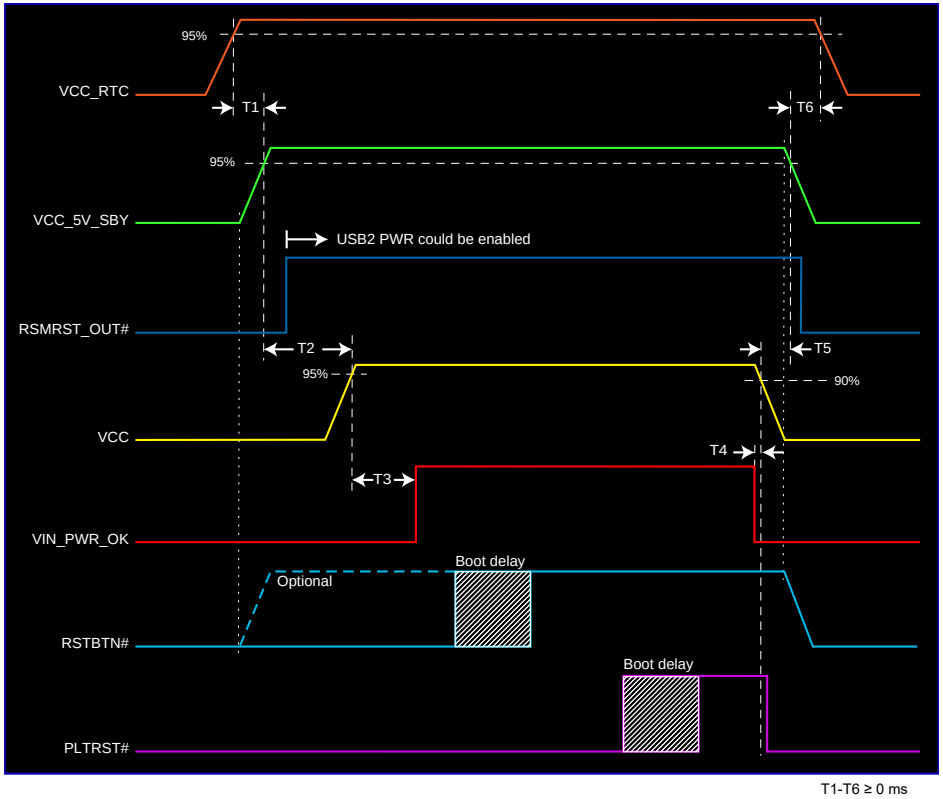
The conga-HPC/cTLH offers 12 general purpose inputs/outputs for custom system design. These GPIOs are controlled by the cBC.

6.15 UART

The conga-HPC/cTLH offers two standard 16C550 UARTs (UART0 and UART1) via the congatec Board Controller. The interfaces support hardware handshake, flow control and up to 115200 baud rate.

6.16 Power Control

The conga-HPC/cTLH operates with 8 V - 12 V wide input voltage range. Its power-up sequence is illustrated below.



The power control signals VIN_PWR_OK, RSTBTN#, SUS_S3# and PWRBTN# are described below. For more information, refer to the COM-HPC® Module Base Specification.

VIN_PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. Carrier board hardware should not drive VIN_PWR_OK low after the input power is stable. Hold RSTBTN# low instead to keep the module in a reset condition if necessary.

SUS_S3#

The SUS_S3# signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. To accomplish this, invert the signal on the carrier board with an inverter or transistor that is supplied by standby voltage.

With SUS_S3#, the conga-HPC/cTLU can control ATX-style power supplies.

Note

If you do not use an ATX power supply, do not connect the conga-HPC/cTLU pins SUS_S3#, VCC_5V_SBY and PWRBTN#.

PWRBTN#

When using ATX-style power supplies, PWRBTN# is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 100 kΩ resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

6.16.1 Power Management

ACPI

The conga-HPC/cTLH supports Advanced Configuration and Power Interface (ACPI) specification, revision 5.0a. It also supports Suspend to RAM (S3). For more information, see section 8.5 “ACPI Suspend Modes and Resume Events”.

DEEP Sx

The Deep Sx is a lower power state employed to minimize the power consumption while in S3/S4/S5. In the Deep Sx state, the system entry condition determines if the system context is maintained or not. All power is shut off except for minimal logic which supports limited set of wake events for Deep Sx.

The Deep Sx on resumption, puts system back into the state it is entered from. In other words, if Deep Sx state was entered from S3 state, then the resume path will place system back into S3.

S5e Power State

The conga-HPC/cTLH features a congatec proprietary Enhanced Soft-Off power state. See section 7.1.6 “Enhanced Soft-Off State” for more information.

7 Additional Features

This section describes the additional features the conga-HPC/cTLH offers.

7.1 congatec Board Controller (cBC)

The conga-HPC/cTLH is equipped with Microchip microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The board controller supports the following features:

- Board information
- General Purpose Input/Output (see section 6.14 “GPIOs”)
- Watchdog
- I²C bus (see section 6.12 “I²C”)
- SMBus (see section 6.13 “SMBus”)
- UART (see section 6.15 “UART”)
- Power loss control
- Port 80 debug information over USB power delivery pins
- Fan control
- Enhanced soft-off state (S5e)
- General Purpose SPI (see section 6.8 “General Purpose SPI”)
- User EEPROM space

7.1.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

7.1.2 Watchdog

The conga-HPC/cTLH is equipped with a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, see the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

Note

The conga-HPC/cTLH module does not support the watchdog NMI mode.

7.1.3 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The term "power loss" implies that all power sources, including the standby power are lost (G3 state). Once power loss (transition to G3) or shutdown (transition to S5) occurs, the board controller continuously monitors the standby power rail. If the standby voltage remains stable for 30 seconds, the cBC assumes the system was switched off properly. If the standby voltage is no longer detected within 30 seconds, the module considers this an AC power loss condition.

The power loss control feature has three different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to "ON".*
2. *The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.*
3. *The 30 seconds monitoring cycle applies only to the "Last State" power loss control mode.*

7.1.4 Port 80 Debug Information

The conga-HPC/cTLH board controller offers BIOS Port 80h debug information over the USB Power Delivery I²C Bus (USB_PD_I2C_DAT and USB_PD_I2C_CLK). The debug information is serialized and must be deserialized on the carrer board.

For information on how to deserialize and display the debug infromation on carrier board 7-segment displays, refer to the COM-HPC® Carrier Design Guide.

7.1.5 Fan Control

The conga-HPC/cTLH has additional signals and functions to further improve system management. One of these signals is FAN_PWMOUT, an output signal that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

1. *A four wire fan must be used to generate the correct speed readout.*

2. *For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express Design Guide.*

7.1.6 Enhanced Soft-Off State

The conga-HPC/cTLH supports an enhanced Soft-Off state (S5e)—a congatec proprietary low-power Soft-Off state. In this state, the CPU module switches off almost all the onboard logic to reduce the power consumption to absolute minimum (between 0.05 mA and 0.09 mA).

Refer to congatec application note AN36_S5e_Implementation.pdf for detailed description of the S5e state.

7.2 OEM BIOS Customization

The conga-HPC/cTLH is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

7.2.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

7.2.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

7.2.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

7.2.4 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

7.3 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery, the latest versions of the conga-HPC/cTLH BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I^2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface, contact your local sales representative.

7.4 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available on the congatec website.

7.5 Security Features

The conga-HPC/cTLH offers a discrete SPI TPM 2.0 (Infineon SLB9670VQ2.0) by default.

7.6 Suspend to Ram

The Suspend to RAM feature is available on the conga-HPC/cTLH.

8 conga Tech Notes

The conga-HPC/cTLH has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

8.1 Adaptive Thermal Monitor and Catastrophic Thermal Protection

Intel® Xeon, Core™ i7/i5/i3 and Celeron® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu "CPU submenu".

The Adaptive Thermal Monitor controls the processor temperature using two methods:

- Adjusting the processor's operating frequency and core voltage (EIST transitions)
- Modulating (start/stop) the processor's internal clocks at a duty cycle of 25% on and 75% off

When activated, the TCC causes both processor core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated. Clock modulation is activated if frequency and voltage adjustments are insufficient. Additional hardware, software driver, or operating system support is not required.

Intel®'s Core™ i7/i5/i3, Celeron® and Pentium® processors use the THERMTRIP# signal to shut down the system if the processor's silicon reaches a temperature of approximately 125°C. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

Note

1. *For THERMTRIP# to switch off the system automatically, use an ATX style power supply*

2. *The maximum operating temperature for Intel® Xeon, Core™ i7/i5/i3 and Celeron® processors is 100°C*

3. *To ensure that the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Xeon, Core™ i7/i5/i3 and Celeron® processor's respective datasheet can provide you with more information about this subject.*

8.2 Processor Performance Control

8.2.1 Intel® SpeedStep® Technology (EIST)

Intel® processors found on the conga-HPC/cTLH run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® Technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it is not being fully used. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime. The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that the power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

The 8th Generation Intel® Core™ processor family supports Intel Speed Shift, a new and energy efficient method for frequency control. This feature is also referred to as Hardware-controlled Performance States (HWP). It is a hardware implementation of the ACPI defined Collaborative Processor Performance Control (CPPC2) and is supported by newer operating systems (Win 8.1 or newer).

With this feature enabled, the processor autonomously selects performance states based on workload demand and thermal limits while also considering information provided by the OS e.g., the performance limits and workload history.

8.2.2 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology allows processor cores to run faster than the base operating frequency if it is operating below power, current, and temperature specification limits. Intel® Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state. The maximum frequency of Intel® Turbo Boost Technology depends on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost 2 Technology state depends on the workload and operating environment.

Any of the following can set the upper limit of Intel® Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency dynamically increases by 100 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached. For more information about Intel® Turbo Boost 2 Technology visit the Intel® website.

Note

1. *Only conga-HPC/cTLH variants that feature the Core™ i7, i5 and i3 processors support Intel® Turbo Boost 2 Technology. Refer to section 2.5 "Power Consumption" for information about the maximum turbo frequency available for each variant of the conga-HPC/cTLH*
2. *For real-time sensitive applications, disable EIST and Turbo Mode in the BIOS setup to ensure a more deterministic performance.*

8.3 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel VT and is verified on all current congatec x86 hardware.

Note

congatec supports RTS Hypervisor.

8.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to implement cooling decisions according to the demands of the application.

The conga-HPC/cTLH offers hardware-based support for passive and active cooling. Passive cooling is implemented in the Intel CPU via the Thermal Control Circuit (TCC) Activation Offset setting in the CPU configuration setup sub-menu. The TCC in the processor is activated at 100°C by default but can be lowered by the Activation Offset—for example, an activation offset of "10" will activate TCC at 90°C. ACPI OS support is not required. See section 8.1 "Adaptive Thermal Monitor and Catastrophic Thermal Protection" for more information.

The congatec board controller supports active cooling solution. The board controller controls the fan's speed based on the temperature readings of the CPU. This feature does not require ACPI OS support. The only software-controlled thermal trip point on conga-HPC/cTLH is the Critical Trip Point. The active or passive cooling policy should ensure that the CPU temperature does not reach this trip point. However, if the critical trip point is reached, the OS will shut down properly in order to prevent damage to the system.

Use the "critical trip point" setup node in the BIOS setup menu to determine the temperature threshold at which the system shuts down.

Note

The Automatic Critical Trip Point BIOS setting shuts down the system at 5°C above the maximum specified temperature of the processor.

8.5 ACPI Suspend Modes and Resume Events

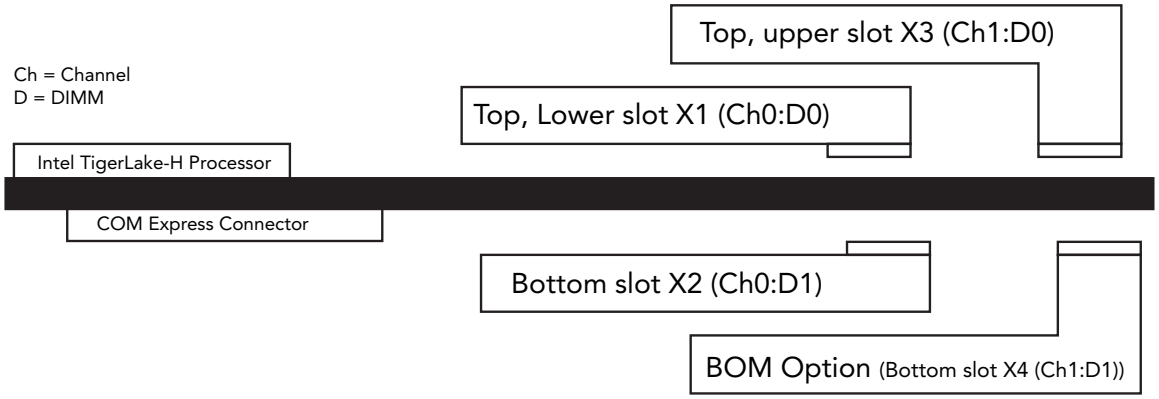
The conga-HPC/cTLH BIOS supports S3, S4 and S5. The table below lists the events that wake the system from S3 - S5.

Table 17 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5
Onboard LAN Event	Device driver must be configured for Wake On LAN support
SMB_ALERT#	Wakes unconditionally from S3-S5; S5e
PCI Express WAKE#	Wakes unconditionally from S3-S5
WAKE#	Wakes unconditionally from S3
PME#	Activate the wake up capabilities of a PCI device using Windows device manager configuration options for this device or set "Resume On PME#" to "Enabled" in the power setup menu
USB Mouse/Keyboard Event	When "Standby mode" is set to S3, USB hardware must be powered by standby power source. Set "USB Device Wakeup" from S3/S4 to "Enabled" in the ACPI setup menu (if setup node is available in BIOS setup program) In device manager, look for the keyboard/mouse devices. Go to the power management tab and check "Allow this device to bring the computer out of standby".
RTC Alarm	Activate and configure "Resume On RTC Alarm" in the power setup menu (only available in S5)
Watchdog Power Button Event	Wakes unconditionally from S3-S5

8.6 SO-DIMM Population Rules

The Intel TigerLake SoC featured on the conga-HPC/cTLH0 supports ECC and non-ECC DDR4 memory modules, up to 3200 MT/s. The diagram below shows the location of the memory slots on the conga-HPC/cTLH.



The following population rules must be observed:

- For single memory module, either of the top slots can be populated (Ch0:D0 or Ch1:D0).
- The top, lower slot (Ch0:D0) must be populated if the bottom slot (Ch0:D1) is populated.
  - The module will not boot (POST code 53) if only the bottom slot is populated in a single memory configuration.
  - The module will not boot (POST code 53) if the bottom slot and the top, upper slot are populated in a double memory configuration.
  - POST code "53" indicates that no memory module is detected.
- Use same DIMMs (same part numbers) in channel 0 (top, upper slot and bottom slot). Mixing DIMMs in this channel will reduce the speed to 2933 Mhz.
- No requirement to match DIMMs between channels.
- For best IA and GFx performance, use same memory capacity in a channel.
- ECC with non-interleave is not supported.

Table 18 Memory Population Compatibility

The table below shows the possible memory combinations and their corresponding results.

Top Lower Slot Channel 0, DIMM 0	Top Upper Slot Channel 1, DIMM 0	Bottom Lower Slot Channel 0, DIMM 1	Bottom Upper Slot (BOM Option)	Result
x	x	x	x	OK
x	x	x	–	OK
x	x	–	–	OK
x	x	–	x	OK
x	–	x	x	OK
x	–	x	–	OK
x	–	–	x	OK
x	–	–	–	OK
–	x	–	–	OK
–	–	x	–	Boot error (POST Code 53)
–	x	x	–	Boot error (POST Code 53)
–	–	x	x	Boot error (POST Code 53)
–	x	x	x	Boot error (POST Code 53)

9 Signal Descriptions and Pinout Tables

This section describes the signals found on the conga-HPC/cTLH. The pinout of the module complies with PICMG® COM-HPC®, revision 1.0. The table below describes the terminology used in this section. The PU/PD column indicates if a pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors. Only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 19 Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
T	Higher voltage tolerance
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Bi-directional 3.3V tolerant active in standby state
LV_DIFF	Low voltage differential signal (under 3.3 V)
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
V_{OL}	Output low voltage
V_{OH}	Output high voltage
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0 and 3.0
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
KR	10GBASE-KR compatible signal
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the carrier board.

9.1 Connectors Signal Descriptions

Table 20 Primary Connector (J1) Pinout

Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A01	VCC	B01	VCC	C01	VCC	D01	VCC
A02	VCC	B02	PWRBTN#	C02	RSTBTN#	D02	VCC
A03	VCC	B03	VCC	C03	VCC	D03	VCC
A04	VCC	B04	THERMTRIP#	C04	CARRIER_HOT#	D04	VCC
A05	VCC	B05	VCC	C05	VCC	D05	VCC
A06	VCC	B06	TAMPER#	C06	VIN_PWROK	D06	VCC
A07	VCC	B07	VCC	C07	VCC	D07	VCC
A08	VCC	B08	SUS_S3#	C08	SUS_S4_S5#	D08	VCC
A09	VCC	B09	VCC	C09	VCC	D09	VCC
A10	GND	B10	WD_STROBE#	C10	GND	D10	WAKE0#
A11	BATLOW#	B11	WD_OUT	C11	FAN_PWMOUT	D11	WAKE1#
A12	PLTRST#	B12	GND	C12	FAN_TACHIN	D12	GND
A13	GND	B13	USB5-	C13	GND	D13	USB1-
A14	USB7-	B14	USB5+	C14	USB3-	D14	USB1+
A15	USB7+	B15	GND	C15	USB3+	D15	GND
A16	GND	B16	USB4-	C16	GND	D16	USB0-
A17	USB6-	B17	USB4+	C17	USB2-	D17	USB0+
A18	USB6+	B18	GND	C18	USB2+	D18	GND
A19	GND	B19	I2S_LRCLK/SNDW_CLK3 [3]	C19	GND	D19	DDI0_SDA_AUX- [3]
A20	DDI1_SDA_AUX-	B20	I2S_DOUT/SNDW_DAT3	C20	SNDW_DMIC_CLK1	D20	DDI0_SCL_AUX+ [3]
A21	DDI1_SCL_AUX+	B21	I2S_MCLK	C21	SNDW_DMIC_DAT1	D21	GND
A22	GND	B22	I2S_DIN/SNDW_DAT2	C22	GND	D22	DDI0_PAIR0-
A23	DDI1_PAIR0-	B23	I2S_CLK/SNDW_CLK2	C23	SNDW_DMIC_CLK0	D23	DDI0_PAIR0+
A24	DDI1_PAIR0+	B24	VCC_5V_SBY	C24	SNDW_DMIC_DAT0	D24	GND
A25	GND	B25	USB67_OC#	C25	GND	D25	DDI0_PAIR1-
A26	DDI1_PAIR1-	B26	USB45_OC#	C26	DDI0_DDC_AUX_SEL	D26	DDI0_PAIR1+
A27	DDI1_PAIR1+	B27	USB23_OC#	C27	DDI1_DDC_AUX_SEL	D27	GND
A28	GND	B28	USB01_OC#	C28	DDI0_HPD	D28	DDI0_PAIR2-
A29	DDI1_PAIR2-	B29	SML1_CLK	C29	DDI1_HPD	D29	DDI0_PAIR2+
A30	DDI1_PAIR2+	B30	SML1_DAT	C30	eDP_HPD	D30	GND
A31	GND	B31	PMCALERT#	C31	eDP_VDD_EN	D31	DDI0_PAIR3-
A32	DDI1_PAIR3-	B32	SML0_CLK	C32	eDP_BKLT_EN	D32	DDI0_PAIR3+
A33	DDI1_PAIR3+	B33	SML0_DAT	C33	eDP_BKLTCTL	D33	GND
A34	GND	B34	USB_PD_ALERT#	C34	GND	D34	AC_PRESENT
A35	eDP_AUX-	B35	USB_PD_I2C_CLK	C35	USB1_AUX-	D35	RSVD
A36	eDP_AUX+	B36	USB_PD_I2C_DAT	C36	USB1_AUX+	D36	GND

A37	GND	B37	USB_RT_ENA	C37	GND	D37	USB1_SSTX0-
A38	eDP_TX0-	B38	USB1_LSRX [3]	C38	USB1_SSRX0-	D38	USB1_SSTX0+
A39	eDP_TX0+	B39	USB1_LSTX	C39	USB1_SSRX0+	D39	GND
A40	GND	B40	USB0_LSRX [3]	C40	GND	D40	USB1_SSTX1-
A41	eDP_TX1-	B41	USB0_LSTX	C41	USB1_SSRX1-	D41	USB1_SSTX1+
A42	eDP_TX1+	B42	GND	C42	USB1_SSRX1+	D42	GND
A43	GND	B43	USB0_AUX-	C43	GND	D43	USB0_SSTX0-
A44	eDP_TX2-	B44	USB0_AUX+	C44	USB0_SSRX0-	D44	USB0_SSTX0+
A45	eDP_TX2+	B45	LID#	C45	USB0_SSRX0+	D45	GND
A46	GND	B46	SLEEP#	C46	GND	D46	USB0_SSTX1-
A47	eDP_TX3-	B47	VCC_BOOT_SPI	C47	USB0_SSRX1-	D47	USB0_SSTX1+
A48	eDP_TX3+	B48	BOOT_SPI_CS#	C48	USB0_SSRX1+	D48	GND
A49	GND	B49	BSEL0	C49	GND	D49	SATA0_RX-
A50	eSPI_IO0	B50	BSEL1	C50	BOOT_SPI_IO0 [3]	D50	SATA0_RX+
A51	eSPI_IO1	B51	BSEL2	C51	BOOT_SPI_IO1	D51	GND
A52	eSPI_IO2	B52	eSPI_ALERT0#	C52	BOOT_SPI_IO2	D52	SATA0_TX-
A53	eSPI_IO3	B53	eSPI_ALERT1#	C53	BOOT_SPI_IO3	D53	SATA0_TX+
A54	eSPI_CLK	B54	eSPI_CS0#	C54	BOOT_SPI_CLK	D54	GND
A55	GND	B55	eSPI_CS1#	C55	GND	D55	SATA1_RX-
A56	PCIe_CLKREQ0_LO#	B56	eSPI_RST#	C56	PCIe_REFCLK0_HI-	D56	SATA1_RX+
A57	PCIe_CLKREQ0_HI#	B57	GND	C57	PCIe_REFCLK0_HI+	D57	GND
A58	GND	B58	PCIe_BMC_RX- [1]	C58	GND	D58	SATA1_TX-
A59	PCIe_BMC_TX- [1]	B59	PCIe_BMC_RX+ [1]	C59	PCIe_REFCLK0_LO-	D59	SATA1_TX+
A60	PCIe_BMC_TX+ [1]	B60	GND	C60	PCIe_REFCLK0_LO+	D60	GND
A61	GND	B61	PCIe08_RX-	C61	GND	D61	PCIe00_TX-
A62	PCIe08_TX-	B62	PCIe08_RX+	C62	PCIe00_RX-	D62	PCIe00_TX+
A63	PCIe08_TX+	B63	GND	C63	PCIe00_RX+	D63	GND
A64	GND	B64	PCIe09_RX-	C64	GND	D64	PCIe01_TX-
A65	PCIe09_TX-	B65	PCIe09_RX+	C65	PCIe01_RX-	D65	PCIe01_TX+
A66	PCIe09_TX+	B66	GND	C66	PCIe01_RX+	D66	GND
A67	GND	B67	PCIe10_RX-	C67	GND	D67	PCIe02_TX-
A68	PCIe10_TX-	B68	PCIe10_RX+	C68	PCIe02_RX-	D68	PCIe02_TX+
A69	PCIe10_TX+	B69	GND	C69	PCIe02_RX+	D69	GND
A70	GND	B70	PCIe11_RX-	C70	GND	D70	PCIe03_TX-
A71	PCIe11_TX-	B71	PCIe11_RX+	C71	PCIe03_RX-	D71	PCIe03_TX+
A72	PCIe11_TX+	B72	GND	C72	PCIe03_RX+	D72	GND
A73	GND	B73	PCIe12_RX-	C73	GND	D73	PCIe04_TX-
A74	PCIe12_TX-	B74	PCIe12_RX+	C74	PCIe04_RX-	D74	PCIe04_TX+
A75	PCIe12_TX+	B75	GND	C75	PCIe04_RX+	D75	GND
A76	GND	B76	PCIe13_RX-	C76	GND	D76	PCIe05_TX-
A77	PCIe13_TX-	B77	PCIe13_RX+	C77	PCIe05_RX-	D77	PCIe05_TX+

A78	PCIe13_TX+	B78	GND	C78	PCIe05_RX+	D78	GND
A79	GND	B79	PCIe14_RX-	C79	GND	D79	PCIe06_TX-
A80	PCIe14_TX-	B80	PCIe14_RX+	C80	PCIe06_RX-	D80	PCIe06_TX+
A81	PCIe14_TX+	B81	GND	C81	PCIe06_RX+	D81	GND
A82	GND	B82	PCIe15_RX-	C82	GND	D82	PCIe07_TX-
A83	PCIe15_TX-	B83	PCIe15_RX+	C83	PCIe07_RX-	D83	PCIe07_TX+
A84	PCIe15_TX+	B84	GND	C84	PCIe07_RX+	D84	GND
A85	GND	B85	TEST#	C85	GND	D85	NBASET0_MDI0-
A86	VCC_RTC	B86	RSMRST_OUT#	C86	SMB_CLK	D86	NBASET0_MDI0+
A87	SUS_CLK	B87	UART1_TX	C87	SMB_DAT	D87	GND
A88	GPIO_00	B88	UART1_RX	C88	SMB_ALERT# [3]	D88	NBASET0_MDI1-
A89	GPIO_01	B89	UART1_RTS#	C89	UART0_TX	D89	NBASET0_MDI1+
A90	GPIO_02	B90	UART1_CTS#	C90	UART0_RX	D90	GND
A91	GPIO_03	B91	IPMB_CLK	C91	UART0_RTS#	D91	NBASET0_MDI2-
A92	GPIO_04	B92	IPMB_DAT	C92	UART0_CTS#	D92	NBASET0_MDI2+
A93	GPIO_05	B93	GP_SPI_MOSI	C93	I2C0_CLK	D93	GND
A94	GPIO_06	B94	GP_SPI_MISO	C94	I2C0_DAT	D94	NBASET0_MDI3-
A95	GPIO_07	B95	GP_SPI_CS0#	C95	I2C0_ALERT#	D95	NBASET0_MDI3+
A96	GPIO_08	B96	GP_SPI_CS1#	C96	I2C1_CLK	D96	GND
A97	GPIO_09	B97	GP_SPI_CS2# [2]	C97	I2C1_DAT	D97	NBASET0_LINK_MAX#
A98	GPIO_10	B98	GP_SPI_CS3# [2]	C98	NBASET0_SDP	D98	NBASET0_LINK_MID#
A99	GPIO_11	B99	GP_SPI_CLK	C99	NBASET0_CTREF [1]	D99	NBASET0_LINK_ACT#
A100	TYPE0	B100	GP_SPI_ALERT#	C100	TYPE1	D100	TYPE2

Note

1. *Not connected*
2. *Not supported*
3. *Bootstrap signals*

Table 21 Secondary Connector (J2) Pinout

Pin	Row E	Pin	Row F	Pin	Row G	Pin	Row H
E1	RAPID_SHUTDOWN	F1	RSVD [1]	G1	RSVD [1]	H1	GND
E2	GND	F2	RSVD [1]	G2	GND	H2	USB2_SSTX0-
E3	DDI2_SDA_AUX-	F3	RSVD [1]	G3	USB2_SSRX0-	H3	USB2_SSTX0+
E4	DDI2_SCL_AUX+	F4	RSVD [1]	G4	USB2_SSRX0+	H4	GND
E5	GND	F5	RSVD [1]	G5	GND	H5	USB2_SSTX1-
E6	DDI2_PAIR0-	F6	RSVD [1]	G6	USB2_SSRX1-	H6	USB2_SSTX1+
E7	DDI2_PAIR0+	F7	RSVD [1]	G7	USB2_SSRX1+	H7	GND
E8	GND	F8	RSVD [1]	G8	GND	H8	USB3_SSTX0-
E9	DDI2_PAIR1-	F9	RSVD [1]	G9	USB3_SSRX0-	H9	USB3_SSTX0+
E10	DDI2_PAIR1+	F10	RSVD [1]	G10	USB3_SSRX0+	H10	GND
E11	GND	F11	RSVD [1]	G11	GND	H11	USB3_SSTX1-
E12	DDI2_PAIR2-	F12	RSVD [1]	G12	USB3_SSRX1-	H12	USB3_SSTX1+
E13	DDI2_PAIR2+	F13	RSVD [1]	G13	USB3_SSRX1+	H13	GND
E14	GND	F14	RSVD [1]	G14	GND	H14	USB2_AUX- [1]
E15	DDI2_PAIR3-	F15	RSVD [1]	G15	USB3_LSRX [2]	H15	USB2_AUX+ [1]
E16	DDI2_PAIR3+	F16	RSVD [1]	G16	USB3_LSTX [2]	H16	GND
E17	GND	F17	RSVD [1]	G17	USB2_LSRX [2]	H17	USB3_AUX- [1]
E18	DDI2_DDC_AUX_SEL	F18	RSVD [1]	G18	USB2_LSTX [2]	H18	USB3_AUX+ [1]
E19	DDI2_HPD	F19	GND	G19	PEG_LANE_REV#	H19	GND
E20	GND	F20	PCIe32_RX-	G20	GND	H20	PCIe40_TX- [1]
E21	PCIe32_TX-	F21	PCIe32_RX+	G21	PCIe40_RX- [1]	H21	PCIe40_TX+ [1]
E22	PCIe32_TX+	F22	GND	G22	PCIe40_RX+ [1]	H22	GND
E23	GND	F23	PCIe33_RX-	G23	GND	H23	PCIe41_TX- [1]
E24	PCIe33_TX-	F24	PCIe33_RX+	G24	PCIe41_RX- [1]	H24	PCIe41_TX+ [1]
E25	PCIe33_TX+	F25	GND	G25	PCIe41_RX+ [1]	H25	GND
E26	GND	F26	PCIe34_RX-	G26	GND	H26	PCIe42_TX- [1]
E27	PCIe34_TX-	F27	PCIe34_RX+	G27	PCIe42_RX- [1]	H27	PCIe42_TX+ [1]
E28	PCIe34_TX+	F28	GND	G28	PCIe42_RX+ [1]	H28	GND
E29	GND	F29	PCIe35_RX-	G29	GND	H29	PCIe43_TX- [1]
E30	PCIe35_TX-	F30	PCIe35_RX+	G30	PCIe43_RX- [1]	H30	PCIe43_TX+ [1]
E31	PCIe35_TX+	F31	GND	G31	PCIe43_RX+ [1]	H31	GND
E32	GND	F32	PCIe36_RX-	G32	GND	H32	PCIe44_TX- [1]
E33	PCIe36_TX-	F33	PCIe36_RX+	G33	PCIe44_RX- [1]	H33	PCIe44_TX+ [1]
E34	PCIe36_TX+	F34	GND	G34	PCIe44_RX+ [1]	H34	GND
E35	GND	F35	PCIe37_RX-	G35	GND	H35	PCIe45_TX- [1]
E36	PCIe37_TX-	F36	PCIe37_RX+	G36	PCIe45_RX- [1]	H36	PCIe45_TX+ [1]
E37	PCIe37_TX+	F37	GND	G37	PCIe45_RX+ [1]	H37	GND
E38	GND	F38	PCIe38_RX-	G38	GND	H38	PCIe46_TX- [1]

E39	PCIe38_TX-	F39	PCIe38_RX+	G39	PCIe46_RX- [1]	H39	PCIe46_TX+ [1]
E40	PCIe38_TX+	F40	GND	G40	PCIe46_RX+ [1]	H40	GND
E41	GND	F41	PCIe39_RX-	G41	GND	H41	PCIe47_TX- [1]
E42	PCIe39_TX-	F42	PCIe39_RX+	G42	PCIe47_RX- [1]	H42	PCIe47_TX+ [1]
E43	PCIe39_TX+	F43	GND	G43	PCIe47_RX+ [1]	H43	GND
E44	GND	F44	PCIe16_RX-	G44	GND	H44	PCIe24_TX-
E45	PCIe16_TX-	F45	PCIe16_RX+	G45	PCIe24_RX-	H45	PCIe24_TX+
E46	PCIe16_TX+	F46	GND	G46	PCIe24_RX+	H46	GND
E47	GND	F47	PCIe17_RX-	G47	GND	H47	PCIe25_TX-
E48	PCIe17_TX-	F48	PCIe17_RX+	G48	PCIe25_RX-	H48	PCIe25_TX+
E49	PCIe17_TX+	F49	GND	G49	PCIe25_RX+	H49	GND
E50	GND	F50	PCIe18_RX-	G50	GND	H50	PCIe26_TX-
E51	PCIe18_TX-	F51	PCIe18_RX+	G51	PCIe26_RX-	H51	PCIe26_TX+
E52	PCIe18_TX+	F52	GND	G52	PCIe26_RX+	H52	GND
E53	GND	F53	PCIe19_RX-	G53	GND	H53	PCIe27_TX-
E54	PCIe19_TX-	F54	PCIe19_RX+	G54	PCIe27_RX-	H54	PCIe27_TX+
E55	PCIe19_TX+	F55	GND	G55	PCIe27_RX+	H55	GND
E56	GND	F56	PCIe20_RX-	G56	GND	H56	PCIe28_TX-
E57	PCIe20_TX-	F57	PCIe20_RX+	G57	PCIe28_RX-	H57	PCIe28_TX+
E58	PCIe20_TX+	F58	GND	G58	PCIe28_RX+	H58	GND
E59	GND	F59	PCIe21_RX-	G59	GND	H59	PCIe29_TX-
E60	PCIe21_TX-	F60	PCIe21_RX+	G60	PCIe29_RX-	H60	PCIe29_TX+
E61	PCIe21_TX+	F61	GND	G61	PCIe29_RX+	H61	GND
E62	GND	F62	PCIe22_RX-	G62	GND	H62	PCIe30_TX-
E63	PCIe22_TX-	F63	PCIe22_RX+	G63	PCIe30_RX-	H63	PCIe30_TX+
E64	PCIe22_TX+	F64	GND	G64	PCIe30_RX+	H64	GND
E65	GND	F65	PCIe23_RX-	G65	GND	H65	PCIe31_TX-
E66	PCIe23_TX-	F66	PCIe23_RX+	G66	PCIe31_RX-	H66	PCIe31_TX+
E67	PCIe23_TX+	F67	GND	G67	PCIe31_RX+	H67	GND
E68	GND	F68	RSVD [1]	G68	GND	H68	RSVD [1]
E69	RSVD [1]	F69	RSVD [1]	G69	RSVD [1]	H69	RSVD [1]
E70	RSVD [1]	F70	GND	G70	RSVD [1]	H70	GND
E71	RSVD [1]	F71	NBASET1_MDI0-	G71	GND	H71	CSI1_RX0-
E72	RSVD [1]	F72	NBASET1_MDI0+	G72	CSI0_RX0-	H72	CSI1_RX0+
E73	RSVD [1]	F73	GND	G73	CSI0_RX0+	H73	GND
E74	RSVD [1]	F74	NBASET1_MDI1-	G74	GND	H74	CSI1_RX1-
E75	RSVD [1]	F75	NBASET1_MDI1+	G75	CSI0_RX1-	H75	CSI1_RX1+
E76	RSVD [1]	F76	GND	G76	CSI0_RX1+	H76	GND
E77	RSVD [1]	F77	NBASET1_MDI2-	G77	GND	H77	CSI1_RX2- [1]
E78	NBASET1_CTREF [1]	F78	NBASET1_MDI2+	G78	CSI0_RX2-	H78	CSI1_RX2+ [1]
E79	NBASET1_SDP	F79	GND	G79	CSI0_RX2+	H79	GND

E80	NBASET1_LINK_MID#	F80	NBASET1_MDI3-	G80	GND	H80	CSI1_RX3- [1]
E81	NBASET1_LINK_ACT#	F81	NBASET1_MDI3+	G81	CSI0_RX3-	H81	CSI1_RX3+ [1]
E82	NBASET1_LINK_MAX#	F82	GND	G82	CSI0_RX3+	H82	GND
E83	GND	F83	RSVD [1]	G83	GND	H83	CSI1_CLK-
E84	RSVD [1]	F84	RSVD [1]	G84	CSI0_CLK-	H84	CSI1_CLK+
E85	RSVD [1]	F85	TEST# (GND)	G85	CSI0_CLK+	H85	GND
E86	GND	F86	ETH0_TX- [1]	G86	GND	H86	CSI1_I2C_CLK
E87	ETH0_RX- [1]	F87	ETH0_TX+ [1]	G87	CSI0_I2C_CLK	H87	CSI1_I2C_DAT
E88	ETH0_RX+ [1]	F88	GND	G88	CSI0_I2C_DAT	H88	CSI1_MCLK
E89	GND	F89	ETH1_TX- [1]	G89	CSI0_MCLK	H89	CSI1_RST#
E90	ETH1_RX- [1]	F90	ETH1_TX+ [1]	G90	CSI0_RST#	H90	CSI1_ENA
E91	ETH1_RX+ [1]	F91	GND	G91	CSI0_ENA	H91	GND
E92	GND	F92	PCIe_REFCLK2-	G92	GND	H92	PCIe_REFCLKIN0- [1]
E93	PCIe_REFCLK1-	F93	PCIe_REFCLK2+	G93	RSVD [1]	H93	PCIe_REFCLKIN0+ [1]
E94	PCIe_REFCLK1+	F94	GND	G94	RSVD [1]	H94	GND
E95	GND	F95	RSVD [1]	G95	GND	H95	PCIe_REFCLKIN1- [1]
E96	PCIe_CLKREQ1#	F96	ETH0-1_PRSNT# [2]	G96	ETH0-1_I2C_CLK [2]	H96	PCIe_REFCLKIN1+ [1]
E97	PCIe_CLKREQ2#	F97	ETH0-1_PHY_RST# [2]	G97	ETH0-1_I2C_DAT [2]	H97	GND
E98	PCIe_CLKREQ_OUT0# [1]	F98	ETH0_SDP [1]	G98	ETH0-1_PHY_INT# [2]	H98	ETH0-1_MDIO_CLK [2]
E99	PCIe_CLKREQ_OUT1# [1]	F99	ETH1_SDP [1]	G99	ETH0-1_INT# [2]	H99	ETH0-1_MDIO_DAT [2]
E100	PCIe_PERST_IN0# [1]	F100	PCIe_PERST_IN1# [1]	G100	PCIe_WAKE_OUT0# [1]	H100	PCIe_WAKE_OUT1# [1]

Note

1. *Not connected*
2. *Not supported*

Table 22 NBASE-T Ethernet Signal Descriptions

<table>
<tr><th>Gigabit Ethernet</th><th>Pin #</th><th>Description</th><th>I/O</th><th>PU/PD</th><th>Comment</th></tr>
<tr><td>NBASET0_MDI0+
NBASET0_MDI0-
NBASET0_MDI1+
NBASET0_MDI1-
NBASET0_MDI2+
NBASET0_MDI2-
NBASET0_MDI3+
NBASET0_MDI3-

NBASET1_MDI0+
NBASET1_MDI0-
NBASET1_MDI1+
NBASET1_MDI1-
NBASET1_MDI2+
NBASET1_MDI2-
NBASET1_MDI3+
NBASET1_MDI3-</td><td>D86
D85
D89
D88
D92
D91
D95
D94

F72
F71
F75
F74
F78
F77
F81
F80</td><td>Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 10 Gbps, 1 Gbps, 100 Mbps and 10 Mbps modes.
Some pairs are unused in some modes, per the following:
<table><tr><th></th><th>10000BASE-T
1000BASE-T</th><th>100BASE-TX</th><th>10BASE-T</th></tr><tr><td>MDI[0]+/-</td><td>B1_DA+/-</td><td>TX+/-</td><td>TX+/-</td></tr><tr><td>MDI[1]+/-</td><td>B1_DB+/-</td><td>RX+/-</td><td>RX+/-</td></tr><tr><td>MDI[2]+/-</td><td>B1_DC+/-</td><td></td><td></td></tr><tr><td>MDI[3]+/-</td><td>B1_DD+/-</td><td></td><td></td></tr></table></td><td>I/O MDI
3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_ACT#
NBASET1_LINK_ACT#</td><td>D99
E81</td><td>NBASE-T Ethernet controller activity indicator, active low.
20 mA or more current sink capability at VOL of 0.4V max.
20 mA or more current source capability at VOH of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_MAX#
NBASET1_LINK_MAX#</td><td>D97
E82</td><td>NBASE-T Ethernet controller maximum speed link indicator (active low). If active, the link is established at the maximum speed that the Ethernet controller is capable of (which may be 10 Gb, 5 Gb, 2.5 Gb etc).
20 mA or more current sink capability at VOL of 0.4 V max.
20 mA or more current source capability at VOH of 2.4 V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_MID#
NBASET1_LINK_MID#</td><td>D98
E80</td><td>NBASE-T Ethernet controller mid speed link indicator (active low). If active, the link is established but at a speed lower than the maximum speed of what the Ethernet controller is capable of.
20 mA or more current sink capability at VOL of 0.4 V max.
20 mA or more current source capability at VOH of 2.4 V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_CTREF
NBASET1_CTREF</td><td>C99
E78</td><td>Reference voltage for carrier board NBASET Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3 V.

If not needed, these pins may be left open on the carrier. The reference voltage output shall be current limited on the module. If the reference is shorted to ground, the current shall be limited to 250 mA or less.</td><td>REF</td><td></td><td>Not connected</td></tr>
<tr><td>NBASET0_SDP
NBASET1_SDP</td><td>C98
E79</td><td>NBASE-T Ethernet controller 0 software-definable pin. Can also be used for IEEE1588 support such as a 1 pps signal.</td><td>I/O 3.3 VSB</td><td></td><td></td></tr>
</table>

Table 23 Ethernet KR and KX Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
ETH0_TX+ ETH0_TX-	F87 F86	Ethernet KR ports, transmit output differential pairs.	O KR		Not connected
ETH0_RX+ ETH0_RX-	E88 E87	Ethernet KR ports, receive input differential pairs.	I KR		
ETH1_TX+ ETH1_TX-	F90 F89	Ethernet KR ports, transmit output differential pairs.	O KR		
ETH1_RX+ ETH1_RX-	E91 E90	Ethernet KR ports, receive input differential pairs.	I KR		
ETH0-1_MDIO_DAT	H99	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports to 1.	I/O 3.3 VSB		Not supported
ETH0-1_MDIO_CLK	H98	Clock signal for Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 1.	O 3.3 VSB		
ETH0-1_INT#	G99	Active low interrupt signal from IO Port expanders for ETH ports 0 to 1.	I 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
ETH0-1_PHY_INT#	G98	Active low PHY interrupt signal from ETH ports 0 to 1	I 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
ETH0-1_PHY_RST#	F97	Active low output PHY reset signal for ETH ports 0 to 1	O 3.3 VSB		
ETH0-1_I2C_DAT	G97	I²C data signal of the 2-wire management interface used by the Ethernet KR controller to access the management registers of an external SFP module or to configure the carrier PHY for ETHx ports 0 to 1 and for serialized status information (e.g. LED states).	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
ETH0-1_I2C_CLK	G96	The I²C clock signals associated with ETH0-2 I²C data lines in the row above.	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
ETH0_SDP ETH1_SDP	F98 F99	Software-Definable Pins. Can also be used for IEEE1588 support such as a PPS signal.	I/O 3.3 VSB		Not connected
ETH0-1_PRSNT#	F96	Carrier pulls this line to GND if there is carrier hardware present to support Ethernet KR signaling on ETH0 or ETH1. If only one KR channel is supported, it should be on ETH0.	I 3.3 VSB	PU 2.2 KΩ 3.3 VSB	Not supported

Note

The conga-HPC/cTLH does not support Ethernet KR and KX interfaces.

Table 24 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_TX+ SATA0_TX-	D53 D52	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification 3.0
SATA0_RX+ SATA0_RX-	D50 D49	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification 3.0
SATA1_TX+ SATA1_TX-	D59 D58	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification 3.0
SATA1_RX+ SATA1_RX-	D56 D55	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification 3.0

Table 25 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIe00_TX+ PCIe00_TX-	D62 D61	PCI Express Transmit Output Differential Pairs 0	O PCIE		Supports PCIe Gen 3
PCIe00_RX+ PCIe00_RX-	C63 C62	PCI Express Receive Input Differential Pairs 0	I PCIE		
PCIe01_TX+ PCIe01_TX-	D65 D64	PCI Express Transmit Output Differential Pairs 1	O PCIE		
PCIe01_RX+ PCIe01_RX-	C66 C65	PCI Express Receive Input Differential Pairs 1	I PCIE		
PCIe02_TX+ PCIe02_TX-	D68 D67	PCI Express Transmit Output Differential Pairs 2	O PCIE		
PCIe02_RX+ PCIe02_RX-	C69 C68	PCI Express Receive Input Differential Pairs 2	I PCIE		
PCIe03_TX+ PCIe03_TX-	D71 D70	PCI Express Transmit Output Differential Pairs 3	O PCIE		
PCIe03_RX+ PCIe03_RX-	C72 C71	PCI Express Receive Input Differential Pairs 3	I PCIE		
PCIe04_TX+ PCIe04_TX-	D74 D73	PCI Express Transmit Output Differential Pairs 4	O PCIE		
PCIe04_RX+ PCIe04_RX-	C75 C74	PCI Express Receive Input Differential Pairs 4	I PCIE		
PCIe05_TX+ PCIe05_TX-	D77 D76	PCI Express Transmit Output Differential Pairs 5	O PCIE		
PCIe05_RX+ PCIe05_RX-	C78 C77	PCI Express Receive Input Differential Pairs 5	I PCIE		

PCIe06_TX+ PCIe06_TX-	D80 D79	PCI Express Transmit Output Differential Pairs 6	O PCIE		Supports PCIe Gen 3
PCIe06_RX+ PCIe06_RX-	C81 C80	PCI Express Receive Input Differential Pairs 6	I PCIE		
PCIe07_TX+ PCIe07_TX-	D83 D82	PCI Express Transmit Output Differential Pairs 7	O PCIE		
PCIe07_RX+ PCIe07_RX-	C84 C83	PCI Express Receive Input Differential Pairs 7	I PCIE		
PCIe08_TX+ PCIe08_TX-	A63 A62	PCI Express Transmit Output Differential Pairs 8	O PCIE		Supports PCIe Gen 4 (1 x4 link)
PCIe08_RX+ PCIe08_RX-	B62 B61	PCI Express Receive Input Differential Pairs 8	I PCIE		
PCIe09_TX+ PCIe09_TX-	A66 A65	PCI Express Transmit Output Differential Pairs 9	O PCIE		
PCIe09_RX+ PCIe09_RX-	B65 B64	PCI Express Receive Input Differential Pairs 9	I PCIE		
PCIe10_TX+ PCIe10_TX-	A69 A68	PCI Express Transmit Output Differential Pairs 10	O PCIE		
PCIE10_RX+ PCIE10_RX-	B68 B67	PCI Express Receive Input Differential Pairs 10	I PCIE		
PCIE11_TX+ PCIE11_TX-	A72 A71	PCI Express Transmit Output Differential Pairs 11	O PCIE		
PCIE11_RX+ PCIE11_RX-	B71 B70	PCI Express Receive Input Differential Pairs 11	I PCIE		
PCIE12_TX+ PCIE12_TX-	B75 A74	PCI Express Transmit Output Differential Pairs 12	O PCIE		Supports PCIe Gen 3
PCIE12_RX+ PCIE12_RX-	B74 B73	PCI Express Receive Input Differential Pairs 12	I PCIE		
PCIE13_TX+ PCIE13_TX-	A78 A77	PCI Express Transmit Output Differential Pairs 13	O PCIE		
PCIE13_RX+ PCIE13_RX-	B77 B76	PCI Express Receive Input Differential Pairs 13	I PCIE		
PCIE14_TX+ PCIE14_TX-	A81 A80	PCI Express Transmit Output Differential Pairs 14	O PCIE		
PCIE14_RX+ PCIE14_RX-	B80 B79	PCI Express Receive Input Differential Pairs 14	I PCIE		
PCIE15_TX+ PCIE15_TX-	A84 A83	PCI Express Transmit Output Differential Pairs 15	O PCIE		
PCIE15_RX+ PCIE15_RX-	B83 B82	PCI Express Receive Input Differential Pairs 15	I PCIE		
PCIE16_TX+ PCIE16_TX-	E46 E45	PCI Express Transmit Output Differential Pairs 16	O PCIE		PEG Port 0 (PCIe Gen 4)
PCIE16_RX+ PCIE16_RX-	F45 F44	PCI Express Receive Input Differential Pairs 16	I PCIE		

PCIE17_TX+ PCIE17_TX-	E49 E48	PCI Express Transmit Output Differential Pairs 17	O PCIE		PEG port 1 (PCIe Gen 4)
PCIE17_RX+ PCIE17_RX-	F48 F47	PCI Express Receive Input Differential Pairs 17	I PCIE		
PCIE18_TX+ PCIE18_TX-	E52 E51	PCI Express Transmit Output Differential Pairs 18	O PCIE		PEG port 2 (PCIe Gen 4)
PCIE18_RX+ PCIE18_RX-	F51 F50	PCI Express Receive Input Differential Pairs 18	I PCIE		
PCIE19_TX+ PCIE19_TX-	E55 E54	PCI Express Transmit Output Differential Pairs 19	O PCIE		PEG port 3 (PCIe Gen 4)
PCIE19_RX+ PCIE19_RX-	F54 F53	PCI Express Receive Input Differential Pairs 19	I PCIE		
PCIE20_TX+ PCIE20_TX-	E58 E57	PCI Express Transmit Output Differential Pairs 20	O PCIE		PEG port 4 (PCIe Gen 4)
PCIE20_RX+ PCIE20_RX-	F57 F56	PCI Express Receive Input Differential Pairs 20	I PCIE		
PCIE21_TX+ PCIE21_TX-	E61 E60	PCI Express Transmit Output Differential Pairs 21	O PCIE		PEG port 5 (PCIe Gen 4)
PCIE21_RX+ PCIE21_RX-	F60 F59	PCI Express Receive Input Differential Pairs 21	I PCIE		
PCIE22_TX+ PCIE22_TX-	E64 E63	PCI Express Transmit Output Differential Pairs 22	O PCIE		PEG port 6 (PCIe Gen 4)
PCIE22_RX+ PCIE22_RX-	F63 F62	PCI Express Receive Input Differential Pairs 22	I PCIE		
PCIE23_TX+ PCIE23_TX-	E67 E66	PCI Express Transmit Output Differential Pairs 23	O PCIE		PEG port 7 (PCIe Gen 4)
PCIE23_RX+ PCIE23_RX-	F66 F65	PCI Express Receive Input Differential Pairs 23	I PCIE		
PCIE24_TX+ PCIE24_TX-	H45 H44	PCI Express Transmit Output Differential Pairs 24	O PCIE		PEG port 8 (PCIe Gen 4)
PCIE24_RX+ PCIE24_RX-	G46 G45	PCI Express Receive Input Differential Pairs 24	I PCIE		
PCIE25_TX+ PCIE25_TX-	H48 H47	PCI Express Transmit Output Differential Pairs 25	O PCIE		PEG port 9 (PCIe Gen 4)
PCIE25_RX+ PCIE25_RX-	G46 G45	PCI Express Receive Input Differential Pairs 25	I PCIE		
PCIE26_TX+ PCIE26_TX-	H51 H50	PCI Express Transmit Output Differential Pairs 26	O PCIE		PEG port 10 (PCIe Gen 4)
PCIE26_RX+ PCIE26_RX-	G52 G51	PCI Express Receive Input Differential Pairs 26	I PCIE		
PCIE27_TX+ PCIE27_TX-	H54 H53	PCI Express Transmit Output Differential Pairs 27	O PCIE		PEG port 11 (PCIe Gen 4)
PCIE27_RX+ PCIE27_RX-	G55 G54	PCI Express Receive Input Differential Pairs 27	I PCIE		

PCIE28_TX+ PCIE28_TX-	H57 H56	PCI Express Transmit Output Differential Pairs 28	O PCIE		PEG port 12 (PCIe Gen 4)
PCIE28_RX+ PCIE28_RX-	G58 G57	PCI Express Receive Input Differential Pairs 28	I PCIE		
PCIE29_TX+ PCIE29_TX-	H60 H59	PCI Express Transmit Output Differential Pairs 29	O PCIE		PEG port 13 (PCIe Gen 4)
PCIE29_RX+ PCIE29_RX-	G61 G60	PCI Express Receive Input Differential Pairs 29	I PCIE		
PCIE30_TX+ PCIE30_TX-	H63 H62	PCI Express Transmit Output Differential Pairs 30	O PCIE		PEG port 14 (PCIe Gen 4)
PCIE30_RX+ PCIE30_RX-	G64 G63	PCI Express Receive Input Differential Pairs 30	I PCIE		
PCIE31_TX+ PCIE31_TX-	H66 H65	PCI Express Transmit Output Differential Pairs 31	O PCIE		PEG port 15 (PCIe Gen 4)
PCIE31_RX+ PCIE31_RX-	G67 G66	PCI Express Receive Input Differential Pairs 31	I PCIE		
PCIE32_TX+ PCIE32_TX-	E22 E21	PCI Express Transmit Output Differential Pairs 32	O PCIE		Supports PCIe Gen 3
PCIE32_RX+ PCIE32_RX-	F21 F20	PCI Express Receive Input Differential Pairs 32	I PCIE		
PCIE33_TX+ PCIE33_TX-	E25 E24	PCI Express Transmit Output Differential Pairs 33	O PCIE		
PCIE33_RX+ PCIE33_RX-	F24 F23	PCI Express Receive Input Differential Pairs 33	I PCIE		
PCIE34_TX+ PCIE34_TX-	E28 E27	PCI Express Transmit Output Differential Pairs 34	O PCIE		
PCIE34_RX+ PCIE34_RX-	F27 F26	PCI Express Receive Input Differential Pairs 34	I PCIE		
PCIE35_TX+ PCIE35_TX-	E31 E30	PCI Express Transmit Output Differential Pairs 35	O PCIE		
PCIE35_RX+ PCIE35_RX-	F30 F29	PCI Express Receive Input Differential Pairs 35	I PCIE		
PCIE36_TX+ PCIE36_TX-	E34 E33	PCI Express Transmit Output Differential Pairs 36	O PCIE		Supports PCIe Gen 3
PCIE36_RX+ PCIE36_RX-	F33 F32	PCI Express Receive Input Differential Pairs 36	I PCIE		
PCIE37_TX+ PCIE37_TX-	E37 E36	PCI Express Transmit Output Differential Pairs 37	O PCIE		
PCIE37_RX+ PCIE37_RX-	F36 F35	PCI Express Receive Input Differential Pairs 37	I PCIE		
PCIE38_TX+ PCIE38_TX-	E40 E39	PCI Express Transmit Output Differential Pairs 38	O PCIE		
PCIE38_RX+ PCIE38_RX-	F39 F38	PCI Express Receive Input Differential Pairs 38	I PCIE		

PCIE39_TX+ PCIE39_TX-	E43 E42	PCI Express Transmit Output Differential Pairs 39	O PCIE		Supports PCIe Gen 3
PCIE39_RX+ PCIE39_RX-	F42 F41	PCI Express Receive Input Differential Pairs 39	I PCIE		
PCIE40_TX+ PCIE40_TX-	H21 H20	PCI Express Transmit Output Differential Pairs 40	O PCIE		Not connected
PCIE40_RX+ PCIE40_RX-	G22 G21	PCI Express Receive Input Differential Pairs 40	I PCIE		
PCIE41_TX+ PCIE41_TX-	H24 H23	PCI Express Transmit Output Differential Pairs 41	O PCIE		
PCIE41_RX+ PCIE41_RX-	G25 G24	PCI Express Receive Input Differential Pairs 41	I PCIE		
PCIE42_TX+ PCIE42_TX-	H27 H26	PCI Express Transmit Output Differential Pairs 42	O PCIE		
PCIE42_RX+ PCIE42_RX-	G28 G27	PCI Express Receive Input Differential Pairs 42	I PCIE		
PCIE43_TX+ PCIE43_TX-	H30 H29	PCI Express Transmit Output Differential Pairs 43	O PCIE		
PCIE43_RX+ PCIE43_RX-	G31 G30	PCI Express Receive Input Differential Pairs 43	I PCIE		
PCIE44_TX+ PCIE44_TX-	H33 H32	PCI Express Transmit Output Differential Pairs 44	O PCIE		
PCIE44_RX+ PCIE44_RX-	G34 G33	PCI Express Receive Input Differential Pairs 44	I PCIE		
PCIE45_TX+ PCIE45_TX-	H36 H35	PCI Express Transmit Output Differential Pairs 45	O PCIE		
PCIE45_RX+ PCIE45_RX-	G37 G36	PCI Express Receive Input Differential Pairs 45	I PCIE		
PCIE46_TX+ PCIE46_TX-	H39 H38	PCI Express Transmit Output Differential Pairs 46	O PCIE		
PCIE46_RX+ PCIE46_RX-	G40 G39	PCI Express Receive Input Differential Pairs 46	I PCIE		
PCIE47_TX+ PCIE47_TX-	H42 H41	PCI Express Transmit Output Differential Pairs 47	O PCIE		
PCIE47_RX+ PCIE47_RX-	G43 G42	PCI Express Receive Input Differential Pairs 47	I PCIE		
PCIE_BMC_TX+ PCIE_BMC_TX-	A60 A59	PCI Express Differential Transmit Pair for carrier BMC	O PCIE		
PCIE_BMC_RX+ PCIE_BMC_RX-	B59 B58	PCI Express Differential Receive Pair for carrier BMC	I PCIE		
PCIe_REFCLK0_LO+ PCIe_REFCLK0_LO-	C60 C59	Reference clock pair for PCIe lanes [0:7], also referred to as PCIe Group 0 Low and for the PCIe_BMC link	O LV_DIFF		
PCIe_REFCLK0_HI+ PCIe_REFCLK0_HI-	C57 C56	Reference clock pair for PCIe lanes [8:15] also referred to as PCIe Group 0 High	O LV_DIFF		

PCIe_REFCLK1+ PCIe_REFCLK1-	E94 E93	Reference clock pair for PCIe lanes [16:31] also referred to as PCIe Group 1	O LV_DIFF		
PCIe_REFCLK2+ PCIe_REFCLK2-	F93 F92	Reference clock pair for PCIe lanes [32:47] also referred to as PCIe Group 2	O LV_DIFF		
PCIe_CLKREQ0_LO#	A56	PCIe reference clock request signal from carrier devices for PCIe_ REFCLK0_LO clock pair	Bi-Dir OD 3.3 V	PU 10 KΩ 3.3 V	
PCIe_CLKREQ0_HI#	A57	PCIe reference clock request signal from carrier devices for PCIe_ REFCLK0_HI clock pair	Bi-Dir OD 3.3 V	PU 10 KΩ 3.3 V	
PCIe_CLKREQ1#	E96	PCIe reference clock request signal from carrier devices for PCIe_ REFCLK1 clock pair	Bi-Dir OD 3.3 V	PU 10 KΩ 3.3 V	
PCIe_CLKREQ2#	E97	PCIe reference clock request signals from carrier devices for PCIe_ REFCLK2 clock pair	Bi-Dir OD 3.3 V	PU 10 KΩ 3.3 V	
PEG_LANE_REV#	G19	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order, otherwise leave COM-HPC® pin open. Pulled up on module or module chipset to chipset specific power rail.	I 3.3 V	PU 100 KΩ 3.3 V	
PCI Express Additional Signals to Support Module-based PCIe Targets					
PCIe_REFCLKIN0+ PCIe_REFCLKIN0-	H93 H92	Reference clock inputs allowing carrier based root to operate with module based PCIe targets. The module designer making use of these clocks should terminate them in a way appropriate to that design.	I LV_DIFF 3.3 V		Not connected
PCIe_REFCLKIN1+ PCIe_REFCLKIN1-	H96 H95	Reference clock inputs allowing carrier based root to operate with module based PCIe targets. The module designer making use of these clocks should terminate them in a way appropriate to that design.	I LV_DIFF 3.3 V		
PCIe_WAKE_OUT0#	G100	Wake request signal from module based PCIe target to an off- module PCIe root complex.	OD 3.3 VSB		
PCIe_WAKE_OUT1#	H100	Wake request signal from module based PCIe target to an off- module PCIe root complex.	OD 3.3 VSB		
PCIe_PERST_IN0#	E100	Reset signals into module to reset module PCIe targets.	I 3.3 V		
PCIe_PERST_IN1#	F100	Reset signals into module to reset module PCIe targets.	I 3.3 V		

Table 26 USB Signal Descriptions

USB	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	D17 D16	USB 2.0 differential pairs, channels 0 through 7. USB0 may be configured as a USB client or as a host, or both at the module designer's discretion. All other USB ports, if implemented, shall be host ports. If any SuperSpeed ports are implemented, then they must be supported by a USB 2.0 port, using one of the USB[0:3] ports from this pool. Specific pairings are detailed below.	I/O USB 3.3 VSB		
USB1+ USB1-	D14 D13		I/O USB 3.3 VSB		
USB2+ USB2-	C18 C17		I/O USB 3.3 VSB		
USB3+ USB3-	C15 C14		I/O USB 3.3 VSB		
USB4+ USB4-	B17 B16		I/O USB 3.3 VSB		
USB5+ USB5-	B14 B13		I/O USB 3.3 VSB		
USB6+ USB6-	A18 A17		I/O USB 3.3 VSB		
USB7+ USB7-	A15 A14		I/O USB 3.3 VSB		
USB0_SSTX0+ USB0_SSTX0-	D44 D43	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 0. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB0 USB 2.0 differential pairs)	O USB SS		Supports USB 4.0
USB0_SSRX0+ USB0_SSRX0-	C45 C44		I USB SS		
USB0_SSTX1+ USB0_SSTX1-	D47 D46		O USB SS		
USB0_SSRX1+ USB0_SSRX1-	C48 C47		I USB SS		
USB1_SSTX0+ USB1_SSTX0-	D38 D37	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 1. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB1 USB 2.0 differential pairs)	O USB SS		
USB1_SSRX0+ USB1_SSRX0-	C39 C38		I USB SS		
USB1_SSTX1+ USB1_SSTX1-	D41 D40		O USB SS		
USB1_SSRX1+ USB1_SSRX1-	C42 C41		I USB SS		
USB2_SSTX0+ USB2_SSTX0-	H03 H02	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 2. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB2 USB 2.0 differential pairs)	O USB SS		Supports USB 3.2 Gen 2 x 2
USB2_SSRX0+ USB2_SSRX0-	G04 G03		I USB SS		
USB2_SSTX1+ USB2_SSTX1-	H06 H05		O USB SS		
USB2_SSRX1+ USB2_SSRX1-	G07 G06		I USB SS		

USB3_SSTX0+ USB3_SSTX0-	H09 H08	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 3. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB3 USB 2.0 differential pairs)	O USB SS		USB 3.2 Gen 2 x 2
USB3_SSRX0+ USB3_SSRX0-	G10 G09		I USB SS		
USB3_SSTX1+ USB3_SSTX1-	H12 H11		O USB SS		
USB3_SSRX1+ USB3_SSRX1-	G13 G12		I USB SS		
USB01_OC#	B28	USB over-current sense, USB channels 0,1; channels 2,3; channels 4,5 and channels 6,7 respectively. A pull-up for each of these lines to the 3.3V Suspend rail shall be present on the module. The pull-up should be 10K. An open drain driver from USB current monitors on the carrier board may drive this line low. The carrier board shall not pull these lines up. Note that the over-current limits for USB 2.0 and USB 3.0 are different; this is a carrier board implementation item.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
USB23_OC#	B27			PU 10 KΩ 3.3 VSB	
USB45_OC#	B26			PU 10 KΩ 3.3 VSB	
USB67_OC#	B25			PU 10 KΩ 3.3 VSB	
RSMRST_OUT#	B86	USB devices that are to be powered in the S5 / S4 / S3 suspend states should not have their 5 V VBUS power enabled before RSMRST_OUT# transitions to the high state.	O 3.3 VSB		

Table 27 USB 4 Support Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0_AUX+ USB0_AUX-	B44 B43	DisplayPort Aux channel for USB4 DP modes High speed differential pair	LV_DIFF		
USB0_LSTX	B41	Sideband TX interface for USB4 Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	
USB0_LSRX [1]	B40	Sideband RX interface for USB4 Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PU 4.75 KΩ 3.3 VSB	Bootstrap signal (see note below)
USB1_AUX+ USB1_AUX-	A48 A47	DisplayPort Aux channel for USB4 DP modes High speed differential pair	LV_DIFF		
USB1_LSTX	B39	Sideband TX interface for USB4 Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	
USB1_LSRX [1]	B38	Sideband RX interface for USB4 Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PU 4.75 KΩ 3.3 VSB	Bootstrap signal (see note below)
USB2_AUX+ USB2_AUX-	H15 H14	DisplayPort Aux channel for USB4 DP modes High speed differential pair	LV_DIFF		Not supported
USB2_LSTX	G18	Sideband TX interface for USB4 Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	Not supported
USB2_LSRX	G17	Sideband RX interface for USB4 Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PD 1 MΩ	
USB3_AUX+ USB3_AUX-	H18 H17	DisplayPort Aux channel for USB4 DP modes High speed differential pair	LV_DIFF		Not supported
USB3_LSTX	G16	Sideband TX interface for USB4 Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	Not supported
USB3_LSRX	G15	Sideband RX interface for USB4 Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PD 1 MΩ	
SML0_DAT	B33	Data line for I²C data based System Management Links between chipset masters and carrier. SML0 is used to control the carrier based USB re-timers and SML1 controls the carrier based USB Power Delivery Controller.	Bi-Dir OD 3.3 VSB	PU 499 Ω 3.3 VSB	
SML1_DAT	B30		Bi-Dir OD 3.3 VSB	PU 1 KΩ 3.3 VSB	
SML0_CLK	B32	Clock lines for System Management Links 0 and 1. SML0 is used to support carrier USB4 Re-Timers SML1 is used to support carrier USB Power Delivery (PD) Controller.	Bi-Dir OD 3.3 VSB	PU 499 Ω 3.3 VSB	
SML1_CLK	B29		Bi-Dir OD 3.3 VSB	PU 1 KΩ 3.3 VSB	
PMCALERT#	B31	Active low Alert signal associated with the SML1 System Management link, from the carrier based USB Power Delivery Controller.	I 3.3 V	PU 10 KΩ 3.3 VSB	
USB_RT_ENA	B37	Power Enable for carrier based USB Retimers. Sourced from chipset GPO. "USB Re-Timer Enable".	O 3.3 V	PD 10 KΩ	
USB_PD_I2C_DAT	B36	I²C data line between module based Embedded Controller master and carrier based USB Power Delivery Controller slave.	Bi-Dir OD 3.3 VSB	PU 1 KΩ 3.3 VSB	

USB_PD_I2C_CLK	B35	I²C clock line between module based Embedded Controller master and carrier based USB Power Delivery Controller slave.	Bi-Dir OD 3.3 VSB	PU 1 KΩ 3.3 VSB	
USB_PD_ALERT#	B34	Active low Alert signal from USB Power Delivery Controller to the module Embedded Controller.	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
Additional Signals to Support USB4 Implementation					
PLTRST#	A12	Platform Reset: output from module to carrier board. Active low. Issued by module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.	O 3.3 VSB	PD 100 KΩ	
SUS_S4_S5#	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3 VSB	PD 100 KΩ	

Note

1. *These signals have special functionality during the reset process. They may bootstrap some important functions of the module. For more information, refer to section 9.2 "Boot Strap Signals".*

Table 28 eSPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eSPI_IO0 eSPI_IO1 eSPI_IO2 eSPI_IO3	A50 A51 A52 A53	eSPI Master Data Input / Outputs. These are bi-directional input/output pins used to transfer data between master and slaves.	I/O 1.8 VSB		
eSPI_CS0# eSPI_CS1#	B54 B55	eSPI Master Chip Select Outputs. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select pin. If an eSPI_CSx# pins is not in use, it shall be either pulled high or actively driven high.	O 1.8 VSB		
eSPI_CLK	A54	eSPI Master Clock Output. This pin provides the reference timing for all the serial input and output operations.	O 1.8 VSB		
eSPI_ALERT0# eSPI_ALERT1#	B52 B53	eSPI pins used by eSPI slave to request service from the eSPI master.	I 1.8 VSB	PU 10 KΩ 1.8 VSB	
eSPI_RST#	B56	eSPI Reset. Resets the eSPI interface for both master and slaves. The eSPI_RST# is typically driven from the eSPI master to eSPI slaves.	O 1.8 VSB	PD 75 KΩ	

Table 29 Boot SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
BOOT_SPI_CS#	B48	Chip select for carrier board SPI If the BOOT_SPI_CS# pin is not in use, it shall be either pulled high or actively driven high.	O VCC_BOOT_SPI	PU 10 KΩ 3.3 VSB	
BOOT_SPI_IO0 [1]	C50	Bidirectional 4 bit data path out of and into a carrier SPI flash operating in Serial Quad Interface (SQI) mode. If the flash memory device is operating in traditional Serial Peripheral Interface (SPI) mode, then signal BOOT_SPI_IO0 is used for getting serial data into the flash device (referred to as SI or MOSI in SPI Flash data sheets) and signal BOOT_SPI_IO1 is used to get serial data from the flash device (referred to as SO or MISO in flash data sheets)	I/O VCC_BOOT_SPI	PU 4.75 KΩ 3.3 VSB	
BOOT_SPI_IO1	C51				
BOOT_SPI_IO2	C52			PU 100 KΩ 3.3 VSB	
BOOT_SPI_IO3	C53			PU 100 KΩ 3.3 VSB	
BOOT_SPI_CLK	C54	Clock from module chipset to carrier SPI	O VCC_BOOT_SPI	PD 100 KΩ	
VCC_BOOT_SPI	B47	Power supply for carrier board SPI – sourced from module – nominally either 1.8V or 3.3V. The module shall provide a minimum of 100mA on VCC_BOOT_SPI. Carriers shall use less than 100mA from this power source. VCC_BOOT_SPI shall only be used to power SPI devices on the carrier board. The module vendor may choose what power domains the BOOT_SPI is active in.	Power (Out from module)		3.3 VSB (active in suspend state)

Note

1. *This signal has special functionality during the reset process. It may bootstrap some important functions of the module. For more information, refer to section 9.2 "Boot Strap Signals".*

Table 30 BIOS Select Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
BSEL2	B51	Boot Select pins. These pins distinguish between a SPI or eSPI BIOS boot and between an on—module or off-module BIOS. Pulled up on module to vendor specific power rail	I 3.3 VSB	PU 10 KΩ 3.3 VSB	Pulled up to 3.3 VSB (active in suspend state)
BSEL1	B50		I 3.3 VSB	PU 10 KΩ 3.3 VSB	
BSEL0	B49		I 3.3 VSB	PU 10 KΩ 3.3 VSB	

Table 31 DDI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI0_PAIR0+ DDI0_PAIR0-	D23 D22	Digital Display Interface 0 differential pair 0	O LV_DIFF		
DDI0_PAIR1+ DDI0_PAIR1-	D26 D25	Digital Display Interface 0 differential pair 1	O LV_DIFF		
DDI0_PAIR2+ DDI0_PAIR2-	D29 D28	Digital Display Interface 0 differential pair 2	O LV_DIFF		
DDI0_PAIR3+ DDI0_PAIR3-	D32 D31	Digital Display Interface 0 differential pair 3	O LV_DIFF		
DDI1_PAIR0+ DDI1_PAIR0-	A24 A23	Digital Display Interface 1 differential pair 0	O LV_DIFF		
DDI1_PAIR1+ DDI1_PAIR1-	A27 A26	Digital Display Interface 1 differential pair 1	O LV_DIFF		
DDI1_PAIR2+ DDI1_PAIR2-	A30 A29	Digital Display Interface 1 differential pair 2	O LV_DIFF		
DDI1_PAIR3+ DDI1_PAIR3-	A33 A32	Digital Display Interface 1 differential pair 3	O LV_DIFF		
DDI2_PAIR0+ DDI2_PAIR0-	E07 E06	Digital Display Interface 2 differential pair 0	O LV_DIFF		
DDI2_PAIR1+ DDI2_PAIR1-	E10 E09	Digital Display Interface 2 differential pair 1	O LV_DIFF		
DDI2_PAIR2+ DDI2_PAIR2-	E13 E12	Digital Display Interface 2 differential pair 2	O LV_DIFF		
DDI2_PAIR3+ DDI2_PAIR3-	E16 E15	Digital Display Interface 2 differential pair 3	O LV_DIFF		
DDI0_DDC_AUX_SEL DDI1_DDC_AUX_SEL DDI2_DDC_AUX_SEL	C26 C28 E18	Selects the function of DDI[0:2]_SCL_AUX+ and DDI[0:2]_SDA_AUX-. This pin shall have a 1M pull-down to logic ground on the module. If this input is unconnected on the carrier, the AUX pair is used for the DP AUX+/- signals. If pulled or driven high on the carrier, the AUX pair contains the HDMI[0:2] I^2C CRTL_CLK and CTRL_DAT signals.	I 3.3 V	PD 1 MΩ	
DDI0_SCL_AUX+ [1] DDI1_SCL_AUX+ DDI2_SCL_AUX+	D20 A21 E04	DP AUX+ function if DDI[0:2]_DDC_AUX_SEL is a no connect or driven to GND on the carrier.	I/O LV_DIFF	PD 100 KΩ	DDI0_SCL_AUX+ is a bootstrap signal (see note below). Enable strap is already populated.
		TMDS I^2C clock if DDI[0:2]_DDC_AUX_SEL is pulled or driven high on the carrier.	I/O OD 3.3 V		

DDI0_SDA_AUX- [1] DDI1_SDA_AUX- DDI2_SDA_AUX-	D19 A20 E03	DP AUX- function if DDI[0:2]_DDC_AUX_SEL is no connect	I/O LV_DIFF	PU 100 KΩ 3.3 V	DDI0_SDA_AUX- is a bootstrap signal (see note below). Enable strap is already populated.
		TMDS I²C data if DDI[0:2]_DDC_AUX_SEL is pulled high	I/O OD 3.3 V		
DDI0_HPD DDI1_HPD DDI2_HPD	C28 C29 E19	DDI Hot-Plug Detect	I 3.3 V	PD 100 KΩ	

Note

1. *These signals have special functionality during the reset process. They may bootstrap some important functions of the module. For more information, refer to section 9.2 "Boot Strap Signals".*

Table 32 DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP0_LANE0+ DP0_LANE0-	D23 D22	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI0_PAIR0+ and DDI0_PAIR0-	O LV_DIFF		
DP0_LANE1+ DP0_LANE1-	D26 D25	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI0_PAIR1+ and DDI0_PAIR1-	O LV_DIFF		
DP0_LANE2+ DP0_LANE2-	D29 D28	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI0_PAIR2+ and DDI0_PAIR2-	O LV_DIFF		
DP0_LANE3+ DP0_LANE3-	D32 D31	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI0_PAIR3+ and DDI0_PAIR3-	O LV_DIFF		
DP1_LANE0+ DP1_LANE0-	A24 A23	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-	O LV_DIFF		
DP1_LANE1+ DP1_LANE1-	A27 A26	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-	O LV_DIFF		
DP1_LANE2+ DP1_LANE2-	A30 A29	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-	O LV_DIFF		

DP1_LANE3+ DP1_LANE3-	A33 A32	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-	O LV_DIFF		
DP2_LANE0+ DP2_LANE0-	E07 E06	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-	O LV_DIFF		
DP2_LANE1+ DP2_LANE1-	E10 E09	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O LV_DIFF		
DP2_LANE2+ DP2_LANE2-	E13 E12	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O LV_DIFF		
DP2_LANE3+ DP2_LANE3-	E16 E15	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O LV_DIFF		
DP0_AUX+ [1] DP1_AUX+ DP2_AUX+	D20 A21 E04	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access Multiplexed with DDI[0:2]_SCL_AUX+	I/O LV_DIFF	PD 100 KΩ	DP0_AUX+ is a bootstrap signal (see note below). Enable strap is already populated.
DP0_AUX- [1] DP1_AUX- DP2_AUX-	D19 A20 E03	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access Multiplexed with DDI[0:2]_SDA_AUX-	I/O LV_DIFF	PU 100 KΩ 3.3 V	DP0_AUX- is a bootstrap signal (see note below). Enable strap is already populated.
DP0_HPD DP1_HPD DP2_HPD	C28 C29 E19	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3 V	PD 100 KΩ	

Note

1. *These signals have special functionality during the reset process. They may bootstrap some important functions of the module. For more information, refer to section 9.2 "Boot Strap Signals".*

Table 33 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS0_CLK+ TMDS0_CLK-	D32 D31	TMDS0 Clock differential pair Multiplexed with DDI0_PAIR3+ and DDI0_PAIR3-	O LV_DIFF		
TMDS1_CLK+ TMDS1_CLK-	A33 A32	TMDS1 Clock differential pair Multiplexed with DDI1_PAIR3+ and DDI0_PAIR3-	O LV_DIFF		
TMDS2_CLK+ TMDS2_CLK-	E16 E15	TMDS3 Clock differential pair Multiplexed with DDI2_PAIR3+ and DDI0_PAIR3-	O LV_DIFF		
TMDS0_DATA0+ TMDS0_DATA0-	D29 D28	TMDS0 lane 0 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI0_PAIR0+ and DDI0_PAIR0-	O LV_DIFF		
TMDS0_DATA1+ TMDS0_DATA1-	D26 D25	TMDS0 lane 1 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI0_PAIR1+ and DDI0_PAIR1-	O LV_DIFF		
TMDS0_DATA2+ TMDS0_DATA2-	D23 D22	TMDS0 lane 2 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI0_PAIR2+ and DDI0_PAIR2-	O LV_DIFF		
TMDS1_DATA0+ TMDS1_DATA0-	A30 A29	TMDS1 lane 0 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-	O LV_DIFF		
TMDS1_DATA1+ TMDS1_DATA1-	A27 A26	TMDS1 lane 1 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-	O LV_DIFF		
TMDS1_DATA2+ TMDS1_DATA2-	A24 A23	TMDS1 lane 2 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-	O LV_DIFF		
TMDS2_DATA0+ TMDS2_DATA0-	E13 E12	TMDS2 lane 0 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-	O LV_DIFF		
TMDS2_DATA1+ TMDS2_DATA1-	E10 E09	TMDS2 lane 1 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O LV_DIFF		
TMDS2_DATA2+ TMDS2_DATA2-	E07 E06	TMDS2 lane 2 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O LV_DIFF		
HDMI0_CTRL_CLK [1] HDMI1_CTRL_CLK HDMI2_CTRL_CLK	D20 A21 E04	TMDS I²C control clock Multiplexed with DDI[0:2]_SCL_AUX+	I/O OD 3.3V	PD 100 KΩ	HDMI0_CTRL_CLK is a bootstrap signal (see note below). Enable strap is already populated.
HDMI0_CTRL_DAT [1] HDMI1_CTRL_DAT HDMI2_CTRL_DAT	D19 A20 E03	TMDS I²C control data Multiplexed with DDI[0:2]_SDA_AUX-	I/O OD 3.3V	PU 100 KΩ 3.3 V	HDMI0_CTRL_DAT is a bootstrap signal (see note below). Enable strap is already populated.

HDMI0_HPD HDMI1_HPD HDMI2_HPD	C28 C29 E19	Detection of Hot Plug/Unplug and notification of the link layer Multiplexed with DP[0:2]_HPD	I 3.3V	PD 100 KΩ	

Note

1. *These signals have special functionality during the reset process. They may bootstrap some important functions of the module. For more information, refer to section 9.2 "Boot Strap Signals".*

Table 34 eDP Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eDP_TX0+ eDP_TX0-	A39 A38	eDP differential data pairs	O LV_DIFF		
eDP_TX1+ eDP_TX1-	A42 A41	eDP differential data pairs	O LV_DIFF		
eDP_TX2+ eDP_TX2-	A45 A44	eDP differential data pair	O LV_DIFF		
eDP_TX3+ eDP_TX3-	A48 A47	eDP differential data pairs	O LV_DIFF		
eDP_AUX+ eDP_AUX-	A36 A35	eDP AUX channel differential pair	I/O PCIE LV_ DIFF		
eDP_VDD_EN	C31	eDP power enable	O 3.3 V		
eDP_BKLT_EN	C32	eDP backlight enable	O 3.3 V		
eDP_BKLT_CTRL	C33	EDP backlight brightness control	O 3.3 V		
eDP_HPD	C30	eDP: Detection of Hot Plug / Unplug and notification of the link layer	I 3.3 V	PD 100 KΩ	

Table 35 MIPI CSI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CSI0_RX0+ CSI0_RX0-	G73 G72	CSI0 differential data input pairs 0	I LV_DIFF		
CSI0_RX1+ CSI0_RX1-	G76 G75	CSI0 differential data input pairs 1	I LV_DIFF		
CSI0_RX2+ CSI0_RX2-	G79 G78	CSI0 differential data input pairs 2	I LV_DIFF		
CSI0_RX3+ CSI0_RX3-	G82 G81	CSI0 differential data input pairs 3	I LV_DIFF		
CSI0_CLK+ CSI0_CLK-	G85 G84	CSI0 differential clock input pairs	I LV_DIFF		
CSI0_MCLK CSI1_MCLK	G89 H88	CSI Master Clock outputs for CSI0 and CSI1	O 1.8 V		
CSI0_I2C_DAT	G88	CSI-2 Mode: I²C Data line	I/O OD 1.8 V	PU 2.2 KΩ 1.8 V	
CSI0_I2C_CLK	G87	CSI-2 Mode: I²C Clock line	O OD 1.8 V	PU 2.2 KΩ 1.8 V	
CSI0_RST#	G90	Active low Reset signals for CSI port 0	O 1.8 V	PU 2.2 KΩ 1.8 V	
CSI0_ENA	G91	Active high Enable signals for CSI port 0	O 1.8 V	PU 2.2 KΩ 1.8 V	
CSI1_RX0+ CSI1_RX0-	H72 H71	CSI1 differential data input pairs 0	I LV_DIFF		Not supported
CSI1_RX1+ CSI1_RX1-	H75 H74	CSI1 differential data input pairs 1	I LV_DIFF		
CSI1_RX2+ CSI1_RX2-	H78 H77	CSI1 differential data input pairs 2	I LV_DIFF		
CSI1_RX3+ CSI1_RX3-	H81 H80	CSI1 differential data input pairs 3	I LV_DIFF		
CSI1_CLK+ CSI1_CLK-	H84 H83	CSI1 differential clock input pairs	I LV_DIFF		
CSI1_I2C_DAT	H87	CSI-2 Mode: I²C Data line	I/O OD 1.8 V		Not supported
CSI1_I2C_CLK	H86	CSI-2 Mode: I²C Clock line	O OD 1.8 V		
CSI1_RST#	H89	Active low Reset signals for CSI port1	O 1.8 V	PU 2.2 KΩ 1.8 V	
CSI1_ENA	H90	Active high Enable signals for CSI port 1	O 1.8 V		

Table 36 Soundwire Audio Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SNDW_DMIC_DAT0	C24	Bi-directional PCM audio data	I/O 1.8 V		
SNDW_DMIC_DAT1	C21	Bi-directional PCM audio data	I/O 1.8 V		
SNDW_DMIC_CLK0	C23	Clock for Soundwire transactions	O 1.8 V		
SNDW_DMIC_CLK1	C20	Clock for Soundwire transactions	O 1.8 V		

Table 37 I2S/Soundwire Audio Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2S_CLK/SNDW_CLK2/HDA_BCLK	B23	I2S Clock Alternative use as Soundwire 2 clock or HDA serial data clock	O 1.8 V		
I2S_DIN/SNDW_DAT2/HDA_SDI	B22	I2S Data In. This pin is an input in I2S mode. Alternative use as bi-directional Soundwire 2 data lane or HDA serial TDM data input	I/O 1.8 V		
I2S_DOUT/SNDW_DAT3/HDA_SDO	B20	I2S Data Out. This pin is an input in I2S mode. Alternative use as bi-directional Soundwire 2 data lane or HDA serial TDM data output	I/O 1.8 V	100 KΩ PD	
I2S_LRCLK/SNDW_CLK3/HDA_SYNC [1]	B19	I2S L/R Clock Alternative use as Soundwire 3 clock or HDA sample synchronization signal	O 1.8 V		Bootstrap signal (see note below). Enable strap is already populated.
I2S_MCLK/HDA_RST#	B21	I2S Master Clock Alternative use as HDA reset output	O 1.8 V		

Note

1. *This signal has special functionality during the reset process. It may bootstrap some important functions of the module. For more information, refer to section 9.2 "Boot Strap Signals".*

Table 38 Asynchronous Serial Port Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
UART0_TX	C89	Logic level asynchronous serial port transmit signal	O 3.3 V		
UART0_RX	C90	Logic level asynchronous serial port receive signal	I 3.3 V	PU 47.5 KΩ 3.3 V	
UART0_RTS#	C91	Logic level asynchronous serial port Request to Send signal, active low	O 3.3 V		
UART0_CTS#	C92	Logic level asynchronous serial port Clear to Send input, active low	I 3.3 V	PU 47.5 KΩ 3.3 V	
UART1_TX	B87	Logic level asynchronous serial port transmit signal	O 3.3 V		
UART1_RX	B88	Logic level asynchronous serial port receive signal	I 3.3 V	PU 47.5 KΩ 3.3 V	
UART1_RTS#	B89	Logic level asynchronous serial port Request to Send signal, active low	O 3.3 V		
UART1_CTS#	B90	Logic level asynchronous serial port Clear to Send input, active low	I 3.3 V	PU 47.5 KΩ 3.3 V	

Table 39 I²C Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C0_CLK	C93	Clock I/O line for the general purpose I2C0 port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
I2C0_DAT	C94	Data I/O line for the general purpose I2C0 port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
I2C0_ALERT#	C95	Alert input / interrupt for I2C0	I 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
I2C1_CLK	C96	Clock I/O line for the general purpose I2C1 port	I/O OD 1.8 VSB	PU 4.75 KΩ 1.8 VSB	
I2C1_DAT	C97	Data I/O line for the general purpose I2C1 port	I/O OD 1.8 VSB	PU 4.75 KΩ 1.8 VSB	

Table 40 IPMB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
IPMB_CLK	B91	Clock I/O line for the multi-master IPMB port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
IPMB_DAT	B92	Data I/O line for the multi-master IPMB port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	

Table 41 General Purpose SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GP_SPI_MISO	B94	Serial data into the COM-HPC® module from the carrier GP_SPI device ("Master In Slave Out")	I 3.3 V	PU 10 KΩ 3.3 V	
GP_SPI_MOSI	B93	Serial data from the COM-HPC® module to the carrier GP_SPI device ("Master Out Slave In")	O 3.3 V		
GP_SPI_CLK	B99	Clock from the module to carrier GP_SPI device	O 3.3 V		
GP_SPI_CS0#	B95	GP_SPI chip selects, active low	O 3.3 V	PU 10 KΩ 3.3 V	
GP_SPI_CS1#	B96			PU 10 KΩ 3.3 V	
GP_SPI_CS2#	B97			PU 10 KΩ 3.3 V	Not supported
GP_SPI_CS3#	B98			PU 10 KΩ 3.3 V	Not supported
GP_SPI_ALERT#	B100	Alert (interrupt) from a carrier GP_SPI device to the module	I 3.3 V	PU 10 KΩ 3.3 V	

Table 42 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B02	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down (with a sustained low).	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
RSTBTN#	C02	Reset button input. The RSTBTN# may be level sensitive (active low) or may be triggered by the falling edge of the signal. The module PLTRST# signal (below) should not be released (driven or pulled high) while the RSTBTN# is low. For situations when RSTBTN# is not able to reestablish control of the system, VIN_PWR_OK or a power cycle may be used.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
PLTRST#	A12	Platform Reset: output from module to carrier board. Active low. Issued by module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.	O 3.3 VSB	PD 100 KΩ	
VIN_PWR_OK	C06	Power OK from main power supply. A high value indicates that the power is good.	I 3.3 V	PU 10 KΩ 3.3 VSB	

SUS_S3#	B08	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the carrier board should be used to enable the non-standby power on a typical ATX supply. Even in single input supply system implementations (AT mode, no standby input), the SUS_S3# module output should be used disable any carrier voltage regulators when SUS_S3# is low, to prevent bleed leakage from carrier circuits into the module.	O 3.3 VSB	PD 100 KΩ	
SUS_S4_S5#	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3 VSB	PD 100 KΩ	
SUS_CLK	A87	32.768 kHz +/- 100 ppm clock used by carrier peripherals such as M.2 cards in their low power modes.	O 3.3 VSB		
WAKE0#	D10	PCI Express wake up signal.	I/O 3.3 VSB	PU 1 KΩ 3.3 VSB	
WAKE1#	D11	General purpose wake up signal. May be used to implement wake- up on PS2 keyboard or mouse activity.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
BATLOW#	A11	Indicates that external battery is low. This port provides a battery-low signal to the module for orderly transitioning to power saving or power cut-off ACPI modes.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
LID#	B45	LID switch. Low active signal used by the ACPI operating system for a LID switch.	I 3.3 VSB	PU 47.5 KΩ 3.3 VSB	
SLEEP#	B46	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
TAMPER#	B06	Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a Tamper event.	I 3.3 VSB	PU 1 MΩ 3.3 VSB	
AC_PRESENT	D34	Driven hard low on carrier if system AC power is not present	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
RSMRST_ OUT#	B86	This is a buffered copy of the internal module RSMRST# (Resume Reset, active low) signal. The internal module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable. USB devices on the carrier that are to be active in S5 / S3 / S0 should not have their 5V supply applied before RSMRST_OUT# goes high. RSMRST_OUT# shall be a 3.3V CMOS module output, active in all power states.	O 3.3 VSB		Not supported

Table 43 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_SHUTDOWN	E01	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs. Pull-down / disable on module if RAPID_SHUTDOWN pin is not asserted.	I 5 VSB	PD 100 KΩ	Not supported

Table 44 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CARRIER_HOT#	C04	Input from off-module temp sensor indicating an over-temp situation.	I 3.3 V	PU 10 KΩ 3.3 V	
THERMTRIP#	B04	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3 V	PD 100 KΩ	

Table 45 SMBus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CLK	C86	System Management Bus bidirectional clock line.	I/O OD 3.3 VSB	PU 100 KΩ 3.3 VSB	
SMB_DAT	C87	System Management Bus bidirectional data line.	I/O OD 3.3 VSB	PU 100 KΩ 3.3 VSB	
SMB_ALERT# [1]	C88	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3 VSB	PU 100 KΩ 3.3 VSB	Bootstrap signal (see note below).

Note

1. *This signal has special functionality during the reset process. It may bootstrap some important functions of the module. For more information, refer to section 9.2 "Boot Strap Signals".*

Table 46 General Purpose Input Output Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPIO_00	A88	General purpose input / output pins. Upon a hardware reset, these pins should be configured as inputs. As inputs, these pins should be able to generate an interrupt to the module host.	I/O 3.3 VSB	PU 100 KΩ 3.3 VSB	
GPIO_01	A89				
GPIO_02	A90				
GPIO_03	A91				
GPIO_04	A92				
GPIO_05	A93				
GPIO_06	A94				
GPIO_07	A95				
GPIO_08	A96				
GPIO_09	A97				
GPIO_10	A98				
GPIO_11	A99				

Table 47 Module Type Definition Signal Description

<table>
<tr><th>Signal</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>TYPE0
TYPE1
TYPE2</td><td>A100
C100
D100</td><td>The TYPE pins indicate to the carrier board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). These pins shall be pulled up on the carrier, to carrier standby voltage rail of 5V or less. Carrier hardware reads the level on these straps.
<table>
<tr><th></th><th colspan="3">Module Connections</th><th>Meaning</th></tr>
<tr><th>Ref</th><th>TYPE2</th><th>TYPE1</th><th>TYPE0</th><th></th></tr>
<tr><td>7</td><td>NC</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>6</td><td>NC</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>5</td><td>NC</td><td>GND</td><td>NC</td><td>Reserved</td></tr>
<tr><td>4</td><td>NC</td><td>GND</td><td>GND</td><td>Server module - Fixed 12 V input</td></tr>
<tr><td>3</td><td>GND</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>2</td><td>GND</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>1</td><td>GND</td><td>GND</td><td>NC</td><td>Client module - Wide range 8 V to 20 V input</td></tr>
<tr><td>0</td><td>GND</td><td>GND</td><td>GND</td><td>Client module - Fixed 12 V input</td></tr>
</table>
The module shall implement all three TYPE[x] pins per the table above.
The carrier board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX PS_ON# signal to an ATX power supply or otherwise deactivates VCC to the COM- HPC module) if an incompatible module pin-out type is detected. All three TYPE[x] pins should be monitored by the carrier. The carrier board logic may also implement a fault indicator such as an LED.</td><td>PDS</td><td>The conga-HPC/cTLH is a Ref 1 Type module (Client module - Wide range 8V to 20V input) therefore the TYPE2 and TYPE1 pins are connected to GND and TYPE0 pin is not connected</td></tr>
</table>

Table 48 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WD_OUT	B11	Output indicating that a watchdog time-out event has occurred. Refer to Section 5.4 for details.	O 3.3 V	PD 100 KΩ	
WD_STROBE#	B10	Strobe input to watchdog timer. Periodic strobing prevents the watchdog, if enabled, from timing out.	I 3.3 V	PU 10 KΩ 3.3 V	
FAN_PWMOUT	C11	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3 V		
FAN_TACHIN	C12	Fan tachometer input for a fan with a two pulse output.	I OD 3.3 V	PU 47.5 KΩ 3.3 V	
TEST#	F85	module input to allow vendor specific module test mode(s). Carrier designers should leave this pin open on the carrier. Designers involved in the design of specialty carriers for module test may pull this line to GND or possibly to a module specific analog voltage between GND and 3.3V to select a test mode.	I OD 3.3 VSB	PU 10 KΩ 3.3 VSB	
RSVD	E69-E77 E84-E85 F01-F18 F68-F69 G01;G69-G70 H68-H69	Reserved pins. These may be assigned functions in future versions of this specification. Reserved pins shall not be connected to anything, and shall not be connected to each other.			Not connected

Table 49 External Power Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	A01-A09 B01,B03, B05, B07, B09 C01, C03, C05, C07, C09 D01-D09	Primary power input: fixed +12V on the Client Type 0; wide range +8V to +20V on the Client Type 1; fixed +12V on the Server. Refer to Section 8 "Module Input Power Specifications" further details. All available VCC pins on the connector shall be used.			
VCC_5V_SBY	B24	Standby power input: +5.0V nominal. Refer to Section 8 "Module Input Power Specifications" for further details. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.			
VCC_RTC	A86	Real-time clock circuit-power input. Nominally +3.0V. Refer to Section 8 "Module Input Power Specifications" for details.			
GND	A10, A13, A16, A19, A22, A25, A28, A31, A34, A37, A40, A43, A46, A49, A55, A58, A61, A64, A67, A70, A73, A76, A79, A82, A85	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane(s).			

GND	B12, B15, B18, B42, B57, B60, B63, B66, B69, B72, B75, B78, B81, B84	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane(s).			
GND	C10, C13, C16, C19, C22, C25, C34, C37, C40, C43, C46, C49, C55, C58, C61, C64, C67, C70, C73, C76, C79, C82, C85	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane(s).			
GND	D12, D15, D18, D21, D24, D27, D30, D33, D36, D39, D42, D45, D48, D51, D54, D57, D60, D63, D66, D69, D72, D75, D78, D81, D84, D87, D90, D93, D96	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane(s).			
GND	E02, E05, E08, E11, E14, E17, E20, E23, E26, E29, E32, E35, E38, E41, E44, E47, E50, E53, E56, E59, E62, E65, E68, E83, E86, E89, E92, E95	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane(s).			
GND	F19, F22, F25, F28, F31, F34, F37, F40, F43, F46, F49, F52, F55, F58, F61, F64, F67, F70, F73, F76, F79, F82, F88, F91, F94	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane(s).			
GND	G02, G05, G08, G11, G14, G20, G23, G26, G29, G32, G35, G38, G41, G44, G47, G50, G53, G56, G59, G62, G65, G68, G71, G74, G77, G80, G83, G86, G92, G95	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane(s).			
GND	H01, H04, H07, H10, H13, H16, H19, H22, H25, H28, H31, H34, H37, H40, H43, H46, H49, H52, H55, H58, H61, H64, H67, H70, H73, H76, H79, H82, H85, H91, H94, H97	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane(s).			

9.2 Boot Strap Signals

Table 50 Boot Strap Signal Descriptions

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
BOOT_SPI_IO0	C50	Bidirectional 4 bit data path out of and into a carrier SPI flash operating in Serial Quad Interface (SQI) mode.	I/O VCC_BOOT_SPI	PU 4.7 KΩ 3.3 VSB	
DDI0_SDA_AUX-	D19	DP AUX- function if DDI[0:2]_DDC_AUX_SEL is no connect	I/O LV_DIFF	PU 100 KΩ 3.3 V	
		TMDS I²C data if DDI[0:2]_DDC_AUX_SEL is pulled high	I/O OD 3.3 V		
DP0_AUX-		Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O LV_DIFF	PU 100 KΩ 3.3 V	
HDMI0_CTRL_DAT		TMDS I²C control data Multiplexed with DDI[0:2]_SDA_AUX-	I/O OD 3.3V	PU 100 KΩ 3.3 V	
SMB_ALERT#	C88	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
DDI1_SDA_AUX-	D20	DP AUX- function if DDI[0:2]_DDC_AUX_SEL is no connect	I/O LV_DIFF	PU 100 KΩ 3.3 V	
		TMDS I²C data if DDI[0:2]_DDC_AUX_SEL is pulled high	I/O OD 3.3 V		
DP1_AUX-		Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O LV_DIFF	PU 100 KΩ 3.3 V	
HDMI1_CTRL_DAT		TMDS I²C control data Multiplexed with DDI[0:2]_SDA_AUX-	I/O OD 3.3V	PU 100 KΩ 3.3 V	
I2S_LRCLK/SNDW_CLK3	B19	I2S L/R Clock Alternative use as Soundwire 3 clock	O 1.8 V		
USB0_LSRX	B40	Sideband RX interface for USB4 Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PU 4.75 KΩ 3.3 VSB	
USB1_LSRX	B38	Sideband RX interface for USB4 Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PU 4.75 KΩ 3.3 VSB	

Note

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), the COM-HPC® or chipset internally implemented resistors pull these signals to the correct state.

Caution

No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM-HPC® module to malfunction or cause irreparable damage to the module.

10 System Resources

10.1 I/O Address Assignment

The I/O address assignment of the conga- HPC/cTLH module is functionally identical with a standard PC/AT.

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

10.1.1 eSPI Bus

On the conga-HPC/cTLH, the PCI Express bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI bus. Only specified I/O ranges are forwarded to the eSPI bus.

In the congatec Embedded BIOS, the I/O address ranges E00h - EFFh are sent to the eSPI bus. These address are always used internally by the congatec board controller.

The conga- HPC/cTLH doesn't route the eSPI bus to the carrier because the chipset has solely one ESPI chip select which is already occupied by the congatec board controller on the module internally.

Note

The default congatec BIOS does not support eSPI CS1 for external devices. For eSPI CS1 support, you need a customized congatec BIOS.

10.2 PCI Configuration Space Map

Table 51 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	HOST and DRAM Controller
00h	02h	00h	Integrated Graphics Device
00h	04h	00h	Dynamic Tuning Technology
00h	01h	00h	PEG10 (connector PCIE port 16-31)
00h	07h	00h	Integrated Thunderbolt PCI Express Root Port 0
00h	07h	01h	Integrated Thunderbolt PCI Express Root Port 1
00h	08h	00h	Gaussian Mixture Model and Neural Network Accelerator
00h	0Ah	00h	Crash-log SRAM
00h	0Dh	00h	Integrated Thunderbolt USB3 xHCI Controller
00h	0Dh	02h	Integrated Thunderbolt DMA Controller 0
00h	14h	00h	USB3 xHCI Controller
00h	14h	02h	Shared SRAM Controller
00h (Note1)	16h	00h	Management Engine (ME) Interface 1
00h (Note1)	16h	01h	Intel ME Interface 2
00h (Note1)	16h	02h	ME IDE Redirection (IDE-R) Interface
00h (Note1)	16h	03h	ME Keyboard and Text (KT) Redirection
00h (Note1)	16h	04h	Intel ME Interface 3
00h (Note1)	16h	05h	Intel ME Interface 4
00h	17h	00h	SATA Controller
00h (Note2)	1Ch	00h	PCI Express Root Port 1 operating in x4 mode
00h (Note2)	1Ch	01h	PCI Express Root Port 2 operating in x4 mode
00h (Note2)	1Ch	02h	PCI Express Root Port 3 operating in x4 mode
00h (Note2)	1Ch	03h	PCI Express Root Port 4 operating in x4 mode
00h (Note2)	1Ch	04h	PCI Express Root Port 5 operating in x1 mode (connector PCIe port 0)
00h (Note2)	1Ch	05h	PCI Express Root Port 6 operating in x1 mode (connector PCIe port 1)
00h (Note2)	1Ch	06h	PCI Express Root Port 7 operating in x1 mode (connector PCIe port 2)
00h (Note2)	1Ch	07h	PCI Express Root Port 8 operating in x1 mode (connector PCIe port 3)
00h (Note2)	1Dh	00h	PCI Express Root Port 13 – GBE 0
00h (Note2)	1Dh	01h	PCI Express Root Port 14 – GBE 1

00h (Note2)	1Dh	02h	PCI Express Root Port 15 – SATA 0
00h (Note2)	1Dh	03h	PCI Express Root Port 16 – SATA 1
00h (Note2)	1Dh	04h	PCI Express Root Port 9 operating in x4 mode (connector PCIe port 4)
00h (Note2)	1Dh	05h	PCI Express Root Port 10 operating in x4 mode (connector PCIe port 5)
00h (Note2)	1Dh	06h	PCI Express Root Port 11 operating in x4 mode (connector PCIe port 6)
00h (Note2)	1Dh	07h	PCI Express Root Port 12 operating in x4 mode (connector PCIe port 7)
00h (Note2)	06h	00	CPU PCIE 4 (connector PCIe port 8-11)
00h (Note2)	1Bh	00h	PCI Express Root Port 17 operating in x4 mode (connector PCIe port 12)
00h (Note2)	1Bh	01h	PCI Express Root Port 18 operating in x4 mode (connector PCIe port 13)
00h (Note2)	1Bh	02h	PCI Express Root Port 19 operating in x4 mode (connector PCIe port 14)
00h (Note2)	1Bh	03h	PCI Express Root Port 20 operating in x4 mode (connector PCIe port 15)
00h (Note2)	1Bh	04h	PCI Express Root Port 21 operating in x4 mode (connector PCIe port 32)
00h (Note2)	1Bh	05h	PCI Express Root Port 22 operating in x4 mode (connector PCIe port 33)
00h (Note2)	1Bh	06h	PCI Express Root Port 23 operating in x4 mode (connector PCIe port 34)
00h (Note2)	1Bh	07h	PCI Express Root Port 24 operating in x4 mode (connector PCIe port 35)
00h	1Fh	00h	PCI to eSPI Bridge
00h	1Fh	03h	Intel® High Definition Audio
00h	1Fh	04h	SMBus Controller
00h	1Fh	05h	SPI Flash Controller
04h	00h	00h	Upstream Port of PCI Express switch (iTBT 0)
05h	01h	00h	Downstream Port of PCI Express switch
06h	00h	00h	Integrated Thunderbolt Controller iTBT
07h – 31h			Reserved for PCIe topology connected to Thunderbolt Port 0. In the following BIOS setup menu, you can specify the number of extra busses reserved per Thunderbolt Port. The default is 42 decimal busses for each port: Advanced -> Platform Settings -> TCSS Platform Settings -> Thunderbolt Configuration -> Integrated Thunderbolt Configuration -> ITBT Root Port Configuration.

32h – 58h			Reserved for PCIe topology connected to Thunderbolt Port 1 (iTBT 1)
02h	00h	00h	PCIe device inserted in PCIE slot 8-11
5Ch	00h	00h	PCIe device inserted in PCIE slot 4-7
5Ah	00h	00h	PCIe device inserted in PCIE slot 32-47
59h	00h	00h	PCIe device inserted in PCIE slot 8-11
5Dh	00h	00h	Intel Ethernet controller GBE 0
5Eh	00h	00h	Intel Ethernet controller GBE 1
01h (Note3)	00h	00h	PCIe device connected to PEG Root Port 1:0

Note

1. *In the standard configuration, the Intel Management Engine (ME) related devices are partly present or not present at all.*
2. *The PCI Express ports are visible only if a device is attached to the PCI Express slot on the carrier board.*
3. *The table represents a case when a single function PCI/PCIe device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*
4. *Internal PCI devices not connected to the conga- HPC/cTLH are not listed.*

11 BIOS Setup Description

The BIOS setup description of the conga-HPC/cTLH can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note “AN42 - BIOS Setup Description” available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

11.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST. The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

11.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-HPC/cTLH is identified as GHTLR1xx or GQTLR1xx, where:

- R is the identifier for a BIOS ROM file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The binary size for GHTL and GQTL is 32 MB.

11.3 Updating the BIOS

BIOS updates are recommeded to correct platform issues or enhance the feature set of the module. The conga-HPC/cTLH features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

11.3.1 Update from External Flash

For instructions on how to update the BIOS from external flash, refer to the AN7_External_BIOS_Update.pdf application note on the congatec website at http://www.congatec.com.

11.4 Supported Flash Devices

The conga-HPC/cTLH supports:

- Winbond W25Q256JVEIQ (DFN5x6 package) 32 MB
- GigaDevice GD25B256DYIG (DFN5x6 package) 32 MB
- Winbond W25Q256JVFIQ (SOIC-16 package) 32 MB

The flash devices can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to the Application Note "AN7_External_BIOS_Update.pdf" on the congatec website at http://www.congatec.com.