



FPA2 Universal Adapter for EPI

Short description of congatec's universal flat panel adapter

Short Description

Revision 1.0



Revision History

RevisionDate (dd.mm.yy)AuthorChanges1.023.12.10GDAOfficial release

FPA2m10



Preface

This short description provides information about the features, connectors and schematics for the FPA2.

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Symbols





Warnings indicate conditions that, if not observed, can cause personal injury.



Cautions warn the user about how to prevent damage to hardware or loss of data.

>Note

Notes call attention to important information that should be observed.



Describes the connector that must be used with the FPA2, not the connector found on the FPA2.



Link to connector layout diagram

This link icon is located in the top right corner of each page. It provides a direct link to the connector layout on page 10 of this document.



Terminology

Term	Description
EPI	Embedded Panel Interface
EDID™	Extended Display Identification Data is a VESA standard data format that contains basic information about a display
FPA2	Flat panel Prototype Adapter 2
LVDS	Low Voltage Differential Signaling, a low noise, low power, low amplitude method for high-speed data transmission
TTL	Transistor-Transistor logic, a common type of digital circuit in which the output is derived from two transistors
I ² C Bus	Inter-Integrated Circuit Bus: is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system.

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1 Introduction

FPA2 (Flat panel Prototype Adapter 2) is a universal adapter board that has been designed for use with congatec's Embedded Panel Interface (EPI). It can be used for either prototyping, demonstration purposes, or for debugging certain issues. It may also serve as a reference for the implementation of panel adaptations on customer specific carrier boards. This document is one of several that should be referred to while using or implementing FPA2 features and/or functions. The following congatec documents should be referenced:

- congatec Backlight Control Design Guide (DG_BacklightControl_1x.pdf)
- congatec System Utility (CGUTLm1x.pdf)
- The User's Guide for the congatec product that will be used with the FPA2.

Links to these documents can be found at www.congatec.com. The following are industry standard documents that should be referred to as well. They include:

- EPI Specification from the EPI consortium at www.epi-standard.org
- E-EDIDTM Implementation Guide Version 1.0 from VESA under the file name **EEDIDguideV1.pdf** at www.vesa.org/public
- Open LVDS Display Interface Specification v0.95 from National Semiconductor at http://www.national.com/appinfo/fpd/0,2132,228,00.html
- Digital Visual Interface DVI Revision 1.0 from the Digital Display Working Group found at www.ddwg.org/downloads.asp
- SPWG v3.5 Specification from the Standard Panel Working Group found at www.spwg.org

The FPA2 is capable of several functions designed to assist you during the evaluation and implementation of flat panel support. They are as follows:

- Power sequencing for panel and backlight.
- Serial I²C EEPROM to store the EPI enhanced EDID[™] file.
- D/A converter enabling backlight brightness control.
- 3.3V power supply for low-voltage panels.
- Panel and backlight supply voltage can be configured by jumpers.



2 Connector Layout

The connector layout picture below shows the silkscreen of the FPA2, which indicates pinout as well as name designators.

Select the Adobe 'Zoom-In-Tool' and zoom in on a given component to see the descriptive silkscreen text. Hover over the component and the 'Zoom-In-Tool' will change indicating there is a link. Click on the link to navigate to the area in the document where the component is described in detail.

Use the mouse icon in the top left hand corner of the destination page to return to the connector layout picture.







3 Connectors

The following section describes the connectors located on the FPA2. Each connector's pinout is listed as well a description of the mating connector that should be used to connect to the specific connector located on the FPA2.

3.1 X1 Connector EPI Input

For a detailed description of the signals listed in the pinout table below refer to the EPI Specification.

Pin	Signal Name	LVDS mode	TTL mode	Pin	Signal Name	LVDS mode	TTL mode
1	LCD_DDC_DAT	I ² C EP	I DATA	18	LCDD9	FL3P	GREEN3
2	LCD_DDC_CLK	I ² C EP	I Clock	19	LCDD8	FL3N	GREEN2
3	-	Currently	y unused	20	GND	GN	ND
4	-	Currently	y unused	21	LCDD10	SLON	GREEN4
5	GND	GI	ND	22	LCDD11	SL0P	GREEN5
6	LCDD0	FLON	RED0	23	GND	GN	ND
7	LCDD1	FL0P	RED1	24	LCDD12	SL1N	BLUE0
8	LCD_VDD_EN	Enable Pa	anel Power	25	LCDD13	SL1P	BLUE1
9	LCDD2	FL1N	RED2	26	GND	GN	ND
10	LCDD3	FL1P	RED3	27	LCDD14	SL2N	BLUE2
11	LCD_BKLT_EN	Enable Bac	klight Power	28	LCDD15	SL2P	BLUE3
12	LCDD5	FL2P	RED5	29	GND	GN	ND
13	LCDD4	FL2N	RED4	30	LCDD17	SLCP	BLUE5
14	LCD_VSYNC		VSYNC	31	LCDD16	SLCN	BLUE4
15	LCDD6	FLCN	GREEN0	32	Detect#	Currently	/ unused
16	LCDD7	FLCP	GREEN1	33	LCDD19	SL3P	DE
17	LCD_HSYNC		HSYNC	34	LCDD18	SL3N	DCLK

EPI Input (X1)

33 31 29 27 25 23 21 19 17 15 13 11 9 7 5 3 1 1

Connector Type

34 pin, 2 row 2mm grid female



3.2 X7 Power Input

The power to the FPA2 is supplied via a 3.5" floppy connector. A quadratic pad on the bottom side indicates pin one. The pinout and connector are described below.

3.5" Floppy	Pin	Signal Name
Connector	1	12V
	2	GND
1■ 2■ 3■ 4■	3	GND
	4	5V



Standard 4 pin 3.5" floppy power connector female





3.3 X2 TTL Output-Single/First Pixel Mode Data

2

1∎ 3∎ 5∎

The X2 connector is used for LVDS/TTL mode. It is responsible for delivering the 18/24 bit single pixel mode data. The pinout and connector are described below.

TTL Output Single/First Pixel (X2)



40 pin, 2 row 2mm grid female

4	6 🗖	8 🗖	10 12	14 🔳 16 🔳 18 🔳 2	20 🗖 22 🗖 24 🗖 2	26 🔳 28 🔳	30 🔳 32 🔳 34 🔳 36	■ 38 ■ 40 ■
3	5 🔳	7 🔳	9 🔳 11 🔳	13 🔳 15 🔳 17 🔳 1	9 🗖 21 🔳 23 🔳 2	25 🔳 27 🔳	29 🔳 31 🔳 33 🔳 35	37 🖬 39 🔳
					1			
			Pin	Signal		Pin	Signal	
			1	GND		21	GREEN5	
			2	DCLK		22	GND	
			3	GND		23	GREEN6	
			4	RED0		24	GREEN7	
			5	RED1		25	BLUE0	
			6	RED2		26	GND	
			7	GND		27	BLUE1	
			8	RED3		28	BLUE2	
			9	RED4		29	BLUE3	
			10	RED5		30	GND	
			11	GND		31	BLUE4	
			12	RED6		32	BLUE5	
			13	RED7		33	BLUE6	
			14	GREEN0		34	GND	
			15	GND		35	BLUE7	
			16	GREEN1		36	HSYNC	
			17	GREEN2		37	VSYNC	
			18	GREEN3		38	GND	
			19	GND		39	DE	
			20	GREEN4		40	GND	





3.4 X6 Panel Power Connector

The power connector provides power and display orientation control for the flat panel. See section 5 of this document for jumper configuration settings. The pinout and connector are described below.



Pa	ne	el F	' 0\	Ne	r ()	(6)
	2	4	6	8 🔳	10	
	1	3	5	7 🔳	9 🔳	

10 pin, 2 row 2.54mm grid female

Pin	Function	Pin	Function
1	Switched VDD	6	Backlight On (active high)
2	Switched VBKL	7	Backlight Dimmer 0-4.7V
3	+5V	8	Backlight On
4	+12V	9	GND
5	Enable Display (active high)	10	GND





4 Brightness Control

The backlight control is implemented using a MAXIM MAX5362MEUK voltage-output, 6-bit DAC that offers full 6-bit performance with less than 1LSB integral nonlinearity (INL) error and less than 1LSB differential nonlinearity (DNL) error ensuring monotonic performance. The device uses a simple two-wire, fastmode I2C-compatible serial interface. It includes an internal reference, an output buffer, and low-current shutdown mode, making it ideal for low-power, highly integrated applications. It is supported by the congatec embedded BIOS allowing for backlight brightness control. For additional information refer to the manufacturer's datasheet.



Note

For more information about this subject refer to the EPI Specification and the user's guide for the congatec System Utility as well as the congatec Backlight Control Design Guide.





5 Configuration

5.1 Timing

The panel timing is configured by an EPI/EDID[™] configuration file, which is either stored on the congatec module or inside the FPA2 onboard EEPROM. It can be accessed through the I²C bus via the congatec System Utility.

Note

For more information about this subject refer to the EPI Specification and the user's guide for the congatec System Utility.

5.2 Jumper Configurations



JP1-3, 2,54mm grid jumpers



JP3: Backlight Polarity Config

Jumper JP3	Configuration
1 - 2	Backlight enable HIGH active (default)
2 - 3	Backlight enable LOW active

JP1: Panel voltage selector

Jumper JP1	Configuration
1 - 2	+5V (default)
2 - 3	+3.3V

JP2: Backlight inverter voltage

Jumper JP2	Configuration
1 - 2	+12V (default)
2 - 3	+5V



6 Mechanical Dimensions





7 Maximum Ratings

7.1 **Power Ratings**

Input Voltage:

Signal	Min. V	Max. V
5V	4.6V	5.2V
12V	4.5V	12.5V

Output Current:

Signal	@ Voltage	Max. Current
Switched VDD	3.3V	0.6A
	5V	2A
	12V	2A
Switched VBKL	5V / 12V	2A

7.2 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%



The above operating temperatures must be strictly adhered to at all times. The maximum operating temperature refers to any measurable spot on the modules surface.

Humidity specifications are for non-condensing conditions.



8 FPA2 Schematics









FPA2 Schematics Continued

