COM Express™ conga-CA6

Intel® Atom™ processor E6x0/E6x0T series with an Intel® Platform Controller Hub EG20T

User's Guide

Revision 1.0

Revision History

Revision	Date (yyyy.mm.dd)	Author	Changes
0.1	2012.05.22	GDA	• Preliminary release
0.2	2013.07.17	AEM	• Added section 1 “Introduction”. Moved COM Express™ Concept and Options Information to section 1 “Introduction”. • Updated section 2.5 “Power Consumption”. • Deleted RTC alarm option and the option to use USB Mouse/Keyboard Event as Wake event in section 7.3 “ACPI Suspend Modes and Resume Events” because these are not supported in the BIOS. • Updated section 10 “BIOS Description Setup”.
0.3	2013.09.26	AEM	• Deleted conga-CA6 variants that are no longer available in sections 1 “Introduction” and 2.5 “Power Consumption”. • Updated section 2.5 “Power Consumption”. Added CMOS battery current in section 2.6.1 “CMOS Battery Power Consumption”. Updated the block diagram in section 3 “Block diagram”. • Deleted section 6.4 “Security Features” because the conga-CA6 does not support TPM. • Official release.

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-CA6. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide
COM Express™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
PCH	Platform Controller Hub
PATA	Parallel ATA
HDA	High Definition Audio
APU	Accelerated Processor Unit
FCH	Fusion Controller Hub
DDI	Digital Display Interface
DP	DisplayPort
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

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List of Tables

1 Introduction

COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available today. COM Express™ modules are available in the following form factors:

- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x 110mm

The COM Express™ specification 2.0 defines five different pinout types.

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports
Type 1	A-B	Up to 6			1
Type 2	A-B C-D	Up to 22	32 bit	1	1
Type 3	A-B C-D	Up to 22	32 bit		3
Type 4	A-B C-D	Up to 32		1	1
Type 5	A-B C-D	Up to 32			3
Type 6	A-B C-D	Up to 24			1
Type 10	A-B	Up to 4			1

The conga-CA6 modules use the COM Express™ Type 2, Rev 2.0 pinout definition. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are a legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 2 pinout provides the ability to offer 32-bit PCI, Parallel ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another- no redesign is necessary.

conga-CA6 Options Information

The conga-CA6 currently offers four variants. This user's guide describes all of the available features these variants offer. Below you will find an order table showing the base configuration modules that are currently offered by congatec AG. For more information about the conga-CA6 variants offered by congatec, contact your local congatec sales representative or visit the congatec website at www.congatec.com.

conga-CA6

Part-No.	061203	061201	061213	061211
Processor	Intel® Atom™ E680 1.6 GHz	Intel® Atom™ E640 1.0 GHz	Intel® Atom™ E680T 1.6 GHz	Intel® Atom™ E640T 1.0 GHz
L2 Cache	512kB	512kB	512kB	512kB
Onboard Memory up to 2GB	1GB DDR2 (800 MT/s)	1GB DDR2 (667 MT/s)	1GB DDR2 (800 MT/s)	1GB DDR2 (667 MT/s)
External PCI Express Lane(s)	2	2	2	2
Gigabit Ethernet	Yes	Yes	Yes	Yes
Onboard Solid-State Drive (SSD)	No	No	No	No
CPU TDP	3.9 W	3.6 W	3.9 W	3.6 W

2 Specifications

2.1 Feature List

Table 1 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 2 Rev. 2.0 (compact size 95 x 95mm)
Processor	Intel® Atom™ E680 1.6 GHz with 512kB L2 cache Intel® Atom™ E640 1.0 GHz with 512kB L2 cache Intel® Atom™ E680T 1.6 GHz with 512kB L2 cache (industrial grade processor) Intel® Atom™ E640T 1.0 GHz with 512kB L2 cache (industrial grade processor)
Memory	Onboard DDR 2 up to 2GB
Chipset	Intel® Platform Controller Hub (PCH) EG20T
Audio	HDA (High Definition Audio)/digital audio interface with support for multiple codecs
Ethernet	Gigabit Ethernet, Micrel KSZ9021RN (commercial temp.) or KSZ9021RNI (industrial temp.) and Phy
Graphics Options	Integrated 3D graphics engine. Dual independent display support. • Flat panel Interface (integrated) 80 MHz LVDS Transmitter Supports 1x18 and 1x24 bit TFT configurations. Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3) Resolutions 640x480 up to 1280x768. • AUX Output 1 x Intel compliant SDVO port (serial DVO). Resolutions up to 1280x1024 @ 85 Hz. Supports external DVI, TV and LVDS transmitters • Video Decode Acceleration: MPEG2 MPEG4 H.264 WMV9/VC1
Peripheral Interfaces	• 4x Serial ATA® • 2x x1 PCI Express Lanes (revision 1.1 (2.5Gbps) compliant) • 6x USB 2.0 (EHCI) • LPC Bus • PCI Bus Rev. 2.3 • 1x EIDE (UDMA-66/100) optional • I²C Bus, Fast Mode (400 kHz) multimaster • SM Bus
Onboard Storage	Optionally equipped with a Solid State Drive (SSD) up to 32 GByte in capacity
BIOS	AMI Aptio® UEFI 2.x firmware, 4MByte serial SPI with congatec Embedded BIOS features
Power Management	ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 11 of this user's guide to determine what options are available on your particular module.

2.2 Supported Operating Systems

The conga-CA6 supports the following operating systems.

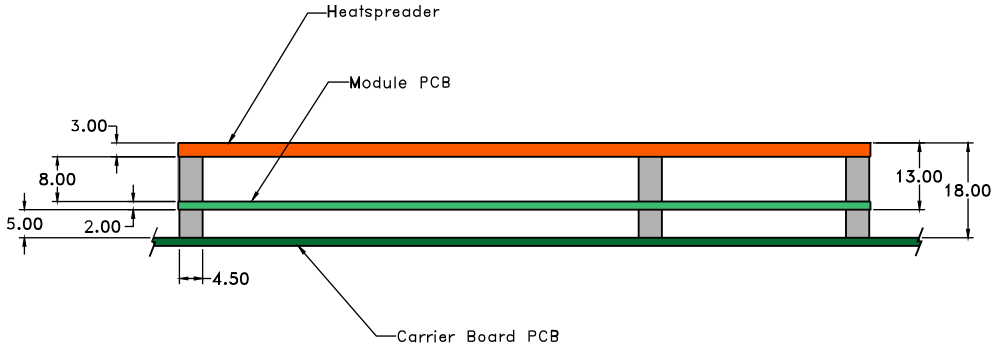
- Microsoft® Windows® 7
- Microsoft® Windows® Embedded Standard 7
- Microsoft® Windows® XP
- Microsoft® Windows® XP Embedded
- Microsoft® Windows® Embedded Compact 7
- Microsoft® Windows® CE 6.0
- Linux
- QNX

Note

DOS is not officially supported by the Intel® Queensbay platform (E6x0 series processors and EG20T Platform Controller Hub (PCH)). As a result, some legacy DOS based applications may not function properly when used in conjunction with the conga-CA6. This limitation is because the EG20T PCH architecture is not designed for legacy applications.

2.3 Mechanical Dimensions

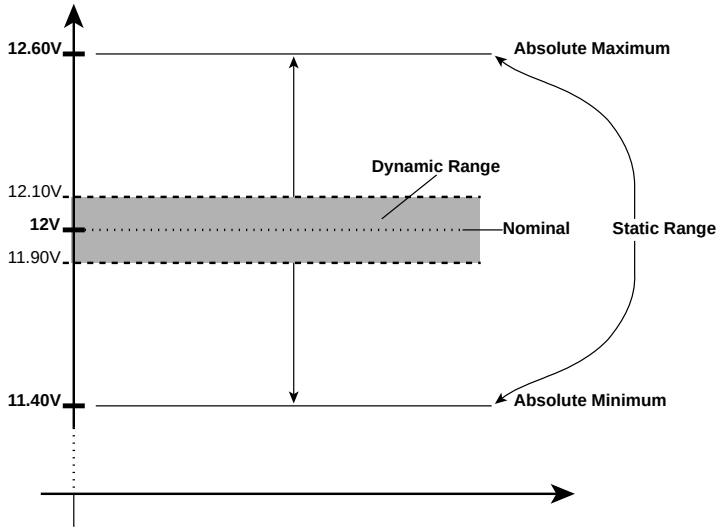
- 95.0 mm x 95.0 mm @ (3.75” x 3.75”)
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm.



2.4 Supply Voltage Standard Power

- 12V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 2 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	16.5	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used includes a conga-CA6 module, conga-CEVAL and conga-Cdebug carrier boards, CRT monitor, SATA drive, and USB keyboard. The conga-Cdebug is modified so that the 12V input is only routed to the module and all other circuity on the carrier itself is powered by the 5V input. The SATA drive was powered externally by an ATX power supply so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. All recorded values were averaged over a 30 second time period. Cooling of the module was done by the module specific heatspreader and a fan cooled heatsink to measure the power consumption under normal thermal conditions.

The conga-Cdebug originally does not provide 5V standby power. Therefore, an extra 5V_SB connection without any external loads was made. Using this setup, the power consumption of the module in S3 (Standby) mode was measured directly.

Each module was measured while running 32 bit Windows 7 Professional and Power Plan set to “Power Saver”. This setting ensures that Core™ processors run in LFM (lowest frequency mode) with minimal core voltage during desktop idle.

To measure the worst case power consumption the cooling solution was removed and the CPU core temperature was allowed to run up to between 95° and 100°C while running 100% workload with the Power Plan set to “Balanced”. The peak current value was then recorded. This value should be taken into consideration when designing the system’s power supply to ensure that the power supply is sufficient during worst case scenarios.

Power consumption values were recorded during the following stages:

Windows 7 (32 bit)

- Desktop Idle (power plan = Power Saver)
- 100% CPU workload (see note below, power plan = Power Saver)
- 100% CPU workload at approximately 100°C peak power consumption (power plan = Balanced)
- Suspend to RAM. Supply power for S3 mode is 5V.

Note

A software tool was used to stress the CPU to Max Frequency.

2.5.1 Intel® Atom™ E680 1.6 GHz 512kB L2 cache

With 1GB onboard memory

conga-CA6/E680-1G Art. No. 061203	Intel® Atom™ E680/E680T 1.6 GHz 512kB L2 cache 45nm Layout Rev. QTOPLA1 /BIOS Rev. QTOPR002		
Memory Size	1GB onboard		
Operating System	Windows 7 (32 bit)		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	0.67 A/8.0 W	0.83 A/10.0 W	0.20 A/1.0 W

2.5.2 Intel® Atom™ E680T 1.6 GHz 512kB L2 cache

With 1GB onboard memory

conga-CA6/E680T-1G Art. No. 061213	Intel® Atom™ E680/E680T 1.6 GHz 512kB L2 cache 45nm Layout Rev. QTOPLA1 /BIOS Rev. QTOPR002		
Memory Size	1GB onboard		
Operating System	Windows 7 (32 bit)		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	0.67 A/8.0 W	0.83 A/10.0 W	0.20 A/1.0 W

2.5.3 Intel® Atom™ E640 1.0 GHz 512kB L2 cache

With 1GB onboard memory

conga-CA6/E640-1G Art. No. 061201	Intel® Atom™ E640/E640T 1.0 GHz 512kB L2 cache 45nm Layout Rev. QTOPLA2 /BIOS Rev. QTOPR002		
Memory Size	1GB onboard		
Operating System	Windows 7 (32 bit)		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	0.63 A/7.5 W	0.74 A/8.9 W	0.22 A/1.1 W

2.5.4 Intel® Atom™ E640T 1.0 GHz 512kB L2 cache

With 1GB onboard memory

conga-CA6/E640T-1G Art. No. 061211	Intel® Atom™ E640/E640T 1.0 GHz 512kB L2 cache 45nm Layout Rev. QTOPLA2 /BIOS Rev. QTOPR002		
Memory Size	1GB onboard		
Operating System	Windows 7 (32 bit)		
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.63 A/7.5 W**	**0.74 A/8.9 W**	**0.22 A/1.1 W**

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

2.6 Supply Voltage Battery Power

- 2.5V-3.6V DC
- Typical 3V DC

2.6.1 CMOS Battery Power Consumption

RTC @ 20°C	Voltage	Current
Integrated in the Intel® Platform Controller Hub EG20T	3V DC	1.71 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

Note

There is a limitation with the Intel® Platform Controller Hub EG20T. The RTC leakage current is extremely high. This means the RTC battery of

a system featuring this chipset depletes after as little as 8 months.

congatec solves this RTC current leakage problem by using the onboard board controller found on the conga-CA6. When the conga-CA6 is powered off, the EG20T RTC is disconnected and the onboard board controller's RTC is used. When the conga-CA6 is restarted, the BIOS overwrites the EG20T system clock with the correct one provided by the congatec board controller.

2.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

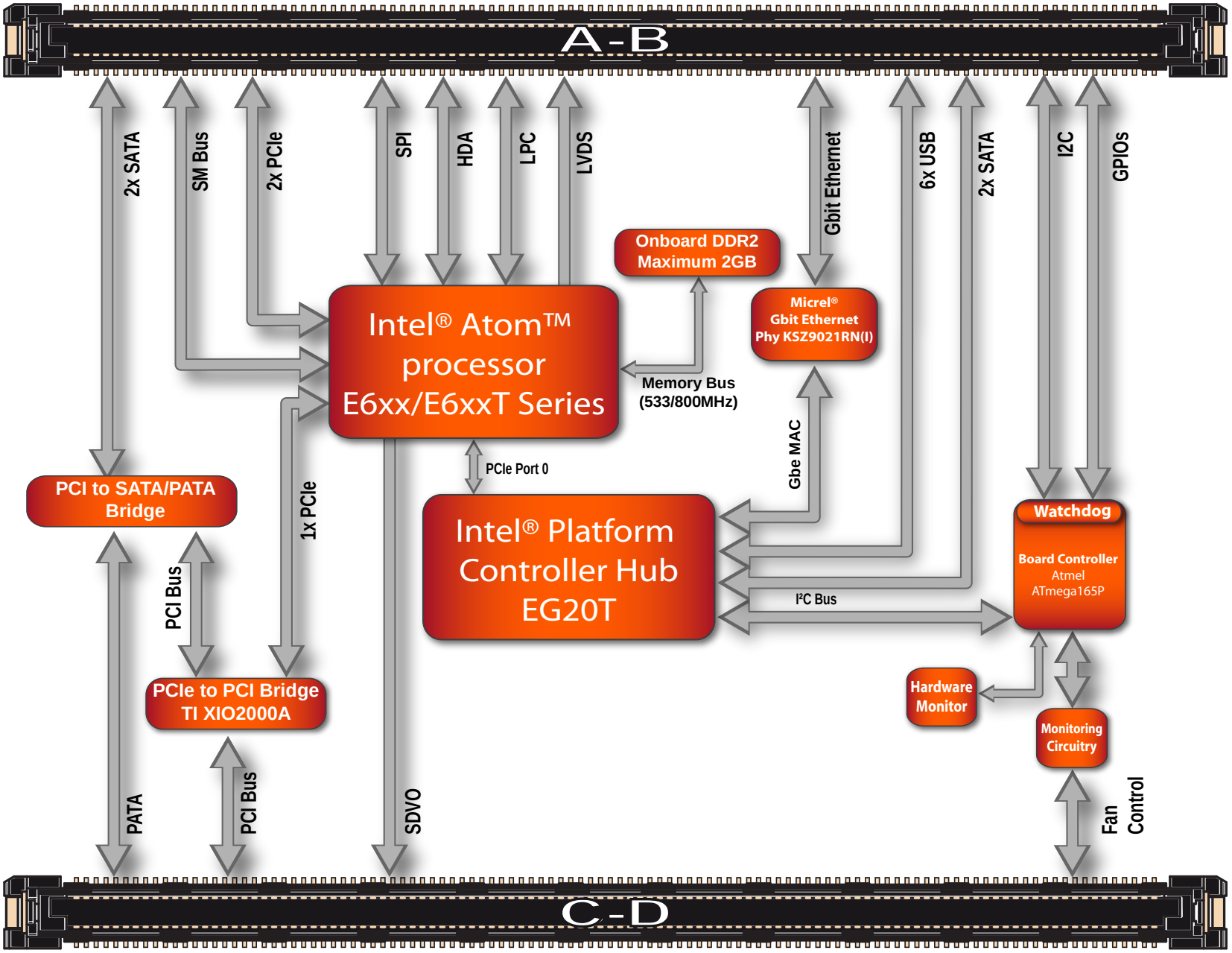
Caution

The above operating temperatures must be strictly adhered to at all times. The congatec heatspreader is only suitable for use within commercial temperature ranges (0° to 60°C). It is not designed to be used within industrial temperature ranges (-40° to 85°C). When using a heatspreader with conga-CA6 commercial grade variants, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution when used in a commercial temperature range.

If it is not possible to use the appropriate congatec module heatspreader for conga-CA6 commercial grade variants or an industrial grade variant of conga-CA6 is being used within industrial temperature ranges, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

3 Block Diagram



4 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module and its aluminum plate is 3mm thick.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

Caution

congatec COM Express™ heaspreaders have been specifically designed for use within commercial temperature ranges (0° to 60°C) only. congatec AG does not recommend using the conga-CA6 heatspreaders in industrial temperature ranges (-40° to 85°C). The user does so at their own risk.

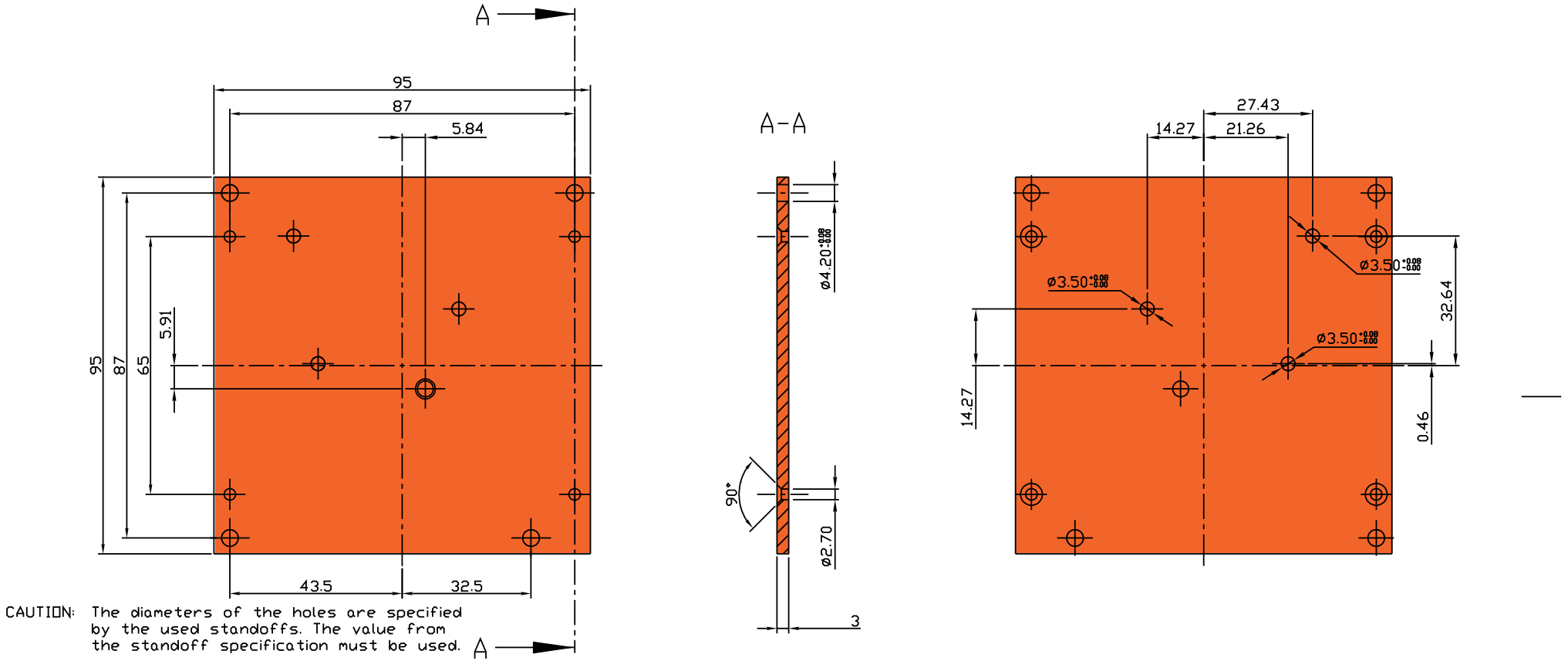
It is the responsibility of the end user to design an optimized thermal solution that meets the needs of their application within the industrial environmental conditions it is required to operate in. Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis.

Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

Only heatspreaders that feature micro pins that secure the thermal stacks should be used for applications that require the heatspreader to be mounted vertically. It cannot be guaranteed that the thermal stacks will not move if a heatspreader that does not have the micro pin feature is used in vertically mounted applications.

Additionally, the gap pad material used on all heatspreaders contains silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification

4.1 Heatspreader Dimensions

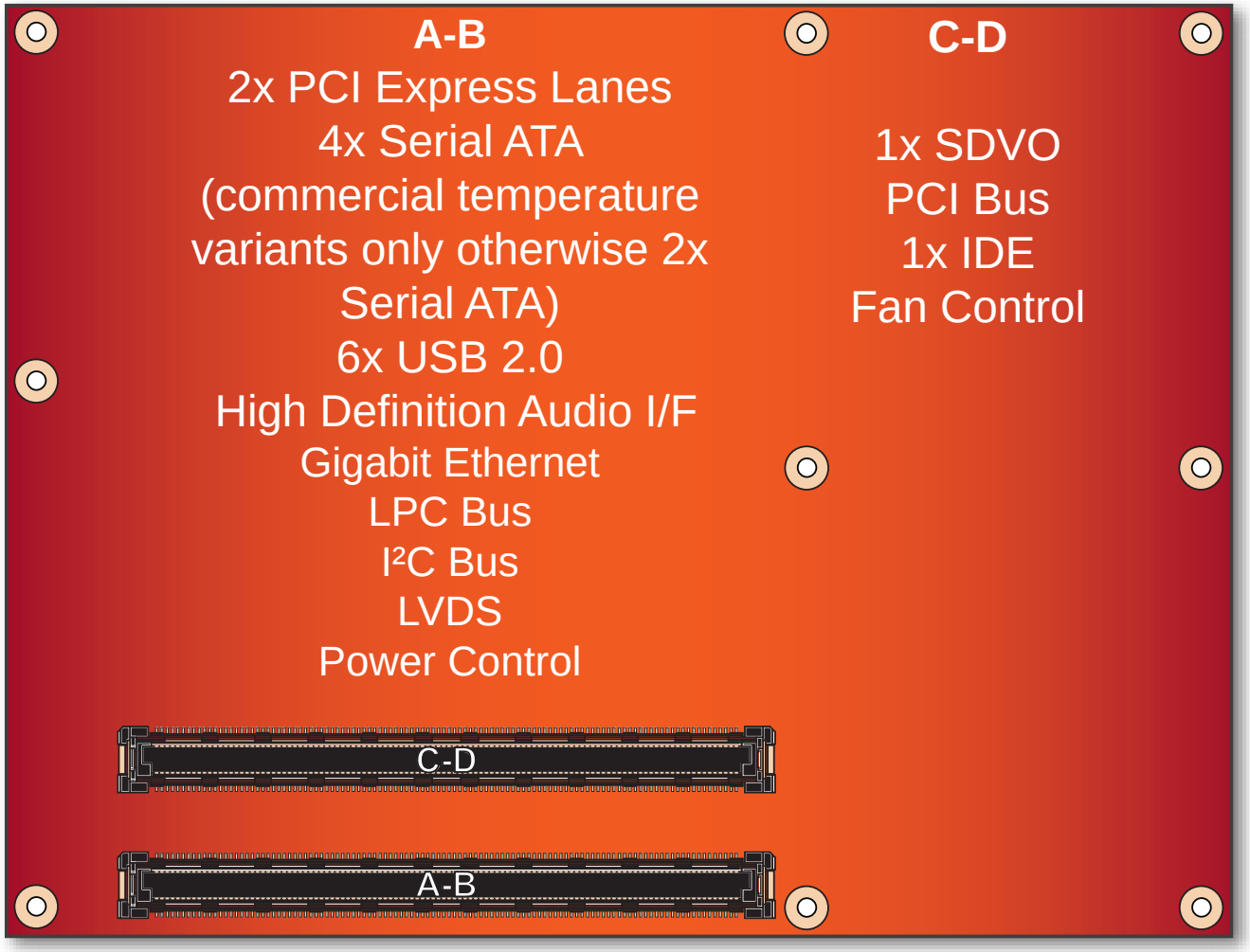


Note

All measurements are in millimeters. Torque specification for heatspreader screws is 0.5 Nm.

5 Connector Subsystems Rows A, B, C, D

The conga-CA6 is connected to the carrier board via two 220-pin connectors (COM Express Type 2 pinout) for a total of 440 pins connectivity. These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.



top view

In this view the connectors are seen “through” the module.

5.1 Primary Connector Rows A and B

The following subsystems can be found on the primary connector rows A and B.

5.1.1 Serial ATA™ (SATA)

Two Serial ATA connections (Ports 0, 1) are provided via the Intel EG20T Platform Controller Hub (PCH) . Additional two Serial ATA connections (Ports 2, 3) are provided by VIA VT6421 PCI SATA to PATA bridge. These ports are however only available on the commercial temperature range variants of the conga-CA6.

The SATA connections (Ports 0, 1, 2, 3) support SATA 1.5-Gbps Gerneration 1 and 3-Gbps Generation 2 speeds. Compliant with Serial ATA specification 2.6 and Advanced Host Controller Interface (AHCI) specification revision 1.1.

Note

The conga-QA6 SATA interface supports AHCI operating mode only on Ports 0, 1 and Legacy operating mode only on Ports 2, 3. SATA Port 1 is not available if the conga-CA6 is equipped with the optional onboard SSD feature.

5.1.2 USB 2.0

The conga-CA6 offers 6 USB host ports provided by the Intel EG20T PCH. These ports comply with USB standard 1.1 and 2.0 and are routed to connector rows A and B. Each port is capable of supporting USB 1.1 and 2.0 compliant devices.

5.1.3 High Definition Audio (HDA) Interface

The conga-CA6 provides an interface that supports the connection of HDA audio codecs.

5.1.4 Gigabit Ethernet

The conga-CA6 is equipped with a Gigabit Ethernet Media Access Controller (GbE MAC) provided by the Intel EG20T PCH that is connected to a Micrel KSZ9021RN(I) Phy via the Reduced Gigabit Media Independent Interface (RGMII). This controller is implemented through the use of a x1 PCI Express link.

The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

Note

It is recommended that the center-taps of the Magnetics are not connected to each other and not connected to the CTREF pin.

5.1.5 LPC Bus

conga-CA6 offers the LPC (Low Pin Count) bus through the use of the Intel E6x0/E6x0T CPU. There are many devices available for this bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific baseboard using this bus.

5.1.6 I²C Bus

The I²C bus is implemented through the use of STMicroelectronics STM32F100R8 microcontroller. It provides a multi-master I²C Bus that has maximum I²C bandwidth.

5.1.7 PCI Express™

The conga-CA6 offers 2x PCI Express™ Gen 2 lanes. These lanes (0, 1) are provided by the Intel E6x0/E6x0T and can be configured to support PCI Express edge cards or ExpressCards. The PCI Express™ interface offers support for full 5 Gb/s bandwidth in each direction per lane.

Note

Some PCI Express devices may have a problem if IRQ 6 or IRQ 12 is assigned to the device. In this case it is necessary to manually assign an IRQ for the device via the PIRQ Routing Submenu found in the BIOS setup program. For more information about this setup node see section 10.5.5 “PIRQ Routing Submenu”.

5.1.8 ExpressCard™

The conga-CA6 supports the implementation of ExpressCards, which requires the dedication of one USB 2.0 port and one x1 PCI Express link for each ExpressCard used.

5.1.9 Graphics Output (VGA/CRT)

The conga-CA6 does not provide a VGA/CRT output.

5.1.10 LCD

The conga-CA6 offers a single channel 80 MHz LVDS interface. This interface is provided by Intel E6x0/E6x0T. It supports the connection of 1x18 or 1x24 bit data mapping up to a resolution of 1280x768@60Hz.

5.1.11 TV-Out

Integrated TV-Out support is not supported on the conga-CA6

5.1.12 Power Control

PWR_OK

Power OK from main power supply. A high value indicates that the power is good. Using this input is optional. Through the use of an internal monitor on the +12V ± 5% input voltage, and/or the internal power supplies, the conga-CA6 module is capable of generating its own power-good signal. According to the COM Express™ Specification PWR_OK is a 3.3V signal and should be driven by open-collector/drain type output.

The conga-CA6 provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-CA6's pins SUS_S3#/PS_ON#, 5V_SB#, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. To accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

12 volt input power is the sole operational power source for the conga-CA6. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-CA6 application:

- It has also been noticed that on some occasions problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any voltage dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

5.1.13 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

5.2 Secondary Connector Rows C and D

The following subsystems can be found on the secondary connector rows C and D.

5.2.1 PCI Express Graphics (PEG)

The PCI Express graphics interface is not supported by the conga-CA6.

5.2.2 SDVO

The conga-CA6 provides one SDVO port via Display Pipe B of the Intel Atom processor E6x0/E6x0T series. The SDVO port can support a variety of display types (VGA, LVDS, DVI, TV-Out, etc.) by using an external SDVO device. This single channel 160MHz SDVO interface supports resolutions up to 1920x1080@60Hz and 1280x1024@85Hz. For more information see the table below.

Table 2 Display Resolutions

Resolution	Refresh	Pixel Clock Freq	SDVO Support	LVDS Support	
640x480	50 Hz	19.75 MHz	Y	Y	
640x480	60 Hz	23.75 MHz	Y	Y	
848x480	50 Hz	26 MHz	Y	Y	
848x480RB	60 Hz	29.75 MHz	Y	Y	
640x480	75 Hz	30.75 MHz	Y	Y	
800x600	50 Hz	30.75 MHz	Y	Y	
848x480	60 Hz	31.5 MHz	Y	Y	
640x480	85 Hz	35 MHz	Y	Y	
800x600RB	60 Hz	35.5 MHz	Y	Y	
800x600	60 Hz	38.25 MHz	Y	Y	
848x480	75 Hz	41 MHz	Y	Y	
848x480	85 Hz	46.75 MHz	Y	Y	
800x600	75 Hz	49 MHz	Y	Y	
1024x768	50 Hz	52 MHz	Y	Y	
1024x768RB	60 Hz	56 MHz	Y	Y	
800x600	85 Hz	56.75 MHz	Y	Y	
1024x768	60 Hz	63.5 MHz	Y	Y	
1280x768	50 Hz	65.25 MHz	Y	Y	
1280x768RB	60 Hz	68.25 MHz	Y	Y	
1280x768	60 Hz	79.5 MHz	Y	Y	Max LVDS interface support
1400x1050	60 Hz	121.75 MHz	Y		
1280x960	75 Hz	130 MHz	Y		

Resolution	Refresh	Pixel Clock Freq	SDVO Support	LVDS Support
1600x1200RB	60 Hz	130.25 MHz	Y	
1600x1200	50 Hz	131.5 MHz	Y	
1920x1080RB	60 Hz	138.5 MHz	Y	
1280x1024	75 Hz	138.75 MHz	Y	
1920x1080	50 Hz	141.5 MHz	Y	
1280x960	85 Hz	148.25 MHz	Y	
1400x1050	75 Hz	156 MHz	Y	
1280x1024	85 Hz	159.5 MHz	Y	Max SDVO interface support

5.2.3 HDMI

The conga-CA6 does not support native HDMI.

5.2.4 DisplayPort (DP)

The conga-CA6 does not support native DisplayPort.

5.2.5 PCI Bus

The PCI bus is implemented using the Intel certified Pericom PI7C9X113SL PCIe to PCI bridge and is connected via one of the PCI Express lanes offered by the Intel Atom processor E6x0/E6x0T series. The PCI bus complies with PCI specification Rev. 2.3 and provides a 32bit parallel PCI bus that is capable of operating at 33MHz.

Note

The PCI interface is specified to be +5V tolerant, with +3.3V signaling.

5.2.6 IDE (PATA)

The conga-CA6 supports an IDE channel that is capable of UDMA-33/66/100 operation. This channel is implemented by converting PCI Bus into an IDE channel using VIA VT6421L single chip solution for PCI to parallel ATA translation. The IDE interface supports the connection of only **one device** at any given moment and this device operates in **Master mode** only.

Note

The IDE interface is only available on commercial temperatures variants of conga-CA6.

6 Additional Features

6.1 Watchdog

The conga-CA6 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog. This means the conga-CA6 does not support external hardware triggering. For more information about the Watchdog feature see the BIOS setup description section 10.5.2 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

6.2 Onboard Microcontroller

The conga-CA6 is equipped with an STMicroelectronics STM32F100R8 microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

6.3 Embedded BIOS

The conga-CA6 is equipped with congatec Embedded BIOS and has the following features:

- ACPI Power Management
- ACPI Battery Support
- Supports Customer Specific CMOS Defaults
- Multistage Watchdog
- User Data Storage
- Manufacturing Data and Board Information
- OEM Splash Screen
- Flat Panel Auto Detection and Backlight Control
- BIOS Setup Data Backup
- Fast Mode I²C Bus

6.4 Suspend to Ram

The Suspend to RAM feature is supported on the conga-CA6.

6.5 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-CA6 BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM^{3}C User's Guide

7 conga Tech Notes

The conga-CA6 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

7.1 Intel® Processor Features

7.1.1 Thermal Monitor and Catastrophic Thermal Protection

Intel® Atom™ processor E6x0/E6x0T series have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature, that the Intel® Thermal Monitor uses to activate the TCC, cannot be configured by the user nor is it software visible.

The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel® Speedstep transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.

Note

The maximum operating temperature for Intel® Atom™ processor E6x0/E6x0T series is 100°C.

Two modes are supported by the Thermal Monitor to activate the TCC. They are called Automatic and On-Demand. No additional hardware, software, or handling routines are necessary when using Automatic Mode.

Note

To ensure that the TCC is active for only short periods of time thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Atom™ processor E6x0/E6x0T series respective datasheet can provide more information about this subject.

7.1.2 Processor Performance Control

Intel® Atom™ processor E6x0/E6x0T series run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states to efficiently operate the processor when it is not fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that your power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

7.1.3 Intel® Virtualization Technology

Virtualization solutions enhanced by Intel® VT will allow Atom™ processor E6x0/E6x0T series to run multiple operating systems and applications in independent partitions. When using virtualization capabilities, one computer system can function as multiple “virtual” systems. With processor and I/O enhancements to Intel®’s various platforms, Intel® Virtualization Technology can improve the performance and robustness of today’s software-only virtual machine solutions.

Intel® VT is a multi-generational series of extensions to Intel® processor and platform architecture that provides a new hardware foundation for virtualization, establishing a common infrastructure for all classes of Intel® based systems. The broad availability of Intel® VT makes it possible to create entirely new applications for virtualization in servers, clients as well as embedded systems thus providing new ways to improve system reliability, manageability, security, and real-time quality of service.

The success of any new hardware architecture is highly dependent on the system software that puts its new features to use. In the case of virtualization technology, that support comes from the virtual machine monitor (VMM), a layer of software that controls the underlying physical platform resources sharing them between multiple “guest” operating systems. Intel® VT is already incorporated into most commercial and open-source VMMs including those from VMware, Microsoft, XenSource, Parallels, Virtual Iron, Jaluna and TenAsys.

You can find more information about Intel Virtualization Technology at: http://developer.intel.com/technology/virtualization/index.htm

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions should be directed to the VMM software vendor and not congatec technical support.

7.2 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-CA6 ACPI thermal solution offers three different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled according to the formula below.

$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

- *ΔP is the performance delta*
- *T_t is the target temperature = critical trip point*

- *The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants. These constants are set to fixed values for the conga-CA6:*
- *TC1= 1*
- *TC2= 5*
- *TSP= 5 seconds*

See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.3 ACPI Suspend Modes and Resume Events

conga-CA6 supports the S3 (STR= Suspend to RAM) power state. For more information about S3 wake events see section 10.5.7 “ACPI Configuration Submenu”. S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by some operating systems (S4_OS= Hibernate). Check with the operating system vendor to determine if S4 (Suspend to Disk) is supported.

This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3 and S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support. Feature must be enabled in BIOS setup.
PCI Express WAKE#	Wakes unconditionally from S3.
Watchdog Power Button Event	Wakes unconditionally from S3 and S5.

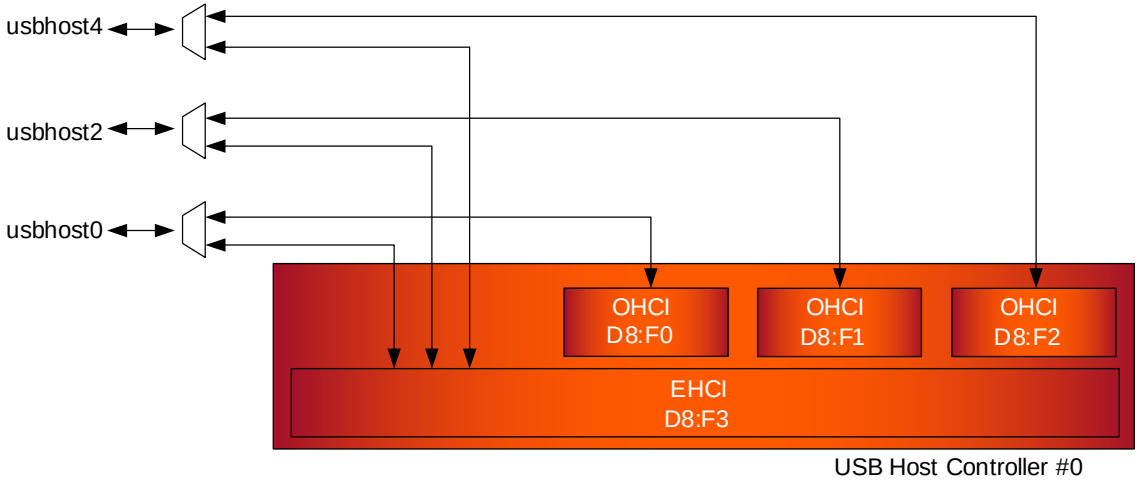
Note

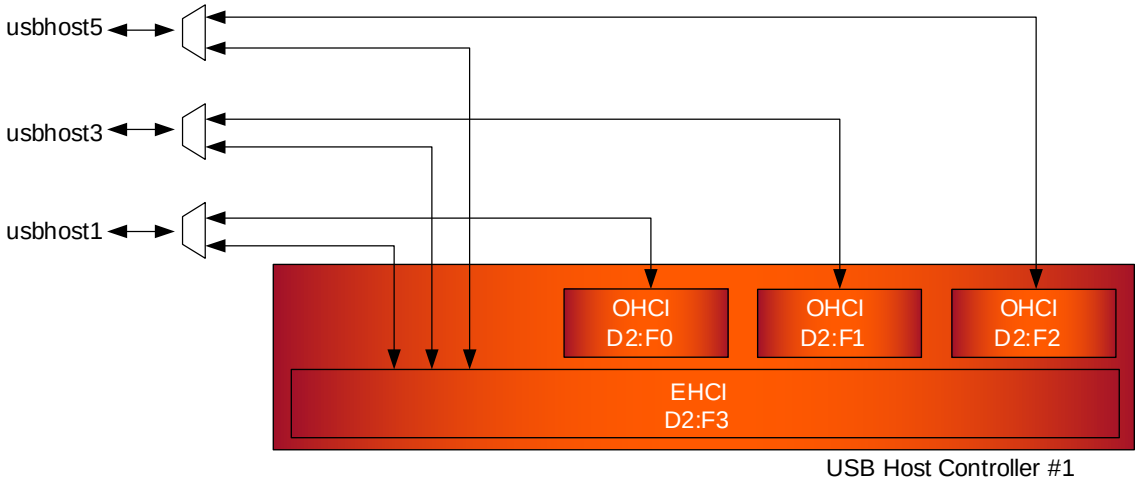
The above list has been verified with a Windows XP SP3 enabled with ACPI

7.4 USB Port Connections

The 6 USB ports are shared between 2 EHCI host controllers. Ports 0-5 are capable of supporting USB 1.1 and 2.0 compliant devices. Port 1 can be configured as either a USB Device (Client) port or Host port.

Routing Diagram





7.4.1 USB Client Controller

The Intel EG20T Platform Controller Hub located on the conga-CA6 features a Universal Serial Bus 2.0 device/client controller. This USB device/client controller allows the conga-CA6 to connect to other computer systems that utilize a USB Host interface. Once connected, the conga-CA6 can perform tasks supported by common USB devices. This includes, but not limited to, such functionality as data transfer and network access.

This USB device/client implementation is designed to achieve maximum flexibility while maintaining hardware simplicity. Most of the behavior above the DMA and USB protocol layer is the responsibility of software. This includes Transaction level formatting, handling USB Descriptors and the implementation of defined Device Classes.

Detailed information about the USB Client Controller is beyond the scope of this document. For more information refer to the Intel® Platform Controller Hub EG20T datasheet.

Note

The EG20T Platform Controller Hub USB device/client port is routed to USB Port 1 on the conga-CA6.

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type II connectors used for congatec AG modules. The pinout of the modules complies with COM Express Type 2.0 Rev. 2.0.

Table 2 describes the terminology used in this section for the signal description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.

Note

The signal description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip’s datasheet.

Table 3 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0
PEG	PCI Express Graphics
SATA	In compliance with Serial ATA specification, Revision 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

8.1 A-B Connector Signal Descriptions

Table 4 Intel® High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC/HDA_RST#	A30	**Intel® High Definition Audio Reset:** This signal is the master hardware reset to external codec(s).	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SYNC	A29	**Intel® High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_BITCLK	A32	**Intel® High Definition Audio Bit Clock Output:** This signal is a 24.000MHz serial data clock generated by the Intel® High Definition Audio controller.	O 3.3VSB		AC'97 codecs are not supported.
AC/HDA_SDOUT	A33	**Intel® High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3VSB		AC'97 codecs are not supported. AC/HDA_SDOUT is a bootstrap signal (see note below)
AC/HDA_SDIN[2:0]	B28-B30	**Intel® High Definition Audio Serial Data In [0]:** These signals are serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	I 3.3VSB		AC'97 codecs are not supported.

Table 5 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 / 100 / 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	O 2.5VSB	PU 4k99 2,5VSB	GBE0_ACT is a bootstrap signal (see note below)
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB	PD 1k	GBE0_LINK# is a bootstrap signal (see note below)
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 2.5VSB	PU 4k99 2,5VSB	GBE0_ LINK100# is a bootstrap signal (see note below)
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB	PD 1k	GBE0_ LINK1000# is a bootstrap signal (see note below)
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.			Not connected

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module.

For more information refer to section 8.5 of this user's guide.

Table 6 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 2.6
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 2.6
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0
ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V	PU 10k 3.3V	

Table 7 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Not supported
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express Gen2 compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 8 ExpressCard Support Pins Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request.	I 3.3V	PU 10k 3.3V	
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3V	PU 10k 3.3V	Connect to CB_RESET#

Table 9 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V		Not supported
LPC_SERIRQ	A50	LPC serial interrupt	I/O OD 3.3V	PU 10k 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		

Table 10 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37	USB Port 6, data + or D+	I/O		Not supported
USB6-	A36	USB Port 6, data - or D-	I/O		Not supported
USB7+	B37	USB Port 7, data + or D+	I/O		Not supported
USB7-	B36	USB Port 7, data - or D-	I/O		Not supported
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB		Not supported

Table 11 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not supported
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not supported
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not supported
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		Not supported
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		Not supported
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O OD 5V		Not supported
VGA_I2C_DAT	B96	DDC data line.	I/O OD 5V		Not supported

Table 12 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		Not supported
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		Not supported
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10k	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10k	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

Table 13 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3V	PU 10k 3.3V	Carrier shall pull to SPI_POWER when external SPI provided but not used.
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3V		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3V	PU 1k 3.3V	
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3V		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	+ 3.3V		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3V		Not connected
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I 3.3V	PU 10K 3.3V	Carrier shall pull to GND or leave no-connect

Table 14 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O 3.3V	PU 2K2 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O 3.3V	PU 2K2 3.3VSB	
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
KBD_RST#	A86	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.	I	PU 10K 3.3V	
KBD_A20GATE	A87	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled high on the module.	I	PU 10K 3.3VSB	

Table 15 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V		
GPO[1]	B54	General purpose output pins.	O 3.3V		
GPO[2]	B57	General purpose output pins.	O 3.3V		
GPO[3]	B63	General purpose output pins.	O 3.3V		
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 4k75 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 4k75 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 4k75 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 4k75 3.3V	

Table 16 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on rising edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low.	I 3.3V	PU 10k 3.3V	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V	PD 20k	
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V		Set by resistor divider to accept 3.3V.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as “PS_ON”) may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		Not supported
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB	PU 100k 5VSB	
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10k 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 10k 3.3V	
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10k 3.3V	
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	I/O 3.3VSB	PU 10k 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	I/O OD 3.3VSB	PU 10k 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	I 3.3VSB	PU 10k 3.3VSB	

Table 17 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A66, A80, A90, A96, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

8.2 A-B Connector Pinout

Table 18 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4- (*)	B56	PCIE_RX4- (*)
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+ (*)	B58	PCIE_RX3+ (*)
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3- (*)	B59	PCIE_RX3- (*)
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+ (*)	B61	PCIE_RX2+ (*)
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2- (*)	B62	PCIE_RX2- (*)
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+ (*)
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0- (*)
A18	SUS_S4# (*)	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+ (*)
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1- (*)
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+ (*)
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2- (*)
A22	SATA2_TX+ (**)	B22	SATA3_TX+ (**)	A77	LVDS_VDD_EN	B77	LVDS_B3+ (*)
A23	SATA2_TX- (**)	B23	SATA3_TX- (**)	A78	LVDS_A3+	B78	LVDS_B3- (*)
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+ (**)	B25	SATA3_RX+ (**)	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX- (**)	B26	SATA3_RX- (**)	A81	LVDS_A_CK+	B81	LVDS_B_CK+ (*)
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK- (*)
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2 (*)	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	KBD_RST#	B86	VCC_5V_SBY
A32	AC/HDA_BITCLK	B32	SPKR	A87	KBD_A20GATE (*)	B87	VCC_5V_SBY
A33	AC/HDA_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0# (*)	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED (*)
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6- (*)	B36	USB7- (*)	A91	SPI_POWER	B91	VGA_GRN (*)
A37	USB6+ (*)	B37	USB7+ (*)	A92	SPI_MISO	B92	VGA_BLU (*)

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A38	USB_6_7_OC# (*)	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC (*)
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC (*)
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK (*)
A41	GND (FIXED)	B41	GND (FIXED)	A96	GND	B96	VGA_I2C_DAT (*)
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	RSVD	B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	RSVD	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	RSVD	B101	RSVD
A47	VCC_RTC	B47	EXCD1_PERST# (*)	A102	RSVD	B102	RSVD
A48	EXCD0_PERST#	B48	EXCD1_CPPE# (*)	A103	RSVD	B103	RSVD
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+ (*)	B52	PCIE_RX5+ (*)	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5- (*)	B53	PCIE_RX5- (*)	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+ (*)	B55	PCIE_RX4+ (*)	A110	GND (FIXED)	B110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-CA6.

The signals marked with an asterisk symbol (**) are not supported on conga-CA6 industrial temperature range variants.

8.3 C-D Connector Signal Descriptions

Table 19 PCI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCI_AD[0, 2, 4, 6, 8, 10, 12] PCI_AD[1, 3, 5, 7] PCI_AD[9, 11, 13, 15] PCI_AD14 PCI_AD[16, 18, 20, 22] PCI_AD[17, 19] PCI_AD[21, 23] PCI_AD[24, 26, 28, 30] PCI_AD[25, 27, 29, 31]	C24-C30 D22-D25 D27-D30 C32 D37-D40 C39-C40 C42-C43 D42-D45 C45-C48	PCI bus multiplexed address and data lines	I/O 3.3V		
PCI_C/BE0# PCI_C/BE1# PCI_C/BE2# PCI_C/BE3#	D26 C33 C38 C44	PCI bus byte enable lines, active low	I/O 3.3V		
PCI_DEVSEL#	C36	PCI bus Device Select, active low.	I/O 3.3V	PU 4K75 3.3V	
PCI_FRAME#	D36	PCI bus Frame control line, active low.	I/O 3.3V	PU 4K75 3.3V	
PCI_IRDY#	C37	PCI bus Initiator Ready control line, active low.	I/O 3.3V	PU 4K75 3.3V	
PCI_TRDY#	D35	PCI bus Target Ready control line, active low.	I/O 3.3V	PU 4K75 3.3V	
PCI_STOP#	D34	PCI bus STOP control line, active low, driven by cycle initiator.	I/O 3.3V	PU 4K75 3.3V	
PCI_PAR	D32	PCI bus parity	I/O 3.3V		
PCI_PERR#	C34	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.	I/O 3.3V	PU 4K75 3.3V	
PCI_REQ0# PCI_REQ1# PCI_REQ2# PCI_REQ3#	C22 C19 C17 D20	PCI bus master request input lines, active low.	I 3.3V	PU 4K75 3.3V	
PCI_GNT0# PCI_GNT1# PCI_GNT2# PCI_GNT3#	C20 C18 C16 D19	PCI bus master grant output lines, active low.	O 3.3V	PU 4k75 3.3V	
PCI_RESET#	C23	PCI Reset output, active low.	O 3.3V		
PCI_LOCK#	C35	PCI Lock control line, active low.	I/O 3.3V	PU 4K75 3.3V	
PCI_SERR#	D33	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition.	I/O 3.3V	PU 4K75 3.3V	
PCI_PME#	C15	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.	I/O OD 3.3VSB	PU 10k 3.3VSB	

Signal	Pin #	Description	I/O	PU/PD	Comment
PCI_CLKRUN#	D48	Bidirectional pin used to support PCI clock run protocol for mobile systems.	I/O 3.3V	PU 10k 3.3V	
PCI_IRQA# PCI_IRQB# PCI_IRQC# PCI_IRQD#	C49 C50 D46 D47	PCI interrupt request lines.	I 3.3V	PU 4K75 3.3V	
PCI_CLK	D50	PCI 33MHz clock output.	O 3.3V		
PCI_M66EN	D49	Module input signal indicates whether an off-module PCI device is capable of 66MHz operation. Pulled to GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66MHz operation. If the module is not capable of supporting 66MHz PCI operation, this input may be a no-connect on the module. If the module is capable of supporting 66MHz PCI operation, and if this input is held low by the Carrier Board, the module PCI interface shall operate at 33MHz.	I 3.3V		Not connected

Note

The PCI interface is specified to be +5V tolerant, with +3.3V signaling.

Table 20 IDE Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
IDE_D0 IDE_D1 IDE_D2 IDE_D3 IDE_D4 IDE_D5 IDE_D6 IDE_D7 IDE_D8 IDE_D9 IDE_D10 IDE_D11 IDE_D12 IDE_D13 IDE_D14 IDE_D15	D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5	Bidirectional data to / from IDE device.	I/O 3.3V		
IDE_A[0.2]	D13-D15	Address lines to IDE device.	O 3.3V		
IDE_IOW#	D9	I/O write line to IDE device. Data latched on trailing (rising) edge.	O 3.3V		
IDE_IOR#	C14	I/O read line to IDE device.	O 3.3V		
IDE_REQ	D8	IDE Device DMA Request. It is asserted by the IDE device to request a data transfer.	I 3.3V		
IDE_ACK#	D10	IDE Device DMA Acknowledge.	O 3.3V		
IDE_CS1#	D16	IDE Device Chip Select for 1F0h to 1FFh range.	O 3.3V		
IDE_CS3#	D17	IDE Device Chip Select for 3F0h to 3FFh range.	O 3.3V		
IDE_IORDY	C13	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.	I 3.3V		
IDE_RESET#	D18	Reset output to IDE device, active low.	O 3.3V		
IDE_IRQ	D12	Interrupt request from IDE device.	I 3.3V		
IDE_CBLID#	D77	Input from off-module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 and 133 modes.	I 3.3V		

Note

The IDE interface is specified to be +5V tolerant, with +3.3V signaling.

Table 21 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs. Some of these lines are multiplexed with SDVO lines. *Note: Can also be used as PCI Express Receive Input differential pairs 16 through 31 known as PCIE_RX[16-31] + and -.*	I PCIE		PCI Express Graphics (PEG) is not supported on the conga-CA6 (see note below).
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+ PEG_TX0- PEG_TX1+ PEG_TX1- PEG_TX2+ PEG_TX2- PEG_TX3+ PEG_TX3- PEG_TX4+ PEG_TX4- PEG_TX5+ PEG_TX5- PEG_TX6+ PEG_TX6- PEG_TX7+ PEG_TX7- PEG_TX8+ PEG_TX8- PEG_TX9+ PEG_TX9- PEG_TX10+ PEG_TX10- PEG_TX11+ PEG_TX11- PEG_TX12+ PEG_TX12- PEG_TX13+ PEG_TX13- PEG_TX14+ PEG_TX14- PEG_TX15+ PEG_TX15-	D52 D53 D55 D56 D58 D59 D61 D62 D65 D66 D68 D69 D71 D72 D74 D75 D78 D79 D81 D82 D85 D86 D88 D89 D91 D92 D94 D95 D98 D99 D101 D102	PCI Express Graphics Transmit Output differential pairs. Some of these lines are multiplexed with SDVO lines. *Note: Can also be used as PCI Express Transmit Output differential pairs 16 through 31 known as PCIE_TX[16-31] + and -.*	O PCIE		Not supported
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I 1.05V		Not supported
PEG_ENABLE#	D97	Strap to enable PCI Express x16 external graphics interface.	I 3.3V		Not supported

Note

The PCI Express Graphics (PEG) signals are multiplexed with HDMI, DisplayPort (DP) and SDVO. The signals for these interfaces are routed to the PEG interface of the COM Express connector. Refer to the SDVO, HDMI and DiplayPort signal description tables in this section for information about the signals routed to the PEG interface of the COM Express connector.

Table 22 SDVO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDVOB_RED+ SDVOB_RED-	D52 D53	Serial Digital Video B red output differential pair. Multiplexed with PEG_TX[0]+ and PEG_TX[0]- pair.	O PCIE		
SDVOB_GRN+ SDVOB_GRN-	D55 D56	Serial Digital Video B green output differential pair. Multiplexed with PEG_TX[1]+ and PEG_TX[1]-.	O PCIE		
SDVOB_BLU+ SDVOB_BLU-	D58 D59	Serial Digital Video B blue output differential pair. Multiplexed with PEG_TX[2]+ and PEG_TX[2]-.	O PCIE		
SDVOB_CK+ SDVOB_CK-	D61 D62	Serial Digital Video B clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]-.	O PCIE		
SDVOB_INT+ SDVOB_INT-	C55 C56	Serial Digital Video B interrupt input differential pair. Multiplexed with PEG_RX[1]+ and PEG_RX[1]-.	I PCIE		
SDVOC_RED+ SDVOC_RED-	D65 D66	Serial Digital Video C red output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]-.	O PCIE		Not supported
SDVOC_GRN+ SDVOC_GRN-	D68 D69	Serial Digital Video C green output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]-.	O PCIE		Not supported
SDVOC_BLU+ SDVOC_BLU-	D71 D72	Serial Digital Video C blue output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]-.	O PCIE		Not supported
SDVOC_CK+ SDVOC_CK-	D74 D75	Serial Digital Video C clock output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]-.	O PCIE		Not supported
SDVOC_INT+ SDVOC_INT-	C68 C69	Serial Digital Video C interrupt input differential pair. Multiplexed with PEG_RX[5]+ and PEG_RX[5]-.	I PCIE		Not supported
SDVO_TVCLKIN+ SDVO_TVCLKIN-	C52 C53	Serial Digital Video TVOUT synchronization clock input differential pair. Multiplexed with PEG_RX[0]+ and PEG_RX[0]-.	I PCIE		
SDVO_FLDSTALL+ SDVO_FLDSTALL-	C58 C59	Serial Digital Video Field Stall input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]-.	I PCIE		
SDVO_I2C_CK (SDVO_CLK)	D73	SDVO I²C clock line to set up SDVO peripherals.	O 3.3V		
SDVO_I2C_DAT (SDVO_DATA)	C73	SDVO I²C data line to set up SDVO peripherals.	I/O OD 2.5V		SDVO_I2C_DAT is a bootstrap signal (see note below)

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 8.5 of this user's guide.

Table 23 HDMI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS_B_CLK + TMDS_B_CLK -	D61 D62	HDMI Port B Clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]- pair.	O PCIE		Not supported
TMDS_B_DATA0+ TMDS_B_DATA0-	D58 D59	HDMI Port B Data0 output differential pair. Multiplexed with PEG_TX[2]+ and PEG_TX[2]-.	O PCIE		Not supported
TMDS_B_DATA1+ TMDS_B_DATA1-	D55 D56	HDMI Port B Data1 output differential pair. Multiplexed with PEG_TX[1]+ and PEG_TX[1]-.	O PCIE		Not supported
TMDS_B_DATA2+ TMDS_B_DATA2-	D52 D53	HDMI Port B Data2 output differential pair. Multiplexed with PEG_TX[0]+ and PEG_TX[0]-.	O PCIE		Not supported
TMDS_B_HPD	C61	HDMI Port B Hot-plug detect. Multiplexed with PEG_RX[3]+.	I PCIE		Not supported
DDPB_CTRLCLK	D73	HDMI port B Control Clock	I/O 3.3V		Not supported
DDPB_CTRLDATA	C73	HDMI port B Control Data	I/O 3.3V		Not supported
TMDS_C_CLK + TMDS_C_CLK -	D74 D75	HDMI Port C Clock output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]- pair.	O PCIE		Not supported
TMDS_C_DATA0+ TMDS_C_DATA0-	D71 D72	HDMI Port C Data0 output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]-.	O PCIE		Not supported
TMDS_C_DATA1+ TMDS_C_DATA1-	D68 D69	HDMI Port C Data1 output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]-.	O PCIE		Not supported
TMDS_C_DATA2+ TMDS_C_DATA2-	D65 D66	HDMI Port C Data2 output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]-.	O PCIE		Not supported
TMDS_C_HPD	C74	HDMI Port C Hot-plug detect. Multiplexed with PEG_RX[7]+.	I PCIE		Not supported
DDPC_CTRLCLK	D63	HDMI port C Control Clock	I/O 3.3V		Not supported
DDPC_CTRLDATA	D64	HDMI port C Control Data	I/O 3.3V		Not supported
TMDS_D_CLK + TMDS_D_CLK -	D88 D89	HDMI Port D Clock output differential pair. Multiplexed with PEG_TX[11]+ and PEG_TX[11]- pair.	O PCIE		Not supported
TMDS_D_DATA0+ TMDS_D_DATA0-	D85 D86	HDMI Port D Data0 output differential pair. Multiplexed with PEG_TX[10]+ and PEG_TX[10]-.	O PCIE		Not supported
TMDS_D_DATA1+ TMDS_D_DATA1-	D81 D82	HDMI Port D Data1 output differential pair. Multiplexed with PEG_TX[9]+ and PEG_TX[9]-.	O PCIE		Not supported
TMDS_D_DATA2+ TMDS_D_DATA2-	D78 D79	HDMI Port D Data2 output differential pair. Multiplexed with PEG_TX[8]+ and PEG_TX[8]-.	O PCIE		Not supported
TMDS_D_HPD	C88	HDMI Port C Hot-plug detect. Multiplexed with PEG_RX[11]+.	I PCIE		Not supported
DDPD_CTRLCLK	C97	HDMI port D Control Clock	I/O 3.3V		Not supported
DDPD_CTRLDATA	D83	HDMI port D Control Data	I/O 3.3V		Not supported

Table 24 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DPB_LANE3+ DPB_LANE3-	D61 D62	DisplayPort B Lane3 output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]- pair.	O PCIE		Not supported
DPB_LANE2+ DPB_LANE2-	D58 D59	DisplayPort B Lane2 output differential pair. Multiplexed with PEG_TX[2]+ and PEG_TX[2]- pair.	O PCIE		Not supported
DPB_LANE1+ DPB_LANE1-	D55 D56	DisplayPort B Lane1 output differential pair. Multiplexed with PEG_TX[1]+ and PEG_TX[1]- pair.	O PCIE		Not supported
DPB_LANE0+ DPB_LANE0-	D52 D53	DisplayPort B Lane0 output differential pair. Multiplexed with PEG_TX[0]+ and PEG_TX[0]- pair.	O PCIE		Not supported
DPB_HPD	C61	DisplayPort B Hot-plug detect. Multiplexed with PEG_RX[3]+.	I PCIE		Not supported
DPB_AUX+ DPB_AUX-	C58 C59	DisplayPort B Aux input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]- pair.	I PCIE		Not supported
DDPB_CTRLDATA	C73	Digital Display port B Control Data	I/O 3.3V		Not supported
DPC_LANE3+ DPC_LANE3-	D74 D75	DisplayPort C Lane3 output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]- pair.	O PCIE		Not supported
DPC_LANE2+ DPC_LANE2-	D71 D72	DisplayPort C Lane2 output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]- pair.	O PCIE		Not supported
DPC_LANE1+ DPC_LANE1-	D68 D69	DisplayPort C Lane1 output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]- pair.	O PCIE		Not supported
DPC_LANE0+ DPC_LANE0-	D65 D66	DisplayPort C Lane0 output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]- pair.	O PCIE		Not supported
DPC_HPD	C74	DisplayPort C Hot-plug detect. Multiplexed with PEG_RX[7]+.	I PCIE		Not supported
DPC_AUX+ DPC_AUX-	C71 C72	DisplayPort C Aux input differential pair. Multiplexed with PEG_RX[6]+ and PEG_RX[6]- pair.	I PCIE		Not supported
DDPC_CTRLDATA	D64	Digital Display port C Control Data	I/O 3.3V		Not supported
DPD_LANE3+ DPD_LANE3-	D88 D89	DisplayPort D Lane3 output differential pair. Multiplexed with PEG_TX[11]+ and PEG_TX[11]- pair.	O PCIE		Not supported
DPD_LANE2+ DPD_LANE2-	D85 D86	DisplayPort D Lane2 output differential pair. Multiplexed with PEG_TX[10]+ and PEG_TX[10]- pair.	O PCIE		Not supported
DPD_LANE1+ DPD_LANE1-	D81 D82	DisplayPort D Lane1 output differential pair. Multiplexed with PEG_TX[9]+ and PEG_TX[9]- pair.	O PCIE		Not supported
DPD_LANE0+ DPD_LANE0-	D78 D79	DisplayPort D Lane0 output differential pair. Multiplexed with PEG_TX[8]+ and PEG_TX[8]- pair.	O PCIE		Not supported
DPD_HPD	C88	DisplayPort D Hot-plug detect. Multiplexed with PEG_RX[11]+.	I PCIE		Not supported
DPD_AUX+ DPD_AUX-	C85 C86	DisplayPort D Aux input differential pair. Multiplexed with PEG_RX[10]+ and PEG_RX[10]- pair.	I PCIE		Not supported
DDPD_CTRLDATA	D83	Digital Display port C Control Data	I/O 3.3V		Not supported

Table 25 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pinout Type 1 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 (no IDE) NC GND NC Pinout Type 4 (no PCI) NC GND GND Pinout Type 5 (no IDE, no PCI) GND NC NC Pinout Type 6 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.	PDS	TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard. The conga-BM67/BS67 is based on the COM Express Type 2 pinout therefore these pins are not connected.
TYPE10#	A97	Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed. TYPE10# NC Pinout R2.0 PD Pinout Type 10 pull down to ground with 4.7k resistor 12V Pinout R1.0 This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7k resistor.	PDS	Not supported

Table 26 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
GND	C1, C11, C21, C31, C41, C51, C60, C70, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D11, D21, D31, D41, D51, D60, D67, D70, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

Table 27 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT	C67	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V	PU 10k 3.3V	
FAN_TACHOIN	C77	Fan tachometer input.	I OD	PU 10k 3.3V	Requires a fan with a two pulse output.
PP_TPM	C83	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V		The conga-CA6 does not support Trusted Platform Module (TPM).

8.4 C-D Connector Pinout

Table 28 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1-	D56	PEG_TX1-
C2	IDE_D7 (**)	D2	IDE_D5 (**)	C57	TYPE1#	D57	TYPE2#
C3	IDE_D6 (**)	D3	IDE_D10 (**)	C58	PEG_RX2+	D58	PEG_TX2+
C4	IDE_D3 (**)	D4	IDE_D11 (**)	C59	PEG_RX2-	D59	PEG_TX2-
C5	IDE_D15 (**)	D5	IDE_D12 (**)	C60	GND (FIXED)	D60	GND (FIXED)
C6	IDE_D8 (**)	D6	IDE_D4 (**)	C61	PEG_RX3+ (*)	D61	PEG_TX3+
C7	IDE_D9 (**)	D7	IDE_D0 (**)	C62	PEG_RX3- (*)	D62	PEG_TX3-
C8	IDE_D2 (**)	D8	IDE_REQ (**)	C63	RSVD	D63	DDPC_CTRLCLK (*)
C9	IDE_D13 (**)	D9	IDE_IOW# (**)	C64	RSVD	D64	DDPC_CTRLDATA (*)
C10	IDE_D1 (**)	D10	IDE_ACK# (**)	C65	PEG_RX4+ (*)	D65	PEG_TX4+ (*)
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4- (*)	D66	PEG_TX4- (*)
C12	IDE_D14 (**)	D12	IDE_IRQ (**)	C67	FAN_PWMOUT	D67	GND
C13	IDE_IORDY (**)	D13	IDE_A0 (**)	C68	PEG_RX5+ (*)	D68	PEG_TX5+ (*)
C14	IDE_IOR# (**)	D14	IDE_A1 (**)	C69	PEG_RX5- (*)	D69	PEG_TX5- (*)
C15	PCI_PME#	D15	IDE_A2 (**)	C70	GND (FIXED)	D70	GND (FIXED)
C16	PCI_GNT2#	D16	IDE_CS1# (**)	C71	PEG_RX6+ (*)	D71	PEG_TX6+ (*)
C17	PCI_REQ2#	D17	IDE_CS3# (**)	C72	PEG_RX6- (*)	D72	PEG_TX6- (*)
C18	PCI_GNT1#	D18	IDE_RESET# (**)	C73	SDVO_DATA	D73	SVDO_CLK
C19	PCI_REQ1#	D19	PCI_GNT3# (*)	C74	PEG_RX7+ (*)	D74	PEG_TX7+ (*)
C20	PCI_GNT0#	D20	PCI_REQ3# (*)	C75	PEG_RX7- (*)	D75	PEG_TX7- (*)
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCI_REQ0#	D22	PCI_AD1	C77	FAN_TACHOIN	D77	IDE_CBLID# (**)
C23	PCI_RESET#	D23	PCI_AD3	C78	PEG_RX8+ (*)	D78	PEG_TX8+ (*)
C24	PCI_AD0	D24	PCI_AD5	C79	PEG_RX8- (*)	D79	PEG_TX8- (*)
C25	PCI_AD2	D25	PCI_AD7	C80	GND (FIXED)	D80	GND (FIXED)
C26	PCI_AD4	D26	PCI_C/BE0#	C81	PEG_RX9+ (*)	D81	PEG_TX9+ (*)
C27	PCI_AD6	D27	PCI_AD9	C82	PEG_RX9- (*)	D82	PEG_TX9- (*)
C28	PCI_AD8	D28	PCI_AD11	C83	PP_TPM	D83	RSVD
C29	PCI_AD10	D29	PCI_AD13	C84	GND	D84	GND
C30	PCI_AD12	D30	PCI_AD15	C85	PEG_RX10+ (*)	D85	PEG_TX10+ (*)
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- (*)	D86	PEG_TX10- (*)
C32	PCI_AD14	D32	PCI_PAR	C87	GND	D87	GND
C33	PCI_C/BE1#	D33	PCI_SERR#	C88	PEG_RX11+ (*)	D88	PEG_TX11+ (*)
C34	PCI_PERR#	D34	PCI_STOP#	C89	PEG_RX11-(*)	D89	PEG_TX11- (*)
C35	PCI_LOCK#	D35	PCI_TRDY#	C90	GND (FIXED)	D90	GND (FIXED)
C36	PCI_DEVSEL#	D36	PCI_FRAME#	C91	PEG_RX12+ (*)	D91	PEG_TX12+ (*)
C37	PCI_IRDY#	D37	PCI_AD16	C92	PEG_RX12- (*)	D92	PEG_TX12- (*)

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C38	PCI_C/BE2#	D38	PCI_AD18	C93	GND	D93	GND
C39	PCI_AD17	D39	PCI_AD20	C94	PEG_RX13+ (*)	D94	PEG_TX13+ (*)
C40	PCI_AD19	D40	PCI_AD22	C95	PEG_RX13- (*)	D95	PEG_TX13- (*)
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	PCI_AD21	D42	PCI_AD24	C97	RVSD	D97	PEG_ENABLE#
C43	PCI_AD23	D43	PCI_AD26	C98	PEG_RX14+ (*)	D98	PEG_TX14+ (*)
C44	PCI_C/BE3#	D44	PCI_AD28	C99	PEG_RX14- (*)	D99	PEG_TX14- (*)
C45	PCI_AD25	D45	PCI_AD30	C100	GND (FIXED)	D100	GND (FIXED)
C46	PCI_AD27	D46	PCI_IRQC#	C101	PEG_RX15+ (*)	D101	PEG_TX15+ (*)
C47	PCI_AD29	D47	PCI_IRQD#	C102	PEG_RX15- (*)	D102	PEG_TX15- (*)
C48	PCI_AD31	D48	PCI_CLKRUN#	C103	GND	D103	GND
C49	PCI_IRQA#	D49	PCI_M66EN (*)	C104	VCC_12V	D104	VCC_12V
C50	PCI_IRQB#	D50	PCI_CLK	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+	D52	PEG_TX0+	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0-	D53	PEG_TX0-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV# (*)	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+	D55	PEG_TX1+	C110	GND (FIXED)	D110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-CA6.

The signals marked with an asterisk symbol (**) are not supported on conga-CA6 industrial temperature range variants.

8.5 Bootstrap Signals

Table 29 Bootstrap Signal Descriptions

Signal	Pin #	Description of Bootstrap Signal	I/O	PU/PD	Comment
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	I/O 2.5VSB	PU 4k99 2.5VSB	GBE0_ACT# is a bootstrap signal (see caution statement below)
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB	PD 1k	GBE0_LINK# is a bootstrap signal (see caution statement below)
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	I/O 2.5VSB	PU 4k99 2.5VSB	GBE0_LINK100# is a bootstrap signal (see caution statement below)
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB	PD 1k	GBE0_LINK1000# is a bootstrap signal (see caution statement below)
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	LVDS_I2C_DAT is a bootstrap signal (see caution statement below).
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		SPKR is a bootstrap signal (see caution statement below)
SDVO_I2C_DAT (SDVO_DATA)	C73	SDVO I²C data line to set up SDVO peripherals.	I/O 3.3V		SDVO_I2C_DAT is a bootstrap signal (see caution statement below)

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either COM Express™ internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM Express™ module to malfunction and/or cause irreparable damage to the module.

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-CA6 module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.2 Interrupt Request (IRQ) Lines

Table 30 IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		IRQ3 via SERIRQ or PCI BUS INTx
4	Yes		IRQ4 via SERIRQ or PCI BUS INTx
5	Yes		IRQ5 via SERIRQ
6	Yes		IRQ6 via SERIRQ or PCI BUS INTx
7	Yes		IRQ7 via SERIRQ or PCI BUS INTx
8	No	Real-time Clock	Not applicable
9	No	SCI	Not applicable
10	Yes		IRQ10 via SERIRQ or PCI BUS INTx
11	Yes		IRQ11 via SERIRQ or PCI BUS INTx
12	Yes		IRQ12 via SERIRQ or PCI BUS INTx
13	No	Math processor	Not applicable
14	Note	IDE Controller 0 (IDE0) / Generic	IRQ14 via SERIRQ or PCI BUS INTx
15	Note	IDE Controller 1 (IDE1) / Generic	IRQ15 via SERIRQ or PCI BUS INTx

In PIC mode, the PCIe bus interrupt lines can be routed to any free IRQ.

Note

If the SATA and PATA interface mode configuration in BIOS setup is NOT set to legacy IDE mode, IRQ14 and 15 are free for PCI/LPC bus. In

ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCIe interrupt line.

Table 31 IRQ Lines in APIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		LPC bus via SERIRQ
4	Yes		LPC bus via SERIRQ
5	Yes		LPC bus via SERIRQ
6	Yes		LPC bus via SERIRQ
7	Yes		LPC bus via SERIRQ
8	No	Real-time Clock	Not applicable
9	Note	Generic	LPC bus via SERIRQ , option for SCI
10	Yes		LPC bus via SERIRQ
11	Yes		LPC bus via SERIRQ
12	No		LPC bus via SERIRQ exclusively
13	No	Math processor	Not applicable
14	Yes		LPC bus via SERIRQ
15	Yes		LPC bus via SERIRQ
16	No		PIRQA, Integrated Graphics Device, HDA Controller, PCIe Bridge #0, PCIe Port #1slot, PCIe Port #2slot, PCIe Port #3slot, PCIe Root Port #0, PCIe Root Port #1, PCIe Root Port #2, PCIe Root Port #3, OHCI Host#1
17	No		PIRQB, PCIe Bridge #0, PCIe Port #1slot, PCIe Port #2slot, PCIe Port #3slot, AHCI Controller
18	No		PIRQC,PCIe Bridge #0, PCIe Port #1slot, PCIe Port #2slot, PCIe Port #3slot, SDIO Host#0, SDIO Host#1
19	No		PIRQD, PCIe Bridge #0, PCIe Port #1slot, PCIe Port #2slot, PCIe Port #3slot, OHCI Host#0, USB Device
20	Yes		PIRQE
21	Yes		PIRQF
22	Yes		PIRQG
23	Yes		PIRQH

In APIC mode, the PCI bus interrupt lines are connected with IRQ 20, 21, 22 and 23.

Note

In ACPI and APIC mode, IRQ9 or IRQ20 is used for the SCI (System Control Interrupt).

9.3 PCI Configuration Space Map

Table 32 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	01h	00h	N.A.	Device ID 4114h
00h	02h	00h	Internal	IGD (integrated graphics device)
00h	03h	00h	Internal	SDVO Unit Display
00h	17h	00h	Internal	PCIe Port 0
00h	18h	00h	Internal	PCIe Port 1
00h	19h	00h	Internal	PCIe Port 2
00h	1Ah	00h	Internal	PCIe Port 3
00h	1Bh	00h	Internal	Intel High Definition Audio
00h	1Fh	00h	Internal	LPC Interface
01h	00h	00h	Internal	PCI Express Bridge
02h	00h	00h	Internal	Packet Hub Control
02h	00h	01h	Internal	Gigabit Ethernet MAC
02h	00h	02h	Internal	GPIO
02h	02h	00h	Internal	USB 2.0 OHCI Host #1
02h	02h	01h	Internal	USB 2.0 OHCI Host #1
02h	02h	02h	Internal	USB 2.0 OHCI Host #1
02h	02h	03h	Internal	USB 2.0 OHCI Host #1
02h	02h	04h	Internal	USB Device
02h	04h	00h	Internal	SDIO #0
02h	04h	01h	Internal	SDIO #1
02h	06h	00h	Internal	SATA
02h	08h	00h	Internal	USB 2.0 OHCI Host #2
02h	08h	01h	Internal	USB 2.0 OHCI Host #2
02h	08h	02h	Internal	USB 2.0 OHCI Host #2
02h	08h	03h	Internal	USB 2.0 OHCI Host #2
02h	0Ah	00h	Internal	Shared DMA
02h	0Ah	01h	Internal	UART #0
02h	0Ah	02h	Internal	UART #1
02h	0Ah	03h	Internal	UART #2
02h	0Ah	04h	Internal	UART #3
02h	0Ch	00h	Internal	Shared DMA
02h	0Ch	01h	Internal	SPI
02h	0Ch	02h	Internal	I2C
02h	0Ch	03h	Internal	CAN
03h	00h	00h	Internal	PCI to PCI Bridge

04h	03h	00h	Internal	RAID Controller

Note

The given bus numbers only apply to a conga-CA6 supporting onboard Gbe LAN with both PCI Express Ports being enabled in the BIOS setup. When using carrier boards with a PCIe packet switch at PCIe slot 1 the bus number of the Onboard LAN controller is increased by the number of PCI bridges within the switch.

9.4 PCI Interrupt Routing Map

Table 33 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line [1]	APIC Mode IRQ	IGD	SDVO	HDA	PCIe Root Port 0	PCIe Root Port 1	PCIe Root Port 2	PCIe Root Port 3	OHCI Host #0	EHCI Host #0	USB Device	OHCI Host #1
A		16	x	x	x	x	x	x	x				x
B		17											
C		18											
D		19								x	x	x	
E	INTA	20											
F	INTB	21											
G	INTC	22											
H	INTD	23											

Table 34 PCI Interrupt Routing Map (continued)

PIRQ	EHCI Host #1	DMA	SPI	I2C	CAN	UART	SATA	LAN	GPIO	PCIe Slot Bridge 0	PCIe Slot Port 1	PCIe Slot Port 2	PCIe Slot Port 3
A	x							x	x	x [2]	x [3]	x [4]	x [5]
B							x			x [3]	x [4]	x [5]	x [2]
C			x	x	x					x [4]	x [5]	x [2]	x [3]
D		x				x				x [5]	x [2]	x [3]	x [4]
E													
F													
G													
H													

Note

[1] These interrupts are available for external devices/slots via the C-D connector rows.

[2] Interrupt used by single function PCI Express devices (INTA).

[3] *Interrupt used by multifunction PCI Express devices (INTB).*

[4] *Interrupt used by multifunction PCI Express devices (INTC).*

[5] *Interrupt used by multifunction PCI Express devices (INTD).*

9.5 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.6 SM Bus

System Management (SM) bus signals are connected to the Intel® EG20T Chipset Hub and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject please contact congatec technical support.

10 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

10.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> key during POST.

10.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used a message will be displayed during POST stating that the “Boot Selection Popup menu has been selected” and the menu itself will be displayed immediately after POST thereby allowing the operator to choose the boot device to be used.

10.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

Main	Advanced	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous values.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

10.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
BIOS ID	no option	Displays the BIOS ID.
OEM BIOS Version	no option	Displays the OEM BIOS ID.
Build Date	no option	Displays the date when the BIOS was built.
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
MAC Address	no option	Displays the MAC address of the board.
Running Time	no option	Displays the time the board is running [in hours max. 65535].
MRC Version	no option	Displays the MRC version number.
System Memory	no option	Displays the total amount of system memory.
►Platform Information	submenu	Opens the platform information submenu.
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24-hour format.*
System Date	Day of week, month/day/year	Specifies the current system date. *Note: The date is in month-day-year format.*

10.4 Platform Information submenu

Feature	Options	Description
Processor Version	no option	Displays the silicon revision of the processor.
IGD VBIOS	no option	Displays the Video BIOS version ID.
PUNIT Build Date	no option	Displays the PUNIT build date.
PUNIT Build Time	no option	Displays the PUNIT build time

10.5 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Power	Exit
	Graphic Configuration				
	Watchdog Configuration				
	PCI Subsystem Settings				
	ACPI Configuration				
	CPU Configuration				
	Chipset Configuration				
	AHCI SATA Configuration				
	SDIO Configuration				
	USB Configuration				
	Super IO Configuration				
	Serial Port Console Redirection				

10.5.1 Graphics Configuration Submenu

Feature	Options	Description
Primary Display	**Auto** IGD PEG	This option allows you to select the primary video device among Internal Graphic Driver, External Card or Auto configuration.
Internal VGA Mode Select	Enabled, 4MB **Enabled, 8MB** Enabled, 16MB Enabled, 32MB Enabled, 64MB	This option allows you to disable the internal VGA controller or enable it with 1MB, 4MB, 8MB, 16MB, 32MB or 64MB initial frame buffer size.
MSAC Mode Select	Enabled 128MB **Enabled 256MB** Enabled 512MB	Determines the size of the graphics memory aperture.
IGD – Boot Type	**No option**	VBIOS Default configuration
Boot Display Device	**Integrated SDVO** Integrated LVDS	Select the display device used for booting up.
Flat Panel Scaling	**Auto** Forced Disabled	Defines the Flat Panel Scaling mode.
Flat Panel Type	Auto VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) **WVGA 640x480 1x24 (01Bh)** SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 1x18 (008h) Customized EDID 1 Customized EDID 2 Customized EDID 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.*
DPST Control	**VBIOS-Default** DPST Disabled DPST Enabled L1 DPST Enabled L2 DPST Enabled L3 DPST Enabled L4 DPST Enabled L5	Determines whether the VBIOS default controls the Display Power Save Technology or the setup configures the desired level.
Backlight Inverter Type	**None** PWM I2C	Select the type of backlight inverter used. PWM = Use IGD PWM signal.
PWM Inverter Frequency	200 - 40000	Select PWM inverter frequency. Default 20300.
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100**%	Actual backlight value in percent of the maximum setting.

Feature	Options	Description
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently. Hidden if Backlight inverter Type is None.
Invert Backlight Setting	**No** Yes	Allow to invert backlight control values if required for the actual backlight hardware controller. Hidden if Backlight inverter Type is None.

10.5.2 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset..
Stop Watchdog For User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One time trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to ‘One time trigger’ the watchdog will be disabled after the first trigger. If set to ‘Single event’, every stage will be executed only once, then the watchdog will be disabled. If set to ‘Repeated event’ the last stage will be executed repeatedly until a reset occurs.
Delay	see Post Watchdog	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	NMI ACPI Event **Reset** Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about ACPI Event see note below.
Event 2	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.

Feature	Options	Description
Timeout 1	0.5sec 1sec 2sec 5sec 10sec **30sec** 1min 2min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

10.5.3 PCI Subsystem Settings Submenu

Feature	Options	Description
PCI BUS Driver Version	**no option**	Displays the PCI Bus driver version ID number
PCI ROM Priority	**[EFI Compatible ROM]** Legacy ROM	In case of multiple Option ROMS, specifies what Option ROM is to be launched.
Launch PXE OpROM	**Disabled** Enabled	*Allows the launching of PXE Option ROMS*
Launch Storage OpROM	Disabled **Enabled**	Allows the launching of Storage Option ROMS
PCI Express Ports Configuration	submenu	Opens the platform information submenu.
PCI Latency Timer	32, 64, 96, ... 248	Specifies the PCI latency using bus clock units.
VGA Palette Snoop	**Disabled** Enabled	Enables or Disables VGA palette registers snooping.
PERR# Generation	**Disabled** Enabled	Enables or Disables PCI device to generate PERR#.
SERR# Generation	**Disabled** Enabled	Enables or Disables PCI device to generate SERR#.
Relaxed Ordering	**Disabled** Enabled	Enables or Disables PCI Express device Relaxed Ordering.
Reserved Interrupt 1	**None** IRQ3 IRQ4 IRQ6 IRQ7 IRQ10 IRQ11 IRQ14 IRQ15	Reserves additional IRQ for custom purposes.

Feature	Options	Description
Reserved Interrupt 2	**None** IRQ3 IRQ4 IRQ6 IRQ7 IRQ10 IRQ11 IRQ14 IRQ15	Reserves additional IRQ for custom purposes.
PIRQ Routing	submenu	
Extended Tag	**Disabled** Enabled	Allows device to use 8-bit tag field as a requester.
No Snoop	**Disabled** Enabled	Enables or Disables PCI Express Device no snoop option.
Maximum Payload	**Auto**, 128, 256, 512, 1024, 2048, 4096	Sets the maximum payload value on bytes or allows the system BIOS to select the value.
Maximum Read Request	**Auto**, 128, 256, 512, 1024, 2048, 4096	Sets the maximum read request value on bytes or allows the system BIOS to select the value.
Automatic ASPM	**Disabled** Enabled	Enables or disables ASPM on reported capabilities and known issues.
Extended Synch	**Disabled** Enabled	Enables or disables the generation of extended synchronization patterns.

10.5.4 PCI Express Ports 1-4 Configuration Submenu

Feature	Options	Description
PCI Express Root Port 0..3	Disabled **Enabled**	Controls the PCI Express Root port.

10.5.5 PIRQ Routing Submenu

Feature	Options	Description
PIRQA...H	**Auto** IRQ3 IRQ4 IRQ6 IRQ7 IRQ10 IRQ11 IRQ14 IRQ15	Sets Interrupt for selected PIRQ. Refer to the board's Resource List for a detailed description of devices connected to the respective PIRQ. This setup node is only effective while operating in PIC (non IOAPIC) interrupt mode.

10.5.6 PCI to PCI Bridge Submenu

Feature	Options	Description
Extra Bus Reserved	**0**-7	Extra BUS reserved for bridges behind the PCI root Bridge. Range 0 to 7

10.5.7 ACPI Configuration Submenu

Feature	Options	Description
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or disables BIOS ACPI Auto Configuration
Enable Hibernation	**Disabled** Enabled	Enables or disables System ability to hibernate (OS/S4 Sleep State).
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the state used for ACPI system sleep/suspend
Critical Trip Point	70, 80, 90, 95, 100, 105, 110, 115, 120, **125°C**, Disabled	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Active Trip Point	Disabled, 30, 40, 50, **60**, 70, 80, 90, 95, 100°C	*Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.*
Passive Trip Point	Disabled, 30, 40, 50, 60, 70, 80, 90, **95**, 100°C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.

Note

In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

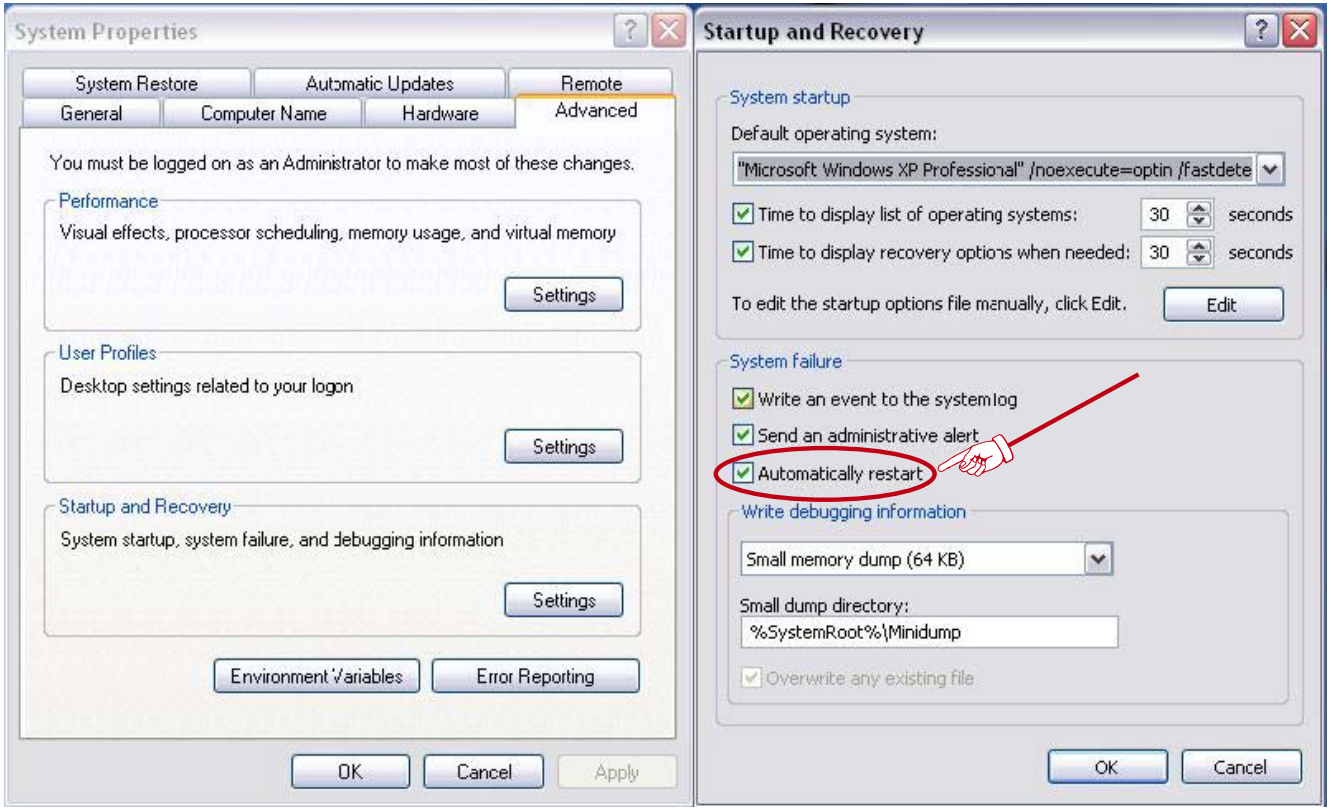
For Restart: An ACPI fatal error is reported to the OS.

It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very brief blue-screen the system will restart.

You can enable this setting buy going to the "System Properties" dialog box and choosing the "Advanced" tab. Once there choose the "Settings" button for the "Startup and Recovery" section. This will open the "Startup and Recovery" dialog box. In this dialog box under "System failure" there are three check boxes that define what Windows will do when a fatal error has been detected. To ensure that the system restarts after a 'Watchdog ACPI Event" is set to 'Restart', you must make sure that the check box for the selection "Automatically restart" is checked. If this

option is not selected then Windows will remain at a blue-screen after a 'Watchdog ACPI Event" that has been configured for 'Restart' has been generated. Below is a Windows screen-shot showing the proper configuration.

Win XP Watchdog ACPI Event restart configuration



10.5.8 CPU Configuration Submenu

Feature	Options	Description
CPU Information	no option	Describes the CPU/Processor main parameters.
Intel(R) SpeedStep(tm)	Disabled **Enabled**	Disabled: CPU speed is set to maximum and cannot be altered by the operating system. Enabled: CPU speed is controlled by the operating system.
Hyperthreading	Disabled **Enabled**	Enables or disables Intel Hyperthreading Technology for being used by the OS.
Execute Disable Bit	Disabled **Enabled**	Enable or disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled, certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting OS.
Limit CPUID Maximum	**Disabled** Enabled	When enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When disabled, the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Intel Virtualization Technology	**Disabled** Enabled	When enabled, a VMM can utilize the additional hardware capabilities provided by the Vanderpool Technology.
C-States	**Disabled** Enabled	Enable support for supported standard CPU idle states.
C-State POPUP	**Enabled** Disabled	Enables or disables C-State POPUP.
Enhanced C-1	**Disabled** Enabled	Enables or disables the Enhanced C1 State.
Enhanced C-2	**Disabled** Enabled	Enables or disables the Enhanced C2 State.
Enhanced C-3	**Disabled** Enabled	Enables or disables the Enhanced C3 State.
Enhanced C-4	**Disabled** Enabled	Enables or disables the Enhanced C4 State.

10.5.9 Chipset Configuration Submenu

Feature	Options	Description
Audio Controller	Auto Enabled **Disabled**	Controls activation of the HDA controller device. Disabled = HDA controller will be unconditionally disabled Enabled = HDA controller will be unconditionally enabled Auto = HDA Controller will be enabled if HDA codec present, disabled otherwise.
Azalia PME Enable	Disabled **Enabled**	Enables or disables the Azalia PME (Power Management Events)
Azalia Vci Enable	Disabled **Enabled**	Enables or disables the Azalia Vci
SMBUS Controller	**Disabled** Enabled	Enables disables the SMBUS Controller
Network Settings	submenu	EG20T MAC Device configuration.
EG20T Ethernet PHY	**Enabled** Disabled during S5 Disabled during S3/S5 Disabled Always	Configures the Chip Power State of Ethernet PHY. Disable S5 and Disable S3/S5 set the PHY on Power off mode saving energy during the system ACPI Power States S3 or S5. Enable/Disabled always configures Power On/Power off for all the ACPI states.
High Precision Timer	Disabled **Enabled**	Enable or disable the high precision event timer (HPET). This timer can be used for precise multimedia or real time application timing. Special software support is required.

Note

The BIOS does not initialize the HDA codec. The codecs remains in default mode and must be initialized by its respective device driver.

10.5.9.1 Network Settings Submenu

Feature	Options	Description
Network Stack	**Disabled** Enabled	Enable/Disable the Network Stack for PXE and UEFI.
Wake on LAN	Disabled **Enabled**	Enables/Disables WOL.
WOL Mode	**Wake Up Frame** Magic packet	Selects WOL Mode. Hidden if Wake on LAN is disabled.
WOL Speed	**10 Mbps** 100Mbps 1000Mbps	Selects WOL Speed. Hidden if Wake on LAN is disabled.

10.5.10 AHCI SATA Configuration

Feature	Options	Description
PORT 0	Disabled **Enabled**	This node enables or disables the Set Transfer mode programming for SATA port 0
PORT 1	Disabled **Enabled**	This node enables or disables the Set Transfer mode programming for SATA port 1

10.5.11 SDIO Configuration Submenu

Feature	Options	Description
SDIO Access Mode	**Auto** DMA PIO	Configures the access to the SD devices. With Auto, the controller determines the SD access method.

10.5.12 USB Configuration Submenu

Feature	Options	Description
USB Device List	no option	List of the USB devices connected to the system updated dynamically.
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
EHCI Hand-off	Disabled **Enabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device Start Unit command timeout.
Controller Timeout	1 sec 5 sec 10 sec **20 sec**	Timeout value for legacy USB control, bulk and interrupt transfers.
USB Mass Storage Device Name *(Auto detected USB mass storage devices are listed here dynamically)*	**Auto** Floppy Forced FDD Hard Disk CD-ROM	Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. Note: *The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly. Select AUTO to let the BIOS auto detect the current formatted media.* If Floppy is selected then the device will be emulated as a floppy drive. Forced FDD allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. Hard Disk allows the device to be emulated as hard disk. CDROM assumes the CD-ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

10.5.13 Super I/O Winbond Configuration Submenu

Feature	Options	Description
Super IO Chip	**no option**	Displays Winbond SIO ID.
Serial Port 0 Configuration	submenu	Opens the Serial Port 0 Configuration submenu.
Serial Port 1 Configuration	submenu	Opens the Serial Port 1 Configuration submenu.
Wake on Ring	Disabled **Enabled**	Enables or disables SIO wake.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

10.5.13.1 Serial Port 0/1 Configuration Submenu

Feature	Options	Description
Serial Port 0	Disabled **Enabled**	Enable or disable serial port 0.
Device Settings	IO=3F8h; IRQ=4;	Fixed configuration of serial port 0 if enabled.
Change Settings	[Auto] [IO=3F8; IRQ=4] [IO=3F8 IRQ=3,4,5,6,7, 8, 9,10,11,12] [IO=2F8 IRQ=3,4,5,6,7, 8, 9,10,11,12] [IO=3E8 IRQ=3,4,5,6,7, 8, 9,10,11,12] [IO=2E8 IRQ=3,4,5,6,7, 8, 9,10,11,12]	Selects the IO port address and Interrupt for the SIO Port
Device Mode	**Normal** High Speed	Changes the serial port mode

10.5.14 Serial Port Console Redirection

Feature	Options	Description
COM0/COM1	no option	
Console Redirection	**Disabled** Enabled	Allows the Console Redirection Settings note selection
Console Redirection Settings	submenu	Opens the Serial Port 1/Port2 Console Redirection submenu. Only selectable when console redirection is enabled
Serial Port for Out-of-Band Management/ Windows EMS	no option	Serial Port for Out-of-Band Management/ Windows Emergency Management Services (EMS)
Console Redirection	Disabled **Enabled**	Allows the Serial redirection for Windows EMS
Out-of-Band Mgmt Port	**COM0** COM1 COM4	Defines the Serial Pot used for the Windows EMS
Terminal Type	VT100 VT100+ **VT-UTF8** ANSI	This note defines the Terminal Type used for the connection.

10.5.14.1 Console Redirection Settings

Feature	Options	Description
Console Redirection Setting	no option	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	**8** 7	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Feature	Options	Description
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/ stop signals. Software flow control uses start/stop ASCII chars, which slows down the data flow and can be problematic if binary data is being sent.
Recorder Mode	**Disabled** Enabled	On this mode enabled only text will be send. This is to capture Terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution.
Legacy OS Redirection Resolution	**80x24** 80x25	Legacy OS Redirection Resolution.

10.6 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

10.6.1 Boot Settings Configuration Submenu

Feature	Options	Description
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. *Note: The default OEM logo is a dark screen.*
Fast Boot	**Disabled** Enabled	Enables or disables UEFI fast boot with initialization of a minimal set of devices required to launch the active boot option.
Setup Prompt Timeout	**1** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot, 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. *Note: Only works with an ATX type power supply.*
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The "Device Based" boot priority list allows you to select from a list of currently detected devices only. The "Type Based" boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the "Device Based" boot priority list might change dynamically in cases when devices are physically removed or added to the system. The "Type Based" boot menu is static and can only be changed by the user.

Feature	Options	Description
1st, 2nd, 3rd, ... Boot Device (Up to 11 boot devices can be prioritized if device based priority list control is selected. If “Type Based” priority list control is enabled only 8 boot devices can be prioritized.)	Disabled SATA 0 Drive SATA 1 Drive Primary Master Secondary Master Addon Via Controller USB Floppy USB Harddisk USB CDROM Onboard LAN External LAN Other BEV Device	This view is only available when in the default “Type Based” mode. When in “Device Based” mode you will only see the devices that are currently connected to the system.
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
CSM16 Module Version	no option	Displays the CSM16 Version ID
GateA20 Active	**Upon Request** Always	Gate A20 control. Upon Request = Gate A20 can be disabled using BIOS services. Always = Do not allow disabling Gate A20.
Option ROM Messages	Force BIOS **Keep Current**	Set display mode for option ROMs.
Interrupt 19 Capture	**Disabled** Enabled	Defines whether option ROMs may trap the INT19h legacy boot vector.

10.7 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

10.7.1 Security Settings

Feature	Options	Description
Setup Administrator Password	Enter password	Specifies the setup administrator password.

10.8 Save & Exit

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen. You can display the Save & Exit screen option by highlighting it using the ← Arrow → Keys.

10.8.1 Save & Exit Menu

Feature	Description
Save Changes and Exit	*Exit setup menu after saving the changes. The system is only reset if settings have been changed.*
Discard Changes and Exit	*Exit setup menu without saving any changes.*
Save Changes and Reset	*Save changes and reset the system.*
Discard Changes and Reset	Reset the system without saving any changes.
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Restore Defaults	Restore default values for all the setup options.

11 Additional BIOS Features

The conga-CA6 uses a congatec/AMI AptioEFI that is stored in an onboard SPI Flash chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as CTOPR1xx, where CTOP is the congatec internal BIOS project name for conga-CA6, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

11.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” refer to the user’s guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

11.2 BIOS Security Features

The BIOS provides a setup administrator password that limits access to the BIOS setup menu.

12 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.3	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
PICMG® COM Express Module™ Base Specification	http://www.picmg.org/
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications