



COM Express™ conga-CA

Intel® Atom™ ZX5xx series processors with an Intel® System Controller Hub US15W

User's Guide

Revision 1.0

Revision History

Revision	Date (dd.mm.yy)	Author	Changes
0.1	10.10.08	GDA	Preliminary release
0.2	11.10.08	GDA	Corrected module size values in section 1.3 "Mechanical Dimensions". Power consumption values are currently not available. Added TBD (To Be Determined) to tables in sections 1.5.1 to 1.5.4 and section 1.6.1.
0.3	19.03.09	GDA	Added power consumption values to tables in sections 1.5.1, 1.5.3 and 1.6.1. Updated section 9 "BIOS Setup Description".
1.0	12.11.09	GDA	Official release. Added new conga-CA variant PN: 061127. Updated drawing in section 1.3 "Mechanical Dimensions". Added pin number columns to pinout tables in section 7 "Signal Descriptions and Pinout Tables." Updated sections 8 "System Resources" and 9 "BIOS Setup Description."

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-CA. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide

COM Express™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols are used in this user's guide:



Warning

Warnings indicate conditions that, if not observed, can cause personal injury.



Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.



Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PATA	Parallel ATA
T.O.M.	Top of memory = max. DRAM installed
HDA	High Definition Audio
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

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COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). It's creation provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available today. COM Express™ modules are available in following form factors:

- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x 110mm

The COM Express™ specification 1.0 defines five different pinout types.

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports
Type 1	A-B	Up to 6			1
Type 2	A-B C-D	Up to 22	32 bit	1	1
Type 3	A-B C-D	Up to 22	32 bit		3
Type 4	A-B C-D	Up to 32		1	1
Type 5	A-B C-D	Up to 32			3

congatec AG modules utilize the Type 2 pinout definition. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are a legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 2 pinout provides the ability to offer 32-bit PCI, Parallel ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

Certification

congatec AG is certified to DIN EN ISO 9001:2000 standard.



Technical Support

congatec AG technicians and engineers are committed to providing the best possible technical support for our customers so that our products can be easily used and implemented. We request that you first visit our website at www.congatec.com for the latest documentation, utilities and drivers, which have been made available to assist you. If you still require assistance after visiting our website then contact our technical support department by email at support@congatec.com

Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device



All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

conga-CA Options Information

The conga-CA is currently available in five different variants. This user's guide describes all of these options. Below you will find an order table showing the different configurations that are currently offered by congatec AG. Check the table for the Part no./Order no. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Part-No.	087477	099881	061125	033321	061127
Processor	Intel® Atom™ Z510 1.1GHz	Intel® Atom™ Z510 1.1GHz	Intel® Atom™ Z530 1.6GHz	Intel® Atom™ Z530 1.6GHz	Intel® Atom™ Z530 1.6GHz
L2 Cache	512kB	512kB	512kB	512kB	512kB
Onboard Memory	512MB DDR2 (400 MT/s)	512MB DDR2 (400 MT/s)	1.0GB DDR2 (533 MT/s)	1.0GB DDR2 (533 MT/s)	1.0GB DDR2 (533 MT/s)
FSB	400MHz	400MHz	533MHz	533MHz	533MHz
PCI Express	No	2x x1 links	No	2x x1 links	1x x1 links
32bit PCI Bus	Yes	No	Yes	No	No
SATA	Yes	No	Yes	No	No
2 Onboard SDIO/MMC sockets	Yes	No	Yes	No	No
Gigabit Ethernet	Yes	No	Yes	No	Yes
CPU TDP	2 W	2 W	2.3 W	2.3 W	2.3 W

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1 Specifications

1.1 Feature List

Table 1 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 2 (Compact size 95 x 95mm)	
Processor	Intel® Atom™ Z510 1.1GHz with 512kB L2 cache Intel® Atom™ Z530 1.6GHz with 512kB L2 cache with Hyper Threading Support	
Memory	Onboard DDR 2 up to a maximum of 1 GB	
Chipset	Intel® System Controller Hub US15W	
Audio	HDA (High Definition Audio)/digital audio interface with support for multiple codecs	
Ethernet	Gigabit Ethernet, Realtek 8111 (uses one x1 PCI Express Link)	
Graphics Options	Intel® Graphics Media Accelerator 500 (Intel® GMA 500), up to 256MB frame buffer supporting DirectX 9.0 and Open GL 2.0. Dual independent display support. <ul style="list-style-type: none"> • Flat panel Interface (integrated) 112MHz LVDS Transmitter Supports 1x18 and 1x24 bit TFT configurations. Supports both conventional (FPDI) and non-conventional (LDI) color mappings. Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3) Resolutions 640x480 up to 1366x768. • AUX Output 1 x Intel compliant SDVO port (serial DVO). Resolutions up to 1280x1024. Supports external DVI, TV and LVDS transmitters • Video Decode Acceleration: MPEG2 MPEG4 H.264 WMV9/VC1 	
Peripheral Interfaces	<ul style="list-style-type: none"> • 2x Serial ATA® (Provided by VIA VT6421 chip connected to the 32bit PCI bus) • 2x onboard SDIO/MMC (Secure Digital Input Output/Multimedia Card) Sockets • 2x x1 PCI Express Links (see note below) • 32 bit PCI Bus Rev. 2.3 	<ul style="list-style-type: none"> • 8x USB 2.0 (8 host ports, or 7 hosts + 1 client) • 1x EIDE (UDMA-66/100) • LPC Bus • I²C Bus, Fast Mode (400 kHz) multimaster
BIOS	Based on AMIBIOS® 1 MByte Flash BIOS with congatec Embedded BIOS features	
Power Management	ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).	


Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 8 of this user's guide to determine what options are available on your particular module.

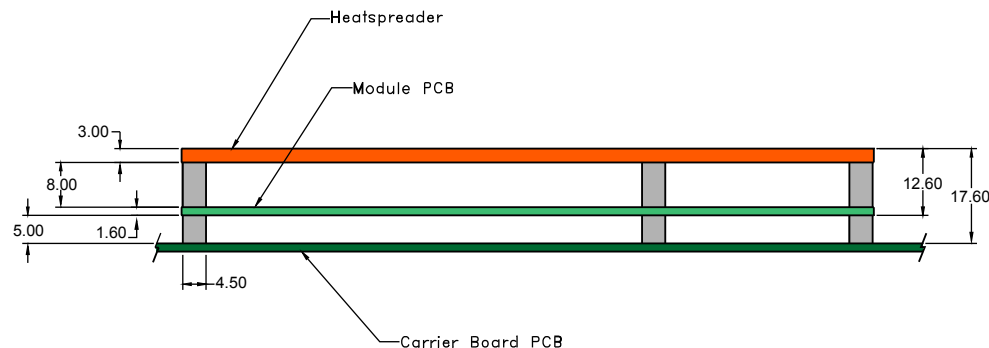
1.2 Supported Operating Systems

The conga-CA supports the following operating systems.

- Microsoft® Windows® Vista
- Microsoft® Windows® XP
- Microsoft® Windows® XP Embedded
- Microsoft® Windows® CE 6.0
- Linux
- QNX

1.3 Mechanical Dimensions

- 95.0 mm x 95.0 mm @ (3.75" x 3.75")
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm.



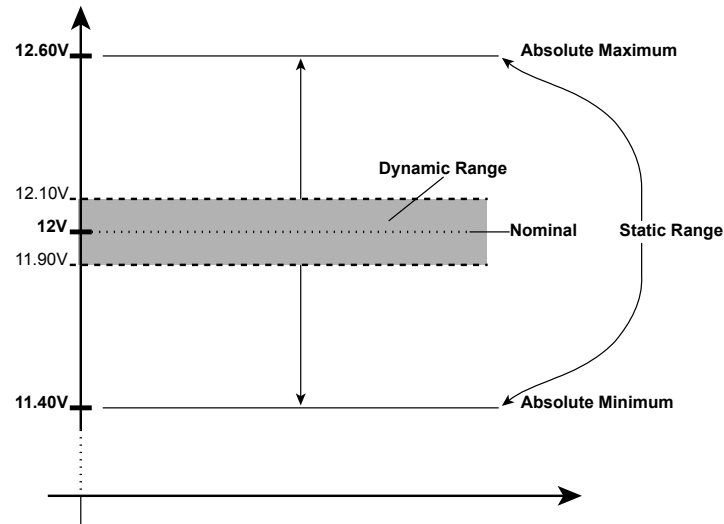
Note

conga-CA modules with hardware revision C.0 and later have a PCB thickness of 1.6mm. All previous hardware revisions of conga-CA have a PCB thickness of 2.0mm.

1.4 Supply Voltage Standard Power

- 12V DC \pm 5%

The dynamic range shall not exceed the static range.



1.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 2 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	16.5	12	11.4-12.6	11.4	+/- 100	188	85%	160
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

1.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum rise time of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

1.5 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used includes a conga-CA module, conga-CEVAL and conga-Cdebug carrier boards, SATA drive, and USB keyboard. When using the conga-Cdebug, the SATA drive was powered externally by an ATX power supply so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. The module was first inserted into the conga-Cdebug, which was powered by a Direct Current (DC) power supply set to output 12V. The current consumption value displayed by the DC power supply's readout is the value that is recorded as the power consumption measurement for Desktop Idle, 100% Workload and Standby modes. The power consumption of the conga-Cdebug (without module attached) was measured and this value was later subtracted from the overall power consumption value measured when the module and all peripherals were connected. All recorded values are approximate.

The conga-Cdebug does not provide 5V Standby power therefore S3 mode was measured using the conga-CEVAL powered by an ATX power supply with a multimeter attached to the 5V Standby power line. The 5V Standby power consumption of the conga-CEVAL (without module attached) and all peripherals connected was first measured and the resulting value was later subtracted from the overall S3 power consumption value measured when the module was attached. All S3 recorded values are approximate.

Each module was measured while running Windows XP Professional with SP2 (service pack 2) and the "Power Scheme" was set to "Portable/Laptop". This setting ensures that the Intel® Atom™ processors run in LFM (lowest frequency mode) with minimal core voltage during desktop idle. Power consumption values were recorded during the following stages:

Windows XP Professional SP2

- Desktop Idle (600MHz for the Intel® Atom™ Z510 and 800MHz for the Intel® Atom™ Z530)
- 100% CPU workload (see note below)
- Suspend to RAM (requires setup node "Suspend Mode" in BIOS to be configured to S3 STR (suspend to RAM)). Supply power for S3 mode is 5V.



Note

A software tool was used to stress the CPU to 100% workload.

Processor Information

In the following power tables there is some additional information about the processors. Intel® describes the type of manufacturing process used for each processor. The following term is used:

nm=nanometer

The manufacturing process description is included in the power tables. See example below. For information about the manufacturing process visit Intel®'s website.

Intel® Atom™ Z530 1.60GHz 512kB L2 cache
45nm

1.5.1 Intel® Atom™ Z510 1.1GHz 512kB L2 cache

With 512MB onboard memory

conga-CA/510-512 Art. No. 087477		Intel® Atom™ Z510 1.1GHz 512kB L2 cache 45nm Layout Rev. CMENLA0 /BIOS Rev. CMENR005		
Memory Size	512MB onboard			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V Input Power	
Power consumption (measured in Amperes/Watts)	0.5 A/6.0 W (12V)	0.6 A/7.2 W (12V)	0.09 A/0.5 W (5V)	

1.5.2 Intel® Atom™ Z510 1.1GHz 512kB L2 cache and PCIe

With 512MB onboard memory

conga-CA/Z510-512 PCIe Art. No. 099881		Intel® Atom™ Z510 1.1GHz 512kB L2 cache 45nm Layout Rev. CMENLC0 /BIOS Rev. CMENR112		
Memory Size	512MB onboard			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V Input Power	
Power consumption (measured in Amperes/Watts)	TBD A/ W (12V)	TBD A/ W (12V)	TBD A/ W (5V)	

1.5.3 Intel® Atom™ Z530 1.6GHz 512kB L2 cache

With 1GB onboard memory

conga-CA/530-1G Art. No. 061125		Intel® Atom™ Z530 1.6GHz 512kB L2 cache 45nm Layout Rev. CMENLA0 /BIOS Rev. CMENR006		
Memory Size	1GB onboard			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V Input Power	
Power consumption (measured in Amperes/Watts)	0.5 A/6.0 W (12V)	0.7 A/8.4 W (12V)	0.09 A/0.5 W (5V)	

1.5.4 Intel® Atom™ Z530 1.6GHz 512kB L2 cache and PCIe

With 1GB onboard memory

conga-CA/Z530-1G PCIe Art. No. 033321		Intel® Atom™ Z530 1.6GHz 512kB L2 cache 45nm Layout Rev. CMENLC0 /BIOS Rev. CMENR112		
Memory Size	1GB onboard			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V Input Power	
Power consumption (measured in Amperes/Watts)	TBD A/ W (12V)	TBD A/ W (12V)	TBD A/ W (5V)	

1.5.5 Intel® Atom™ Z530 1.6GHz 512kB L2 cache and GBE/PCIe

With 1GB onboard memory

conga-CA/Z530-1G GBE/PCIe Art. No. 061127		Intel® Atom™ Z530 1.6GHz 512kB L2 cache 45nm Layout Rev. CMENLC0 /BIOS Rev. CMENR112		
Memory Size	1GB onboard			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Suspend to Ram (S3) 5V Input Power	
Power consumption (measured in Amperes/Watts)	TBD A/ W (12V)	TBD A/ W (12V)	TBD A/ W (5V)	



All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Supply power for S3 mode is 5V while all other measured modes are supplied with 12V power. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

1.6 Supply Voltage Battery Power

- 2.0V-3.6V DC
- Typical 3V DC

1.6.1 CMOS Battery Power Consumption

RTC @ 20°C	Voltage	Current
Integrated in the Intel® System Controller Hub US15W	3V DC	2.7 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

1.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%



Caution

The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

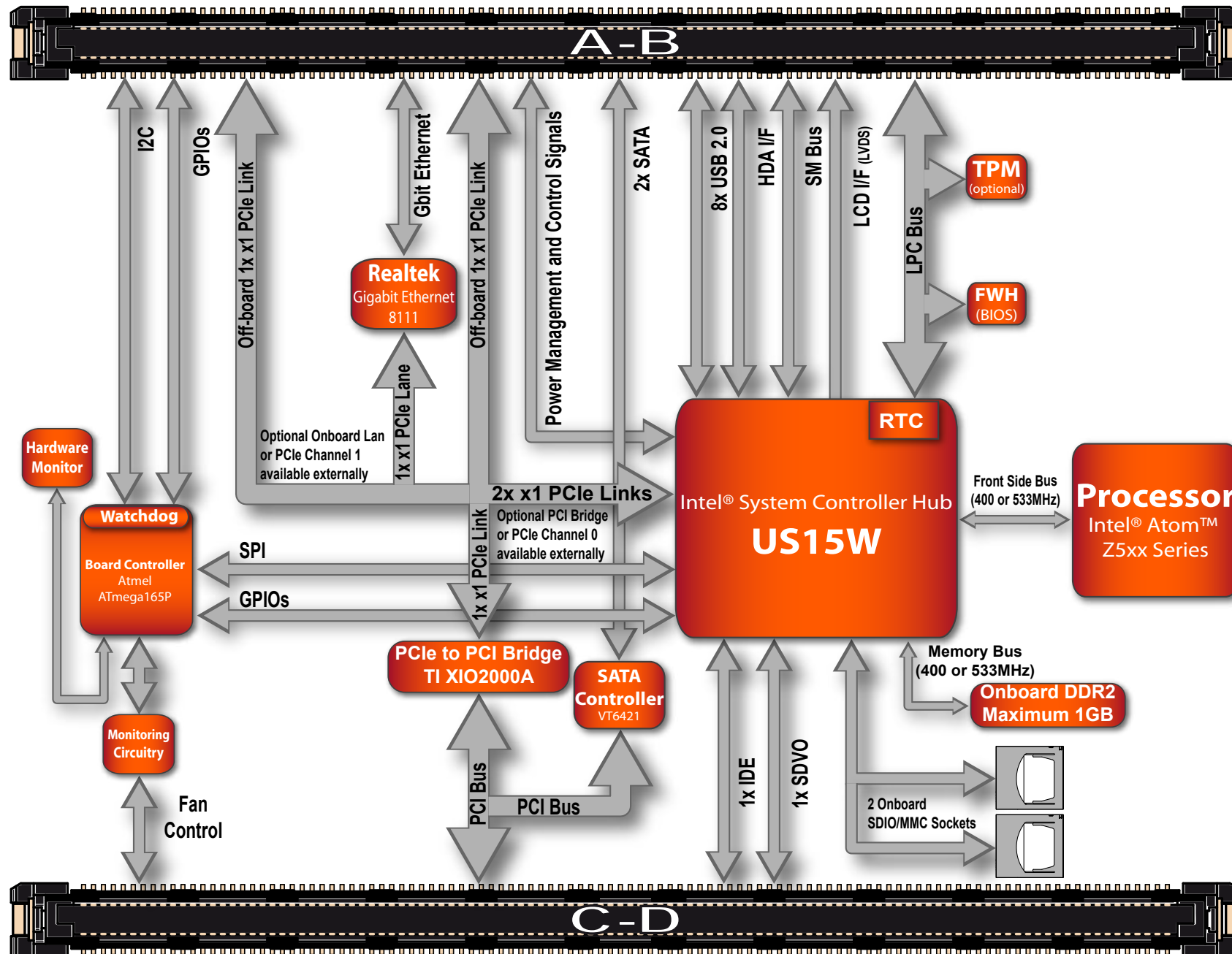
congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.

If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

For more information about operating a congatec module without heatspreader contact congatec technical support.

Humidity specifications are for non-condensing conditions.

2 Block Diagram



3 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module. It is a 3mm thick aluminum plate.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

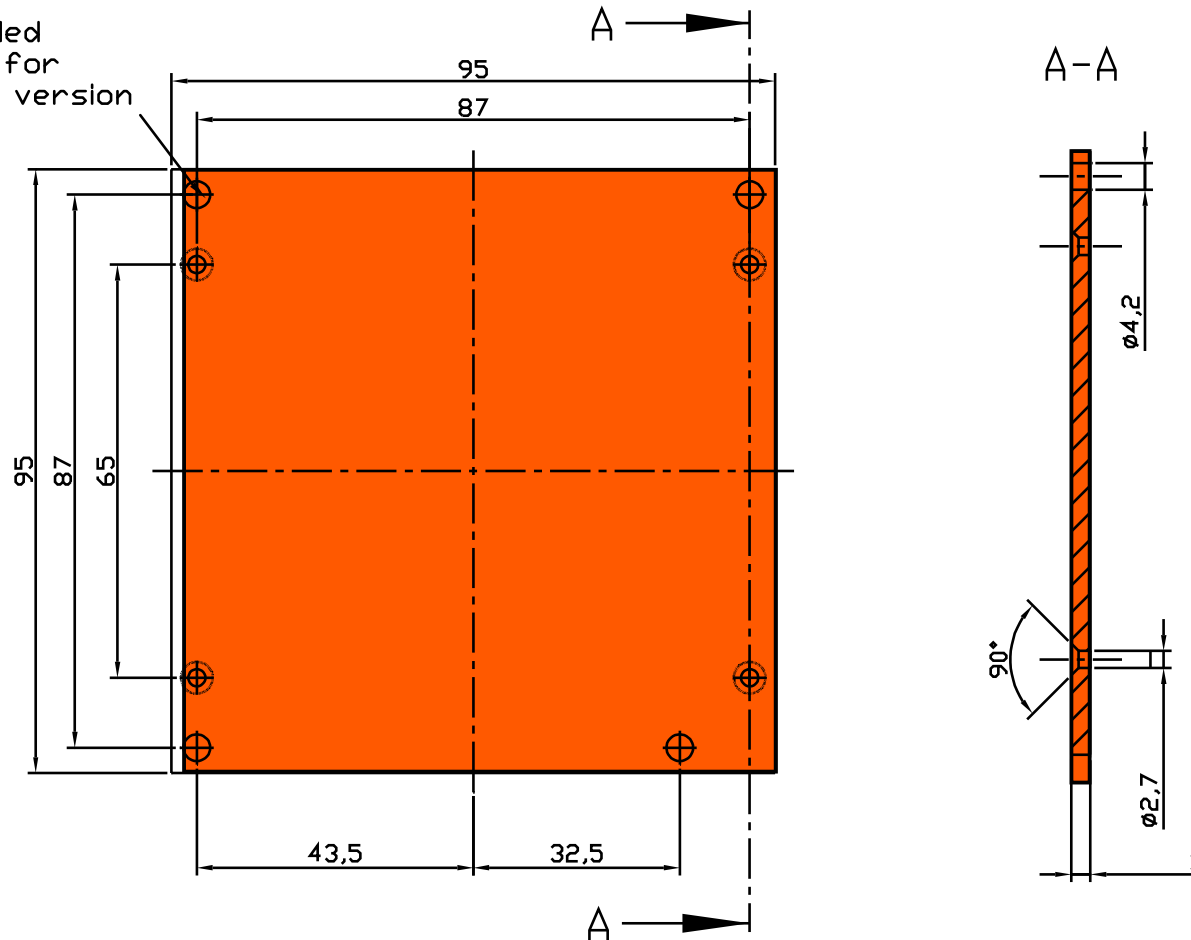


Caution

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

3.1 Heatspreader Dimensions

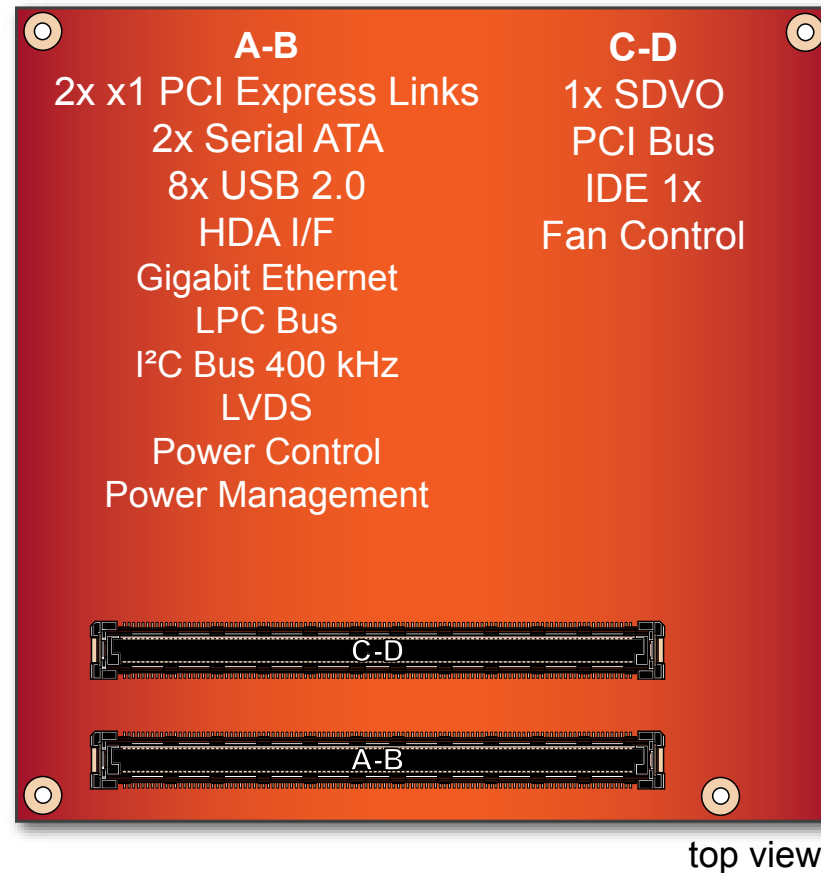
M2.5x11mm
 threaded standoff
 for threaded version
 or
 Ø2.7x11mm
 nonthreaded
 standoff for
 bore hole version



All measurements are in millimeters. Torque specification for heatspreader screws is 0.5 Nm.

4 Connector Subsystems Rows A, B, C, D

The conga-CA is connected to the carrier board via two 220-pin connectors (COM Express Type 2 pinout) for a total of 440 pins connectivity. These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.



In this view the connectors are seen “through” the module.



Not all the interfaces described above are available on all conga-CA variants. Use the article number of the module and refer to the options table on page 8 to determine the options available on the module.

4.1 Primary Connector Rows A and B

The following subsystems can be found on the primary connector rows A and B.

4.1.1 Serial ATA™ (SATA)

Two Serial ATA150 connections are provided by a VIA VT6421 PCI to 2 port Serial ATA host controller. SATA is an enhancement of the parallel ATA therefore offering higher performance. As a result of this enhancement the traditional restrictions of parallel ATA are overcome with respect to speed and EMI. SATA starts with a transfer rate of 150 Mbytes/s and can be expanded up to 600 Mbytes/s in order to accommodate future developments. SATA is completely protocol and software compatible to parallel ATA.



Not all variants of the conga-CA are equipped with a SATA controller.

4.1.2 USB 2.0

The conga-CA offers 3 UHCI USB host controllers and one EHCI USB host controller provided by the Intel® System Controller Hub US15W. These controllers comply with USB standard 1.1 and 2.0 and offer a total of 8 USB ports via connector rows A and B. Ports 0-5 are capable of supporting USB 1.1 and 2.0 compliant devices. Ports 6 and 7 are not multiplexed onto a UHCI controller, so they are only capable of high-speed operation and therefore only support the connection of USB 2.0 compliant devices. Additionally, the Intel® System Controller Hub US15W features a Universal Serial Bus 2.0 client controller. The USB client is configured to run on USB port 2. If the USB client controller is enabled then there are 7 host ports + 1 client port versus 8 host ports available on the conga-CA. For more information about the USB Client Controller and how the USB host controllers are routed see section 6.5.

4.1.3 High Definition Audio (HDA)

The conga-CA provides an interface that supports the connection of HDA audio codecs.

4.1.4 Gigabit Ethernet

The conga-CA is equipped with a Realtek 8111 Gigabit Ethernet Controller. This controller is implemented through the use of the second x1 PCI Express link found on the Intel® System Controller Hub US15W. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.



Note

Not all variants of the conga-CA are equipped with a Gigabit Ethernet controller.

4.1.5 LPC Bus

conga-CA offers the LPC (Low Pin Count) bus through the use of the Intel® System Controller Hub US15W. There are already many devices available for this Intel® defined bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific carrier board using this bus. See section 8.2.1 for more information about the LPC Bus.

4.1.6 I²C Bus 400kHz

The I²C bus is implemented through the use of ATMEL ATmega165P microcontroller. It provides a Fast Mode (400kHz max.) multi-master I²C Bus that has maximum I²C bandwidth.

4.1.7 PCI Express™

The conga-CA offers 2x x1 PCI Express links via the Intel® System Controller Hub US15W, which can be configured to support PCI Express edge cards or ExpressCards. These 2 x1 PCI Express links are available on the A,B connector row. The PCI Express interface is based on the PCI Express Specification 1.1.



Note

Not all variants of the conga-CA offer PCI Express links externally. Use the article number of the module and refer to the options table on page 8 to determine the options available on the module.

4.1.8 ExpressCard™

The conga-CA variants that provide PCI Express links at the connector can support the implementation of one ExpressCard, which requires the dedication of one USB port and one PCI Express link. Refer to section 7, “Signal Descriptions and Pinout Tables” for information about which ExpressCard port is supported.



Note

Not all variants of the conga-CA offer PCI Express links externally.

4.1.9 Graphics Output (VGA/CRT)

The conga-CA does not provide a VGA/CRT output.

4.1.10 LCD

The Intel® System Controller Hub US15W, found on the conga-CA, offers an integrated single channel LVDS interface that is internally connected to Display Pipe B. It supports the connection of 1x18 or 1x24 Bit TFT configurations.

4.1.11 TV-Out

The conga-CA does not offer a dedicated TV-Out interface. TV-Out can be made available via the SDVO interface offered by the conga-CA.

4.1.12 Power Control

PWR_OK

Power OK from main power supply. A high value indicates that the power is good. Using this input is optional. Through the use of an internal monitor on the +12V \pm 5% input voltage and/or the internal power supplies the conga-CA module is capable of generating its own power-on reset. According to the COM Express™ Specification PWR_OK is a 3.3V signal.

The conga-CA provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-CA's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

12 volt input power is the sole operational power source for the conga-CA. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A baseboard designer should be aware of the following important information when designing a power supply for a conga-CA application:

- It has also been noticed that on some occasions problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

4.1.13 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

4.2 Secondary Connector Rows C and D

The following subsystems can be found on the secondary connector rows C and D.

4.2.1 PCI Express Graphics (PEG)

The conga-CA does not support PCI Express Graphics.

4.2.2 SDVO

conga-CA provides one SDVO port via Display Pipe A of the Intel® System Controller Hub US15W. The SDVO port can support a variety of display types (VGA, LVDS, DVI, TV-Out) by an external SDVO device.

4.2.3 PCI Bus

The implementation of the PCI bus complies with PCI specification Rev. 2.3 and provides a 32bit parallel PCI bus that is capable of operating at 33/66MHz.



The PCI interface is specified to be +5V tolerant, with +3.3V signaling. Not all variants of the conga-CA offer the PCI Bus.

4.2.4 IDE (PATA)

The IDE host adapter is capable of UDMA-100 operation. Only the Primary IDE channel is supported.

5 Additional Features

5.1 Watchdog

The conga-CA is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-CA does not support external hardware triggering. For more information about the Watchdog feature see the BIOS setup description section 9.4.13 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

5.2 Onboard Microcontroller

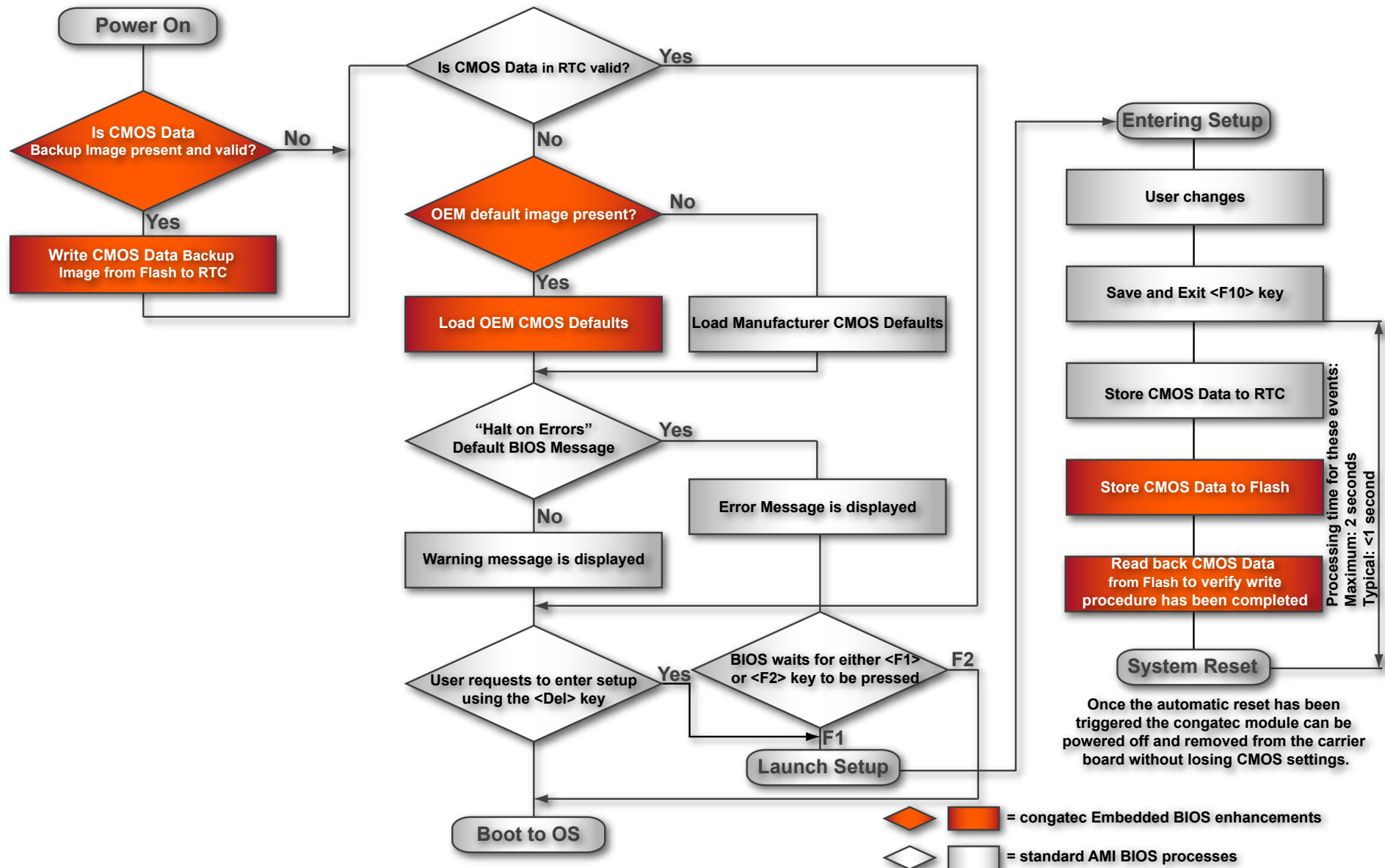
The conga-CA is equipped with an ATMEL Atmega165P microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

5.3 Embedded BIOS

The conga-CA is equipped with congatec Embedded BIOS and has the following features:

- ACPI Power Management
- ACPI Battery Support
- Supports Customer Specific CMOS Defaults
- Multistage Watchdog
- User Data Storage
- Manufacturing Data and Board Information
- OEM Splash Screen
- Flat Panel Auto Detection and Backlight Control
- BIOS Setup Data Backup (see section 5.3.1)
- Exclusive PCI Interrupts
- Fast Mode I²C Bus

5.3.1 Simplified Overview of BIOS Setup Data Backup



The above diagram provides an overview of how the BIOS Setup Data is backed up on congatec modules. OEM default values mentioned above refer to customer specific CMOS settings created using the congatec System Utility tool.

Once the BIOS Setup Program has been entered and the settings have been changed, the user saves the settings and exits the BIOS Setup Program using the F10 key feature. After the F10 function has been evoked, the CMOS Data is stored in a dedicated non-volatile CMOS Data Backup area located in the BIOS Flash Memory chip as well as RTC. The CMOS Data is written to and read back from the CMOS Data Backup area and verified. Once verified the F10 Save and Exit function continues to perform some minor processing tasks and finally reaches an automatic reset point, which instructs the module to reboot. After the Automatic Reset has been triggered the congatec module can be powered off and if need be removed from the baseboard without losing the new CMOS settings.

5.4 Onboard SDIO/MMC Sockets

The Intel® System Controller Hub US15W found on the conga-CA provides SDIO/MMC expansion ports used to communicate with a variety of SDIO and MMC devices. Two of these offered ports have been routed to onboard SDIO/MMC sockets located on the conga-CA module. Each port supports SDIO Revision 1.1 and MMC Revision 4.0 and is backward-compatible with previous interface specifications.

5.5 Security Features

The conga-CA can be equipped optionally with a “Trusted Platform Module“ (TPM 1.2). This TPM 1.2 includes coprocessors to calculate efficient hash and RSA algorithms with key lengths up to 2,048 bits as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity and confidence levels.

5.6 Suspend to RAM

The Suspend to RAM feature is available on the conga-CA.

5.7 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-CA BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM²C User's Guide

6 conga Tech Notes

The conga-CA has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

6.1 Comparison of I/O APIC to 8259 PIC Interrupt mode

I/O APIC (Advanced Programmable Interrupt controller) mode deals with interrupts differently than the 8259 PIC.

The method of interrupt transmission used by APIC mode is implemented by transmitting interrupts through the system bus and they are handled without the requirement of the processor to perform an interrupt acknowledge cycle.

Another difference between I/O APIC and 8259 PIC is the way the interrupt numbers are prioritized. Unlike the 8259 PIC, the I/O APIC interrupt priority is independent of the actual interrupt number.

A major advantage of the I/O APIC found in the chipset of the conga-CA is that it's able to provide more interrupts, a total of 24 to be exact. It must be mentioned that the APIC is not supported by all operating systems. In order to utilize the APIC mode it must be enabled in the BIOS setup program before the installation of the OS and it only functions in ACPI mode. You can find more information about APIC in the IA-32 Intel Architecture Software Developer's Manual, Volume 3 in chapter 8.



Note

You must ensure that your operating system supports APIC mode in order to use it.

6.2 Intel® Processor Features

6.2.1 Thermal Monitor and Catastrophic Thermal Protection

Intel® Atom™ Z5xx series processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature, that the Intel® Thermal Monitor uses to activate the TCC, cannot be configured by the user nor is it software visible.

The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel® Speedstep transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.



Note

The maximum operating temperature for Intel® Atom™ Z5xx series processors is 100°C.

Two modes are supported by the Thermal Monitor to activate the TCC. They are called Automatic and On-Demand. No additional hardware, software, or handling routines are necessary when using Automatic Mode.



Note

To ensure that the TCC is active for only short periods of time thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Atom™ Z5xx series processor's respective datasheet can provide more information about this subject.

THERMTRIP# signal is used by Intel® Atom™ Z5xx series processors for catastrophic thermal protection. If the processor's silicon reaches a temperature of approximately 115°C then the processor signal THERMTRIP# will go active and the system will automatically shut down to prevent any damage to the processor as a result of overheating. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.



Note

In order for THERMTRIP# to be able to automatically switch off the system it is necessary to use an ATX style power supply.

6.2.2 Processor Performance Control

Intel® Atom™ Z5xx series processors run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it's not being fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting found in the control panel option applet.



If the "Home/Office" or "Always On" power scheme is selected when using Windows operating systems then the processor will always run at the highest performance state. For more information about this subject see chapter 8 of the ACPI Specification Revision 2.0c, which can be found at www.acpi.info . Also visit Microsoft's website and search for the document called "Windows Native Processor Performance Control".

6.2.3 Intel® Virtualization Technology

Virtualization solutions enhanced by Intel® VT will allow Intel® Atom™ Z5xx series processors, that feature 2 Thread Support, to run multiple operating systems and applications in independent partitions. When using virtualization capabilities, one computer system can function as multiple “virtual” systems. With processor and I/O enhancements to Intel®’s various platforms, Intel® Virtualization Technology can improve the performance and robustness of today’s software-only virtual machine solutions.

Intel® VT is a multi-generational series of extensions to Intel® processor and platform architecture that provides a new hardware foundation for virtualization, establishing a common infrastructure for all classes of Intel® based systems. The broad availability of Intel® VT makes it possible to create entirely new applications for virtualization in servers, clients as well as embedded systems thus providing new ways to improve system reliability, manageability, security, and real-time quality of service.

The success of any new hardware architecture is highly dependent on the system software that puts its new features to use. In the case of virtualization technology, that support comes from the virtual machine monitor (VMM), a layer of software that controls the underlying physical platform resources sharing them between multiple “guest” operating systems. Intel® VT is already incorporated into most commercial and open-source VMMs including those from VMware, Microsoft, XenSource, Parallels, Virtual Iron, Jaluna and TenAsys.

You can find more information about Intel Virtualization Technology at: <http://developer.intel.com/technology/virtualization/index.htm>



Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

6.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system’s thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-CAACPI thermal solution offers three different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the “passive cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the “active cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the “critical trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

**Note**

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled according to the formula below.

$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

- ΔP is the performance delta
- T_t is the target temperature = critical trip point
- The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants. These constants are set to fixed values for the conga-CA:
- TC1= 1
- TC2= 5
- TSP= 5 seconds

See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

6.4 ACPI Suspend Modes and Resume Events

conga-CA supports the S3 (STR= Suspend to RAM) power state. For more information about S3 wake events see section 9.4.1 “ACPI Configuration Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by some operating systems (S4_OS= Hibernate). Check with the operating system vendor to determine if S4 (Suspend to Disk) is supported.

This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3 and S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	<p>When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event.</p> <p>USB Hardware must be powered by standby power source.</p> <p>Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu.</p> <p>Under Windows XP add following registry entries:</p> <p>Add this key: HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\usb</p> <p>Under this key add the following value: “USBBIOSx”=DWORD:00000000</p> <p><i>Note that Windows XP disables USB wakeup from S3, so this entry has to be added to re-enable it.</i></p> <p>Configure USB keyboard/mouse to be able to wake up the system: In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check ‘Allow this device to bring the computer out of standby’.</p> <p><i>Note: When the standby state is set to S3 in the ACPI setup menu, the power management tab for USB keyboard /mouse devices only becomes available after adding the above registry entry and rebooting to allow the registry changes to take affect.</i></p>
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu.
Watchdog Power Button Event	Wakes unconditionally from S3 and S5.



Note

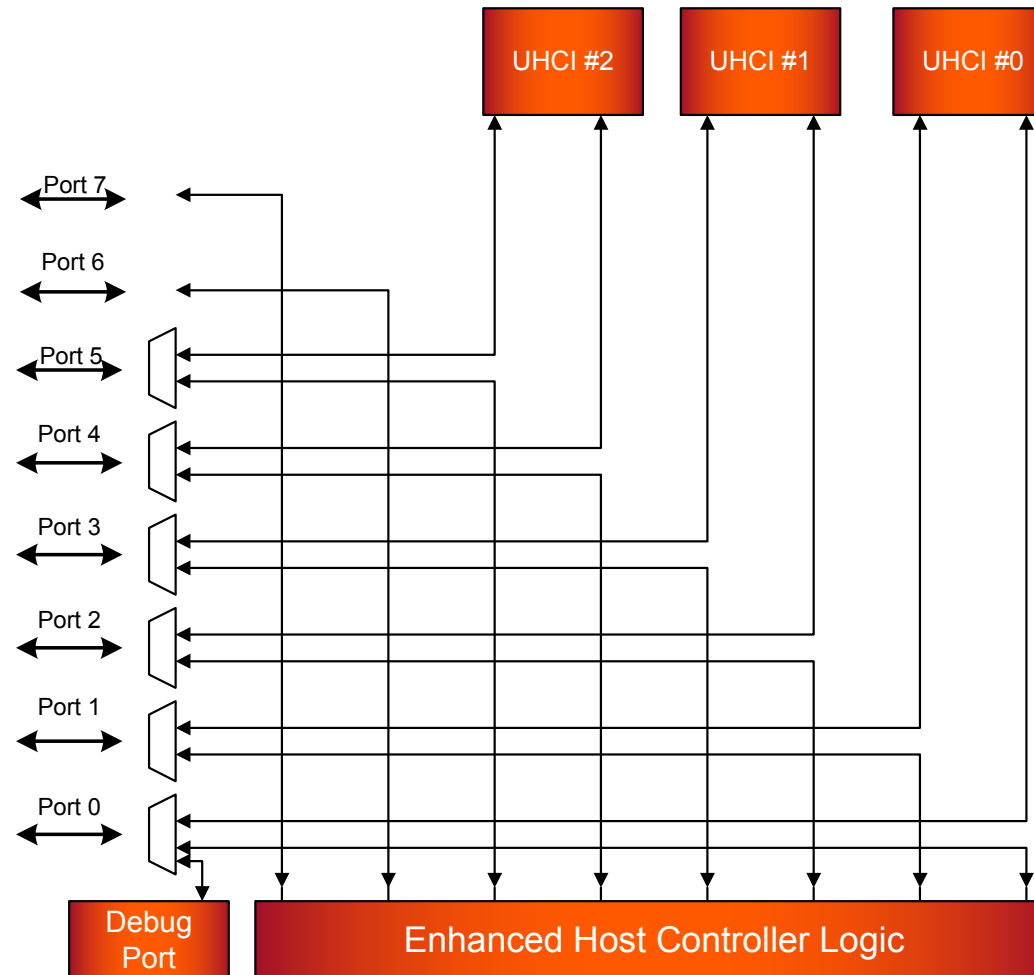
The above list has been verified using a Windows XP SP2 ACPI enabled installation.

6.5 USB Port Connections

The 8 USB ports are shared between an EHCI host controller and the 3 UHCI host controllers.

Within the EHC functionality there is a port-routing logic that executes the mixing between the two different types of host controllers (EHCI and UHCI). This means that when a USB device is connected the routing logic determines who owns the port. If the device is not USB 2.0 compliant, or if the software drivers for EHCI support are not installed, then the UHCI controller owns the ports. Ports 0-5 are capable of supporting USB 1.1 and 2.0 compliant devices. Ports 6 and 7 are not multiplexed onto a UHCI controller, so they are only capable of high-speed operation and therefore only support the connection of USB 2.0 compliant devices.

Routing Diagram



6.5.1 USB Client Controller

The Intel US15W system controller hub located on the conga-CA features a Universal Serial Bus 2.0 client controller that is configured to run on USB port 2. This means that if the USB client controller is enabled then 7 of the 8 available USB ports are host ports and 1 is a client port. This USB client controller allows the conga-CA to connect to other computer systems that utilize a USB Host interface. Once connected, the conga-CA has the ability to perform tasks supported by common USB devices. This can include, but is not limited to, such functionality as data transfer and network access.

This USB client implementation is designed to achieve maximum flexibility while maintaining hardware simplicity. Most of the behavior above the DMA and USB protocol layer is the responsibility of software. This includes Transaction level formatting, handling USB Descriptors and the implementation of defined Device Classes.

Detailed information about the USB Client Controller is beyond the scope of this document. For more information refer to the Intel® System Controller Hub US15W datasheet.

7 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type II connectors used for congatec AG modules.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.



The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip’s datasheet.

Not all the signals described in this section are available on all conga-CA variants. Use the article number of the module and refer to the options table on page 8 to determine the options available on the module.

Table 2 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.1
SATA	In compliance with Serial ATA specification, Revision 1.0a
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

7.1 A-B Connector Signal Descriptions

Table 3 Intel® High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC_RST#	A30	Intel® High Definition Audio Reset: This signal is the master hardware reset to external codec(s).	O 3.3V		AC'97 codecs are not supported
AC_SYNC	A29	Intel® High Definition Audio Sync: This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		AC'97 codecs are not supported
AC_BITCLK	A32	Intel® High Definition Audio Bit Clock Output: This signal is a 24.000MHz serial data clock generated by the Intel® High Definition Audio controller. This signal has an Intel® integrated pull-down resistor so that AC_BIT_CLK doesn't float when an Intel® High Definition Audio codec (or no codec) is connected.	O 3.3V		AC'97 codecs are not supported
AC_SDOOUT	A33	Intel® High Definition Audio Serial Data Out: This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3V		AC'97 codecs are not supported
AC_SDIN[2:0]	B28-B30	Intel® High Definition Audio Serial Data In [0]: These serial inputs are single-pumped for a bit rate of 24 MB/s. They have integrated pull-down resistors that are always enabled.	I 3.3V		AC'97 codecs are not supported HDA_SDIN1 and HDA_SDIN2 are connected together so that only two codecs can be supported.


Note

The connection of AC'97 codecs is not supported on the conga-CA.

Table 4 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment				
GBE0_MDI0+	A13	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:	I/O Analog		Twisted pair signals for external transformer.				
GBE0_MDI0-	A12								
GBE0_MDI1+	A10					1000	100	10	
GBE0_MDI1-	A9								
GBE0_MDI2+	A7					MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
GBE0_MDI2-	A6					MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
GBE0_MDI3+	A3					MDI[2]+/-	B1_DC+/-		
GBE0_MDI3-	A2					MDI[3]+/-	B1_DD+/-		
GBE0_ACT#	B2					Gigabit Ethernet Controller 0 activity indicator, active low.	OD		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB						
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	OD						
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	OD						
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.	REF		Not connected				

Table 5 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+	A19	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA0_RX-	A20				
SATA0_TX+	A16	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA0_TX-	A17				
SATA1_RX+	B19	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA1_RX-	B20				
SATA1_TX+	B16	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA1_TX-	B17				
SATA2_RX+	A25	Serial ATA channel 2, Receive Input differential pair.	I SATA		Not supported
SATA2_RX-	A26				
SATA2_TX+	A22	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Not supported
SATA2_TX-	A23				
SATA3_RX+	B25	Serial ATA channel 3, Receive Input differential pair.	I SATA		Not supported
SATA3_RX-	B26				
SATA3_TX+	B22	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Not supported
SATA3_TX-	B23				
ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	OC 3.3V		



Not all variants of the conga-CA offer the SATA interface.

Table 6 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Not supported
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		


Note

Not all variants of the conga-CA offer PCI Express links externally.

Table 7 ExpressCard Support Pins Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request.	I 3.3V	PU 10k 3.3V	EXCD1_CPPE# not supported
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3V	PU 10k 3.3V	EXCD1_PERST# not supported


Note

Carrier board ExpressCard implementations require the dedication of one USB port and one PCI Express link. Not all variants of the conga-CA offer PCI Express links externally.

Table 8 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request			Not supported
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3V	PU 8k2 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		The LPC clock output operates at 1/4th of FSB frequency. By default, the LPC clock is only active when LPC bus transfers occur. Because of this behavior, LPC clock must be routed directly to the bus device; they cannot go through a clock buffer or other circuit that could delay the signal going to the end device.

Table 9 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant only. NOT backwards compatible to USB 1.1
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant only. NOT backwards compatible to USB 1.1
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant only. NOT backwards compatible to USB 1.1
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant only. NOT backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.


Note

USB ports 6 and 7 are not multiplexed onto a UHCI controller, so they are only capable of high-speed operation and therefore only support the connection of USB 2.0 compliant devices.

Table 10 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not Supported
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not Supported
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not Supported
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		Not Supported
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		Not Supported
VGA_I2C_CK	B95	DDC clock line (I ² C port dedicated to identify VGA monitor capabilities)	I/O 5V		Not Supported
VGA_I2C_DAT	B96	DDC data line.	I/O 5V		Not Supported

Table 11 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+	A71	LVDS Channel A differential pairs	O LVDS		
LVDS_A0-	A72				
LVDS_A1+	A73				
LVDS_A1-	A74				
LVDS_A2+	A75				
LVDS_A2-	A76				
LVDS_A3+	A78				
LVDS_A3-	A79				
LVDS_A_CK+	A81	LVDS Channel A differential clock	O LVDS		
LVDS_A_CK-	A82				
LVDS_B0+	B71	LVDS Channel B differential pairs	O LVDS		Not Supported
LVDS_B0-	B72				
LVDS_B1+	B73				
LVDS_B1-	B74				
LVDS_B2+	B75				
LVDS_B2-	B76				
LVDS_B3+	B77				
LVDS_B3-	B78				
LVDS_B_CK+	B81	LVDS Channel B differential clock	O LVDS		Not Supported
LVDS_B_CK-	B82				
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10k	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10k	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 10k 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 10k 3.3V	

Table 12 TV-Out Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TV_DAC_A	B97	TVDAC Channel A Output supports the following: Composite video: CVBS Component video: Chrominance (Pb) analog signal S-Video: not used	O Analog		Not supported
TV_DAC_B	B98	TVDAC Channel B Output supports the following: Composite video: not used Component video: Luminance (Y) analog signal. S-Video: Luminance analog signal.	O Analog		Not supported
TV_DAC_C	B99	TVDAC Channel C Output supports the following: Composite video: not used Component: Chrominance (Pr) analog signal. S-Video: Chrominance analog signal.	O Analog		Not supported

Table 13 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CLK	B33	General purpose I ² C port clock output/input	I/O 3.3V	PU 4k7 3.3V	
I2C_DAT	B34	General purpose I ² C port data I/O line	I/O 3.3V	PU 4k7 3.3V	
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		
BIOS_DISABLE#	A34	Module BIOS disable input. Pull low to disable module BIOS. Used to allow off-module BIOS implementations.	I 3.3V	PU 10k 3.3V	
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PU 10k 3.3V	
KBD_RST#	A86	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.	I	PU 10k 3.3V	
KBD_A20GATE	A87	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled low on the module.	I		Not connected

Table 14 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO[0]	A93	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V	PU 10k 3.3V	
GPO[1]	B54	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V	PU 10k 3.3V	
GPO[2]	B57	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V	PU 10k 3.3V	
GPO[3]	B63	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V	PU 10k 3.3V	
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	

Table 15 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on rising edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V		Set by resistor divider to accept 3.3V.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB	PU 10k 3.3VSB	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB	PU 10k 3.3VSB	
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB	PU 10k 3.3VSB	SUS_S4# and SUS_S5# are connected together.
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB	PU 10k 3.3VSB	SUS_S4# and SUS_S5# are connected together.
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB		Not supported
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10k 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 10k 3.3V	
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V		Not connected
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	I/O 3.3VSB	PU 2k2 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	I/O 3.3VSB	PU 2k2 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	I 3.3VSB	PU 10k 3.3VSB	

Table 16 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A97-A99 A101-A109 B101-B109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A66, A80, A90, A96, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

7.2 A-B Connector Pinout

Table 17 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4- (*)	B56	PCIE_RX4- (*)
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+ (*)	B58	PCIE_RX3+ (*)
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3- (*)	B59	PCIE_RX3- (*)
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+ (*)	B61	PCIE_RX2+ (*)
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2- (*)	B62	PCIE_RX2- (*)
A8	GBE0_LINK#	B8	LPC_DRQ0# (*)	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# (*)	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1# (*)
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+ (*)
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0- (*)
A18	SUS_S4#	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+ (*)
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1- (*)
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+ (*)

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2- (*)
A22	SATA2_TX+ (*)	B22	SATA3_TX+ (*)	A77	LVDS_VDD_EN	B77	LVDS_B3+ (*)
A23	SATA2_TX- (*)	B23	SATA3_TX- (*)	A78	LVDS_A3+	B78	LVDS_B3- (*)
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+ (*)	B25	SATA3_RX+ (*)	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX- (*)	B26	SATA3_RX- (*)	A81	LVDS_A_CK+	B81	LVDS_B_CK+ (*)
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK- (*)
A28	ATA_ACT#	B28	AC_SDIN2	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC_SYNC	B29	AC_SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC_RST#	B30	AC_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	KBD_RST#	B86	VCC_5V_SBY
A32	AC_BITCLK	B32	SPKR	A87	KBD_A20GATE (*)	B87	VCC_5V_SBY
A33	AC_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	RSVD
A34	BIOS_DISABLE#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED (*)
A35	THRMTRIP# (*)	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	RSVD	B91	VGA_GRN (*)
A37	USB6+	B37	USB7+	A92	RSVD	B92	VGA_BLU (*)
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC (*)
A39	USB4-	B39	USB5-	A94	RSVD	B94	VGA_VSYNC (*)
A40	USB4+	B40	USB5+	A95	RSVD	B95	VGA_I2C_CK (*)
A41	GND (FIXED)	B41	GND (FIXED)	A96	GND	B96	VGA_I2C_DAT (*)
A42	USB2-	B42	USB3-	A97	VCC_12V	B97	TV_DAC_A (*)
A43	USB2+	B43	USB3+	A98	VCC_12V	B98	TV_DAC_B (*)
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	VCC_12V	B99	TV_DAC_C (*)
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	VCC_12V	B101	VCC_12V
A47	VCC_RTC	B47	EXCD1_PERST# (*)	A102	VCC_12V	B102	VCC_12V
A48	EXCD0_PERST#	B48	EXCD1_CPPE# (*)	A103	VCC_12V	B103	VCC_12V
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+ (*)	B52	PCIE_RX5+ (*)	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5- (*)	B53	PCIE_RX5- (*)	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+ (*)	B55	PCIE_RX4+ (*)	A110	GND (FIXED)	B110	GND (FIXED)


Note

The signals marked with an asterisk symbol (*) are not supported on the conga-CA.

7.3 C-D Connector Signal Descriptions

Table 18 PCI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCI_AD[0, 2, 4, 6, 8, 10, 12] PCI_AD[1, 3, 5, 7] PCI_AD[9, 11, 13, 15] PCI_AD14 PCI_AD[16, 18, 20, 22] PCI_AD[17, 19] PCI_AD[21, 23] PCI_AD[24, 26, 28, 30] PCI_AD[25, 27, 29, 31]	C24- C30 D22- D25 D27- D30 C32 D37- D40 C39-C40 C42-C43 D42- D45 C45- C48	PCI bus multiplexed address and data lines	I/O 3.3V		
PCI_C/BE0# PCI_C/BE1# PCI_C/BE2# PCI_C/BE3#	D26 C33 C38 C44	PCI bus byte enable lines, active low	I/O 3.3V		
PCI_DEVSEL#	C36	PCI bus Device Select, active low.	I/O 3.3V	PU 10k 3.3V	
PCI_FRAME#	D36	PCI bus Frame control line, active low.	I/O 3.3V	PU 10k 3.3V	
PCI_IRDY#	C37	PCI bus Initiator Ready control line, active low.	I/O 3.3V	PU 10k 3.3V	
PCI_TRDY#	D35	PCI bus Target Ready control line, active low.	I/O 3.3V	PU 10k 3.3V	
PCI_STOP#	D34	PCI bus STOP control line, active low, driven by cycle initiator.	I/O 3.3V	PU 10k 3.3V	
PCI_PAR	D32	PCI bus parity	I/O 3.3V		
PCI_PERR#	C34	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.	I/O 3.3V	PU 10k 3.3V	
PCI_REQ0# PCI_REQ1# PCI_REQ2# PCI_REQ3#	C22 C19 C17 D20	PCI bus master request input lines, active low.	I 3.3V	PU 10k 3.3V	
PCI_GNT0# PCI_GNT1# PCI_GNT2# PCI_GNT3#	C20 C18 C16 D19	PCI bus master grant output lines, active low.	O 3.3V		
PCI_RESET#	C23	PCI Reset output, active low.	O 3.3V		
PCI_LOCK#	C35	PCI Lock control line, active low.	I/O 3.3V	PU 10k 3.3V	
PCI_SERR#	D33	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition.	I/O 3.3V	PU 10k 3.3V	
PCI_PME#	C15	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.	I 3.3VSB	PU 10k 3.3VSB	

Signal	Pin #	Description	I/O	PU/PD	Comment
PCI_CLKRUN#	D48	Bidirectional pin used to support PCI clock run protocol for mobile systems.	I/O 3.3V	PU 8k2 3.3V	
PCI_IRQA#	C49	PCI interrupt request lines.	I 3.3V	PU 10k 3.3V	
PCI_IRQB#	C50				
PCI_IRQC#	D46				
PCI_IRQD#	D47				
PCI_CLK	D50	PCI 33MHz clock output.	O 3.3V		
PCI_M66EN	D49	Module input signal indicates whether an off-module PCI device is capable of 66MHz operation. Pulled to GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66MHz operation. If the module is not capable of supporting 66MHz PCI operation, this input may be a no-connect on the module. If the module is capable of supporting 66MHz PCI operation, and if this input is held low by the Carrier Board, the module PCI interface shall operate at 33MHz.	I		Not connected


Note

The PCI interface is specified to be +5V tolerant, with +3.3V signaling.

Table 19 IDE Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
IDE_D0	D7	Bidirectional data to / from IDE device.	I/O 3.3V		
IDE_D1	C10				
IDE_D2	C8				
IDE_D3	C4				
IDE_D4	D6				
IDE_D5	D2				
IDE_D6	C3				
IDE_D7	C2				
IDE_D8	C6				
IDE_D9	C7				
IDE_D10	D3				
IDE_D11	D4				
IDE_D12	D5				
IDE_D13	C9				
IDE_D14	C12				
IDE_D15	C5				
IDE_A[0.2]	D13-D15	Address lines to IDE device.	O 3.3V		
IDE_IOW#	D9	I/O write line to IDE device. Data latched on trailing (rising) edge.	O 3.3V		
IDE_IOR#	C14	I/O read line to IDE device.	O 3.3V		
IDE_REQ	D8	IDE Device DMA Request. It is asserted by the IDE device to request a data transfer.	I 3.3V		
IDE_ACK#	D10	IDE Device DMA Acknowledge.	O 3.3V		
IDE_CS1#	D16	IDE Device Chip Select for 1F0h to 1FFh range.	O 3.3V		
IDE_CS3#	D17	IDE Device Chip Select for 3F0h to 3FFh range.	O 3.3V		
IDE_IORDY	C13	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.	I 3.3V	PU 4k7 3.3V	
IDE_RESET#	D18	Reset output to IDE device, active low.	O 3.3V		
IDE_IRQ	D12	Interrupt request from IDE device.	I 3.3V	PU 8k2 3.3V	
IDE_CBLID#	D77	Input from off-module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 and 133 modes.	I 3.3V	PD 10k	

Table 20 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs. Some of these lines are multiplexed with SDVO lines. <i>Note: Can also be used as PCI Express Receive Input differential pairs 16 through 31 known as PCIE_RX[16-31] + and -.</i>	I PCIE		Not supported
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

PEG_TX0+	D52	PCI Express Graphics Transmit Output differential pairs. Some of these lines are multiplexed with SDVO lines. <i>Note: Can also be used as PCI Express Transmit Output differential pairs 16 through 31 known as PCIE_TX[16-31] + and -.</i>	O PCIE		Not supported
PEG_TX0-	D53				
PEG_TX1+	D55				
PEG_TX1-	D56				
PEG_TX2+	D58				
PEG_TX2-	D57				
PEG_TX3+	D61				
PEG_TX3-	D62				
PEG_TX4+	D65				
PEG_TX4-	D66				
PEG_TX5+	D68				
PEG_TX5-	D69				
PEG_TX6+	D71				
PEG_TX6-	D72				
PEG_TX7+	D74				
PEG_TX7-	D75				
PEG_TX8+	D78				
PEG_TX8-	D79				
PEG_TX9+	D81				
PEG_TX9-	D82				
PEG_TX10+	D85				
PEG_TX10-	D86				
PEG_TX11+	D88				
PEG_TX11-	D89				
PEG_TX12+	D91				
PEG_TX12-	D92				
PEG_TX13+	D94				
PEG_TX13-	D95				
PEG_TX14+	D98				
PEG_TX14-	D99				
PEG_TX15+	D101				
PEG_TX15-	D102				
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order. Be aware that the SDVO lines that share this interface do not necessarily reverse order if this strap is low.	I 1.05V		Not supported
PEG_ENABLE#	D97	Strap to enable PCI Express x16 external graphics interface. Pull low to disable internal graphics and enable the x16 interface.	I 3.3V		Not supported

Table 21 SDVO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDVOB_RED+	D52	Serial Digital Video B red output differential pair. Multiplexed with PEG_TX[0]+ and PEG_TX[0]- pair.	O PCIE		
SDVOB_RED-	D53				
SDVOB_GRN+	D55	Serial Digital Video B green output differential pair. Multiplexed with PEG_TX[1]+ and PEG_TX[1]-.	O PCIE		
SDVOB_GRN-	D56				
SDVOB_BLU+	D58	Serial Digital Video B blue output differential pair. Multiplexed with PEG_TX[2]+ and PEG_TX[2]-.	O PCIE		
SDVOB_BLU-	D59				
SDVOB_CK+	D61	Serial Digital Video B clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]-.	O PCIE		
SDVOB_CK-	D62				
SDVOB_INT+	C55	Serial Digital Video B interrupt input differential pair. Multiplexed with PEG_RX[1]+ and PEG_RX[1]-.	I PCIE		
SDVOB_INT-	C56				
SDVOC_RED+	D65	Serial Digital Video C red output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]-.	O PCIE		Not supported
SDVOC_RED-	D66				
SDVOC_GRN+	D68	Serial Digital Video C green output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]-.	O PCIE		Not supported
SDVOC_GRN-	D69				
SDVOC_BLU+	D71	Serial Digital Video C blue output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]-.	O PCIE		Not supported
SDVOC_BLU-	D72				
SDVOC_CK+	D74	Serial Digital Video C clock output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]-.	O PCIE		Not supported
SDVOC_CK-	D75				
SDVOC_INT+	C68	Serial Digital Video C interrupt input differential pair. Multiplexed with PEG_RX[5]+ and PEG_RX[5]-.	I PCIE		Not supported
SDVOC_INT-	C69				
SDVO_TVCLKIN+	C52	Serial Digital Video TVOUT synchronization clock input differential pair. Multiplexed with PEG_RX[0]+ and PEG_RX[0]-.	I PCIE		
SDVO_TVCLKIN-	C53				
SDVO_FLDSTALL+	C58	Serial Digital Video Field Stall input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]-.	I PCIE		
SDVO_FLDSTALL-	C59				
SDVO_I2C_CLK (SDVO_CLK)	D73	SDVO I ² C clock line to set up SDVO peripherals.	O 3.3V		
SDVO_I2C_DAT (SDVO_DATA)	C73	SDVO I ² C data line to set up SDVO peripherals.	I/O OD 3.3V		

Table 22 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE0#	C54	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pinout Type 1 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 (no IDE) NC GND NC Pinout Type 4 (no PCI) NC GND GND Pinout Type 5 (no IDE, no PCI)	PDS	TYPE[0:2]# signals are available on all modules following the Type 2-5 Pinout standard. The conga-CA is based on the COM Express Type 2 pinout therefore these pins are not connected.
TYPE1#	C57			
TYPE2#	D57			
		The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.		

Table 23 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
GND	C1, C11, C21, C31, C41, C51, C60, C70, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D11, D21, D31, D41, D51, D60, D67, D70, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

Table 24 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT	C67	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD		
FAN_TACHOIN	C77	Fan tachometer input.	I OD		Requires a fan with a two pulse output.
PP_TPM	C83	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V		Trusted Platform Module chip is optional.

7.4 C-D Connector Pinout

Table 25 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1- (*)	D56	PEG_TX1- (*)
C2	IDE_D7	D2	IDE_D5	C57	TYPE1#	D57	TYPE2#
C3	IDE_D6	D3	IDE_D10	C58	PEG_RX2+ (*)	D58	PEG_TX2+ (*)
C4	IDE_D3	D4	IDE_D11	C59	PEG_RX2- (*)	D59	PEG_TX2- (*)
C5	IDE_D15	D5	IDE_D12	C60	GND (FIXED)	D60	GND (FIXED)
C6	IDE_D8	D6	IDE_D4	C61	PEG_RX3+ (*)	D61	PEG_TX3+ (*)
C7	IDE_D9	D7	IDE_D0	C62	PEG_RX3- (*)	D62	PEG_TX3- (*)
C8	IDE_D2	D8	IDE_REQ	C63	RSVD	D63	RSVD
C9	IDE_D13	D9	IDE_IOW#	C64	RSVD	D64	RSVD
C10	IDE_D1	D10	IDE_ACK#	C65	PEG_RX4+ (*)	D65	PEG_TX4+ (*)
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4- (*)	D66	PEG_TX4- (*)
C12	IDE_D14	D12	IDE_IRQ	C67	RSVD	D67	GND
C13	IDE_IORDY	D13	IDE_A0	C68	PEG_RX5+ (*)	D68	PEG_TX5+ (*)
C14	IDE_IOR#	D14	IDE_A1	C69	PEG_RX5- (*)	D69	PEG_TX5- (*)
C15	PCI_PME#	D15	IDE_A2	C70	GND (FIXED)	D70	GND (FIXED)
C16	PCI_GNT2#	D16	IDE_CS1#	C71	PEG_RX6+ (*)	D71	PEG_TX6+ (*)
C17	PCI_REQ2#	D17	IDE_CS3#	C72	PEG_RX6- (*)	D72	PEG_TX6- (*)
C18	PCI_GNT1#	D18	IDE_RESET#	C73	SDVO_DATA	D73	SVDO_CLK
C19	PCI_REQ1#	D19	PCI_GNT3#	C74	PEG_RX7+ (*)	D74	PEG_TX7+ (*)
C20	PCI_GNT0#	D20	PCI_REQ3#	C75	PEG_RX7- (*)	D75	PEG_TX7- (*)
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCI_REQ0#	D22	PCI_AD1	C77	RSVD	D77	IDE_CBLID#
C23	PCI_RESET#	D23	PCI_AD3	C78	PEG_RX8+ (*)	D78	PEG_TX8+ (*)
C24	PCI_AD0	D24	PCI_AD5	C79	PEG_RX8- (*)	D79	PEG_TX8- (*)
C25	PCI_AD2	D25	PCI_AD7	C80	GND (FIXED)	D80	GND (FIXED)
C26	PCI_AD4	D26	PCI_C/BE0#	C81	PEG_RX9+ (*)	D81	PEG_TX9+ (*)
C27	PCI_AD6	D27	PCI_AD9	C82	PEG_RX9- (*)	D82	PEG_TX9- (*)
C28	PCI_AD8	D28	PCI_AD11	C83	RSVD	D83	RSVD
C29	PCI_AD10	D29	PCI_AD13	C84	GND	D84	GND
C30	PCI_AD12	D30	PCI_AD15	C85	PEG_RX10+ (*)	D85	PEG_TX10+ (*)
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- (*)	D86	PEG_TX10- (*)
C32	PCI_AD14	D32	PCI_PAR	C87	GND	D87	GND
C33	PCI_C/BE1#	D33	PCI_SERR#	C88	PEG_RX11+ (*)	D88	PEG_TX11+ (*)
C34	PCI_PERR#	D34	PCI_STOP#	C89	PEG_RX11- (*)	D89	PEG_TX11- (*)
C35	PCI_LOCK#	D35	PCI_TRDY#	C90	GND (FIXED)	D90	GND (FIXED)
C36	PCI_DEVSEL#	D36	PCI_FRAME#	C91	PEG_RX12+ (*)	D91	PEG_TX12+ (*)
C37	PCI_IRDY#	D37	PCI_AD16	C92	PEG_RX12- (*)	D92	PEG_TX12- (*)

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C38	PCI_C/BE2#	D38	PCI_AD18	C93	GND	D93	GND
C39	PCI_AD17	D39	PCI_AD20	C94	PEG_RX13+ (*)	D94	PEG_TX13+ (*)
C40	PCI_AD19	D40	PCI_AD22	C95	PEG_RX13- (*)	D95	PEG_TX13- (*)
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	PCI_AD21	D42	PCI_AD24	C97	RSVD	D97	PEG_ENABLE# (*)
C43	PCI_AD23	D43	PCI_AD26	C98	PEG_RX14+ (*)	D98	PEG_TX14+ (*)
C44	PCI_C/BE3#	D44	PCI_AD28	C99	PEG_RX14- (*)	D99	PEG_TX14- (*)
C45	PCI_AD25	D45	PCI_AD30	C100	GND (FIXED)	D100	GND (FIXED)
C46	PCI_AD27	D46	PCI_IRQC#	C101	PEG_RX15+ (*)	D101	PEG_TX15+ (*)
C47	PCI_AD29	D47	PCI_IRQD#	C102	PEG_RX15- (*)	D102	PEG_TX15- (*)
C48	PCI_AD31	D48	PCI_CLKRUN#	C103	GND	D103	GND
C49	PCI_IRQA#	D49	PCI_M66EN (*)	C104	VCC_12V	D104	VCC_12V
C50	PCI_IRQB#	D50	PCI_CLK	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+ (*)	D52	PEG_TX0+ (*)	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0- (*)	D53	PEG_TX0- (*)	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV# (*)	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+ (*)	D55	PEG_TX1+ (*)	C110	GND (FIXED)	D110	GND (FIXED)



The signals marked with an asterisk symbol () are not supported on the conga-CA.*

8 System Resources

8.1 System Memory Map

Table 26 Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(TOM- FB) – TOM	N.A.	1, 4 or 8MB	VGA frame buffer *
(TOM – FB – TSEG) – (TOM - FB)	N.A.	1MB	TSEG**
(TOM - FB – TSEG – BIOS) - (TOM – FB – TSEG)	N.A.	448kB or 192kB	Used by BIOS firmware with ACPI enabled respectively disabled**
1024kB – (TOM - FB – TSEG – BIOS)	100000 – N.A	N.A.	Extended memory
869kB – 1024kB	E0000 - FFFFF	128kB	Runtime BIOS
832kB – 869kB	D0000 - DFFFF	64kB	Upper memory
640kB – 832kB	A0000 - CFFFF	192kB	Video memory and BIOS
639kB – 640kB	9FC00 - 9FFFF	1kB	EBDA=Extended BIOS Data Area
0 – 639kB	00000 - 9FC00	512kB	Conventional memory



Note

T.O.M. = Top of memory = max. DRAM installed

FB = VGA frame buffer

TSEG = Designated as internally used by system BIOS for SMI handling.

** VGA frame buffer can be reduced to 1MB in setup.*

*** Only if ACPI Aware OS is set to YES in setup.*

8.2 I/O Address Assignment

The I/O address assignment of the conga-CA module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

Table 27 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
0100 - 010F	16 bytes	No	congatec System Control
01F0 - 01F7	8 bytes	No	Primary IDE channels
03B0 - 03DF	16 bytes	No	Video system
03F6	1 byte	No	Primary IDE channel command port
03F7	1 byte	No	Primary IDE channel status port
0400 - 04BF	192 bytes	No	Motherboard resources
04D0 - 04D1	2 bytes	No	Motherboard resources
0900 - 09FF	256 bytes	No	Motherboard resources
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
0D00 - FFFF		See note	PCI / PCI Express bus

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

8.3 Interrupt Request (IRQ) Lines

Table 28 IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Can be used for:
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		LPC bus via SERIRQ or PCI INTx
4	Yes		LPC bus via SERIRQ or PCI INTx
5	Yes		LPC bus via SERIRQ or PCI INTx
6	Yes		LPC bus via SERIRQ or PCI INTx
7	Yes		LPC bus via SERIRQ or PCI INTx
8	No	Real-time Clock	Not applicable
9	Note 2	SCI / Generic	LPC bus via SERIRQ or PCI INTx
10	Yes		LPC bus via SERIRQ or PCI INTx
11	Yes		LPC bus via SERIRQ or PCI INTx
12	Yes		LPC bus via SERIRQ or PCI INTx
13	No	Math processor	Not applicable
14	Note 1	IDE Controller 0 (IDE0) / Generic	LPC bus via SERIRQ or PCI INTx
15	Yes		LPC bus via SERIRQ or PCI INTx

In PIC mode, the PCI bus interrupt lines can be routed to any free IRQ.



Note

1. If the ATA/IDE controller is set to disabled, IRQ14 is free for PCI/LPC bus.
2. In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCI interrupt line.

Table 29 IRQ Lines in APIC mode

IRQ#	Available	Typical Interrupt Source	Can be used for:
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		LPC bus via SERIRQ
4	Yes		LPC bus via SERIRQ
5	Yes		LPC bus via SERIRQ
6	Yes		LPC bus via SERIRQ
7	Yes		LPC bus via SERIRQ
8	No	Real-time Clock	Not applicable
9	Note 2	Generic	LPC bus via SERIRQ, option for SCI
10	Yes		LPC bus via SERIRQ
11	Yes		LPC bus via SERIRQ
12	Yes		LPC bus via SERIRQ
13	No	Math processor	Not applicable
14	Note 1	IDE Controller 0 (IDE0) / Generic	LPC bus via SERIRQ
15	Yes		LPC bus via SERIRQ
16	Yes		Integrated VGA controller, PCI Express Root Port 1, PCIe slot 1 or PCIe to PCI bridge, PCI Bus INTA
17	Yes		PCI Express Root Port 2, PCIe slot 2 or onboard Gigabit LAN controller, UHCI Host Controller 1, PCI Bus INTB
18	Yes		USB client controller, SDIO Ports 0, 1, 2, PCI Bus INTC
19	Yes		HDA controller, Serial ATA controller, PCI Bus INTD
20	Note 2		Option for SCI, UHCI Host Controller 0
21	No		UHCI Host Controller 1
22	No		UHCI Host Controller 2
23	No		EHCI Host Controller


Note

1. If the ATA/IDE controller is set to disabled in BIOS setup, IRQ14 is available via SERIRQ.
2. In ACPI and APIC mode, IRQ9 or IRQ 20 is used for the SCI (System Control Interrupt).

8.4 PCI Configuration Space Map

Table 30 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	02h	00h	Internal	IGD (Intergrated graphics)
00h	1Ah	00h	Internal	USB 2.0
00h	1Bh	00h	Internal	Intel High Definition Audio Controller (Azalia)
00h (see Note)	1Ch	00h	Internal	PCI Express Root Port 1
00h (see Note)	1Ch	01h	Internal	PCI Express Root Port 2
00h	1Dh	00h	Internal	UHCI Host Controller 0
00h	1Dh	01h	Internal	UHCI Host Controller 1
00h	1Dh	02h	Internal	UHCI Host Controller 2
00h	1Dh	07h	Internal	EHCI Host Controller
00h	1Eh	00h	Internal	SDIO/MMC Port 0 (Not routed)
00h	1Eh	01h	Internal	SDIO/MMC Port 1
00h	1Eh	02h	Internal	SDIO/MMC Port 2
00h	1Fh	00h	N.A.	LPC Interface
00h	1Fh	01h	Internal	Parallel ATA Controller
01h (see Note)	00h	00h	Internal	PCI Express to PCI Bridge
02h (see Note)	04h - 07h		INTA - INTD	32bit parallel PCI Bus slots 1-4
02h (see Note)	03h	00h	INTD	SATA Controller
03h (see Note)	00h	00h	Internal	Onboard Gigabit LAN Controller

Note

The given bus numbers only apply to a conga-CA supporting PCI, Gigabit Ethernet and SATA with both PCI Express Ports being enabled in the BIOS setup.

8.5 PCI Interrupt Routing Map

Table 31 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line ¹	APIC Mode IRQ	IGD	Azalia HDA	UHCI 0	UHCI 1	UHCI 2	EHCI	USB 2.0 Client	LAN	SATA	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Slot1	PCI-EX Slot2	SDIO0	SDIO1	SDIO2
A	INTA	16	x									x		x ²	x ⁵			
B	INTB	17								x			x	x ³	x ²			
C	INTC	18							x					x ⁴	x ³	x	x	x
D	INTD	19		x							x			x ⁵	x ⁴			
E		20			x													
F		21				x												
G		22					x											
H		23						x										

Note

¹ These interrupts are available for external devices/slots via the C-D connector rows.

² Interrupt used by single function PCI Express devices (INTA).

³ Interrupt used by multifunction PCI Express devices (INTB).

⁴ Interrupt used by multifunction PCI Express devices (INTC).

⁵ Interrupt used by multifunction PCI Express devices (INTD).

8.6 PCI Bus Masters

The conga-CA variants with the PCIe to PCI bridge support 4 external PCI Bus Masters. There are no limitations in connecting bus master PCI devices.



If there are two devices connected to the same PCI REQ/GNT pair and they are transferring data at the same time then the latency time of these shared PCI devices can not be guaranteed.

8.7 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

8.8 SM Bus

System Management (SM) bus signals are connected to the Intel® I/O System Controller Hub US15W and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

9 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.



The BIOS Setup Program described in the following section depicts the BIOS that will be used for mass production conga-CA modules and does not necessarily describe the BIOS Setup Program found on early engineering samples currently being shipped.

9.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the key during POST.

9.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used a message will be displayed during POST stating that the “Boot Selection Popup menu has been selected” and the menu itself will be displayed immediately after POST thereby allowing the operator to choose the boot device to be used.

9.1.2 Manufacturer Default Settings

Pressing the <End> key repeatedly, immediately after power is initiated will result in the manufacturer default settings being loaded for that boot sequence and only that boot sequence. This is helpful when a previous BIOS setting is no longer desired. If you want to change the BIOS settings, or save the manufacturer default settings, then you must enter the BIOS setup program and use the ‘Save and Exit’ function. This feature is enabled by default and only works with a PS/2 keyboard, it is not available when using a USB keyboard. See setup node in the “BIOS Setup Description” section 9.6.1 “Security Settings”.

9.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:



Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

Main	Advanced	Boot	Security	Power	Exit
------	----------	------	----------	-------	------

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2/F3	Change Colors of setup screen.
F7	Discard Changes.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

9.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
System Time	Hour:Minute:Second	Specifies the current system time. <i>Note: The time is in 24-hour format.</i>
System Date	Day of week, month/day/year	Specifies the current system date. <i>Note: The date is in month-day-year format.</i>
BIOS ID	no option	Displays the BIOS ID.
Processor	no option	Displays the processor type.
CPU Frequency	no option	Displays CPU frequency.
System Memory	no option	Displays the total amount of system memory.
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
Running Time	no option	Displays the time the board is running [in hours max. 65535].

9.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Power	Exit
	ACPI Configuration				
	PCI Configuration				
	Graphics Configuration				
	CPU Configuration				
	Chipset Configuration				
	I/O Interface Configuration				
	IDE Configuration				
	USB Configuration				
	Keyboard/Mouse Configuration				
	Hardware Health Configuration				
	Watchdog Configuration				

9.4.1 ACPI Configuration Submenu

Feature	Options	Description
ACPI Aware O/S	No Yes	Set this value to allow the system to utilize the Intel ACPI (Advanced Configuration and Power Interface). Set to <i>NO</i> for non ACPI aware operating system like DOS and Windows NT. Set to <i>YES</i> if your OS complies with the ACPI specification (e.g. Windows 2000, XP)
ACPI Version Features	ACPI v1.0 ACPI v2.0 ACPI v3.0	ACPI version supported by the BIOS ACPI code and tables.
System Off Mode	G3/Mech Off S5/Soft Off	Select the actual power down mode when the system performs a shutdown with a congatec battery system connected. <i>Note: This node is only visible when the system is connected to a congatec battery system.</i>
ACPI APIC support	Enabled Disabled	Set to enable to include the APIC support table to ACPI.
Suspend mode	S3 (STR)	Select the state used for ACPI system suspend. <i>Note: Only S3 is supported.</i>
USB Device Wakeup From S3/S4	Disabled Enabled	Enable or disable USB device wakeup from S3 and S4 state.
Active Cooling Trip Point	Disabled 50, 60, 70, 80, 90°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Cooling Trip Point	Disabled 50, 60, 70, 80, 90 °C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.
Critical Trip Point	Disabled, 80, 85, 90, 95, 100, 105 , 110°C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Watchdog ACPI Event	Shutdown Restart	Select the event that is initiated by the watchdog ACPI event. When the watchdog times out a critical but orderly OS shutdown or restart can be performed (see note below).



Note

In ACPI mode it is not possible for a “Watchdog ACPI Event” handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

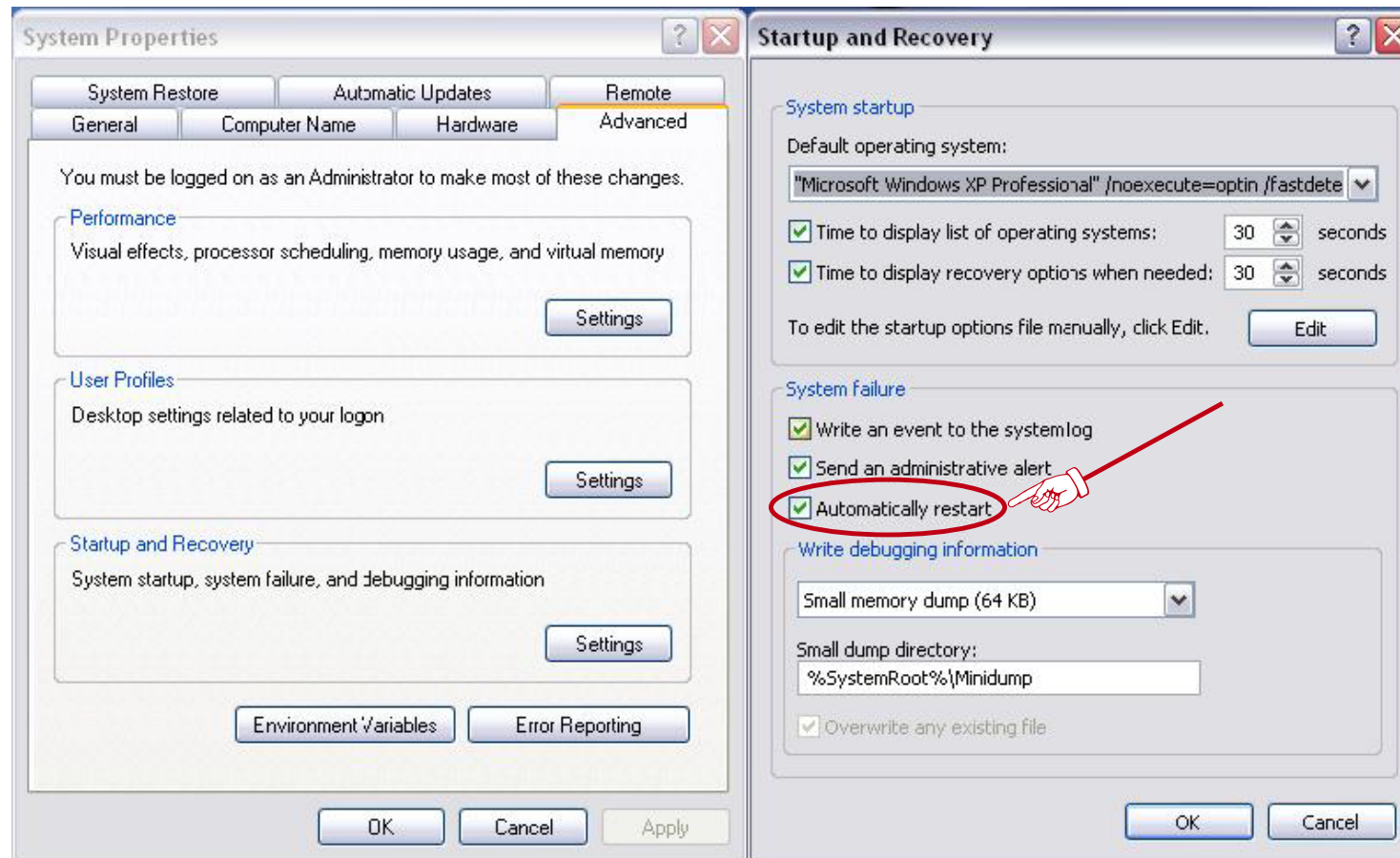
For Restart: An ACPI fatal error is reported to the OS.

It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP/2000 there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very brief blue-screen the system will restart.

You can enable this setting buy going to the “System Properties” dialog box and choosing the “Advanced” tab. Once there choose the “Settings” button for the “Startup and Recovery” section. This will open the “Startup and Recovery” dialog box. In this dialog box under “System failure” there are three check boxes that define what Windows will do when a fatal error has been detected. In order to ensure that the system restarts

after a 'Watchdog ACPI Event' that is set to 'Restart', you must make sure that the check box for the selection "Automatically restart" has been checked. If this option is not selected then Windows will remain at a blue-screen after a 'Watchdog ACPI Event' that has been configured for 'Restart' has been generated. Below is a Windows screen-shot showing the proper configuration.

Win XP/2000 Watchdog ACPI Event restart configuration



9.4.2 PCI Configuration Submenu

Feature	Options	Description
Plug & Play O/S	No Yes	Specifies if manual configuration is desired. Set to <i>NO</i> for operating systems that do not meet the Plug and Play specification. In this case the BIOS configures all devices in the system. Select <i>YES</i> to let the operating system configure PnP devices that are not required for booting.
PCI Latency Timer	32, 64 , 96, ... 248	This option allows you to adjust the latency timer of all devices on the PCI bus.
Allocate IRQ to PCI VGA	Yes No	Allow or restrict the BIOS from giving the VGA controller an IRQ resource.
▶ PCI IRQ Resource Exclusion	sub menu	Opens PCI IRQ Resource Exclusion sub menu.
▶ PCI Interrupt Routing	sub menu	Opens PCI Interrupt Routing sub menu.

9.4.2.1 PCI IRQ Resource Exclusion Submenu

Feature	Options	Description
IRQ xx	Available Reserved	Allow or restrict the BIOS from giving IRQ resource to PCI/PNP devices. <i>Note: Assigned IRQ resources are shaded and listed as 'Allocated'.</i>

9.4.2.2 PCI Interrupt Routing Submenu

Feature	Options	Description
PIRQ xx (devices)	Auto , 3, 4, ..., 14, 15	Select fixed IRQ for PCI interrupt line or set to <i>AUTO</i> to let the BIOS and operating system route an IRQ. <i>Note: Only those IRQs that are free are listed.</i>
1st Exclusive PCI IRQ	None , [IRQs assigned manually above]	The selected IRQ will only be assigned to the PIRQ line it has been set to manually. PIRQs set to <i>AUTO</i> will not be assigned this IRQ.
2nd Exclusive PCI IRQ	None , [IRQs assigned manually above]	The selected IRQ will only be assigned to the PIRQ line it has been set to manually. PIRQs set to <i>AUTO</i> will not be assigned this IRQ.

9.4.3 Graphics Configuration Submenu

Feature	Options	Description
Primary Video Device	IGD PCIe/IGD	Select primary video adapter to be used during boot up. IGD: Internal Graphics Device PCIe: PCI Express Graphics Device
Internal VGA Mode Select	Disabled Enabled, 1MB Enabled, 4MB Enabled, 8MB	This option allows you to disable the internal VGA controller or enable it with 1MB, 4MB or 8MB initial frame buffer size.
Graphics Aperture Size	128MB 256MB	Determines the size of the graphics memory aperture.
Boot Display Device	Auto Integrated LVDS External DVI/HDMI External TV External CRT External LVDS	Select the display device(s) used for boot up. External display devices are connected to the SDVO interface. External TV and External LVDS options are only visible if the 3 rd supported SDVO type (setup node below) is set to TV or LVDS.
Local Flat Panel Scaling	Auto Forced Scaling Disabled	Select whether and how to scale the actual video mode resolution to the local flat panel resolution.
Local Flat Panel Type	Auto VGA 1x18 (002h) VGA 1x18 (013h) WVGA 1x18 (01Bh) SVGA 1x18 (01Ah) XGA 1x18 (006h) XGA 1x24 (008h) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I ² C bus. The number in brackets specifies the congatec internal number of the respective panel data set. <i>Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.</i> VGA = 640x480 WVGA = 800x480 SVGA = 800x600 XGA = 1024x768
3 rd supported SDVO Type	Disabled TV LVDS DVI-i	Select the 3 rd supported SDVO device type. <i>Note: Analog CRT and DVI codecs are supported by default.</i>
SDVO Flat Panel Type	VGA 1x18 (002h) VGA 1x18 (013h) WVGA 1x18 (01Bh) SVGA 1x18 (01Ah) XGA 1x18 (006h) XGA 2x18 (007h) XGA 1x24 (008h) XGA 2x24 (012h) SXGA 2x24 (018h) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select the predefined LFP type for the external LVDS. Only visible if the 3 rd supported SDVO Type is set to LVDS.

Feature	Options	Description
TV Standard	VBIOS-Default NTSC PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3	Select TV standard that should be supported. TV connection type is automatically detected by the Video BIOS. Only visible if the 3 rd supported SDVO Type is set to TV.
TV Sub-Type	(Options depend on selected TV standard)	Select sub-type for selected TV standard.
Backlight Control	Auto , 0%, 25%, 50%, 75%, 100%	Select local flat panel backlight control value. If set to Auto, the BIOS tries to read the backlight brightness value from the EPI data set.
Inhibit Backlight	No Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Control	No Yes	Allow the inversion of backlight control values if required by the actual backlight hardware controller.
PWM Backlight Control	Disabled Enabled	Enable/Disable backlight PWM output of COM Express.

9.4.4 CPU Configuration Submenu

Feature	Options	Description
Processor Info Block	No option	Displays the processor manufacturer, brand, frequency, and cache sizes.
Max CPUID Value Limit	Disabled Enabled	When enabled , the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When disabled , the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Execute Disable Bit	Disabled Enabled	Enable or disable the hardware support for data execution prevention.
Hyper Threading Technology	Disabled Enabled	Enable Hyper Threading Technology for operating systems that are optimized for it.
Intel SpeedStep tech.	Disabled Enabled	Enabled: CPU speed is controlled by the operating system. Disabled: No SpeedStep, default CPU speed.
Intel C-State tech	Disabled Enabled	Enables the processor C-State support when in IDLE mode.
Enhanced C-States	Disabled Enabled	Processor IDLE is set to enhanced C-states.
C6 State	Disabled Enabled	When enabled, C6 is the lowest C-State supported.

9.4.5 Chipset Configuration Submenu

Feature	Options	Description
Serial IRQ Mode	Continuos Quiet	Selects the Serial IRQ mode.
APIC ACPI SCI IRQ	Disabled Enabled	If set to Disabled IRQ9 is used for the SCI. If set to Enabled IRQ20 is used for the SCI.
PCIE Port 0	Auto Enabled Disabled	Enable or disable PCI Express port.
PCIE Port 1	Auto Enabled Disabled	Enable or disable PCI Express port.
PCIE Base Spec Compliance	Disabled Enabled	Enable PCI Express Base Specification Compliance if you use off-board PCI Express devices (see Note below).
Active State Power Management	Disabled Enabled	Enable or disable PCI Express L0s and L1 link power states.
US15W Silicon Revision	D.2	Chipset revision
Atom Silicon Revision	C.0	Processor revision
CMC Lo-Module and Hi-Module Revision:	0D2.053x 0D2.017x	CMC Binary version number. Might change with future BIOS revisions.



Note

The conga-CA supports two x1 PCIe root ports that comply with the Mobile Graphics Low-Power Addendum to the PCI Express Base Specification versus complying fully with the PCI Express Base Specification. This is the default configuration of the chipset. Enabling the PCI Express Base Specification Compliance setup node results in the two x1 PCIe root ports being fully compliant with the PCI Express Base Specification.

9.4.6 I/O Interface Configuration Submenu

Feature	Options	Description
SDIO Controller	Enabled Disabled	N/A
HDA Controller	Auto Enabled Disabled	When set to Enabled, the HDA will be enabled no matter if a codec is present or not. When set to Auto the HDA will only be enabled if a HDA codec is present on the carrier board.
▶ SIO Winbond W83627 Configuration	sub menu	Opens submenu. <i>Note: This setup node is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.</i>
▶ SIO SMSC SCH3114 Configuration	sub menu	Opens submenu. <i>Note: This setup node is only available if an external SMSC SCH3114 Super I/O has been implemented on the carrier board.</i>



Note
 The BIOS does not initialize the HDA codec. The codec remains in default mode and must be initialized by the codec's driver.

9.4.6.1 SIO Winbond W83627 Configuration

Feature	Options	Description
Serial Port 1/2 Configuration	Disabled 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Specifies the I/O base address and IRQ of serial port 1/2.
Parallel Port Address	Disabled 378 278 3BC	Specifies the I/O base address used by the parallel port.
Parallel Port Mode	Normal Bi-directional ECP EPP ECP&EPP	Specifies the parallel port mode.
EPP Version	1.9 1.7	Specifies the EPP version.
Parallel Port DMA	DMA0 DMA1 DMA3	Specifies the DMA channel for parallel port in ECP mode.
Parallel Port IRQ	None IRQ5 IRQ7	Specifies the interrupt for the parallel port.



Note
 This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

9.4.6.2 SIO SMSC SCH3114 Configuration

Feature	Options	Description
Serial Port 1/2/3/4 Address	Disabled 3F8 2F8 3E8 2E8	Specifies the I/O base address of serial port 1/2/3/4.
Serial Port 1/2/3/4 IRQ	3 4 10 11	Specifies the interrupt of serial port 1/2/3/4.
Serial Port 2 Mode	Normal IrDA ASK IR	Select serial port 2 mode.
IR Duplex Mode	Full Duplex Half Duplex	Serial port 2 infrared duplex mode.
Receiver Polarity	High Low	Serial port 2 infrared receiver polarity.
Xmitter Polarity	High Low	Serial port 2 infrared transmitter polarity.


Note

This setup menu is only available if an external SMSC SCH3114 Super I/O has been implemented on the carrier board.

9.4.7 IDE Configuration Submenu

Feature	Options	Description
IDE Controller	Disabled Enabled	Enables/Disables the integrated parallel ATA controller.
▶ Primary IDE Master	sub menu	Reports type of connected IDE device.
▶ Primary IDE Slave	sub menu	Reports type of connected IDE device.
Hard Disk Write Protect	Disabled Enabled	If enabled, protects the hard drive from being erased. Disabled allows the hard drive to be used normally. Read, write and erase functions can be performed to the disk.
IDE Detect Time Out (s)	0, 5, 10, ... 30, 35	Set this option to stop the BIOS from searching for IDE devices within the specified number of seconds. Basically, this allows you to fine-tune the settings to allow for faster boot times. Adjust this setting until a suitable timing can be found that will allow for all IDE disk drives that are attached to be detected.
ATA(Pi) 80Pin Cable Detection	Host&Device Host Device	Select the mechanism for detecting 80Pin ATA(Pi) cable. <i>Note: The use of an 80-conductor ATA cable is mandatory for running UDMA66 and faster hard disk drives. The standard 40-conductor ATA cable cannot handle the higher speeds.</i>

Note

Not all disk drives function properly when connected as a Slave drive without a Master drive present. It is strongly recommend that any disk drive that is intended to be used as a Slave drive, without a Master drive present, be tested thoroughly to ensure proper functionality.

9.4.7.1 Primary/Secondary IDE Master/Slave Submenu

Feature	Options	Description
Device	Hard Disk ATAPI CDROM	Displays the type of drive detected. The 'grayed-out' items below are the IDE disk drive parameters taken from the firmware of the IDE disk
Vendor	no option	Manufacturer of the device.
Size	no option	Total size of the device.
LBA Mode	supported not supported	Shows whether the device supports Logical Block Addressing.
Block Mode	number of sectors	Block mode boosts IDE performance by increasing the amount of data transferred. Only 512 byte of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 kB per interrupt.
PIO Mode	0, 1, 2, 3, 4	IDE PIO mode programs timing cycles between the IDE drive and the programmable IDE controller. If PIO mode increases, the cycle time decreases.
Async DMA	no option	This indicates the highest Asynchronous DMA Mode that is supported.
Ultra DMA	no option	This indicates the highest Synchronous DMA Mode that is supported.
S.M.A.R.T	no option	Self-Monitoring Analysis and Reporting Technology protocol used by IDE drives of some manufacturers to predict drive failures.
Type	Not Installed Auto CD/DVD ARMD	Sets the type of device that the BIOS attempts to boot from after the POST has completed. <i>Not Installed</i> prevents the BIOS from searching for an IDE disk. <i>Auto</i> allows the BIOS to auto detect the IDE disk drive type. <i>CD/DVD</i> specifies that an IDE CD/DVD drive is attached. The BIOS will not attempt to search for other types of IDE disk drives. <i>ARMD</i> specifies an ATAPI Removable Media Device. This includes, but is not limited to ZIP and LS-120.
LBA/Large Mode	Disabled Auto	Set to <i>AUTO</i> to let the BIOS auto detect LBA mode control. Set to Disabled to prevent the BIOS from using LBA mode.
Block (Multi-Sector Transfer)	Disabled Auto	Set to <i>AUTO</i> to let the BIOS auto detect device support for multi sector transfer. The data transfer to and from the device will occur multiple (the number of sectors, see above) sectors at a time. Set to Disabled to prevent the BIOS from using block mode. The data transfer to and from the device will occur one sector at a time.
PIO Mode	Auto 0, 1, 2, 3, 4	Set to <i>AUTO</i> to let the BIOS auto detect the supported PIO mode.
DMA Mode	Auto Disabled SWDMA 1, 2 MWDMA0, 1, 2 UDMA0, 1, 2, 3, 4, 5, 6	Set to <i>AUTO</i> to let the BIOS auto detect the supported DMA mode. SWDMA = Single Word DMA MWDMA = Multi Word DMA UDMA = Ultra DMA
S.M.A.R.T	Auto Disabled Enabled	Set to <i>AUTO</i> to let the BIOS auto detect hard disk drive support. Set to <i>Disabled</i> to prevent the BIOS from using SMART feature. Set to <i>Enabled</i> to allow the BIOS to use SMART feature on supported hard disk drives.
32Bit Data Transfer	Disabled Enabled	Enable/Disable 32-bit data transfers on supported hard disk drives.
ARMD Emulation Type	Auto Floppy Hard disk drive	ARMD is a device that uses removable media, such as the LS120, MO (Magneto-optical), or Iomega Zip drives. If you want to boot from media on ARMD, it is required that you emulate boot up from a floppy or hard disk drive. This is essentially necessary when trying to boot to DOS. You can select the type of emulation used if you are booting such a device.

9.4.8 USB Configuration Submenu

Feature	Options	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports 6 USB Ports	Disable US15W USB host controllers. Enable UHCI host controller 0. Enable UHCI host controller 0 + 1. Enable UHCI host controller 0 + 1 + 2.
USB 2.0 Controller	Enabled Disabled	Enable the US15W USB 2.0 (EHCI) host controller.
USB Client Controller	Enabled Disabled	conga-CA offers USB client support on USB port 1. See section 6.5.1 “USB Client Controller” of this document for more details.
Legacy USB Support	Disabled Enabled Auto	Legacy USB Support refers to the USB keyboard, USB mouse and USB mass storage device support. If this option is <i>Disabled</i> , any attached USB device will not become available until a USB compatible operating system is booted. However, legacy support for USB keyboard will be present during POST. When this option is <i>Enabled</i> , those USB devices can control the system even when there is no USB driver loaded. <i>AUTO</i> disables legacy support if no USB devices are connected.
USB Keyboard Legacy Support	Disabled Enabled	Enable/Disable USB keyboard legacy support. <i>NOTE: This option has to be used with caution. If the system is equipped with USB keyboard only then the user cannot enter setup to enable the option back</i>
USB Mouse Legacy Support	Disabled Enabled	Enable/Disable USB mouse legacy support.
USB Storage Device Support	Disabled Enabled	Enable/Disable USB mass storage device support.
USB 2.0 Controller Mode	FullSpeed HiSpeed	Configures the USB 2.0 host controller in HiSpeed (480Mbps) or Full Speed (12Mbps).
BIOS EHCI Hand-Off	Disabled Enabled	Enable workaround for OSes without EHCI hand-off support.
USB Beep Message	Disabled Enabled	Enable/Disable the beep during USB device enumeration.
USB Stick Default Emulation	Auto Hard Disk	Select default USB stick emulation type. Auto selects floppy or hard disk emulation based on the storage size of the USB stick, but the emulation type can be manually reconfigured for each device using the Mass Storage Device Configuration sub menu.
USB Mass Storage Reset Delay	10 Sec 20 Sec 30 Sec 40 Sec	Number of seconds the legacy USB support BIOS routine waits for the USB mass storage device after the start unit command.
► USB Mass Storage Device Configuration	sub menu	Opens sub menu.

9.4.8.1 USB Mass Storage Device Configuration Submenu

Feature	Options	Description
Emulation Type	Auto	Every USB MSD that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device.
	Floppy	<i>Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.</i>
	Forced FDD	Select <i>AUTO</i> to let the BIOS auto detect the current formatted media.
	Hard Disk	If Floppy is selected then the device will be emulated as a floppy drive.
	CDROM	<i>Forced FDD</i> allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. <i>Hard Disk</i> allows the device to be emulated as hard disk. <i>CDROM</i> assumes the CD.ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

9.4.9 Keyboard/Mouse Configuration Submenu

Feature	Options	Description
Bootup Num-Lock	Off	Specifies the power-on state of the Num-lock feature on the numeric keypad of the keyboard.
	On	
Typematic Rate	Slow	Specifies the rate at which the computer repeats a key that is held down. <i>Slow</i> sets a rate of under 8 times per second. <i>Fast</i> sets a rate of over 20 times per second.
	Fast	
PS/2 Mouse Support	Disabled	Configure PS/2 mouse support.
	Enabled	<i>Note: PS/2 support for mouse or keyboard is only available if a Winbond W83627 Super I/O or a SSMC SCH3114 Super I/O has been implemented on the carrier board.</i>
	Auto	

9.4.10 Hardware Monitoring Submenu

Feature	Options	Description
H/W Health Function	Disabled Enabled	Enable hardware health monitoring device and display the readings.
Board Temperature	No option	Current board temperature
CPU Temperature	No option	Current processor die temperature
CPU Fan Speed	No option	Current CPU FAN speed
VcoreA	No option	Current Core A reading
+3.3VSB	No option	Current 3.3V standby reading
+5VSB	No option	Current 5V standby reading
+12Vin	No option	Current 12V in reading
VRTC	No option	Current VRTC reading

9.4.11 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	Disabled 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset..
Stop Watchdog For User Interaction	No Yes	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	Disabled One time trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to ' <i>One time trigger</i> ' the watchdog will be disabled after the first trigger. If set to ' <i>Single event</i> ', every stage will be executed only once, then the watchdog will be disabled. If set to ' <i>Repeated event</i> ' the last stage will be executed repeatedly until a reset occurs.
Delay	see Post Watchdog	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about <i>ACPI Event</i> see section 9.4.1 of this user's guide.
Event 2	Disabled NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	Disabled NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	0.5sec 1sec 2sec 5sec 10sec 30sec 1min 2min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.

9.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen. In the upper part of the screen the Boot setup allows you to prioritize the available boot devices. The lower part of this setup screen shows options related to the BIOS boot.

9.5.1 Boot Device Priority

Feature	Options	Description
Boot Priority Selection	Device Based Type Based	Select between device and type based boot priority lists. The “Device Based” boot priority list allows you to select from a list of currently detected devices only. The “Type Based” boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the “Device Based” boot priority list might change dynamically in cases when devices are physically removed or added to the system. The “Type Based” boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if device based priority list control is selected. If “Type Based” priority list control is enabled only 8 boot devices can be prioritized.)	Disabled Primary Master Primary Slave Secondary Master Secondary Slave Legacy Floppy USB Harddisk USB CDROM USB Removable Dev. Onboard LAN External LAN PCI Mass Storage PCI SCSI Card Any PCI BEV Device Onboard PCI SATA Third Master Third Slave PCI RAID Local BEV ROM	This view is only available when in the default “Type Based” mode. When in “Device Based” mode you will only see the devices that are currently connected to the system. The default boot priority is <i>Removables 1st, ATAPI CDROM 2nd, Hard Disk 3rd, BEV 4th</i> (BEV = Boot Entry Vector, e.g. Network or SCSI Option-ROMs).

9.5.2 Boot Settings Configuration

Feature	Options	Description
Quick Boot	Disabled Enabled	If <i>Enabled</i> , some POST tasks will be skipped to speed-up the BIOS boot process.
Quiet Boot	Disabled Enabled	<i>Disabled</i> displays normal POST diagnostic messages. <i>Enabled</i> displays OEM logo instead of POST messages. <i>Note: The default OEM logo is a dark screen.</i>
Boot Display	Clear Maintain	Controls the end of POST boot display handling, if Quiet Boot is enabled. If set to <i>Maintain</i> the BIOS will maintain the current display contents and graphics video mode used for POST display. If set to <i>Clear</i> the BIOS will clear the screen and switch to VGA text mode at end of POST.
Automatic Boot List Retry	Disabled Enabled	
Add-On ROM Display Mode	Force BIOS Keep current	Set display mode for Option ROM.
Halt On Error	Disabled Enabled	Determines whether the BIOS halts and displays an error message if an error occurs. If set to <i>Enabled</i> the BIOS waits for user input.
Hit 'DEL' Message Display	Disabled Enabled	Allows/Prevents the BIOS to display the ' <i>Hit Del to enter Setup</i> ' message.
Interrupt 19 Capture	Disabled Enabled	Allows/Prevents the option ROMs (such as network controllers) from trapping the boot strap interrupt 19.
PXE Boot to LAN	Disabled Enabled	Disable/Enable PXE boot to LAN <i>Note: When set to 'Enabled', the system has to be rebooted in order for the Intel Boot Agent device to be available in the Boot Device Menu. Only visible for variants with onboard Gigabit Ethernet controller.</i>
Boot from SATA	Disabled Enabled	Enables the boot ROM for the onboard SATA controller. <i>Note: Only visible for variants with onboard SATA controller.</i>
Power Loss Control (see note below)	Remain Off Turn On Last State	Specifies the mode of operation if an AC power loss occurs. <i>Remain Off</i> keeps the power off until the power button is pressed. <i>Turn On</i> restores power to the computer. <i>Last State</i> restores the previous power state before power loss occurred. <i>Note: Only works with an ATX type power supply.</i>



Note

1. The term 'AC power loss' stands for the state when the module loses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.
2. Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.

3. Unlike other module designs available in the embedded market, a CMOS battery is not required by congatec modules to support the 'Power Loss Control' feature.

9.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

9.6.1 Security Settings

Feature	Options	Description
Supervisor Password	Installed Not Installed	Reports if there is a supervisor password set.
User Password	Installed Not Installed	Reports if there is a user password set.
Change Supervisor Password	enter password	Specifies the supervisor password.
User Access Level	No Access View Only Limited Full Access	Sets BIOS setup utility access rights for user level.
Boot Selection Popup Menu Access	Anybody Setup User Setup Supervisor No Access	Select who can access the boot selection popup menu, when setup passwords are installed.
Change User Password	enter password	Specifies the user password.
Password Check	Setup Always	Setup: Check password while invoking setup Always: Check password also on each boot.
Boot Sector Virus Protection	Disabled Enabled	Select <i>Enabled</i> to enable boot sector protection. The BIOS displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. If enabled, the following appears when a write is attempted to the boot sector. You may have to type N several times to prevent the boot sector write. <i>Boot Sector Write!</i> <i>Possible VIRUS: Continue (Y/N)?</i> The following appears after any attempt to format any cylinder, head or sector of any hard disk drive via the BIOS INT13 hard disk drive service: <i>Format!!!</i> <i>Possible VIRUS: Continue (Y/N)?</i>
BIOS Update & Write Protection	Disabled Enabled	Only visible if a supervisor password is installed. If enabled the BIOS update and modification utilities will ask for the supervisor password before allowing any write accesses to the BIOS flash ROM chip.
END-Key Loads CMOS Defaults	Yes No	If set to Yes, the user can force the loading of CMOS defaults by pressing the END key during POST.

9.7 Exit Menu

Select the Exit tab from the setup menu to enter the Exit setup screen.

You can display an Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup and reboot so the new system configuration parameters can take effect.
Discard Changes and Exit	Exit setup without saving any changes made in the BIOS setup program.
Discard Changes	Discard changes without exiting setup. The option values presented when the computer was turned on are used.
Load CMOS Defaults	Load the CMOS defaults of all the setup options.

10 Additional BIOS Features

The conga-CA uses a congatec/AMIBIOS that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as CMENR1xx, where CMEN is the congatec internal project name, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

10.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” refer to the user’s guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

10.2 BIOS Recovery

The “BIOS recovery” scenario is recommended for situations when the normal flash update fails and the user can no longer boot back to an OS to restore the system. The code that handles BIOS recovery resides in a section of the flash referred to as “boot block”.

For more information about “BIOS Recovery” refer to application note AN6_BIOS_Recovery.pdf, which can be found on the congatec AG website at www.congatec.com.

10.2.1 BIOS Recovery via Storage Devices

In order to make a BIOS recovery from an IDE CD-ROM (ISO9660), USB floppy or USB CD-ROM, the BIOS file must be copied into the root directory of the storage device and renamed *AMIBOOT.ROM*.

For more information about “BIOS Recovery via Storage Devices” refer to application note AN6_BIOS_Recovery.pdf, which can be found on the congatec AG website at www.congatec.com.

10.3 BIOS Security Features

The BIOS provides both a supervisor and user password. If you use both passwords, the supervisor password must be set first. The system can be configured so that all users must enter a password every time the system boots or when setup is executed.

The two passwords activate two different levels of security. If you select password support you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed.

The supervisor password (supervisor mode) gives unrestricted access to view and change all the setup options. The user password (user mode) gives restricted access to view and change setup options.

If only the supervisor password is set, pressing <Enter> at the password prompt of the BIOS setup program allows the user restricted access to setup.

Setting the password check to 'Always' restricts who can boot the system. The password prompt will be displayed before the system attempts to load the operating system. If only the supervisor password is set, pressing <Enter> at the prompt allows the user to boot the system.

11 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.2	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
PICMG® COM Express Module™ Base Specification	http://www.picmg.org/
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications