COM Express™ conga-BM57/BS57/BE57

Intel® Core™ i7, i5, i3 or Celeron processor with an Intel® 5 Series HM55 chipset

User's Guide

Revision 1.2

Revision History

Revision	Date (dd.mm.yy)	Author	Changes
0.1	29.09.10	GDA	• Preliminary release
1.0	23.09.11	GDA	• Updated manual throughout. Official release.
1.1	17.02.12	GDA	• Added Caution note about the mandatory use of ECC memory on conga-BE57. Updated section 9 “BIOS Setup Description.”
1.2	06.12.12	AEM	• Changed maximum torque rating for heatspreader screws in section 3.1 “Heatspreader Dimensions” and added a caution statement. • Updated section 4.1.12 “Power Control”. Added note about the limitation of ethernet controller in section 4.1.4 “Gigabit Ethernet” and in table 4 of section 7.1 “A-B Connector Signal Description”. • Corrected pins C97 and D83 signal names to DDPD_CTRLCLK and DDPD_CTRLDATA respectively in section 7.4 “C-D Connector Pinout”. • Deleted the F7 key option in section 9.2 “Setup Menu and Navigation“. Deleted the power column in section 9.4 “Advanced Setup“.

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-BM57/BS57/BE57. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide

COM Express™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

Disclaimer

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Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
PCH	Platform Controller Hub
PATA	Parallel ATA
T.O.M.	Top of memory = max. DRAM installed
HDA	High Definition Audio
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

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COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). It's creation provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available today. COM Express™ modules are available in following form factors:

- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x 110mm

The COM Express™ specification 2.0 defines seven different pinout types.

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports
Type 1	A-B	Up to 6			1
Type 2	A-B C-D	Up to 22	32 bit	1	1
Type 3	A-B C-D	Up to 22	32 bit		3
Type 4	A-B C-D	Up to 32		1	1
Type 5	A-B C-D	Up to 32			3
Type 6	A-B C-D	Up to 24			1
Type 10	A-B	Up to 4			1

conga-BM57/BS57/BE57 modules utilize the Type 2 pinout definition. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are a legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 2 pinout provides the ability to offer 32-bit PCI, Parallel ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

Certification

congatec AG is certified to DIN EN ISO 9001 standard.

Technical Support

congatec AG technicians and engineers are committed to providing the best possible technical support for our customers so that our products can be easily used and implemented. We request that you first visit our website at www.congatec.com for the latest documentation, utilities and drivers, which have been made available to assist you. If you still require assistance after visiting our website then contact our technical support department by email at support@congatec.com

conga-BM57/BS57/BE57 Options Information

The conga-BM57 is available in three different variants, the conga-BS57 is available in four different variants while the conga-BE57 is available in five variants. This user's guide describes all of these variants. The tables below show the different configurations available. Check for the Part No. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

conga-BM57

Part-No.	046002	046001	046005
Processor (Socketed rPGA988A)	Intel® Core™ i7-620M 2.66 GHz	Intel® Core™ i5-520M 2.4 GHz	Intel® Celeron P4500 1.86 GHz 2 Core™
Intel® Smart Cache	4 MByte	3MByte	2 MByte
ECC Memory Support	No	No	No
PEG	No	No	No
SDVO	1 Port	1 Port	1 Port
DisplayPort (DP)	Yes	Yes	Yes
HDMI	Yes	Yes	Yes
Processor TDP	35 W	35 W	35 W

conga-BS57

Part-No.	040100	040105	040106	040107
Processor	Intel® Core™ i7-620LE 2.0 GHz	Intel® Core™ i7-620UE 1.06 GHz	Intel® Core™ i3-330E 2.13 GHz	Intel® Celeron U3405 1.07 GHz 2 Core™
Intel® Smart Cache	4 MByte	4 MByte	3 MByte	2 MByte
ECC Memory Support	No	No	No	No
PEG	No	No	No	No
SDVO	1 Port	1 Port	1 Port	1 Port
DisplayPort (DP)	Yes	Yes	Yes	Yes
HDMI	Yes	Yes	Yes	Yes
Processor TDP	25 W	18 W	35 W	18 W

conga-BE57

Part-No.	040203	040202	040204	040201	040200
Processor	Intel® Core™ i7-620LE 2.0 GHz	Intel® Core™ i7-610E 2.53 GHz	Intel® Core™ i3-330E 2.13 GHz	Intel® Celeron P4505 1.86 GHz 2 Core™	Intel® Celeron U3405 1.07 GHz 2 Core™
Intel® Smart Cache	4 MByte	4 MByte	3 MByte	2 MByte	2 MByte
ECC Memory Support	Yes	Yes	Yes	Yes	Yes
PEG	No	No	No	No	No
SDVO	1 Port	1 Port	1 Port	1 Port	1 Port
DisplayPort (DP)	Yes	Yes	Yes	Yes	Yes
HDMI	Yes	Yes	Yes	Yes	Yes
Processor TDP	25 W	25 W	35 W	35 W	18 W

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1 Specifications

1.1 Feature List

Table 1 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 2 (Basic size 95 x 125mm)
Processor	**conga-BM57:** Intel® Core™ i7-620M 2.66 GHz with 4-MByte Intel® Smart Cache (Socketed rPGA988) **conga-BM57:** Intel® Core™ i5-520M 2.4 GHz 3-MByte Intel® Smart Cache (Socketed rPGA988) **conga-BM57:** Intel® Celeron P4500 1.86 GHz 2 Core™ 1-MByte Intel® Smart Cache (Socketed rPGA988) **conga-BS57:** Intel® Core™ i7-620LE 2.0 GHz with 4-MByte Intel® Smart Cache **conga-BS57:** Intel® Core™ i7-620UE 1.06 GHz with 4-MByte Intel® Smart Cache **conga-BS57:** Intel® Core™ i3-330E 2.13 GHz with 3-MByte Intel® Smart Cache **conga-BS57:** Intel® Celeron U3405 1.07 GHz 2 Core™ with 2-MByte Intel® Smart Cache **conga-BE57:** Intel® Core™ i7-620LE 2.0 GHz with 4-MByte Intel® Smart Cache (supports ECC memory only) **conga-BE57:** Intel® Core™ i7-610E 2.53 GHz with 4-MByte Intel® Smart Cache (supports ECC memory only) **conga-BE57:** Intel® Core™ i3-330LE 2.13 GHz with 3-MByte Intel® Smart Cache (supports ECC memory only) **conga-BE57:** Intel® Celeron P4505 1.86 GHz 2 Core™ with 2-MByte Intel® Smart Cache (supports ECC memory only) **conga-BE57:** Intel® Celeron U3405 1.07 GHz 2 Core™ with 2-MByte Intel® Smart Cache (supports ECC memory only)
Memory	2 sockets: SO-DIMM DDR3 1333MHz up to 8-GByte. Sockets located top and bottom side of module. Only conga-BE57 supports ECC memory.
Chipset	Intel® 5 Series Chipset: Intel® BD82HM55 PCH
Audio	HDA (High Definition Audio)/digital audio interface with support for multiple codecs
Ethernet	Gigabit Ethernet: Integrated within the Intel® HM55 + Intel® 82577LM Phy.
Graphics Options	Intel® HD Graphics Controller, Intel® Dynamic Video Memory Technology (Intel® DVMT) OpenGL 2.1 and DirectX10 support. Two independent pipelines for full dual view support. • CRT Interface 350 MHz RAMDAC Resolutions up to 2048x1536 @ 75Hz (QXGA) • Flat panel Interface (integrated) 2x25-112MHz single/dual-channel LVDS Transmitter Single-channel LVDS interface support: 1 x 18 bpp OR 1 x 24 bpp Dual-channel LVDS interface support: 2 x 18 bpp OR 2 x 24 bpp panel support Supports VESA LVDS color mappings. Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3) Resolutions 640x480 up to 1900x1200 (WUXGA) • HDMI: 3x HDMI ports on digital ports B, C and D. Multiplexed with DisplayPort (DP). • DisplayPort 1.1 (DP): 3x DisplayPorts ports on digital ports B, C and D. Multiplexed with HDMI ports. Hot-Plug detect support. • DVI: 3x DVI ports on digital ports B, C and D. Multiplexed with HDMI/DP ports. Hot-Plug detect support. • AUX Output 1 x Intel® compliant SDVO port (serial DVO) 200MPixel/sec on digital port B and multiplexed with HDMI/DP/DVI ports. Supports external DVI, TV and LVDS transmitters.
Peripheral Interfaces	• 3x Serial ATA® no RAID support (4x Serial ATA® if SATA to PATA chip is not used) • 5 PCI Express® Lanes. Support for full 2.5 Gb/s bandwidth in each direction per x1 links (can be configured via BIOS firmware to support one x1s and one x4 link. A special BIOS is required for one x4 link). • 8x USB 2.0 (EHCI) • PCI Bus Rev. 2.3 • 1x EIDE (UDMA-66/100) • LPC Bus • I²C Bus, Fast Mode (400 kHz) multimaster
BIOS	AMI Aptio® UEFI 2.x firmware, 4MByte serial SPI with congatec Embedded BIOS features
Power Management	ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 8 of this user's guide to determine what options are available on your particular module.

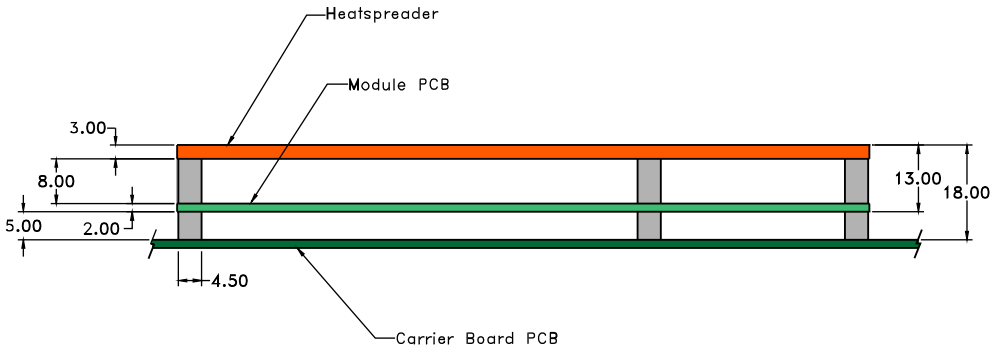
1.2 Supported Operating Systems

The conga-BM57/BS57/BE57 supports the following operating systems.

- Microsoft® Windows® 7
- Microsoft® Windows® XP
- Microsoft® Windows® Embedded Standard
- Linux
- QNX

1.3 Mechanical Dimensions

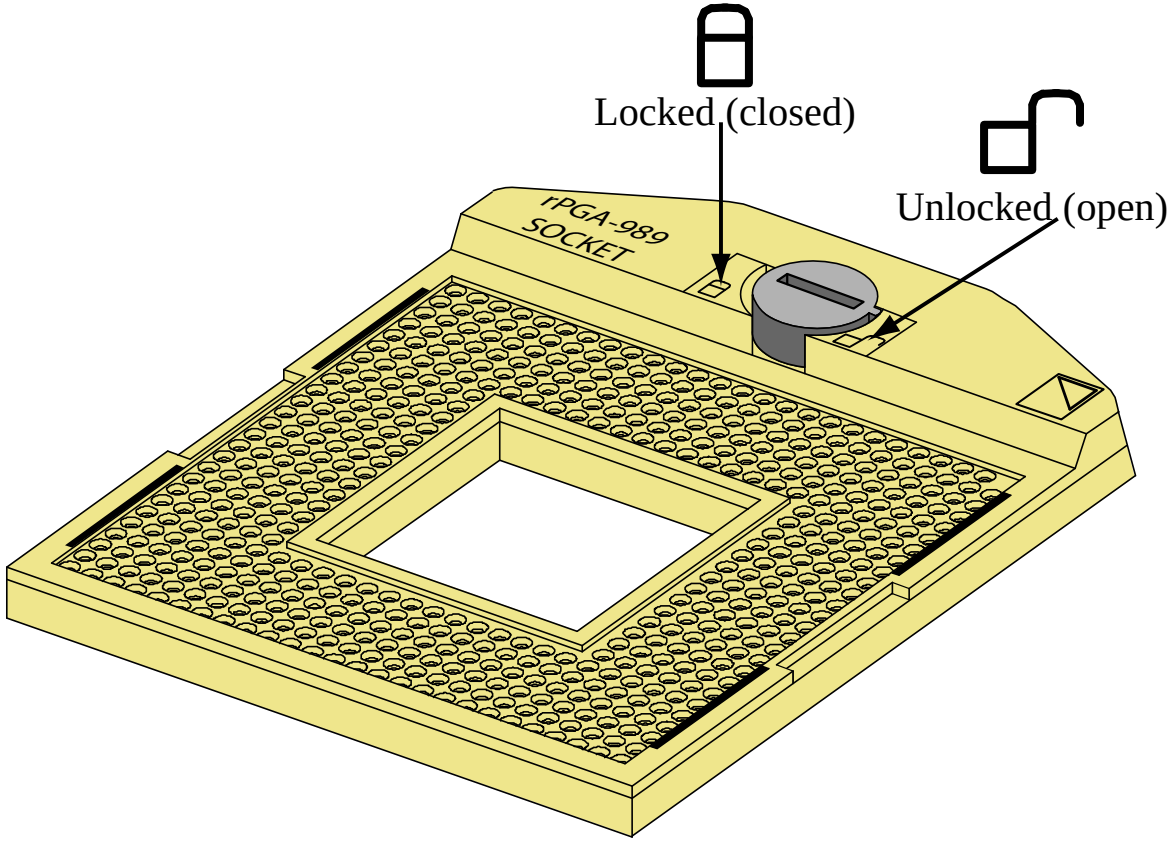
- 95.0 mm x 125.0 mm (3.74" x 4.92")
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm.



1.4 Socketed Variant of conga-BM57

The conga-BM57 is equipped with a PGA socket. This socket has 989 contacts and mates with a rPGA package that has a maximum of 988 pins. The insertion and extraction forces are zero when the socket is not engaged (in the “open” position).

There are clear indicator marks located on the actuation mechanism that identify the lock (closed) and unlock (open) positions of the cover as well as the actuation direction (see picture below). These marks remain visible after the processor is inserted into the socket.



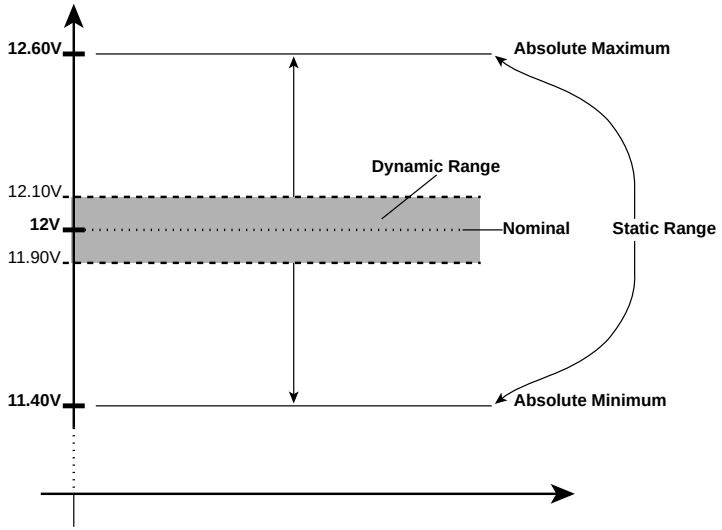
Electrostatic Sensitive Device

The conga-BM57 is an electrostatic sensitive device. Do not handle the conga-BM57, or processor, except at an electrostatic-free workstation. Failure to do so may cause damage to the module and/or processor and void the manufacturer’s warranty.

1.5 Supply Voltage Standard Power

- 12V DC ± 5%

The dynamic range shall not exceed the static range.



1.5.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 2 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

1.5.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum rise time of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

1.6 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used for testing includes a conga-BM57/BS57/BE57 module, conga-Cdebug carrier board, CRT monitor, SATA drive, and USB keyboard. The conga-Cdebug is modified so that the 12V input is only routed to the module and all other circuity on the carrier itself is powered by the 5V input. The SATA drive was powered externally by an ATX power supply so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. All recorded values were averaged over a 30 second time period. Cooling of the module was done by the module specific heatpipe heatspreader and a fan cooled heatsink to measure the power consumption under normal thermal conditions.

The conga-Cdebug originally does not provide 5V standby power. Therefore, an extra 5V_SB connection without any external loads was made. Using this setup, the power consumption of the module in S3 (Standby) mode was measured directly.

Each module was measured while running Windows 7 Professional 64Bit, Hyper Threading enabled, Speed Step enabled, CPU Turbo Mode enabled and Power Plan set to “Power Saver”. This setting ensures that Core™ processors run in LFM (lowest frequency mode) with minimal core voltage during desktop idle. Each module was tested while using two 1GB memory modules. For the conga-BE57 a 2GB ECC memory module was used. Using different sizes of RAM, as well as one or two memory modules, will cause slight variances in the measured results.

To measure the worst case power consumption the cooling solution was removed and the CPU core temperature was allowed to run up to between 95° and 100°C while running 100% workload with the Power Plan set to “Balanced”. The peak current value was then recorded. This value should be taken into consideration when designing the system’s power supply to ensure that the power supply is sufficient during worst case scenarios.

Power consumption values were recorded during the following stages:

Windows 7 (64 bit)

- Desktop Idle (power plan = Power Saver)
- 100% CPU workload (see note below, power plan = Power Saver)
- 100% CPU workload at approximately 100°C peak power consumption (power plan = Balanced)
- Suspend to RAM. Supply power for S3 mode is 5V.

Note

A software tool was used to stress the CPU to Max Turbo Frequency.

Processor Information

In the following power tables there is some additional information about the processors. Intel® offers processors that are considered to be low power consuming. These processors can be identified by their voltage status and Intel® uses specific terms to describe the voltage status. For example with the i7-620UE, the U represents ultra low voltage. For more information about these naming conventions visit the Intel® website.

Intel® also describes the type of manufacturing process used for each processor. The following term is used:

nm=nanometer

The manufacturing process description is included in the power tables as well. See example below. For information about the manufacturing process visit Intel®'s website.

Intel® Core™ i7-620LE 2.0 GHz 4MB Intel® Smart Cache

32nm

1.6.1 conga-BM57 Intel® Core™ i7-620M 2.66 GHz 4MB Cache

conga-BM57 Art. No. 046002	Intel® Core™ i7-620M 2.66 GHz 4MB Intel® Smart Cache 32nm Layout Rev. BM57LA0 /BIOS Rev. BM57R006			
Max Turbo Frequency	3.333 GHz			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.6 A/7.2 W (12V)**	**4.9 A/58.8 W (12V)**	**6.2 A/74.4 W (12V)**	**0.17 A/0.85 W (5V)**

1.6.2 conga-BM57 Intel® Core™ i5-520M 2.4 GHz 3MB Cache

conga-BM57 Art. No. 046001	Intel® Core™ i5-520M 2.4 GHz 3MB Intel® Smart Cache 32nm Layout Rev. BM57LA0 /BIOS Rev. BM57R006			
Max Turbo Frequency	2.933 GHz			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.6 A/7.2 W (12V)**	**4.4 A/52.8 W (12V)**	**5.8 A/69.6 W (12V)**	**0.17 A/0.85 W (5V)**

1.6.3 conga-BM57 Intel® Celeron® P4500 1.86 GHz 2 Core™ 2MB Cache

conga-BM57 Art. No. 046005	Intel® P4500 1.86 GHz 2 Core™ 2MB Intel® Smart Cache 32nm Layout Rev. BM57LA0 /BIOS Rev. BM57R006			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**1.1 A/13.2 W (12V)**	**3.4 A/40.8 W (12V)**	**4.4 A/52.8 W (12V)**	**0.14 A/0.70 W (5V)**

1.6.4 conga-BS57 Intel® Core™ i7-620LE 2.0 GHz 4MB Cache

conga-BS57 Art. No. 040100	Intel® Core™ i7-620LE 2.0 GHz 4MB Intel® Smart Cache 32nm Layout Rev. BS57LX0 /BIOS Rev. BM57R006			
Max Turbo Frequency	2.8 GHz			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.6** A/7.2 W (12V)	**3.7** A/44.4 W (12V)	**4.2** A/50.4 W (12V)	**0.19** A/0.95 W (5V)

1.6.5 conga-BS57 Intel® Core™ i7-620UE 1.06 GHz 4MB Cache

conga-BS57 Art. No. 040105	Intel® Core™ i7-620UE 1.06 GHz 4MB Intel® Smart Cache 32nm Layout Rev. BS57LX0 /BIOS Rev. BM57R006			
Max Turbo Frequency	2.13 GHz			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**TBD** A/ W (12V)	**TBD** A/ W (12V)	**TBD** A/ W (12V)	**TBD** A/ W (5V)

1.6.6 conga-BS57 Intel® Core™ i3-330E 2.13 GHz 3MB Cache

conga-BS57 Art. No. 040106	Intel® Core™ i3-330E 2.13 GHz 3MB Intel® Smart Cache 32nm Layout Rev. BS57LX0 /BIOS Rev. BM57R006			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**TBD** A/ W (12V)	**TBD** A/ W (12V)	**TBD** A/ W (12V)	**TBD** A/ W (5V)

1.6.7 conga-BS57 Intel® Celeron® U3405 1.07 GHz 2 Core™ 2MB Cache

conga-BS57 Art. No. 040107	Intel® Celeron® 1.06 GHz 2 Core™ 2MB Intel® Smart Cach 32nm Layout Rev. BS57LX0 /BIOS Rev. BM57R006			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**0.6 A/7.2 W (12V)**	**1.9 A/22.8 W (12V)**	**2.6 A/31.2 W (12V)**	**0.14 A/0.70 W (5V)**

1.6.8 conga-BE57 Intel® Core™ i7-620LE 2.0 GHz 4MB Cache

conga-BE57 Art. No. 040203	Intel® Core™ i7-620LE 2.0 GHz 4MB Intel® Smart Cache 32nm Layout Rev. BE57LX0 /BIOS Rev. BM57R006			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**TBD A/ W (12V)**	**TBD A/ W (12V)**	**TBD A/ W (12V)**	**TBD A/ W (5V)**

1.6.9 conga-BE57 Intel® Core™ i7-610E 2.53 GHz 4MB Cache

conga-BE57 Art. No. 040202	Intel® Core™ i7-610E 2.53 GHz 4MB Intel® Smart Cache 32nm Layout Rev. BE57LX0 /BIOS Rev. BM57R006			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**TBD A/ W (12V)**	**TBD A/ W (12V)**	**TBD A/ W (12V)**	**TBD A/ W (5V)**

1.6.10 conga-BE57 Intel® Core™ i3-330E 2.13 GHz 3MB Cache

With 2GB ECC memory installed

conga-BE57 Art. No. 040204	Intel® Core™ i3-330E 2.13 GHz 4MB Intel® Smart Cache 32nm Layout Rev. BE57LX0 /BIOS Rev. BM57R006			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	**Windows 7 (64 bit)**			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	**TBD A/ W (12V)**	**TBD A/ W (12V)**	**TBD A/ W (12V)**	**TBD A/ W (5V)**

1.6.11 conga-BE57 Intel® Celeron® P4505 1.80 GHz 2 Core™ 2MB Cache

With 2GB ECC memory installed

conga-BE57 Art. No. 040201	Intel® Celeron® P4505 1.80GHz 2 Core™ 2MB Intel® Smart Cache 32nm Layout Rev. BE57LX0 /BIOS Rev. BM57R006			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	Windows 7 (64 bit)			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	TBD A/ W (12V)	TBD A/ W (12V)	TBD A/ W (12V)	TBD A/ W (5V)

1.6.12 conga-BE57 Intel® Celeron® U3405 1.07 GHz 2 Core™ 2MB Cache

With 2GB ECC memory installed

conga-BE57 Art. No. 040200	Intel® Celeron® 1.06GHz 2 Core™ 2MB Intel® Smart Cache 32nm Layout Rev. BE57LX0 /BIOS Rev. BM57R006			
Max Turbo Frequency	Not supported			
Memory Size	2GB			
Operating System	Windows 7 (64 bit)			
Power State	Desktop Idle	100% workload	100% workload approx. 100°C CPU temp (peak)	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	TBD A/ W (12V)	TBD A/ W (12V)	TBD A/ W (12V)	TBD A/ W (5V)

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Supply power for S3 mode is 5V while all other measured modes are supplied with 12V power. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

1.7 Supply Voltage Battery Power

- 2.0V-3.5V DC
- Typical 3V DC

1.7.1 CMOS Battery Power Consumption

RTC @ 20ºC	Voltage	Current
Integrated in the Intel® BD82HM55 PCH	3V DC	2.83 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

1.8 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

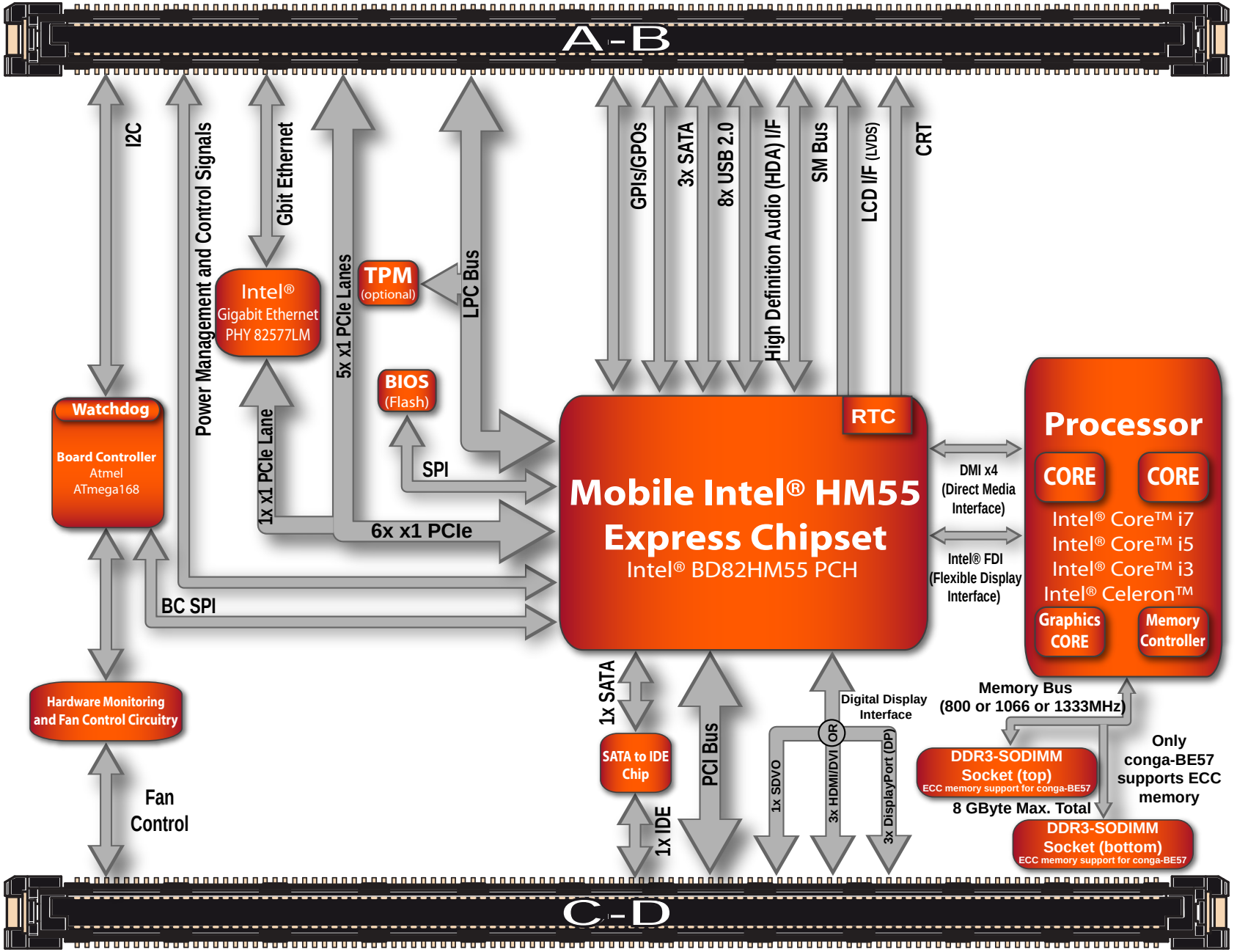
congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.

If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

For more information about operating a congatec module without heatspreader contact congatec technical support.

Humidity specifications are for non-condensing conditions.

2 Block Diagram



3 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module. It is a 3mm thick aluminum plate.

The heatspreader is thermally coupled to the CPU and other heat generating components via a heat pipe.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

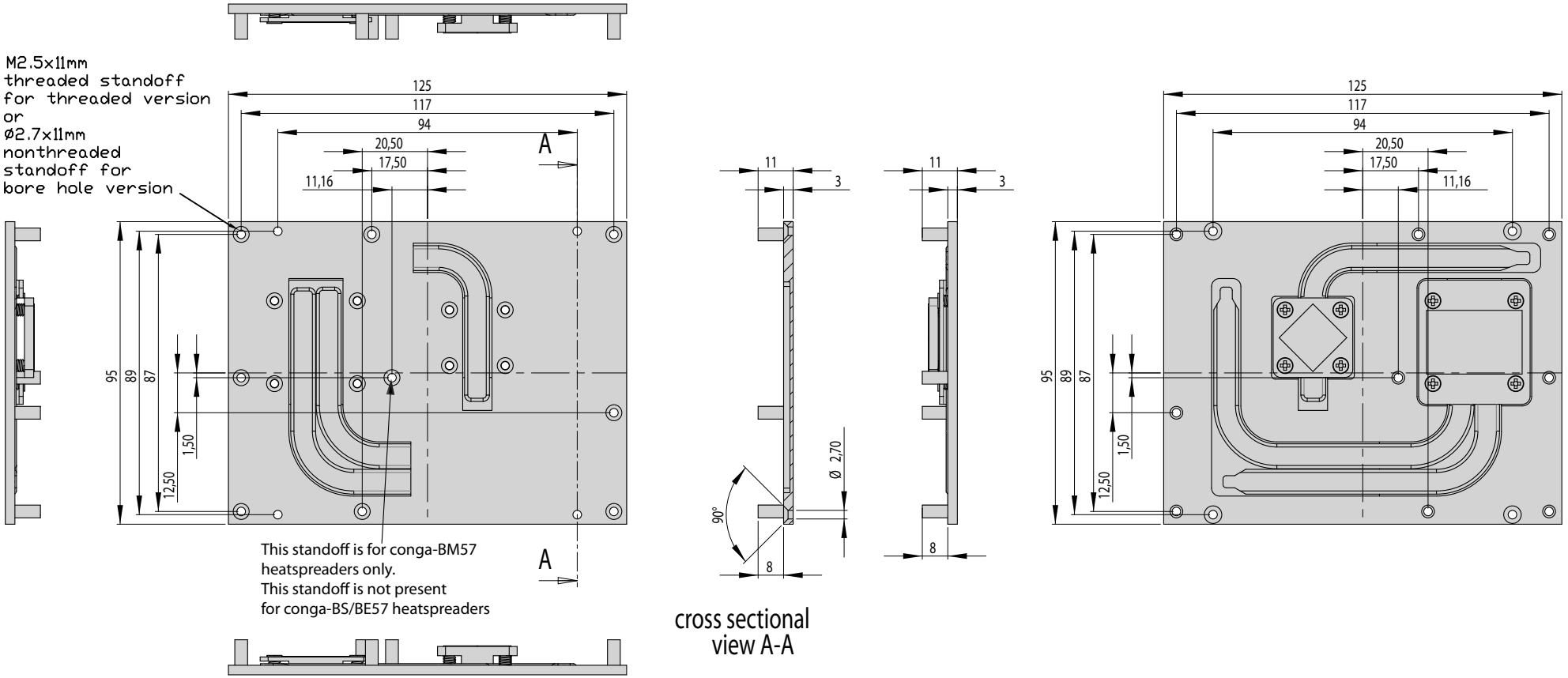
For additional information about the conga-BM57/BS57/BE57 heatspreader, refer to section 3.2 of this document.

Caution

There are mounting holes on the heatspreader designed to attach the heatspreader to the module. These mounting holes must be used to ensure that all components that are required to make contact with heatspreader do so. Failure to utilize the these mounting holes will result in improper contact between these components and heatspreader thereby reducing heat dissipation efficiency.

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

3.1 Heatspreader Dimensions



Note

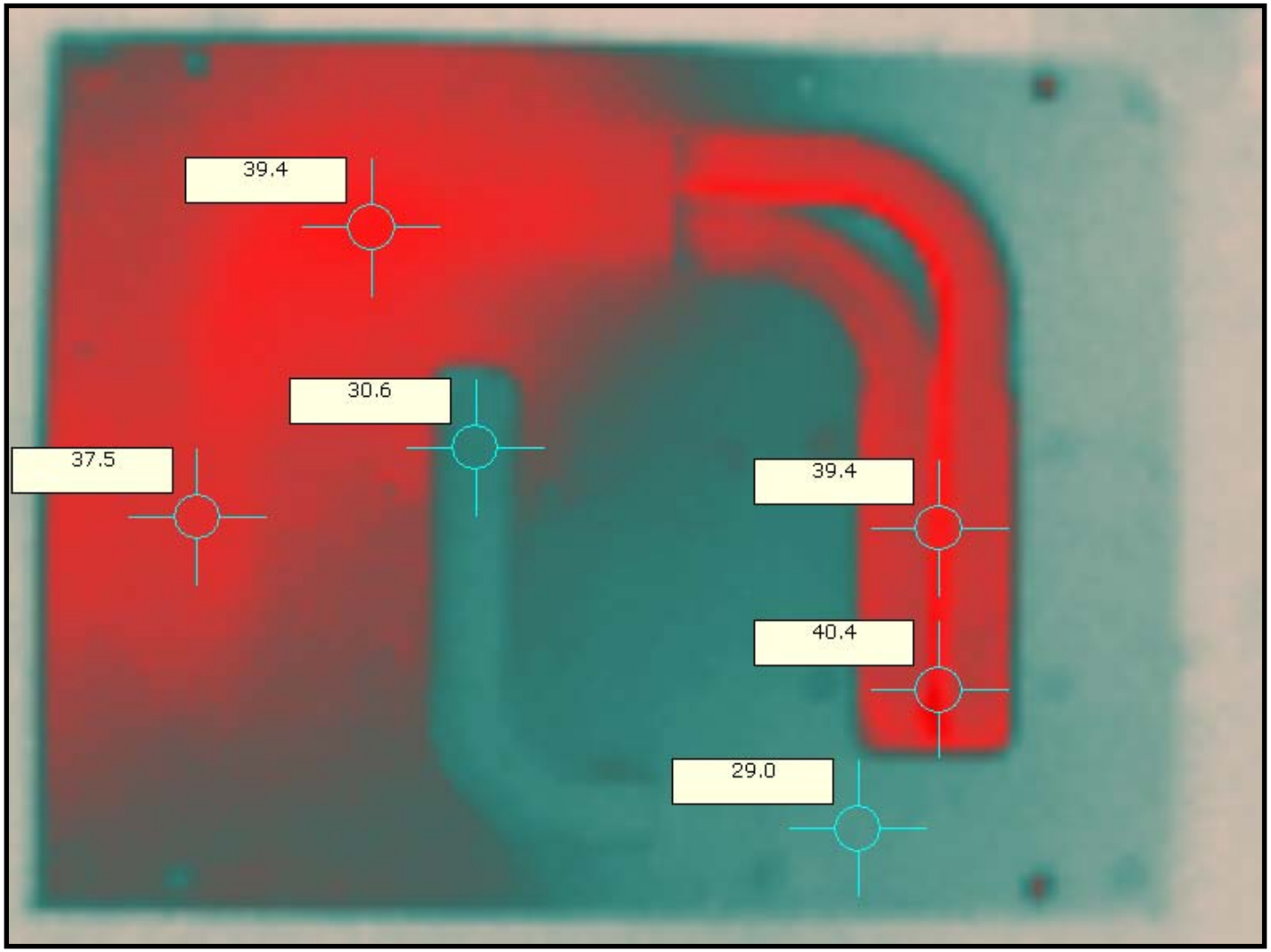
All measurements are in millimeters. Torque specification for heatspreader screws is 0.3 Nm. Mechanical system assembly mounting shall follow the valid DIN/IS0 specifications.

Caution

When using the heatspreader in a high shock and/or vibration environment, congatec recommends the use of a thread-locking fluid on the heatspreader screws to ensure the above mentioned torque specification is maintained.

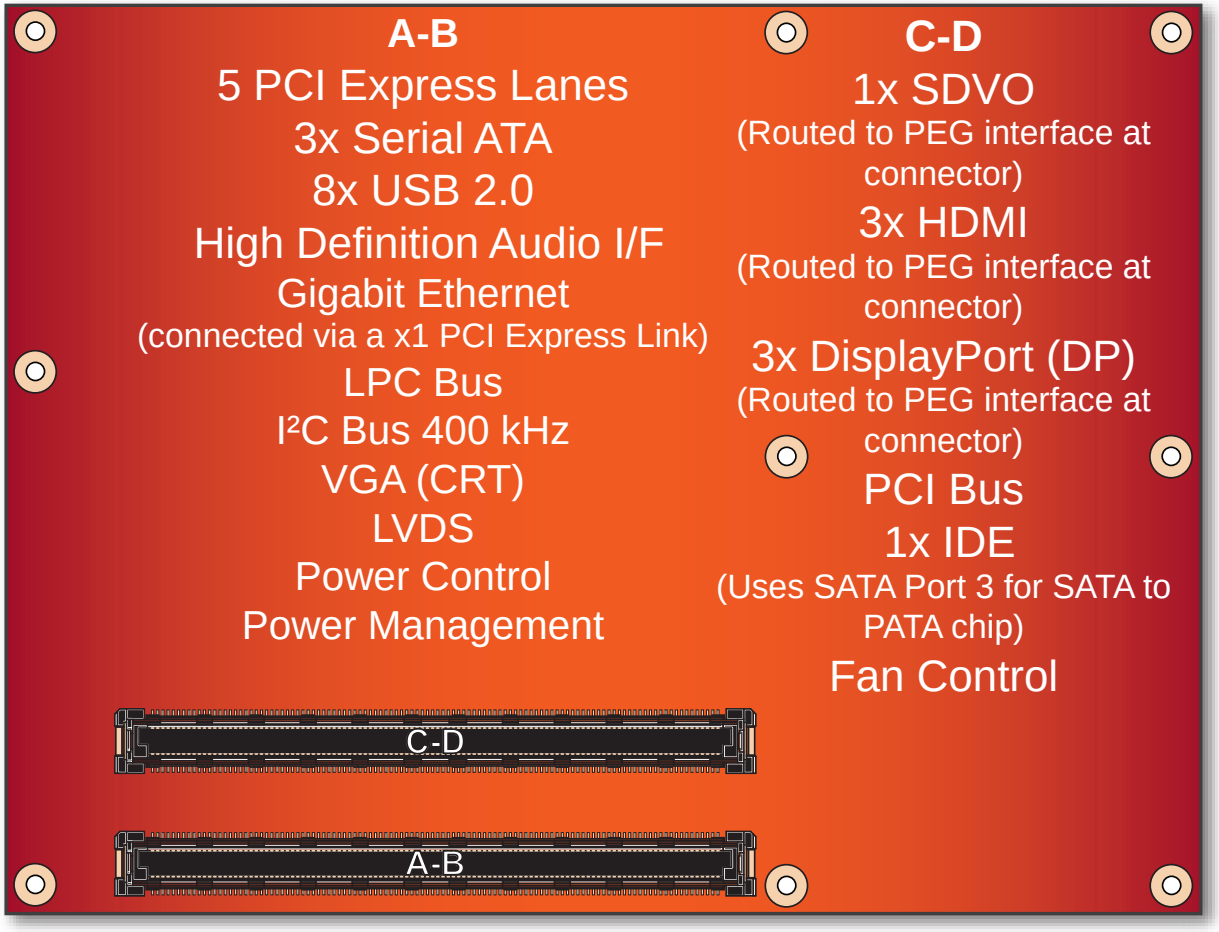
3.2 Heatspreader Thermal Imagery

The conga-BM57/BS57/BE57 heatspreader solution features heat pipes. A heat pipe is a simple device that can quickly transfer heat from one point to another. They are often referred to as the “superconductors” of heat as they possess an extra ordinary heat transfer capacity and rate with almost no heat loss. The thermal image below provides a reference to where the heat is being transferred to on the heatspreader surface area when using the conga-BM57 Intel® Core™ i7-620M 2.66GHz. All surface temperatures shown in the thermal image are in centigrade. System designers must ensure that the system’s cooling solution is designed to dissipate the heat from the hottest surface spots of the heatspreader.



4 Connector Subsystems Rows A, B, C, D

The conga-BM57/BS57/BE57 is connected to the carrier board via two 220-pin connectors (COM Express Type 2 pinout) for a total of 440 pins connectivity. These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.



top view

In this view the connectors are seen “through” the module.

4.1 Primary Connector Rows A and B

The following subsystems can be found on the primary connector rows A and B.

4.1.1 Serial ATA™ (SATA)

Three Serial ATA connections are provided via the Intel® BD82HM55 (HM55) PCH. These SATA ports are capable of up to 3.0 Gb/s transfer rate. If the conga-BM57/BS57/BE57 does not support the PATA interface then four SATA connections are available at connector rows A and B.

4.1.2 USB 2.0

The conga-BM57/BS57/BE57 offers two EHCI USB host controllers provided by the Intel® BD82HM55 (HM55) PCH. These controllers comply with USB standard 1.1 and 2.0 and offer a total of 8 USB ports via connector rows A and B. Each port is capable of supporting USB 1.1 and 2.0 compliant devices. For more information about how the USB host controllers are routed see section 6.6.

Note

The USB controller is a PCI bus device. The BIOS allocates the necessary system resources when configuring the PCI devices.

4.1.3 High Definition Audio (HDA) Interface

The conga-BM57/BS57/BE57 provides an interface that supports the connection of HDA audio codecs.

4.1.4 Gigabit Ethernet

The conga-BM57/BS57/BE57 is equipped with a Gigabit Ethernet Controller that is integrated within the Intel® BD82HM55 (HM55) PCH. This controller is combined with an Intel® 82577LM Phy that is implemented through the use of the sixth PCI Express lane. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

Note

The GBE0_LINK# output is only active during a 100Mbit or 1Gbit connection, it is not active during a 10Mbit connection. This is a limitation of Ethernet controller since it only has 3 LED outputs, ACT#, LINK100# and LINK1000#. The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-BM/BS/BE57 module.

4.1.5 LPC Bus

conga-BM57/BS57/BE57 offers the LPC (Low Pin Count) bus through the use of the Intel® BD82HM55 (HM55) PCH. There are many devices available for this Intel® defined bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific baseboard using this bus. See section 8.2.1 for more information about the LPC Bus.

4.1.6 I²C Bus 400kHz

The I²C bus is implemented through the use of ATMEL ATmega168 microcontroller. It provides a Fast Mode (400kHz max.) multi-master I²C Bus that has maximum I²C bandwidth.

4.1.7 PCI Express™

The conga-BM57/BS57/BE57 offers 6 PCI Express™ lanes via the Intel® BD82HM55 (HM55) PCH. The PCI Express™ interface offers support for full 2.5 Gb/s bandwidth in each direction per x1 link.

One of the six PCI Express lanes is utilized by the onboard Gigabit Ethernet interface therefore there are only 5 PCI Express lanes available on the A,B connector row. Default configuration for these 5 lanes is 5x x1. A 1x x4 and 1x x1 link configuration is also possible but requires a special/customized BIOS firmware. Contact congatec technical support for more information about this subject.

The PCI Express interface is based on the PCI Express Specification 2.0 running at 2.5 GT/s.

4.1.8 ExpressCard™

The conga-BM57/BS57/BE57 supports the implementation of ExpressCards, which requires the dedication of one USB port and a x1 PCI Express link for each ExpressCard used.

4.1.9 Graphics Output (VGA/CRT)

The conga-BM57/BS57/BE57 graphics are driven by a Mobile Intel® 5 Series HD graphics engine, which is incorporated within the processor found on the conga-BM57/BS57/BE57. This graphic engine offers significantly higher performance than previous Intel® graphics engines found on previous Intel® chipsets.

4.1.10 LCD

The Intel® BD82HM55 PCH found on the conga-BM57/BS57/BE57, offers an integrated dual channel LVDS interface. There are two LVDS transmitter channels (Channel A and Channel B) in the LVDS interface. Channel A and Channel B consist of 4-data pairs and a clock pair each.

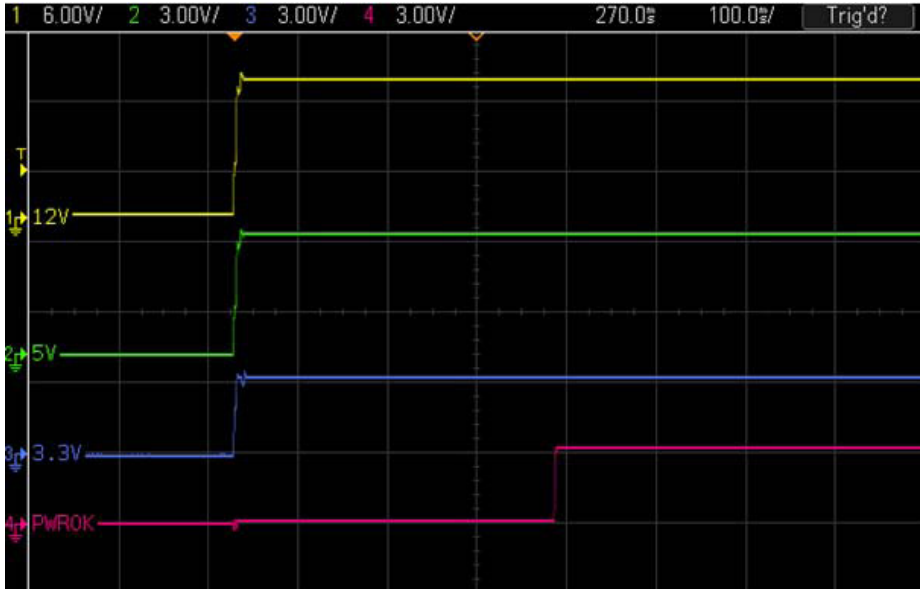
4.1.11 TV-Out

Integrated TV-Out support is not supported on the conga-BM57/BS57/BE57

4.1.12 Power Control

PWR_OK

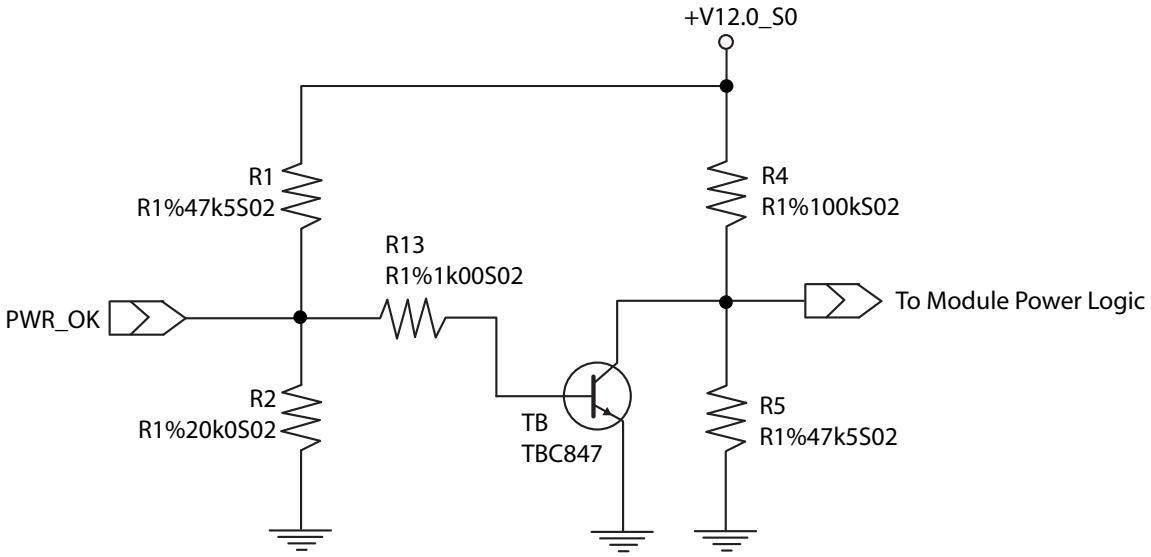
Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. See screenshot below.



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The conga-BM57/BS57/BE57 PWR_OK input circuitry is implemented as shown below:



The voltage divider ensures that the input complies with 3.3V CMOS characteristic and also allows for carrier board designs that are not driving PWR_OK. Although the PWR_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

When considering the above shown voltage divider circuitry and the transistor stage, the voltage measured at the PWR_OK input pin may be only around 0.8V when the 12V is applied to the module. Actively driving PWR_OK high is compliant to the COM Express specification but this can cause back driving. Therefore, congatec recommends driving the PWR_OK low to keep the module in reset and tri-state PWR_OK when the carrier board hardware is ready to boot.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the “power good” signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, it must be ensured that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-BM57/BS57/BE57 provides support for controlling ATX-style power supplies. When not using an ATX power supply, then the conga-BM57/BS57/BE57's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

12 volt input power is the sole operational power source for the conga-BM57/BS57/BE57. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-BM57/BS57/BE57 application:

- It has also been noticed that on some occasions problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

4.1.13 Power Management

ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

4.2 Secondary Connector Rows C and D

The following subsystems can be found on the secondary connector rows C and D.

4.2.1 PCI Express Graphics (PEG)

The PCI Express graphics interface is not supported by the conga-BM57/BS57/BE57.

4.2.2 SDVO

The Serial Digital Video Output (SDVO) is multiplexed with HDMI and DisplayPort on the PCI Express Graphics (PEG) interface pins of the COM Express connector. It may be used for a third party SDVO compliant device connected to port B. See section 7.5 of this document for more information about enabling SDVO peripherals.

Note

The standard variants of conga-BM57/BS57/BE57 do not support the FIELD_STALL signal pair used by some SDVO to LVDS and TV transmitters. The FIELD_STALL signal pair can be optionally made available. For more information about this subject contact congatec technical support.

4.2.3 HDMI

The Intel® BD82HM55 (HM55) PCH on the conga-BM57/BS57/BE57 supports integrated HDMI, which is multiplexed onto the PCI Express Graphics (PEG) interface of the COM Express connector. The Intel® HM55 provides three ports capable of supporting HDMI. See section 7.5 of this document for more information about enabling HDMI peripherals.

Note

For more information about implementing a HDMI interface on COM Express™ carrier boards, refer to application note AN17_HDMI_DP_Implementation.pdf, which can be found on the congatec website.

4.2.4 DisplayPort (DP)

The conga-BM57/BS57/BE57 offers three DP ports, each capable of supporting link-speeds of 1.62 Gbps and 2.7 Gbps on 1, 2 or 4 data lanes. The DP is multiplexed onto the PCI Express Graphics (PEG) interface of the COM Express connector. The DisplayPort specification is a VESA standard aimed at consolidating internal and external connection methods to reduce device complexity, supporting key cross industry applications, and providing performance scalability to enable the next generation of displays. The Intel® BD82HM55 (HM55) PCH can support a maximum of 2 DP ports simultaneously. See section 7.5 of this document for more information about enabling DisplayPort peripherals.

Note

For more information about implementing a DisplayPort (DP) interface on COM Express™ carrier boards, refer to application note AN17_HDMI_DP_Implementation.pdf, which can be found on the congatec website.

4.2.5 PCI Bus

The PCI bus complies with PCI specification Rev. 2.3 and provides a 32bit parallel PCI bus that is capable of operating at 33MHz.

Note

The PCI interface is specified to be +5V tolerant, with +3.3V signaling.

4.2.6 IDE (PATA)

The conga-BM57/BS57/BE57 supports an IDE channel that is capable of UDMA-100 operation. This channel is implemented by converting SATA Port 3 to an IDE channel using JMicron's single chip solution for serial and parallel ATA translation. The IDE interface supports the connection of only one device (master) at any given moment.

5 Additional Features

5.1 congatec Board Controller (cBC)

The conga-BM57/BS57/BE57 is equipped with an ATMEL Atmega168 microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

5.2 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

5.3 Watchdog

The conga-BM57/BS57/BE57 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-BM57/BS57/BE57 does not support external hardware triggering. For more information about the Watchdog feature see the BIOS setup description section 9.4.2 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

5.4 I²C Bus

The conga-BM57/BS57/BE57 offers support for the frequently used I²C bus. Thanks to the I²C host controller in the cBC the I²C bus is multimaster capable and runs at speeds up to 400kHz (fast mode).

5.5 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behaviour of the system after a AC power loss condition. Supported modes are “Always On”, “Remain Off” and “Last State”.

5.6 Embedded BIOS

The conga-BM57/BS57/BE57 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. These are the most important embedded PC features:

5.6.1 CMOS Backup in Non Volatile Memory

A copy of the CMOS memory (SRAM) is stored in the BIOS flash device. This prevents the system from not booting up with the correct system configuration if the backup battery (RTC battery) has failed. Additionally, it provides the ability to create systems that do not require a CMOS backup battery.

5.6.2 OEM CMOS Default Settings and OEM BIOS Logo

This feature allows system designers to create and store their own CMOS default configuration and BIOS logo (splash screen) within the BIOS flash device. Customized BIOS development by congatec for these changes is no longer necessary because customers can easily do these changes by themselves using the congatec system utility CGUITL.

5.6.3 OEM BIOS Code

With the congatec embedded BIOS it is even possible for system designers to add their own code to the BIOS POST process. Except for custom specific code, this feature can also be used to support Win XP SLP installation, Window 7 SLIC table, verb tables for HDA codecs, rare graphic modes and Super I/O controllers.

For more information about customizing the congatec embedded BIOS refer to the congatec System Utility user's guide, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com or contact congatec technical support.

5.6.4 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-BM57/BS57/BE57 BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBM²C User's Guide

5.6.5 API Support (CGOS/EAPI)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux and QNX. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website .

Other COM (Computer on Modules) vendors offer similar driver solutions for these kind of embedded PC features, which are by nature proprietary. All the API solutions that can be found on the market are not compatible to each other. As a result, writing application software that can run on more than one vendor's COM is not so easy. Customers have to change their application software when switching to another COM vendor. EAPI (Embedded Application Programming Interface) is a programming interface defined by the PICMG that addresses this problem. With this unified API it is now possible to run the same application on all vendor's COMs that offer EAPI driver support. Contact congatec technical support for more information about EAPI.

5.7 Security Features

The conga-BM57/BS57/BE57 can be equipped optionally with a “Trusted Platform Module“ (TPM 1.2). This TPM 1.2 includes coprocessors to calculate efficient hash and RSA algorithms with key lengths up to 2,048 bits as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity and confidence levels.

5.8 Suspend to Ram

The Suspend to RAM feature is available on the conga-BM57/BS57/BE57.

5.9 ECC Memory Support

Error-Correcting Code (ECC) memory is a memory system that tests for and corrects errors automatically, very often without the operating system being aware of it, let alone the user. As data are written into memory, ECC circuitry generates checksums from the binary sequences in the bytes and stores them in an additional seven bits of memory for 32-bit data paths or eight bits for 64-bit paths. When data are retrieved from memory, the checksum is recomputed to determine if any of the data bits have been corrupted.

The conga-BE57 supports ECC memory. The conga-BM57 and conga-BS57 **DO NOT** support ECC memory.

Caution

The conga-BE57 only supports the use of ECC memory. Using non ECC memory will cause irreparable damage to the module and this type of damage will not be covered by the warranty.

6 conga Tech Notes

The conga-BM57/BS57/BE57 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

6.1 Intel Turbo Boost

Intel® Turbo Boost Technology allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits. Intel® Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state. The maximum frequency of Intel® Turbo Boost Technology is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost Technology state depends on the workload and operating environment. Any of the following can set the upper limit of Intel® Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase by 133 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached. For more information about Intel® Turbo Boost Technology visit the Intel® website.

Note

Only conga-BM57/BS57/BE57 module variants that feature the Core™ i7 and i5 processors support Intel® Turbo Boost Technology. Refer to the power consumption tables in section 1.6 of this document for information about the max turbo frequency available for each variant of the conga-BM57/BS57/BE57.

6.2 Intel® Matrix Storage Technology

The Intel® BD82HM55 (HM55) PCH provides support for Intel® Matrix Storage Technology, providing AHCI functionality.

6.2.1 AHCI

The HM55 PCH provides hardware support for Advanced Host Controller Interface (AHCI), a new programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

6.3 Intel® Processor Features

6.3.1 Thermal Monitor and Catastrophic Thermal Protection

Intel® Core™ i7/i5/i3 and Celeron® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature, that the Intel® Thermal Monitor uses to activate the TCC, cannot be configured by the user nor is it software visible.

The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel Speedstep transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.

Note

The maximum operating temperature for Intel® Core™ i7/i5/i3 and Celeron® processors is 100°C. TM2 mode is used for Intel® Core™ i7/i5/i3 and the latest generation of Celeron® processors.

Two modes are supported by the Thermal Monitor to activate the TCC. They are called Automatic and On-Demand. No additional hardware, software, or handling routines are necessary when using Automatic Mode.

Note

To ensure that the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Core™ i7/i5/i3 and Celeron® processor's respective datasheet can provide you with more information about this subject.

THERMTRIP# signal is used by Intel®'s Core™ i7/i5/i3 and Celeron® processors for catastrophic thermal protection. If the processor's silicon reaches a temperature of approximately 125°C then the processor signal THERMTRIP# will go active and the system will automatically shut down to prevent any damage to the processor as a result of overheating. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

Note

In order for THERMTRIP# to be able to automatically switch off the system it is necessary to use an ATX style power supply.

6.3.2 Processor Performance Control

Intel® Core™ i7/i5/i3 and Celeron® processors found on the conga-BM57/BS57/BE57 run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it's not being fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that your power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

6.3.3 Intel® 64

The formerly known Intel® Extended Memory 64 Technology is an enhancement to Intel®'s IA-32 architecture. Intel® 64 is only available on Intel® Core™ i7/i5/i3 and Celeron® processors and is designed to run with newly written 64-bit code and access more than 4GB of memory. Processors with Intel® 64 architecture support 64-bit-capable operating systems from Microsoft, Red Hat and SuSE. Processors running in legacy mode remain fully compatible with today's existing 32-bit applications and operating systems

Platforms with Intel® 64 can be run in three basic ways :

1. **Legacy Mode:** 32-bit operating system and 32-bit applications. In this mode no software changes are required, however the benefits of Intel® 64 are not utilized.

2. **Compatibility Mode:** 64-bit operating system and 32-bit applications. This mode requires all device drivers to be 64-bit. The operating system will see the 64-bit extensions but the 32-bit application will not. Existing 32-bit applications do not need to be recompiled and may or may not benefit from the 64-bit extensions. The application will likely need to be re-certified by the vendor to run on the new 64-bit extended operating system.

3. **64-bit Mode:** 64-bit operating system and 64-bit applications. This usage requires 64-bit device drivers. It also requires applications to be

modified for 64-bit operation and then recompiled and validated.

Intel® 64 provides support for:

- 64-bit flat virtual address space
- 64-bit pointers
- 64-bit wide general purpose registers
- 64-bit integer support
- Up to one Terabyte (TB) of platform address space

You can find more information about Intel® 64 Technology at: http://developer.intel.com/technology/intel64/index.htm

6.3.4 Intel® Virtualization Technology

Virtualization solutions enhanced by Intel® VT will allow a Core™ i7/i5/i3 platform to run multiple operating systems and applications in independent partitions. When using virtualization capabilities, one computer system can function as multiple “virtual” systems. With processor and I/O enhancements to Intel®’s various platforms, Intel® Virtualization Technology can improve the performance and robustness of today’s software-only virtual machine solutions.

Intel® VT is a multi-generational series of extensions to Intel® processor and platform architecture that provides a new hardware foundation for virtualization, establishing a common infrastructure for all classes of Intel® based systems. The broad availability of Intel® VT makes it possible to create entirely new applications for virtualization in servers, clients as well as embedded systems thus providing new ways to improve system reliability, manageability, security, and real-time quality of service.

The success of any new hardware architecture is highly dependent on the system software that puts its new features to use. In the case of virtualization technology, that support comes from the virtual machine monitor (VMM), a layer of software that controls the underlying physical platform resources sharing them between multiple “guest” operating systems. Intel® VT is already incorporated into most commercial and open-source VMMs including those from VMware, Microsoft, XenSource, Parallels, Virtual Iron, Jaluna and TenAsys.

You can find more information about Intel Virtualization Technology at: http://developer.intel.com/technology/virtualization/index.htm

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

6.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-BM57/BS57/BE57 ACPI thermal solution offers three different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (4°C hysteresis).

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled according to the formula below.

$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

- *ΔP is the performance delta*
- *T_t is the target temperature = critical trip point*

- *The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants. These constants are set to fixed values for the conga-BM57/BS57/BE57:*
- *TC1= 1*
- *TC2= 5*
- *TSP= 5 seconds*

See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

6.5 ACPI Suspend Modes and Resume Events

conga-BM57/BS57/BE57 supports S3 (STR= Suspend to RAM). For more information about S3 wake events see section 9.4.1 “ACPI Configuration Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Windows 7, Windows Vista, Linux, Windows XP and Windows 2K

This table lists the “Wake Events” that resume the system from S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S3-S5.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event. USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). Under Windows XP add following registry entries: Add this key: HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\usb Under this key add the following value: “USBBIOSx“=DWORD:00000000 *Note that Windows XP disables USB wakeup from S3, so this entry has to be added to re-enable it.* Configure USB keyboard/mouse to be able to wake up the system: In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check ‘Allow this device to bring the computer out of standby’. *Note: When the standby state is set to S3 in the ACPI setup menu, the power management tab for USB keyboard /mouse devices only becomes available after adding the above registry entry and rebooting to allow the registry changes to take affect.*
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

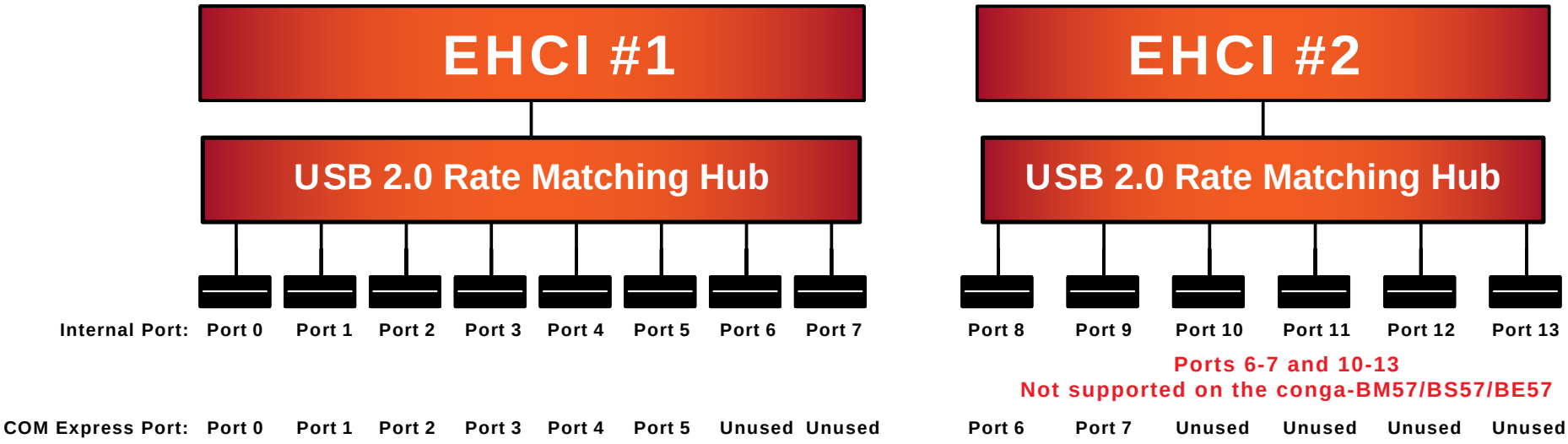
Note

The above list has been verified using a Windows XP SP3 ACPI enabled installation.

6.6 USB 2.0 EHCI Host Controller Support

The 8 available USB ports are provided by two USB 2.0 Rate Matching Hubs (RMH) integrated within the Intel® BD82HM55 (HM55) PCH. Each EHCI controller has one hub connected to it as shown below. The Hubs convert low and full-speed traffic into high-speed traffic. When the RMHs are enabled, they will appear to software like an external hub is connected to Port 0 of each EHCI controller. In addition, port 1 of each of the RMHs is muxed with Port 1 of the EHCI controllers and is able to bypass the RMH for use as the Debug Port. The hub operates like any USB 2.0 Discrete Hub and will consume one tier of hubs allowed by the USB 2.0 Spec. A maximum of four additional non-root hubs can be supported on any of the PCH USB Ports. The RMH will report the following Vendor ID = 8087h and Product ID = 0020h.

Routing Diagram



7 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type II connectors used for congatec AG modules. The pinout of the modules complies with COM Express Type 2 Rev. 1.0 and have the ability to be optionally compliant with COM Express Type 2.0 Rev. 2.0.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip’s datasheet.

Table 2 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0
PEG	PCI Express Graphics
SATA	In compliance with Serial ATA specification, Revision 1.0a
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

7.1 A-B Connector Signal Descriptions

Table 3 Intel® High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC_RST#	A30	**Intel® High Definition Audio Reset:** This signal is the master hardware reset to external codec(s).	O 3.3V		AC'97 codecs are not supported.
AC_SYNC	A29	**Intel® High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		AC'97 codecs are not supported. AC_SYNC is a boot strap signal (see note below)
AC_BITCLK	A32	**Intel® High Definition Audio Bit Clock Output:** This signal is a 24.000MHz serial data clock generated by the Intel® High Definition Audio controller (the Intel® BD82HM55 PCH). This signal has an Intel® integrated pull-down resistor so that AC_BIT_CLK doesn't float when an Intel® High Definition Audio codec (or no codec) is connected but the signals are temporarily configured as AC '97.	I 3.3V O 3.3V		AC'97 codecs are not supported.
AC_SDOUT	A33	**Intel® High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3V		AC'97 codecs are not supported. AC_SDOUT is a boot strap signal (see note below)
AC_SDIN[2:0]	B28-B30	**Intel® High Definition Audio Serial Data In [0]:** These signals are serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	I 3.3V		AC'97 codecs are not supported.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module.

For more information refer to section 7.5 of this user's guide.

Table 4 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 / 100 / 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.			Not connected

Note

The GBE0_LINK# output is only active during a 100Mbit or 1Gbit connection, it is not active during a 10Mbit connection. This is a limitation of Ethernet controller since it only has 3 LED outputs, ACT#, LINK100# and LINK1000#. The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-BM/BS/BE57 module.

Table 5 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a. Serial ATA channel 3 is used for SATA to PATA conversion and therefore not available.

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a. Serial ATA channel 3 is used for SATA to PATA conversion and therefore not available.
ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	OC 3.3V		

Table 6 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Not available. Used by onboard Gigabit Ethernet.
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Not available. Used by onboard Gigabit Ethernet.
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		

Table 7 ExpressCard Support Pins Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request.	I 3.3V	PU 10k 3.3V	
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3V	PU 10k 3.3V	

Table 8 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V		
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3V	PU 10k 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		

Table 9 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

Table 10 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O 5V	PU 2k2 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/O 5V	PU 2k2 3.3V	

Table 11 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10k	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V		
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	LVDS_I2C_DAT is a boot strap signal (see note below).

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module.

For more information refer to section 7.5 of this user's guide.

Table 12 TV-Out Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TV_DAC_A	B97	TVDAC Channel A Output supports the following: Composite video: CVBS Component video: Chrominance (Pb) analog signal S-Video: not used	O Analog		Analog output Not supported
TV_DAC_B	B98	TVDAC Channel B Output supports the following: Composite video: not used Component video: Luminance (Y) analog signal. S-Video: Luminance analog signal.	O Analog		Analog output Not supported
TV_DAC_C	B99	TVDAC Channel C Output supports the following: Composite video: not used Component: Chrominance (Pr) analog signal. S-Video: Chrominance analog signal.	O Analog		Analog output Not supported

Table 13 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O 3.3V	PU 4k7 3.3V	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O 3.3V	PU 4k7 3.3V	
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		SPEAKER is a boot strap signal (see note below)
BIOS_DISABLE#	A34	Module BIOS disable input. Pull low to disable module BIOS. Used to allow off-module BIOS implementations.	I 3.3V	PU 10k 3.3V	
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PU 10k 3.3V	
KBD_RST#	A86	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.	I	PU 10k 3.3V	
KBD_A20GATE	A87	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled low on the module.	I	PU 10k 3.3V	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user’s guide.

Table 14 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3VSB	PU 1k 3.3VSB	GPO[0] is a boot strap signal (see note below).
GPO[1]	B54	General purpose output pins.	O 3.3VSB	PU 10k 3.3VSB	
GPO[2]	B57	General purpose output pins.	O 3.3VSB	PD 10k	
GPO[3]	B63	General purpose output pins.	O 3.3VSB	PD 10k	
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3VSB	PU 10k 3.3VSB	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3VSB	PU 10k 3.3VSB	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3VSB	PU 10k 3.3VSB	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3VSB	PU 10k 3.3VSB	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user's guide.

Table 15 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on rising edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V	PD 100k	
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V		Set by resistor divider to accept 3.3V.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB	PU 10k 3.3VSB	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		Not supported
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10k 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 10k 3.3V	
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10k 3.3V	
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	I/O 3.3VSB	PU 2k2 3.3VSB	

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	I/O 3.3VSB	PU 2k2 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	I 3.3VSB	PU 10k 3.3VSB	

Table 16 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A66, A80, A90, A96, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

7.2 A-B Connector Pinout

Table 17 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4# (*)	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+	B22	SATA3_TX+	A77	LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX-	B23	SATA3_TX-	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+	B25	SATA3_RX+	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX-	B26	SATA3_RX-	A81	LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK-
A28	ATA_ACT#	B28	AC_SDIN2	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC_SYNC	B29	AC_SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC_RST#	B30	AC_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	KBD_RST#	B86	VCC_5V_SBY
A32	AC_BITCLK	B32	SPKR	A87	KBD_A20GATE	B87	VCC_5V_SBY
A33	AC_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	RSVD
A34	BIOS_DISABLE#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	RSVD	B91	VGA_GRN
A37	USB6+	B37	USB7+	A92	RSVD	B92	VGA_BLU

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC
A39	USB4-	B39	USB5-	A94	RSVD	B94	VGA_VSYNC
A40	USB4+	B40	USB5+	A95	RSVD	B95	VGA_I2C_CK
A41	GND (FIXED)	B41	GND (FIXED)	A96	GND	B96	VGA_I2C_DAT
A42	USB2-	B42	USB3-	A97	RSVD	B97	TV_DAC_A (*)
A43	USB2+	B43	USB3+	A98	RSVD	B98	TV_DAC_B (*)
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	RSVD	B99	TV_DAC_C (*)
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	RSVD	B101	RSVD
A47	VCC_RTC	B47	EXCD1_PERST#	A102	RSVD	B102	RSVD
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	RSVD	B103	RSVD
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-BM57/BS57/BE57. PCIE_TX5± and PCIE_RX5± are used for the onboard Gigabit Ethernet and therefore are not available externally. SATA3_TX+, SATA3_TX-, SATA3_RX+, and SATA3_RX- are used for SATA to PATA conversion and therefore not available externally.

7.3 C-D Connector Signal Descriptions

Table 18 PCI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCI_AD[0, 2, 4, 6, 8, 10, 12] PCI_AD[1, 3, 5, 7] PCI_AD[9, 11, 13, 15] PCI_AD14 PCI_AD[16, 18, 20, 22] PCI_AD[17, 19] PCI_AD[21, 23] PCI_AD[24, 26, 28, 30] PCI_AD[25, 27, 29, 31]	C24-C30 D22-D25 D27-D30 C32 D37-D40 C39-C40 C42-C43 D42-D45 C45-C48	PCI bus multiplexed address and data lines	I/O 3.3V		
PCI_C/BE0# PCI_C/BE1# PCI_C/BE2# PCI_C/BE3#	D26 C33 C38 C44	PCI bus byte enable lines, active low	I/O 3.3V		
PCI_DEVSEL#	C36	PCI bus Device Select, active low.	I/O 3.3V	PU 8k2 3.3V	
PCI_FRAME#	D36	PCI bus Frame control line, active low.	I/O 3.3V	PU 8k2 3.3V	
PCI_IRDY#	C37	PCI bus Initiator Ready control line, active low.	I/O 3.3V	PU 8k2 3.3V	
PCI_TRDY#	D35	PCI bus Target Ready control line, active low.	I/O 3.3V	PU 8k2 3.3V	
PCI_STOP#	D34	PCI bus STOP control line, active low, driven by cycle initiator.	I/O 3.3V	PU 8k2 3.3V	
PCI_PAR	D32	PCI bus parity	I/O 3.3V		
PCI_PERR#	C34	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.	I/O 3.3V	PU 8k2 3.3V	
PCI_REQ0# PCI_REQ1# PCI_REQ2# PCI_REQ3#	C22 C19 C17 D20	PCI bus master request input lines, active low.	I 3.3V	PU 8k2 3.3V	
PCI_GNT0# PCI_GNT1# PCI_GNT2# PCI_GNT3#	C20 C18 C16 D19	PCI bus master grant output lines, active low.	O 3.3V		PCI_GNT[0..3]# are boot strap signals (see note below)
PCI_RESET#	C23	PCI Reset output, active low.	O 3.3V		
PCI_LOCK#	C35	PCI Lock control line, active low.	I/O 3.3V	PU 8k2 3.3V	
PCI_SERR#	D33	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition.	I/O 3.3V	PU 8k2 3.3V	
PCI_PME#	C15	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.	I 3.3VSB		

Signal	Pin #	Description	I/O	PU/PD	Comment
PCI_CLKRUN#	D48	Bidirectional pin used to support PCI clock run protocol for mobile systems.	I/O 3.3V	PU 10k 3.3V	
PCI_IRQA# PCI_IRQB# PCI_IRQC# PCI_IRQD#	C49 C50 D46 D47	PCI interrupt request lines.	I 3.3V	PU 8k2 3.3V	
PCI_CLK	D50	PCI 33MHz clock output.	O 3.3V		
PCI_M66EN	D49	Module input signal indicates whether an off-module PCI device is capable of 66MHz operation. Pulled to GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66MHz operation. If the module is not capable of supporting 66MHz PCI operation, this input may be a no-connect on the module. If the module is capable of supporting 66MHz PCI operation, and if this input is held low by the Carrier Board, the module PCI interface shall operate at 33MHz.	I		Not connected

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user's guide.

The PCI interface is specified to be +5V tolerant, with +3.3V signaling.

Table 19 IDE Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
IDE_D0 IDE_D1 IDE_D2 IDE_D3 IDE_D4 IDE_D5 IDE_D6 IDE_D7 IDE_D8 IDE_D9 IDE_D10 IDE_D11 IDE_D12 IDE_D13 IDE_D14 IDE_D15	D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5	Bidirectional data to / from IDE device.	I/O 3.3V	IDE_D7 PD 10k	
IDE_A[0.2]	D13-D15	Address lines to IDE device.	O 3.3V		
IDE_IOW#	D9	I/O write line to IDE device. Data latched on trailing (rising) edge.	O 3.3V		
IDE_IOR#	C14	I/O read line to IDE device.	O 3.3V		
IDE_REQ	D8	IDE Device DMA Request. It is asserted by the IDE device to request a data transfer.	I 3.3V	PD 5k1	
IDE_ACK#	D10	IDE Device DMA Acknowledge.	O 3.3V		
IDE_CS1#	D16	IDE Device Chip Select for 1F0h to 1FFh range.	O 3.3V		
IDE_CS3#	D17	IDE Device Chip Select for 3F0h to 3FFh range.	O 3.3V		
IDE_IORDY	C13	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.	I 3.3V	PU 4k7 3.3V	
IDE_RESET#	D18	Reset output to IDE device, active low.	O 3.3V		
IDE_IRQ	D12	Interrupt request from IDE device.	I 3.3V	PD 10k	
IDE_CBLID#	D77	Input from off-module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 and 133 modes.	I 3.3V	PD 1k	

Note

The PATA (IDE) interface is an option conga-BM57/BS57/BE57. When this option is used, Serial ATA channel 3 is not available.

Table 20 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs. Some of these lines are multiplexed with SDVO lines. *Note: Can also be used as PCI Express Receive Input differential pairs 16 through 31 known as PCIE_RX[16-31] + and -.*	I PCIE		PCI Express Graphics (PEG) is not supported on the conga-BM57/BS57/BE57 (see note below).
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+	D52	PCI Express Graphics Transmit Output differential pairs. Some of these lines are multiplexed with SDVO lines. *Note: Can also be used as PCI Express Transmit Output differential pairs 16 through 31 known as PCIE_TX[16-31] + and -.*	O PCIE		
PEG_TX0-	D53				
PEG_TX1+	D55				
PEG_TX1-	D56				
PEG_TX2+	D58				
PEG_TX2-	D59				
PEG_TX3+	D61				
PEG_TX3-	D62				
PEG_TX4+	D65				
PEG_TX4-	D66				
PEG_TX5+	D68				
PEG_TX5-	D69				
PEG_TX6+	D71				
PEG_TX6-	D72				
PEG_TX7+	D74				
PEG_TX7-	D75				
PEG_TX8+	D78				
PEG_TX8-	D79				
PEG_TX9+	D81				
PEG_TX9-	D82				
PEG_TX10+	D85				
PEG_TX10-	D86				
PEG_TX11+	D88				
PEG_TX11-	D89				
PEG_TX12+	D91				
PEG_TX12-	D92				
PEG_TX13+	D94				
PEG_TX13-	D95				
PEG_TX14+	D98				
PEG_TX14-	D99				
PEG_TX15+	D101				
PEG_TX15-	D102				
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I 1.05V		Not supported
PEG_ENABLE#	D97	Strap to enable PCI Express x16 external graphics interface.	I 3.3V	PU 10k 3.3V	Not supported

Note

The PCI Express Graphics (PEG) signals are multiplexed with HDMI, DisplayPort (DP) and SDVO. The signals for these interfaces are routed to the PEG interface of the COM Express connector. Refer to the SDVO, HDMI and DiplayPort signal description tables in this section for information about the signals routed to the PEG interface of the COM Express connector.

Table 21 SDVO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDVOB_RED+ SDVOB_RED-	D52 D53	Serial Digital Video B red output differential pair. Multiplexed with PEG_TX[0]+ and PEG_TX[0]- pair.	O PCIE		
SDVOB_GRN+ SDVOB_GRN-	D55 D56	Serial Digital Video B green output differential pair. Multiplexed with PEG_TX[1]+ and PEG_TX[1]-.	O PCIE		
SDVOB_BLU+ SDVOB_BLU-	D58 D59	Serial Digital Video B blue output differential pair. Multiplexed with PEG_TX[2]+ and PEG_TX[2]-.	O PCIE		
SDVOB_CK+ SDVOB_CK-	D61 D62	Serial Digital Video B clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]-.	O PCIE		
SDVOB_INT+ SDVOB_INT-	C55 C56	Serial Digital Video B interrupt input differential pair. Multiplexed with PEG_RX[1]+ and PEG_RX[1]-.	I PCIE		
SDVOC_RED+ SDVOC_RED-	D65 D66	Serial Digital Video C red output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]-.	O PCIE		Not supported
SDVOC_GRN+ SDVOC_GRN-	D68 D69	Serial Digital Video C green output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]-.	O PCIE		Not supported
SDVOC_BLU+ SDVOC_BLU-	D71 D72	Serial Digital Video C blue output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]-.	O PCIE		Not supported
SDVOC_CK+ SDVOC_CK-	D74 D75	Serial Digital Video C clock output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]-.	O PCIE		Not supported
SDVOC_INT+ SDVOC_INT-	C68 C69	Serial Digital Video C interrupt input differential pair. Multiplexed with PEG_RX[5]+ and PEG_RX[5]-.	I PCIE		Not supported
SDVO_TVCLKIN+ SDVO_TVCLKIN-	C52 C53	Serial Digital Video TVOUT synchronization clock input differential pair. Multiplexed with PEG_RX[0]+ and PEG_RX[0]-.	I PCIE		
SDVO_FLDSTALL+ SDVO_FLDSTALL-	C58 C59	Serial Digital Video Field Stall input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]-.	I PCIE		Standard variants of conga-BM57/BS57/BE57 do not support the SDVO_FLDSTALL+ and SDVO_FLDSTALL- signal pair (see note below).
SDVO_I2C_CK (SDVO_CLK)	D73	SDVO I²C clock line to set up SDVO peripherals.	O 3.3V		
SDVO_I2C_DAT (SDVO_DATA)	C73	SDVO I²C data line to set up SDVO peripherals.	I/O OD 2.5V		SDVO_I2C_DAT is a boot strap signal (see note below)

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user's guide.

The standard variants of conga-BM57/BS57/BE57 do not support the SDVO FIELD_STALL signal pair on digital display port B. By default, the signals DPB_AUX+ (PEG_RX[2]+) and DPB_AUX- (PEG_RX[2]-) are routed to the PCI Express Graphics (PEG) interface of the COM Express connector instead of SDVO_FLDSTALL+ and SDVO_FLDSTALL-.

If the SDVO FIELD_STALL signal pair is required, contact congatec technical support.

Table 22 HDMI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS_B_CLK + TMDS_B_CLK -	D61 D62	HDMI Port B Clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]- pair.	O PCIE		
TMDS_B_DATA0+ TMDS_B_DATA0-	D58 D59	HDMI Port B Data0 output differential pair. Multiplexed with PEG_TX[2]+ and PEG_TX[2]-.	O PCIE		
TMDS_B_DATA1+ TMDS_B_DATA1-	D55 D56	HDMI Port B Data1 output differential pair. Multiplexed with PEG_TX[1]+ and PEG_TX[1]-.	O PCIE		
TMDS_B_DATA2+ TMDS_B_DATA2-	D52 D53	HDMI Port B Data2 output differential pair. Multiplexed with PEG_TX[0]+ and PEG_TX[0]-.	O PCIE		
TMDS_B_HPD	C61	HDMI Port B Hot-plug detect. Multiplexed with PEG_RX[3]+.	I PCIE		
DDPB_CTRLCLK	D73	HDMI port B Control Clock	I/O OD 3.3V		This signal is multiplexed with SDVO_I2C_CK (SDVO_CLK)
DDPB_CTRLDATA	C73	HDMI port B Control Data	I/O OD 3.3V		This signal is multiplexed with SDVO_I2C_DAT (SDVO_DATA) DDPB_CTRLDATA is a boot strap signal (see note below)
TMDS_C_CLK + TMDS_C_CLK -	D74 D75	HDMI Port C Clock output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]- pair.	O PCIE		
TMDS_C_DATA0+ TMDS_C_DATA0-	D71 D72	HDMI Port C Data0 output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]-.	O PCIE		
TMDS_C_DATA1+ TMDS_C_DATA1-	D68 D69	HDMI Port C Data1 output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]-.	O PCIE		
TMDS_C_DATA2+ TMDS_C_DATA2-	D65 D66	HDMI Port C Data2 output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]-.	O PCIE		
TMDS_C_HPD	C74	HDMI Port C Hot-plug detect. Multiplexed with PEG_RX[7]+.	I PCIE		
DDPC_CTRLCLK	D63	HDMI port C Control Clock	I/O OD 3.3V		This signal is not supported by COM Express standard but is mandatory to support the HDMI interface on conga-BM57/BS57/BE57. Therefore congatec has used the reserved (RSVD) pin D63 for this signal.
DDPC_CTRLDATA	D64	HDMI port C Control Data	I/O OD 3.3V		This signal is not supported by COM Express standard but is mandatory to support the HDMI interface on conga-BM57/BS57/BE57. Therefore congatec has used the reserved (RSVD) pin D64 for this signal. DDPC_CTRLDATA is a boot strap signal (see note below)
TMDS_D_CLK + TMDS_D_CLK -	D88 D89	HDMI Port D Clock output differential pair. Multiplexed with PEG_TX[11]+ and PEG_TX[11]- pair.	O PCIE		
TMDS_D_DATA0+ TMDS_D_DATA0-	D85 D86	HDMI Port D Data0 output differential pair. Multiplexed with PEG_TX[10]+ and PEG_TX[10]-.	O PCIE		
TMDS_D_DATA1+ TMDS_D_DATA1-	D81 D82	HDMI Port D Data1 output differential pair. Multiplexed with PEG_TX[9]+ and PEG_TX[9]-.	O PCIE		
TMDS_D_DATA2+ TMDS_D_DATA2-	D78 D79	HDMI Port D Data2 output differential pair. Multiplexed with PEG_TX[8]+ and PEG_TX[8]-.	O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS_D_HPD	C88	HDMI Port C Hot-plug detect. Multiplexed with PEG_RX[11]+.	I PCIE		
DDPD_CTRLCLK	C97	HDMI port D Control Clock	I/O OD 3.3V		This signal is not supported by COM Express standard but is mandatory to support the HDMI interface on conga-BM57/BS57/BE57. Therefore congatec has used the reserved (RSVD) pin C97 for this signal.
DDPD_CTRLDATA	D83	HDMI port D Control Data	I/O OD 3.3V		This signal is not supported by COM Express standard but is mandatory to support the HDMI interface on conga-BM57/BS57/BE57. Therefore congatec has used the reserved (RSVD) pin D83 for this signal. DDPD_CTRLDATA is a boot strap signal (see note below)

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user's guide.

Table 23 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DPB_LANE3+ DPB_LANE3-	D61 D62	DisplayPort B Lane3 output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]- pair.	O PCIE		
DPB_LANE2+ DPB_LANE2-	D58 D59	DisplayPort B Lane2 output differential pair. Multiplexed with PEG_TX[2]+ and PEG_TX[2]- pair.	O PCIE		
DPB_LANE1+ DPB_LANE1-	D55 D56	DisplayPort B Lane1 output differential pair. Multiplexed with PEG_TX[1]+ and PEG_TX[1]- pair.	O PCIE		
DPB_LANE0+ DPB_LANE0-	D52 D53	DisplayPort B Lane0 output differential pair. Multiplexed with PEG_TX[0]+ and PEG_TX[0]- pair.	O PCIE		
DPB_HPD	C61	DisplayPort B Hot-plug detect. Multiplexed with PEG_RX[3]+.	I PCIE		
DPB_AUX+ DPB_AUX-	C58 C59	DisplayPort B Aux input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]- pair.	I PCIE		
DDPB_CTRLDATA	C73	Digital Display port B Control Data	I/O OD 3.3V		This signal is multiplexed with SDVO_I2C_DAT (SDVO_DATA). This signal is not used on the DisplayPort interface but it must be used to enable the DisplayPort interface. DDPB_CTRLDATA is a boot strap signal (see note below)
DPC_LANE3+ DPC_LANE3-	D74 D75	DisplayPort C Lane3 output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]- pair.	O PCIE		
DPC_LANE2+ DPC_LANE2-	D71 D72	DisplayPort C Lane2 output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]- pair.	O PCIE		
DPC_LANE1+ DPC_LANE1-	D68 D69	DisplayPort C Lane1 output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]- pair.	O PCIE		
DPC_LANE0+ DPC_LANE0-	D65 D66	DisplayPort C Lane0 output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]- pair.	O PCIE		
DPC_HPD	C74	DisplayPort C Hot-plug detect. Multiplexed with PEG_RX[7]+.	I PCIE		
DPC_AUX+ DPC_AUX-	C71 C72	DisplayPort C Aux input differential pair. Multiplexed with PEG_RX[6]+ and PEG_RX[6]- pair.	I PCIE		
DDPC_CTRLDATA	D64	Digital Display port C Control Data	I/O OD 3.3V		This signal is not supported by COM Express standard but is mandatory to support the DisplayPort interface on conga-BM57/BS57/BE57. Therefore congatec has used the reserved (RSVD) pin D64 for this signal. This signal is not used on the DisplayPort interface but it must be used to enable the DisplayPort interface. DDPC_CTRLDATA is a boot strap signal (see note below)
DPD_LANE3+ DPD_LANE3-	D88 D89	DisplayPort D Lane3 output differential pair. Multiplexed with PEG_TX[11]+ and PEG_TX[11]- pair.	O PCIE		
DPD_LANE2+ DPD_LANE2-	D85 D86	DisplayPort D Lane2 output differential pair. Multiplexed with PEG_TX[10]+ and PEG_TX[10]- pair.	O PCIE		
DPD_LANE1+ DPD_LANE1-	D81 D82	DisplayPort D Lane1 output differential pair. Multiplexed with PEG_TX[9]+ and PEG_TX[9]- pair.	O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
DPD_LANE0+ DPD_LANE0-	D78 D79	DisplayPort D Lane0 output differential pair. Multiplexed with PEG_TX[8]+ and PEG_TX[8]- pair.	O PCIE		
DPD_HPD	C88	DisplayPort D Hot-plug detect. Multiplexed with PEG_RX[11]+.	I PCIE		
DPD_AUX+ DPD_AUX-	C85 C86	DisplayPort D Aux input differential pair. Multiplexed with PEG_RX[10]+ and PEG_RX[10]- pair.	I PCIE		
DDPD_CTRLDATA	D83	Digital Display port C Control Data	I/O OD 3.3V		This signal is not supported by COM Express standard but is mandatory to support the DisplayPort interface on conga-BM57/BS57/BE57. Therefore congatec has used the reserved (RSVD) pin D83 for this signal. This signal is not used on the DisplayPort interface but it must be used to enable the DisplayPort interface. DDPD_CTRLDATA is a boot strap signal (see note below)

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user's guide.

Table 24 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pinout Type 1 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 (no IDE) NC GND NC Pinout Type 4 (no PCI) NC GND GND Pinout Type 5 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.	PDS	TYPE[0:2]# signals are available on all modules following the Type 2-5 Pinout standard. The conga-BM57/BS57/ BE57 is based on the COM Express Type 2 pinout therefore these pins are not connected.

Table 25 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
GND	C1, C11, C21, C31, C41, C51, C60, C70, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D11, D21, D31, D41, D51, D60, D67, D70, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

Table 26 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT	C67	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD		
FAN_TACHOIN	C77	Fan tachometer input.	I OD		Requires a fan with a two pulse output.
PP_TPM	C83	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V		Trusted Platform Module chip is optional.

7.4 C-D Connector Pinout

Table 27 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1-	D56	PEG_TX1-
C2	IDE_D7	D2	IDE_D5	C57	TYPE1#	D57	TYPE2#
C3	IDE_D6	D3	IDE_D10	C58	PEG_RX2+	D58	PEG_TX2+
C4	IDE_D3	D4	IDE_D11	C59	PEG_RX2-	D59	PEG_TX2-
C5	IDE_D15	D5	IDE_D12	C60	GND (FIXED)	D60	GND (FIXED)
C6	IDE_D8	D6	IDE_D4	C61	PEG_RX3+	D61	PEG_TX3+
C7	IDE_D9	D7	IDE_D0	C62	PEG_RX3- (*)	D62	PEG_TX3-
C8	IDE_D2	D8	IDE_REQ	C63	RSVD	D63	DDPC_CTRLCLK
C9	IDE_D13	D9	IDE_IOW#	C64	RSVD	D64	DDPC_CTRLDATA
C10	IDE_D1	D10	IDE_ACK#	C65	PEG_RX4+ (*)	D65	PEG_TX4+
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4- (*)	D66	PEG_TX4-
C12	IDE_D14	D12	IDE_IRQ	C67	FAN_PWMOUT	D67	GND
C13	IDE_IORDY	D13	IDE_A0	C68	PEG_RX5+ (*)	D68	PEG_TX5+
C14	IDE_IOR#	D14	IDE_A1	C69	PEG_RX5- (*)	D69	PEG_TX5-
C15	PCI_PME#	D15	IDE_A2	C70	GND (FIXED)	D70	GND (FIXED)
C16	PCI_GNT2#	D16	IDE_CS1#	C71	PEG_RX6+	D71	PEG_TX6+
C17	PCI_REQ2#	D17	IDE_CS3#	C72	PEG_RX6-	D72	PEG_TX6-
C18	PCI_GNT1#	D18	IDE_RESET#	C73	SDVO_DATA	D73	SVDO_CLK
C19	PCI_REQ1#	D19	PCI_GNT3#	C74	PEG_RX7+	D74	PEG_TX7+
C20	PCI_GNT0#	D20	PCI_REQ3#	C75	PEG_RX7- (*)	D75	PEG_TX7-
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCI_REQ0#	D22	PCI_AD1	C77	FAN_TACHOIN	D77	IDE_CBLID#
C23	PCI_RESET#	D23	PCI_AD3	C78	PEG_RX8+ (*)	D78	PEG_TX8+
C24	PCI_AD0	D24	PCI_AD5	C79	PEG_RX8- (*)	D79	PEG_TX8-
C25	PCI_AD2	D25	PCI_AD7	C80	GND (FIXED)	D80	GND (FIXED)
C26	PCI_AD4	D26	PCI_C/BE0#	C81	PEG_RX9+ (*)	D81	PEG_TX9+
C27	PCI_AD6	D27	PCI_AD9	C82	PEG_RX9- (*)	D82	PEG_TX9-
C28	PCI_AD8	D28	PCI_AD11	C83	PP_TPM	D83	DDPD_CTRLDATA
C29	PCI_AD10	D29	PCI_AD13	C84	GND	D84	GND
C30	PCI_AD12	D30	PCI_AD15	C85	PEG_RX10+	D85	PEG_TX10+
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10-	D86	PEG_TX10-
C32	PCI_AD14	D32	PCI_PAR	C87	GND	D87	GND
C33	PCI_C/BE1#	D33	PCI_SERR#	C88	PEG_RX11+	D88	PEG_TX11+
C34	PCI_PERR#	D34	PCI_STOP#	C89	PEG_RX11-(*)	D89	PEG_TX11-
C35	PCI_LOCK#	D35	PCI_TRDY#	C90	GND (FIXED)	D90	GND (FIXED)
C36	PCI_DEVSEL#	D36	PCI_FRAME#	C91	PEG_RX12+ (*)	D91	PEG_TX12+ (*)
C37	PCI_IRDY#	D37	PCI_AD16	C92	PEG_RX12- (*)	D92	PEG_TX12- (*)

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C38	PCI_C/BE2#	D38	PCI_AD18	C93	GND	D93	GND
C39	PCI_AD17	D39	PCI_AD20	C94	PEG_RX13+ (*)	D94	PEG_TX13+ (*)
C40	PCI_AD19	D40	PCI_AD22	C95	PEG_RX13- (*)	D95	PEG_TX13- (*)
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	PCI_AD21	D42	PCI_AD24	C97	DDPD_CTRLCLK	D97	PEG_ENABLE#
C43	PCI_AD23	D43	PCI_AD26	C98	PEG_RX14+ (*)	D98	PEG_TX14+ (*)
C44	PCI_C/BE3#	D44	PCI_AD28	C99	PEG_RX14- (*)	D99	PEG_TX14- (*)
C45	PCI_AD25	D45	PCI_AD30	C100	GND (FIXED)	D100	GND (FIXED)
C46	PCI_AD27	D46	PCI_IRQC#	C101	PEG_RX15+ (*)	D101	PEG_TX15+ (*)
C47	PCI_AD29	D47	PCI_IRQD#	C102	PEG_RX15- (*)	D102	PEG_TX15- (*)
C48	PCI_AD31	D48	PCI_CLKRUN#	C103	GND	D103	GND
C49	PCI_IRQA#	D49	PCI_M66EN (*)	C104	VCC_12V	D104	VCC_12V
C50	PCI_IRQB#	D50	PCI_CLK	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+	D52	PEG_TX0+	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0-	D53	PEG_TX0-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV# (*)	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+	D55	PEG_TX1+	C110	GND (FIXED)	D110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-BM57/BS57/BE57.

7.5 Boot Strap Signals

Table 28 Boot Strap Signal Descriptions

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
AC_SYNC	A29	**Intel® High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		AC_SYNC is a boot strap signal (see caution statement below)
AC_SDOUT	A33	**Intel® High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3V		AC_SDOUT is a boot strap signal (see caution statement below)
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	LVDS_I2C_DAT is a boot strap signal (see caution statement below).
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		SPKR is a boot strap signal (see caution statement below)
GPO[0]	A93	General purpose output pins.	O 3.3VSB	PU 1k 3.3VSB	GPO[0] is a boot strap signal (see caution statement below).
SDVO_I2C_DAT (SDVO_DATA) (DDPB_CTRLDATA)	C73	SDVO I²C data line to set up SDVO/HDMI/DisplayPort peripherals.	I/O OD 2.5V		SDVO_I2C_DAT is a boot strap signal (see caution statement below)
PCI_GNT0#	C20	PCI bus master grant output lines, active low.	O 3.3V		PCI_GNT0# is a boot strap signal (see caution statement below)
DDPC_CTRLDATA	D64	Digital Display port C Control Data line to set up HDMI/DisplayPort.	I/O OD 3.3V		DDPC_CTRLDATA is a boot strap signal (see caution statement below)
DDPD_CTRLDATA	D83	Digital Display port C Control Data line to set up HDMI/DisplayPort.	I/O OD 3.3V		DDPD_CTRLDATA is a boot strap signal (see caution statement below)
PCI_GNT1#	C18	PCI bus master grant output lines, active low.	O 3.3V		PCI_GNT1# is a boot strap signal (see caution statement below)
PCI_GNT2#	C16	PCI bus master grant output lines, active low.	O 3.3V		PCI_GNT2# is a boot strap signal (see caution statement below)
PCI_GNT3#	D19	PCI bus master grant output lines, active low.	O 3.3V		PCI_GNT3# is a boot strap signal (see caution statement below)

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either COM Express™ internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table with the exception of SDVO_I2C_DAT, DDPC_CTRLDATA and DDPD_CTRLDATA. External resistors may override the internal strap states and cause the COM Express™ module to malfunction and/or cause irreparable damage to the module.

SDVO_I2C_DAT (DDPB_CTRLDATA) can be pulled-up (using 2.2KΩ resistor) to 3.3V in order to set up SDVO/HDMI/DisplayPort peripherals.

DDPC_CTRLDATA can be pulled-up (using 2.2KΩ resistor) to 3.3V in order to set up HDMI/DisplayPort.

DDPD_CTRLDATA can be pulled-up (using 2.2KΩ resistor) to 3.3V in order to set up HDMI/DisplayPort.

Note

For more information about implementing a HDMI or DisplayPort interface on COM Express™ carrier boards, refer to application note AN17_HDMI_DP_Implementation.pdf, which can be found on the congatec website.

8 System Resources

8.1 System Memory Map

Table 29 Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(TOM-384kB) – TOM	N.A.	384kB	ACPI reclaim, MPS and NVS area
(TOM-128MB-384kB) – (TOM-384kB)	N.A.	32MB up to 128MB	VGA frame buffer
1024kB – (TOM-128MB-384kB)	100000 – N.A	N.A.	Extended memory
869kB – 1024kB	E0000 - FFFFF	128kB	Runtime BIOS
832kB – 869kB	D0000 - DFFFF	64kB	Upper memory
640kB – 832kB	A0000 - CFFFF	192kB	Video memory and BIOS
639kB – 640kB	9FC00 - 9FFFF	1kB	Extended BIOS data
0 – 639kB	00000 - 9FC00	512kB	Conventional memory

Note

T.O.M. = Top of memory = max. DRAM installed

8.2 I/O Address Assignment

The I/O address assignment of the conga-BM57/BS57/BE57 module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

Table 30 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
03B0 – 03DF	16 bytes	No	Video system
04D0 – 04D1	2 bytes	No	Motherboard resources
0500 – 053F	64 bytes	No	Motherboard resources
0800 – 087F	128 bytes	No	Motherboard resources
0A00 – 0A7F	128 bytes	No	Motherboard resources
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
0D00 – FFFF		See note	PCI / PCI Express bus

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

8.2.1 LPC Bus

On the conga-BM57/BS57/BE57 the PCI Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Bus not the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus. In addition to legacy interfaces such as COM port, LPT port and keyboard controller, the I/O range A00h - A0Fh is forwarded to the LPC Bus. the A00h I/O base provides the ability to utilize the hardware monitoring functionality of a carrier board implemented Winbond W83627 Super I/O.

If a Super I/O is not implemented on the carrier board then these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

8.3 Interrupt Request (IRQ) Lines

Table 31 IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		IRQ3 via SERIRQ or PCI BUS INTx
4	Yes		IRQ4 via SERIRQ or PCI BUS INTx
5	Yes		IRQ5 via SERIRQ or PCI BUS INTx
6	Yes		IRQ6 via SERIRQ or PCI BUS INTx
7	Yes		IRQ7 via SERIRQ or PCI BUS INTx
8	No	Real-time Clock	Not applicable
9	No	SCI	Not applicable
10	Yes		IRQ10 via SERIRQ or PCI BUS INTx
11	Yes		IRQ11 via SERIRQ or PCI BUS INTx
12	Yes		IRQ12 via SERIRQ or PCI BUS INTx
13	No	Math processor	Not applicable
14	Yes		PCI BUS INTx
15	Yes		PCI BUS INTx

In PIC mode, the PCI bus interrupt lines can be routed to any free IRQ.

Table 32 IRQ Lines in APIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		IRQ3 via SERIRQ
4	Yes		IRQ4 via SERIRQ
5	Yes		IRQ5 via SERIRQ
6	Yes		IRQ6 via SERIRQ
7	Yes		IRQ7 via SERIRQ
8	No	Real-time Clock	Not applicable
9	No	SCI	SCI
10	Yes		IRQ10 via SERIRQ
11	Yes		IRQ11 via SERIRQ
12	Yes		IRQ12 via SERIRQ
13	No	Math processor	Not applicable
14	Yes		
15	Yes		
16	No		PIRQA, Integrated VGA Controller, PCI Express Root Port 0, PCI Express Root Port 4, EHCI Host Controller 3
17	No		PIRQB, PCI Express Root Port 1
18	No		PIRQC, PCI Express Root Port 2, SMBus Controller
19	No		PIRQD, PCI Express Root Port 3, Serial ATA Host Controller 1, Serial ATA Host Controller 2
20	Yes		PIRQE, PCI Bus INTD, onboard Gigabit LAN Controller
21	Yes		PIRQF, PCI Bus INTA
22	Yes		PIRQG, PCI Bus INTB, Intel High Definition Audio Controller
23	Yes		PIRQH, PCI Bus INTC, EHCI Host Controller 1

In APIC mode, the PCI bus interrupt lines are connected with IRQ 20, 21, 22 and 23.

8.4 PCI Configuration Space Map

Table 33 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	02h	00h	Internal	VGA Graphics
00h	16h	00h	Internal	Intel Management Interface
00h	19h	00h	Internal	Onboard Gigabit LAN Controller
00h	1Ah	00h	Internal	EHCI Host Controller 2
00h	1Bh	00h	Internal	Intel High Definition Audio Controller
00h (see Note 1)	1Ch	00h	Internal	PCI Express Root Port 0
00h (see Note 1)	1Ch	01h	Internal	PCI Express Root Port 1
00h (see Note 1)	1Ch	02h	Internal	PCI Express Root Port 2
00h (see Note 1)	1Ch	03h	Internal	PCI Express Root Port 3
00h (see Note 1)	1Ch	04h	Internal	PCI Express Root Port 4
00h	1Dh	00h	Internal	EHCI Host Controller 1
00h	1Eh	00h	Internal	PCI to PCI Bridge
00h	1Fh	00h	N.A.	PCI to LPC Bridge
00h	1Fh	02h	Internal	Serial ATA Controller 1
00h	1Fh	03h	Internal	SMBus Host Controller
00h	1Fh	05h	Internal	Serial ATA Controller 2
00h	1Fh	06h	Internal	Thermal Subsystem
01h (see Note 2)	00h	00h	Internal	PCI Express Port 0
02h (see Note 2)	00h	00h	Internal	PCI Express Port 1
03h (see Note 2)	00h	00h	Internal	PCI Express Port 2
04h (see Note 2)	00h	00h	Internal	PCI Express Port 3
05h (see Note 2)	00h	00h	Internal	PCI Express Port 4
06h (see Note 2)	04h	00h	INTA-INTD	PCI Bus Slot 1
06h (see Note 2)	05h	00h	INTA-INTD	PCI Bus Slot 2
06h (see Note 2)	06h	00h	INTA-INTD	PCI Bus Slot 3
06h (see Note 2)	07h	00h	INTA-INTD	PCI Bus Slot 4
3fh	00h	00h	N.A.	Chipset Configuration Registers
3fh	00h	01h	N.A.	Chipset Configuration Registers
3fh	02h	00h	N.A.	Chipset Configuration Registers
3fh	02h	01h	N.A.	Chipset Configuration Registers
3fh	02h	02h	N.A.	Intel reserved
3fh	02h	03h	N.A.	Intel reserved

Note

1. The PCI Express Ports are only visible if the PCI Express Port is set to “Auto” in the BIOS setup program and a device is attached to the

corresponding PCI Express port on the carrier board.

2. *The above table represents a case when a single function PCI/PCIe device is connected to all possible slots on carrier board. The given bus numbers will change based on the actual configuration of the hardware .*

8.5 PCI Interrupt Routing Map

Table 34 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line [1]	APIC Mode IRQ	VGA	HDA	EHCI 1	EHCI 2	SMBus	LAN	SATA1	SATA2	PCI-EX Root Port 0	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	PCI-EX Root Port 4	PCI-EX Port 0	PCI-EX Port 1	PCI-EX Port 2	PCI-EX Port 3	PCI-EX Port 4
A		16	x			x					x				x	x [2]	x [5]	x [4]	x [3]	x [2]
B		17										x				x [3]	x [2]	x [5]	x [4]	x [3]
C		18					x						x			x [4]	x [3]	x [2]	x [5]	x [4]
D		19							x	x				x		x [5]	x [4]	x [3]	x [2]	x [5]
E	INTD	20						x												
F	INTA	21																		
G	INTB	22		x																
H	INTC	23			x															

Note

[1] *These interrupts are available for external devices/slots via the C-D connector rows.*

[2] *Interrupt used by single function PCI Express devices (INTA).*

[3] *Interrupt used by multifunction PCI Express devices (INTB).*

[4] *Interrupt used by multifunction PCI Express devices (INTC).*

[5] *Interrupt used by multifunction PCI Express devices (INTD).*

8.6 PCI Bus Masters

The conga-BM57/BS57/BE57 supports 4 external PCI Bus Masters. There are no limitations in connecting bus master PCI devices.

Note

If there are two devices connected to the same PCI REQ/GNT pair and they are transferring data at the same time then the latency time of these shared PCI devices can not be guaranteed.

8.7 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

8.8 SM Bus

System Management (SM) bus signals are connected to the Intel® BD82HM55 (HM55) PCH and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

9 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

9.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> or <F2> key during POST.

9.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used, a selection will be displayed immediately after POST allowing the operator to select either the boot device that should be used or an option to enter the BIOS setup program.

9.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

Main	Advanced	Boot	Security	Save & Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2	Load previous settings.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

9.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
Main BIOS Version	no option	Displays the main BOIS version.
OEM BIOS Version	no option	Displays the additional OEM BIOS version.
Build Date	no option	Displays the date the BIOS was built.
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
Running Time	no option	Displays the time the board is running [in hours max. 65535].
► Platform Information	submenu	Opens the Platform Information submenu
System Date	Day of the week, month/day/year	Specifies the current system date *Note: The date is in month/day/year format.*
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24 hour format.*

9.3.1 Platform Information

The Platform Information submenu offers additional hardware and software information.

Feature	Options	Description
Processor Type	no option	Displays the processor ID string.
Processor Speed	no option	Displays the processor speed.
Processor Stepping	no option	Displays the processor stepping.
Microcode Revision	no option	Displays the processor microcode revision.
Processor Core	no option	Displays the number of processor cores.
IGD VBIOS Version	no option	Displays the video BIOS version.
GMCH Version	no option	Displays the version of the memory and graphics controller hub.
Total Memory	no option	Displays the total amount of installed memory.
Memory Slot0	no option	Displays the amount of installed memory in the top memory slot.
Memory Slot2	no option	Displays the amount of installed memory in the bottom memory slot.
PCH Version	no option	Displays the version of the platform controller hub.
ME FW Version	no option	Displays the version of the integrated Intel management engine firmware.

9.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Save & Exit
	Graphics Configuration			
	Watchdog Configuration			
	ACPI Settings			
	RTC Wake Settings			
	CPU Configuration			
	Chipset Configuration			
	SATA/PATA Configuration			
	PCI Configuration			
	USB Configuration			
	Super I/O Configuration			
	Serial Port Console Redirection			

9.4.1 Graphics Configuration Submenu

Feature	Options	Description
Primary Graphics Device	**Auto** IGD PCI/PCIe	Select primary graphics adapter to be used during boot up. Auto: Try to use external PCI/PCI Express Graphics Device if present. If not, IGD is used. IGD: Internal Graphics Device PCI/PCIe: Standard PCI Express or PCI Graphics Device
IGD Pre-Allocated Graphics Memory	**32MB** 64MB 128MB	Select amount of pre-allocated (fixed) graphics memory used by the Internal Graphics Device.
IGD Total Graphics Memory	128MB **256MB** MAX	Select amount of total graphics memory that maybe used by the Internal Graphics Device. Memory above the fixed graphics memory will be dynamically allocated by the graphics driver according to DVMT 5.0 specification. MAX = Use as much graphics memory as possible. Depends on total system memory installed and the operating system used (see DVMT 5.0 specification).
Gfx Turbo Mode	Disabled **Enabled**	Enable or Disable graphics and memory controller Turbo Mode.
IGD Boot Display Device	**Auto** CRT LFP CRT+LFP LFP-SDVO EFP2 EFP3 EFP CRT+LFP-SDVO CRT+EFP	Select the IGD display device(s) used for boot up. LFP (Local Flat Panel) selects a LVDS panel connected to the integrated LVDS port. LFP-SDVO selects a LVDS panel connected to display port B using a SDVO to LVDS converter. EFPx (External Flat Panel) selects a HDMI/DVI or DisplayPort device connected to the display ports B, C or D.
Active LFP Configuration	No Local Flat Panel **Integrated LVDS** SDVO LVDS Integrated + SDVO LVDS	Select the active local flat panel configuration. SDVO LVDS additionally requires appropriate configuration of display port B interface.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel or the SDVO Local Flat Panel. When no external EDID data set can be found, then the data set selected under 'Local Flat Panel Type' or 'SDVO Local Flat Panel Type' will be used as a fallback data set.

Feature	Options	Description
Local Flat Panel Type	**Auto** VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) XGA 1024x768 1x24 (008h) XGA 1024x768 2x24 (012h) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.*
SDVO Local Flat Panel Type	VGA 640x480 1x18 (002h) VGA 640x480 1x18 (013h) WVGA 800x480 1x24 (01Bh) SVGA 800x600 1x18 (01Ah) XGA 1024x768 1x18 (006h) XGA 1024x768 2x18 (007h) **XGA 1024x768 1x24 (008h)** XGA 1024x768 2x24 (012h) WXGA 1280x768 1x24 (01Ch) SXGA 1280x1024 2x24 (00Ah) SXGA 1280x1024 2x24 (018h) UXGA 1600x1200 2x24 (00Ch) WUXGA 1920x1200 2x18 (015h) WUXGA 1920x1200 2x24 (00Dh) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	A SDVO local flat panel is a LVDS panel connected to a SDVO LVDS transmitter on display port B.
Backlight Inverter Type	None **PWM** I2C	Select the type of backlight inverter used. PWM = Use IGD PWM signal. I2C = Use I2C backlight inverter device connected to the video I²C bus.
PWM Inverter Polarity	Normal Inverted	Select PWM inverter polarity.
PWM Inverter Frequency	200 - 40000	Select PWM inverter frequency.
Backlight Setting	0%, 10%, 25%, 40%, 50%, 60%, 75%, 90%, **100%**	Actual backlight value in percent of the maximum setting.

Feature	Options	Description
Inhibit Backlight	**No** Permanent Until End Of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited until the end of BIOS POST or permanently.
Invert Backlight Control	**No** Yes	Allow to invert backlight control values if required for the actual backlight hardware controller.
Display Port B Interface	**Disabled** SDVO Display Port HDMI/DVI	Select the interface the physical display port should offer.
Select SDVO Device	SDVO DVI SDVO TV **SDVO LVDS**	Select the SDVO device type connected to display port B.
Display Port C Interface	**Disabled** Display Port HDMI/DVI	Select the interface the physical display port should offer.
Display Port D Interface	**Disabled** Display Port HDMI/DVI	Select the interface the physical display port should offer.
Display Mode Persistence	**Disabled** Enable	Display mode persistence means that previous display device configurations can be ‘remembered’ and restored by the system. E.g. a dual view DVI configuration will automatically be restored if both DVI monitors are connected again even if during an earlier boot only one DVI monitor had been connected and active.

9.4.2 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset..
Stop the Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One time trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to '*One time trigger'* the watchdog will be disabled after the first trigger. If set to *'Single event'*, every stage will be executed only once, then the watchdog will be disabled. If set to *'Repeated event'* the last stage will be executed repeatedly until a reset occurs.
Delay	see Post Watchdog	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	**NMI** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 1 is reached.
Event 2	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	0.5sec 1sec 2sec 5sec **10sec** 30sec 1min 2min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.
Watchdog ACPI Event	**Shutdown** Restart	Select the operating system event that is initiated by the watchdog ACPI event. These options perform a critical but orderly operating system shutdown or restart.

Note

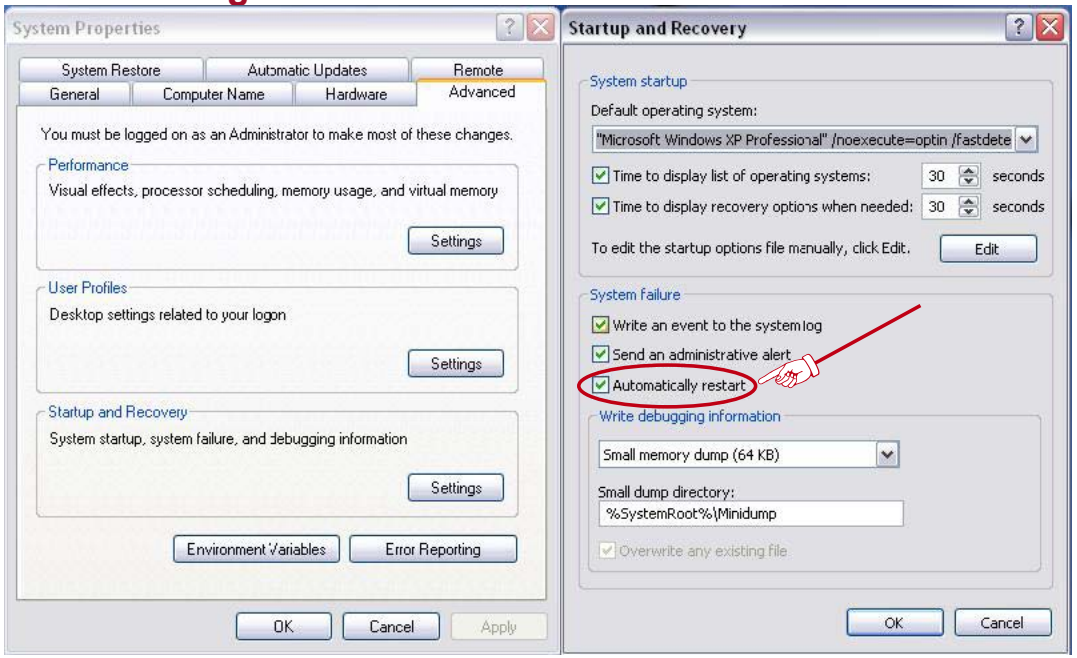
In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very brief blue-screen the system will restart. You can enable this setting by going to the "System Properties" dialog box and choosing the "Advanced" tab. Once there choose the "Settings" button for the "Startup and Recovery" section. This will open the "Startup and Recovery" dialog box. In this dialog box under "System failure" there are three check boxes that define what Windows will do when a fatal error has been detected. In order to ensure that the system restarts after a 'Watchdog ACPI Event" that is set to 'Restart', you must make sure that the check box for the selection "Automatically restart" has been checked. If this option is not selected then Windows will remain at a blue-screen after a 'Watchdog ACPI Event" that has been configured for 'Restart' has been generated. Below is a Windows XP screen-shot showing the proper configuration.

Win XP Watchdog ACPI Event restart configuration



9.4.3 ACPI Configuration Submenu

Feature	Options	Description
ACPI Sleep State	Suspend Disabled **Suspend to RAM**	Select the state used for ACPI system suspend.
Native PCIE Support	**Disabled** Enabled	Enable or disable additional native PCI Express ACPI support. This is only applicable for operating systems that in general already support PCI Express natively (e.g. Windows7 but not Windows XP).
Critical Trip Point	80, 85, 90, 95, 100, **111**, 119°C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Active Trip Point	**Disabled** 50, 60, 70, 80, 90°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Trip Point	Disabled 50, 60, 70, 80, **90**°C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.

9.4.4 RTC Wake Configuration Submenu

Feature	Options	Description
Wake System At Fixed Time	**Disabled** Enabled	Enable system to wake from S5 using RTC alarm.
Wake up hour	0-23	Specify wake up hour.
Wake up minute	0-59	Specify wake up minute.
Wake up second	0-59	Specify wake up second.

9.4.5 CPU Configuration Submenu

Feature	Options	Description
Active Processor Cores	**All** 1 2	Set number of cores to be enabled in each available processor package.
Hyper-Threading	Disabled **Enabled**	Enable or disable Hyper-Threading support.
Execute Disable Bit	Disabled **Enabled**	Enable or disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting OS.
Limit CPUID Maximum	**Disabled** Enabled	When **Enabled**, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When **Disabled**, the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Hardware Prefetcher	Disabled **Enabled**	Enable or disable the MLC streamer prefetcher.
Adjacent Cache Line Prefetch	Disabled **Enabled**	Enable or disable prefetching of adjacent cache lines.
Intel Virtualization Technology	Disabled **Enabled**	Enable or disable support for the Intel virtualization technology.
Intel® SpeedStep™	Disabled **Enabled**	Disabled: No SpeedStep, default CPU speed. Enabled: CPU speed is controlled by the operating system.
Boot Performance Mode	**Max Performance** Max Battery	Select the performance state that the BIOS will set before OS handoff. Max Performance: Maximum CPU speed at POST. Max Battery: Minimum CPU speed at POST.
CPU Turbo Mode	**Enabled** Disabled	Enable or disable the CPU Turbo Mode.
C-States	**Disabled** Enabled	Enable support for supported standard CPU idle states.
Enhanced C-States	Disabled **Enabled**	Enable support for enhanced CPU idle states.

9.4.6 Chipset Configuration Submenu

Feature	Options	Description
PCH LAN Controller	**Enabled** Disabled	Enable or disable the onboard, PCH integrated Ethernet controller.
Wake On LAN Enable	**Enabled** Disabled	Enable or disable the wake on LAN capability of the onboard, PCH integrated Ethernet controller.
PXE ROM	Enabled **Disabled**	Enable or disable PXE option ROM execution for onboard LAN.
HDA Controller	Disabled Enabled **Auto**	Control activation of the HDA controller device. Disabled = HDA controller will be unconditionally disabled Enabled = HDA controller will be unconditionally enabled Auto = HDA Controller will be enabled if HDA codec present, disabled otherwise.
HDA Controller internal HDMI Codec	Enabled **Disabled**	Enable or disable the internal HDMI codec for the HDA Controller.
High Precision Timer	Enabled **Disabled**	Enable or disable the high precision event timer (HPET). This timer can be used for precise multimedia or real time application timing. Special software support is required.
Clock Spread Spectrum	**Disabled** Enabled	Enable or disable clock spread spectrum.
POST Code Output	LPC Bus **PCI Bus**	Select whether port 80h/84h BIOS POST code output should be routed to the PCI bus or the LPC bus.

9.4.7 SATA/PATA Configuration Submenu

Feature	Options	Description
SATA Controller(s)	**Enabled** Disabled	Enable or disable the onboard SATA controllers.
PATA Port	**Enabled** Disabled	Enable or disable the PATA port. In fact this enables or disables the SATA channel on which the onboard SATA to PATA converter is attached. When set to enabled the system boot will be delayed for the time specified in PATA Port Detection Timeout if no PATA device is connected.
PATA Port Detection Timeout	1, 2, **3**, 5, 10, 20, 30 seconds	Define the maximum time to wait for drive detection on PATA port.
SATA Mode Selection	**Native IDE** AHCI	Select SATA controller mode.

9.4.8 PCI Configuration Submenu

Feature	Options	Description
PCI ROM Priority	Legacy ROM **EFI Compatible ROM**	Specify which PCI option ROM to launch in case that multiple option ROMs (legacy and EFI compatible) are present.
Launch Storage Option ROM	Disabled **Enabled**	Enable or disable start of option ROMs for legacy mass storage devices.
PCI Latency Timer	**32**, 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks	Select value to be programmed into PCI latency timer register.
SERR# Generation	Disabled **Enabled**	Enable or disable PCI device SERR# generation.
PCI Express Clock Gating	Disabled **Enabled**	Enable or disable dynamic PCI Express clock gating for all root ports.
DMI Link ASPM Control	Disabled **Enabled**	Control active state power management of the DMI link between CPU/GMCH and PCH.
Generate EXCD0/1_PERST#	Disabled 1ms 5ms **10ms** 50ms 100ms 150ms 200ms 250ms	Select whether and how long the COM Express EXCD0_PERST# and EXCD1_PERST# pins should be driven low during POST.
► PCI Express Root Port 0	submenu	Opens the PCI Express Root Port submenu
► PCI Express Root Port 1	submenu	Opens the PCI Express Root Port submenu.
► PCI Express Root Port 2	submenu	Opens the PCI Express Root Port submenu.
► PCI Express Root Port 3	submenu	Opens the PCI Express Root Port submenu.
► PCI Express Root Port 4	submenu	Opens the PCI Express Root Port submenu.

9.4.9 PCI Express Root Port Submenu

Feature	Options	Description
PCI Express Root Port x	Disabled **Enabled**	Enable or disable the respective PCI Express root port x. Root port 0 cannot be disabled.
Automatic ASPM	**Disabled** L0s L1 L0sL1 Auto	Automatically enable ASPM based on reported capabilities and know issues.
PME SCI	**Disabled** Enabled	Enable or disable PCI Express PME (power management event) SCI.
Hot Plug	**Disabled** Enabled	Enable or disable PCI Express hot plug support.
Extra Bus Reserved	0-7 Default : **0**	Extra busses reserved (0-7) for bridges behind this root bridge.
Reserved Memory	1-20 Default : **10**	Reserved memory and prefetchable memory range for this root bridge (1MB-20MB).
Reserved I/O	4,8,12,16,20 Default : **4**	Opens the PCI Express Root Port submenu

9.4.10 USB Configuration Submenu

Feature	Options	Description
EHCI1	Disabled **Enabled**	Enable or disable EHCI controller 1. At least one EHCI controller must always be enabled.
EHCI2	Disabled **Enabled**	Enable or disable EHCI controller 2. At least one EHCI controller must always be enabled.
USB RMH Mode	Disabled **Enabled**	Enable or disable the USB rate matching hub mode of the USB controllers. (Only change for debug purposes.)
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
EHCI Hand-off	Disabled **Enabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
Device Reset Timeout	10 sec **20 sec** 30 sec 40 sec	USB legacy mass storage device Start Unit command timeout.
Controller Timeout	1 sec 5 sec 10 sec **20 sec**	Timeout value for legacy USB control, bulk and interrupt transfers.
USB Mass Storage Device Name *(Auto detected USB mass storage devices are listed here dynamically)*	**Auto** Floppy Forced FDD Hard Disk CD-ROM	Every USB mass storage device that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. *Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.* Select AUTO to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. Forced FDD allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. Hard Disk allows the device to be emulated as hard disk. CD-ROM assumes the CD-ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

9.4.11 Super I/O Configuration Submenu

Feature	Options	Description
Serial Port 0	Disabled **Enabled**	Enable or disable serial port 0.
Device Settings	IO=3F8h; IRQ=4;	Fixed configuration of serial port 0 if enabled.
Serial Port 1	Disabled **Enabled**	Enable or disable serial port 1.
Device Settings	IO=2F8h; IRQ=3;	Fixed configuration of serial port 1 if enabled.
Parallel Port	Disabled **Enabled**	Enable or disable parallel port.
Device Settings	IO=378h; IRQ=7;	Fixed configuration of the parallel port if enabled.
Device Mode	**Standard Parallel Mode** EPP Mode ECP Mode EPP Mode & ECP Mode	Set the parallel port mode.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

9.4.12 Serial Port Console Redirection

Feature	Options	Description
COM0 Console Redirection	**Disabled** Enabled	Enable or disable serial port 0 console redirection.
►Console Redirection Settings	submenu	Opens console redirection configuration submenu.
COM1 Console Redirection	**Disabled** Enabled	Enable or disable serial port 1 console redirection.
►Console Redirection Settings	submenu	Opens console redirection configuration submenu.

9.4.13 Console Redirection Configuration Submenu

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Select terminal type.
Baudrate	9600, 19200, 38400, 57600, **115200**	Select baudrate.
Data Bits	**7** **8**	Set number of data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Set number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
Recorder Mode	**Disabled** Enabled	With recorder mode enabled, only text output will be sent over the terminal. This is helpful to capture and record terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution in UEFI environment.
Legacy OS Redirection Resolution	**80x24** 80x25	Number of rows and columns supported for legacy OS redirection.

9.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

9.5.1 Boot Settings Configuration

Feature	Options	Description
Quiet Boot	**Disabled** Enabled	Disabled displays normal POST diagnostic messages. Enabled displays OEM logo instead of POST messages. *Note: The default OEM logo is a dark screen.*
UEFI Boot	**Disabled** Enabled	Enables or disables UEFI native boot from disk drives.
Setup Prompt Timeout	**2** 0 - 65535	Number of seconds to wait for setup activation key. 0 means no wait for fastest boot, 65535 means infinite wait.
Bootup NumLock State	**On** Off	Select the keyboard numlock state.
POST/Setup VGA Support	**Disabled** Enabled	Select VGA mode for setup and POST screen. Enables setup and POST screen output support for VGA and WVGA display resolutions.
Power Loss Control	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. Remain Off keeps the power off until the power button is pressed. Turn On restores power to the computer. Last State restores the previous power state before power loss occurred. *Note: Only works with an ATX type power supply.*
Enable Popup Boot Menu	No **Yes**	Select whether the popup boot menu can be started.
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The “Device Based” boot priority list allows you to select from a list of currently detected devices only. The “Type Based” boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the “Device Based” boot priority list might change dynamically in cases when devices are physically removed or added to the system. The “Type Based” boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if device based priority list control is selected. If “Type Based” priority list control is enabled only 8 boot devices can be prioritized.)	Disabled SATA 0 Drive SATA 1 Drive SATA 3 Drive PATA Drive USB Floppy USB Hard disk USB CDROM Onboard LAN External LAN Other BEV Device	This view is only available when in the default “Type Based” mode. When in “Device Based” mode you will only see the devices that are currently connected to the system.

Feature	Options	Description
System Off Mode	**G3/Mech Off** S5/Soft Off	Define system state after shutdown when a battery system is present.
GateA20 Active	**Upon Request** Always	Gate A20 control. Upon Request = Gate A20 can be disabled using BIOS services. Always = Do not allow disabling Gate A20.
Option ROM Messages	**Disabled** Enabled	Set display mode for option ROMs.
Interrupt 19 Capture	**Disabled** Enabled	Defines whether option ROMs may trap the INT19h legacy boot vector.

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

3. *Unlike other module designs available in the embedded market, a CMOS battery is not required by congatec modules to support the 'Power Loss Control' feature.*

9.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

9.6.1 Security Settings

Feature	Options	Description
Setup Administrator Password	enter password	Specifies the setup administrator password.
► **HDD Security Configuration** *List of all detected hard disks supporting the security feature set.*	Select device to open device security configuration submenu	

9.6.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

9.6.3 Save & Exit Menu

Select the Save & Exit tab from the setup menu to enter the Save & Exit setup screen.

You can display an Save & Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup menu after saving the changes. The system is only reset if settings have been changed.
Discard Changes and Exit	Exit setup menu without saving any changes.
Save Changes and Reset	Save changes and reset the system.
Discard Changes and Reset	Reset the system without saving any changes.
Save Changes	Save changes made so far to any of the setup options. Stay in setup menu.
Discard Changes	Discard changes made so far to any of the setup options. Stay in setup menu.
Load CMOS Defaults	Load the CMOS defaults of all the setup options.
► **Boot Override** *List of all boot devices currently detected.*	Select device to leave setup menu and boot from the selected device.

10 Additional BIOS Features

The conga-BM57/BS57/BE57 uses a congatec/AMI AptioEFI that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as BM57R1xx, where BM57 is the congatec internal BIOS project name for conga-BM57/BS57/BE57, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

10.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” refer to the user’s guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

10.2 BIOS Security Features

The BIOS provides a setup administrator password that limits access to the BIOS setup menu.

10.3 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to ‘lock’ and ‘unlock’ drives using the security password. A ‘locked’ drive will be detected by the system, but no data can be accessed. Accessing data on a ‘locked’ drive requires the proper password to ‘unlock’ the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within five attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

11 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.2	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
PICMG® COM Express Module™ Base Specification	http://www.picmg.org/
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications