

congatec Application Note

Affected Products	Type 7 Products
Subject	Type 7 LAN LED Design Notes
Confidential/Public	Public
Author	GMX

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
1.0	2019.09.12	GMX	Initial Revision

Preface

This Application Note explains the fundamentals of the COM-Express Type 7 related 10GbE LAN LED behavior.

In addition, we show our implementation for the 10GbE LAN LED related circuits with our evaluation board schematics and give design notes on certain circuits.

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Symbols

The following are symbols used in this application note.



Note

Notes call attention to important information that should be observed.



Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.



Warning

Warnings indicate that personal injury can occur if the information is not observed.

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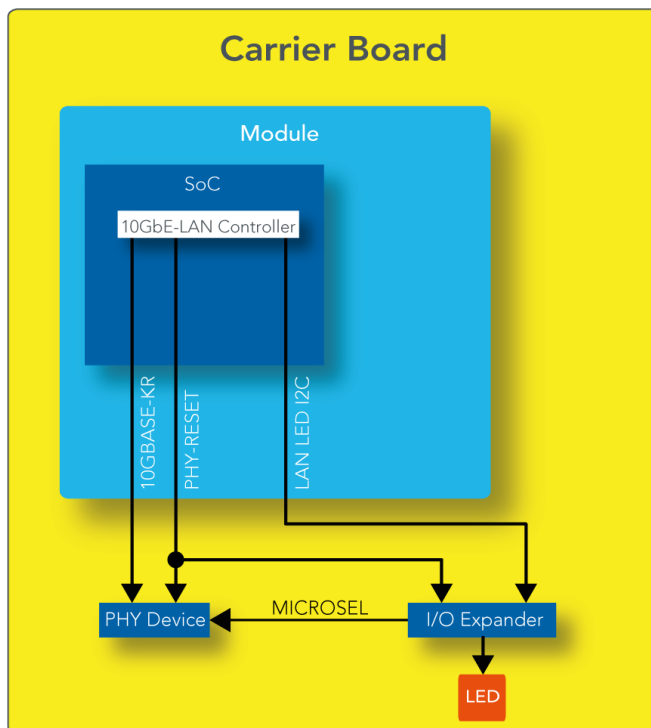
Terminology

Term	Description
SoC	System-on-a-Chip
PHY	Physical Layer Transceiver
LED	Light-emitting Diode
10GbE	10-Gigabit-Ethernet
LAN	Local Area Network

1 Introduction

This AN explains how to implement 10GbE LAN LEDs on a carrier board for the conga-B7XD and conga-B7AC modules on the example of the conga-X7/EVAL evaluation carrier board. The full schematic of the conga-X7/EVAL is available on www.congatec.com.

The block diagram below gives an overview of the implementation with one PHY device:



PHY Device Control Interface (MDIO or I2C)

- 1) The 10GbE-LAN controller negotiates the required control interface with the PHY device via the 10GBASE-KR interface.
- 2) The 10GbE-LAN controller communicates the required control interface to the I/O expander via the two-wire LAN LED I2C bus.
- 3) The I/O expander selects the control interface by setting the MICROSEL signals. The MICROSEL signals are connected to the PHY device via bootstrapping. For more information, see section 2.1.3 .

LED Behavior

- 1) The 10GbE-LAN controller communicates the required LED behavior to the I/O expander via the two-wire LAN LED I2C bus. For more information, see section 2.1.1 .
- 2) The I/O expander controls the behavior of the connected LED. For more information, see section 2.1 .

PHY-RESET

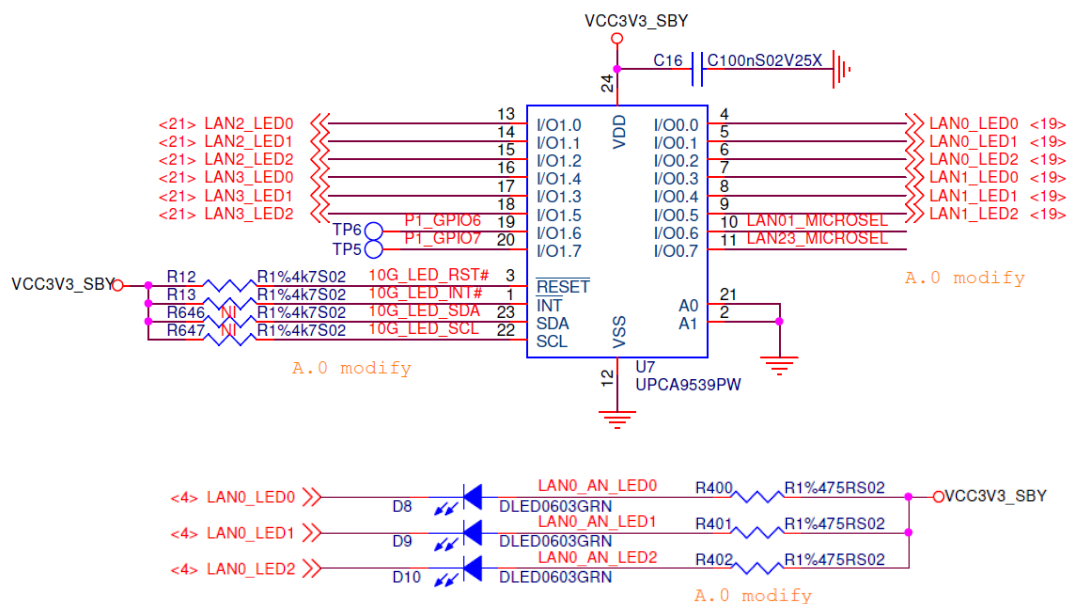
- 1) The 10GbE-LAN controller resets the PHY device and I/O expander via the PHY-RESET signal. For more information, see section 0.2.12

2 Design Notes

2.1 I/O Expander

The COM Express Module Base Specification, Revision 3.0, section 4.3.4, specifies that the carrier board should use a PCA9539 or compatible I2C I/O expander. Furthermore, the specification allows for up to three LEDs per 10GbE-LAN controller.

The schematic below shows how the I/O expander and three LEDs are implemented on the conga-X7/EVAL:



The table below describes the relevant signals of the schematic:

Signal	Description
10G_LED_SDA	This signal is routed directly from the COM Express connector (Pin 36, Row C and Pin 37, Row C respectively) to the PCA9539. The signal does not require a pull-up resistor on the carrier board because it is already pulled up on congatec modules ("NI" for not installed).
10G_LED_SCL	This signal is routed directly from the COM Express connector (Pin 36, Row C and Pin 37, Row C respectively) to the PCA9539. The signal does not require a pull-up resistor on the carrier board because it is already pulled up on congatec modules ("NI" for not installed).
LANx_LEDx	This signal is transmitted by the I/O expander to an LED circuit. The signal is active low and must be connected to the cathode of the LED via an appropriate resistor. Note: The Intel 10GbE-LAN controller on conga-B7XD and conga-B7AC only supports LANx_LED0 and LANx_LED1 signals as specified in the Intel Ethernet Controller Specification. Therefore, LANx_LED2 signals can be left unconnected.
P1_GPIO6	This signal is not specified and can be left unconnected. In this schematic, this signal is used as a test point.
P1_GPIO7	This signal is not specified and can be left unconnected. In this schematic, this signal is used as a test point.
10G_LED_INT#	This signal is transmitted by the I/O expander. It indicates changes in potentially input controlled ports by the I/O expander. This output can remain pulled up to 3.3V because all ports are configured as outputs.

2.1.1 I2C Data Mapping

The table below gives an overview of the I2C data mapping to the I/O expander of the COM Express Module Base Specification, the conga-B7XD, and conga-B7AC:

Port Pin	Signal Name	COMe 3.0 defined function	conga-B7XD function if different	conga-B7AC function if different
P0_0	10G_KR_LED0_0#	PHY0, LED 0 – Status/ACT	PHY 0, LED 0 - on if Link-Up indicated	PHY 0, LED 0 - on if Link-Up indicated
P0_1	10G_KR_LED0_1#	PHY0, LED 1 – Link Speed Max	PHY 0, LED 1 - blinking if 10Gb/s Link indicated	PHY 0, LED 1 – On if Link-Up is indicated, blinking if there is packet activity
P0_2	10G_KR_LED0_2#	PHY 0, LED 2 – Link Speed	Unused	Unused
P0_3	10G_KR_LED1_0#	PHY1, LED 0 – Status/ACT	PHY 1, LED 0 - on if Link-Up indicated	PHY 1, LED 0 - on if Link-Up indicated
P0_4	10G_KR_LED1_1#	PHY1, LED 1 – Link Speed Max	PHY 1, LED 1 - blinking if 10Gb/s Link indicated	PHY 1, LED 1 – On if Link-Up is indicated, blinking if there is packet activity
P0_5	10G_KR_LED1_2#	PHY 1, LED 2 – Link Speed	Unused	Unused
P0_6	10G_KR_STRAP01	PHY 0-1 Strap		
P0_7	10g_KR_STRAP23	PHY 2-3 Strap	Unused	
P1_0	10G_KR_LED0_0#	PHY2, LED 0 – Status/ACT	N/A	PHY 2, LED 0 - on if Link-Up indicated
P1_1	10G_KR_LED0_1#	PHY2, LED 1 – Link Speed Max	N/A	PHY 2, LED 1 – On if Link-Up is indicated, blinking if there is packet activity
P1_2	10G_KR_LED0_2#	PHY 2, LED 2 – Link Speed	N/A	Unused
P1_3	10G_KR_LED1_0#	PHY3, LED 0 – Status/ACT	N/A	PHY 3, LED 0 - on if Link-Up indicated
P1_4	10G_KR_LED1_1#	PHY3, LED 1 – Link Speed Max	N/A	PHY 3, LED 1 – On if Link-Up is indicated, blinking if there is packet activity
P1_5	10G_KR_LED1_2#	PHY 3, LED 2 – Link Speed	N/A	Unused
P1_6	Reserved	TBD		
P1_7	Reserved	TBD		



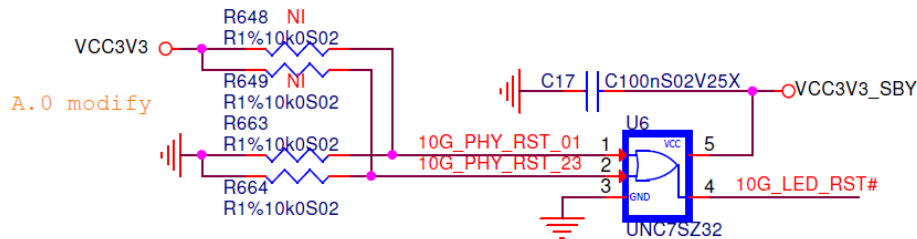
Note

The signal name can be misleading as it does not always reflect the signal function of a particular module. The signal names are defined in the COM Express Module Base Specification but the LED signal functions are defined by Intel for their PHY devices and are therefore reflected on the conga-B7XD and conga-B7AC.

2.1.2 PHY-RESET

The 10GbE-LAN controller resets the I/O expander via the 10G_PHY_RST_xx signals.

The schematic below shows how they are implemented on the conga-X7/EVAL:



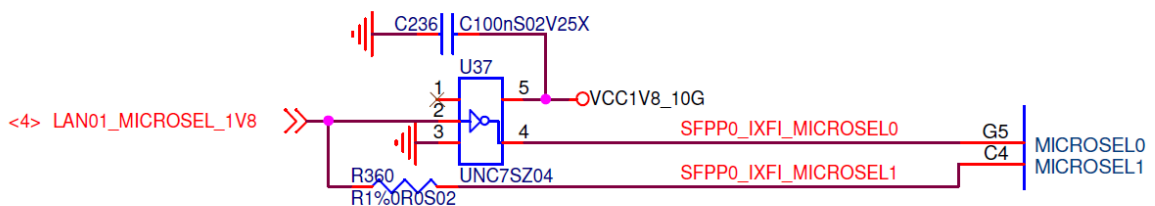
The table below describes the relevant signals of the schematic:

Signal	Description
10G_PHY_RST_01	The I/O expander provides LED signals for up to four 10GbE-LAN controllers. Therefore, a logic OR chip is required for both reset signals. This is achieved by the NC7SZ32.
10G_PHY_RST_23	Note: Here, the signals are pulled-down. Initially, this keeps the devices in reset.

2.1.3 MICROSEL

Some PHY devices support MDIO and I2C interfaces. To select either interface, the I/O expander must set the LANxx_MICROSEL signals for the PHY device via bootstrapping.

The schematic below shows how they are implemented on the conga-X7/EVAL:



The table below describes the relevant signal of the schematic:

Signal	Description
LAN01_MICROSEL_1V8	This signal is transmitted by the I/O expander to the PHY device. The signal is inverted by the NC7SZ04 to set the the Inphi CS4227 PHY device control interface to either MDIO or I2C.

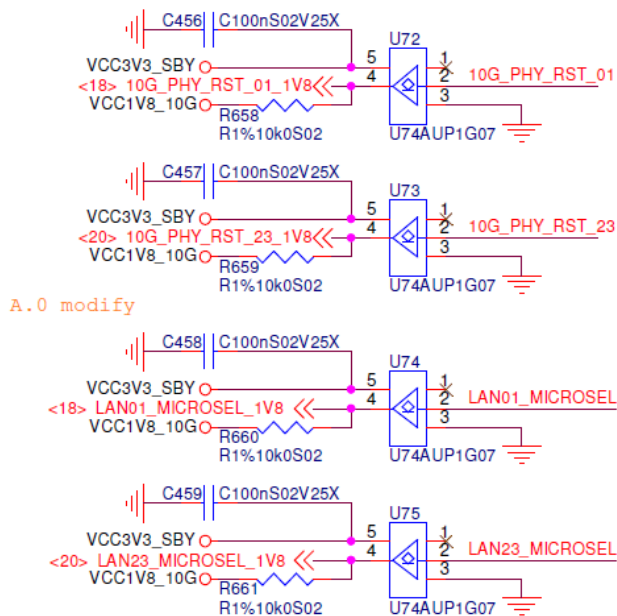
Note

To select the PHY device control interface via bootstrapping, the COM Express pins 10G_PHY_CAP_01 and 10G_PHY_CAP_23 must be connected to ground. If these two pins are unconnected, the PHY device control interface is set to MDIO and it is not possible to select the interface via bootstrapping. For more information, refer to the COM Express Module Base Specification, Revision 3.0, section 4.3.4.

2.2 Level-Shifters for the Inphi CS4227 PHY Device

The Inphi CS4227 PHY device operates at 1.8V signal levels. Therefore, several level-shifters must be implemented to translate the 3.3V PHY-RESET and MICROSEL signals transmitted by the 10GbE-LAN controller and I/O expander respectively to the PHY device.

The schematic below shows how they are implemented on the conga-X7/EVAL:



The table below describes the relevant signals of the schematic:

Signal	Description
10G_PHY_RST_01_1V8	This signal is transmitted by the 10GbE-LAN controller and received by the PHY device. This signal is translated from 3.3V to 1.8V by the U74AUP1G07 level-shifter.
10G_PHY_RST_23_1V8	
LAN01_MICROSEL_1V8	This signal is transmitted by the I/O expander and received by the PHY device. This signal is translated from 3.3V to 1.8V by the U74AUP1G07 level-shifter.
LAN23_MICROSEL_1V8	