# Application Note

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# congatec Application Note

| | |
|---|---|
| **Applicable Products** | conga-BM45, conga-BS45, conga-CS45, conga-BM57, conga-BS57, conga-BE57, conga-BM67 and conga-BS67, conga-BS77, conga-CCA, conga-BAF |
| **Application Note Subject** | Implementation Guide for HDMI and DisplayPort interface |
| **Document Name** | AN17_HDMI_DP_Implementation |
| **Usage Designation** | External |

*Application Note #17*

*Revision 1.7*

# Application Note

**Revision History**

| Revision | Date (dd.mm.yy) | Author | Changes |
|---|---|---|---|
| 1.0 | 24.08.09 | C. Hoch | Initial release |
| 1.1 | 19.05.10 | C. Hoch | Added description for DVI implementation, added BM57, BS57 and BE57. |
| 1.2 | 23.09.10 | C. Hoch | Added schematics for DVI, HDMI and DP |
| 1.3 | 04.10.10 | C. Hoch | Updated schematics. Added Note about HPDEN pin of Chrontel CH7318. |
| 1.4 | 28.12.10 | C. Hoch | Updated sections HDMI and DP Audio, DisplayPort D and SDVO Port C. Corrected minor mistakes. |
| 1.5 | 16.02.11 | C. Hoch | Updated schematics HDMI, DVI and DP. Corrected minor mistakes. |
| 1.6 | 03/27/12 | C. Hoch<br>C. Riesinger | Corrected minor mistakes.<br>Added conga-Bx67 (BM67 and BS67) |
| 1.7 | 02/07/13 | C. Riesinger | Added conga-CCA, conga-BAF and conga-BS77 |

# Preface

This application note provides information about implementing a HDMI or DisplayPort interface on COM Express™ carrier boards.

## Disclaimer

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## Intended Audience

This Application Note is intended for technically qualified personnel. It is not intended for general audiences.

## Symbols

The following symbols may be used in this Application Note:

**Warning**

*Warnings indicate conditions that, if not observed, can cause personal injury.*

**Caution**

*Cautions warn the user about how to prevent damage to hardware or loss of data.*

**Note**

*Notes call attention to important information that should be observed.*

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# Application Note AN17

## Electrostatic Sensitive Device

## Terminology

Some of the following terms may be used throughout this document.

| Term | Description |
| --- | --- |
| T.B.D. | To be determined |
| HDMI | High Definiton Multimedia Interface |
| SDVO | Serial Digital Video Out |
| DVI | Digital Video Interface |
| PEG | PCI Express Graphics |
| DP | DisplayPort Interface |
| conga-Bx57 | conga-BM57, conga-BS57, conga-BE57 |
| conga-Bx67 | conga-BM67, conga-BS67 |

## Copyright Notice

## Trademarks

# Contents

# 1 Introduction

The latest chipsets used on congatec COM Express™ modules not only provide LVDS and SDVO graphics interfaces but also the new generation of interfaces such as HDMI and DisplayPort.

High-Definition Multimedia Interface (HDMI) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data and audio data into TMDS for digital transmission and is fully backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video. Additionally, HDMI adds the ability to send up to 8 separate channels of uncompressed digital audio and auxiliary control data during the horizontal and vertical blanking intervals of the TDMS video stream.

DisplayPort is an open industry standard digital display interface that is under development within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect intended to be used primarily between a computer and its display monitor.

# 2 Pinout on congatec COM Express™ Modules

**Table 1 Shared signals PCI Express, SDVO, HDMI and DisplayPort on congatec Type 2 COM Express™ modules**

| COM Express™ | | x16 PCI Express (PEG) | | Corresponds with SDVO signal | | Corresponds with HDMI signal | | Corresponds with DisplayPort signal | |
|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Pin Name | Description | Pin Name | Description | Pin Name | Description |
| D52 | PEG_TX[0]+ | B14 | HSOp(0) | SDVOB_RED+ | Digital Video B red output differential pair | TMDS_B_DATA2+ | HDMI Port B Data2 output differential pair. | DPB_LANE0+ | DisplayPort B Lane0 output differential pair. |
| D53 | PEG_TX[0]- | B15 | HSOn(0) | SDVOB_REDSerial | | TMDS_B_DATA2- | | DPB_LANE0- | |
| D55 | PEG_TX[1]+ | B19 | HSOp(1) | SDVOB_GRN+ | Digital Video B green output differential pair | TMDS_B_DATA1+ | HDMI Port B Data1 output differential pair. | DPB_LANE1+ | DisplayPort B Lane1 output differential pair. |
| D56 | PEG_TX[1]- | B20 | HSOn(1) | SDVOB_GRNSerial | | TMDS_B_DATA1- | | DPB_LANE1- | |
| D58 | PEG_TX[2]+ | B23 | HSOp(2) | SDVOB_BLU+ | Digital Video B blue output differential pair | TMDS_B_DATA0+ | HDMI Port B Data0 output differential pair. | DPB_LANE2+ | DisplayPort B Lane2 output differential pair. |
| D59 | PEG_TX[2]- | B24 | HSOn(2) | SDVOB_BLUSerial | | TMDS_B_DATA0- | | DPB_LANE2- | |
| D61 | PEG_TX[3]+ | B27 | HSOp(3) | SDVOB_CK+ | Digital Video B clock output differential pair | TMDS_B_CLK + | HDMI Port B Clock output differential pair. | DPB_LANE3+ | DisplayPort B Lane3 output differential pair. |
| D62 | PEG_TX[3]- | B28 | HSOn(3) | SDVOB_CKSerial | | TMDS_B_CLK - | | DPB_LANE3- | |
| D65 | PEG_TX[4]+ | B33 | HSOp(4) | SDVOC_RED+ | Digital Video C red output differential pair | TMDS_C_DATA2+ | HDMI Port C Data2 output differential pair. | DPC_LANE0+ | DisplayPort C Lane0 output differential pair. |
| D66 | PEG_TX[4]- | B34 | HSOn(4) | SDVOC_REDSerial | | TMDS_C_DATA2- | | DPC_LANE0- | |
| D68 | PEG_TX[5]+ | B37 | HSOp(5) | SDVOC_GRN+ | Digital Video C green output differential pair | TMDS_C_DATA1+ | HDMI Port C Data1 output differential pair. | DPC_LANE1+ | DisplayPort C Lane1 output differential pair. |
| D69 | PEG_TX[5]- | B38 | HSOn(5) | SDVOC_GRNSerial | | TMDS_C_DATA1- | | DPC_LANE1- | |
| D71 | PEG_TX[6]+ | B41 | HSOp(6) | SDVOC_BLU+ | Digital Video C blue output differential pair | TMDS_C_DATA0+ | HDMI Port C Data0 output differential pair. | DPC_LANE2+ | DisplayPort C Lane2 output differential pair. |
| D72 | PEG_TX[6]- | B42 | HSOn(6) | SDVOC_BLUSerial | | TMDS_C_DATA0- | | DPC_LANE2- | |
| D74 | PEG_TX[7]+ | B45 | HSOp(7) | SDVOC_CK+ | Digital Video C clock output differential pair | TMDS_C_CLK + | HDMI Port C Clock output differential pair. | DPC_LANE3+ | DisplayPort C Lane3 output differential pair. |
| D75 | PEG_TX[7]- | B46 | HSOn(7) | SDVOC_CKSerial | | TMDS_C_CLK - | | DPC_LANE3- | |
| D78 | PEG_TX[8]+ | B50 | HSOp(8) | - | | - | | DPD_LANE0+ | DisplayPort D Lane0 output differential pair. |
| D79 | PEG_TX[8]- | B51 | HSOn(8) | - | | - | | DPD_LANE0- | |
| D81 | PEG_TX[9]+ | B54 | HSOp(9) | - | | - | | DPD_LANE1+ | DisplayPort D Lane1 output differential pair. |
| D82 | PEG_TX[9]- | B55 | HSOn(9) | - | | - | | DPD_LANE1- | |
| D85 | PEG_TX[10]+ | B58 | HSOp(10) | - | | - | | DPD_LANE2+ | DisplayPort D Lane2 output differential pair. |
| D86 | PEG_TX[10]- | B59 | HSOn(10) | - | | - | | DPD_LANE2- | |
| D88 | PEG_TX[11]+ | B62 | HSOp(11) | - | | - | | DPD_LANE3+ | DisplayPort D Lane3 output differential pair. |
| D89 | PEG_TX[11]- | B63 | HSOn(11) | - | | - | | DPD_LANE3- | |
| C52 | PEG_RX[0]+ | A16 | HSIp(0) | SDVO_TVCLKIN+ | Digital Video TVOUT synchronization clock input differential pair | - | | - | |
| C53 | PEG_RX[0]- | A17 | HSIn(0) | SDVO_TVCLKINSerial | | - | | - | |
| C55 | PEG_RX[1]+ | A21 | HSIp(1) | SDVOB_INT+ | Digital Video B interrupt input differential pair | - | | - | |
| C56 | PEG_RX[1]- | A22 | HSIn(1) | SDVOB_INTSerial | | - | | - | |
| C58 | PEG_RX[2]+ | A25 | HSIp(2) | SDVO_FLDSTALL+ | Digital Video Field Stall input differential pair | - | | DPB_AUX+ | DisplayPort B Aux input differential pair. |
| C59 | PEG_RX[2]- | A26 | HSIn(2) | SDVO_FLDSTALLSerial | | - | | DPB_AUX- | |

| COM Express™ | | x16 PCI Express | | Corresponds with SDVO signal | | Corresponds with HDMI signal | | Corresponds with DisplayPort signal | |
|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Pin Name | Description | Pin Name | Description | Pin Name | Description |
| C61 | PEG_RX[3]+ | A29 | HSIp(3) | - | | TMDS_B_HPD | HDMI Port B Hot-plug detect. | DPB_HPD | DisplayPort B Hot-plug detect. |
| C68 | PEG_RX[5]+ | A39 | HSIp(5) | SDVOC_INT+ | Digital Video C interrupt input differential pair | - | | - | |
| C69 | PEG_RX[5]- | A40 | HSIn(5) | SDVOC_INT- | | - | | - | |
| C71 | PEG_RX[6]+ | A43 | HSIp(6) | - | | - | | DPC_AUX+ | DisplayPort C Aux input differential pair. |
| C72 | PEG_RX[6]- | A44 | HSIn(6) | - | | - | | DPC_AUX- | |
| C74 | PEG_RX[7]+ | A47 | HSIp(7) | - | | TMDS_C_HPD | HDMI Port C Hot-plug detect. | DPC_HPD | DisplayPort C Hot-plug detect. |
| C85 | PEG_RX[10]+ | A60 | HSIp(10) | - | | - | | DPD_AUX+ | DisplayPort D Aux input differential pair. |
| C86 | PEG_RX[10]- | A61 | HSIn(10) | - | | - | | DPD_AUX- | |
| C88 | PEG_RX[11]+ | A64 | HSIp(11) | - | | - | | DPD_HPD# | DisplayPort D Hot-plug detect. |
| D73 | SDVO_CLK | B17 | PRSNT#2 | SDVO_I2C_CK | SDVO I²C clock line to set up SDVO peripherals | DDPB_CTRLCLK | HDMI port B Control Clock | - | |
| C73 | SDVO_DATA | B31 | PRSNT#2 | SDVO_I2C_DAT | SDVO I²C data line to set up SDVO peripherals | DDPB_CTRLDATA | HDMI port B Control Data DDPB_CTRLDATA is a boot strap signal (see note below) | DDPB_CTRLDATA | DDPB_CTRLDATA is a boot strap signal (see note below) |
| D63 | RSVD | A1 | PRSNT#1 | - | | DDPC_CTRLCLK | HDMI port C Control Clock | - | |
| D64 | RSVD | B81 | PRSNT#2 | - | | DDPC_CTRLDATA | HDMI port C Control Data DDPC_CTRLDATA is a boot strap signal (see note below) | DDPC_CTRLDATA | DDPC_CTRLDATA is a boot strap signal (see note below) |
| D83 | RSVD | - | - | - | | - | | DDPD_CTRLDATA | DDPC_CTRLDATA is a boot strap signal (see note below) |

These signals are not supported on conga-Bx57, conga-Bx67 and conga-BS77    These signals are not supported on conga-Bx45 and conga-CS45

**conga-CCA offers HDMI and DisplayPort support on Port B only**          **conga-BAF offers HDMI and DisplayPort support on Port B and C**

## Note

*This signal has to be pulled up to 3.3V using a 2.2kOhm resistor to enable the respective graphics port. This does not apply to the conga-BAF module. Refer to section 3.1.2 and 5.1.3 of this application note for more information.*

# 3 High Definition Multimedia Interface (HDMI)

The congatec COM Express™ modules offer two single-link HDMI interfaces (Port B and Port C) with a pixel clock rate of up to 165MHz. The appropriate TDMS receive and transmit differential signal pair, as well as additional control signals, can be found on the COM Express™ module connector. This interface is shared with the PEG, SDVO and DisplayPort signals (see Table 1).

The HDMI port provides a two-wire point-to-point communication path between the HDMI device and the Intel GMCH. The HDMI control clock and data (DDPx_CTRLDATA and DDPx_CTRLCLK) provide similar functionality to I²C. However, unlike I²C this interface is intended to be point-to-point and will require the SDVO device to act as a switch and direct traffic from the SDVO control bus to the appropriate receiver. Additionally, this control bus will be able to run at faster speeds (up to 1MHz) than a traditional I²C interface.

## 3.1 HDMI Implementation

The HDMI interface on congatec COM Express™ modules is provided by the chipset's integrated graphics engine. This HDMI interface is multiplexed with the PCI Express Graphics (PEG), SDVO and DisplayPort interface. Since all of these interfaces are low-swing AC coupled differential inputs, high speed HDMI level shifters are required to translate the signals to the HDMI compliant open-drain current steering Rx terminated differential output.

HDMI level shifters are available from different manufacturers such as Chrontel CH7318 (http://www.chrontel.com), Parade Technologies PS101QFN48G (http://www.paradetech.com) or Pericom Semiconductor PI3VDV411LSZDE (http://www.pericom.com).
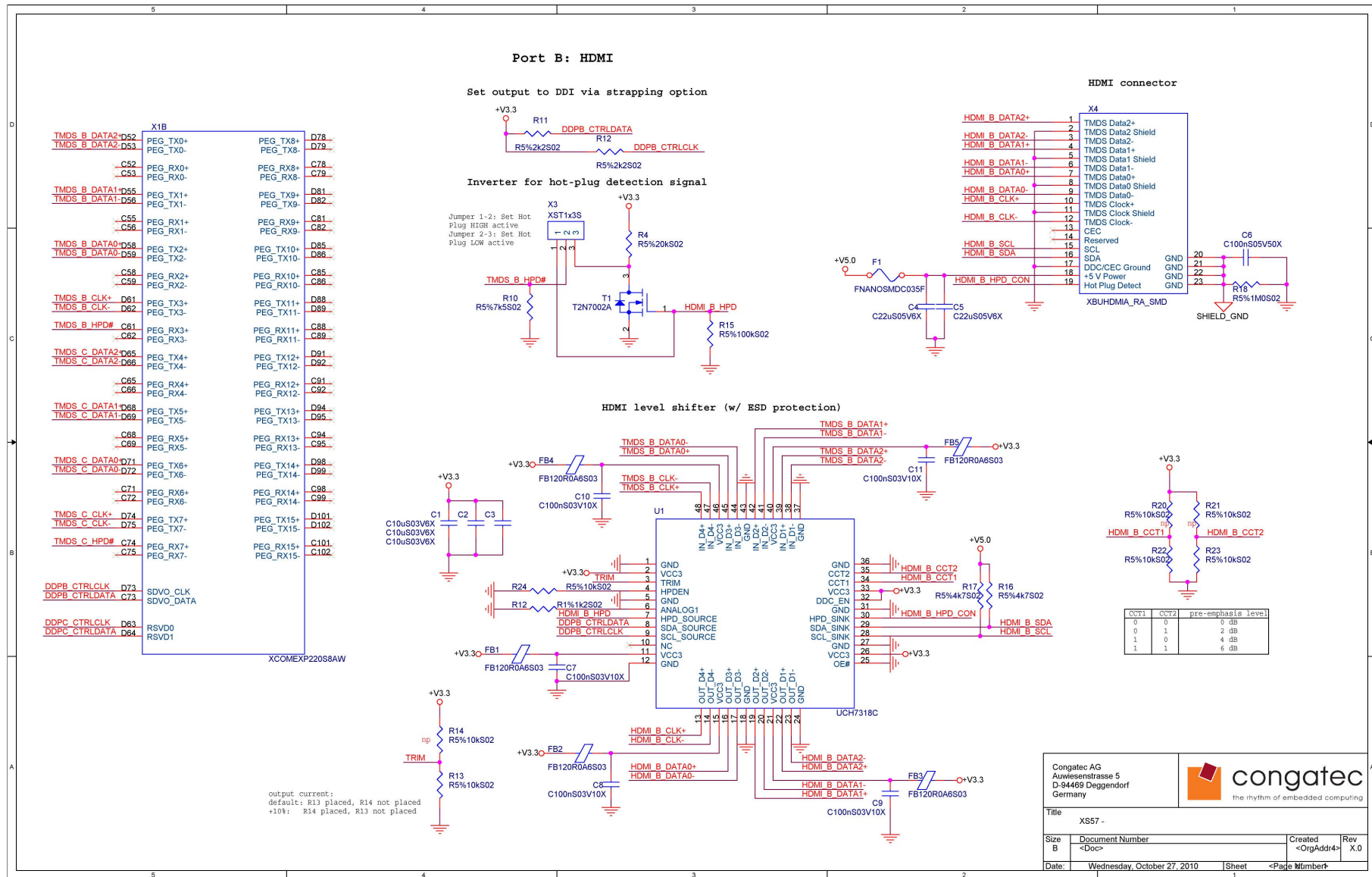
> **Note**
>
> *In order for the HDMI interface to be compliant with the HDMI Specification, level shifters must be implemented on the carrier board for the HDMI signals.*

### 3.1.1 HDMI Example Schematics

The following schematic example is based on the Chrontel CH7318C level shifter.

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Port B: HDMI

Set output to DDI via strapping option

HDMI connector

+V3.3
R11
DDPB_CTRLDATA
R5%2k2S02
R12
DDPB_CTRLCLK
R5%2k2S02

Inverter for hot-plug detection signal

Jumper 1-2: Set Hot Plug HIGH active
Jumper 2-3: Set Hot Plug LOW active

X3
XST1x3S
+V3.3
R4
R5%20kS02
TMDS_B_HPD#
R10
R5%7k5S02
T1
T2N7002A
HDMI_B_HPD
R15
R5%100kS02

**X1B**

| | | | |
|---|---|---|---|
| TMDS_B_DATA2+ | D52 | PEG_TX0+ | PEG_TX8+ D78 |
| TMDS_B_DATA2- | D53 | PEG_TX0- | PEG_TX8- D79 |
| C52 | PEG_RX0+ | PEG_RX8+ | C78 |
| C53 | PEG_RX0- | PEG_RX8- | C79 |
| TMDS_B_DATA1+ | D55 | PEG_TX1+ | PEG_TX9+ D81 |
| TMDS_B_DATA1- | D56 | PEG_TX1- | PEG_TX9- D82 |
| C55 | PEG_RX1+ | PEG_RX9+ | C81 |
| C56 | PEG_RX1- | PEG_RX9- | C82 |
| TMDS_B_DATA0+ | D58 | PEG_TX2+ | PEG_TX10+ D85 |
| TMDS_B_DATA0- | D59 | PEG_TX2- | PEG_TX10- D86 |
| C58 | PEG_RX2+ | PEG_RX10+ | C85 |
| C59 | PEG_RX2- | PEG_RX10- | C86 |
| TMDS_B_CLK+ | D61 | PEG_TX3+ | PEG_TX11+ D88 |
| TMDS_B_CLK- | D62 | PEG_TX3- | PEG_TX11- D89 |
| TMDS_B_HPD# | C61 | PEG_RX3+ | PEG_RX11+ C88 |
| C62 | PEG_RX3- | PEG_RX11- | C89 |
| TMDS_C_DATA2+ | D65 | PEG_TX4+ | PEG_TX12+ D91 |
| TMDS_C_DATA2- | D66 | PEG_TX4- | PEG_TX12- D92 |
| C65 | PEG_RX4+ | PEG_RX12+ | C91 |
| C66 | PEG_RX4- | PEG_RX12- | C92 |
| TMDS_C_DATA1+ | D68 | PEG_TX5+ | PEG_TX13+ D94 |
| TMDS_C_DATA1- | D69 | PEG_TX5- | PEG_TX13- D95 |
| C68 | PEG_RX5+ | PEG_RX13+ | C94 |
| C69 | PEG_RX5- | PEG_RX13- | C95 |
| TMDS_C_DATA0+ | D71 | PEG_TX6+ | PEG_TX14+ D98 |
| TMDS_C_DATA0- | D72 | PEG_TX6- | PEG_TX14- D99 |
| C71 | PEG_RX6+ | PEG_RX14+ | C98 |
| C72 | PEG_RX6- | PEG_RX14- | C99 |
| TMDS_C_CLK+ | D74 | PEG_TX7+ | PEG_TX15+ D101 |
| TMDS_C_CLK- | D75 | PEG_TX7- | PEG_TX15- D102 |
| TMDS_C_HPD# | C74 | PEG_RX7+ | PEG_RX15+ C101 |
| C75 | PEG_RX7- | PEG_RX15- | C102 |
| DDPB_CTRLCLK | D73 | SDVO_CLK | |
| DDPB_CTRLDATA | C73 | SDVO_DATA | |
| DDPC_CTRLCLK | D63 | RSVD0 | |
| DDPC_CTRLDATA | D64 | RSVD1 | |

XCOMEXP220S8AW

**X4**

| | | |
|---|---|---|
| HDMI_B_DATA2+ | 1 | TMDS Data2+ |
| HDMI_B_DATA2- | 2 | TMDS Data2 Shield |
| HDMI_B_DATA1+ | 3 | TMDS Data2- |
| | 4 | TMDS Data1+ |
| HDMI_B_DATA1- | 5 | TMDS Data1 Shield |
| HDMI_B_DATA0+ | 6 | TMDS Data1- |
| | 7 | TMDS Data0+ |
| HDMI_B_DATA0- | 8 | TMDS Data0 Shield |
| HDMI_B_CLK+ | 9 | TMDS Data0- |
| | 10 | TMDS Clock+ |
| HDMI_B_CLK- | 11 | TMDS Clock Shield |
| | 12 | TMDS Clock- |
| | 13 | CEC |
| HDMI_B_SCL | 14 | Reserved |
| HDMI_B_SDA | 15 | SCL |
| | 16 | SDA |
| | 17 | DDC/CEC Ground |
| | 18 | +5 V Power |
| HDMI_B_HPD_CON | 19 | Hot Plug Detect |
| | 20 | GND |
| | 21 | GND |
| | 22 | GND |
| | 23 | GND |

XBUHDMIA_RA_SMD

+V5.0 F1
FNANOSMDC035F
C4 C22uS05V6X
C5 C22uS05V6X

C6 C100nS05V50X
R19 R5%1M0S02
SHIELD_GND

HDMI level shifter (w/ ESD protection)

TMDS_B_DATA1+
TMDS_B_DATA1-
TMDS_B_DATA0-
TMDS_B_DATA0+
TMDS_B_DATA2+
TMDS_B_DATA2-
+V3.3 FB4
FB120R0A6S03
FB5 +V3.3
FB120R0A6S03
C11 C100nS03V10X
TMDS_B_CLK-
TMDS_B_CLK+
+V3.3
C10 C100nS03V10X

C1 C2 C3
C10uS03V6X
C10uS03V6X
C10uS03V6X

**U1 — UCH7318C**

| | | |
|---|---|---|
| 1 | GND | |
| 2 | VCC3 | |
| 3 | TRIM | +V3.3 TRIM R24 R5%10kS02 |
| 4 | HPDEN | |
| 5 | GND | R12 R1%1k2S02 |
| 6 | ANALOG1 | |
| 7 | HPD_SOURCE | HDMI_B_HPD |
| 8 | SDA_SOURCE | DDPB_CTRLDATA |
| 9 | SCL_SOURCE | DDPB_CTRLCLK |
| 10 | NC | |
| 11 | VCC3 | +V3.3 FB1 FB120R0A6S03 C7 C100nS03V10X |
| 12 | GND | |
| 36 | GND | |
| 35 | CCT2 | HDMI_B_CCT2 |
| 34 | CCT1 | HDMI_B_CCT1 |
| 33 | VCC3 | +V3.3 |
| 32 | DDC_EN | |
| 31 | GND | |
| 30 | HPD_SINK | HDMI_B_HPD_CON |
| 29 | SDA_SINK | HDMI_B_SDA |
| 28 | SCL_SINK | HDMI_B_SCL |
| 27 | GND | |
| 26 | VCC3 | +V3.3 |
| 25 | OE# | |

R17 R5%4k7S02  R16 R5%4k7S02  +V5.0

+V3.3
R14 R5%10kS02
TRIM np
R13 R5%10kS02

output current:
default: R13 placed, R14 not placed
+10%:   R14 placed, R13 not placed

+V3.3 FB2
FB120R0A6S03
C8 C100nS03V10X
HDMI_B_CLK+
HDMI_B_CLK-
HDMI_B_DATA0+
HDMI_B_DATA0-
HDMI_B_DATA1-
HDMI_B_DATA1+
HDMI_B_DATA2-
HDMI_B_DATA2+
FB3 +V3.3
FB120R0A6S03
C9 C100nS03V10X

+V3.3
R20 R5%10kS02   R21 R5%10kS02
np np
HDMI_B_CCT1   HDMI_B_CCT2
R22 R5%10kS02   R23 R5%10kS02

| CCT1 | CCT2 | pre-emphasis level |
|---|---|---|
| 0 | 0 | 0 dB |
| 0 | 1 | 2 dB |
| 1 | 0 | 4 dB |
| 1 | 1 | 6 dB |

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## 3.1.2 Enable HDMI Support

To enable HDMI support, the control data line of the respective HDMI Port B or Port C (DDPx_CTRLDATA - see Table 1) must be pulled to +3.3V by a 2.2kOhm resistor (not applicable to conga-BAF).

Additionally, a BIOS setup configuration is necessary to enable the HDMI interface. The setup nodes shown below (located in the Graphics Configuration sub-menu within the congatec BIOS Setup Program) must be set to 'HDMI Port' for the respective port (Port B or C).

**Table 2 BIOS Graphics Configuration Submenu of conga-BM45, conga-BS45 and conga-CS45**

| Feature | Options | Description |
|---------|---------|-------------|
| SDVO Port B Configuration | Disabled<br>**HDMI Port**<br>Display Port<br>SDVO DVI (default setting)<br>….... | Select the SDVO device connected to this SDVO port or configure the port as HDMI or Display Port. |
| SDVO Port C Configuration | Disabled<br>**HDMI Port**<br>Display Port<br>SDVO DVI (default setting)<br>….... | Select the SDVO device connected to this SDVO port or configure the port as HDMI or Display Port. |

**conga-Bx57, conga-Bx67 and conga-BS77**

| Feature | Options | Description |
|---------|---------|-------------|
| Display Port B Interface | Disabled (default setting)<br>SDVO<br>Display Port<br>**HDMI/DVI** | Select the interface the physical display port should offer. |
| Display Port C Interface | Disabled (default setting)<br>Display Port<br>**HDMI/DVI** | Select the interface the physical display port should offer. |
| Display Port D Interface | Disabled (default setting)<br>Display Port<br>**HDMI/DVI** | Select the interface the physical display port should offer. |

### conga-CCA

| Feature | Options | Description |
|---|---|---|
| DDI Port B | Disabled<br>Display Port<br>**HDMI/DVI** | Select the Digital Display Interface offered by the Graphic Pipe B. |

### conga-BAF

| Feature | Options | Description |
|---|---|---|
| Display Channel 0 Output | Display Port C<br>**HDMI C**<br>LVDS<br>Disabled | Define output mode and connection of the integrated display channel 0.<br>This port can also be used for LVDS support provided by an on-board eDP to LVDS converter chip. |
| Display Channel 1 Output | Display Port B<br>**HDMI B**<br>Disabled | Define output mode and connection of the integrated display channel1. |

### 3.1.3 HDMI Connector Pinout

**Figure 3-1 HDMI Connector (Type A - male, front view)**
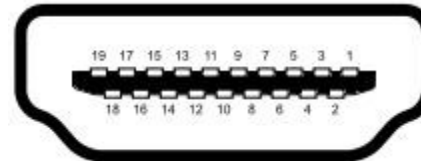


**Table 3 Pinout HDMI Connector**

| Pin# | Signal | Description | Pin# | Signal | Description |
|---|---|---|---|---|---|
| 1 | TMDS Data 2+ | HDMI Lane 2 (positive) | 2 | TMDS Data 2 Shield | Shield of Data 2 pair |
| 3 | TMDS Data 2- | HDMI Lane 2 (negative) | 4 | TMDS Data 1+ | HDMI Lane 1 (positive) |
| 5 | TMDS Data 1 Shield | Shield of Data 1 pair | 6 | TMDS Data 1- | HDMI Lane 1 (negative) |
| 7 | TMDS Data 0+ | HDMI Lane 0 (positive) | 8 | TMDS Data0 Shield | Shield of Data 0 pair |
| 9 | TMDS Data 0- | HDMI Lane 0 (negative) | 10 | TMDS Clock- | HDMI Clock (positive) |
| 11 | TMDS Clock Shield | Shield of Clock pair | 12 | TMDS Clock- | HDMI Clock (negative) |
| 13 | CEC | Consumer Electronics Control Interface | 14 | Reserved | N.C. |
| 15 | DDC Clock | DDC based control signal (clock) | 16 | DDC Data | DDC based control signal (data) |
| 17 | GND | Ground | 18 | +5V | +5V Power Supply |
| 19 | HPD | Hot plug detect | | | |

## 3.1.4 HDMI Hot-plug Detection

Due to the different chipsets used on the congatec COM Express modules, the hot-plug detection signal for the HDMI and the DisplayPort reacts differently to signal levels. The HDMI and the DisplayPort hot-plug detection is activated with low-active signal on the conga-BM45, conga-BS45, conga-CS45 and conga-BAF modules while on the conga-Bx57, conga-Bx67, conga-BS77 and conga-CCA modules with a high-active signal.

In order to ensure compatible carrier board designs among these modules and/or future modules, congatec recommends the design of an optional inverter as shown in the schematics example in section 3.1.1 .

**Note**

*Instead of the inverter for the hot-plug detection signal (HDMI_B_HPD) shown in the schematics in section 3.1.1 , the 'HPDEN' signal input of the Chrontel CH7318 controller can be used to generate the adequate polarity of the hot-plug detection signal required by congatec modules. Keep in mind that when the signal inversion is performed by using the 'HPDEN' pin, the 'HDMI_B_HPD' signal level must be additionally adapted according to the application notes provided by Chrontel (http://www.chrontel.com).*

## 3.2 HDMI Audio

congatec conga-BM45, conga-BS45 and conga-CS45 COM Express™ modules do not support HDMI audio. The conga-Bx57, conga-Bx67, conga-BS77 and conga-CCA support HDMI audio. HDMI audio has to be enabled in the BIOS setup (see Table 4) and additionally, the module's operating system graphics driver has to be installed (or reinstalled).

**Table 4 BIOS Chipset Configuration Submenu conga-Bx57, Bx67 and BS77**

| Feature | Options | Description |
| --- | --- | --- |
| HDA Controller internal HDMI Codec | **Enabled**<br>Disabled (default setting) | Enable or disable the internal HDMI codec for the HDA Controller. |

## 3.3 HDCP

HDMI can use HDCP (High-bandwidth Digital Content Protection) to encrypt the signal if this is required by the source device. Digital Rights Management (DRM) requires HDCP on the HDMI interface when playing back encrypted DVD Video, DVD Audio, HD DVD, and Blue-Ray Disc. HDCP controls the authentication and switching/distribution of the HDMI signal so that it can only be routed to the corresponding device.

HDCP is not supported by default on the the congatec COM Express™ modules. For more information about HDCP support on congatec modules, contact congatec technical support.

# 4    Digital Video Interface (DVI)

The video signals used on the DVI interface are electrically compatible with HDMI video signals. No signal conversion is required and no loss in video quality occurs when the HDMI signal of the congatec COM Express™ module is used to implement a DVI interface.

**Note**

*Some DVI devices may not support HDCP (see section 3.3 of this document). Ensure that a HDCP-enabled signal source is not used in this case.*

## 4.1    DVI Implementation

Refer to the description in the section 3.1 of this document.

**Note**

*As described in section 3.1 for HDMI implementation, the DVI signals also require level shifters on the carrier board to be compliant with the DVI Specification.*

*For compatibility with congatec COM Express™ modules that do not support HDMI, the DVI interface can be implemented by using a SDVO-to-DVI transmitter. This does not apply to the conga-CCA and conga-BAF COM Express™ modules because they do not support SDVO. For more details on this solution, consult the congatec "Design Guide for SDVO" on the congatec website at (http://www.congatec.com).*

### 4.1.1    DVI Example Schematics

The following schematic example is based on the Chrontel CH7318C level shifter.

Port B: DVI

Set output to DDI via strapping option

DVI connector

Inverter for hot-plug detection signal

TMDS level shifter (w/ ESD protection)

| CCT1 | CCT2 | pre-emphasis level |
|------|------|--------------------|
| 0 | 0 | 0 dB |
| 0 | 1 | 2 dB |
| 1 | 0 | 4 dB |
| 1 | 1 | 6 dB |

output current:
default: R13 placed, R14 not placed
+10%:   R14 placed, R13 not placed

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Title: DVI Ref. Schematic

| Size B | Document Number <Doc> | | Created <OrgAddr4> | Rev X.0 |
|--------|------------------------|--|---------------------|---------|
| Date: | Friday, September 17, 2010 | Sheet | <Page Number> | |
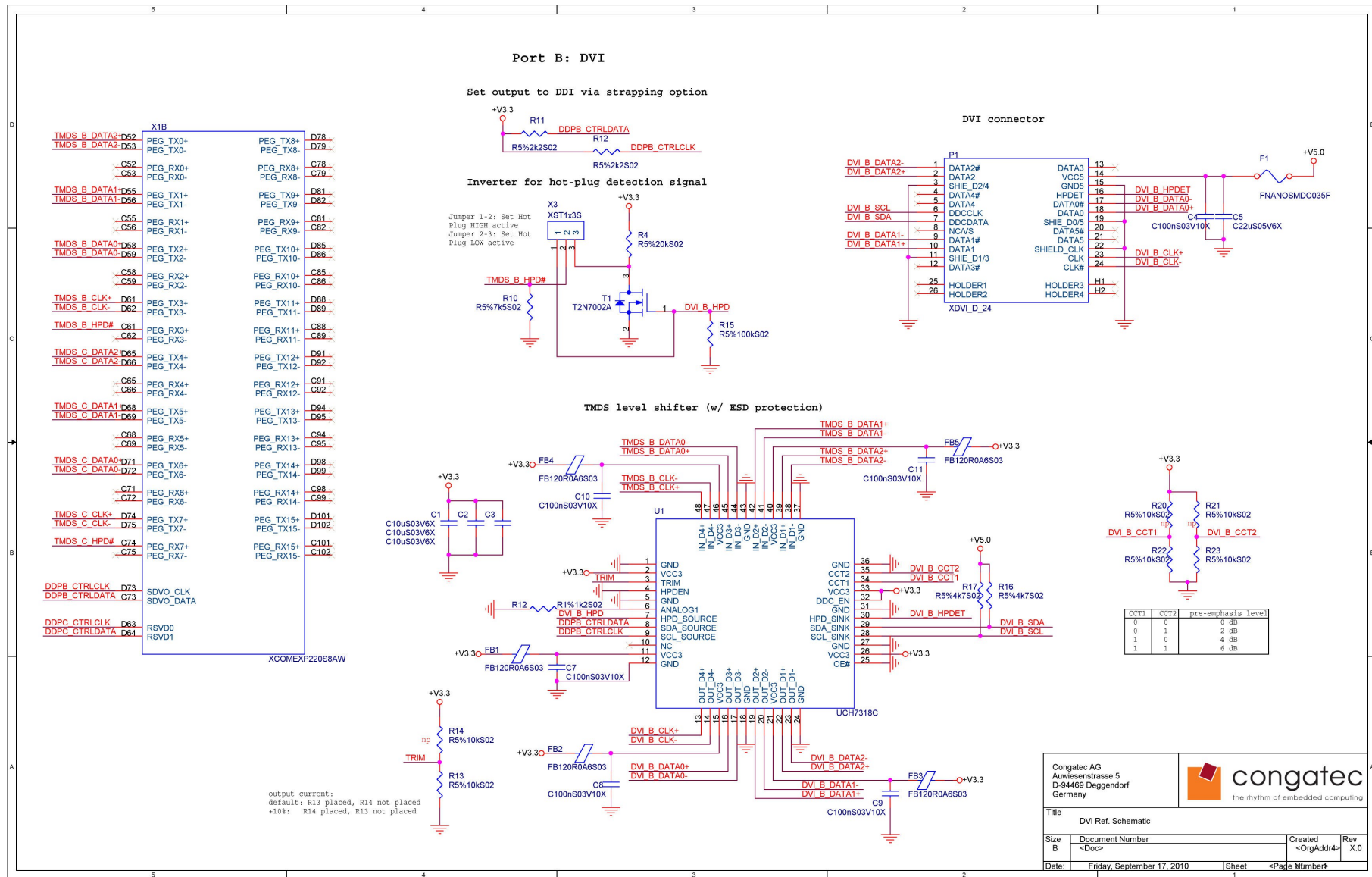
## 4.1.2   Enable DVI Support

Refer to the description in section 3.1.2 of this document.

> **Note**
>
> *The same configuration as described in section 3.1.2 should be used. Do not use the BIOS setting 'SDVO DVI'. This setting must be applied when an SDVO to DVI codec is used on the carrier board. For details about SDVO, refer to the 'Design Guide for SDVO' on the congatec website.*

## 4.1.3   DVI Pinout
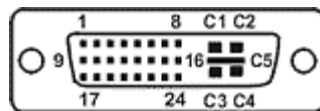
**Figure 4-1 DisplayPort Connector (female, front view)**



**Table 5 Pinout DVI-I Connector**

| Pin# | Signal | Description | Pin# | Signal | Description |
|---|---|---|---|---|---|
| 1 | TMDS Data 2- | DVI Lane 2 (negative) | 2 | TMDS Data 2+ | DVI Lane 2 (positive) |
| 3 | TMDS Data 2/4 SHIELD | Shield of Data pair 2 and 4 | 4 | TMDS Data 4- | DVI Lane 4 (negative) |
| 5 | TMDS Data 4+ | DVI Lane 4 (positive) | 6 | DDC Clock | DDC based control signal (clock) |
| 7 | DDC Data | DDC based control signal (data) | 8 | ANALOG VERT SYNC | Analog Vertical Synchronization |
| 9 | TMDS Data 1- | DVI Lane 1 (negative) | 10 | TMDS DATA 1+ | DVI Lane 1 (negative) HDMI Clock (positive) |
| 11 | TMDS DATA 1/3 SHIELD | Shield of Data pair 1 and 3 | 12 | TMDS DATA 3- | DVI Lane 3 (negative) |
| 13 | TMDS DATA 3+ | DVI Lane 3 (positive) | 14 | +5V | +5V Power Supply |
| 15 | GND | Ground | 16 | HPD | Hot plug detect |
| 17 | TMDS Data 0- | DVI Lane 0 (negative) | 18 | TMDS Data 0+ | DVI Lane 0 (positive) |
| 19 | TMDS Data 0/5 SHIELD | Shield of Data pair 0 and 5 | 20 | TMDS Data 5- | DVI Lane 5 (negative) |
| 21 | TMDS Data 5+ | DVI Lane 5 (positive) | 22 | TMDS Clock Shield | Shield of Clock pair |

| Pin# | Signal | Description | Pin# | Signal | Description |
|------|--------|-------------|------|--------|-------------|
| 23 | TMDS Clock+ | DVI Clock (positive) | 24 | TMDS Clock - | DVI Clock (negative) |
| C1 | ANALOG RED | Analog Red | C2 | ANALOG GREEN | Analog Green |
| C3 | ANALOG BLUE | Analog Blue | C4 | ANALOG HORZ SYNC | Analog Horizontal Synchronization |
| C5 | ANALOG GND | Analog ground (Return for R, G and B signals) | | | |

Different kinds of video signals can be implemented depending on the DVI connector pinout. The DVI-D connector implements only the digital video signals while the DVI-A connector implements only the analog video signals (marked in light grey in the table above). When a DVI connector incorporates both digital and analog video signals it is referred to as DVI-I (integrated).

## 4.1.4   DVI Hot-plug Detection

Refer to section 3.1.4  of this Application Note.

# 5 DisplayPort (DP)

The congatec conga-CCA COM Express™ module supports only one DisplayPort interface (Port B). Two DisplayPort interfaces (Port B and Port C) are supported on the conga-BM45, conga-BS45, conga-CS45 and conga-BAF while the conga-Bx57, conga-Bx67 and BS77 modules support three DisplayPort interfaces (Port B, C and D)

The appropriate TDMS receive and transmit differential signal pair, as well as additional control signals, can be found on the connector of the COM Express™ module. This interface might be shared with the PEG, SDVO and HDMI/DVI signals (see Table 1).

> **Note**
>
> *The boot strap signal used to enable the DisplayPort D (DDPD_CTRLDATA ) is not part of the COM Express™ standard. congatec used a reserved (RSVD) pin for this signal. The signal is also not available at the PCI Express Graphics (PEG) connector. This means that the boot strapping must be implemented on the customers COM Express™ carrier board. This does not apply to the conga-BAF module.*
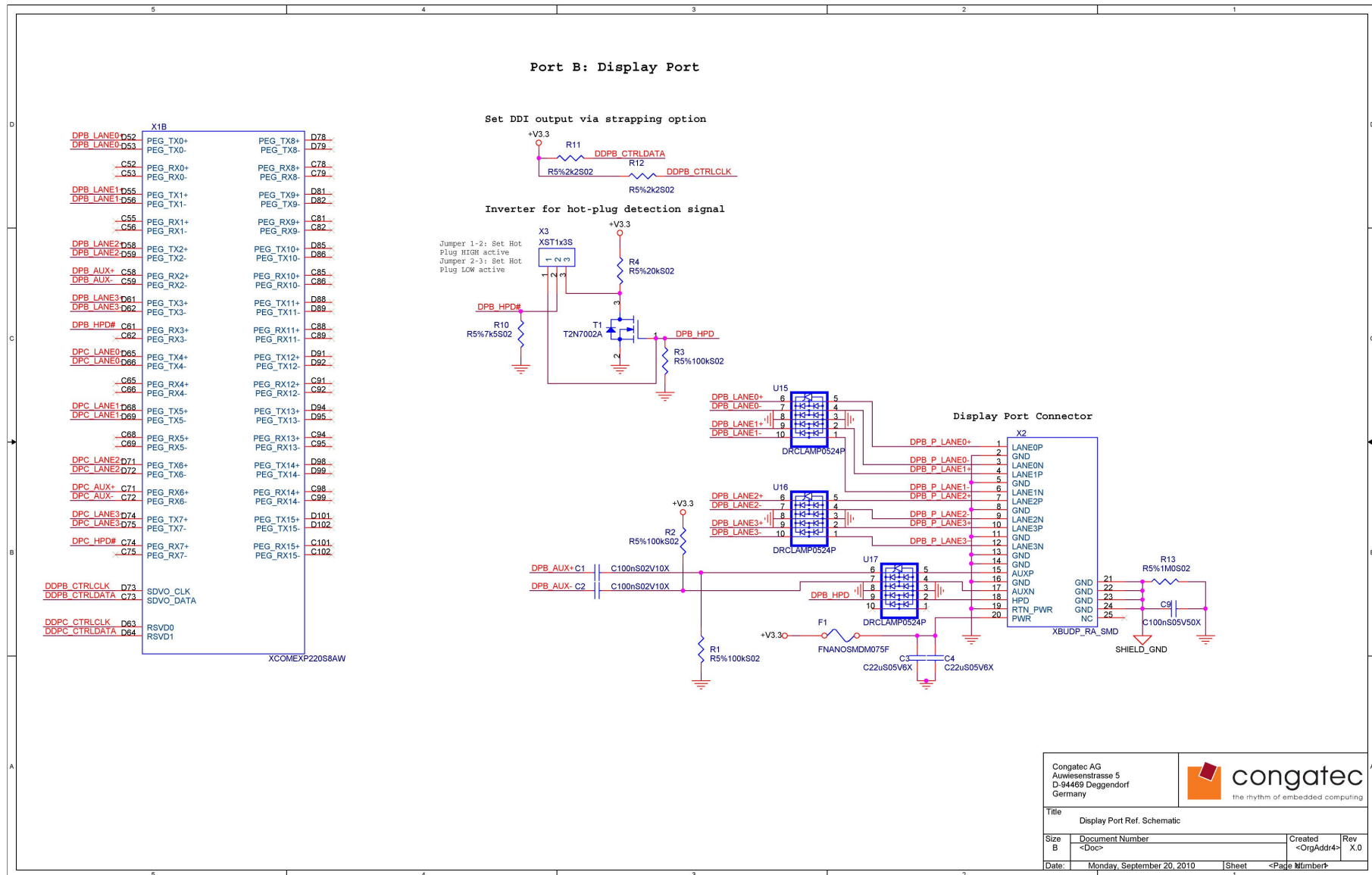
## 5.1 DisplayPort Implementation

The DisplayPort interface supports 1, 2, or 4 data pairs that carry the video signal, clock and optional audio signals. The video signal of the DisplayPort interface is not compatible with DVI or HDMI but a DisplayPort connector can pass these signals through. While HDMI/DVI require separate clock signals, DisplayPort embeds the clock in the data signal. Unlike the separate HDMI/DVI and LVDS standards, DisplayPort supports both external (monitor) or internal (LCD panel) display connections.

### 5.1.1 DP Example Schematics

See the following page.

**Port B: Display Port**

**Set DDI output via strapping option**

**Inverter for hot-plug detection signal**

Jumper 1-2: Set Hot Plug HIGH active
Jumper 2-3: Set Hot Plug LOW active

**Display Port Connector**

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Title: Display Port Ref. Schematic

| Size | Document Number | Created | Rev |
|------|-----------------|---------|-----|
| B | <Doc> | <OrgAddr4> | X.0 |

Date: Monday, September 20, 2010   Sheet

## 5.1.2    DisplayPort Hot-plug Detection

Refer to the description in the section 3.1.4  of this document

## 5.1.3    Enable DisplayPort Support

To enable the DisplayPort support, the control data lines of the respective Graphics Port B, Port C or Port D (DDPx_CTRLDATA - see Table 1) must be pulled to +3.3V by a 2.2kOhm resistor.

Additionally, a BIOS setup configuration is necessary to enable the DisplayPort interface. The setup nodes shown below (located in the Graphics Configuration Submenu within the congatec BIOS Setup Program) have to be set to 'DisplayPort Port' for the respective port (Port B or C).

**Table 6 BIOS Graphics Configuration Submenu conga-BM45, conga-BS45 and conga-CS45:**

| Feature | Options | Description |
| --- | --- | --- |
| SDVO Port B Configuration | Disabled<br>HDMI Port<br>**Display Port**<br>SDVO DVI (default setting)<br>…....... | Select the SDVO device connected to this SDVO port or configure the port as HDMI or Display Port. |
| SDVO Port C Configuration | Disabled<br>HDMI Port<br>**Display Port**<br>SDVO DVI (default setting)<br>…....... | Select the SDVO device connected to this SDVO port or configure the port as HDMI or Display Port. |

### conga-Bx57, conga-Bx67 and conga-BS77

| Feature | Options | Description |
|---|---|---|
| Display Port B Interface | Disabled (default setting)<br>SDVO<br>**Display Port**<br>HDMI/DVI | Select the interface the physical display port should offer. |
| Display Port C Interface | Disabled (default setting)<br>**Display Port**<br>HDMI/DVI | Select the interface the physical display port should offer. |
| Display Port D Interface | Disabled (default setting)<br>**Display Port**<br>HDMI/DVI | Select the interface the physical display port should offer. |

### conga-CCA

| Feature | Options | Description |
|---|---|---|
| DDI Port B | Disabled<br>**Display Port**<br>HDMI/DVI | Select the Digital Display Interface offered by the Graphic Pipe B. |

### conga-BAF

| Feature | Options | Description |
|---|---|---|
| Display Channel 0 Output | **Display Port C**<br>HDMI C<br>LVDS<br>Disabled | Define output mode and connection of the integrated display channel 0.<br>This port can also be used for LVDS support provided by an on-board eDP to LVDS converter chip. |
| Display Channel 1 Output | **Display Port B**<br>HDMI B<br>Disabled | Define output mode and connection of the integrated display channel1. |

## 5.1.4    DisplayPort Connector Pinout
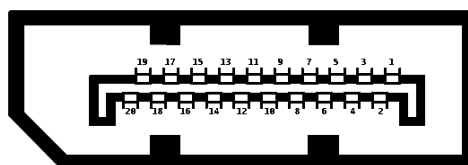
**Figure 5-1 DisplayPort Connector (male, front view)**



**Table 7 Pinout DisplayPort Connector**

| Pin# | Signal | Description | Pin# | Signal | Description |
|------|--------|-------------|------|--------|-------------|
| 1 | DP_LANE0+ | DisplayPort Lane 0 (positive) | 2 | GND | Ground |
| 3 | DP_LANE0- | DisplayPort Lane 0 (negative) | 4 | DP_LANE1+ | DisplayPort Lane 1 (positive) |
| 5 | GND | Ground | 6 | DP_LANE1- | DisplayPort Lane 1 (negative) |
| 7 | DP_LANE2+ | DisplayPort Lane 2 (positive) | 8 | GND | Ground |
| 9 | DP_LANE2- | DisplayPort Lane 2 (negative) | 10 | DP_LANE3+ | DisplayPort Lane 3 (positive) |
| 11 | GND | Ground | 12 | DP_LANE3- | DisplayPort Lane 3 (negative) |
| 13 | CONFIG1 | Configuration Pin 1 (connected to Ground) | 14 | CONFIG2 | Configuration Pin 2 (connected to Ground) |
| 15 | DP_AUX+ | Auxiliary Channel (positive) | 16 | GND | Ground |
| 17 | DP_AUX- | Auxiliary Channel (negative) | 18 | DP_HPD# | Hot Plug Detect |
| 19 | RETURN | Return For Power | 20 | DP_PWR | Power For Connector |

## 5.1.5    DisplayPort Hot-plug Detection

Refer to section 3.1.4  of this Application Note.

## 5.2   DisplayPort Audio

Refer to section 3.2  of this Application Note.

# 6    Layout Design Constraints

For HDMI, DVI or DisplayPort hardware design, congatec highly recommends complete adherence to the PCI Express Trace Routing Guidelines described in the PICMG COM Express™ (COM.0) Design Guide (http://www.picmg.org/).